



uCOM-TWL

SMARC Module

User's Manual 1st Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● uCOM-TWL	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
18. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

产品中有毒有害物质或元素名称及含量

AAEON 主板/子板/背板

QQ4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period))：10年

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

SMARC Module

UCOM-TWL

Name and content of hazardous substances in product

AAEON Main Board/Daughter Board/Backplane

QQ4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○

The table is prepared in accordance with the provisions of SJ/T 11364.

○: Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×: Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years

Notes: This product defined period of use is under normal condition.

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Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	SMARC Module
CPU	Intel® Core™ 3 Processor N355 (8C/8T, up to 3.9 GHz, 15W) Intel® Processor N150 (4C/4T, up to 3.6 GHz, 6W)
Chipset	Integrated with Intel® SoC
Memory	Onboard LPDDR5x 4800MHz, up to 8GB
Onboard Storage	eMMC, up to 128GB
BIOS	AMI UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Dimension (L x W)	3.23" x 1.97" (82mm x 50mm)
Security	TPM 2.0

Power

Power Requirement	+5V for ATX / AT
Power Type	AT (default)/ATX, switch by BIOS
Power Consumption (Typical)	Intel® Core™ i3-N305, 4.23A @+5V

Display

Graphics Controller	Intel® UHD Graphics
Video Output	Up to 3 Simultaneous Displays: DP++ x 2 / DP++ x 1 + HDMI x 1, up to 3840 x 2160 (by SKU) eDP x 1, up to 3840 x 2160

I/O

Ethernet	Intel® Ethernet Controller I226, 2.5GbE x 2
Audio	High Definition Audio Interface (Optional: I2S)
USB Port	USB 2.0 x 6 USB 3.2 x 2
Serial Port	2-Wire UART x 2 (Tx/Rx) 4-Wire UART x 2 (Tx/Rx/RTS/CTS)
HDD Interface	SATA 6Gb/s x 1
Expansion	PCIe 3.0 [x2] x 1 + [x1] x 2 (Optional: PCIe [x1] x 3) MIPI CSI x 2

Note: To get a fourth PCIe Gen 3 [x1] interface, please contact the AAEON support team

GPIO 7-bit (up to 14-bit by customization)

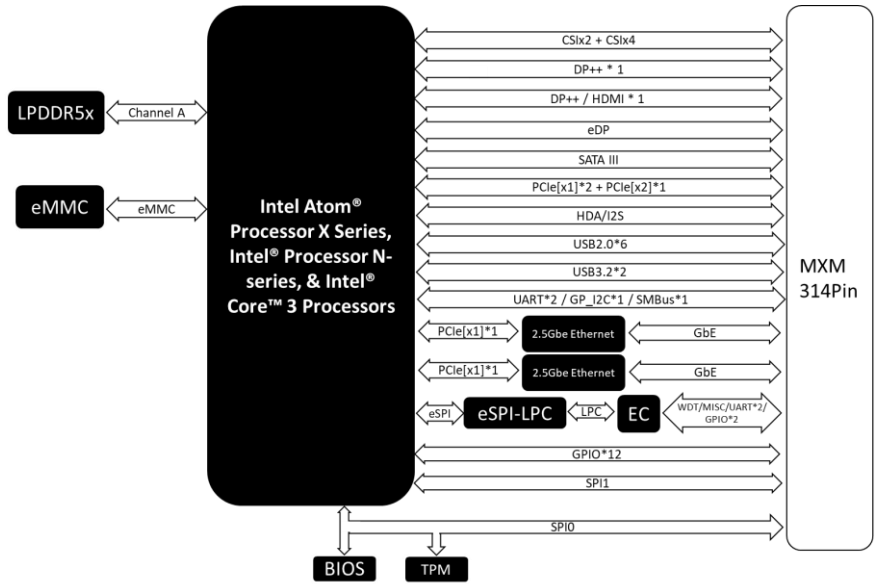
Note: Another 7-bit GPIO through multiplexed pins P108-P114 can be activated by custom BIOS. Please contact the AAEON support team

SMBus/I2C GP_I2C x 1
SMBus x 1

Environmental

Operating Temperature	-4°F – 158°F (-20°C – 70°C) Extended Temp: -40°F – 185°F (-40°C – 85°C)
Storage Temperature	-40°F – 185°F (-40°C – 85°C)
Operating Humidity	0% – 90% relative humidity, non-condensing
EMC	CE/FCC Class A
OS Support	Windows® 10 (64-bit) Windows 11® (64-bit) Linux Ubuntu 24.04/Kernel 6.11
Weight	0.14 lb (0.06 kg)

1.2 Block Diagram



Note 1: To get a fourth PCIe Gen 3 [x1] interface, please contact the AAEON support team.

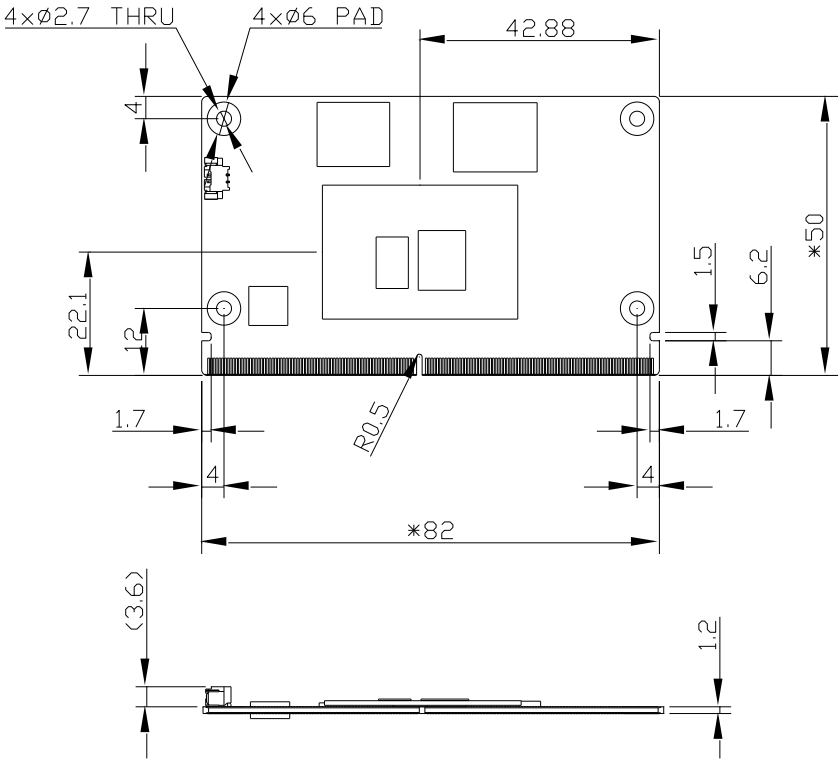
Note 2: MIPI CSI interface tested using Innodisk camera.

Chapter 2

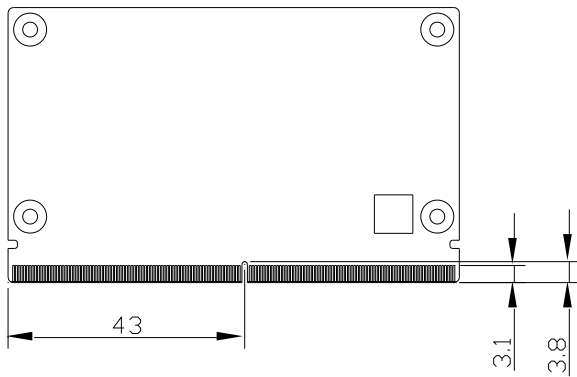
Hardware Information

2.1 Dimensions

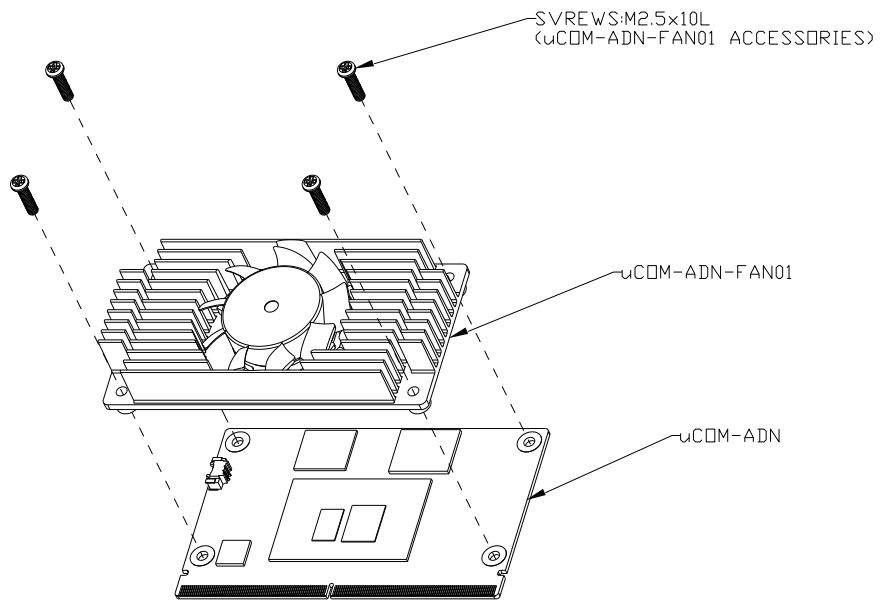
Top Side



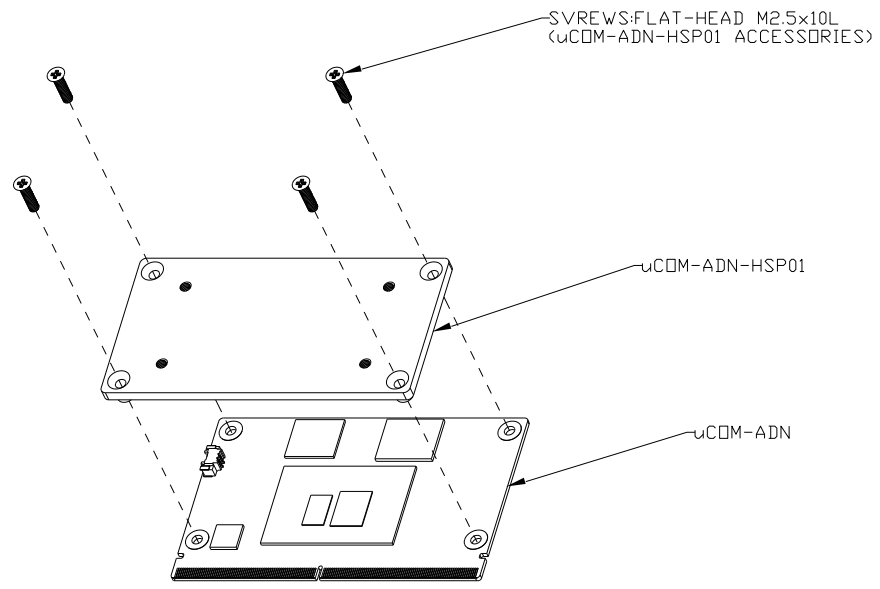
Bottom Side



With Active Cooling (Part No: uCOM-ADN-FAN01)

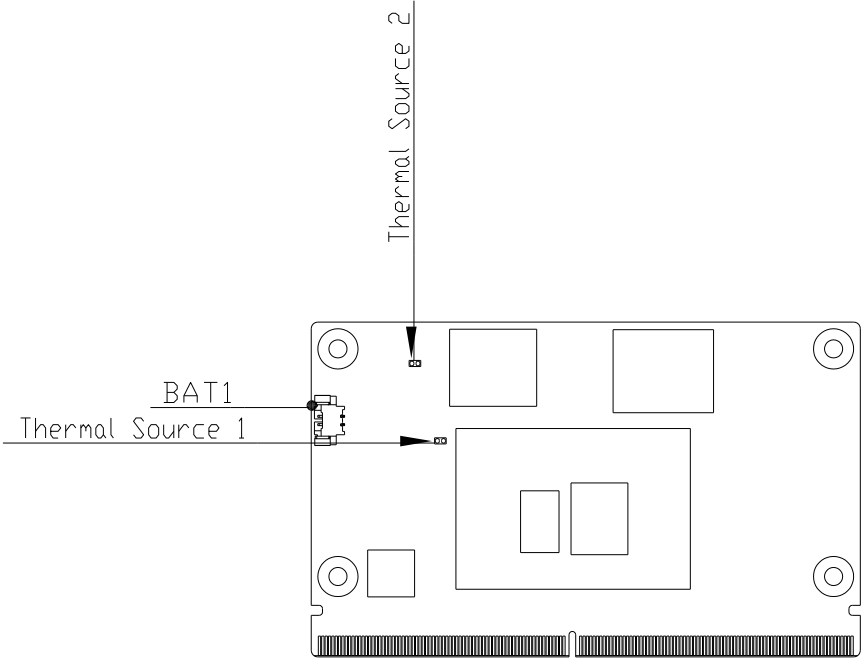


With Heatspreader (Part No: uCOM-ADN-HSP01)

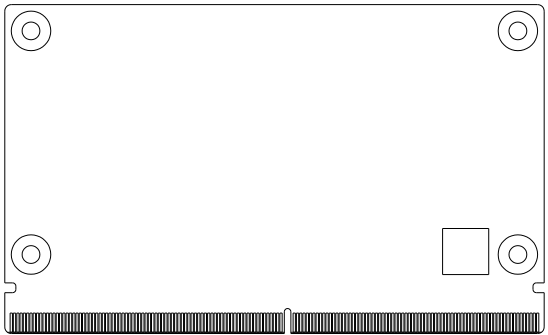


2.2 Jumpers and Connectors

Top Side



Bottom Side



2.3 Extra DC 5V Power in (BAT1)

Pin	Pin Name
1	+5V
2	GND

2.4 MXM Gold Finger (GF2)

Pin	Pin Name	Pin	Pin Name
P1	SMB_ALERT#	S1	CSI1_TX+/I2C_CAM1_CK
P2	GND	S2	CSI1_TX-/I2C_CAM1_DAT
P3	CSI1_CK+	S3	GND
P4	CSI1_CK-	S4	RSVD
P5	GBE1_SDP	S5	CSI0_TX+/I2C_CAM0_CK
P6	GBE0_SDP	S6	CAM_MCK
P7	CSI_B_DP_0	S7	CSI0_TX1/I2C_CAM0_DAT
P8	CSI_B_DN_0	S8	CSI0_CK+
P9	GND	S9	CSI0_CK-
P10	CSI_B_DP_1	S10	GND
P11	CSI_B_DN_1	S11	CSI_C_DP_0
P12	GND	S12	CSI_C_DN_0
P13	CSI_B_DP_2	S13	GND
P14	CSI_B_DN_2	S14	CSI_C_DP_1
P15	GND	S15	CSI_C_DN_1
P16	CSI_B_DP_3	S16	GND
P17	CSI_B_DN_3	S17	GBE1_MDIO+
P18	GND	S18	GBE1_MDIO-
P19	GBE0_MDIO-	S19	GBE1_LINK1000#
P20	GBE0_MDIO+	S20	GBE1_MDIO+
P21	GBE0_LINK1000#	S21	GBE1_MDIO-
P22	GBE0_LINK2500#	S22	GBE1_LINK2500#
P23	GBE0_MDIO-	S23	GBE1_MDIO+
P24	GBE0_MDIO+	S24	GBE1_MDIO-
P25	GBE0_LINK_ACT#	S25	GND
P26	GBE0_MDIO-	S26	GBE1_MDIO+
P27	GBE0_MDIO+	S27	GBE1_MDIO-
P28	GBE0_CTREF	S28	GBE1_CTREF
P29	GBE0_MDIO-	S29	PCIE_D_TX+/SERDES_0_TX+
P30	GBE0_MDIO+	S30	PCIE_D_TX-/SERDES_0_TX-

Pin	Pin Name	Pin	Pin Name
P31	SPI0_CS1#	S31	GBE1_LINK_ACT#
P32	GND	S32	PCIE_D_RX+/SERDES_0_RX+
P33	SDIO_WP	S33	PCIE_D_RX-/SERDES_0_RX-
P34	SDIO_CMD	S34	GND
P35	SDIO_CD#	S35	USB4+
P36	SDIO_CK	S36	USB4-
P37	SDIO_PWR_EN	S37	USB3_VBUS_DET
P38	GND	S38	AUDIO_MCK
P39	SDIO_D0	S39	I2S0_LRCK
P40	SDIO_D1	S40	I2S0_SDOUT
P41	SDIO_D2	S41	I2S0_SDIN
P42	SDIO_D3	S42	I2S0_CK
P43	SPI0_CS0#	S43	ESPI_ALERT0#
P44	SPI0_CK	S44	ESPI_ALERT1#
P45	SPI0_DIN	S45	MDIO_CLK
P46	SPI0_DO	S46	MDIO_DAT
P47	GND	S47	GND
P48	SATA_TX+	S48	I2C_GP_CK
P49	SATA_TX-	S49	I2C_GP_DAT
P50	GND	S50	HDA_SYNC/I2S2_LRCK
P51	SATA_RX+	S51	HDA_SDO/I2S2_SDOUT
P52	SATA_RX-	S52	HDA_SDI/I2S2_SDIN/
P53	GND	S53	HDA_CK/I2S2_CK
P54	ESPI_CS0#/SPI1_CS0#/QSPI_CS0#	S54	SATA_ACT#
P55	ESPI_CS1#/SPI1_CS1#/QSPI_CS1#	S55	USB5_EN_OC#
P56	ESPI_CK/SPI1_CK/QSPI_CK	S56	ESPI_IO_2/QSPI_IO_2
P57	ESPI_IO_1/SPI1_DIN/QSPI_IO_1	S57	ESPI_IO_3/QSPI_IO_3
P58	ESPI_IO_0/SPI1_DO/QSPI_IO_0	S58	ESPI_RESET#
P59	GND	S59	USB5+
P60	USB0+	S60	USB5-
P61	USB0-	S61	GND
P62	USB0_EN_OC#	S62	USB3_SSTX+
P63	USB0_VBUS_DET	S63	USB3_SSTX-
P64	USB0_OTG_ID	S64	GND
P65	USB1+	S65	USB3_SSRX+
P66	USB1-	S66	USB3_SSRX-
P67	USB1_EN_OC#	S67	GND
P68	GND	S68	USB3+
P69	USB2+	S69	USB3-

Pin	Pin Name	Pin	Pin Name
P70	USB2-	S70	GND
P71	USB2_EN_OC#	S71	USB2_SSTX+
P72	RSVD	S72	USB2_SSTX-
P73	RSVD	S73	GND
P74	USB3_EN_OC#	S74	USB2_SSRX+
P75	PCIE_A_RST#	S75	USB2_SSRX-
P76	USB4_EN_OC#	S76	PCIE_B_RST#
P77	PCIE_B_CLKREQ#	S77	PCIE_C_RST#
P78	PCIE_A_CLKREQ#	S78	PCIE_C_RX+/SERDES_1_RX+
P79	GND	S79	PCIE_C_RX-/SERDES_1_RX-
P80	PCIE_C_REFCK+	S80	GND
P81	PCIE_C_REFCK-	S81	PCIE_C_TX+/SERDES_1_TX+
P82	GND	S82	PCIE_C_TX-/SERDES_1_TX-
P83	PCIE_A_REFCK+	S83	GND
P84	PCIE_A_REFCK-	S84	PCIE_B_REFCK+
P85	GND	S85	PCIE_B_REFCK-
P86	PCIE_A_RX+	S86	GND
P87	PCIE_A_RX-	S87	PCIE_B_RX+
P88	GND	S88	PCIE_B_RX-
P89	PCIE_A_TX+	S89	GND
P90	PCIE_A_TX-	S90	PCIE_B_TX+
P91	GND	S91	PCIE_B_TX-
P92	HDMI_D2+/DP1_LANE0+	S92	GND
P93	HDMI_D2-/DP1_LANE0-	S93	DP0_LANE0+
P94	GND	S94	DP0_LANE0-
P95	HDMI_D1+/DP1_LANE1+	S95	DP0_AUX_SEL
P96	HDMI_D1-/DP1_LANE1-	S96	DP0_LANE1+
P97	GND	S97	DP0_LANE1-
P98	HDMI_D0+/DP1_LANE2+	S98	DP0_HPDP
P99	HDMI_D0-/DP1_LANE2-	S99	DP0_LANE2+
P100	GND	S100	DP0_LANE2-
P101	HDMI_CK+/DP1_LANE3+	S101	GND
P102	HDMI_CK-/DP1_LANE3-	S102	DP0_LANE3+
P103	GND	S103	DP0_LANE3-
P104	HDMI_HPDP/DP1_HDP	S104	USB3_OTG_ID
P105	HDMI_CTRL_CK/DP1_AUX+	S105	DP0_AUX+
P106	HDMI_CTRL_DAT/DP1_AUX-	S106	DP0_AUX-
P107	DP1_AUX_SEL	S107	LCD1_BKLT_EN

Pin	Pin Name	Pin	Pin Name
P108	GPIO0/CAM0_PWR#	S108	LVDS1_CK+/eDP1_AUX+/DSI1_C LK+
P109	GPIO1/CAM1_PWR#	S109	LVDS1_CK-/eDP1_AUX-/DSI1_C LK-
P110	GPIO2/CAM0_RST#	S110	GND
P111	GPIO3/CAM1_RST#	S111	LVDS1_0+/eDP1_TX0+/DSI1_D0+
P112	GPIO4/HDA_RST#	S112	LVDS1_0-/eDP1_TX0-/DSI1_D0-
P113	GPIO5/PWM_OUT	S113	eDP1_HPD/DSI1_TE
P114	GPIO6/TACHIN	S114	LVDS1_1+/eDP1_TX1+/DSI1_D1+
P115	GPIO7	S115	LVDS1_1-/eDP1_TX1-/DSI1_D1-
P116	GPIO8	S116	LCD1_VDD_EN
P117	GPIO9	S117	LVDS1_2+/eDP1_TX2+/DSI1_D2+
P118	GPIO10	S118	LVDS1_2-/eDP1_TX2-/DSI1_D2-
P119	GPIO11	S119	GND
P120	GND	S120	LVDS1_3+/eDP1_TX3+/DSI1_D3+
P121	I2C_PM_CK	S121	LVDS1_3-/eDP1_TX3-/DSI1_D3-
P122	I2C_PM_DAT	S122	LCD1_BKLT_PWM
P123	BOOT_SEL0#	S123	GPIO13
P124	BOOT_SEL1#	S124	GND
P125	BOOT_SEL2#	S125	LVDS0_0+/eDP0_TX0+/DSI0_D0+
P126	RESET_OUT#	S126	LVDS0_0-/eDP0_TX0-/DSI0_D0-
P127	RESET_IN#	S127	LCD0_BKLT_EN
P128	POWER_BTN#	S128	LVDS0_1+/eDP0_TX1+/DSI0_D1+
P129	SER0_TX	S129	LVDS0_1-/eDP0_TX1-/DSI0_D1-
P130	SER0_RX	S130	GND
P131	SER0_RTS#	S131	LVDS0_2+/eDP0_TX2+/DSI0_D2+
P132	SER0_CTS#	S132	LVDS0_2-/eDP0_TX2-/DSI0_D2-
P133	GND	S133	LCD0_VDD_EN
P134	SER1_TX	S134	LVDS0_CK+/eDP0_AUX+/DSI0_C LK+
P135	SER1_RX	S135	LVDS0_CK-/eDP0_AUX-/DSI0_C LK-
P136	SER2_TX	S136	GND
P137	SER2_RX	S137	LVDS0_3+/eDP0_TX3+/DSI0_D3+
P138	SER2_RTS#	S138	LVDS0_3-/eDP0_TX3-/DSI0_D3-
P139	SER2_CTS#	S139	I2C_LCD_CK
P140	SER3_TX	S140	I2C_LCD_DAT

Pin	Pin Name	Pin	Pin Name
P141	SER3_RX	S141	LCD0_BKLT_PWM
P142	GND	S142	GPIO12
P143	CAN0_TX	S143	GND
P144	CAN0_RX	S144	eDP0_HPD/DSIO_TE
P145	CAN1_TX	S145	WDT_TIME_OUT#
P146	CAN1_RX	S146	PCIE_WAKE#
P147	VDD_IN	S147	VDD_RTC
P148	VDD_IN	S148	LID#
P149	VDD_IN	S149	SLEEP#
P150	VDD_IN	S150	VIN_PWR_BAD#
P151	VDD_IN	S151	CHARGING#
P152	VDD_IN	S152	CHARGER_PRSNT#
P153	VDD_IN	S153	CARRIER_STBY#
P154	VDD_IN	S154	CARRIER_PWR_ON
P155	VDD_IN	S155	FORCE_RECOV#
P156	VDD_IN	S156	BATLOW#
		S157	TEST#
		S158	GND

Note: Bold: Default function.

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The module uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

- You are starting your system for the first time.
- You have changed the hardware attached to your system.
- The system configuration is reset by Clear-CMOS jumper
- The CMOS memory has lost power and the configuration information has been erased.

The uCOM-TWL CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off.

To enter Setup, power on the computer and press immediately.

The function of each menu is as follows:

Main – Date and time can be set here. Use <Tab> to switch between date elements.

Advanced – Enable/disable boot option for legacy network devices.

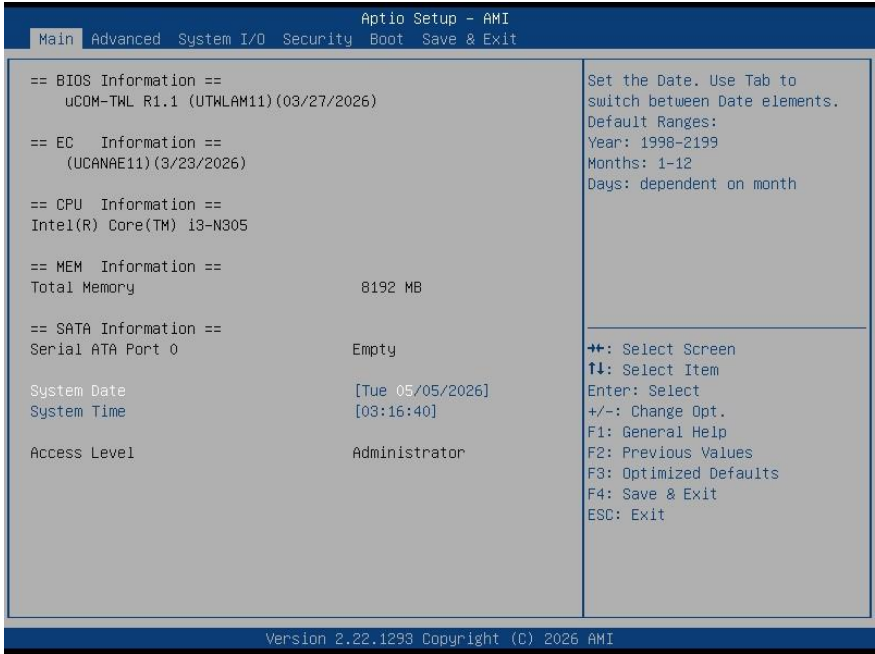
System I/O – For hosting bridge parameters.

Security – Password for setup administrator can be set here.

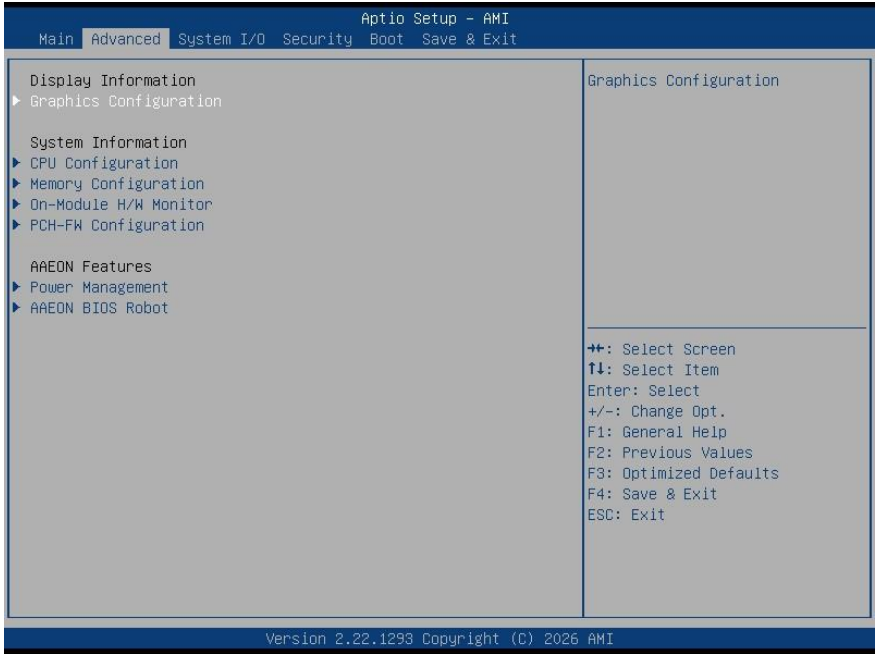
Boot – Enable/disable Quiet Boot option.

Save & Exit – Save changes and exit Setup.

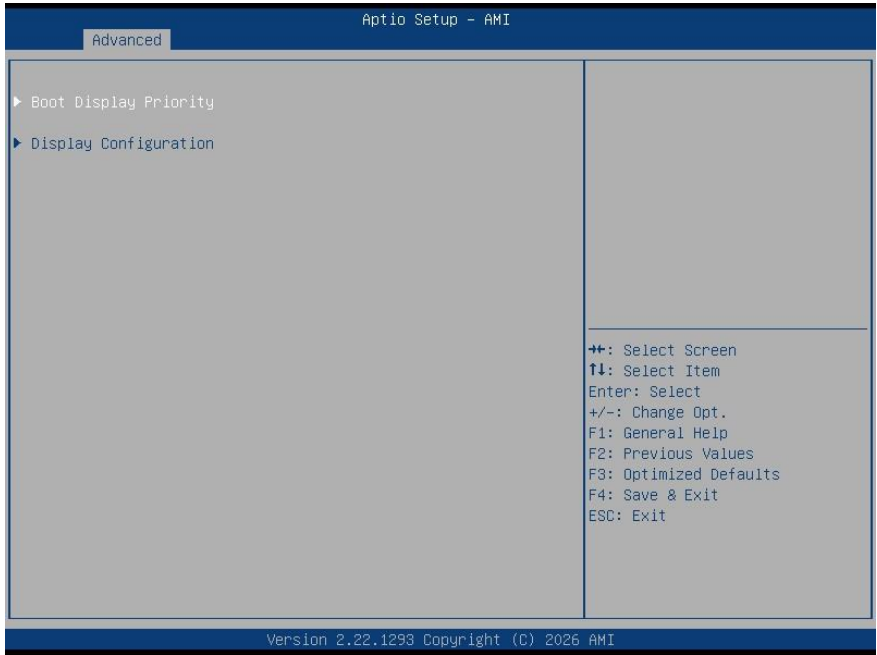
3.3 Setup Submenu: Main



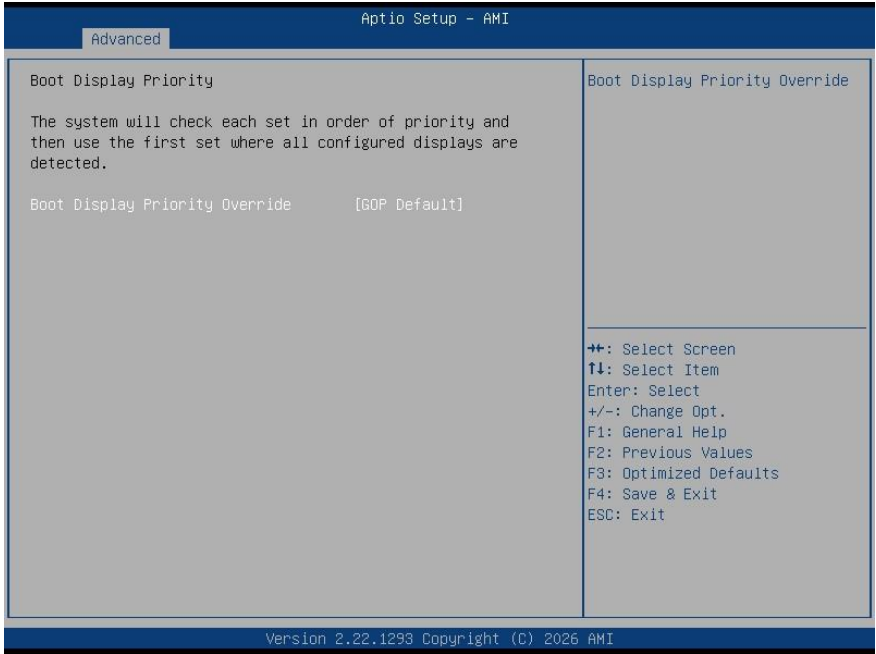
3.4 Setup Submenu: Advanced



3.4.1 Graphics Configuration

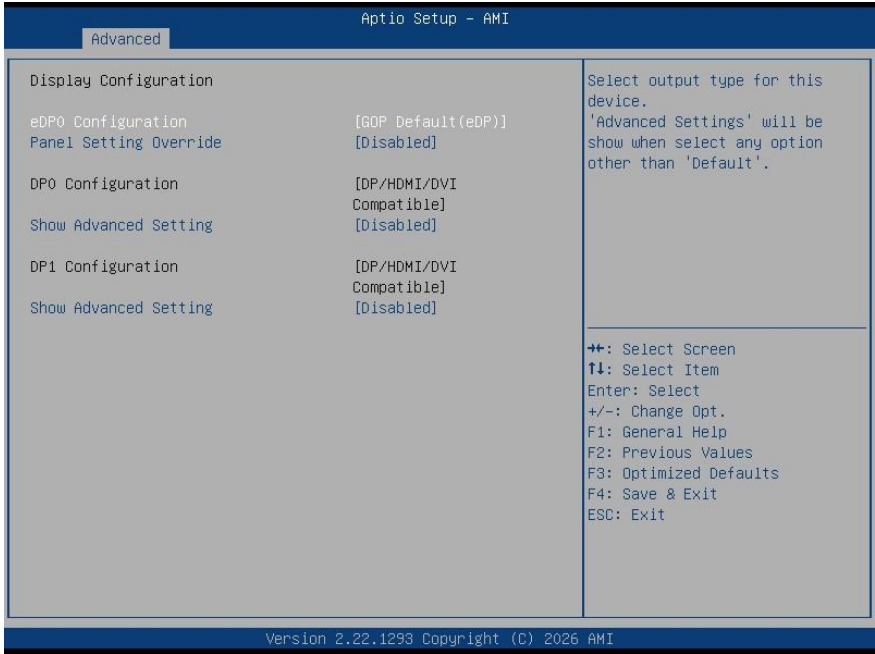


3.4.2 Boot Display Priority



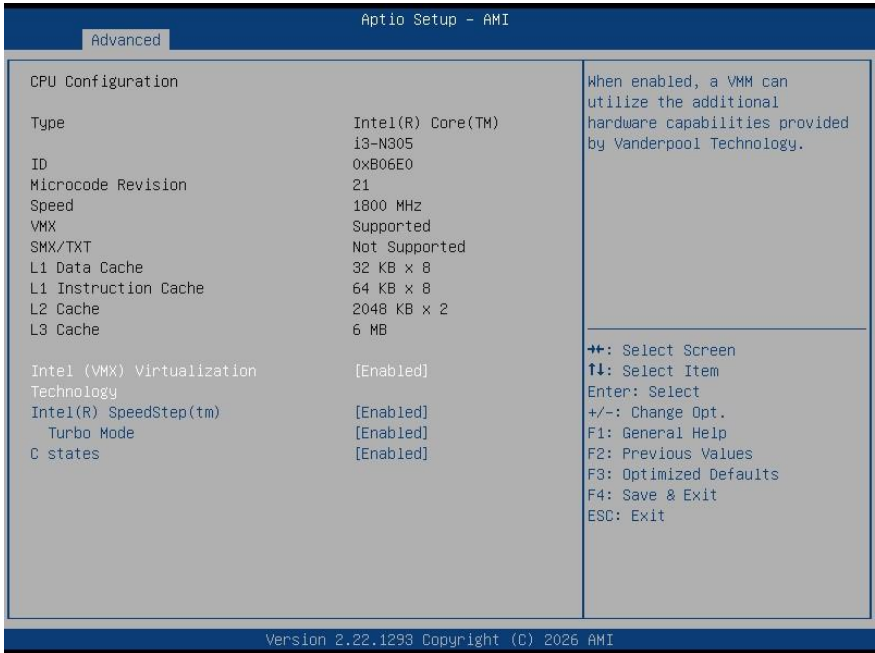
Options Summary		
Boot Display Priority	Enabled	
Override	GOP Default	Optimal Default, Failsafe Default
Boot Display Priority Override.		

3.4.2.1 Display Configuration



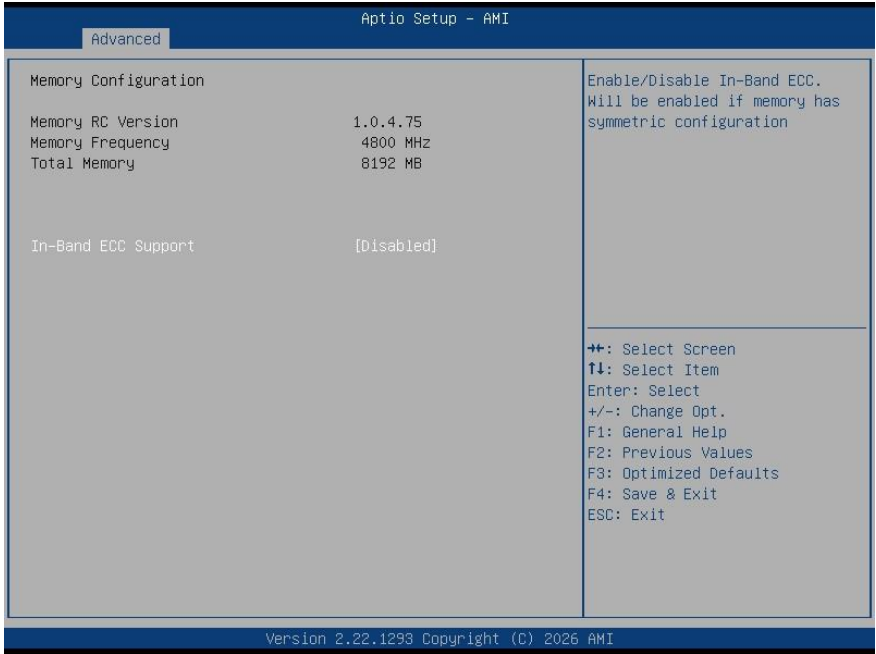
Options Summary		
eDP0 Configuration	GOP Default(eDP)	Optimal Default, Failsafe Default
	No Device (Disable)	
Select the output type for this device. The Advanced Settings menu will appear when any option other than Default is selected.		
Panel Setting Override	Enabled	
	Disabled	Optimal Default, Failsafe Default
Panel Setting Override.		
DP0 Configuration	DP/HDMI/DVI	Optimal Default, Failsafe Default
	Compatible	
Select output type for this device.		
DP1 Configuration	DP/HDMI/DVI	According to HW SKU
	Compatible	
	HDMI/DVI	According to HW SKU
Select output type for this device.		

3.4.3 CPU Configuration



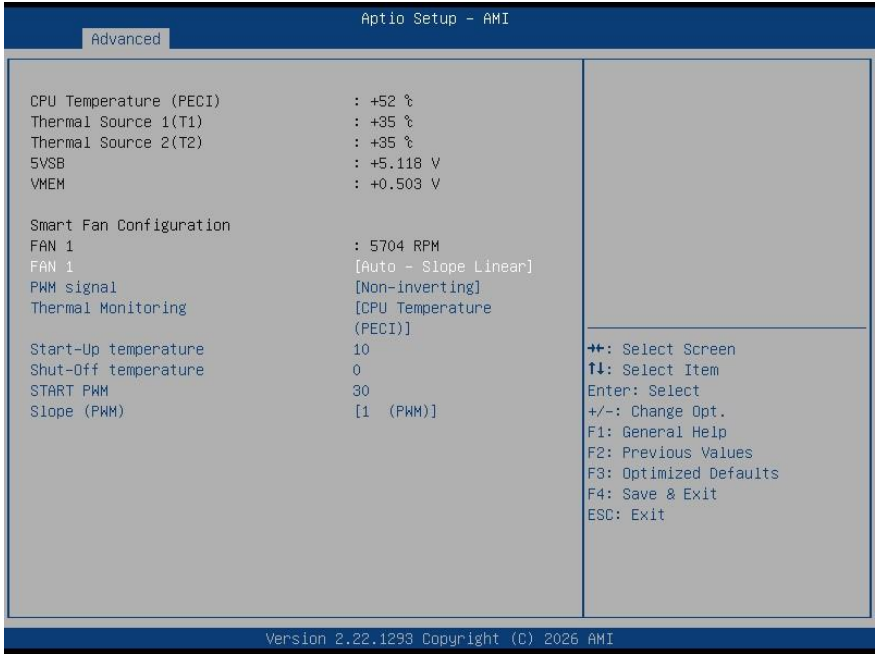
Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel® SpeedStep™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode.		
C states	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.		

3.4.4 Memory Configuration



Options Summary		
In-Band ECC Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable In-Band ECC. Will be enabled if memory has symmetric configuration.		

3.4.5 On-Module H/W Monitor



Options Summary		
Smart Fan	Full Mode	
	Manual Mode	
	Auto – Slope Linear	Optimal Default, Failsafe Default
Fan Mode select.		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal.		
Thermal Monitoring	CPU Temperature (PECI)	Optimal Default, Failsafe Default
	Thermal Source 1 (T1)	
	Thermal Source 2 (T2)	
Monitoring thermal sensor select.		
Start-Up temperature	10	
PWM output when monitoring thermal sensor is exceeded.		
Range: 0 - 100		
Shut-Off temperature	0	

Options Summary

PWM turns off when monitored thermal sensor is less or equal to.
Range: 0 – 100

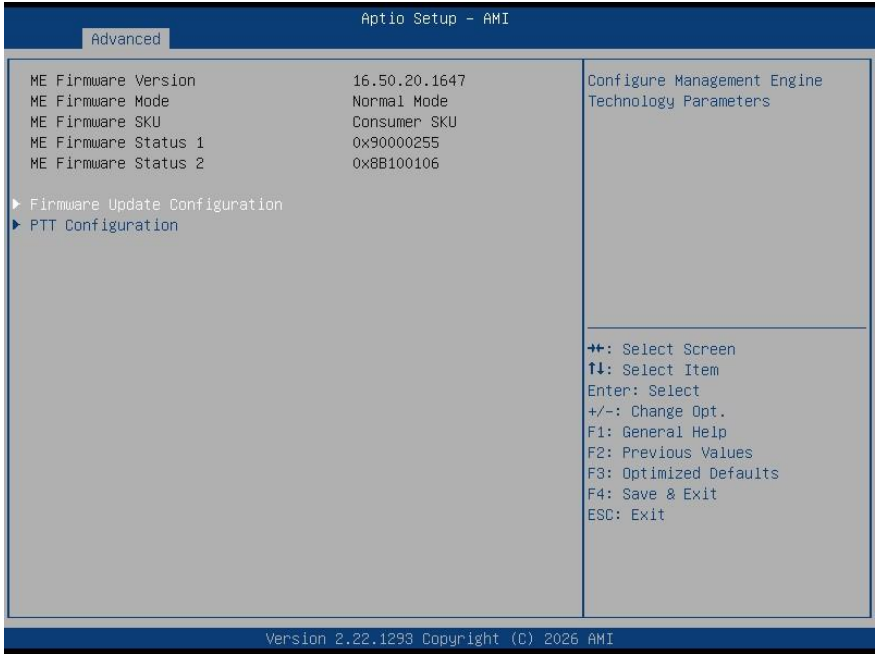
START PWM	30
------------------	----

The beginning PWM output value when Start-Up temperature is triggered.

Slope (PWM)	0 (PWM)	
	1 (PWM)	Optimal Default, Failsafe Default
	2 (PWM)	
	4 (PWM)	
	8 (PWM)	
	16 (PWM)	
	32 (PWM)	
	64 (PWM)	

When the monitored temperature is higher than the Start-Up temperature, the PWM output increases per degree.

3.4.6 PCH-FW Configuration



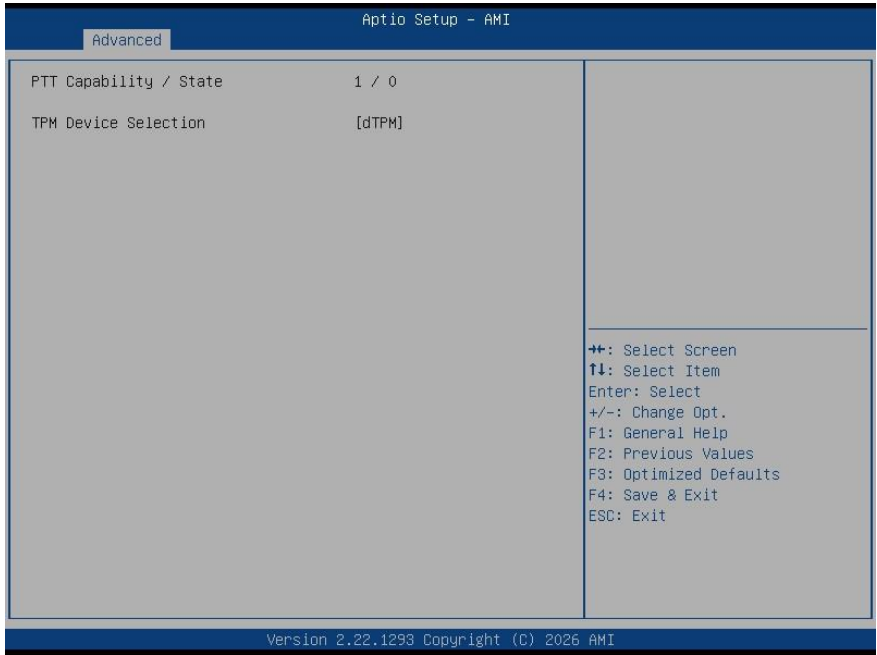
Options Summary		
TPM Device Selection	dTPM	Optimal Default, Failsafe Default
	PTT	
<p>Select the TPM device to use: PTT or dTPM.</p> <p>PTT – Enables Intel® Platform Trust Technology (PTT) in SkuMgr. dTPM 1.2 – Disables PTT in SkuMgr and uses a discrete TPM 1.2 device.</p> <p>Warning: Switching between PTT and dTPM will disable the currently active TPM device, and all data stored in it will be lost.</p>		

3.4.6.1 Firmware Update Configuration

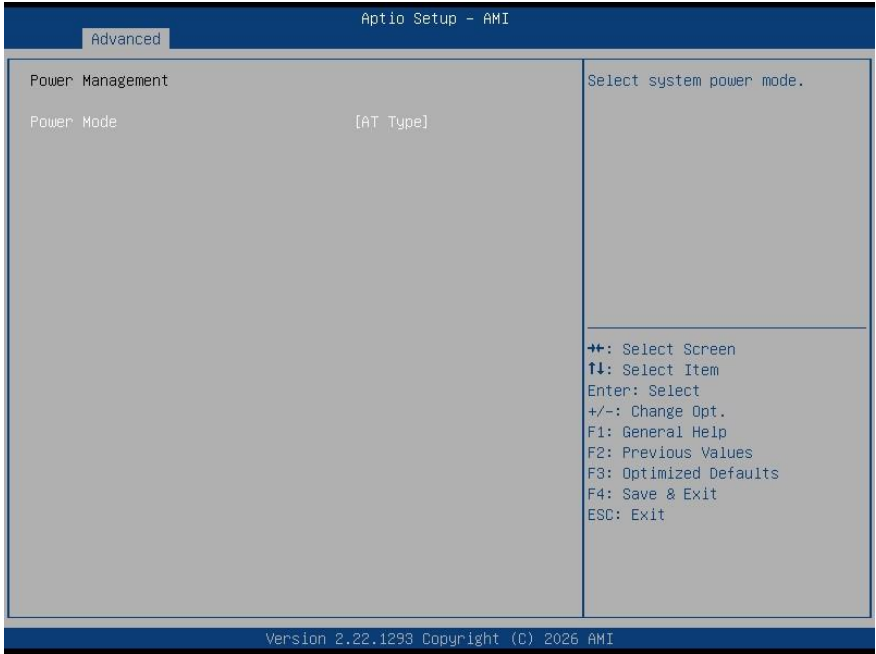


Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable the ME firmware image re-flash function.		

3.4.6.2 PTT Configuration

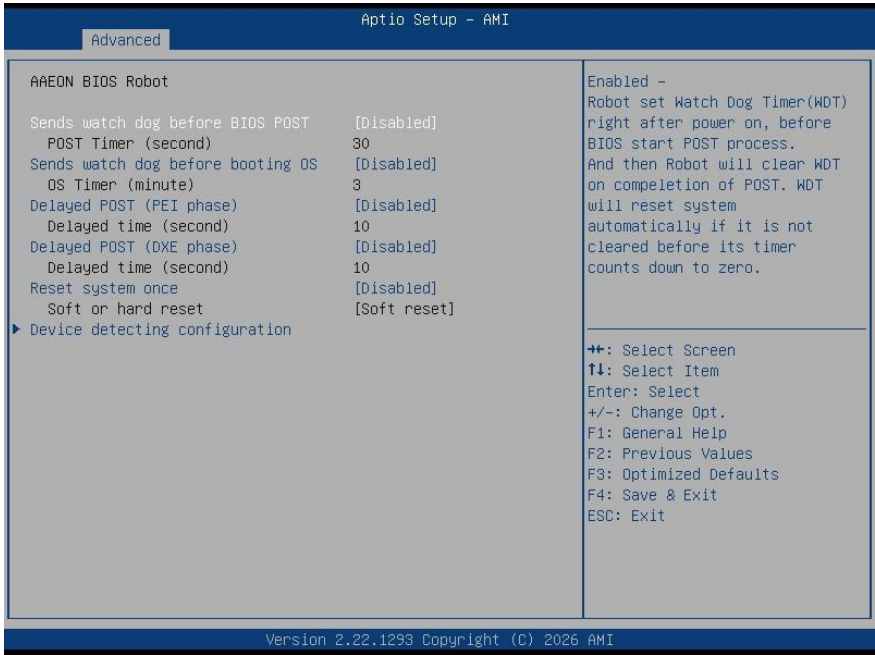


3.4.7 Power Management



Options Summary		
Power Mode	ATX Type	
	AT Type	Optimal Default, Failsafe Default
Select system power mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
Restore AC Power Loss.		
Soft-Off (S5) Wake On RTC	Disabled	Optimal Default, Failsafe Default
	By Date	
	By Weekday	
	Bypass	
By Date: System will wake on the day with hr::min::sec specified.		
By Weekday: System will wake on the enabled weekday with hr::min::sec specified.		
Bypass: BIOS will not control RTC wake function.		

3.4.8 AAEON BIOS Robot



Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
<p>Enabled – The robot sets the Watch Dog Timer (WDT) immediately after power-on, before the BIOS begins the POST process. The robot clears the WDT after POST is completed. If the WDT is not cleared before the timer expires, the system will automatically reset.</p>		
POST Timer (second)	30	Optimal Default, Failsafe Default
<p>Set the timer count for the Watch Dog Timer (WDT) during POST.</p> <p>Warning: Do not set the timer value equal to or shorter than the normal POST time. Otherwise, the system may continuously reset and fail to complete POST unless the BIOS settings are cleared. It is recommended to set the value to more than twice the normal POST time.</p>		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	

Options Summary

Enabled – The robot sets the Watch Dog Timer (WDT) after POST completion, before the BIOS transfers control to the operating system.

Warning: Before enabling this function, an OS-level program must be responsible for clearing the WDT. This function should be disabled if the operating system is performing an update.

OS Timer (minute)	3	Optimal Default, Failsafe Default
-------------------	---	-----------------------------------

Timer count set to Watch Dog Timer for OS loading.

Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	

Enabled – The robot delays BIOS from starting POST immediately after power-on. This allows the POST process to begin with stable power or after the system has physically warmed up.

Note: This delay occurs before the Watch Dog Timer is set.

Delayed time (second)	10	Optimal Default, Failsafe Default
-----------------------	----	-----------------------------------

Period of time for Robot to hold BIOS from POST.

Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	

Enabled – The robot holds the BIOS before POST completion. This ensures that the POST process completes under stable power or after the system has physically warmed up.

Note: This hold occurs after the Watch Dog Timer is set but before POST finishes.

Delayed time (second)	10	Optimal Default, Failsafe Default
-----------------------	----	-----------------------------------

Period of time for Robot to hold BIOS from POST.

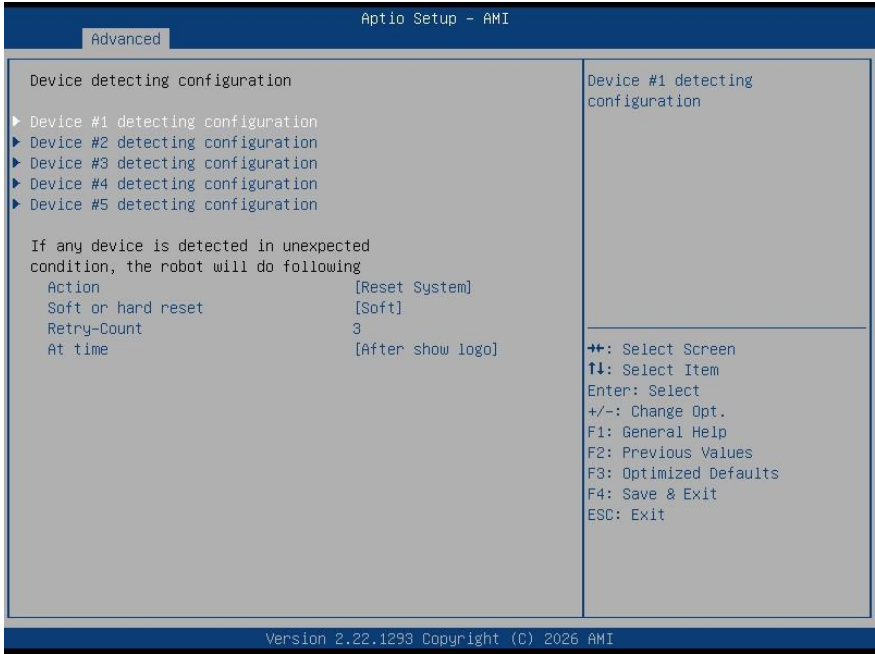
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	

Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.

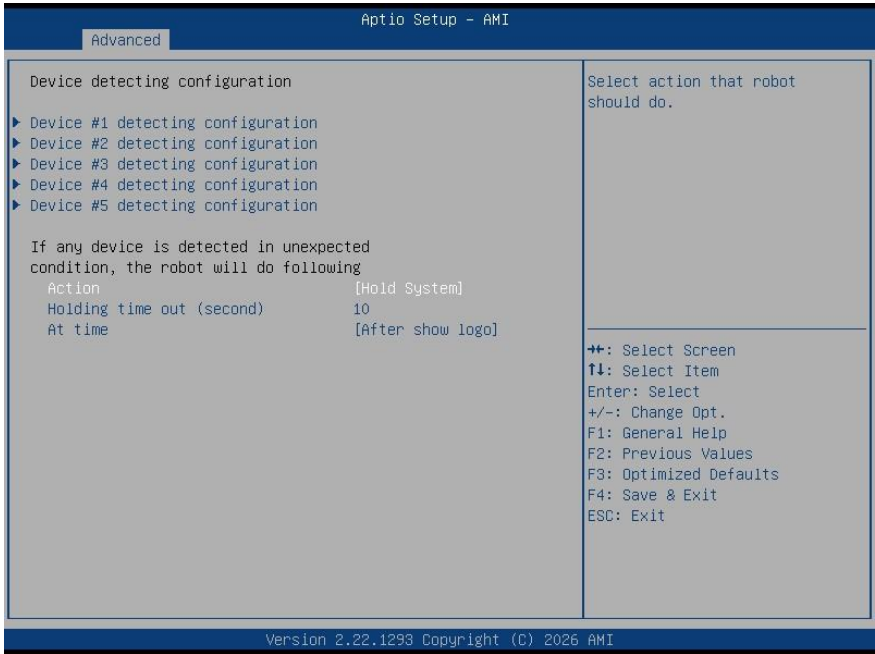
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset"	

Select reset type robot should send on each boot.

3.4.8.1 Device Detecting Configuration



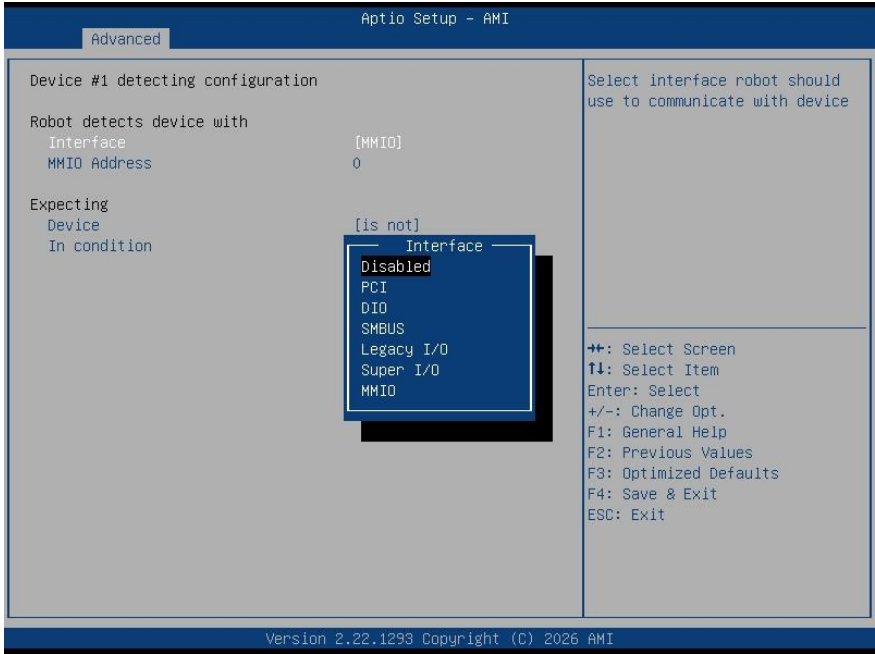
Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do action after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		



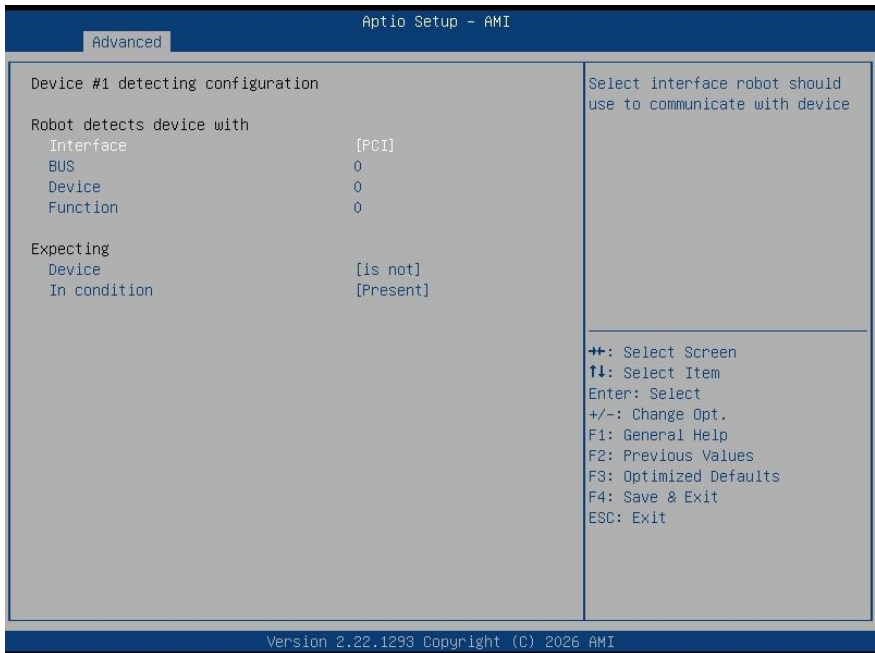
Options Summary

Action	Reset System	
	Hold System	Optimal Default, Failsafe Default
Select action that robot should do.		
Holding time out (second)	10	Optimal Default, Failsafe Default
Fill hold time out here. Robot will hold system no longer than time-out value, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do action after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

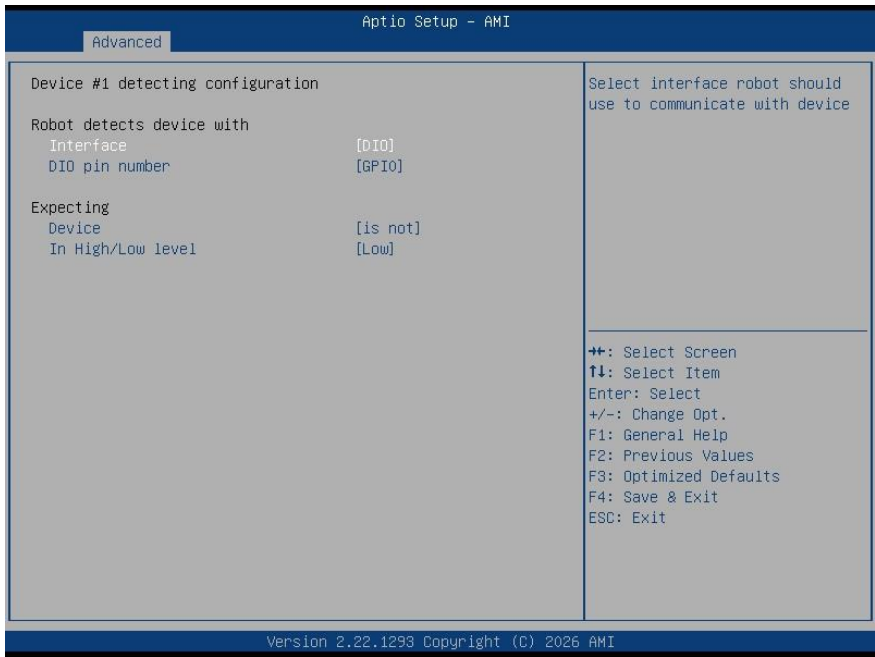
3.4.8.2 Device #* Detecting Configuration



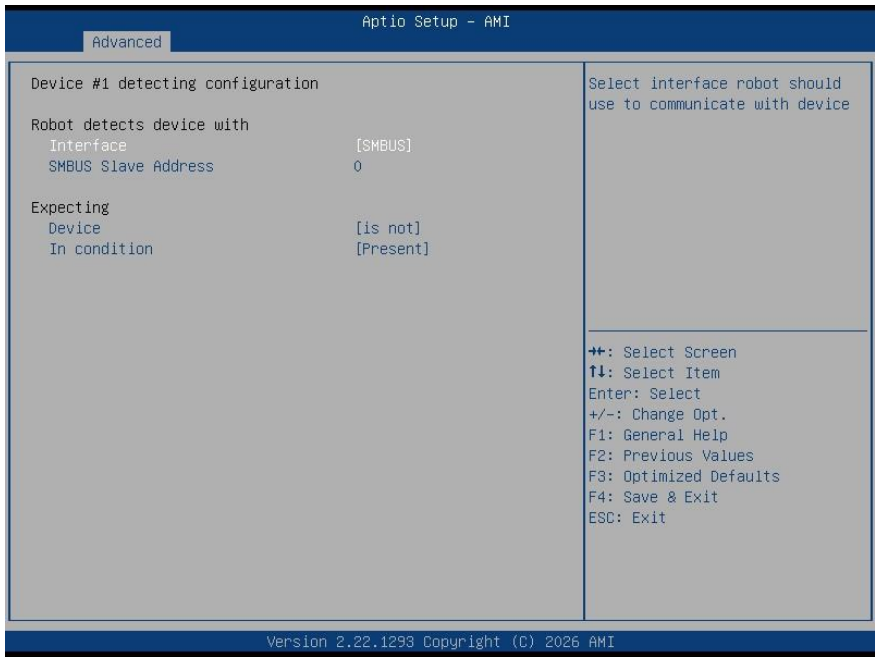
Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		



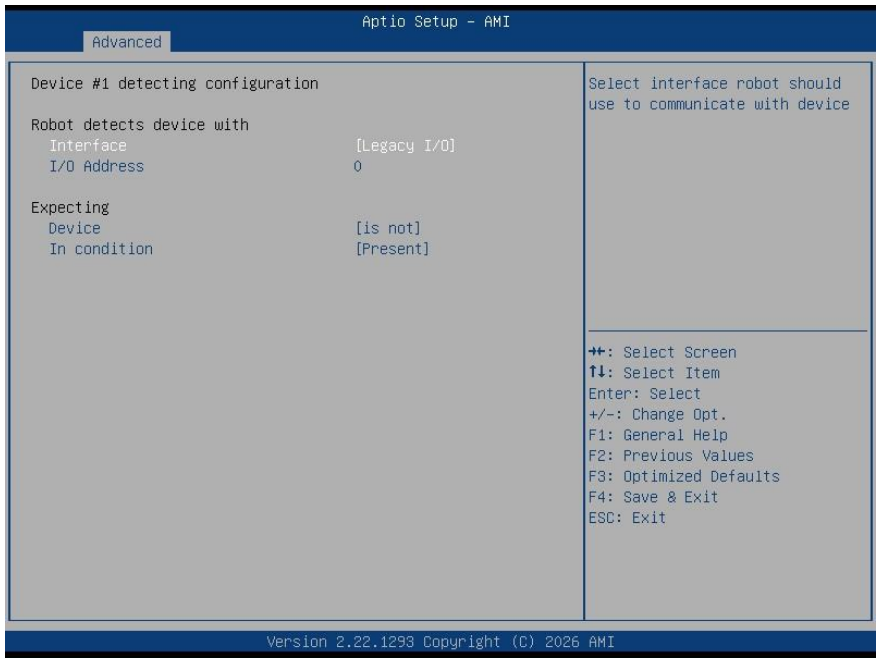
Interface item set to "PCI"		
Options Summary		
BUS	0	Optimal Default, Failsafe Default
Fill BUS number to a PCI device, in hexadecimal. Range: 0 – FF.		
Device	0	Optimal Default, Failsafe Default
Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 – FF.		
Function	0	Optimal Default, Failsafe Default
Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 – FF.		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected. According to register - Robot read register according to configuration.		
Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		



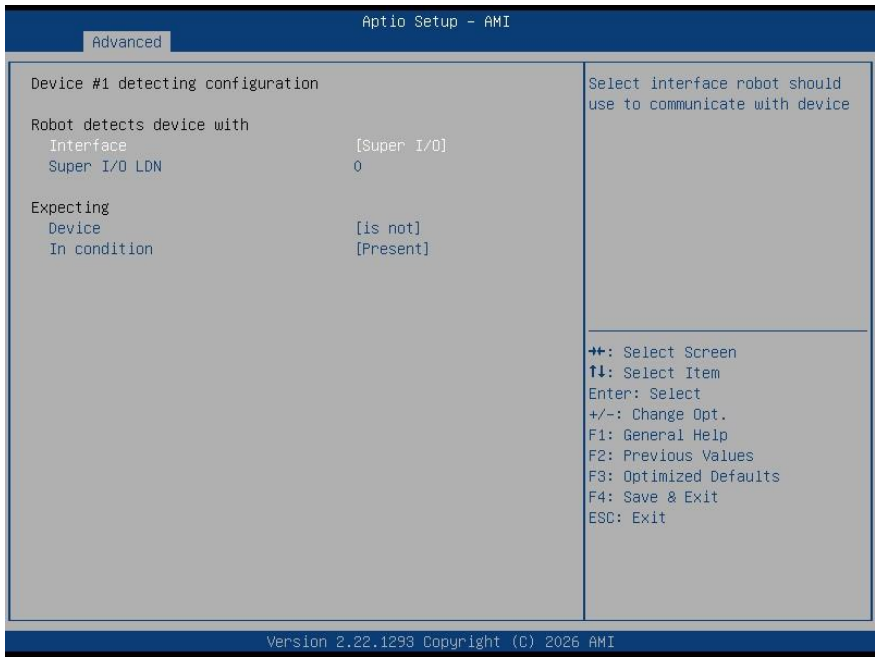
Interface item set to "DIO"		
Options Summary		
DIO pin number	GPIO 0	Optimal Default, Failsafe Default
	GPIO *	
Fill DIO pin number, 0 - DIO, 1 - DIO1, and so on. For COM express product: 0-3 - GPIO-3 4-7 - GPO0-3		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In High/Low level	Low	Optimal Default, Failsafe Default
	High	
Select High/Low level of the DIO pin that robot should perform action.		



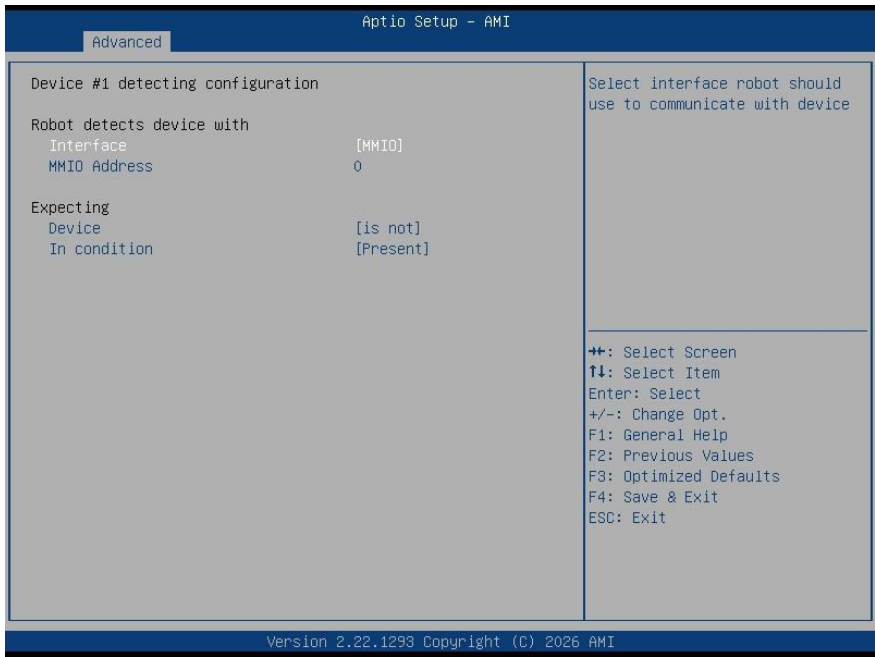
Interface item set to "SMBUS"		
Options Summary		
SMBUS Slave Address	0	Optimal Default, Failsafe Default
Fill slave address to a SMBUS device, in hexadecimal. Range: 0 – FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration.		
Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		



Interface item set to "Legacy I/O"		
Options Summary		
I/O Address	0	Optimal Default, Failsafe Default
Fill I/O address device is responding to. Range: 0~FFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected. According to register - Robot read register according to configuration.		
Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

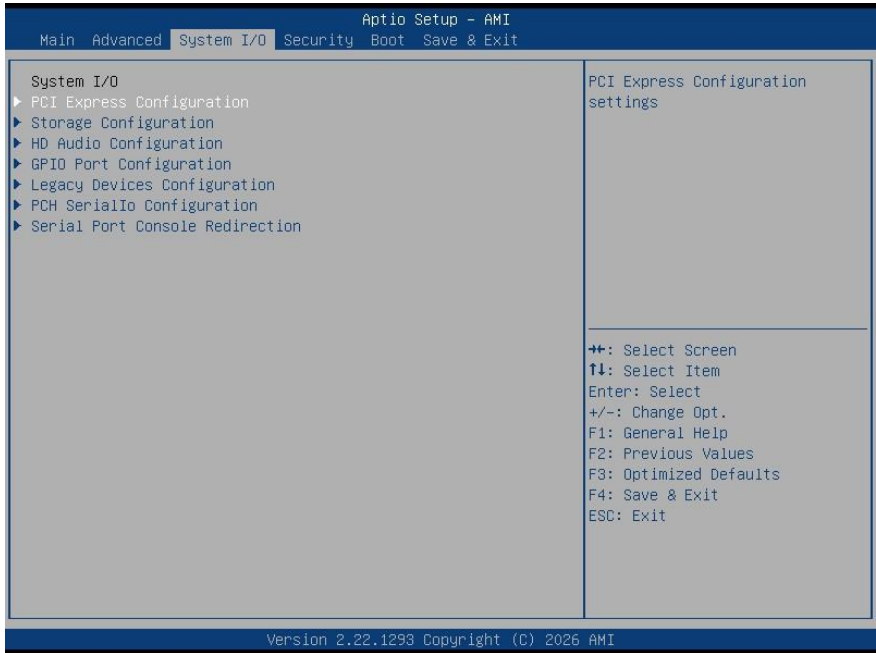


Interface item set to "Super I/O"		
Options Summary		
Super I/O LDN	0	Optimal Default, Failsafe Default
Fill LDN number to a Super I/O device. Range: 0~FF.		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected. According to register - Robot read register according to configuration.		
Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF		

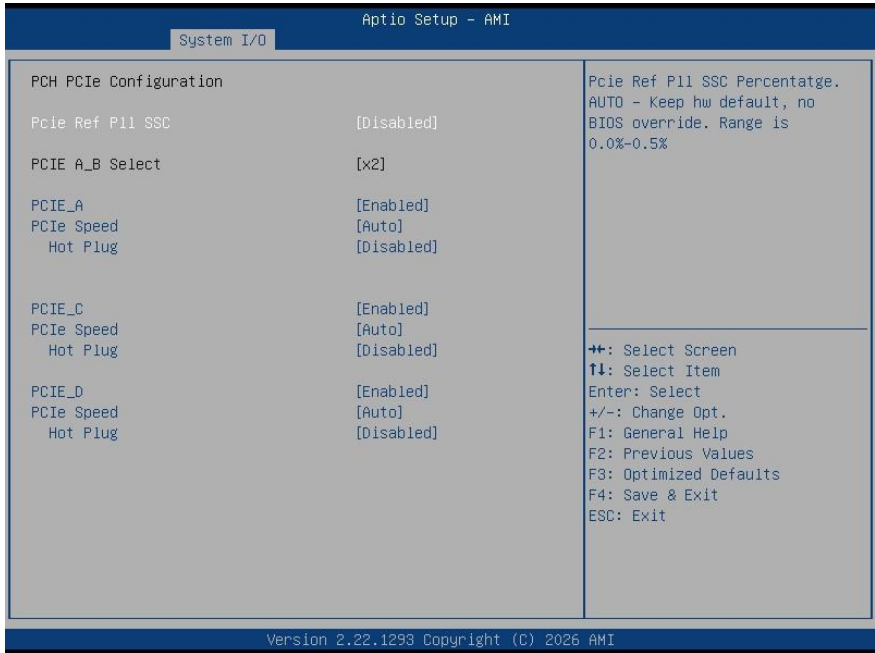


Interface item set to "MMIO"		
Options Summary		
MMIO Address	0	Optimal Default, Failsafe Default
Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF.		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected. According to register - Robot read register according to configuration.		
Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

3.5 Setup Submenu: System I/O



3.5.1 PCI Express Configuration



Options Summary		
Pcie Ref Pll SSC	Auto	
	0.0%	
	0.1%	
	0.2%	
	0.3%	
	0.4%	
	0.5%	
	Disable	Optimal Default, Failsafe Default
Configure the PCIe Reference PLL Spread Spectrum Clocking (SSC) percentage. Auto – Uses the hardware default setting with no BIOS override. 0.0%–0.5% – Manually set the SSC percentage within the supported range. Disable – Disables PCIe Reference PLL SSC.		
PCIe_A C D	Disable	
	Enable	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		

Options Summary

PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
	Gen4	
Configure PCIe Speed.		
Hot Plug	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/Disable PCI Express Hot Plug.		

3.5.2 Storage Configuration

Aptio Setup - AMI

System I/O

<p>▶ NVMe Configuration</p> <p>eMMC 5.1 Controller [Enabled]</p> <p>SATA Controller(s) [Enabled]</p> <p>SATA Speed [Auto]</p> <p>Serial ATA Port 0 Empty</p> <p> Software Preserve Unknown</p> <p> Port 0 [Enabled]</p> <p> Hot Plug [Disabled]</p> <p> Configured as eSATA Hot Plug supported</p> <p> SATA Device Type [Hard Disk Drive]</p>	<p>NVMe Device Options Settings</p> <p>++: Select Screen</p> <p>f1: Select Item</p> <p>Enter: Select</p> <p>+/-: Change Opt.</p> <p>F1: General Help</p> <p>F2: Previous Values</p> <p>F3: Optimized Defaults</p> <p>F4: Save & Exit</p> <p>ESC: Exit</p>
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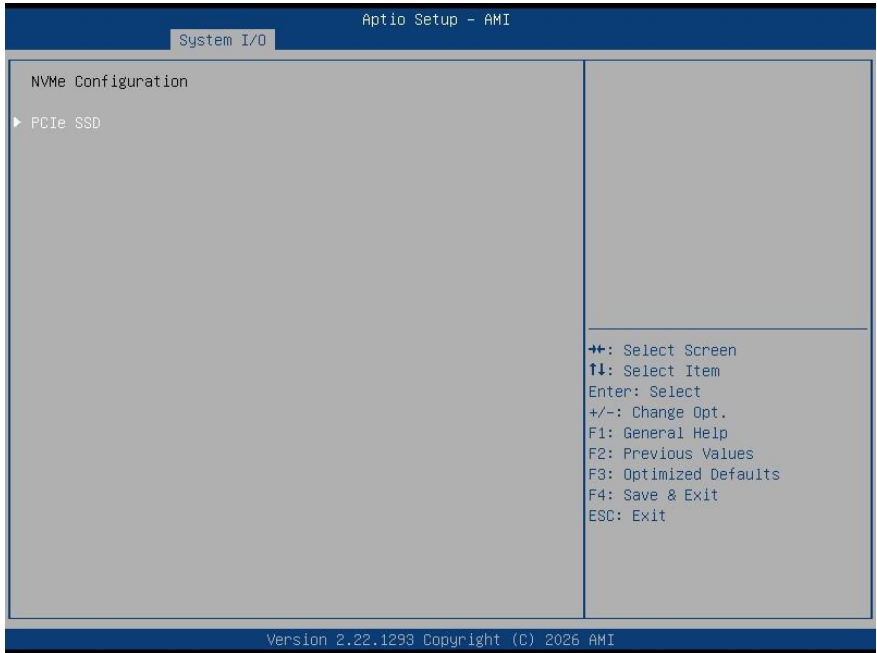
Version 2.22.1293 Copyright (C) 2026 AMI

Options Summary

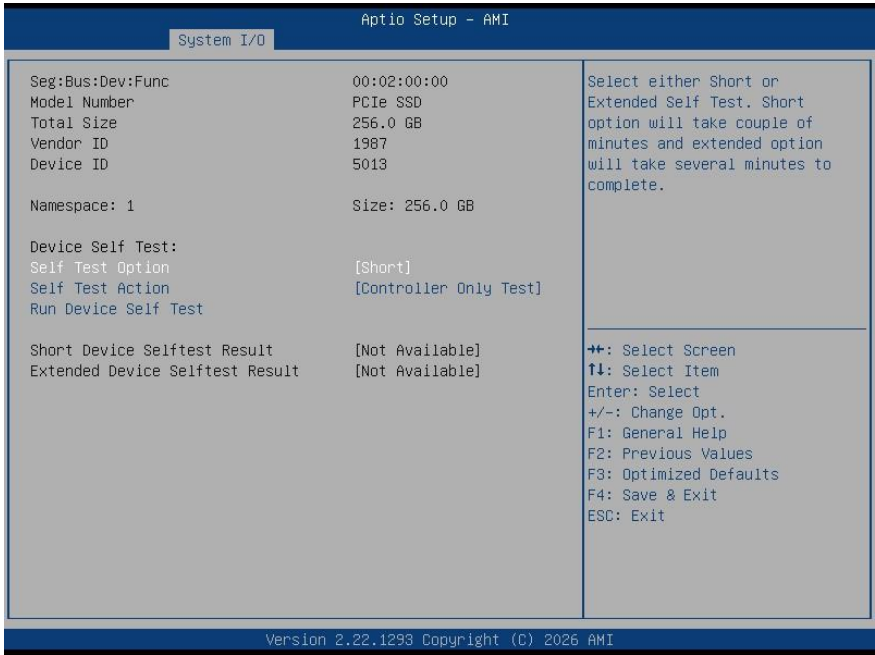
eMMC 5.1 Controller	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SCSI eMMC 5.1 Controller		

Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
SATA Controller(s)	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure the maximum supported SATA link speed: Gen1 – 1.5 Gb/s Gen2 – 3.0 Gb/s Gen3 – 6.0 Gb/s		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		
SATA Device Type	Hard Disk Drive	Optimal Default, Failsafe Default
	Solid State Drive	
Identify whether the connected SATA device is a Solid State Drive (SSD) or a Hard Disk Drive (HDD).		

3.5.2.1 NVMe Configuration

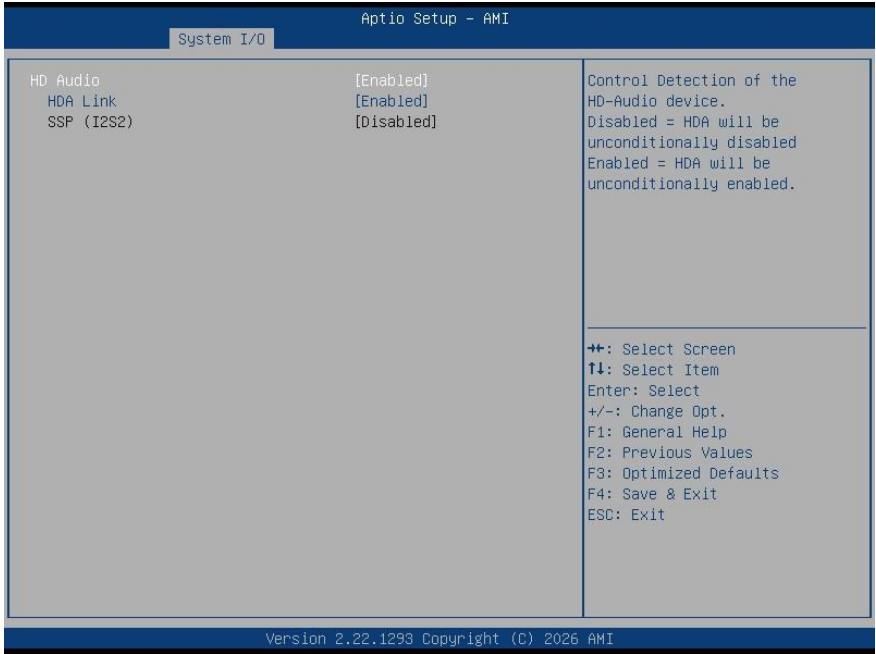


3.5.2.2 PCIe SSD



Options Summary		
Self Test Option	Short	Optimal Default, Failsafe Default
	Extended	
Select the type of self-test to perform on the SATA device: Short – Completes in a few minutes. Extended – Takes several minutes to complete for a more thorough test.		
Self Test Action	Controller only test	Optimal Default, Failsafe Default
	Controller and NameSpace test	
Select the scope of the self-test for the NVMe device: Controller Only – Tests the controller alone. Controller and Namespace – Tests both the controller and namespace. This option takes significantly longer to complete.		

3.5.3 HD Audio Configuration



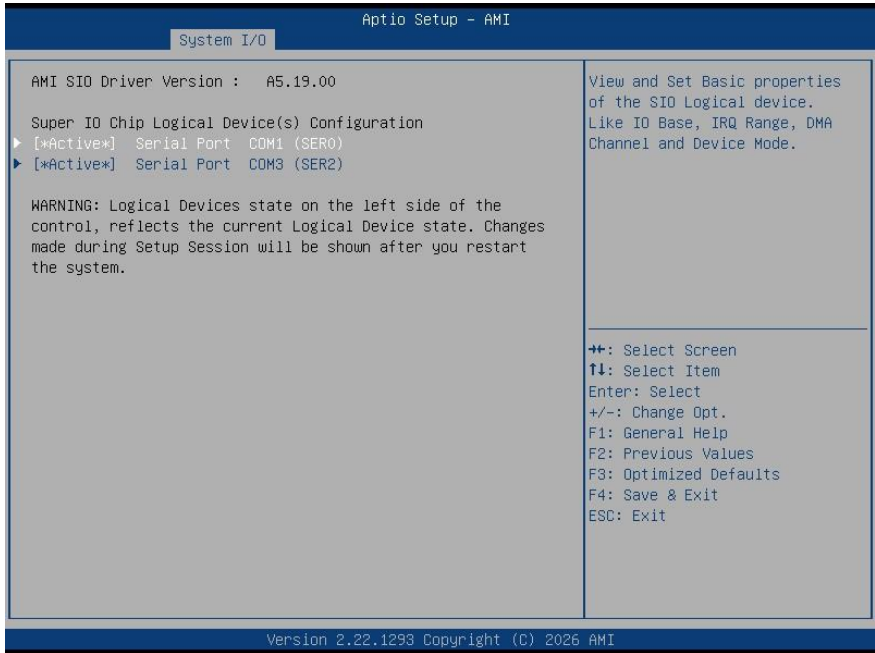
Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled.		
HAD Link	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable the HAD link. Supports multiplexed interfaces: HDA or SSP (I2S2).		
SSP (I2S2)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable the SSP (I2S2) interface. Supports multiplexed interfaces: HDA or SSP (I2S2).		

3.5.4 Digital IO Port Configuration

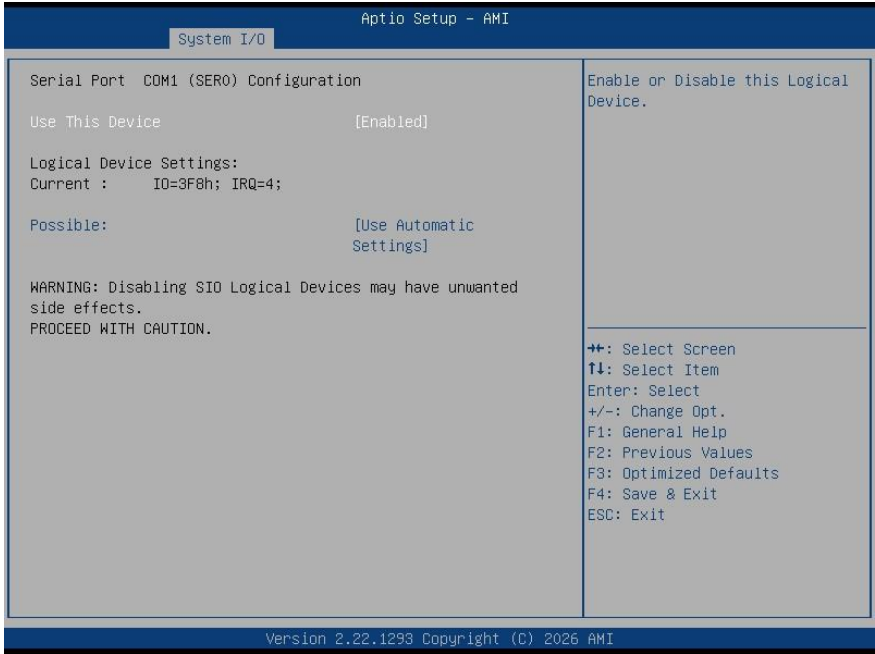


Options Summary		
GPIO 7 – 13	Input	Optimal Default, Failsafe Default
	Output	
Set GPIO as Input or Output.		
Output Level	High	
	Low	Optimal Default, Failsafe Default
Set output level when GPIO pin is output.		

3.5.5 Legacy Logical Devices Configuration

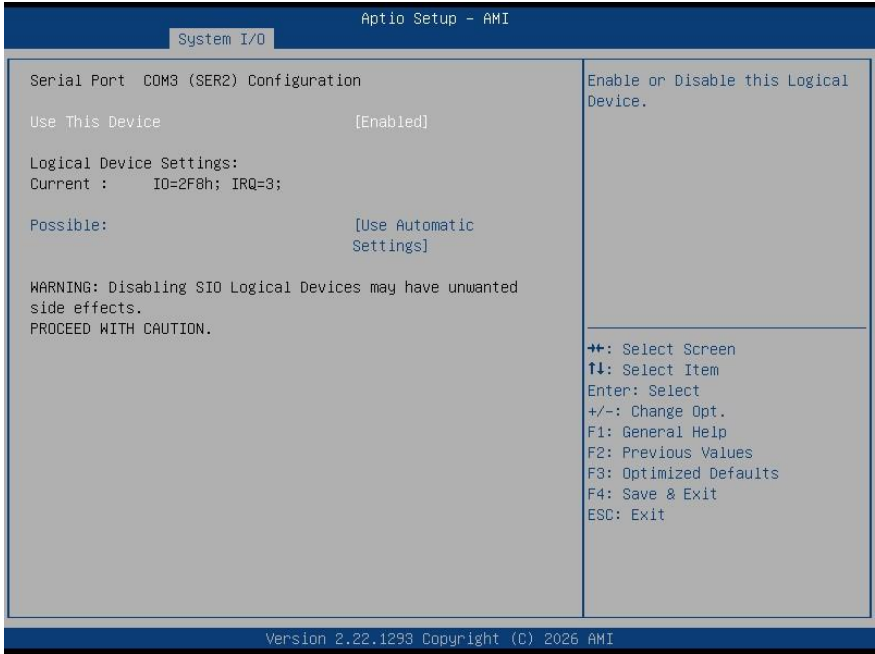


3.5.5.1 Serial Port COM1 (SER0)



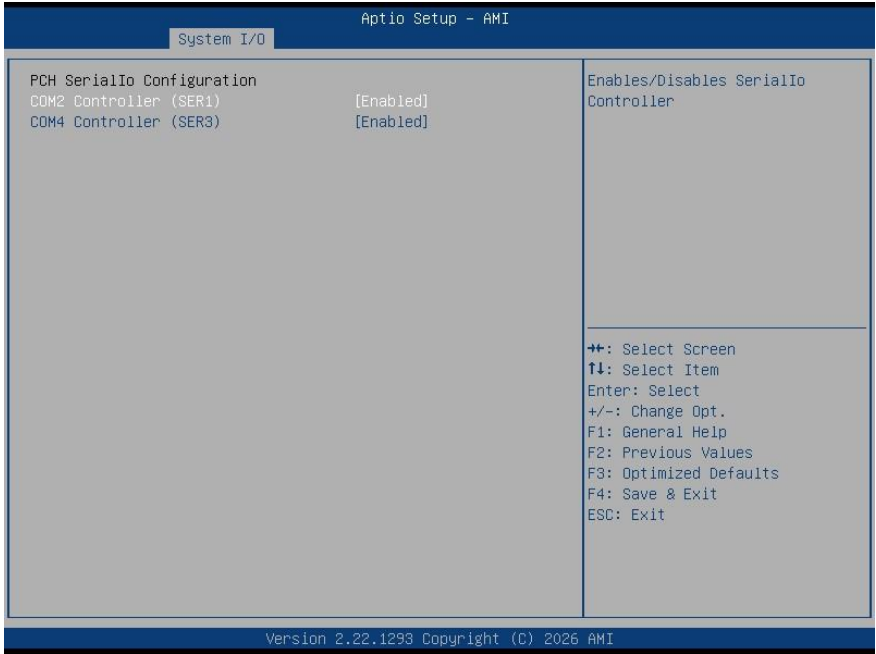
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Use This Device	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4; DMA;	
	IO=2C8h; IRQ=11; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.5.2 Serial Port COM3 (SER2)



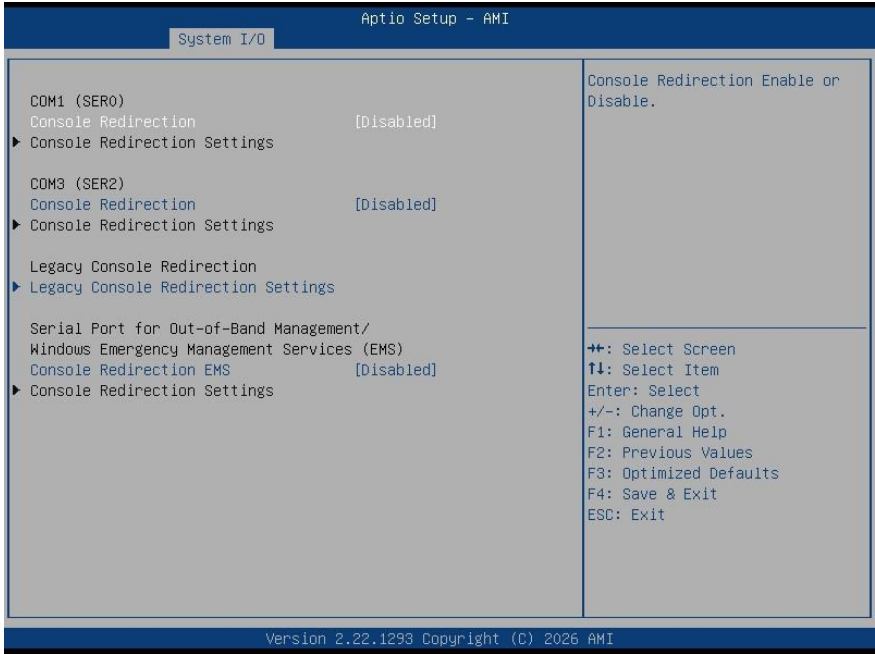
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Use This Device	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3; DMA;	
	IO=2d8h; IRQ=10; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.6 PCH Serial IO Configuration



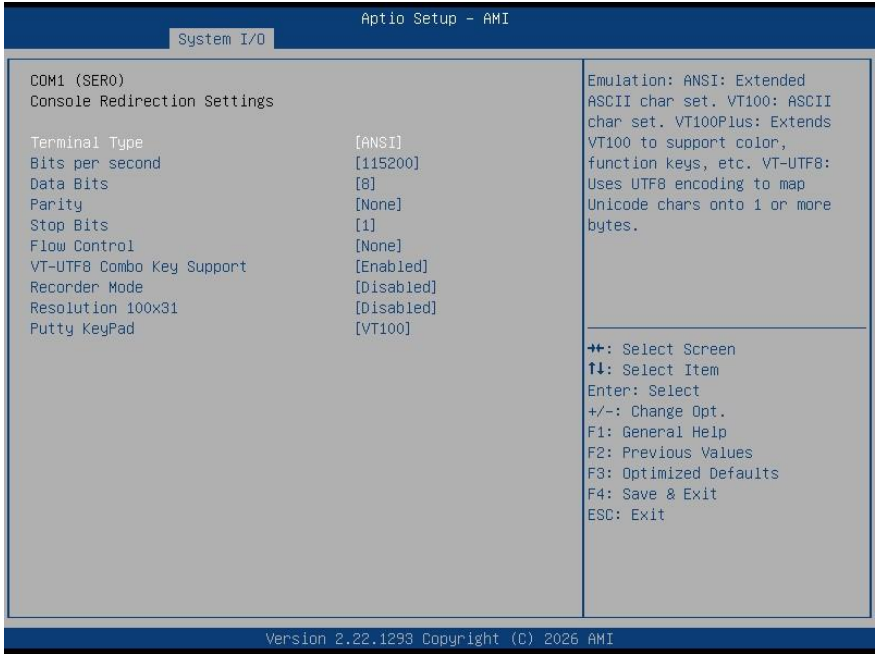
Options Summary		
COM2 Controller (SER1)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables/Disables SerialIo Controller		
COM4 Controller (SER3)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables/Disables SerialIo Controller		

3.5.7 Serial Port Console Redirection



Options Summary		
COM1 (SER0) Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection.		
COM3 (SER2) Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection.		

3.5.7.1 COM1 (SER0) Console Redirection Settings



Options Summary		
COM1 (SER0) Console Redirection	VT100	
	VT100Plus	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
	230400	

Options Summary		
Bits per second (cont.)	460800	
	921600	
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
<p>A parity bit can be sent with the data bits to detect some transmission errors.</p> <p>Even: parity bit is 0 if the num of 1's in the data bits is even.</p> <p>Odd: parity bit is 0 if num of 1's in the data bits is odd.</p> <p>Mark: parity bit is always 1.</p> <p>Space: Parity bit is always 0.</p> <p>Mark and Space Parity do not allow for error detection.</p> <p>They can be used as an additional data bit.</p>		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
<p>Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning).</p> <p>The standard setting is 1 stop bit.</p> <p>Communication with slow devices may require more than 1 stop bit.</p>		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
<p>Flow control helps prevent data loss due to buffer overflow. When sending data, if the receiving buffer is full, a stop signal is sent to pause the data flow. Once the buffer has space, a start signal resumes the flow. Hardware flow control uses two wires (RTS/CTS) to transmit the start and stop signals.</p>		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
<p>When enabled, only text data will be sent.</p> <p>This mode is used to capture terminal output for logging purposes.</p>		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	

Options Summary

Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.5.7.2 COM3 (SER2) Console Redirection Settings

The screenshot shows the 'System I/O' menu in the Aptio Setup - AMI BIOS. The 'COM3 (SER2) Console Redirection Settings' are displayed on the left, and a help menu is on the right.

System I/O	
COM3 (SER2) Console Redirection Settings	
Terminal Type	[ANSI]
Bits per second	[115200]
Data Bits	[8]
Parity	[None]
Stop Bits	[1]
Flow Control	[None]
VT-UTF8 Combo Key Support	[Enabled]
Recorder Mode	[Disabled]
Resolution	100x31
Putty KeyPad	[VT100]

Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100Plus: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

++: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 ESC: Exit

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Options Summary

Terminal Type	VT100	
	VT100Plus	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default

Options Summary

Emulation:

ANSI: Extended ASCII char set.

VT100: ASCII char set.

VT100Plus: Extends VT100 to support color, function keys.

VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
	230400	
	460800	
	921600	

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

Data Bits	7	
	8	Optimal Default, Failsafe Default

Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	

A parity bit can be sent with the data bits to detect some transmission errors.

Even: parity bit is 0 if the num of 1's in the data bits is even.

Odd: parity bit is 0 if num of 1's in the data bits is odd.

Mark: parity bit is always 1.

Space: Parity bit is always 0.

Mark and Space Parity do not allow for error detection.

They can be used as an additional data bit.

Stop Bits	1	Optimal Default, Failsafe Default
	2	

Stop bits indicate the end of a serial data packet.

(A start bit indicates the beginning).

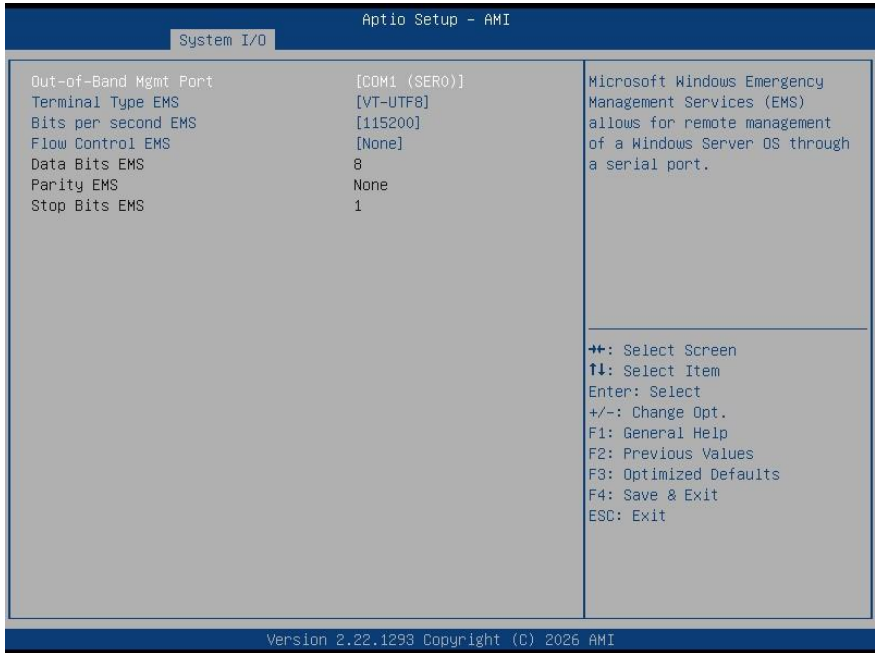
The standard setting is 1 stop bit.

Communication with slow devices may require more than 1 stop bit.

Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	

Options Summary		
Flow control prevents data loss from buffer overflow. If the receiving buffer is full, a stop signal pauses data transmission. Once the buffer has space, a start signal resumes the flow. Hardware flow control uses two wires (RTS/CTS) to send start and stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, only text data will be sent. This mode is used to capture terminal output for logging purposes.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

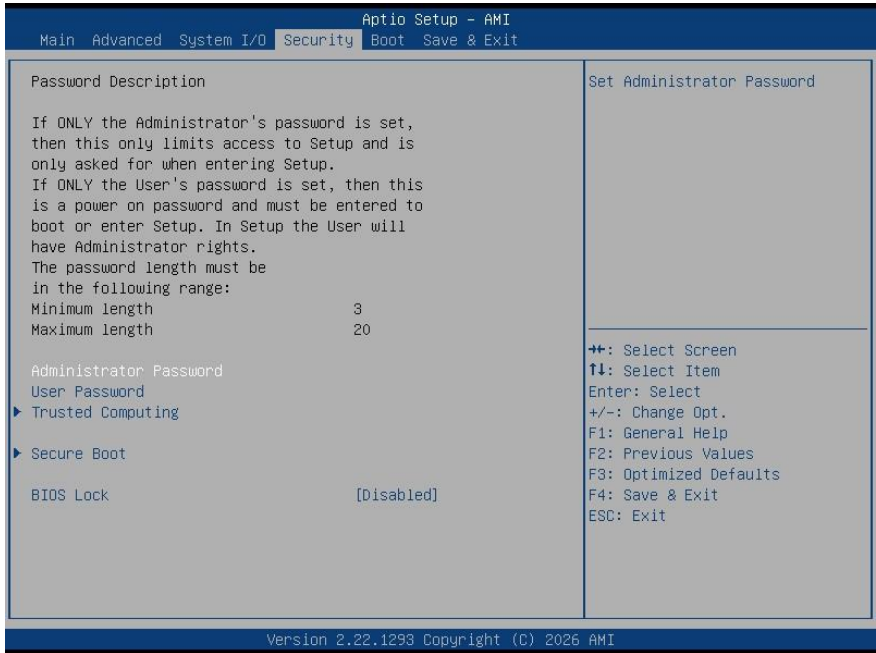
3.5.7.3 Console Redirection Settings – Out-of-Band Mgmt



Options Summary		
Out-of-Band Mgmt Port	COM1	
	COM2	Optimal Default, Failsafe Default
Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port		
Terminal Type EMS	VT100	
	VT100Plus	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits per second EMS	9600	
	19200	
	38400	
	57600	

Options Summary		
Bits per second EMS (cont.)	115200	Optimal Default, Failsafe Default
	230400	
	460800	
	921600	
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Flow Control EMS	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software Xon/Xoff	
<p>Flow control can prevent data loss from buffer overflow.</p> <p>When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow.</p> <p>Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.</p>		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

Options Summary

BIOS Lock	Disabled	
	Enabled	Optimal Default, Failsafe Default

Enable or Disable the PCH BIOS Lock feature.
Note: This must be enabled to ensure SMM (System Management Mode) protection of the BIOS flash.

3.6.1 Trusted Computing

Aptio Setup - AMI

Security

TPM 2.0 Device Found Firmware Version: 7.2 Vendor: NTC Security Device Support [Enable] Active PCR banks SHA256 Available PCR banks SHA256,SHA384 SHA256 PCR Bank [Enabled] SHA384 PCR Bank [Disabled] Pending operation [None] Platform Hierarchy [Enabled] Storage Hierarchy [Enabled] Endorsement Hierarchy [Enabled] Physical Presence Spec Version [1.3] TPM 2.0 InterfaceType [TIS] Device Select [TPM 2.0] Disable Block Sid [Disabled]	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
---	---

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Options Summary

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default

Enable or Disable BIOS support for the security device.
 When Disabled, the operating system will not detect the security device, and both the TCG EFI protocol and INT1A interface will be unavailable.

SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default

Options Summary

Enable or Disable SHA256 PCR Bank.

SHA384 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default

Enable or Disable SHA384 PCR Bank.

Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	

Schedule an Operation for the Security Device. **Note:** Your Computer will reboot during restart in order to change State of Security Device.

Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default

Enable or disable Platform Hierarchy.

Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default

Enable or Disable Storage Hierarchy.

Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default

Enable or Disable Endorsement Hierarchy.

Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default

Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.

Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default

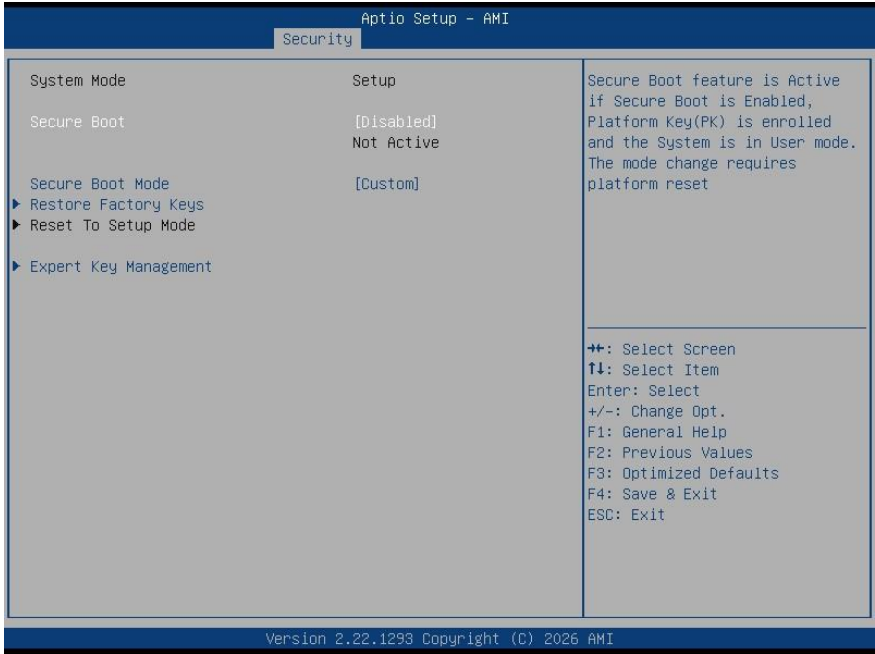
TPM 1.2 will restrict support to TPM 1.2 devices.

TPM 2.0 will restrict support to TPM 2.0 devices.

Auto will support both with the default set to TPM 2.0 devices if not found.

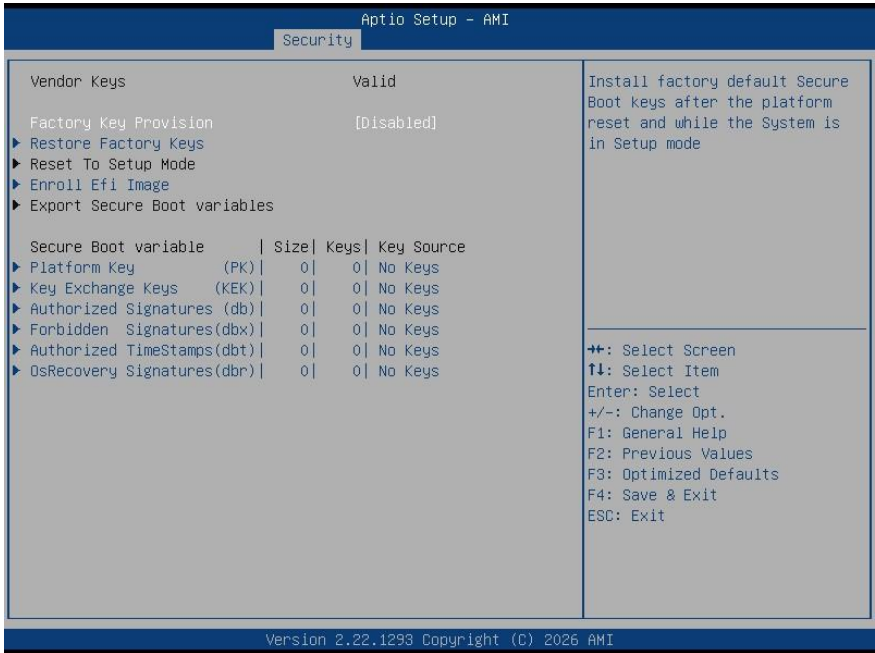
TPM 1.2 devices will be enumerated.

3.6.2 Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
The Secure Boot feature is active when Secure Boot is Enabled, the Platform Key (PK) is enrolled, and the system is in User mode.		
Note: Changing the Secure Boot mode requires a platform reset.		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Select the Secure Boot mode: Standard or Custom.		
Standard – Uses default Secure Boot policies.		
Custom – Allows a physically present user to configure Secure Boot policy variables without full authentication.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Restore To Setup Mode		
Force System Delete all Secure Boot key databases from NVRAM.		

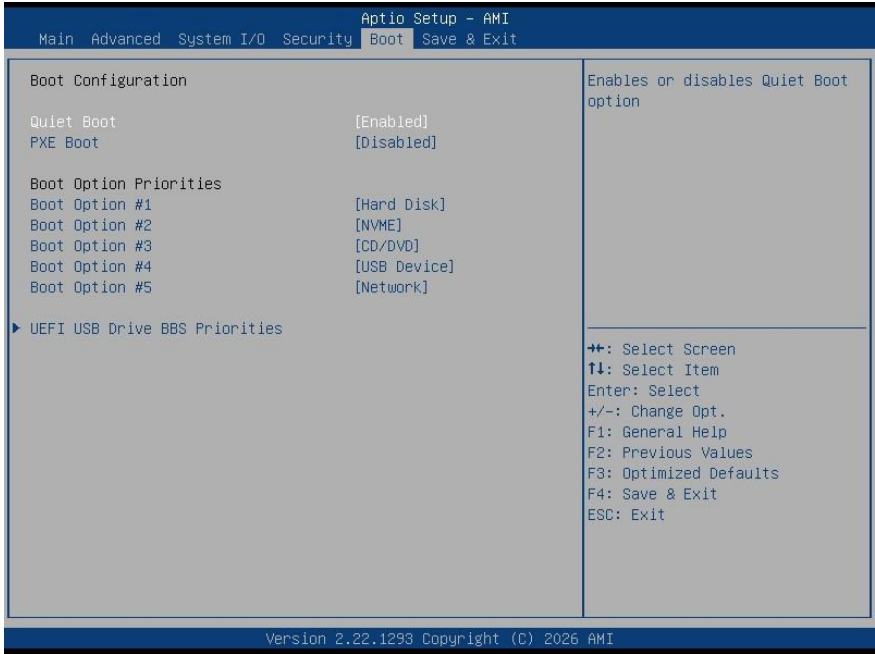
3.6.2.1 Expert Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Reset to Setup Mode		
Delete all Secure Boot key databases from NVRAM.		
Export Secure Boot variables		
Save NVRAM content of Secure Boot variable to a file.		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).		
Platform Key (PK)	Details	
	Export	

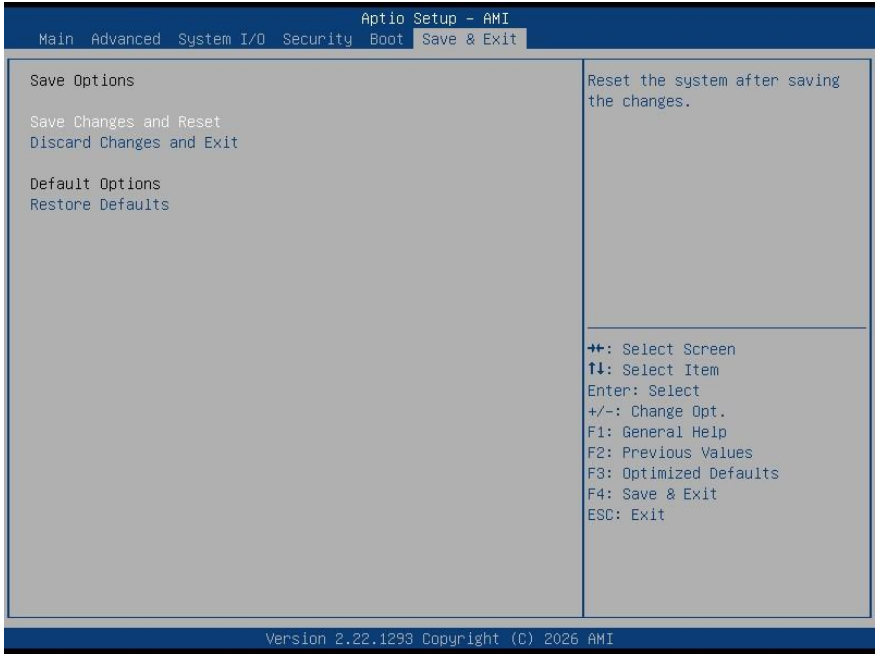
Options Summary	
Platform Key (PK) (cont.)	Update
	Delete
Key Exchange Keys (KEK)	Details
	Export
	Update
	Append
	Delete
Authorized Signatures (db)	Details
	Export
	Update
	Append
	Delete
Forbidden Signatures (dbx)	Details
	Export
	Update
	Append
	Delete
Authorized TimeStamps (dbt)	Update
	Append
OsRecovery Signatures (dbr)	Update
	Append
<p>Enroll Factory Defaults or load certificates from a file:</p> <ol style="list-style-type: none"> 1. Public Key Certificate: <ol style="list-style-type: none"> a. EFI_SIGNATURE_LIST b. EFI_CERT_X509 (DER) c. EFI_CERT_RSA2048 (bin) d. EFI_CERT_SHAXXX 2. Authenticated UEFI Variable 3. EFI PE/COFF Image (SHA256) <p>Key Source: Factory, Modified, Mixed</p>	

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the uCOM-TWL can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en>

Download the driver(s) you need and follow the steps below to install them.

Chipset Driver

1. Open the folder where you unzipped the **Chipset Drivers**
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Graphics Driver

1. Open the folder where you unzipped the **Graphics Drivers**
2. Run the **gfx_win_101.4644.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

LAN Drivers

1. Open the folder where you unzipped the **LAN Drivers**
2. Run the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Install Audio Drivers

Note: Ensure Intel Smart Sound Driver (v10.29.00.7919) is installed before the Realtek Audio driver (Realtek Audio 6.0.9034.2)

Install Intel Smart Sound Driver

1. Open the **Audio** folder
2. Open the **10.29.00.8102** subfolder
3. Follow the setup information within the file to manually install driver.

Install Realtek Audio Driver

1. Open the **Audio** folder
2. Open the **Realtek Audio 6.0.9034.2** folder
3. Run the **Setup.exe** file in the folder
4. Follow the instructions
5. Driver will be installed automatically

Install ME Driver

1. Open the **ME** folder
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Install Serial IO Driver

1. Open the **Serial IO Driver** folder
2. Run the **SetupSerialIO.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Install Camera Driver

1. Open the **Camera Drivers** folder
2. Follow the instructions in the setup guides provided to manually install driver(s)

Appendix A

I/O Information



A.1 I/O Address Map

Address Range	Device Name
[0000000000000000 - 00000000000000CF7]	PCI Express Root Complex
[00000000000000020 - 0000000000000021]	Programmable interrupt controller
[00000000000000024 - 0000000000000025]	Programmable interrupt controller
[00000000000000028 - 0000000000000029]	Programmable interrupt controller
[0000000000000002C - 000000000000002D]	Programmable interrupt controller
[0000000000000002E - 000000000000002F]	Motherboard resources
[00000000000000030 - 0000000000000031]	Programmable interrupt controller
[00000000000000034 - 0000000000000035]	Programmable interrupt controller
[00000000000000038 - 0000000000000039]	Programmable interrupt controller
[0000000000000003C - 000000000000003D]	Programmable interrupt controller
[00000000000000040 - 0000000000000043]	System timer
[0000000000000004E - 000000000000004F]	Motherboard resources
[00000000000000050 - 0000000000000053]	System timer
[00000000000000061 - 0000000000000061]	Motherboard resources
[00000000000000063 - 0000000000000063]	Motherboard resources
[00000000000000065 - 0000000000000065]	Motherboard resources
[00000000000000067 - 0000000000000067]	Motherboard resources
[00000000000000068 - 0000000000000068]	Microsoft ACPI-Compliant Embedded Controller
[0000000000000006C - 000000000000006C]	Microsoft ACPI-Compliant Embedded Controller
[00000000000000070 - 0000000000000070]	Motherboard resources
[00000000000000080 - 0000000000000080]	Motherboard resources
[00000000000000092 - 0000000000000092]	Motherboard resources
[000000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[000000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[000000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[000000000000000AC - 00000000000000AD]	Programmable interrupt controller
[000000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[000000000000000B2 - 00000000000000B3]	Motherboard resources
[000000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[000000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[000000000000000BC - 00000000000000BD]	Programmable interrupt controller
[000000000000002F8 - 00000000000002FF]	Communications Port (COM2)
[000000000000003F8 - 00000000000003FF]	Communications Port (COM1)
[000000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[00000000000000680 - 0000000000000069F]	Motherboard resources
[00000000000000D00 - 0000000000000FFFF]	PCI Express Root Complex
[0000000000000164E - 0000000000000164F]	Motherboard resources
[00000000000001854 - 00000000000001857]	Motherboard resources
[00000000000002000 - 000000000000020FE]	Motherboard resources
[00000000000003000 - 00000000000003FFF]	PCI Express Root Port #9 - 54B0
[00000000000004000 - 0000000000000403F]	Intel(R) UHD Graphics
[00000000000004000 - 00000000000004FFF]	PCI Express Root Port #3 - 54BA
[00000000000004060 - 0000000000000407F]	Standard SATA AHCI Controller
[00000000000004080 - 00000000000004083]	Standard SATA AHCI Controller
[00000000000004090 - 00000000000004097]	Standard SATA AHCI Controller
[0000000000000EFA0 - 000000000000EFBF]	SMBus - 54A3

A.2 Memory Address Map





















































▼	Memory	
📁	[0000000000A0000 - 0000000000BFFFFF]	PCI Express Root Complex
📁	[0000000080400000 - 0000000080DFFFFF]	PCI Express Root Port #9 - 54B0
📁	[0000000080400000 - 00000000BFFFFF]	PCI Express Root Complex
📁	[0000000080E00000 - 0000000080EFFFFF]	Intel(R) Ethernet Controller I226-V #2
📁	[0000000080E00000 - 0000000080FFFFF]	PCI Express Root Port #10 - 54B1
📁	[0000000080F00000 - 0000000080F03FFF]	Intel(R) Ethernet Controller I226-V #2
📁	[0000000081000000 - 00000000810FFFFF]	Intel(R) Ethernet Controller I226-V
📁	[0000000081000000 - 00000000811FFFFF]	PCI Express Root Port #7 - 54BE
📁	[0000000081100000 - 0000000081103FFF]	Intel(R) Ethernet Controller I226-V
📁	[0000000081200000 - 0000000081201FFF]	Standard SATA AHCI Controller
📁	[0000000081200000 - 00000000812FFFFF]	PCI Express Root Port #3 - 54BA
📁	[0000000081202000 - 00000000812027FF]	Standard SATA AHCI Controller
📁	[0000000081203000 - 00000000812030FF]	Standard SATA AHCI Controller
📁	[00000000C0000000 - 00000000CFFFFFFF]	Motherboard resources
📁	[00000000FD690000 - 00000000FD69FFFFF]	Intel(R) Serial IO GPIO Host Controller - INTC1057
📁	[00000000FD6A0000 - 00000000FD6AFFFFF]	Intel(R) Serial IO GPIO Host Controller - INTC1057
📁	[00000000FD6D0000 - 00000000FD6DFFFFF]	Intel(R) Serial IO GPIO Host Controller - INTC1057
📁	[00000000FD6E0000 - 00000000FD6EFFFFF]	Intel(R) Serial IO GPIO Host Controller - INTC1057
📁	[00000000FE010000 - 00000000FE010FFF]	SPI (flash) Controller - 54A4
📁	[00000000FE03E000 - 00000000FE03E007]	Communications Port (COM3)
📁	[00000000FE03E008 - 00000000FE03EFFF]	Motherboard resources
📁	[00000000FE03F000 - 00000000FE03FFFFF]	Motherboard resources
📁	[00000000FE040000 - 00000000FE040007]	Communications Port (COM4)
📁	[00000000FE040008 - 00000000FE040FFF]	Motherboard resources
📁	[00000000FE041000 - 00000000FE041FFF]	Motherboard resources
📁	[00000000FED00000 - 00000000FED003FF]	High precision event timer
📁	[00000000FED20000 - 00000000FED27FFF]	Motherboard resources
📁	[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 2.0
📁	[00000000FED45000 - 00000000FED8FFFFF]	Motherboard resources
📁	[00000000FED90000 - 00000000FED93FFF]	Motherboard resources
📁	[00000000FEDA0000 - 00000000FEDA0FFF]	Motherboard resources
📁	[00000000FEDA1000 - 00000000FEDA1FFF]	Motherboard resources
📁	[00000000FEDC0000 - 00000000FEDC7FFF]	Motherboard resources
📁	[00000000FEE00000 - 00000000FEEFFFFF]	Motherboard resources
📁	[0000004000000000 - 0000004000FFFFFFF]	Intel(R) UHD Graphics
📁	[0000006000000000 - 00000060009FFFFF]	PCI Express Root Port #9 - 54B0
📁	[0000006000A00000 - 0000006000AFFFFF]	PCI Express Root Port #3 - 54BA
📁	[0000006001000000 - 0000006001FFFFFFF]	Intel(R) UHD Graphics
📁	[0000006002100000 - 000000600210FFFFF]	Intel(R) USB 3.1o eXtensible Host Controller - 1.20 (Microsoft)
📁	[0000006002110000 - 0000006002117FFF]	Performance Monitor
📁	[0000006002128000 - 00000060021280FF]	SMBus - 54A3
📁	[0000006002129000 - 0000006002129FFF]	Intel SD Host Controller
📁	[0000007FFFFE6000 - 0000007FFFFE6FFF]	Intel(R) Serial IO I2C Host Controller - 54C5
📁	[0000007FFFFE7000 - 0000007FFFFE7FFF]	Intel(R) Management Engine Interface #1
📁	[0000007FFFFE8000 - 0000007FFFFE8FFF]	Intel(R) Serial IO I2C Host Controller - 54EB
📁	[0000007FFFFE9000 - 0000007FFFFE9FFF]	Intel(R) Serial IO I2C Host Controller - 54E9
📁	[0000007FFFFEA000 - 0000007FFFFEAFFF]	Intel(R) Serial IO I2C Host Controller - 54E8
📁	[0000007FFFFEB000 - 0000007FFFFEBFFF]	Intel(R) Serial IO I2C Host Controller - 54C6
📁	[0000007FFFFEC000 - 0000007FFFFEFFFFF]	Intel® Smart Sound Technology BUS
📁	[0000007FFFFE0000 - 0000007FFFFEFFFFF]	Intel® Smart Sound Technology BUS





















































A.3 Large Memory Address Map





















































- ▼  Large Memory
 -  [0000004000000000 - 000007FFFFFFFF] PCI Express Root Complex





















































A.4 IRQ Mapping Chart





















































▼	Interrupt request (IRQ)	
	(ISA) 0x00000000 (00)	System timer
	(ISA) 0x00000003 (03)	Communications Port (COM2)
	(ISA) 0x00000004 (04)	Communications Port (COM1)
	(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INTCT1057
	(ISA) 0x00000010 (16)	Communications Port (COM3)
	(ISA) 0x00000011 (17)	Communications Port (COM4)
	(ISA) 0x00000037 (55)	Microsoft ACPI-Compliant System
	(ISA) 0x00000038 (56)	Microsoft ACPI-Compliant System
	(ISA) 0x00000039 (57)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003A (58)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003B (59)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003C (60)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003D (61)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003E (62)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003F (63)	Microsoft ACPI-Compliant System
	(ISA) 0x00000040 (64)	Microsoft ACPI-Compliant System
	(ISA) 0x00000041 (65)	Microsoft ACPI-Compliant System
	(ISA) 0x00000042 (66)	Microsoft ACPI-Compliant System
	(ISA) 0x00000043 (67)	Microsoft ACPI-Compliant System
	(ISA) 0x00000044 (68)	Microsoft ACPI-Compliant System
	(ISA) 0x00000045 (69)	Microsoft ACPI-Compliant System
	(ISA) 0x00000046 (70)	Microsoft ACPI-Compliant System
	(ISA) 0x00000047 (71)	Microsoft ACPI-Compliant System
	(ISA) 0x00000048 (72)	Microsoft ACPI-Compliant System
	(ISA) 0x00000049 (73)	Microsoft ACPI-Compliant System
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	(ISA) 0x00000063 (99)	Microsoft ACPI-Compliant System





















































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


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 (ISA) 0x000001FD (509)	Microsoft ACPI-Compliant System
 (ISA) 0x000001FE (510)	Microsoft ACPI-Compliant System
 (ISA) 0x000001FF (511)	Microsoft ACPI-Compliant System
 (PCI) 0x00000010 (16)	Intel SD Host Controller
 (PCI) 0x0000001B (27)	Intel(R) Serial IO I2C Host Controller - 54E8
 (PCI) 0x0000001F (31)	Intel(R) Serial IO I2C Host Controller - 54C5

 (PCI) 0x00000020 (32)	Intel(R) Serial IO I2C Host Controller - 54C6
 (PCI) 0x00000021 (33)	Intel(R) Serial IO I2C Host Controller - 54EB
 (PCI) 0x00000028 (40)	Intel(R) Serial IO I2C Host Controller - 54E9
 (PCI) 0xFFFFFFFF0 (-16)	Intel(R) Management Engine Interface #1
 (PCI) 0xFFFFFFFF1 (-15)	Intel® Smart Sound Technology BUS
 (PCI) 0xFFFFFFFF2 (-14)	Intel(R) Ethernet Controller I226-V
 (PCI) 0xFFFFFFFF3 (-13)	Intel(R) Ethernet Controller I226-V
 (PCI) 0xFFFFFFFF4 (-12)	Intel(R) Ethernet Controller I226-V
 (PCI) 0xFFFFFFFF5 (-11)	Intel(R) Ethernet Controller I226-V
 (PCI) 0xFFFFFFFF6 (-10)	Intel(R) Ethernet Controller I226-V
 (PCI) 0xFFFFFFFF7 (-9)	Intel(R) Ethernet Controller I226-V #2
 (PCI) 0xFFFFFFFF8 (-8)	Intel(R) Ethernet Controller I226-V #2
 (PCI) 0xFFFFFFFF9 (-7)	Intel(R) Ethernet Controller I226-V #2
 (PCI) 0xFFFFFFFFA (-6)	Intel(R) Ethernet Controller I226-V #2
 (PCI) 0xFFFFFFFFB (-5)	Intel(R) Ethernet Controller I226-V #2
 (PCI) 0xFFFFFFFFC (-4)	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
 (PCI) 0xFFFFFFFFD (-3)	Intel(R) UHD Graphics
 (PCI) 0xFFFFFFFFE (-2)	Standard SATA AHCI Controller