FWS-7840

Network Appliance

User's Manual 1st Ed

Last Updated: February 13, 2025

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Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7840	1
● Console Cable	1
● Ear Brackets	2
● SATA Cable	2
● SATA Power Cable	2
● HDD Kit	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period)) : 10 年

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON System QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	O	O	O	O	O
Connector and Cable	×	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU and Memory	×	O	O	O	O	O
Hard Disk	×	O	O	O	O	O
LCD Modules	×	O	O	O	O	O
CD-ROM/DVD-ROM	×	O	O	O	O	O
Touch Modules	×	O	O	O	O	O
Power	×	O	O	O	O	O
Battery	×	O	O	O	O	O

The table is prepared in accordance with the provisions of SJ/T 11364.

O：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years.

Notes：

1. This product defined period of use is under normal condition.
2. In above part, CPU/Memory/ Hard Disk/CD-ROM/DVD-ROM/ Power are optional.
3. In above part, LCD Modules/ Touch Modules are for all-in-one product model.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	1U Rackmount Network Platform
Processor	Intel® Xeon® W Processors (Comet Lake)
System Memory	2 x DDR4 2666-2933 U-DIMM
Chipset	Intel® W480
Ethernet	8 x Intel® i350 AM4 Gigabit Ethernet Ports
Bypass	Two-pair Bypass
BIOS	AMI BIOS
Serial ATA	2 x SATA III (6.0 Gbps) ports
Storage	2 x 2.5" HDD
Expansion	2 x NIM Slots
	1 x PCIe [x8] slot
	1 x Mini PCIe Slot
Watchdog Timer	1~255 steps, software programmable
RTC	Internal RTC
System Fan	2
Front I/O	1 x Power LED
	1 x Status LED
	1 x HDD Active LED
Rear I/O	1 x AC Power Input
	1 x Power Switch
	VGA Port (Optional)
	2 x Rear Expansion Slots (Optional)
Color	Black
Power Supply	250W Single PSU
Dimensions	430 mm x 305 mm x 44 mm

System	
Power Consumption	TBD
MTBF	TBD

Display	
Chipset	Intel® W480
Graphic Engine	HDMI from CPU Optional
Resolution	3840 x 2160
Connector	HDMI (Optional)

I/O	
Serial Port	1 x RJ-45 Console
Keyboard and Mouse	N/A
USB	2 x USB3.0

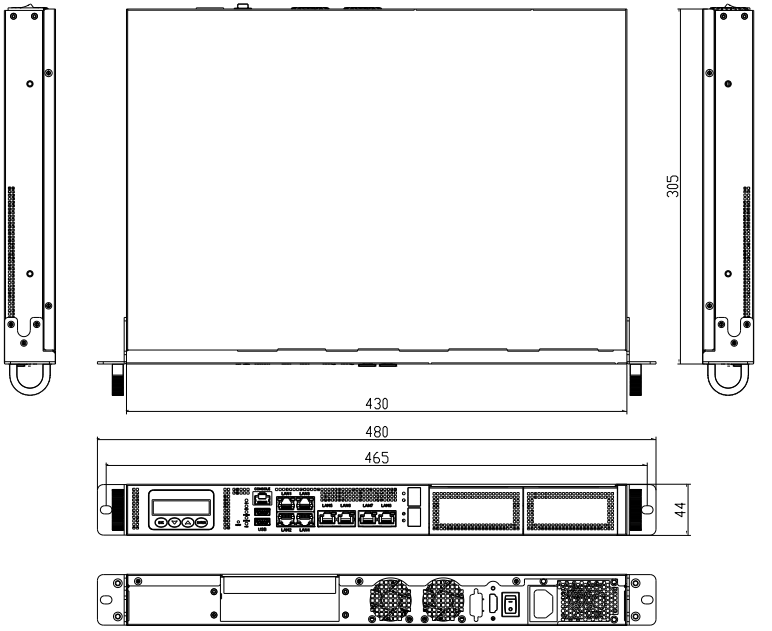
Environmental	
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10% ~ 80% relative humidity, non-condensing
Storage Humidity	10% ~ 80% at 40°C, non-condensing
Vibration	0.5 Grms/ 5~500Hz / operation (with 2.5" HDD) 1.5 Grms/ 5~500Hz / non-operation
Shock	10 G peak acceleration (11 msec. duration) operation 20 G peak acceleration (11 msec. duration) non-operation

Chapter 2

Hardware Information

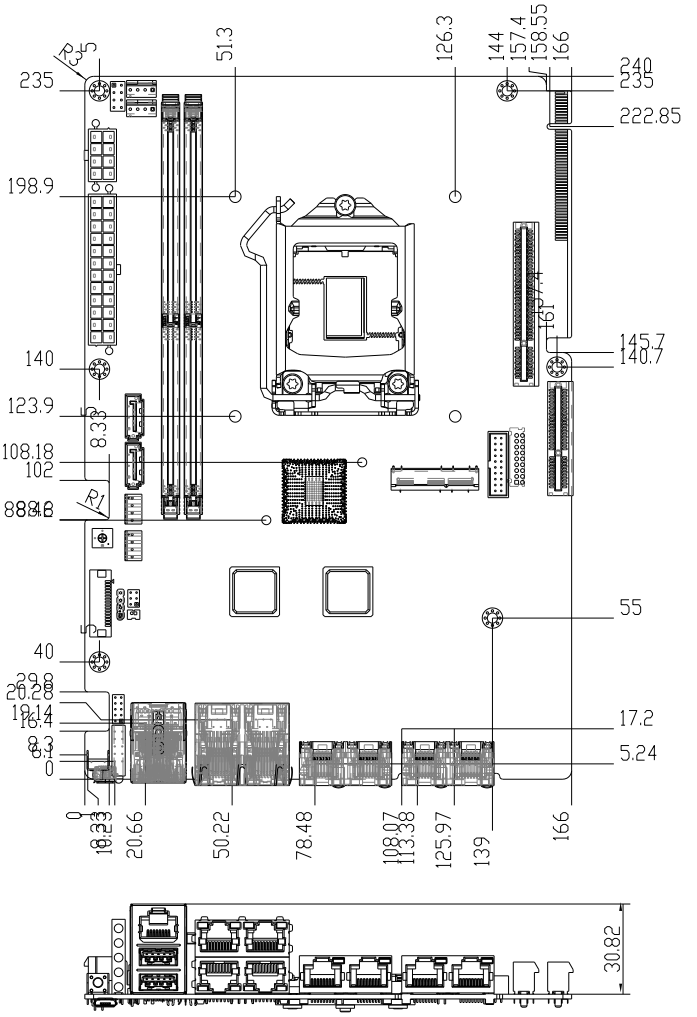
2.1 Dimensions

2.1.1 FWS-7840 System

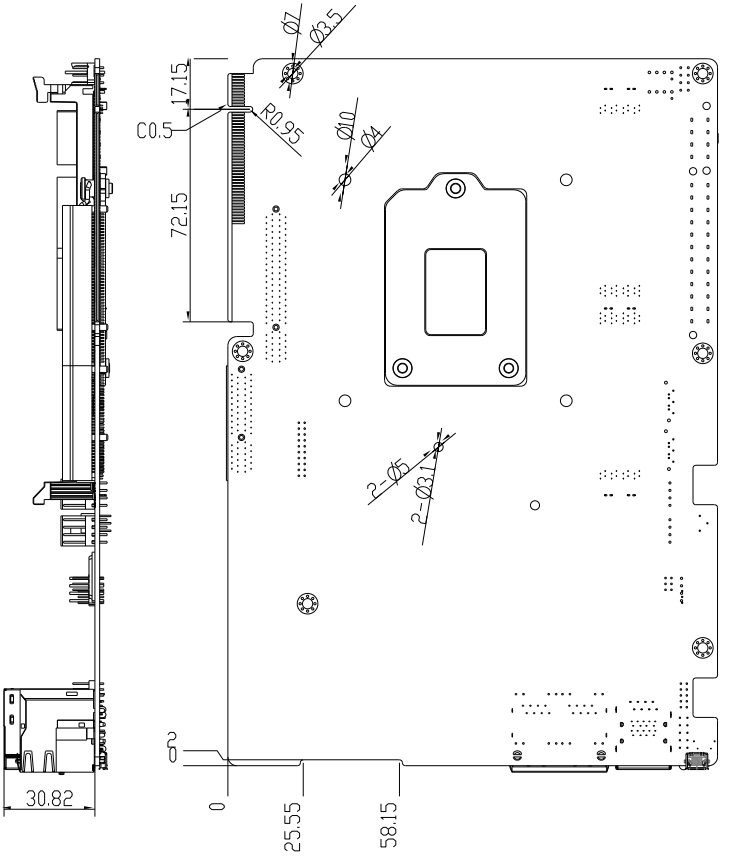


2.1.2 FWS-7840 Main Board

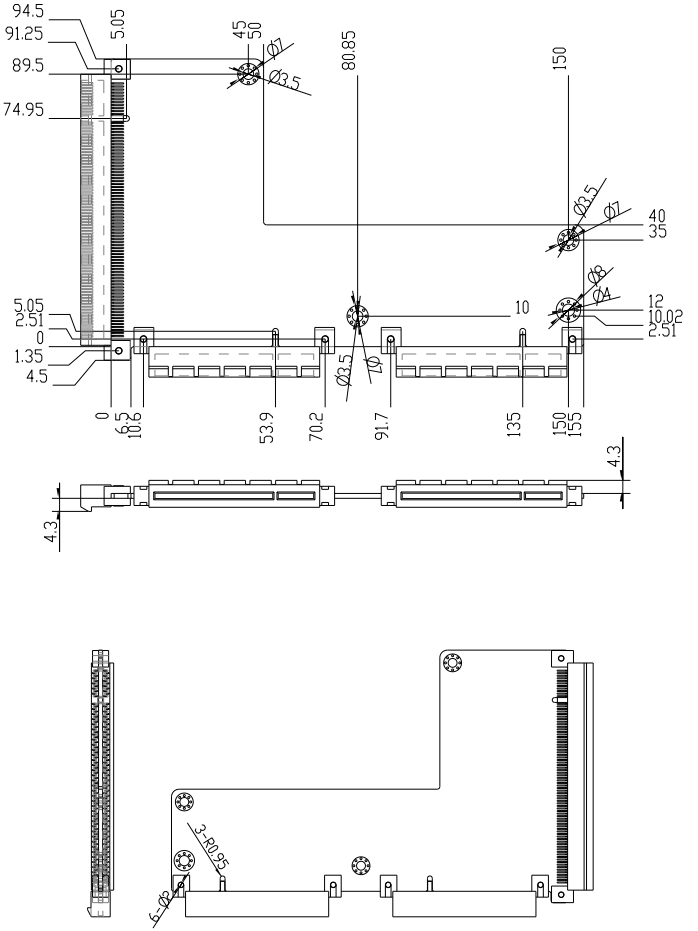
Component Side



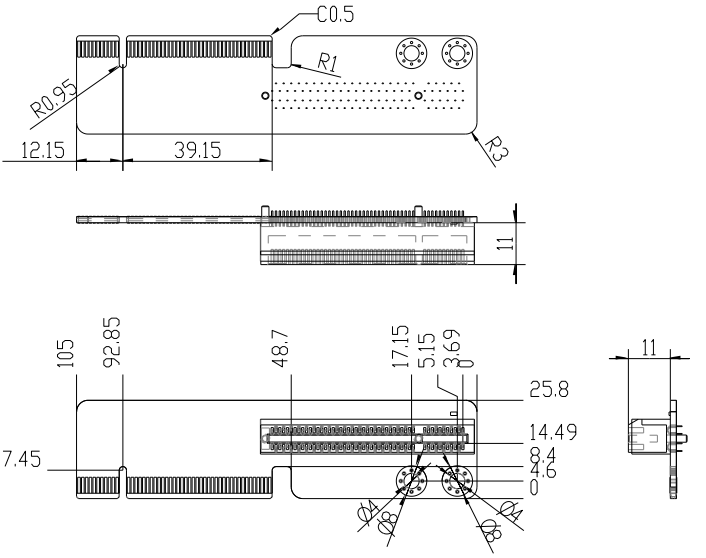
Main Board Solder Side



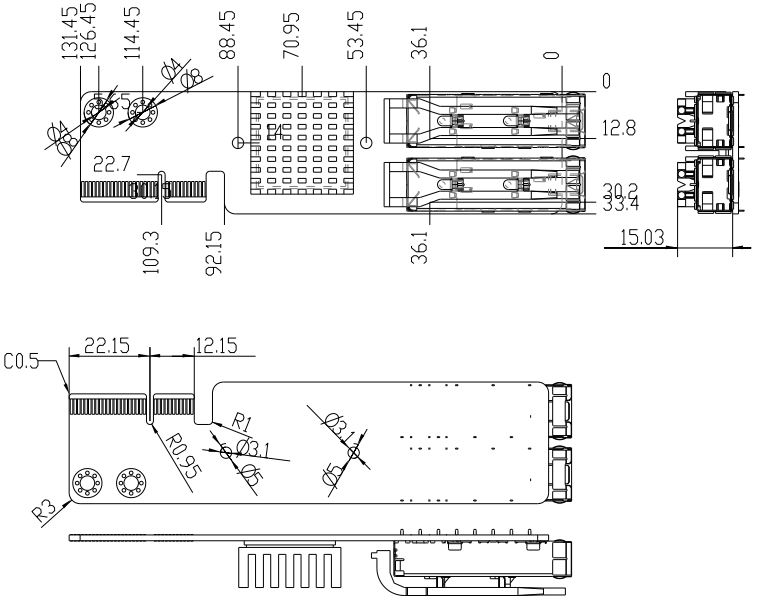
2.1.3 PER-T629 NIM Two Slot Riser Card



2.1.4 PER-T636 PCIe [x8] Riser Card

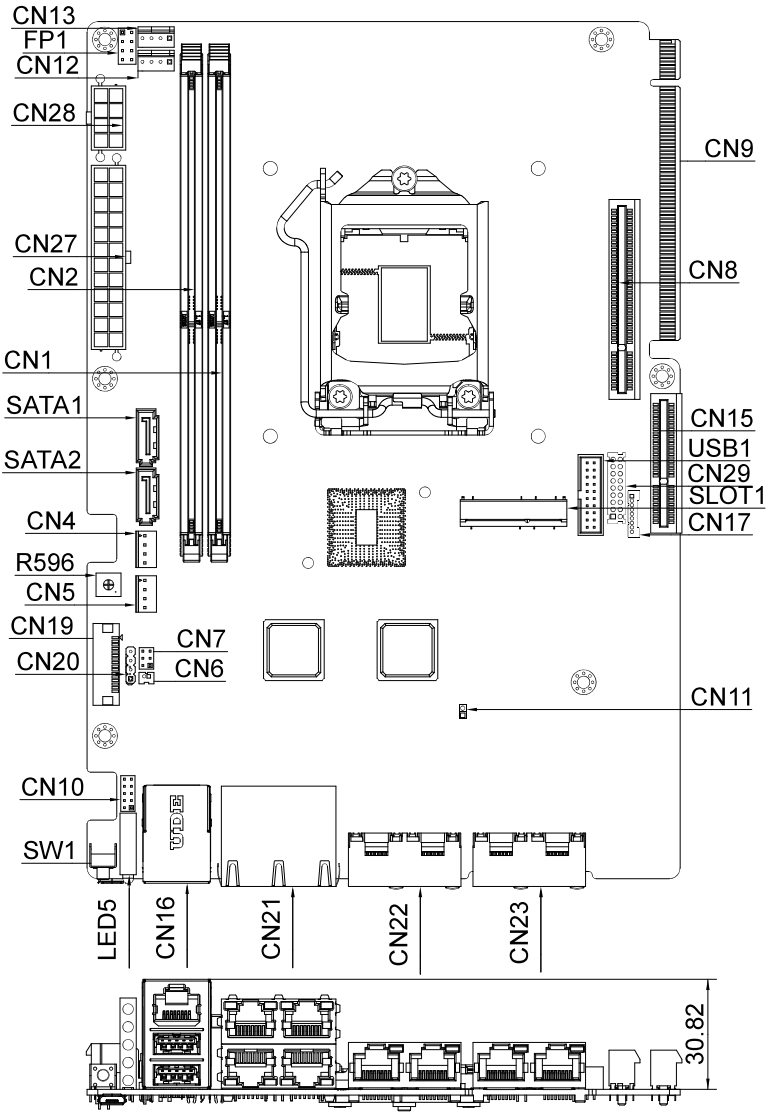


2.1.5 PER-T639 Dual SFP+ Port Expansion Card

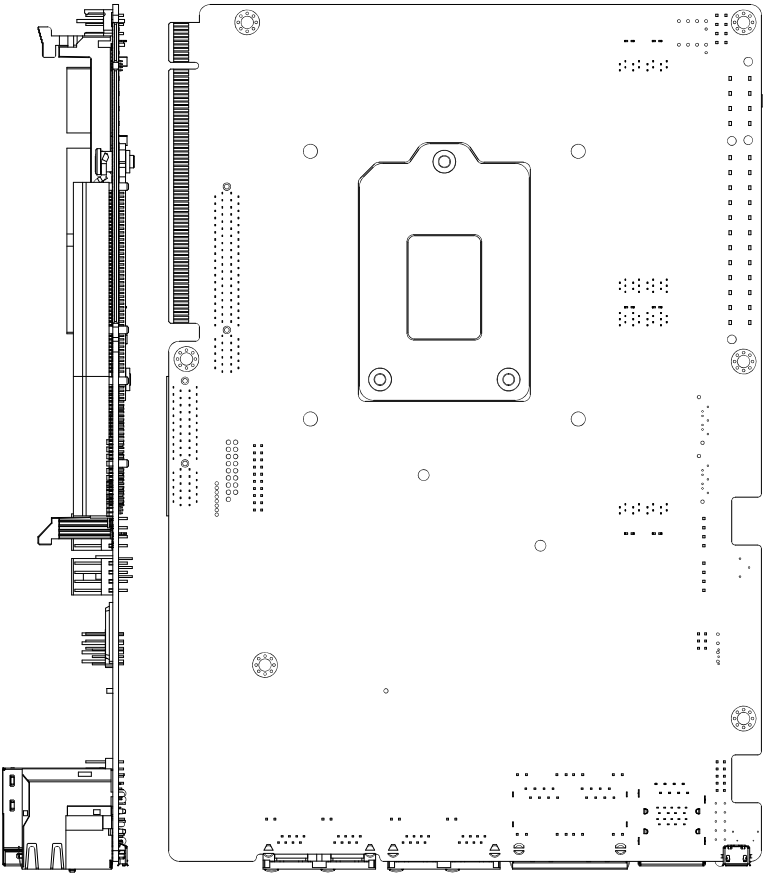


2.2 Jumpers and Connectors

Component Side



Solder Side

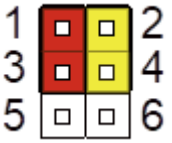


2.3 List of Jumpers

The FWS-7840 system board is configured with a number of jumpers which can be configured for your application. This section details those jumpers and their settings.

Label	Function
CN7	Clear CMOS

2.3.1 Clear CMOS



1-3, 2-4
Normal (**Default**)

3-5, 4-6
Clear CMOS

Note: To avoid unintended operation or damage to the system, do not use any other configuration than the ones shown.

2.4 List of Connectors

The FWS-7840 system board is configured with a number of connectors which can be used for configuring your system and connecting with external modules. This section details those connectors and settings.

Label	Function
CN1	DDR4 UDIMM Slot
CN2	DDR4 UDIMM Slot
CN4	SATA Power
CN5	SATA Power
CN6	Battery Header
CN8	PCIe [x8] Slot
CN9	PCIe [x16] Gold Finger
CN10	DIO Header
CN11	Case Open Sensor
CN12	FAN1
CN13	FAN2
CN15	PCIe [x4] Slot
CN16	Dual USB3.1 + RJ-45 Connector (Console)
CN17	COM Port
CN19	LCM
CN20	LCM
CN21	Quad RJ45 1Gbps Port Connector
CN22	Dual RJ45 1Gbps Port Connector
CN23	Dual RJ45 1Gbps Port Connector (Colay with M2, M3)
CN27	ATX Power Connector
CN28	ATX Power Connector
CN29	HDMI Header

Label	Function
FP1	Front Panel Header
LED5	Status LED
M2	SFP 1Gbps Port (Optional, Colay with CN23)
M3	SFP 1Gbps Port (Optional, Colay with CN23)
SATA1	SATA Connector
SATA2	SATA Connector
SLOT1	Mini Card socket (Optional, mSATA)
USB1	USB3.1 Header

2.4.1 Battery Header (CN6)

Pin	Signal
1	+3.3V
2	GND

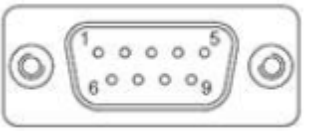
2.4.2 Digital I/O Header (CN10)

Pin	Signal	Pin	Signal
1	Digital I/O bit1	2	Digital I/O bit2
3	Digital I/O bit3	4	Digital I/O bit4
5	Digital I/O bit5	6	Digital I/O bit6
7	Digital I/O bit7	8	Digital I/O bit8
9	+5V	10	GND

2.4.3 Case Open Sensor (CN11)

Pin	Signal
1	Case Open
2	GND

2.4.4 COM Port (C17)

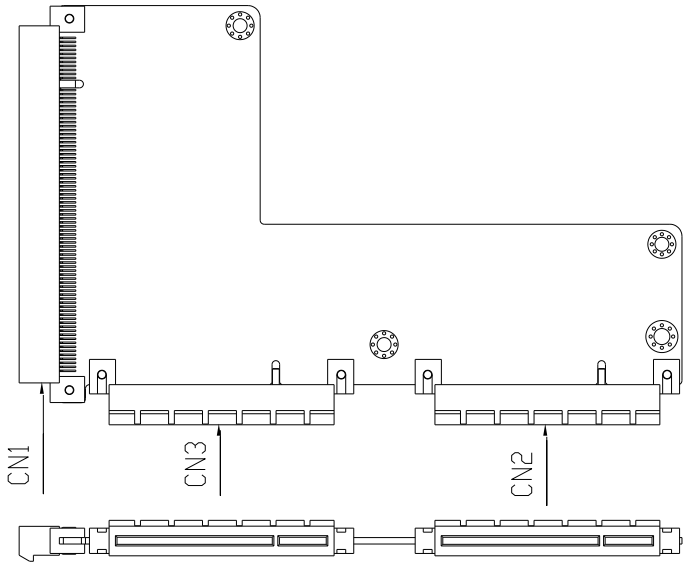


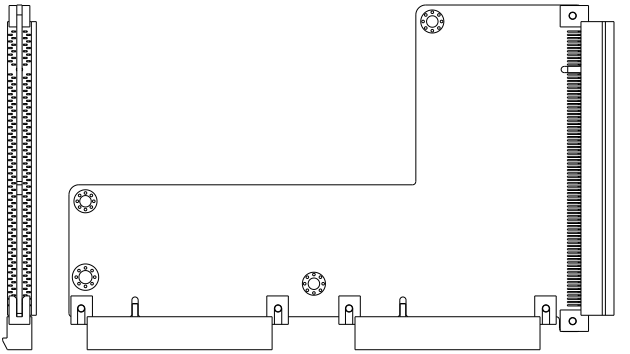
Pin	Signal	Pin	Signal
1	DCD2	2	DSR2
3	RXD2	4	RTS2
5	TXD2	6	CTS2
7	DTR2	8	RI2
9	GND		

2.4.5 Front Panel Pin Header (FP1)

Pin	Signal	Pin	Signal
1	Power Button SW+	2	Ground
3	Hardware Reset SW+	4	Ground
5	PWRLED	6	Ground
7	HDDACT	8	HDD LED-

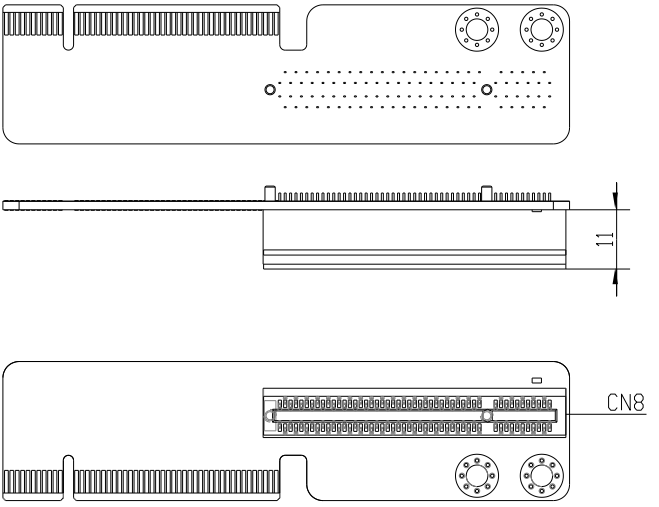
2.5 PER-T629 Connectors





2.6 PER-T636 PCIe [x8] Riser Card

2.6.1 PER-T636 Connectors

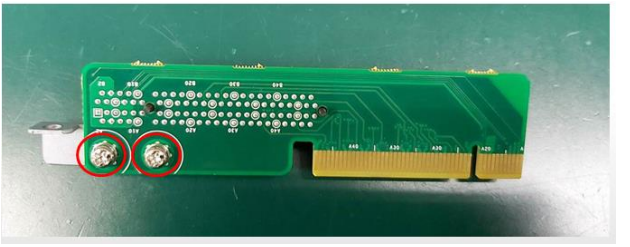


2.6.2 PER-T636 Installation Steps

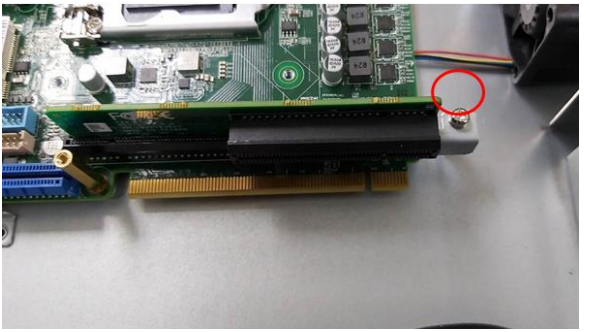
Before beginning installation make sure the system is powered down and the power sources are disconnected. Have the PER-T636 PCIe [x8] Riser Card and the PCIe card you wish to install ready.

Step 1: Remove the upper panel of the chassis by unscrewing seven (7) retaining screws.

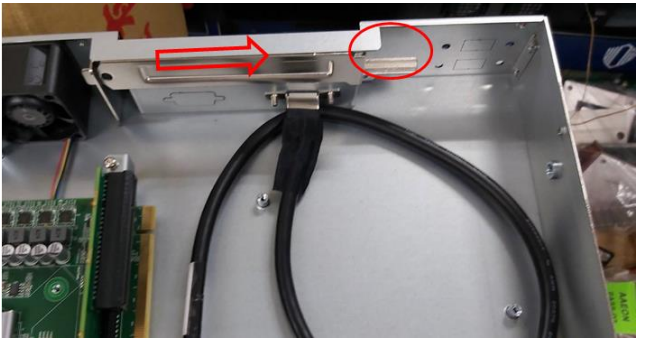
Step 2: Attach the bracket to the PER-T636 card with two screws, as shown:



Step 3: Insert PER-T636 card into the PCIe [x8] slot on the board. Secure the card by fastening a screw to the bracket.



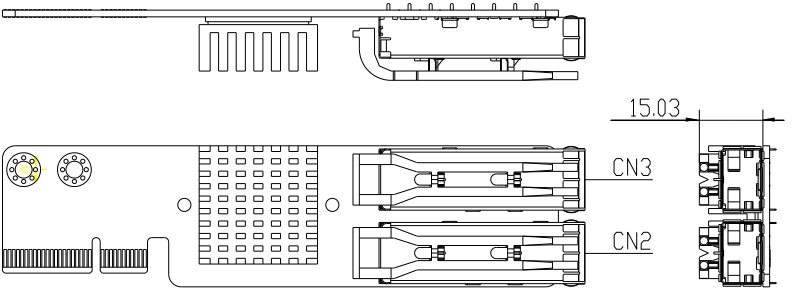
Step 4: Remove the rear I/O bracket by removing the retaining screw and sliding the bracket out.



Step 5: Insert the expansion card, ensuring the rear bracket lines up and the card inserts into the riser card. Secure with the screw removed in Step 4.

2.7 PER-639 Dual SFP+ Port Expansion Card

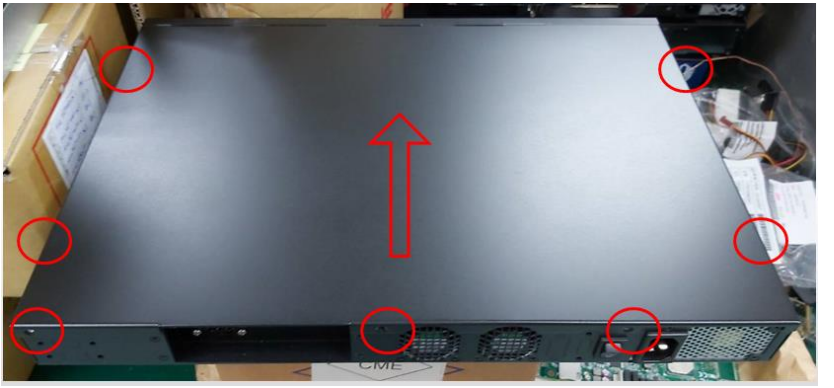
2.7.1 PER-639 Connectors



2.7.2 PER-639 Installation

Before beginning installation make sure the system is powered down and the power sources are disconnected. Have the PER-T639 Expansion Card ready to install.

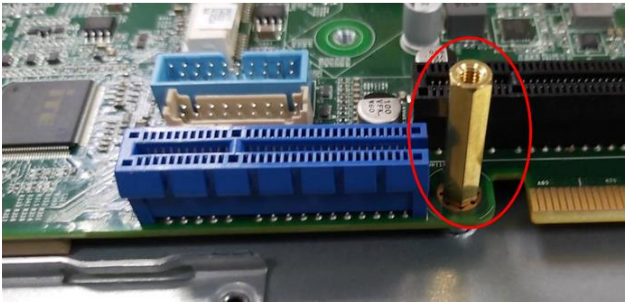
Step 1: Remove the upper panel of the chassis by unscrewing seven (7) retaining screws.



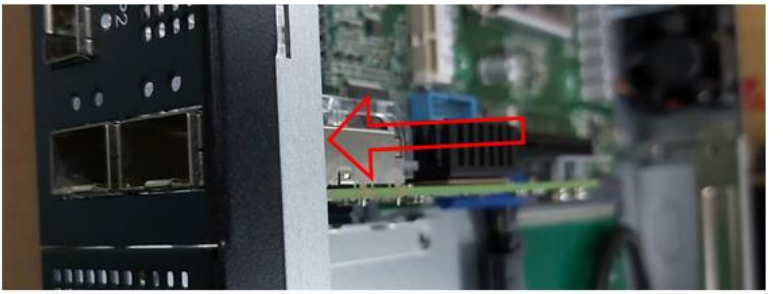
Step 2: Attach the bracket to the PER-T639 card with two screws, as shown:

Step 3: Remove the punchouts at the front of the system.

Step 4: Attach the M3*22mm spacer to the main board as shown.



Step 5: Insert the PER-T639 card by first aligning the SFP+ ports with the punchouts, then inserting the card into the slot. Finally, secure the card by fastening the bracket to the standoff with a screw.

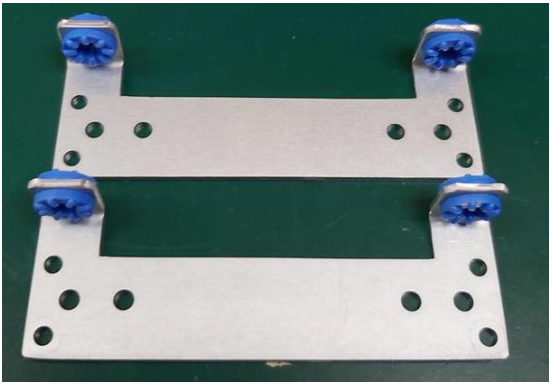


2.8 2.5″ Drive Installation

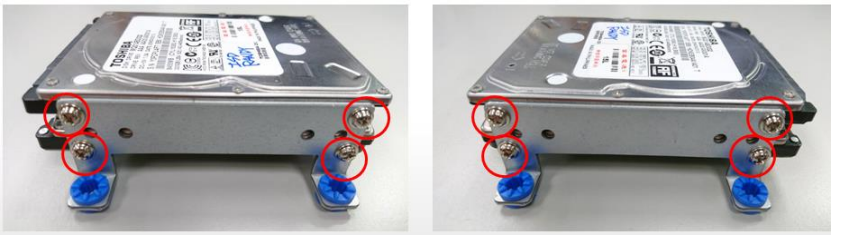
This section details the steps of how to install the dual 2.5″ drive assembly for the FWS-7840. Before beginning installation make sure the system is powered down and the power sources are disconnected. You will need to have your 2.5″ drives and 2.5″ drive assembly brackets ready to install.

Step 1: Remove the upper panel of the chassis by unscrewing seven (7) retaining screws.

Step 2: Place the bracket cushions on the drive brackets as shown.

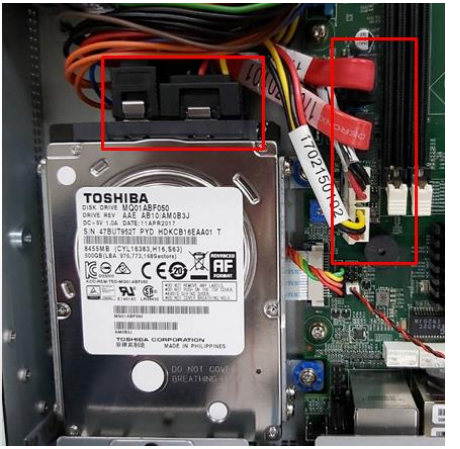


Step 3: Mount the two 2.5" drives onto the drive brackets as shown, with four screws on each side.



Step 4: Mount the assembly onto the chassis, securing with four screws.

Step 5: Attach the SATA and SATA Power cables, first to the bottom drive, then the top drive.

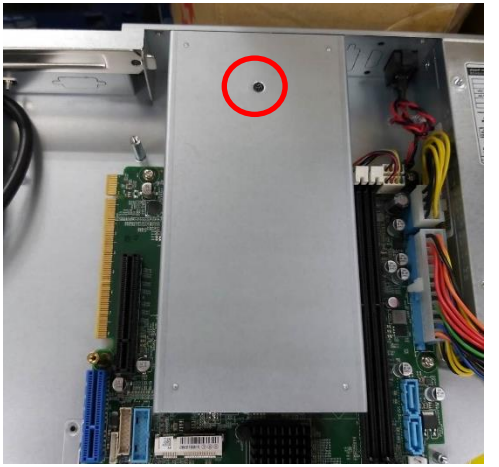


2.9 CPU and Heatsink Installation

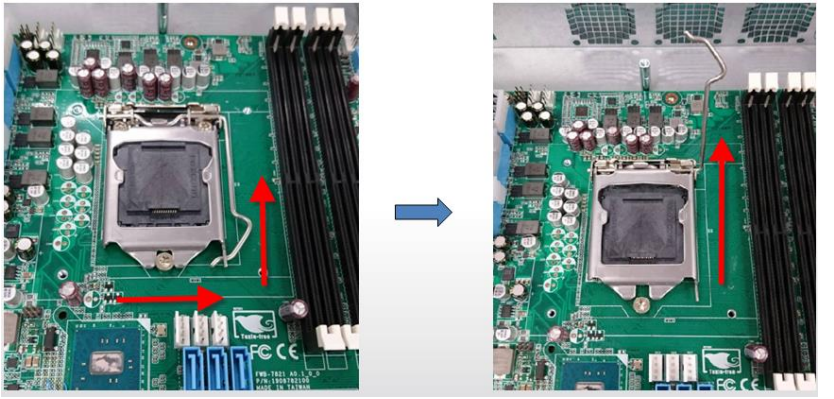
This section details the steps of how to install the CPU and heatsink for the FWS-7840. Before beginning installation make sure the system is powered down and the power sources are disconnected. Make sure you have your CPU and heatsink ready to install.

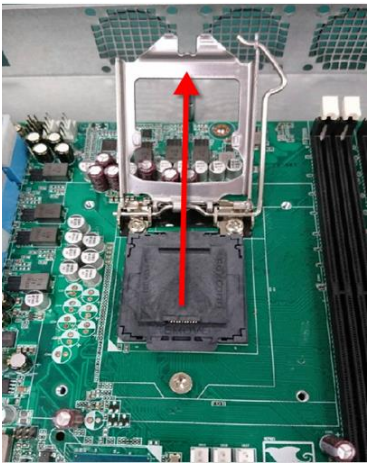
Step 1: Remove the upper panel of the chassis by unscrewing seven (7) retaining screws.

Step 2: Remove the fan duct by loosening the fastening screw.

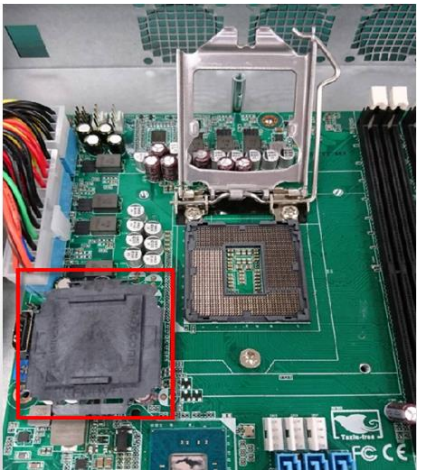


Step 3: Unlock the CPU retaining bracket and lift up the bracket.

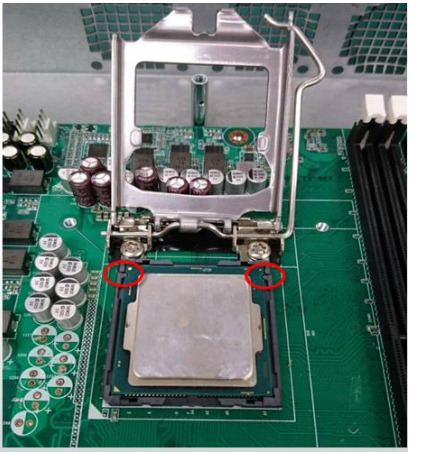




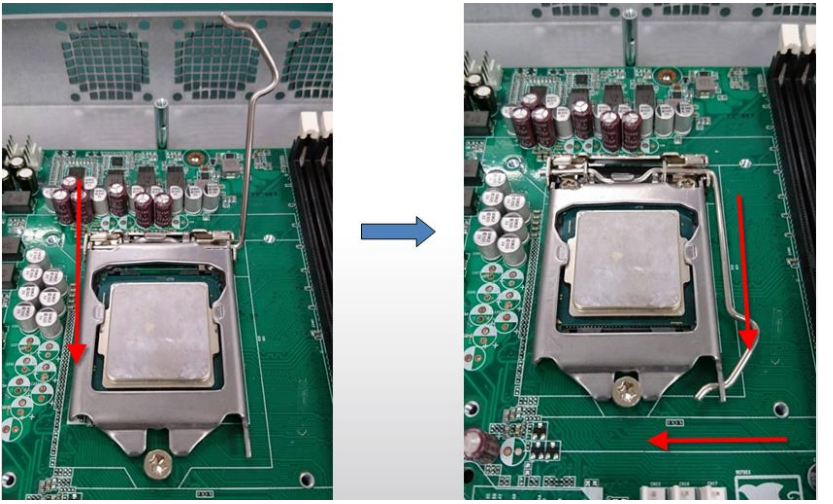
Step 4: Remove the plastic cover.



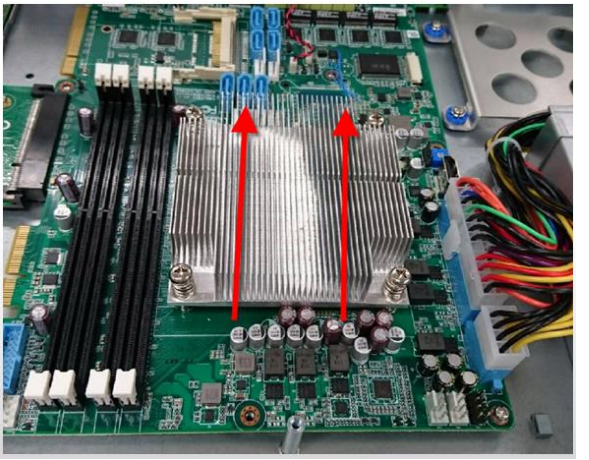
Step 5: Insert the CPU into the socket. Ensure the notches on the CPU line up correctly with the socket. If you haven't already, apply a thin layer of thermal paste to the top of the CPU.



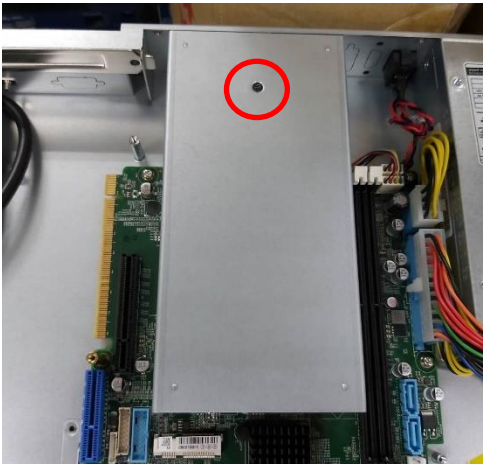
Step 6: Close and lock the CPU bracket in place.



Step 7: Place the heatsink and secure with four post screws. Ensure the heatsink is orientated so the fins are parallel to the airflow direction.



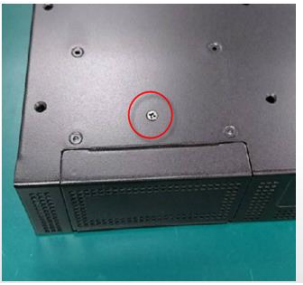
Step 8: Replace the air duct, securing with the screw from Step 2.



2.10 Installing NIM Modules

This section details the steps of how to install NIM modules for the FWS-7840. This applies for new installation, or removal/replacement of modules. Before beginning installation make sure the system is powered down and the power sources are disconnected.

Step 1: Loosen the retaining screw on the bottom of the chassis.



No NIM Module

Replacing NIM Module

Step 2: Remove the cover/old NIM module by sliding it out.

Step 3: Insert the new NIM Module (or cover) and secure with a screw on the bottom of the chassis.

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- System configuration was reset by Clear CMOS jumper
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

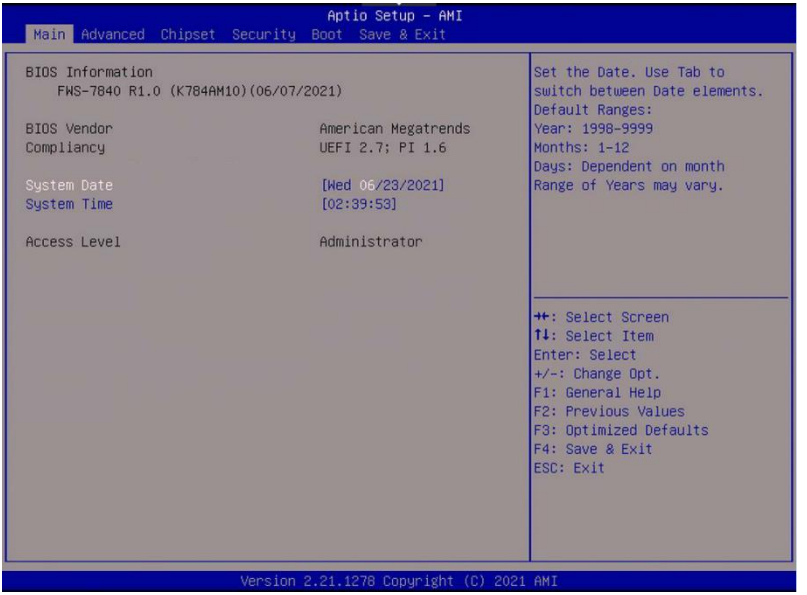
Chipset - Host bridge parameters.

Security – The setup administrator password can be set here

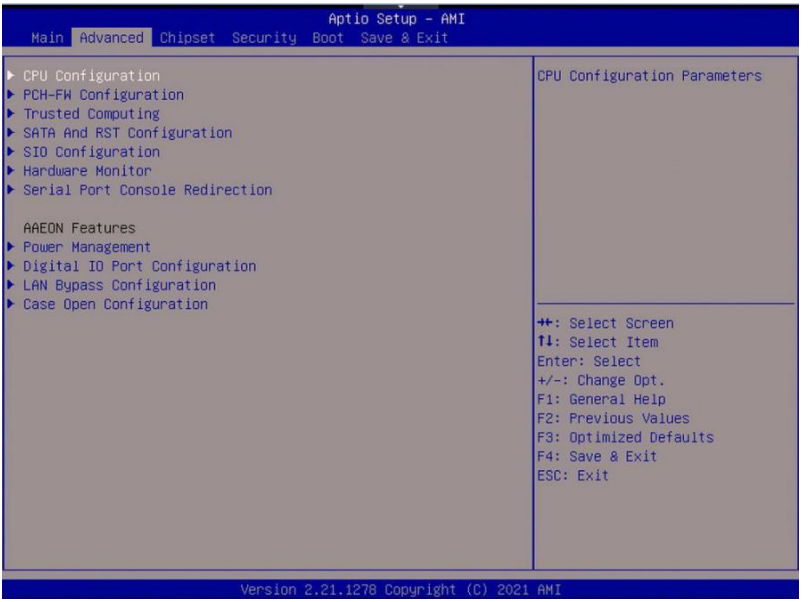
Boot – Enable/ Disable quiet Boot Option

Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main



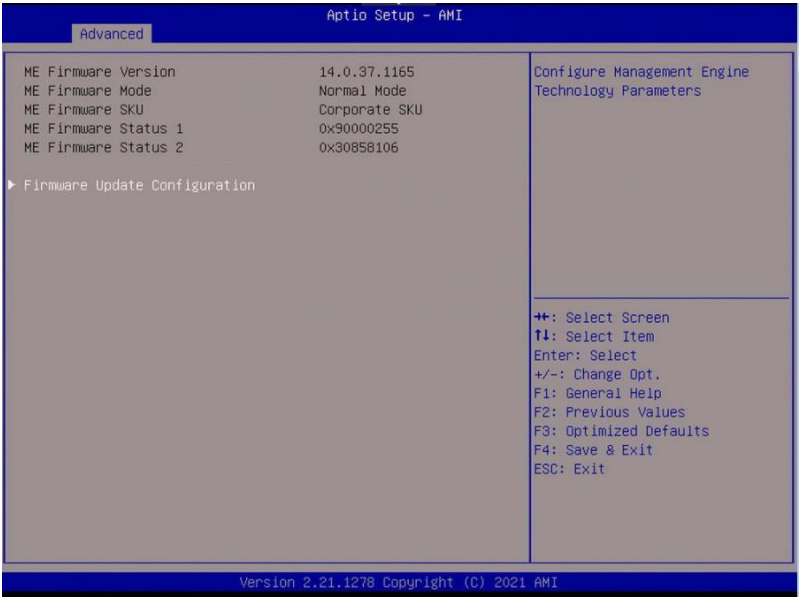
3.4 Setup Submenu: Advanced



3.4.1 CPU Configuration

Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1~5	
Number of cores to enable in each processor package.		
Hyper-Threading	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Hyper-Threading Technology		
Intel® Speed Shift Technology	Disable	
	Enable	Optimal Default, Failsafe Default
Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware-controlled P-states.		

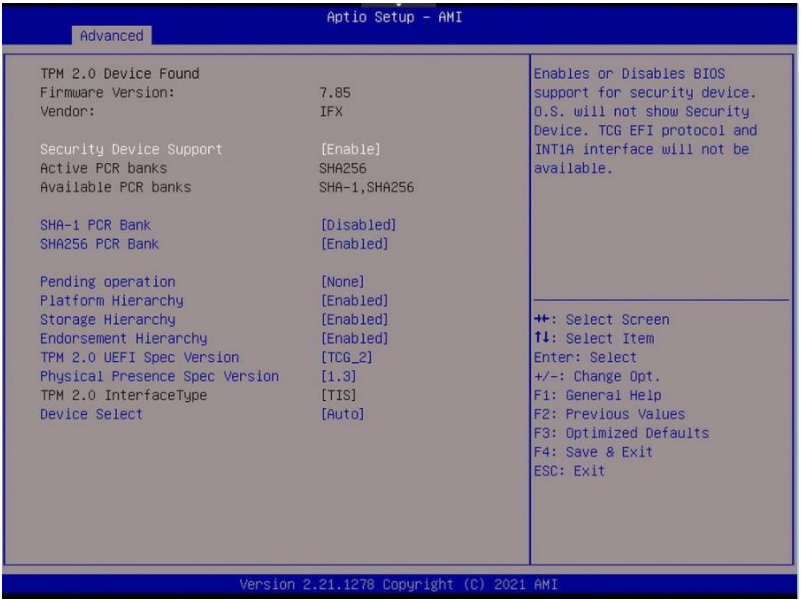
3.4.2 PCH-FW Configuration



3.4.2.1 Firmware Update Configuration

Options Summary		
Me FW Image Re-Flash	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/ Disable ME FW Update function		

3.4.3 Trusted Computing



Options Summary		
Security Deice Support	Enable	Optimal Default, Failsafe Default
	Disable	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA256 PCR Bank.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

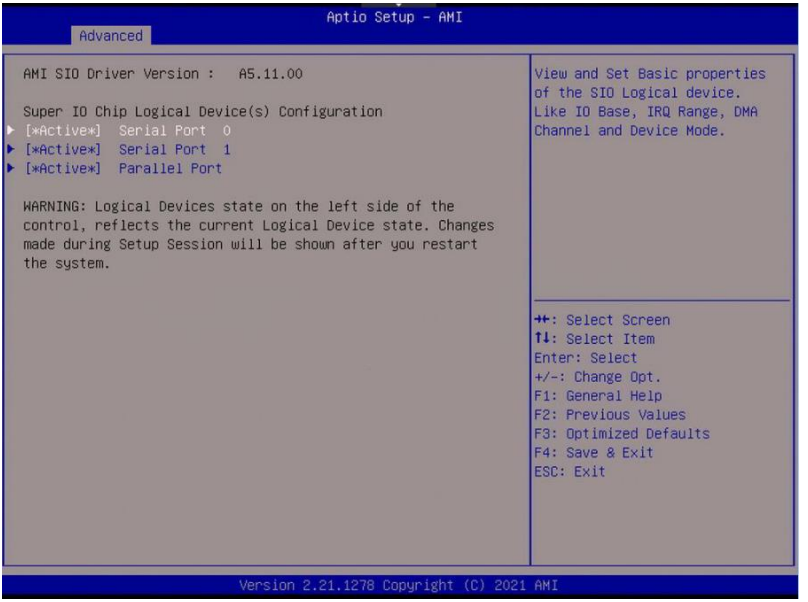
Table continues on Next Page...

Options Summary		
Platform Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Endorsement Hierarchy		
TPM 2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCH2 Spec Version Support. TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.3	Optimal Default, Failsafe Default
	1.2	
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3		
Device Select	Auto	Optimal Default, Failsafe Default
	TPM 1.2	
	TPM 2.0	
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.		

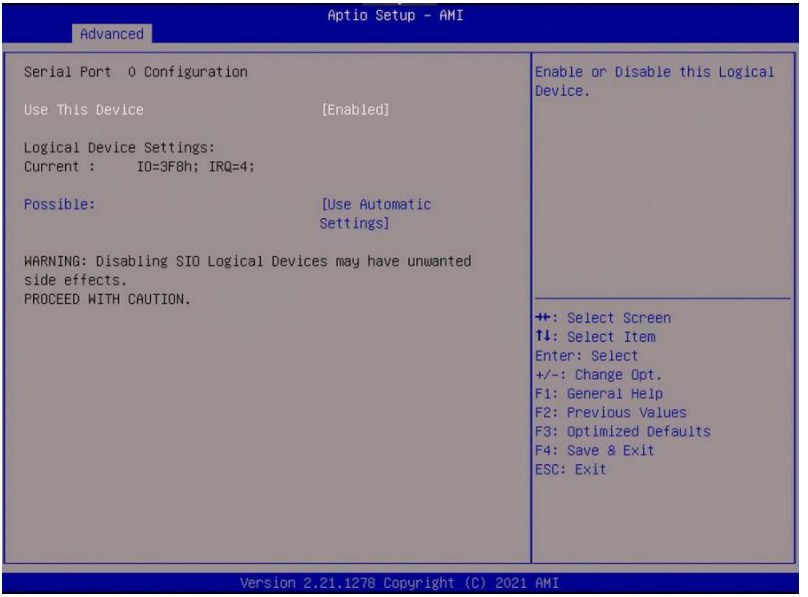
3.4.4 SATA And RST Configuration

Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable SATA Device.		
SATA Mode Selection	AHCI	Optimal Default, Failsafe Default
	Intel RST Premium With Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.5 SIO Configuration

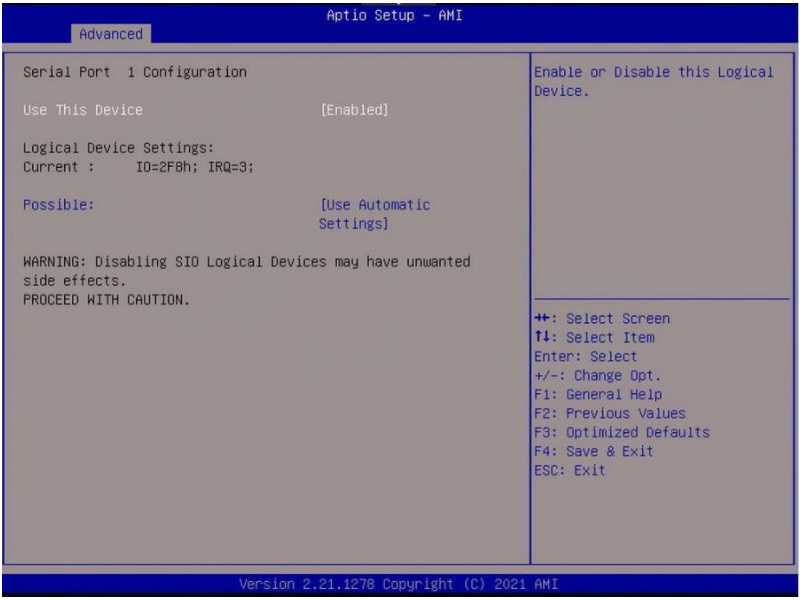


3.4.5.1 Serial Port 0 Configuration



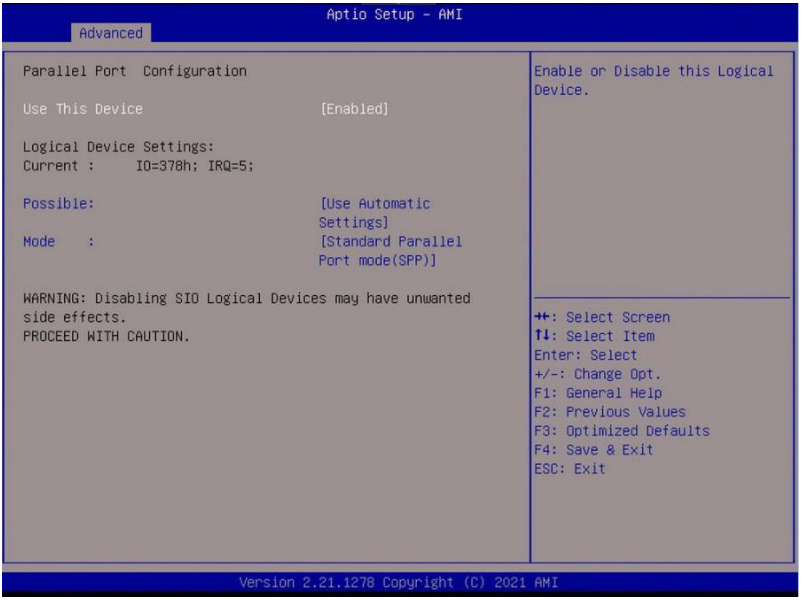
Options Summary		
Use This Device	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Allow user to change device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.5.2 Serial Port 1 Configuration



Options Summary		
Use This Device	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Allow user to change device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.5.3 Parallel Port Configuration



Options Summary		
Use This Device	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=378h; IRQ=5;	
	IO=378h; IRQ=5,6,7,10,11,12;	
	IO=278h; IRQ=5,6,7,10,11,12;	
	IO=3BCh; IRQ=5,6,7,10,11,12;	
Allow user to change device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode	Standard Parallel Port mode(SPP)	Optimal Default, Failsafe Default
	EPP Mode	
	ECP Mode	
	EPP mode & ECP mode	
Change Parallel Port mode. Some of the Modes required a DMA resource. After Mode changing, Reset the System to reflect actual device settings.		

3.4.6 Hardware Monitor

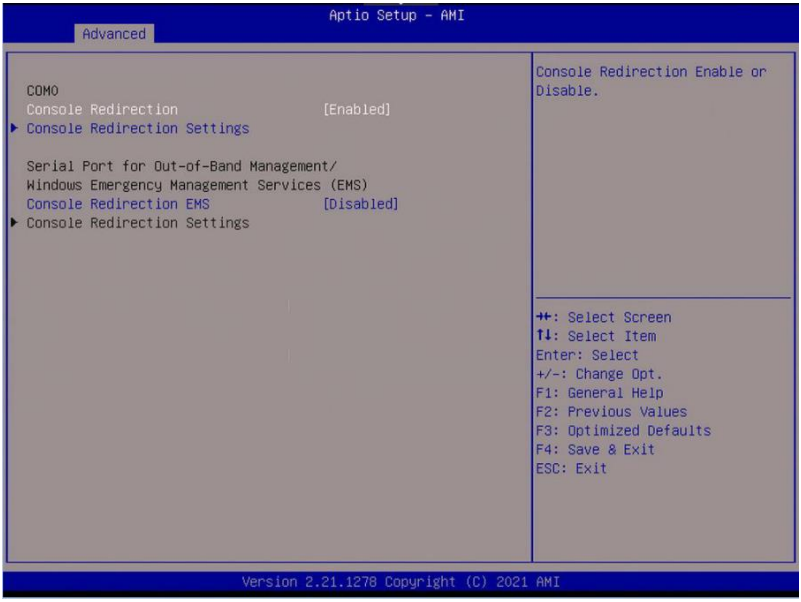
3.4.6.1 Smart Fan Function

3.4.6.1.1 Fan 1/ 2 Setting

Options Summary		
Smart Fan 1/2 Mode	Software Mode	Optimal Default, Failsafe Default
	Automatic Mode	
Smart Fan Mode Select		
Manual PWM Setting	127	Optimal Default, Failsafe Default
	0~255	
Manual Mode: Fan will work with this Manual PWM Value		
Temperature select	CPU Temperature (DTS)	Optimal Default, Failsafe Default
	System Temperature	
Temperature input selection		
Fan off temperature limit	16	Optimal Default, Failsafe Default
Fan will off when temperature lower than this limit		
Fan start temperature limit	32	Optimal Default, Failsafe Default
Fan will work when temperature higher than this limit		

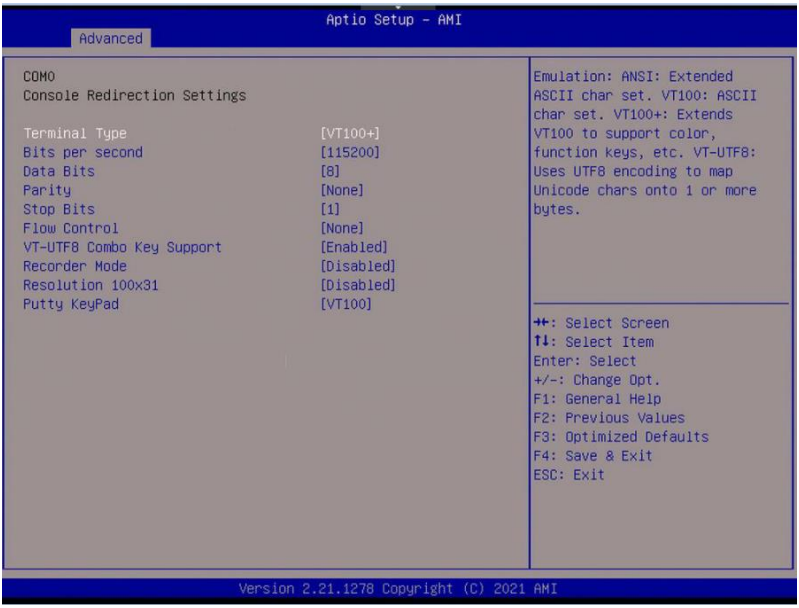
Options Summary		
Fan full Speed Temperature limit	127	Optimal Default, Failsafe Default
Fan will full speed when temperature higher than this limit		
Fan start PWM	128	Optimal Default, Failsafe Default
Fan will start with this PWM value		

3.4.7 Serial Port Console Redirection



Options Summary		
Console Redirection	Enabled	Optimal Default, Failsafe Default
	Disabled	
Console Redirection Enable or Disable		
Console Redirection Settings		
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.		
Console Redirection EMS	Enabled	Optimal Default, Failsafe Default
	Disabled	
Console Redirection Enable or Disable		

3.4.7.1 COM0 Console Redirection Settings

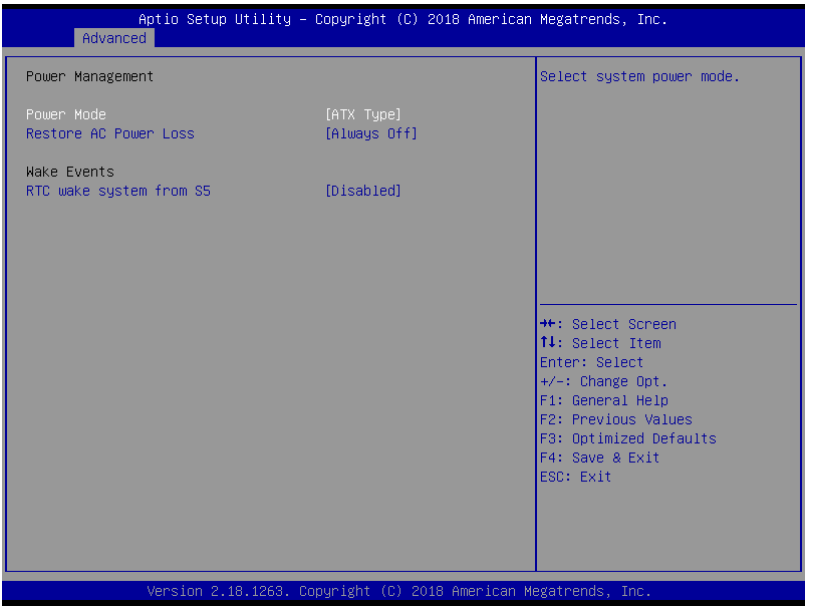


Options Summary		
Terminal Type	VT100	
	VT100+	Optimal Default, Failsafe Default
	VT-UTF8	
	ANSI	
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Options Summary		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. **Even**: parity bit is 0 if the num of 1's in the data bits is even. **Odd**: parity bit is 0 if the num of 1's in the data bits is odd. **Mark**: parity bit is always 1. **Space**: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	

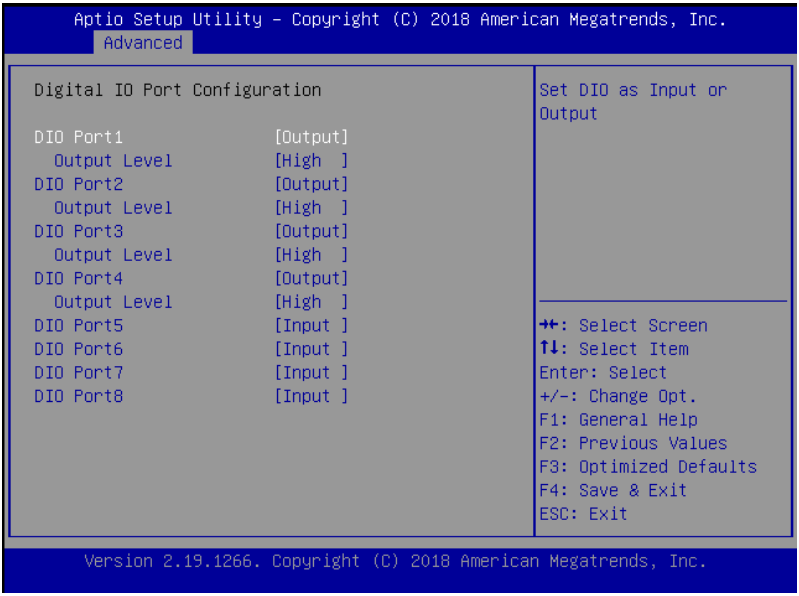
Options Summary
Select FunctionKey and KeyPad on Putty.

3.4.8 Power Management



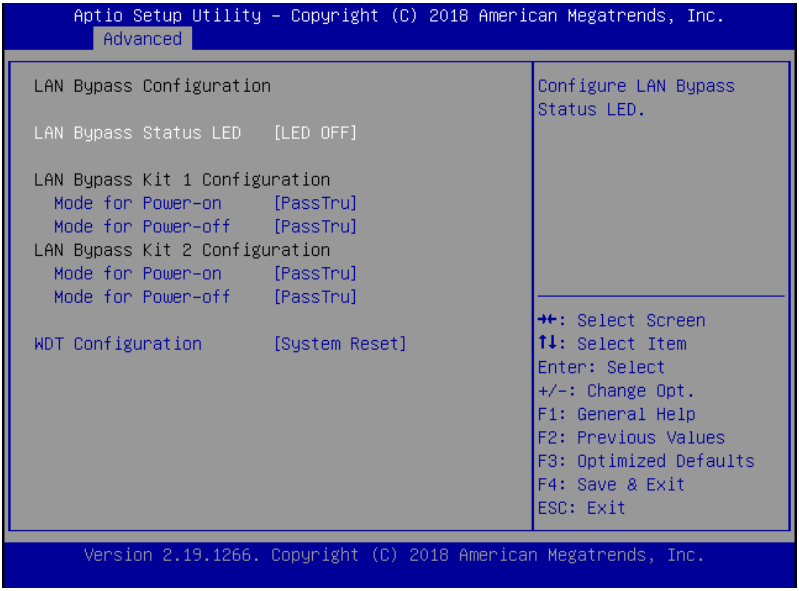
Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time: System will wake on the hr :: min :: sec specified Dynamic Time : System will wake on the current time + Increase minutes(s). Bypass: BIOS will not control RTC wake function during system shutdown		

3.4.9 Digital IO Port Configuration



Options Summary		
DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input or Output		

3.4.10 LAN Bypass Configuration



Options Summary		
Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
LAN Bypass Status LED		
Mode for Power-on	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through)		
Mode for Power-off	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through)		

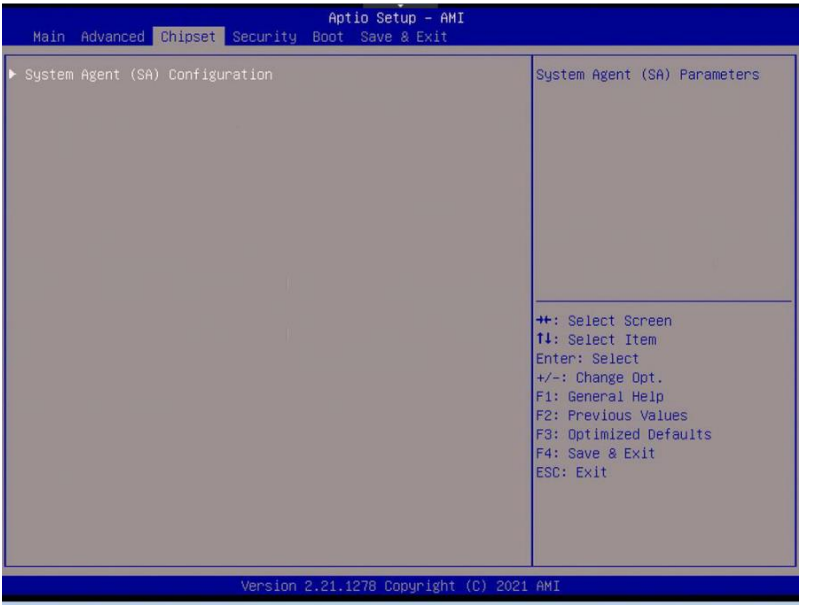
Table continues on Next Page...

Options Summary		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure LAN kit behavior when WDT is triggered. (Bypass/Pass Through)		

3.4.11 Case Open Configuration

Options Summary		
Case Open Warning	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Clear	
Case Open detecting function		

3.5 Setup Submenu: Chipset



3.5.1 System Agent (SA) Configuration

Options Summary		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
VT-d capability		

3.6 Setup Submenu: Security

Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

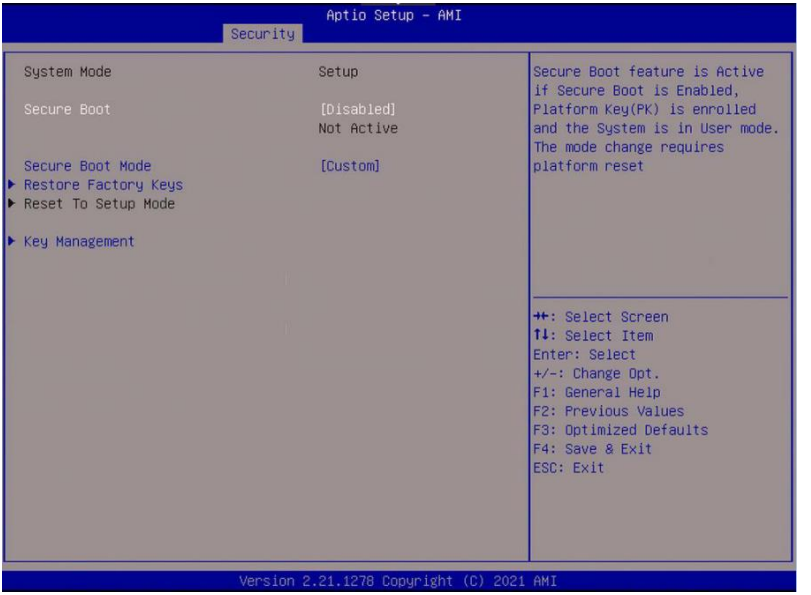
Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

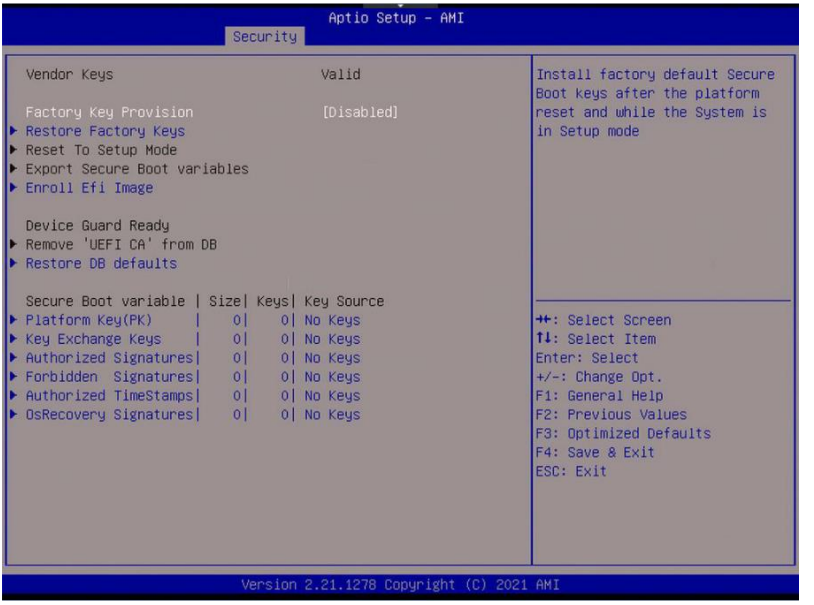
.

3.6.1 Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled, and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		

3.6.1.1 Key Management



Options Summary		
Provision Factory Defaults	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode		
Restore Factory Keys	Force System to User Mode. Install factory default Secure Boot key databases.	
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	
Restore DB defaults	Restore DB variable to factory defaults	

Secure Boot Variables

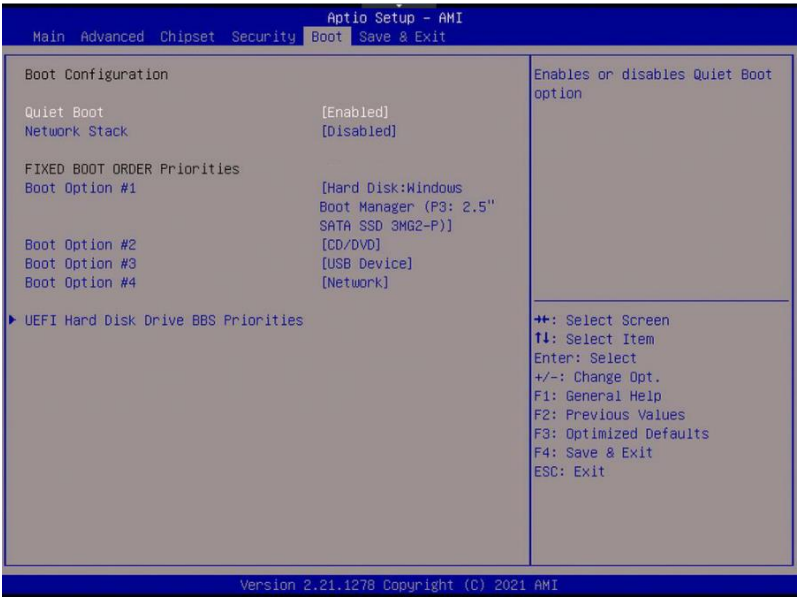
Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:
   a) EFI_SIGNATURE_LIST
   b) EFI_CERT_X509 (DER encoded)
   c) EFI_CERT_RSA2048 (bin)
   d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/COFF Image (SHA256)

Key Source:

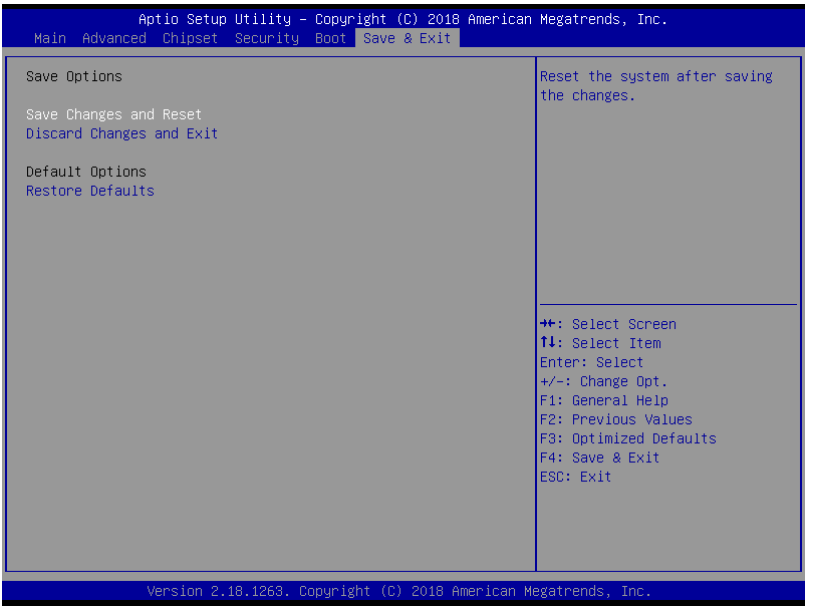
Default, External, Mixed

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		
UEFI Hard Disk Drive BBS Priorities.	Specifies the Boot Device Priority sequence from available UEFI Hard Disk Drives.	

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the FWS-7840 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/rackmount-network-appliance-fws-7840

Download the driver(s) you need and follow the steps below to install them.

Step 1 – LAN Drivers

1. Open the **Step 1 - LAN** folder.
2. Extract the archived file igb-5.7.2.tar.gz
3. Extract the archived file i40e-2.16.11.tar.gz
4. Follow instructions in README

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID   WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*******************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       Switch(SIOIndex){
              Case 0x2E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0x55);
                        Break;
              Case 0x4E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0xAA);
                     Break;
       }
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0x02);
       IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}
*****************************************************************************
```

```
*******************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*******************************************************************************
```

Appendix B

Standard LAN Bypass Platform Setting

B.1 Status LED

The FWS-7840 features a Status LED indicator which can be configured using the AAEON SDK. The Status LED can be programed to indicate different system statuses. This section provides information on how to program and configure the Status LED.

B.1.1 Status LED Configuration

Table 1 : Truth Table of Status LED			
STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table 2 : Status LED relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

B.1.2 Sample Code

```
*****************************************************************************************
****
#define Byte  CPLD_SLAVE_ADDRESS      //This parameter is represented from Note1
#define Byte  OFFSET                  //This parameter is represented from Note2
*****************************************************************************************
****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
```

```
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
**********************************************************************************************
****
```

B.2 LAN Bypass

The FWS-7840 provides a LAN Bypass kit, allowing uninterrupted network traffic even if a single in-line appliance is shut down or hangs. This section details how to configure and program the LAN Bypass.

B.2.1 LAN Bypass Configuration

Table 1 : ID Select table of LAN kit				
LAN_ID3	LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	0	LAN Kit 1 Selected
0	0	0	1	LAN Kit 2 Selected
0	0	1	0	LAN Kit 3 Selected
...				...
1	1	1	1	LAN Kit 16 Selected

Table 2 : LAN Bypass relative register table	
Function	Description
LAN_ID3 LAN_ID2 LAN_ID1 LAN_ID0	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3 : LAN Bypass relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

****

B.2.2 Sample Code

```
*****************************************************************************************
****
#define Byte  CPLD_SLAVE_ADDRESS      //This parameter is represented from Note1
#define Byte  OFFSET                  //This parameter is represented from Note2
*****************************************************************************************
****
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)      // Pass Through
        bData = bData & 0xBF;
else                                  // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)      // Pass Through
```

```
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)   // Reset
        bData = bData & 0xEF;
else                                    // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*********************************************************************************
```

B.3 Software Reset Button (General Propose Input)

The FWS-7840 provides a general purpose input button which can be configured by the AAEON SDK. This section details how to configure and program this feature.

B.3.1 Software Reset Button Configuration

Table 2 : Software Reset Button register table	
Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1 : Soft Reset Button register mapping table				
	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

B.3.2 Sample Code

```
*********************************************************************************
#define Word BTN_STS          //This parameter is represented from Note1
#define Byte  BTN_STS_R       //This parameter is represented from Note2
*********************************************************************************
Byte   GET_Value (Word IoAddr, Byte BitNum,Byte Value){
        BYTE   TmpValue;

        TmpValue = inportb (IoAddr);
         return   (TmpValue & (1 << BitNum))
}
*********************************************************************************
VOID   Main(){
        Byte RstBtn;

        RstBtn = GET_Value (BTN_STS, BTN_STS_R);          // Active Low
}
*********************************************************************************
```

Appendix C

Digital I/O Ports

C.1 Digital I/O Register

Table 2: SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	Register	BitNum	Note
GPIO1 Direction	0x07	0xC8	1	0: input, 1: output
GPIO2 Direction	0x07	0xC8	2	
GPIO3 Direction	0x07	0xC8	4	
GPIO4 Direction	0x07	0xC8	5	
GPIO5 Direction	0x07	0xCA	4	
GPIO6 Direction	0x07	0xCA	5	
GPIO7 Direction	0x07	0xCD	3	
GPIO8 Direction	0x07	0xCB	7	

Table 4: Digital GPIO Status relative IO address table			
	IO Address	BitNum	Note
GPIO1 State	0x0A00	1	0: low, 1: high
GPIO2 State	0x0A00	2	
GPIO3 State	0x0A00	4	
GPIO4 State	0x0A00	5	
GPIO5 State	0x0A02	4	
GPIO6 State	0x0A02	5	
GPIO7 State	0x0A05	3	
GPIO8 State	0x0A03	7	

C.2 Digital I/O Sample Program

```
**********************************************************************
// SuperIO relative definition (Please reference to Table 2)
#define  SIOIndex  0x2E
#define  SIOData   0x2F
#define  DIOLDN    0x07
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define  DirReg1     0xC8      // GPIO1- GPIO4
#define  DirReg2     0xCA      // GPIO5-GPIO6
#define  DirReg3     0xCD      // GPIO7
#define  DirReg4     0xCB      // GPIO8
   #define  InputPin    0x00
   #define  OutputPin   0x01
#define  StatusReg1   0xA00      // GPIO1-GPIO4
#define  StatusReg2   0xA02      // GPIO5-GPIO6
#define  StatusReg3   0xA05      // GPIO7
#define  StatusReg4   0xA03      // GPIO8
   #define  PinLow      0x00
   #define  PinHigh     0x01
#define  Pin1Bit     0x00
#define  Pin2Bit     0x01
#define  Pin3Bit     0x02
#define  Pin4Bit     0x03
#define  Pin5Bit     0x04
#define  Pin6Bit     0x05
#define  Pin7Bit     0x06
#define  Pin8Bit     0x07
**********************************************************************
```

```
*************************************************************************
VOID  Main(){
     Boolean PinStatus ;

     // Procedure : AaeonReadPinStatus
     // Input :
     //   Example, Read Digital I/O Pin 3 status
      // Output :
      //  InputStatus :
      //        0: Digital I/O Pin level is low
      //        1: Digital I/O Pin level is High
     PinStatus = AaeonReadPinStatus(Pin3Bit);

     // Procedure : AaeonSetOutputLevel
     // Input :
     //   Example, Set Digital I/O Pin 2 to high level
     AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*************************************************************************
```

```
*************************************************************************
Boolean  AaeonReadPinStatus(byte PinBit){
     Boolean PinStatus ;
      If (PinBit < Pin5Bit) {
         If (PinBit < Pin3Bit) {
           PinBit + 1;
         } else {
           PinBit + 2;
         }
         PinStatus = IoBitRead(StatusReg1, PinBit);
      } else if ((PinBit > Pin4Bit) && (PinBit < Pin7Bit))
      {
         PinStatus = IoBitRead(StatusReg2, (PinBit - PinBit4) + 3);
      } else if (PinBit == Pin7Bit)
      {
         PinStatus = IoBitRead(StatusReg3,3);
      } else
      {
          PinStatus = IoBitRead(StatusReg4,7);
      }
     Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte PinBit, byte Value){
     ConfigDioMode(PinBit, OutputPin);
      If (PinBit < Pin5Bit) {
         If (PinBit < Pin3Bit) {
           PinBit + 1;
         } else {
           PinBit + 2;
         }
         IoBitSet (StatusReg1, PinBit, Value);
      } else if ((PinBit > Pin4Bit) && (PinBit < Pin7Bit))
      {
         IoBitSet (StatusReg2, (PinBit - PinBit4) + 3, Value);
      } else if (PinBit == Pin7Bit) {
         IoBitSet (StatusReg3, 3, Value);
     } else {
         IoBitSet (StatusReg4, 7, Value);
      }
}
*************************************************************************
```

```
*********************************************************************
VOID  SIOEnterMBPnPMode(){
     IOWriteByte(SIOIndex, 0x87);
     IOWriteByte(SIOIndex, 0x01);
     IOWriteByte(SIOIndex, 0x55);
     IOWriteByte(SIOIndex, 0x55);
}

VOID  SIOExitMBPnPMode(){
     IOWriteByte(SIOIndex, 0x02);
     IOWriteByte(SIOData, 0x01);
}

VOID  SIOSelectLDN(byte LDN){
      IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
     IOWriteByte(SIOData, LDN);
}
*********************************************************************
```

```
**************************************************************************
Boolean  IoBitRead(byte Address, byte BitNum){
     Byte TmpValue;

      TmpValue = IOReadByte(Address);
     TmpValue &= (1 << BitNum);
     If(TmpValue == 0)
          Return 0;
     Return 1;
}
Boolean  IoBitSet(byte Address, byte BitNum, Byte Value){
     Byte TmpValue;

      TmpValue = IOReadByte(Address);
     TmpValue &= ~(1 << BitNum);
     TmpValue |= (Value & 0x01) << BitNum;
      IOWriteByte(Address, TmpValue);

     Return 1;
}
VOID  ConfigDioMode(byte PinBit, byte Mode){
     Byte TmpValue;

     SIOEnterMBPnPMode();
      SIOSelectLDN(DIOLDN);
      If (PinBit < Pin5Bit) {
         If (PinBit < Pin3Bit) {
           PinBit + 1;
         } else {
           PinBit + 2;
         }
         IOWriteByte(SIOIndex, DirReg1);
         TmpValue = IOReadByte(SIOData);
         TmpValue &= (1 << PinBit);
         TmpValue |= (Mode << PinBit);
         IOWriteByte(SIOData, TmpValue);
      } else if ((PinBit > Pin4Bit) && (PinBit < Pin7Bit))
      {
         IOWriteByte(SIOIndex, DirReg2);
         TmpValue = IOReadByte(SIOData);
         TmpValue &= ~(1 << ((PinBit – Pin4Bit) + 3));
```

```
        TmpValue |= (Mode << ((PinBit - Pin4Bit) + 3));
        IOWriteByte(SIOData, TmpValue);
      }
      } else if (PinBit == Pin7Bit) {
        IOWriteByte(SIOIndex, DirReg3);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << 3));
        TmpValue |= (Mode << 3));
        IOWriteByte(SIOData, TmpValue);
      } else
      {
        IOWriteByte(SIOIndex, DirReg4);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << 7));
        TmpValue |= (Mode << 7));
        IOWriteByte(SIOData, TmpValue);
      }
      SIOExitMBPnPMode();
}
**************************************************************************
```