



FWS-7831

Network Appliance

User's Manual 4th Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7831	1
● 2.5" HDD Bay	2
● SATA Cable	2
● SATA Power Cable	2
● Console Cable	1
● Ear Bracket Kit	1
● CPU Heatsink	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period))：10 年

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON System

QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU and Memory	×	○	○	○	○	○
Hard Disk	×	○	○	○	○	○
LCD Modules	×	○	○	○	○	○
CD-ROM/DVD-ROM	×	○	○	○	○	○
Touch Modules	×	○	○	○	○	○
Power	×	○	○	○	○	○
Battery	×	○	○	○	○	○
The table is prepared in accordance with the provisions of SJ/T 11364. ○ : Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572. × : Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1). EFUP (Environment Friendly Use Period) value: 10 years. Notes: 1. This product defined period of use is under normal condition. 2. In above part, CPU/Memory/ Hard Disk/CD-ROM/DVD-ROM/ Power are optional. 3. In above part, LCD Modules/ Touch Modules are for all-in-one product model.						

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Chapter 1

Product Specifications

1.1 Specifications

Platform

Form Factor	1U Rackmount Network Platform
Processor	Intel® Xeon® E-2400 Processors (Intel® C246 Chipset) 8 th Generation Intel® Core™/Celeron® Processors (Intel® H310 Chipset)
Chipset	Intel® C246/H310 Chipset
System Memory	DDR4 1600/1866/2133 SODIMM x 2, up to 64GB, ECC

Network

Ethernet	Intel® Ethernet Controller I210, GbE x 8 (Intel® H310 Chipset) Intel® Ethernet Controller I210, GbE x 6 + SFP x 2 (Intel® C246 Chipset)
Bypass	2 Pairs
NIM Slot	Requires configuration via Riser Card

Display

Graphic Controller	Intel® UHD Graphics 630
Connector	HDMI x 1 (Optional)

Storage

HDDs	Internal 2.5" HDD Bay x 2 or 3.5" HDD Bay x 1 (not compatible with optional NIM)
CF/CFast/mSATA	mSATA

Expansion

PCIe slot	—
Mini-PCIe slot	Mini Card x 1 (PCIe [x1] + mSATA)
IPMI	—
Keyboard and Mouse	N/A
USB	USB 3.2 Gen 1 x 2

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	GPIO Programmable push button x 1
TPM	TPM 2.0 (Optional)
GPIO	4-bit Input, 4-bit Output
FAN	2
MTBF (Hours)	362,825
Color	Black

Environmental

Power Requirement	220W ATX PSU
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz / operation (2.5" HDD) 1.5 Grms/ 5 ~ 500Hz / non-operation
Dimension (W x D x H)	16.93" x 7.87" x1.73" (430mm x 200mm x 44mm)

I/O Interface

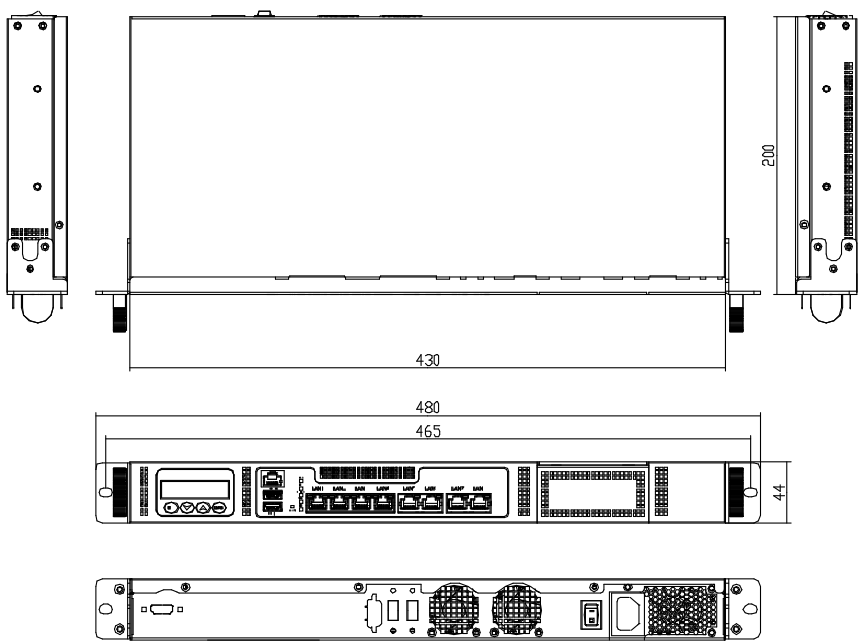
Front Panel	Power LED x 1
	Status LED x 1
	HDD Active LED x 1
	USB 3.2 Gen 1 x 2
	RJ-45 Console x 1
Rear Panel	AC Power Input x 1
	Power Switch x 1
	Rear Expansion Slot x 1 (Optional)

Chapter 2

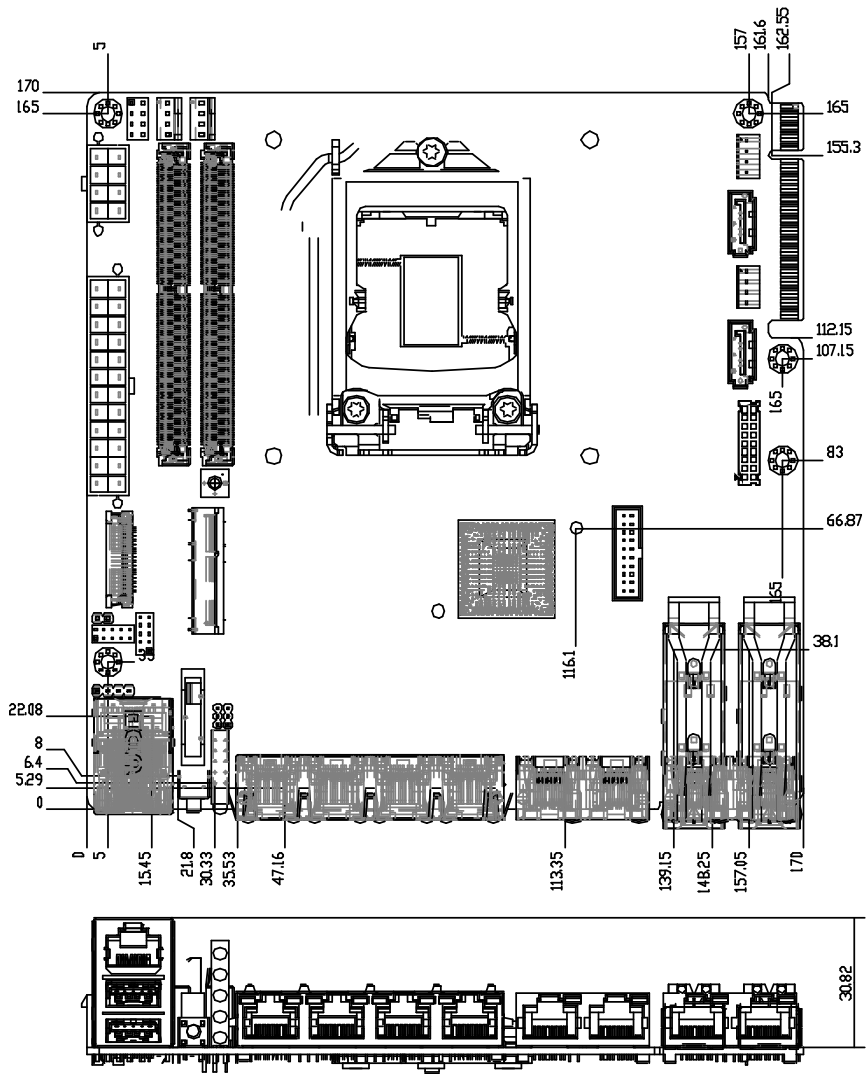
Hardware Information

2.1 Dimensions

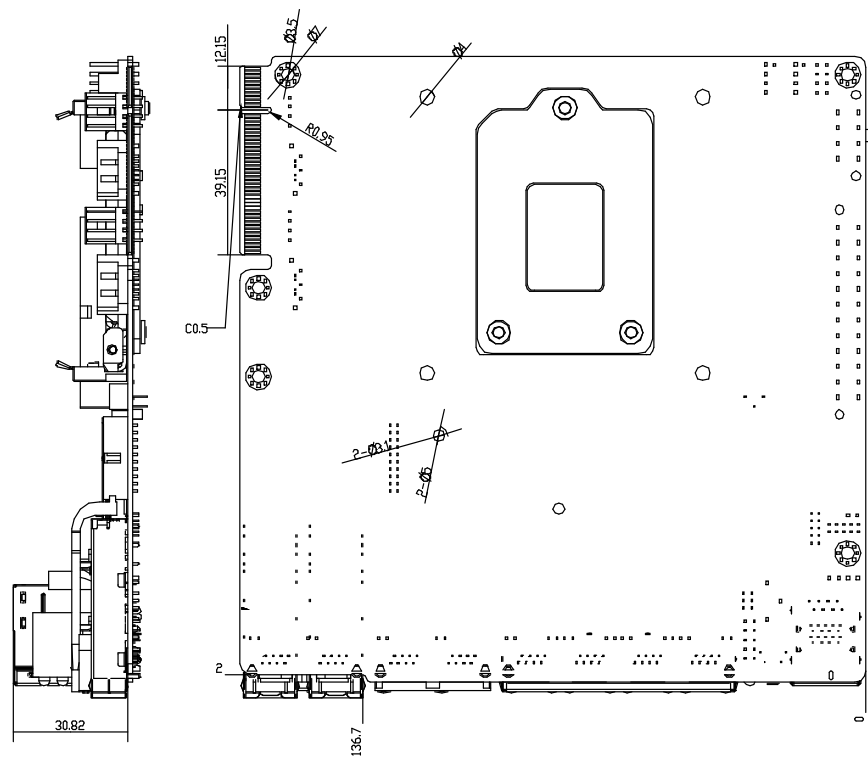
System



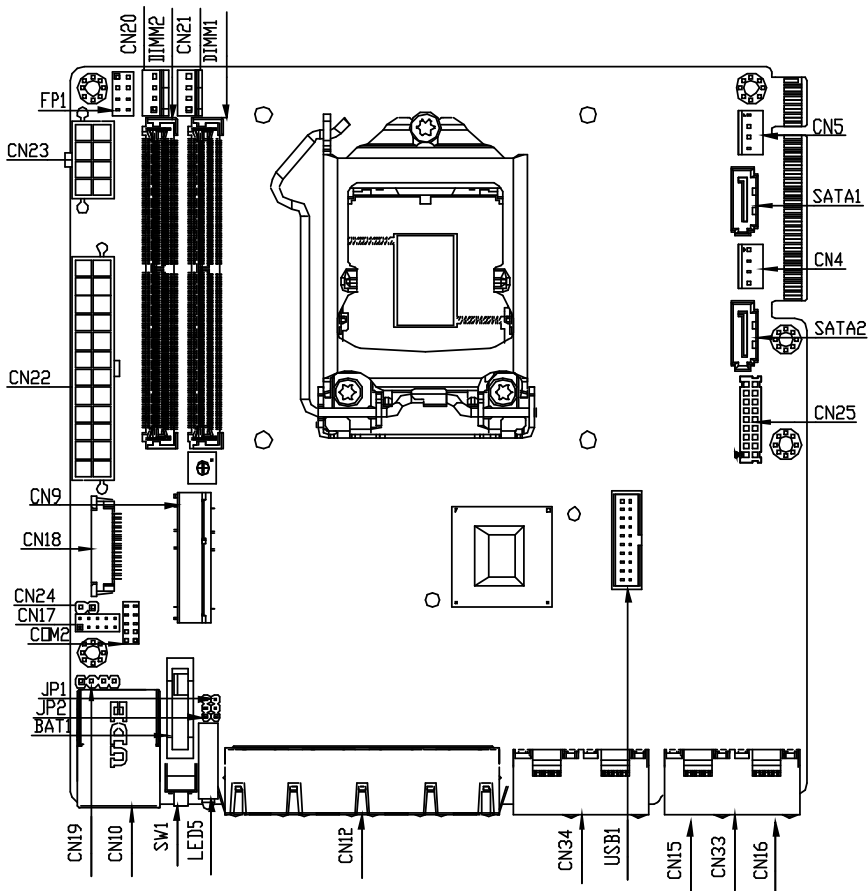
Component Side



Solder Side



2.2 Jumpers and Connectors

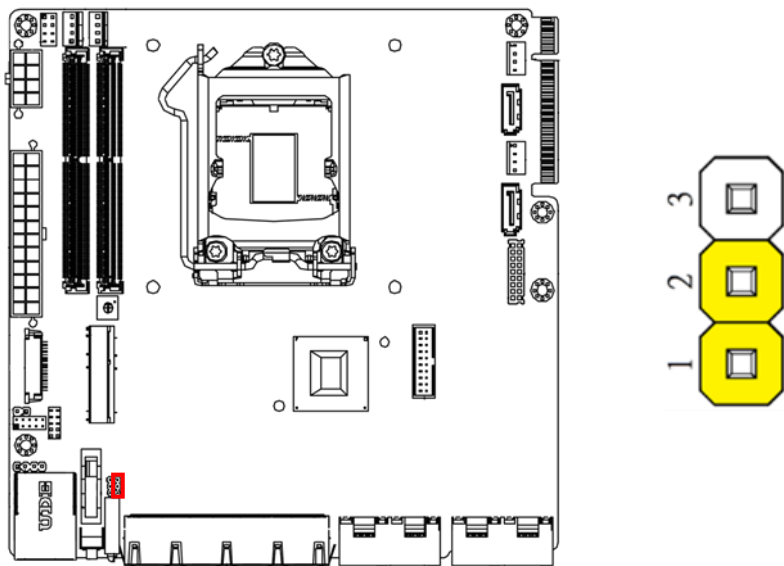


2.3 List of Jumpers

The FWS-7831 system board is configured with a number of jumpers which can be configured for your application. This section details those jumpers and their settings.

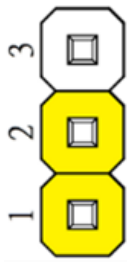
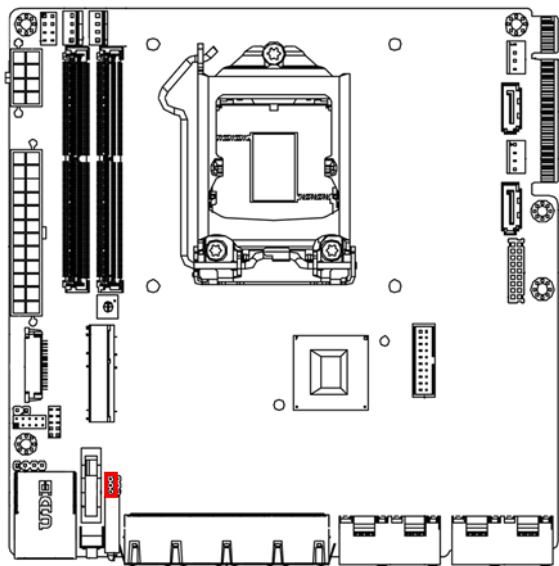
Label	Function
JP1	RTC Reset
JP2	Auto Power Button

2.3.1 RTC Reset (JP1)



Normal (Default)	1-2
Clear CMOS	2-3

2.3.2 Auto Power Button (JP2)



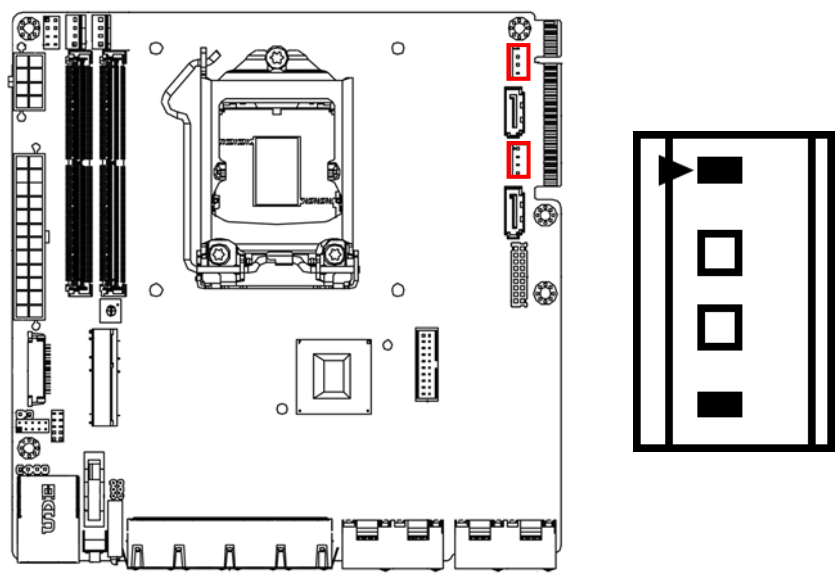
Don't use Auto PWRBTN (Default)	1-2
Use Auto PWRBTN	2-3

2.4 List of Connectors

The FWS-7831 system board is configured with a number of connectors which can be used for configuring your system and connecting with external modules. This section details those connectors and settings.

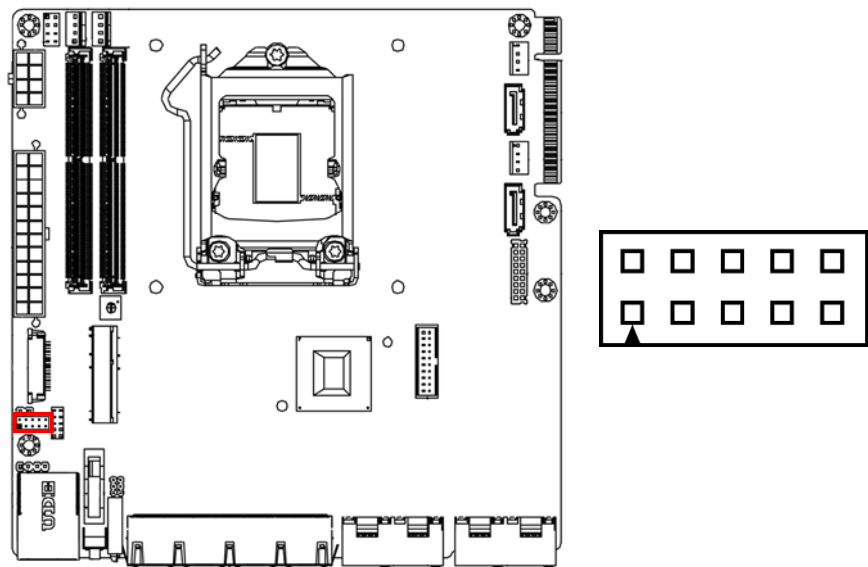
Label	Function
CN4	HDD Power Connector
CN5	HDD Power Connector
CN9	mSATA Socket
CN10	Dual USB 3.0 Port + RJ-45 Console Connector
CN12	LAN 1 ~ LAN 4 RJ-45
CN15	SFP Port 1
CN16	SFP Port 2
CN17	Digital I/O
CN18	LCM Connector
CN19	Key Pad Connector
CN20	SYS_FAN1
CN21	SYS_FAN2
CN22	24-Pin ATX Power Connector
CN23	8-Pin 12V Power Connector
CN24	Case Open Header
CN25	HDMI
CN33	LAN 7, LAN 8 RJ-45
CN34	LAN 5, LAN 6 RJ-45
COM2	COM Port
FP1	Front Panel Pin Header
SATA1	SATA
SATA2	SATA
USB1	USB 3.0 Port

2.4.1 HDD Power Connector (CN4 & CN5)



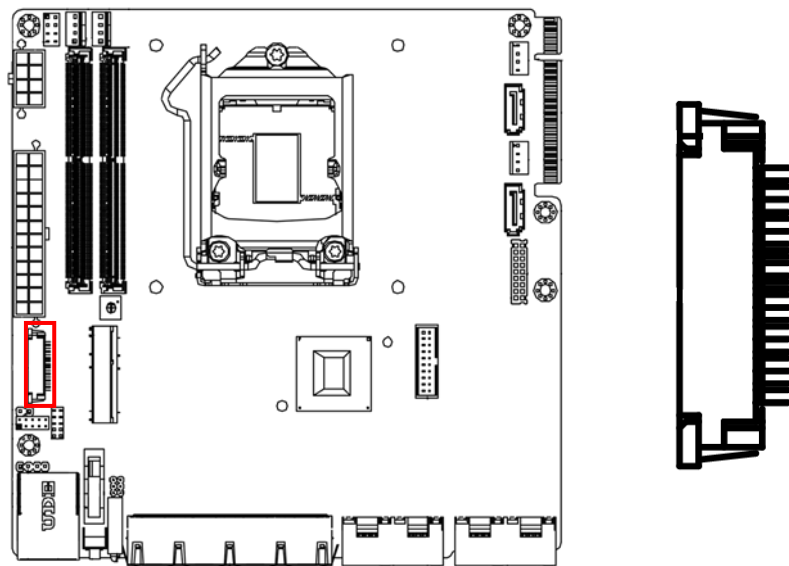
Pin	Signal	Signal Type
1	+12V	PWR
2	GND	GND
3	GND	GND
4	+5V	PWR

2.4.2 Digital I/O (CN17)



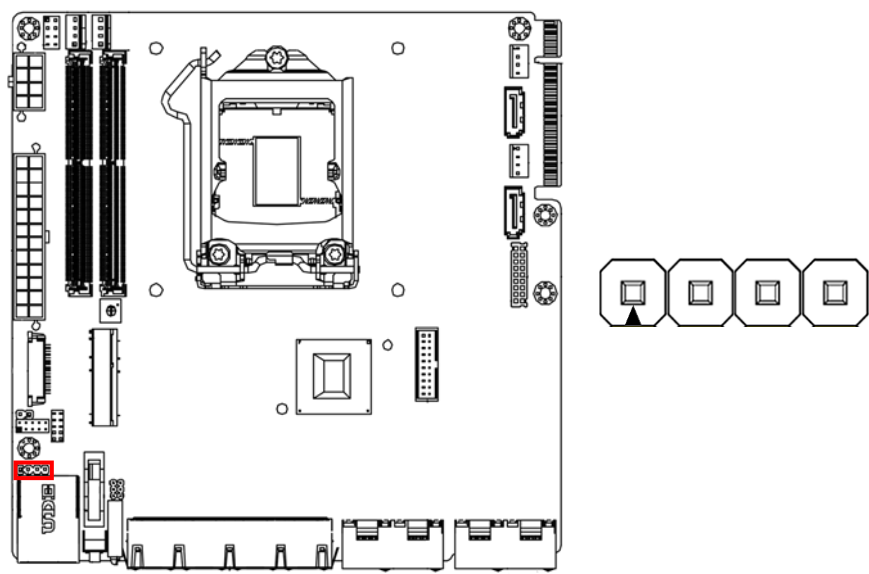
Pin	Signal	Signal Type
1	DIO0	Input / Output
2	DIO1	Input / Output
3	DIO2	Input / Output
4	DIO3	Input / Output
5	DIO4	Input / Output
6	DIO5	Input / Output
7	DIO6	Input / Output
8	DIO7	Input / Output
9	+3.3V	PWR
10	GND	GND

2.4.3 LCM Connector (CN18)



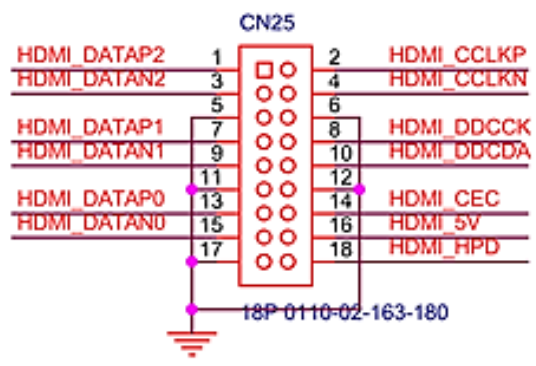
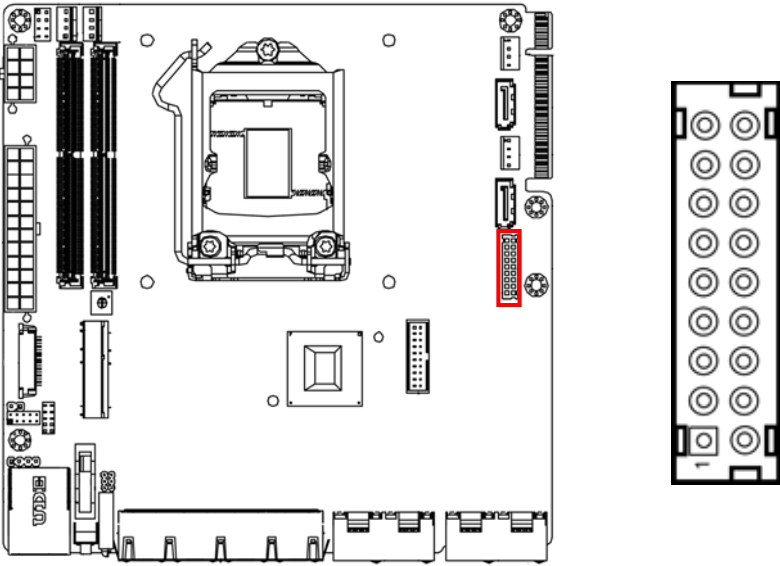
Pin	Signal	Signal Type
1	LCMGND	GND
2	LCMVCC	PWR
3	VEE	PWR
4	SLIN#	Output
5	INIT#	Output
6	AFD#	Output
7	DATA0	Input / Output
8	DATA1	Input / Output
9	DATA2	Input / Output
10	DATA3	Input / Output
11	DATA4	Input / Output
12	DATA5	Input / Output
13	DATA6	Input / Output
14	DATA7	Input / Output
15	+5V	PWR
16	LCD#	Output

2.4.4 Key Pad Connector (CN19)



Pin	Signal	Signal Type
1	KEY PAD Down	Input
2	KEY PAD Up	Input
3	KEY PAD Right	Input
4	KEY PAD Left	Input

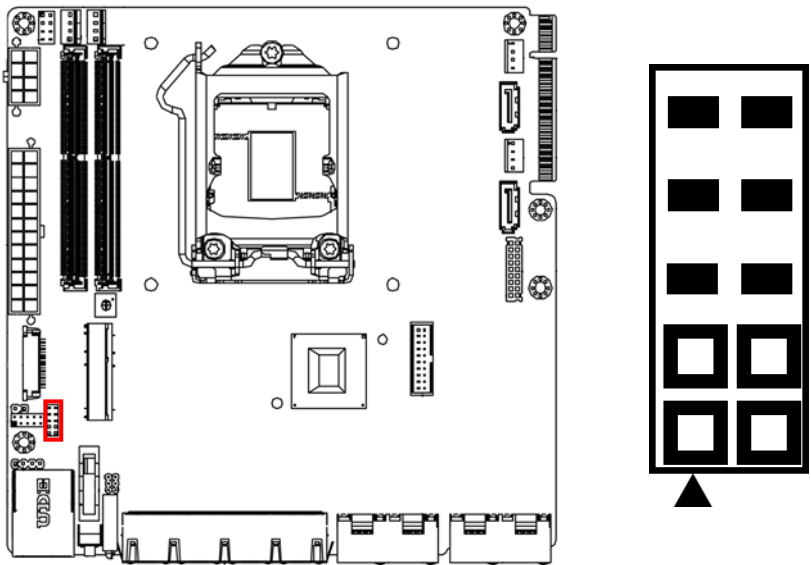
2.4.5 HDMI Connector (CN25)



Pin	Signal	Pin	Signal
1	HDMI_DATAP2	2	HDMI_CCLKP
3	HDMI_DATAN2	4	HDMI_CCLKN
5	GND	6	GND
7	HDMI_DATAP1	8	HDMI_DDCCK

Pin	Signal	Pin	Signal
9	HDMI_DATAN1	10	HDMI_DDCDA
11	GND	12	GND
13	HDMI_DATA0	14	HDMI_CEC
15	HDMI_DATAN0	16	HDMI_5V
17	GND	18	HDMI_HPD

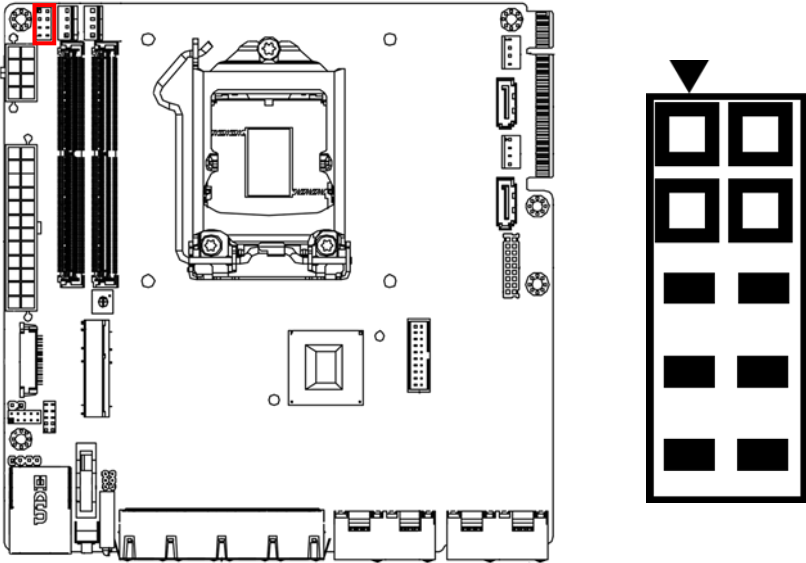
2.4.6 COM Port (COM2)



RS-232		
Pin	Signal	Signal Type
1	DCD	Input
2	RXD	Input
3	TXD	Output
4	DTR	Output
5	GND	GND
6	DSR	Input
7	RTS	Output
8	CTS	Input
9	RI	Input

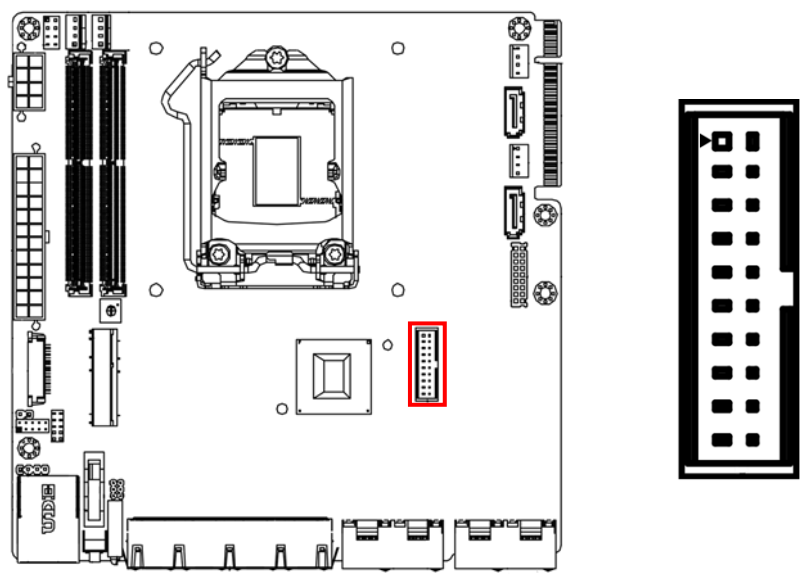
RS-232		
Pin	Signal	Signal Type
10	N.C.	

2.4.7 Front Panel Pin Header (FP1)



Pin	Signal	Signal Type
1	Power On Button (+)	Input
2	Power On Button (-)	GND
3	Reset Switch (+)	Input
4	Reset Switch (-)	GND
5	Power LED (+)	POWER
6	Power LED (-)	GND
7	HDD LED (+)	Output
8	HDD LED (-)	Output

2.4.8 USB 3.0 Port (USB1)



Pin	Signal	Signal Type
1	+5V_USB	PWR
2	USB3_RX1_DN	DIFF
3	USB3_RX1_DP	DIFF
4	GND	GND
5	USB3_TX1_DN	DIFF
6	USB3_TX1_DP	DIFF
7	GND	GND
8	USBP_ON	DIFF
9	USBP_OP	DIFF
10	NC	
11	USBP_1P	DIFF
12	USBP_1N	DIFF
13	GND	GND
14	USB3_TX2_DP	DIFF
15	USB3_TX2_DN	DIFF
16	GND	GND
17	USB3_RX2_DP	DIFF

Pin	Signal	Signal Type
18	USB3_RX2_DN	DIFF
19	+5V_USB	PWR

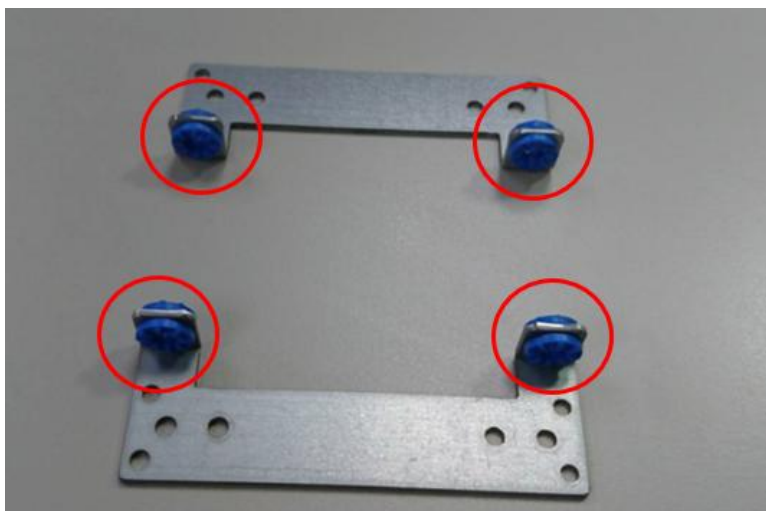
2.5 3.5" Hard Drive Installation

This section details the steps of how to install a 3.5" hard drive for the FWS-7831.

1. Remove the screws securing the top cover, then remove the cover.



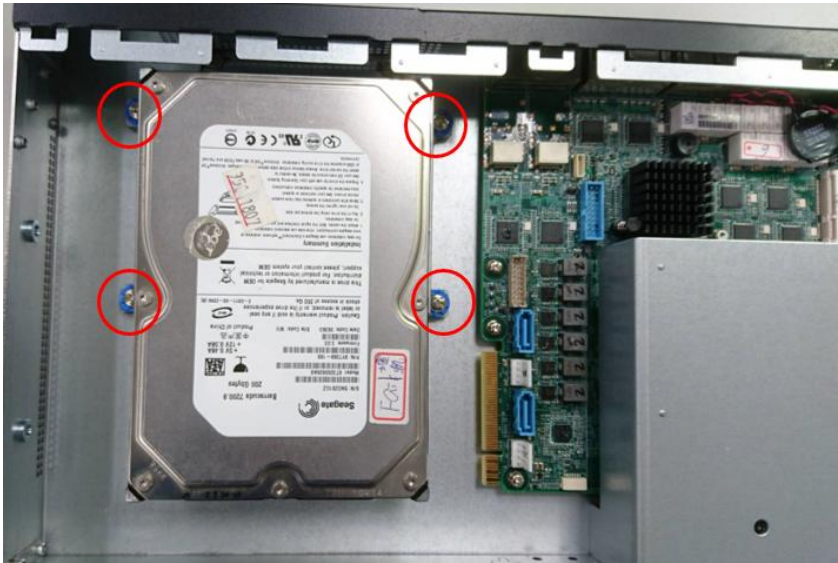
2. Install the bracket cushions on the hard drive brackets as shown.



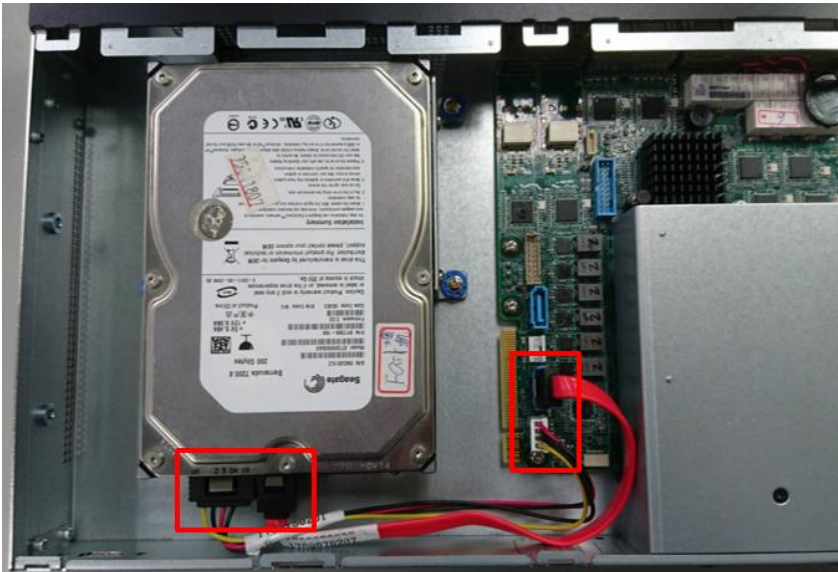
3. Install brackets onto hard drive with screws.



- Fasten the assembled hard drive and brackets to the chassis with screws.



- Connect the SATA cable and power cable to the hard drive and system board.



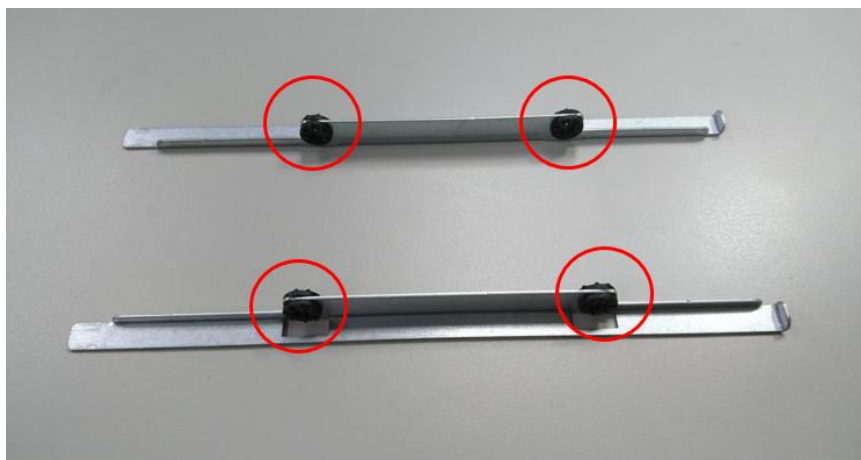
2.6 2.5" Hard Drive Installation

This section details the steps of how to install a 2.5" hard drive for the FWS-7831. This section includes steps for installing one or two 2.5" hard drives.

1. Remove the screws securing the top cover, then remove the cover.



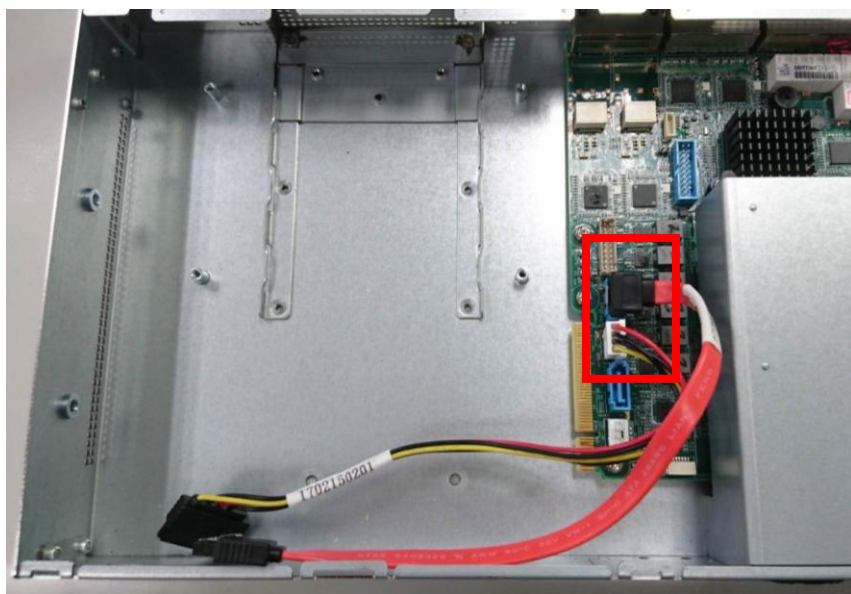
2. Install the bracket cushions on the hard drive brackets as shown.



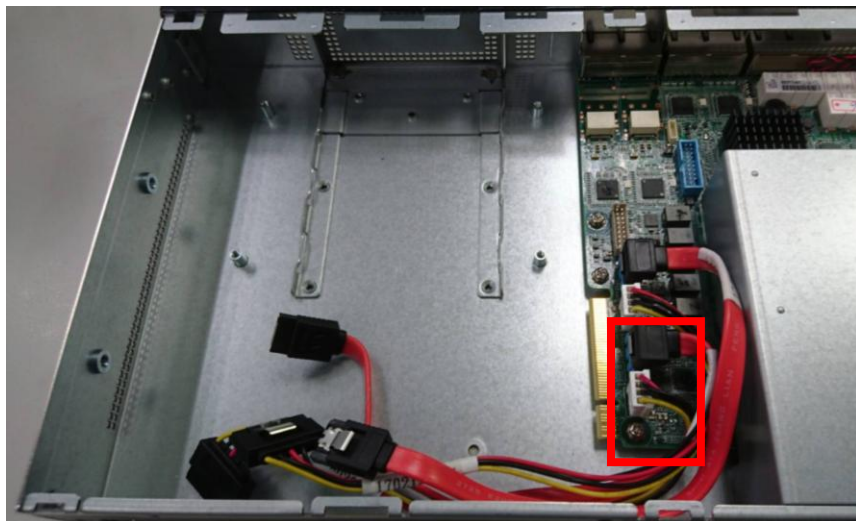
3. Install brackets onto hard drive with screws. Repeat Steps 2 & 3 with the second set of brackets if you are installing two hard drives.



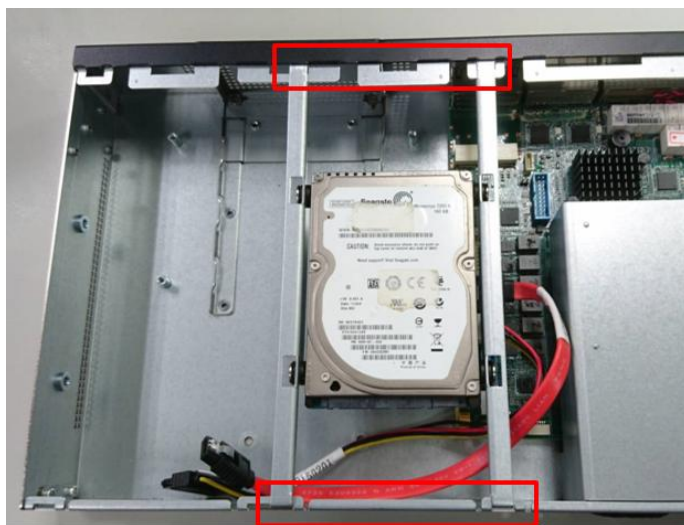
4. Attach SATA and power cables to system board as shown for the first hard drive.



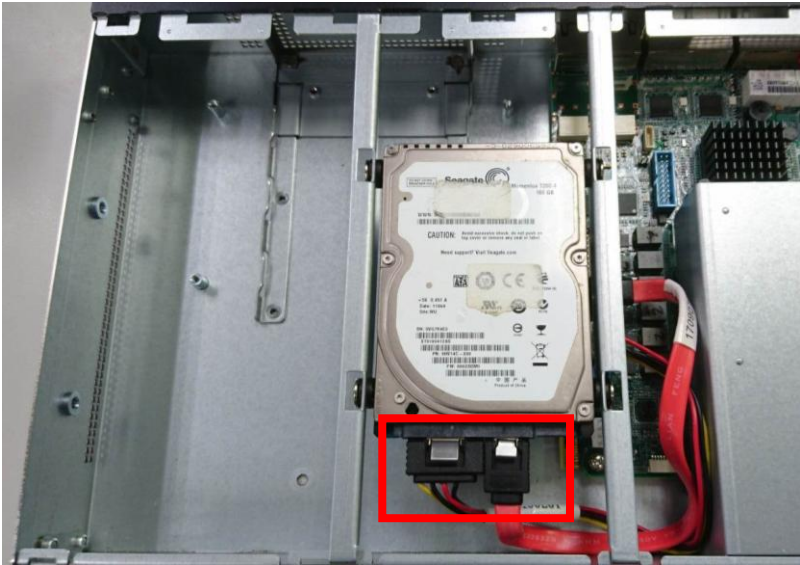
5. Attach SATA and power cables to system board as shown for the second hard drive (skip this step if only installing one hard drive).



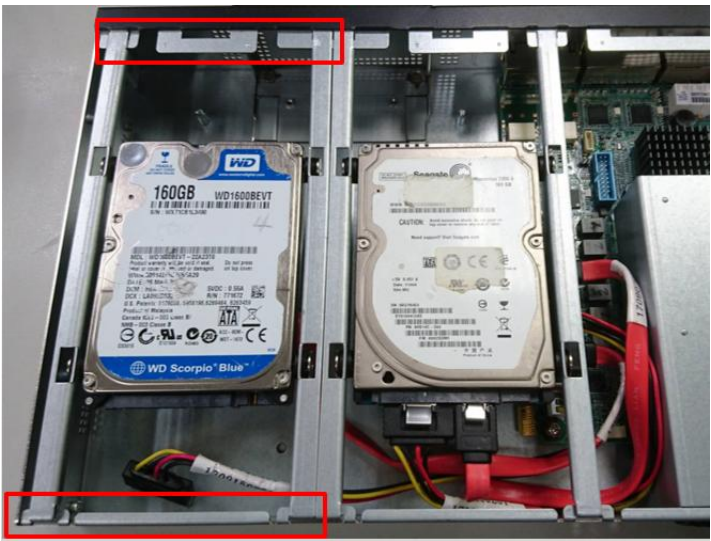
6. Place first hard drive assembly onto installation brackets as shown. **Note:** Make sure that SATA and power cables are under the hard drive.



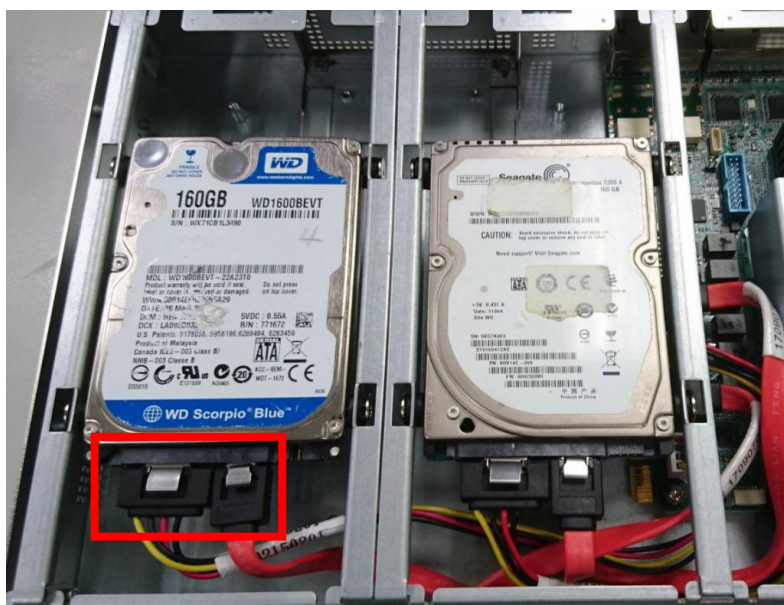
- Connect SATA and power cable to first hard drive as shown.



- Place the second hard drive onto installation brackets as shown. **Note:** Make sure that SATA and power cables are under the hard drive.



9. Connect SATA and power cable to the second hard drive as shown.



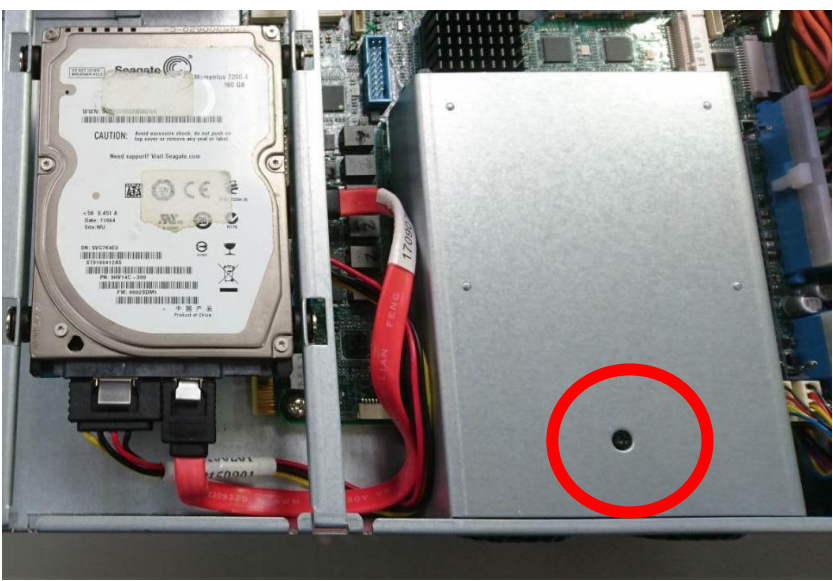
2.7 CPU and Heat Sink Installation

This section details the steps of how to install the CPU and heat sink for the FWS-7831.

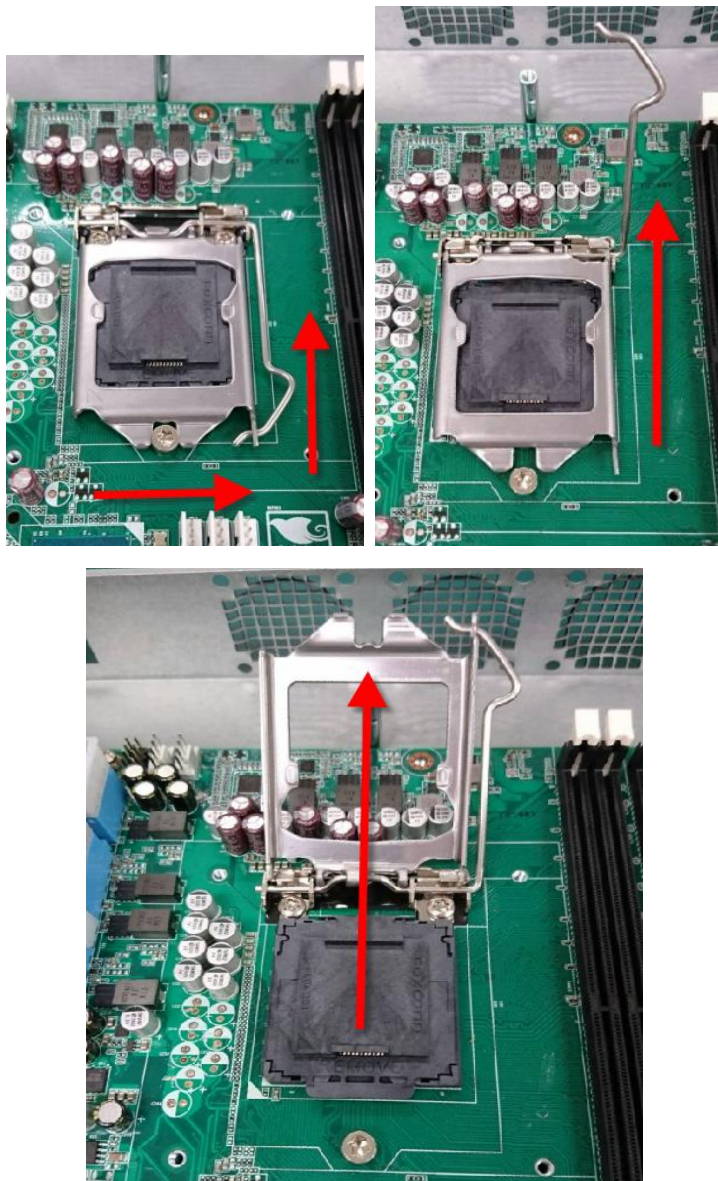
1. Remove the screws securing the top cover, then remove the cover.



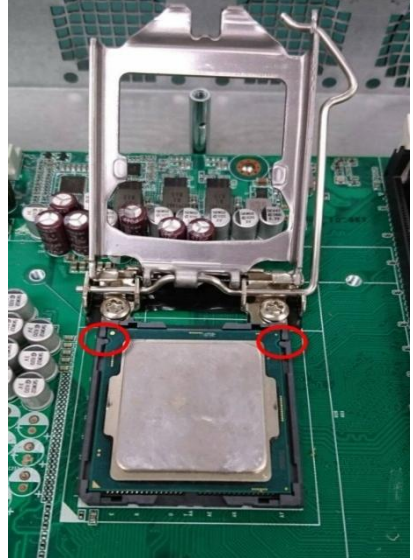
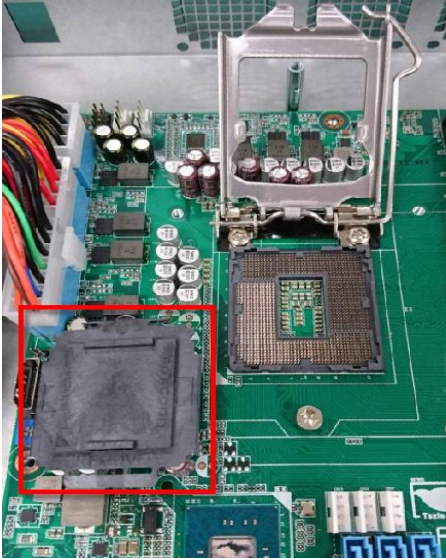
2. Remove the highlighted screw, then remove the fan duct.



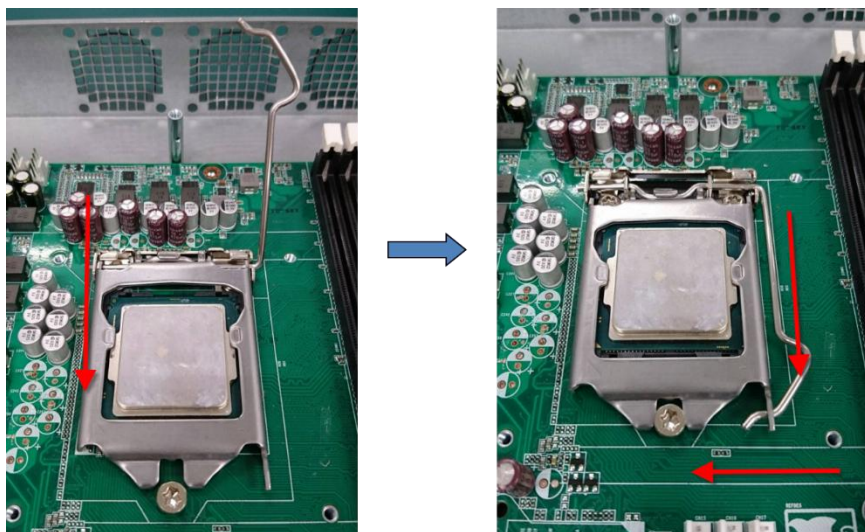
3. Open the CPU bracket.



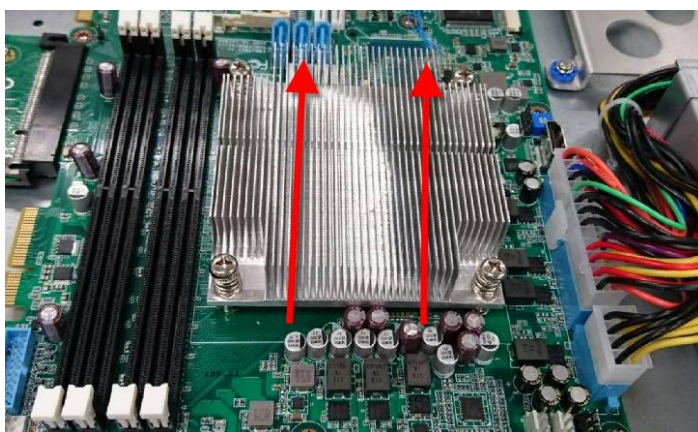
4. Remove the pin cover and place the CPU into the socket. Use the notches to ensure proper alignment. **Note:** The CPU should fit into the socket easily. DO NOT force the CPU into the socket. Pushing on the CPU can cause damage to the CPU pins or socket.



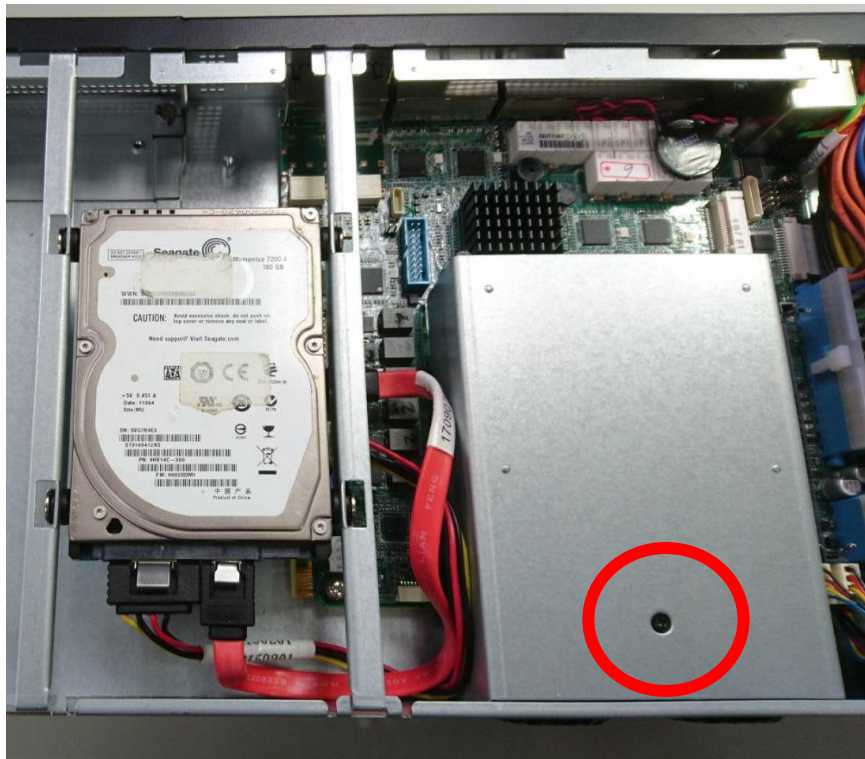
5. Close the bracket and lock the bracket pole into position. **Note:** Please ensure you have applied thermal paste according to CPU manufacturer's guidelines before installing the heat sink.



6. Place the heatsink onto the CPU and fasten the heatsink screws. Make sure the heatsink is aligned with the airflow of the fan.



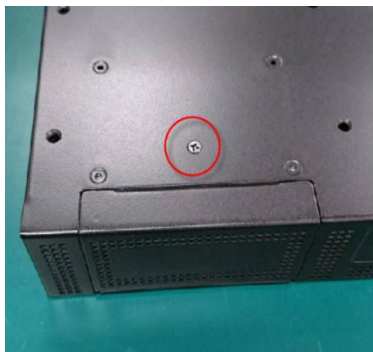
7. Replace the fan cover and secure with the fastening screw.



2.8 NIM Module Installation

This section details how to install NIM modules for the FWS-7831. This applies for new installation, or the removal/replacement of modules.

1. Remove the highlighted screw on the chassis bottom.



2. Remove the null module cover or existing module.



3. Insert the new module (or null module cover) firmly and secure with the screw.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset - Host bridge parameters.

Security – The setup administrator password can be set here

Boot – Enable/ Disable quiet Boot Option

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main

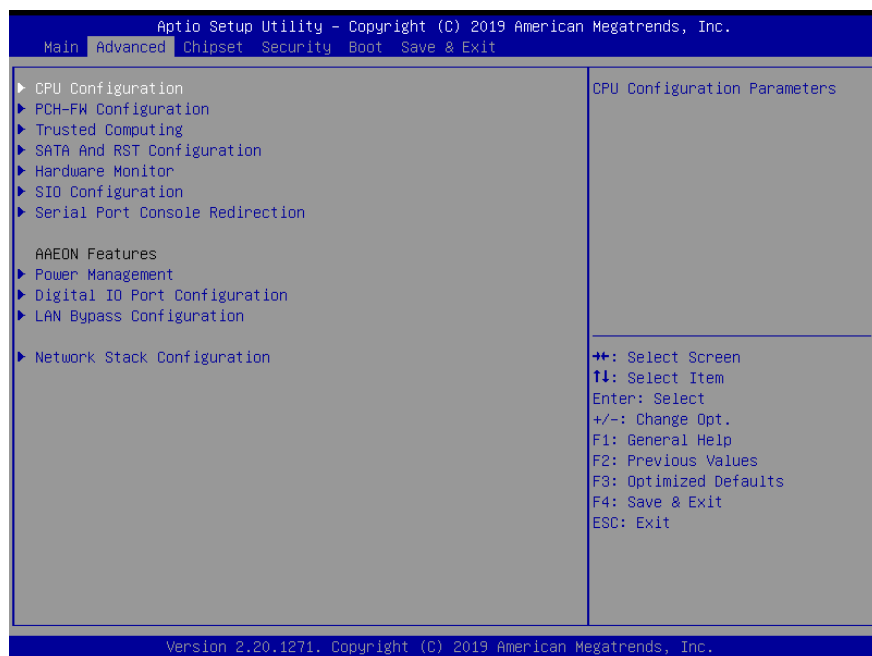
Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

Main Advanced Chipset Security Boot Save & Exit

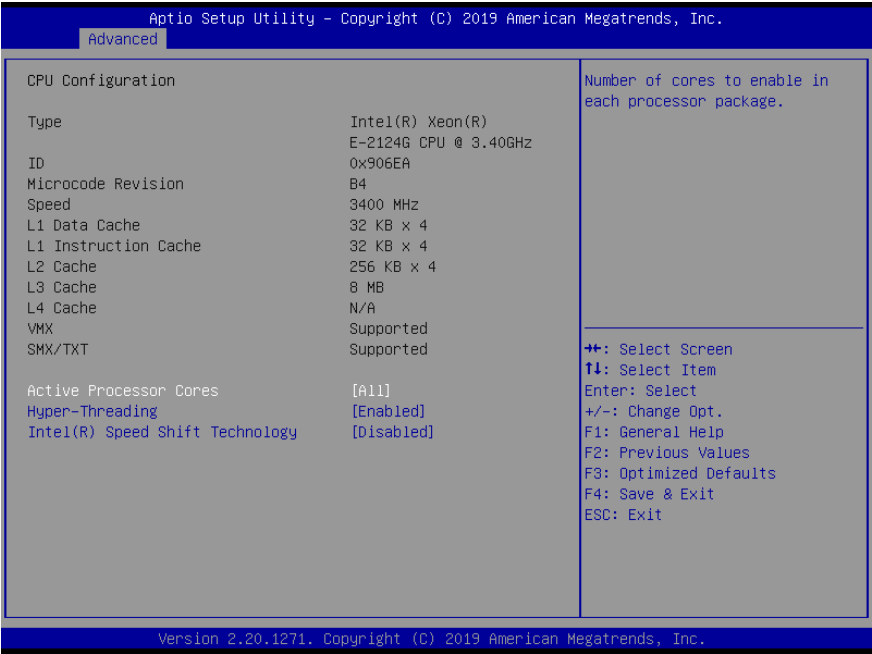
BIOS Information FWS-7831 R1.0 (K783BM10)(04/24/2019)		Set the Date. Use Tab to switch between Date elements. Default Ranges: Year: 2005-2099 Months: 1-12 Days: dependent on month
BIOS Vendor	American Megatrends	
Compliance	UEFI 2.7; PI 1.6	
System Date	[Mon 05/27/2019]	
System Time	[10:45:18]	
Access Level	Administrator	
		++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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3.4 Setup Submenu: Advanced

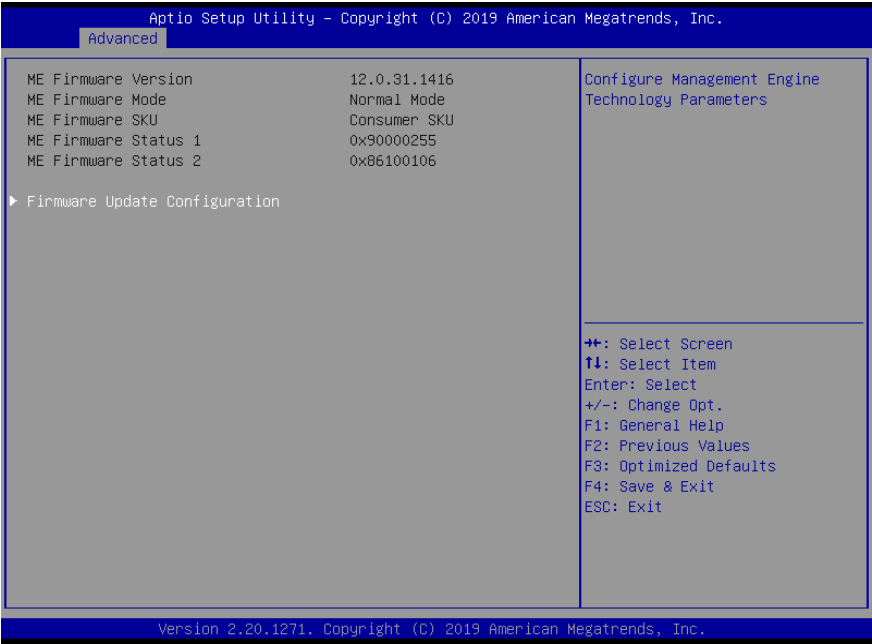


3.4.1 CPU Configuration

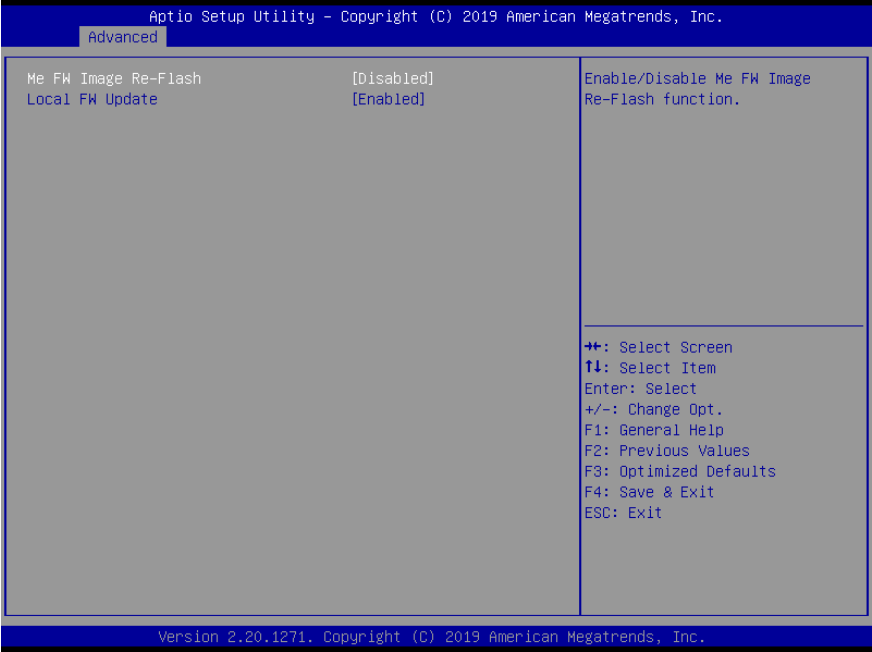


Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe Default
	Other Core numbers	
Number of cores to enable in each processor package.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (operating systems optimized for Hyper-Threading Technology). Disabled for other operating systems that are not optimized for Hyper-Threading Technology.		
Intel® Speed Shift Technology	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable support. When enabled, the CPPC v2 interface is exposed, allowing the processor to autonomously control P-states for faster and more efficient frequency scaling.		

3.4.2 PCH-FW Configuration

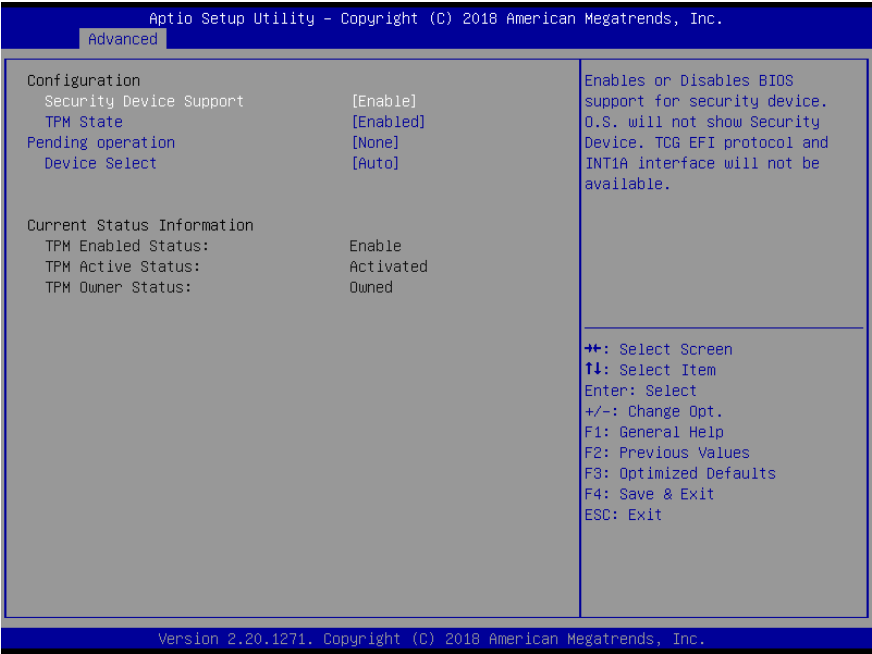


3.4.2.1 Firmware Update Configuration



Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable the ability to re-flash the Intel® Management Engine (ME) firmware image.		
Local FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Select the policy for allowing local firmware updates of the Intel® Management Engine (ME):		
Disabled – Prevents all local firmware updates.		
Enabled – Allows local firmware updates without restriction.		
Via Platform BIOS Control – Firmware updates can only be performed through the system BIOS interface and its security policies.		

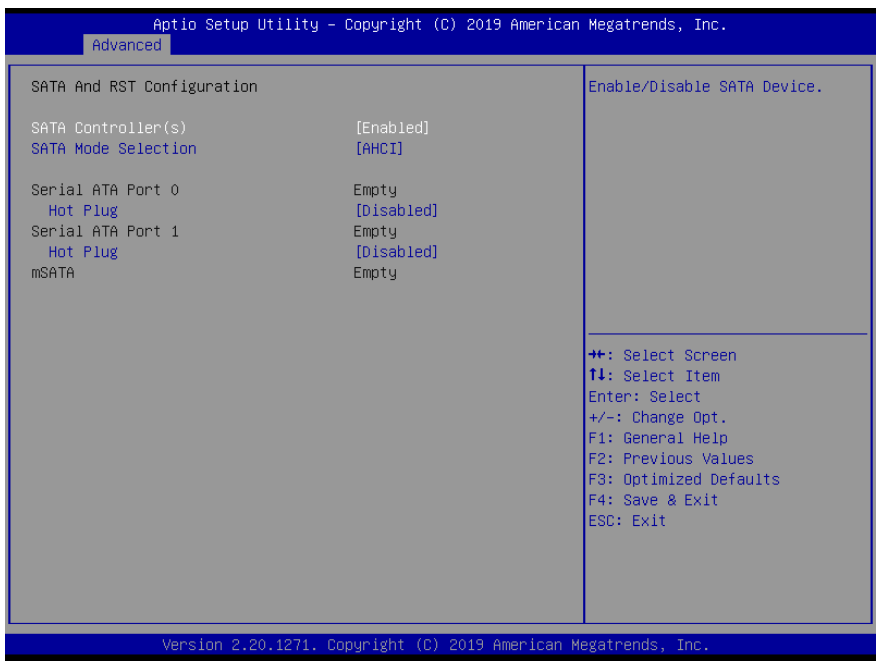
3.4.3 Trusted Computing



Options Summary		
Security Device Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables BIOS support for the security device.		
When disabled, the operating system will not detect the security device, and both the TCG EFI protocol and INT1A interface will be unavailable.		
TPM State	Disabled	
	Enabled	Optimal Default, Failsafe Default
This setting allows you to enable or disable the security device.		
Note: The system will automatically reboot during restart to apply any change to the device state.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
This option allows you to schedule an operation for the security device.		
Note: The system will automatically reboot during restart to apply the change to the device state.		

Options Summary		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
This setting determines the supported TPM (Trusted Platform Module) version: TPM 1.2 – Restricts support to TPM 1.2 devices only. TPM 2.0 – Restricts support to TPM 2.0 devices only. Auto – Supports both TPM 1.2 and TPM 2.0. If a TPM 2.0 device is not found, TPM 1.2 devices will be enumerated by default.		

3.4.4 SATA And RST Configuration



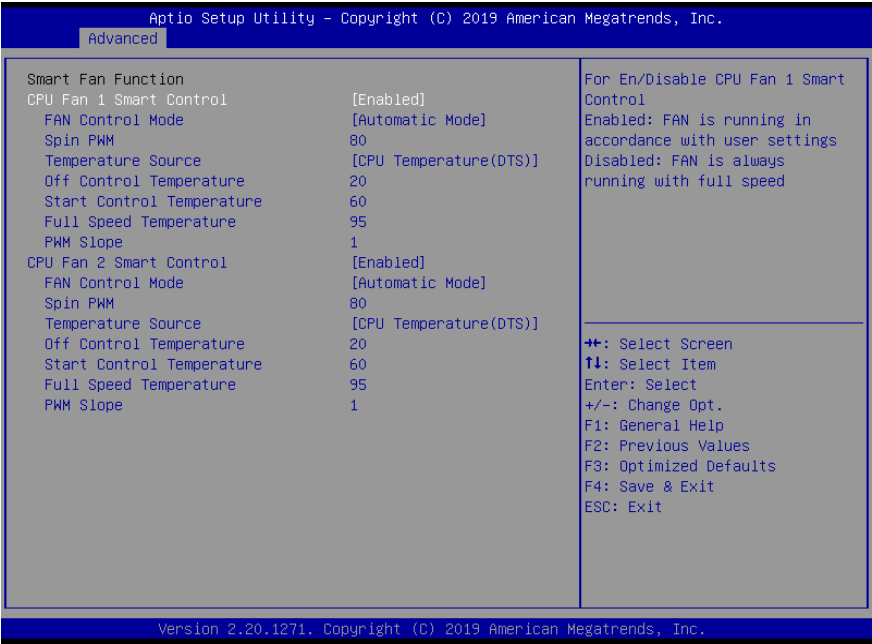
Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	

Options Summary		
Enable/Disable SATA Device.		
SATA Mode Selection	AHCI	Optimal Default, Failsafe Default
SATA Mode Selection (Cont.)	Intel RST Premium with Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.5 Hardware Monitor

Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.	
Advanced	
Pc Health Status	Smart Fan Function Settings
▶ Smart Fan Function CPU Temperature(DTS) : +84 ℃ System Temperature : +34 ℃ CPU Fan 1 Speed : 5037 RPM CPU Fan 2 Speed : N/A VCCORE : +1.248 V VMEM : +1.212 V +12V : +11.952 V +5V : +5.040 V +VCCIO : +0.948 V 5VDUAL : +5.045 V VBAT : +2.904 V	
++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019 American Megatrends, Inc.	

3.4.5.1 Smart Fan Function

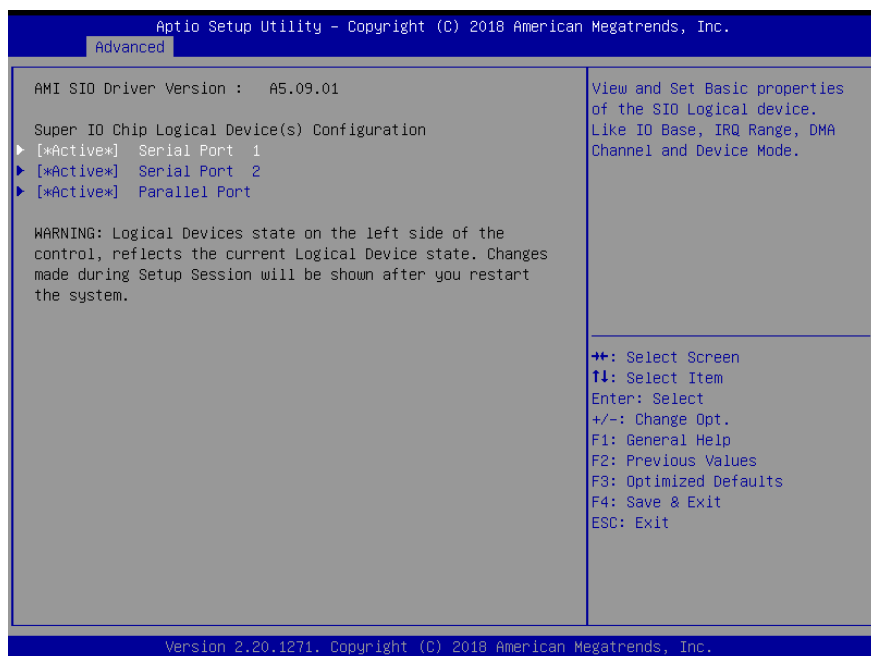


Options Summary

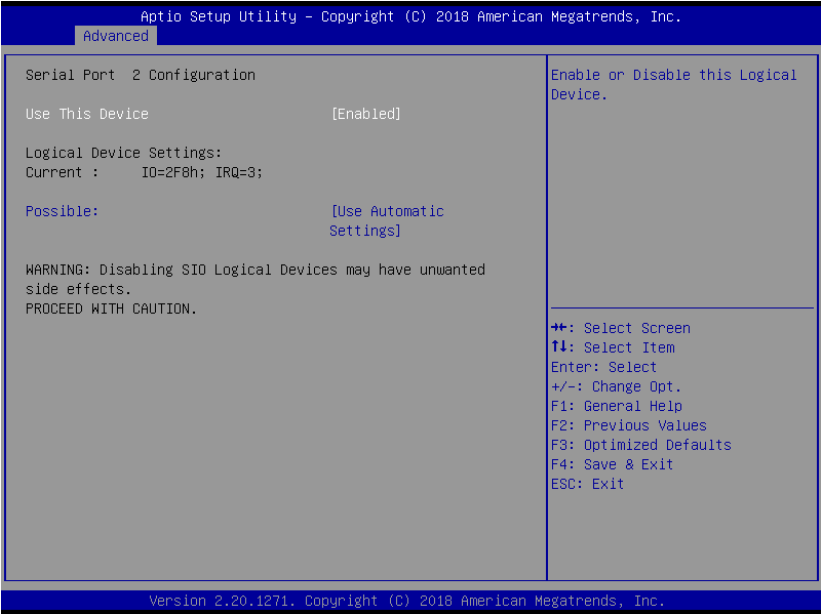
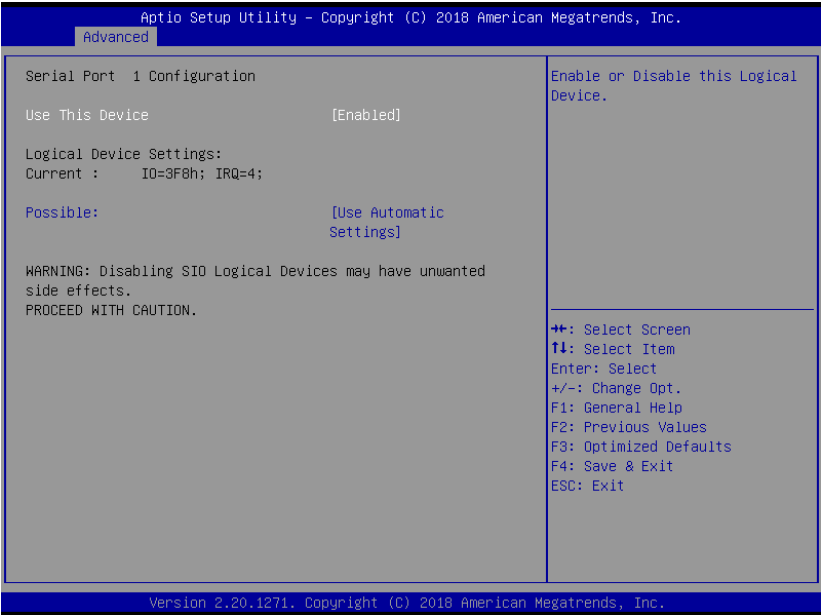
CPU Fan 1 / 2 Smart Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable CPU Fan Smart Control.		
Enabled – The CPU fan speed is automatically adjusted based on user-defined settings.		
Disabled – The CPU fan always runs at full speed.		
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
CPU Fan Control Mode – Select how the CPU fan speed is managed.		
Manual Mode – Fan speed is controlled directly by the PWM duty cycle.		
Automatic Mode – Fan speed is automatically adjusted based on CPU temperature.		
Spin PWM	80	Optimal Default, Failsafe Default
FAN PWM Duty – Set the PWM duty cycle for fan speed control. Range: 0–255.		

Options Summary		
Temperature Source	System Temperature	
	CPU Temperature (DTS)	Optimal Default, Failsafe Default
Reference Temperature Input Selection.		
Off Control Temperature	20	Optimal Default, Failsafe Default
Set the temperature at which the fan stops spinning.		
Note: Some fans may continue to run at a minimum speed even if the PWM value is set to 0.		
Start Control Temperature	60	Optimal Default, Failsafe Default
FAN Start Temperature – Set the temperature at which the fan begins to spin.		
Full Speed Temperature	95	Optimal Default, Failsafe Default
FAN Full Speed Temperature – Set the temperature at which the fan reaches its maximum speed.		
PWM Slope	1	Optimal Default, Failsafe Default
FAN Speed PWM Slope – Set the PWM increment per °C for fan speed control. Range: 1–15.		
PWM Duty	200	Optimal Default, Failsafe Default
Manual Mode PWM Duty – Set the PWM duty value for fan speed control in Manual Mode. Range: 0–255.		

3.4.6 SIO Configuration



3.4.6.1 Serial Port Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Allow the user to modify the device's resource settings. Changes will take effect on this setup page after the system restarts.		

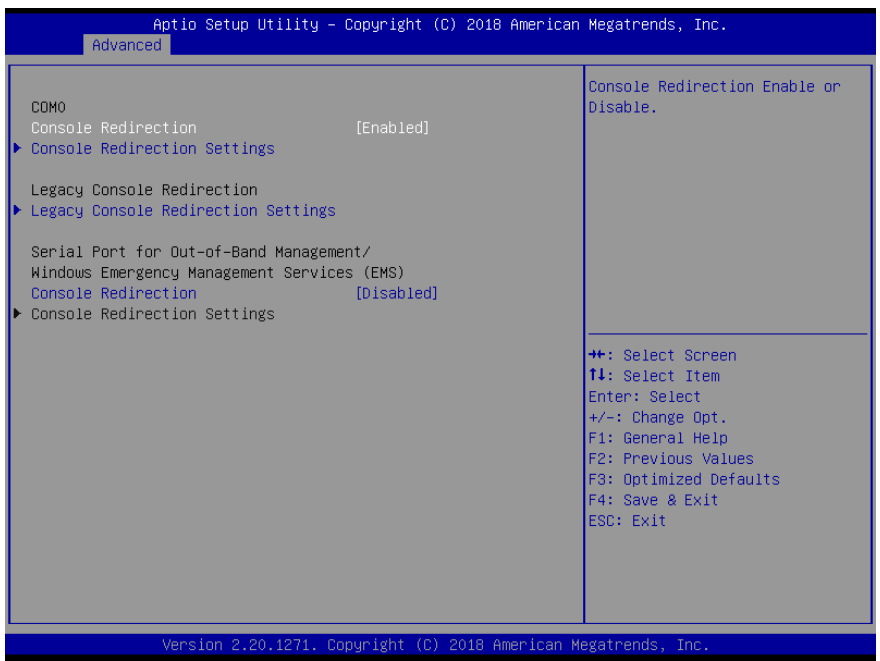
3.4.6.2 Parallel Port Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=378; IRQ=5;	
	IO=378; IRQ=5,6,7,9,10,11,12;	
	IO=278; IRQ=5,6,7,9,10,11,12;	
	IO=3BC; IRQ=5,6,7,9,10,11,12;	
Allow the user to modify the device's resource settings.		
Changes will take effect on this setup page after the system restarts.		

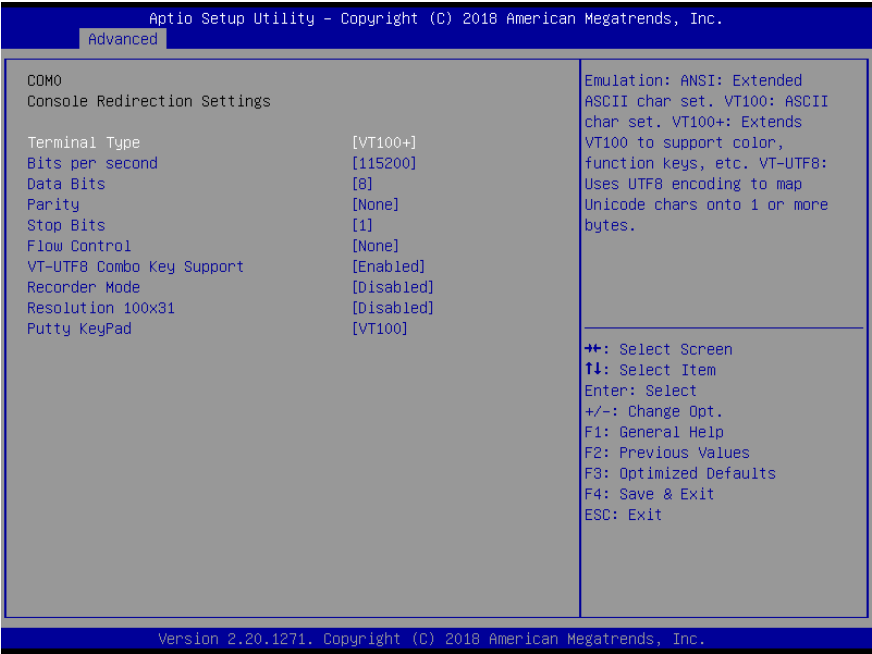
Options Summary		
Mode	Standard Parallel Port mode (SPP)	Optimal Default, Failsafe Default
	EPP Mode	
	ECP Mode	
	EPP mode & ECP mode	
Change the Parallel Port mode. Some modes require a DMA resource. After changing the mode, restart the system to apply the new device settings.		

3.4.7 Serial Port Console Redirection



Options Summary		
COM0 Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Console Redirection		
Serial Port for Out-of-Band Management / Windows EMS		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection.		

3.4.7.1 COM0 Console Redirection



Options Summary		
Terminal Type	VT100	
	VY100+	Optimal Default, Failsafe Default
	VT-UTF8	
	ANSI	
Parallel Port Emulation – Select the emulation type:		
ANSI – Uses the extended ASCII character set.		
VT100 – Uses the standard ASCII character set.		
VT100+ – Extends VT100 to support colors, function keys, and additional features.		
VT-UTF8 – Uses UTF-8 encoding to map Unicode characters onto one or more bytes.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default

Options Summary		
Select the serial port transmission speed. The speed must match the device at the other end. For long or noisy lines, a lower speed may be required.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
Serial Port Parity – Select the parity bit setting to help detect transmission errors: Even – Parity bit is 0 if the number of 1's in the data bits is even. Odd – Parity bit is 0 if the number of 1's in the data bits is odd. Mark – Parity bit is always 1. Space – Parity bit is always 0.		
Note: Mark and Space parity do not provide error detection.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Serial Port Stop Bits – Stop bits indicate the end of a serial data packet (a start bit indicates the beginning). The standard setting is 1 stop bit. Slower devices may require more than 1 stop bit for reliable communication.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Serial Port Flow Control – Flow control prevents data loss due to buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal halts the data flow. Once buffers are empty, a 'start' signal resumes transmission. Hardware flow control uses two dedicated wires to send these start/stop signals.		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable VT-UTF8 combination key support for ANSI and VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
When this mode is enabled, only text data will be sent. Use this mode to capture terminal output.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		

Options Summary		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select the Function Key and Keypad mode for PuTTY.		

3.4.7.2 Legacy Console Redirection Settings

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Advanced

Legacy Console Redirection Settings

Redirection COM Port [COM0]
Resolution [80x24]
Redirect After POST [Always Enable]

Select a COM port to display redirection of Legacy OS and Legacy OPRM Messages

++: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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Options Summary		
Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select the COM port for redirecting Legacy OS and Legacy Option ROM messages.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
Specify the number of rows and columns supported for redirection on a Legacy OS.		

Options Summary		
Redirection After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	

Select the Legacy Console Redirection behavior.
BootLoader – Legacy Console Redirection is disabled before booting to a legacy OS.
Always Enable – Legacy Console Redirection remains enabled for legacy OS. This is the default setting.

3.4.8 Power Management

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Advanced

Power Management

Power Mode [ATX Type]
Restore AC Power Loss [Last State]

Wake Events
RTC wake system from S5 [Enabled]
Wake up day 0
Wake up hour 0
Wake up minute 0
Wake up second 0

Select system power mode.

++: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	

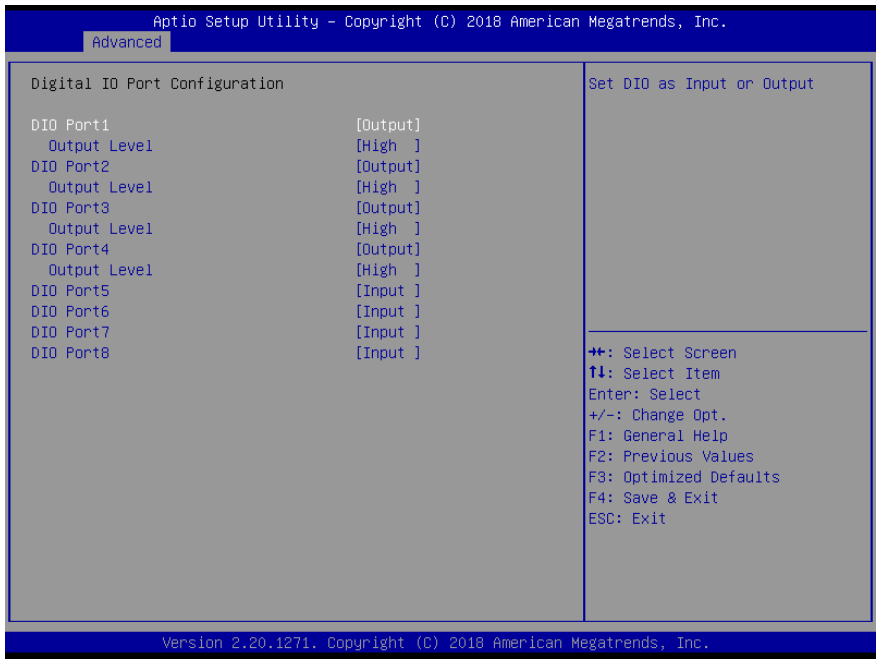
Select power supply mode.

Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	

Select the system power state to enter when power is restored after a power failure.

Options Summary		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Enabled	
Select the wake-up time method: Fixed Time – System wakes at the specified hour, minute, and second. Dynamic Time – System wakes at the current time plus the specified number of minutes.		

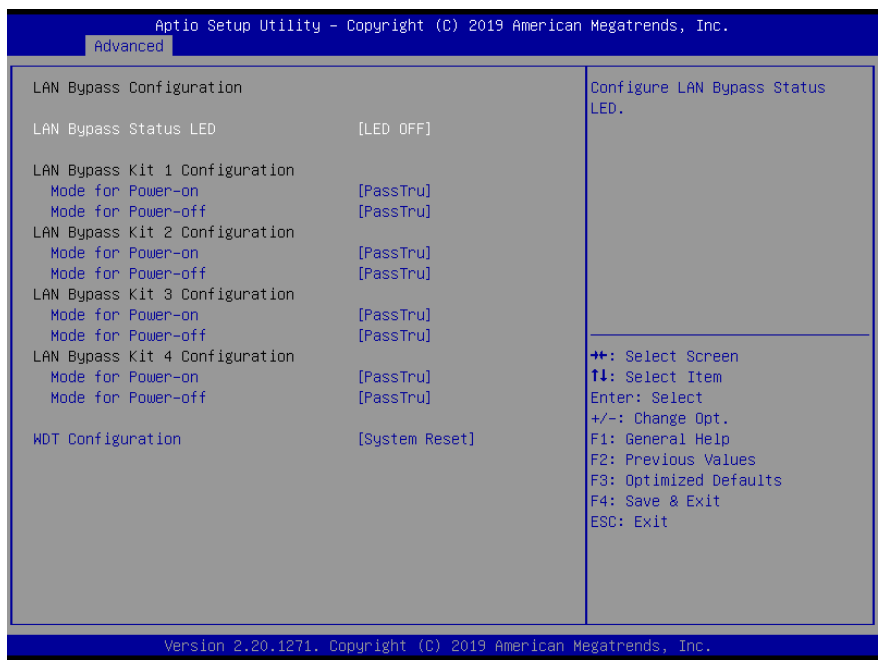
3.4.9 Digital IO Port Configuration



Options Summary		
DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default

Options Summary
Set DIO as Input or Output

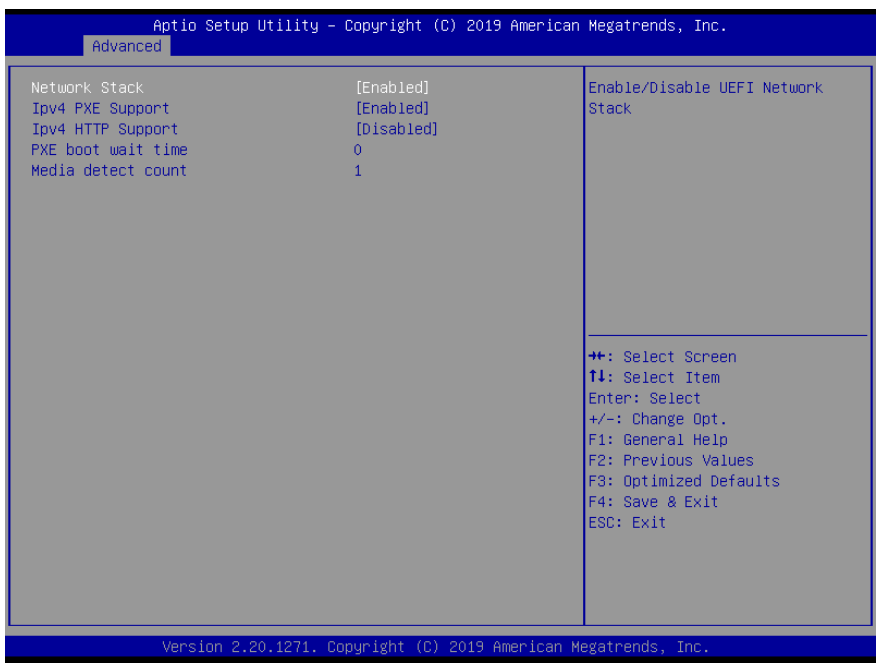
3.4.10 LAN Bypass Configuration



Options Summary		
Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
LAN Bypass Status LED		
Mode for Power-on	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure the LAN kit behavior when the system is powered on: Bypass or Pass Through.		

Options Summary		
Mode for Power-off	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure the LAN kit behavior when the system is powered off: Bypass or Pass Through.		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure the LAN kit behavior when the Watch Dog Timer (WDT) is triggered: Bypass or Pass Through.		

3.4.11 Network Stack Configuration



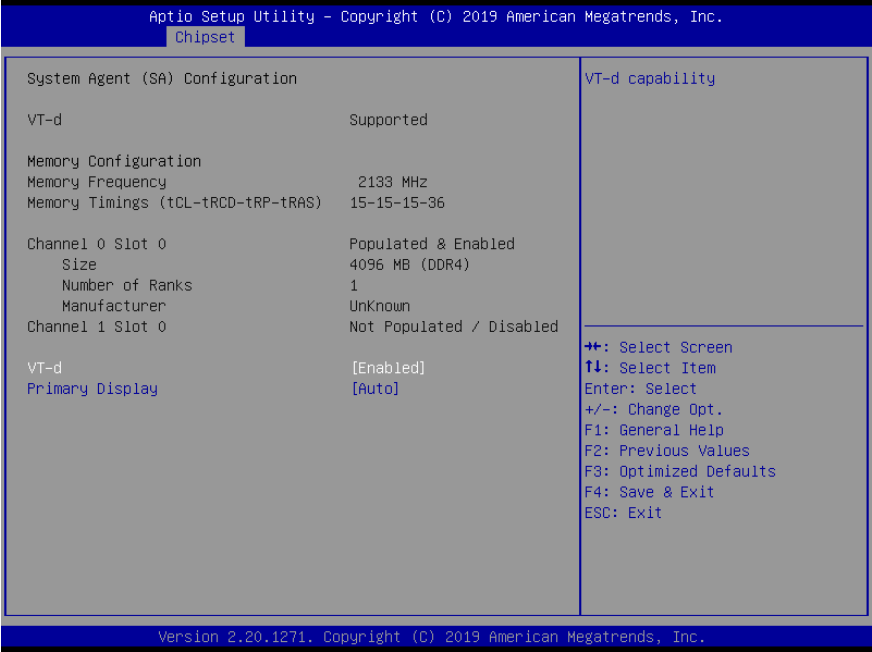
Options Summary		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		
Ipv4 PXE Support	Disabled	
	Enabled	Optimal Default, Failsafe Default

Options Summary		
Enable or disable IPv4 PXE boot support. If disabled, the system will not support IPv4 PXE boot.		
Ipv4 HTTP Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or disable IPv4 HTTP boot support. If disabled, the system will not support IPv4 HTTP boot.		
PXE boot wait time	0	Optimal Default, Failsafe Default
Set the wait time (in seconds) to press the ESC key to abort PXE boot. Use numeric or +/- keys to adjust the value.		
Media detect count	1	Optimal Default, Failsafe Default
Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.		

3.5 Setup Submenu: Chipset



3.5.1 System Agent (SA) Configuration



Options Summary		
VT-d	Disabled	
	Enabled	Optimal Default, Failsafe Default
VT-d capability		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCI	
Select the primary display device: IGFX, PEG, PCI, or SG for Switchable Graphics.		

3.6 Setup Submenu: Security



Change User/Administrator Password

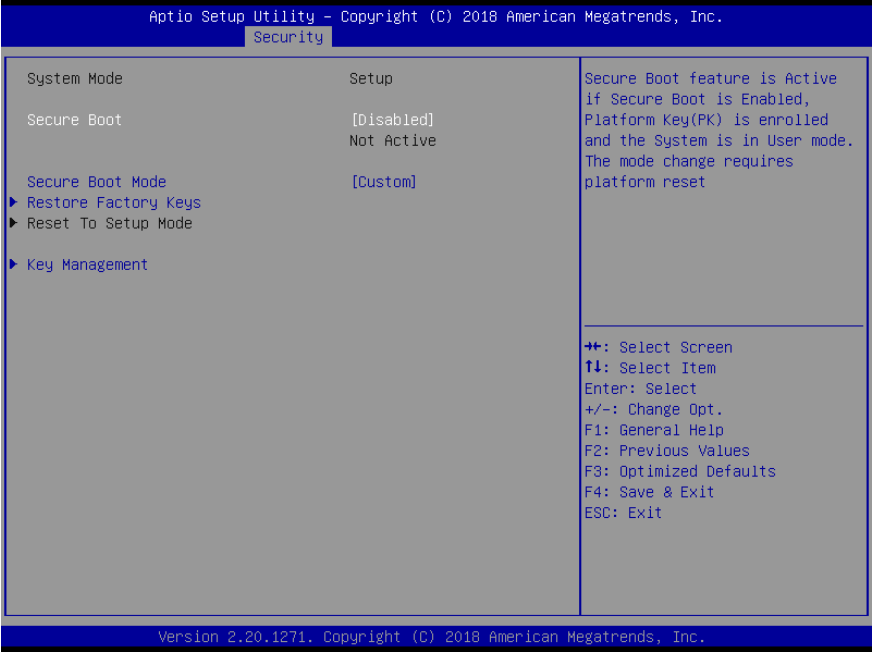
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

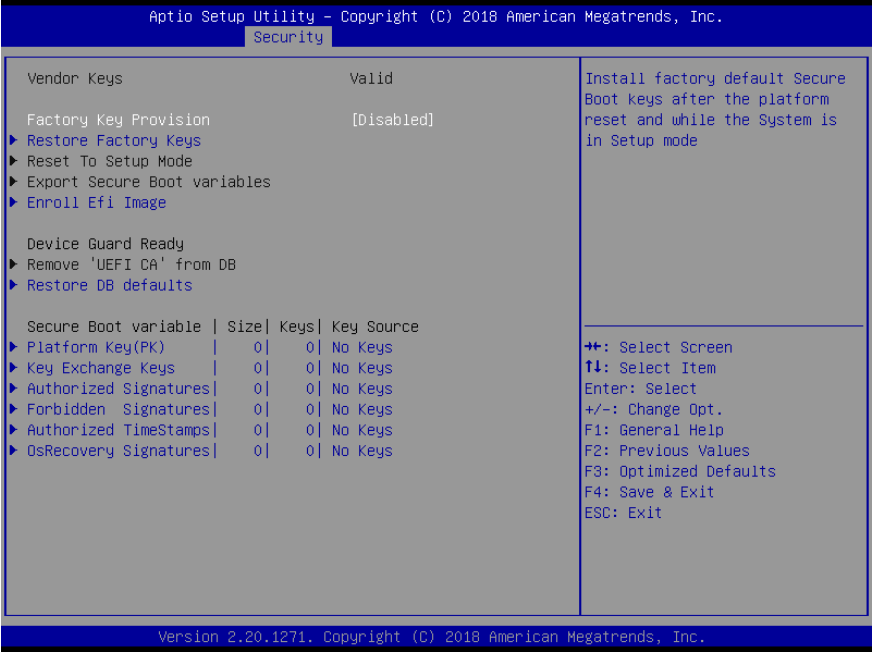
3.6.1 Secure Boot



Options Summary

Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
The Secure Boot feature is active when Secure Boot is enabled, the Platform Key (PK) is enrolled, and the system is in User mode. Changing the mode requires a platform reset.		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
In Custom mode, Secure Boot Policy variables can be configured by a physically present user without requiring full authentication.		
Restore Factory Keys	No	Select 'Yes' to restore factory default keys
	Yes	
Force the system into User Mode and install the factory default Secure Boot key databases.		
Reset To Setup Mode	No	Select 'Yes' to reset to setup mode
	Yes	
Delete all Secure Boot key databases from NVRAM, placing the system in Setup Mode.		

3.6.1.1 Secure Boot: Key Management



Options Summary

Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install the factory default Secure Boot keys after a platform reset while the system is in Setup mode.		
Restore Factory Keys	No	Press 'Yes' to restore factory default keys
	Yes	
Force the system into User Mode and install the factory default Secure Boot key databases.		
Reset To Setup Mode	No	Press 'Yes' to reset to setup mode
	Yes	
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables	Select a File system to export Secure Boot variables	
Copy the contents of Secure Boot variables from NVRAM to files in the root folder of a file system device.		

Options Summary	
Enroll Efi Image	Select a File system to enroll Efi image into Authorized Signature Database.
Allow the image to run in Secure Boot mode by enrolling the SHA256 hash certificate of a PE image into the Authorized Signature Database (db).	
Remove 'UEFI CA' from DB	
For a Device Guard-ready system, the 'Microsoft UEFI CA' certificate must not be listed in the Authorized Signature Database (db).	
Restore DB defaults	Press 'Yes' to restore DB variable to factory defaults
Restore DB variable to factory defaults	

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Quiet Boot option.		
CSM Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CSM Support.		
Launch PXE ROM	Do not launch	Optimal Default, Failsafe Default
	UEFI	
	Legacy	
Controls the execution of UEFI and Legacy Network Option ROMs.		
Note: The Network Stack must be enabled when selecting UEFI PXE boot.		
Boot mode select	Legacy	
	UEFI	Optimal Default, Failsafe Default
	DUAL	
Select the system boot mode: Legacy or UEFI.		

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the FWS-7831 can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/product/detail/1u-rackmount-network-appliance-fws-7831/download>

Download the driver(s) you need and follow the steps below to install them.

LAN Driver

1. Open the **LAN** folder.
2. Extract the archived file igb-5.3.5.22.tar.gz
3. Extract the archived file igb-5.3.5.22.tar
4. Open igb-5.3.5.22
5. Follow instructions in README

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: SuperIO Relative Register Table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Watchdog Relative Register Table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN  //This parameter is represented from Note9
#define byte   EnableReg  //This parameter is represented from Note10
#define byte   EnableBit  //This parameter is represented from Note11
#define byte   EnableVal  //This parameter is represented from Note12
#define byte   StatusLDN  // This parameter is represented from Note13
#define byte   StatusReg  // This parameter is represented from Note14
#define byte   StatusBit  // This parameter is represented from Note15
*****
```

```
*****
VOID  Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID  SIOEnterMBPnPMode(){
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****

```

```
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;
```

```
    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
```

```
}
```

```
VOID SIOByteSet(byte LDN, byte Register, byte Value){
```

```
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
```

```
}
```

Appendix B

I/O Information

B.1 I/O Address Map

▼	Input/output (IO)
	[0000000000000000 - 000000000000CF7] PCI Express Root Complex
	[0000000000000020 - 0000000000000021] Programmable interrupt controller
	[0000000000000024 - 0000000000000025] Programmable interrupt controller
	[0000000000000028 - 0000000000000029] Programmable interrupt controller
	[000000000000002C - 000000000000002D] Programmable interrupt controller
	[000000000000002E - 000000000000002F] Motherboard resources
	[0000000000000030 - 0000000000000031] Programmable interrupt controller
	[0000000000000034 - 0000000000000035] Programmable interrupt controller
	[0000000000000038 - 0000000000000039] Programmable interrupt controller
	[000000000000003C - 000000000000003D] Programmable interrupt controller
	[0000000000000040 - 0000000000000043] System timer
	[000000000000004E - 000000000000004F] Motherboard resources
	[0000000000000050 - 0000000000000053] System timer
	[0000000000000061 - 0000000000000061] Motherboard resources
	[0000000000000063 - 0000000000000063] Motherboard resources
	[0000000000000065 - 0000000000000065] Motherboard resources
	[0000000000000067 - 0000000000000067] Motherboard resources
	[0000000000000070 - 0000000000000070] Motherboard resources
	[0000000000000080 - 0000000000000080] Motherboard resources
	[0000000000000092 - 0000000000000092] Motherboard resources
	[00000000000000A0 - 00000000000000A1] Programmable interrupt controller
	[00000000000000A4 - 00000000000000A5] Programmable interrupt controller
	[00000000000000A8 - 00000000000000A9] Programmable interrupt controller
	[00000000000000AC - 00000000000000AD] Programmable interrupt controller
	[00000000000000B0 - 00000000000000B1] Programmable interrupt controller
	[00000000000000B2 - 00000000000000B3] Motherboard resources
	[00000000000000B4 - 00000000000000B5] Programmable interrupt controller
	[00000000000000B8 - 00000000000000B9] Programmable interrupt controller
	[00000000000000BC - 00000000000000BD] Programmable interrupt controller
	[00000000000000F0 - 00000000000000F0] Numeric data processor
	[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
	[0000000000000378 - 000000000000037F] Printer Port (LPT1)
	[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
	[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
	[0000000000000680 - 000000000000069F] Motherboard resources
	[0000000000000A00 - 0000000000000A2F] Motherboard resources
	[0000000000000A30 - 0000000000000A3F] Motherboard resources
	[0000000000000A40 - 0000000000000A4F] Motherboard resources
	[0000000000000D00 - 0000000000000FFF] PCI Express Root Complex
	[000000000000164E - 000000000000164F] Motherboard resources
	[0000000000001800 - 00000000000018FE] Motherboard resources
	[0000000000001854 - 0000000000001857] Motherboard resources
	[0000000000002000 - 00000000000020FE] Motherboard resources
	[0000000000003000 - 0000000000003FFF] Intel(R) PCI Express Root Port #12 - A333
	[0000000000004000 - 0000000000004FFF] Intel(R) PCI Express Root Port #11 - A332
	[0000000000005000 - 0000000000005FFF] Intel(R) PCI Express Root Port #8 - A33F
	[0000000000006000 - 0000000000006FFF] Intel(R) PCI Express Root Port #7 - A33E
	[0000000000007000 - 0000000000007FFF] Intel(R) PCI Express Root Port #6 - A33D
	[0000000000008000 - 0000000000008FFF] Intel(R) PCI Express Root Port #5 - A33C
	[0000000000009000 - 0000000000009FFF] Intel(R) PCI Express Root Port #18 - A341
	[000000000000A000 - 000000000000AFFF] Intel(R) PCI Express Root Port #17 - A340

	[000000000000A000 - 000000000000AFFF] Intel(R) PCI Express Root Port #17 - A340
	[000000000000B000 - 000000000000B03F] Intel(R) UHD Graphics P630
	[000000000000B060 - 000000000000B07F] Standard SATA AHCI Controller
	[000000000000B080 - 000000000000B083] Standard SATA AHCI Controller
	[000000000000B090 - 000000000000B097] Standard SATA AHCI Controller
	[000000000000EFA0 - 000000000000EFBF] Intel(R) SMBus - A323

B.2 Memory Address Map

▼	Memory
	[0000000000A0000 - 0000000000BFFFF] PCI Express Root Complex
	[0000000040000000 - 00000000403FFFF] Motherboard resources
	[0000000090000000 - 000000009FFFFFF] Intel(R) UHD Graphics P630
	[0000000090000000 - 00000000DFFFFFF] PCI Express Root Complex
	[00000000A0000000 - 00000000A0FFFFFF] Intel(R) UHD Graphics P630
	[00000000A1000000 - 00000000A10FFFF] Intel(R) PCI Express Root Port #12 - A333
	[00000000A10DC000 - 00000000A10DFFF] Intel(R) I211 Gigabit Network Connection #8
	[00000000A10E0000 - 00000000A10FFFF] Intel(R) I211 Gigabit Network Connection #8
	[00000000A1100000 - 00000000A11FFFF] Intel(R) PCI Express Root Port #11 - A332
	[00000000A11DC000 - 00000000A11DFFF] Intel(R) I211 Gigabit Network Connection #7
	[00000000A11E0000 - 00000000A11FFFF] Intel(R) I211 Gigabit Network Connection #7
	[00000000A1200000 - 00000000A12FFFF] Intel(R) PCI Express Root Port #8 - A33F
	[00000000A12DC000 - 00000000A12DFFF] Intel(R) I211 Gigabit Network Connection #6
	[00000000A12E0000 - 00000000A12FFFF] Intel(R) I211 Gigabit Network Connection #6
	[00000000A1300000 - 00000000A13FFFF] Intel(R) PCI Express Root Port #7 - A33E
	[00000000A13DC000 - 00000000A13DFFF] Intel(R) I211 Gigabit Network Connection #5
	[00000000A13E0000 - 00000000A13FFFF] Intel(R) I211 Gigabit Network Connection #5
	[00000000A1400000 - 00000000A141FFFF] Intel(R) I211 Gigabit Network Connection #4
	[00000000A1400000 - 00000000A14FFFF] Intel(R) PCI Express Root Port #6 - A33D
	[00000000A1420000 - 00000000A1423FFF] Intel(R) I211 Gigabit Network Connection #4
	[00000000A1500000 - 00000000A151FFF] Intel(R) I211 Gigabit Network Connection #3
	[00000000A1500000 - 00000000A15FFFF] Intel(R) PCI Express Root Port #5 - A33C
	[00000000A1520000 - 00000000A1523FFF] Intel(R) I211 Gigabit Network Connection #3
	[00000000A1600000 - 00000000A16FFFF] Intel(R) PCI Express Root Port #18 - A341
	[00000000A16DC000 - 00000000A16DFFF] Intel(R) I211 Gigabit Network Connection #2
	[00000000A16E0000 - 00000000A16FFFF] Intel(R) I211 Gigabit Network Connection #2
	[00000000A1700000 - 00000000A17FFFF] Intel(R) PCI Express Root Port #17 - A340
	[00000000A17DC000 - 00000000A17DFFF] Intel(R) I211 Gigabit Network Connection
	[00000000A17E0000 - 00000000A17FFFF] Intel(R) I211 Gigabit Network Connection
	[00000000A1800000 - 00000000A180FFF] Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
	[00000000A1810000 - 00000000A181FFF] Standard SATA AHCI Controller
	[00000000A1814000 - 00000000A18140FF] Intel(R) SMBus - A323
	[00000000A1815000 - 00000000A18157FF] Standard SATA AHCI Controller
	[00000000A1816000 - 00000000A18160FF] Standard SATA AHCI Controller
	[00000000A1819000 - 00000000A1819FFF] Intel(R) Thermal Subsystem - A379
	[00000000E0000000 - 00000000EFFFFFF] Motherboard resources
	[00000000FC800000 - 00000000FE7FFFF] PCI Express Root Complex
	[00000000FD000000 - 00000000FD69FFF] Motherboard resources
	[00000000FD6A0000 - 00000000FD6AFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
	[00000000FD6B0000 - 00000000FD6BFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
	[00000000FD6C0000 - 00000000FD6CFFF] Motherboard resources
	[00000000FD6D0000 - 00000000FD6DFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
	[00000000FD6E0000 - 00000000FD6EFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
	[00000000FD6F0000 - 00000000FDFFFF] Motherboard resources
	[00000000FE000000 - 00000000FE01FFF] Motherboard resources
	[00000000FE010000 - 00000000FE010FFF] Intel(R) SPI (flash) Controller - A324
	[00000000FE1FF000 - 00000000FE1FFFF] Intel(R) Management Engine Interface
	[00000000FE200000 - 00000000FE7FFFF] Motherboard resources
	[00000000FED00000 - 00000000FED003FF] High precision event timer
	[00000000FED10000 - 00000000FED17FFF] Motherboard resources
	[00000000FED18000 - 00000000FED18FFF] Motherboard resources

	[00000000FED19000 - 00000000FED19FFF]	Motherboard resources
	[00000000FED20000 - 00000000FED3FFFF]	Motherboard resources
	[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 1.2
	[00000000FED45000 - 00000000FED8FFFF]	Motherboard resources
	[00000000FED90000 - 00000000FED93FFF]	Motherboard resources
	[00000000FEE00000 - 00000000FFFFFFF]	Motherboard resources
	[00000000FF000000 - 00000000FFFFFFFF]	Motherboard resources

B.3 IRQ Mapping Chart

- ▼  Interrupt request (IRQ)
 -  (ISA) 0x00000000 (00) System timer
 -  (ISA) 0x00000003 (03) Communications Port (COM2)
 -  (ISA) 0x00000004 (04) Communications Port (COM1)
 -  (ISA) 0x0000000D (13) Numeric data processor
 -  (ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3450

Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

The FWS-7831 features a Status LED indicator which can be configured using the AAEON SDK. The Status LED can be programmed to indicate different system statuses. This section provides information on how to program and configure the Status LED.

C.1.1 Status LED Configuration

Table 1: Truth Table of Status LED

STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table 2: Status LED Relative Register Mapping Table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

C.1.2 Sample Code

```

*****
***
#define Byte CPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define Byte OFFSET //This parameter is represented from Note2
*****
***

bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
//LED Off
//BIT2=0, BIT1=0, BIT0=0
bData = bData & 0xF8;
break;
}
case 1:
{
//Red LED On
//BIT2=0, BIT1=0, BIT0=1
bData = (bData & 0xF8) | 0x01;
break;
}
case 2:
{
//Red LED Blink
//BIT2=0, BIT1=1, BIT0=0
bData = (bData & 0xF8) | 0x02;
break;
}
case 3:
{
//Red LED Fast Blink
//BIT2=0, BIT1=1, BIT0=1
bData = (bData & 0xF8) | 0x03;
break;
}
case 4:

```

```
{
    //Green LED On
    //BIT2=1, BIT1=1, BIT0=1
    bData = (bData & 0xF8) | 0x07;
    break;
}
case 5:
{
    //Green LED Blink
    //BIT2=1, BIT1=0, BIT0=1
    bData = (bData & 0xF8) | 0x05;
    break;
}
case 6:
{
    //Green LED Fast Blink
    //BIT2=1, BIT1=1, BIT0=0
    bData = (bData & 0xF8) | 0x06;
    break;
}
default:
    break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*****
***
```

C.2 LAN Bypass

The FWS-7831 provides a LAN Bypass kit, allowing uninterrupted network traffic even if a single in-line appliance is shut down or hangs. This section details how to configure and program the LAN Bypass.

C.2.1 LAN Bypass Configuration

Table 1: ID Select Table of LAN Kit

LAN_ID3	LAN_ID2	LAN_ID1	LAN_ID0	LAN Kit selected
0	0	0	0	LAN Kit 1 Selected
0	0	0	1	LAN Kit 2 Selected
0	0	1	0	LAN Kit 3 Selected
1	1	1	1	LAN Kit 16 Selected

Table 2: LAN Bypass Relative Register Table

Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3: LAN Bypass Relative Register Mapping Table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

C.2.2 Sample Code

```

*****
***
#define Byte CPLD_SLAVE_ADDRESS    //This parameter is represented from Note1
#define Byte OFFSET                //This parameter is represented from Note2
*****
***
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
    bData = bData | 0x08;
else
    bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
    bData = bData | 0x04;
else
    bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
    bData = bData | 0x02;
else
    bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
    bData = bData | 0x01;
else
    bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)    // Pass Through
    bData = bData & 0xBF;
else                    // Bypass
    bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)    // Pass Through

```

```
        bData = bData & 0xDF;
else                                     // Bypass
    bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET) // Reset
    bData = bData & 0xEF;
else                                     // Bypass
    bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*****
```

C.3 Software Reset Button (General Propose Input)

The FWS-7831 provides a general-purpose input button which can be configured by the AAeon SDK. This section details how to configure and program this feature.

C.3.1 Software Reset Button Configuration

Table 2: Software Reset Button Register Table	
Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1: Soft Reset Button Register Mapping Table				
	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

C.3.2 Sample Code

```
*****
#define Word BTN_STS      //This parameter is represented from Note1
#define Byte  BTN_STS_R   //This parameter is represented from Note2
*****

Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
    BYTE  TmpValue;

    TmpValue = inportb (IoAddr);
    return  (TmpValue & (1 << BitNum))
}
*****

VOID  Main(){
    Byte RstBtn;

    RstBtn = GET_Value (BTN_STS, BTN_STS_R);      // Active Low
}
*****
```