

FWS-7360

Network Appliance

User's Manual 5th Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7360	1
● Console Cable	1
● Ear Brackets	2

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page on AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future reference.

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent the system from falling.
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader while the system is running.

16. Never pour any liquid into the openings. This could cause fire or electric shock.
17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**
20. The system must be grounded (earthed). The power plug must be connected to a properly wired ground-to-earth outlet. Failing to properly ground the system can place hazardous voltages across the metal parts of the system.

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System

QQ4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。
○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。
×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。
环保使用期限(EFUP (Environmental Friendly Use Period))：10 年
备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。
三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON System

QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU and Memory	×	○	○	○	○	○
Hard Disk	×	○	○	○	○	○
LCD Modules	×	○	○	○	○	○
CD-ROM/DVD-ROM	×	○	○	○	○	○
Touch Modules	×	○	○	○	○	○
Power	×	○	○	○	○	○
Battery	×	○	○	○	○	○
The table is prepared in accordance with the provisions of SJ/T 11364. ○ : Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572. × : Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1). EFUP (Environment Friendly Use Period) value: 10 years. Notes: 1. This product defined period of use is under normal condition. 2. In above part, CPU/Memory/ Hard Disk/CD-ROM/DVD-ROM/ Power are optional. 3. In above part, LCD Modules/ Touch Modules are for all-in-one product model.						

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Chapter 1

Product Specifications

1.1 Specifications

Platform

Form Factor	1U Rackmount Network Platform
Processor	Intel® C3758 SoC Processor, optional support up to 16 cores
Chipset	SoC
System Memory	DDR4 1866/2133/2400 ECC Up to 64GB 218-pin DIMM/RDIMM x 4

Network

Ethernet	Intel® X553 RJ45 x 2 Intel® i211 GbE x 3 SFP+ x 2 from CPU
Bypass	Onboard 2 pairs bypass, others depend on NIM module
NIM Slot	1

Display

Graphics Controller	-
Connector	-

Storage

HDD	2.5" HDD Bay x 2
CF/CFast/mSATA	Default SATA III port x 2 (MSATA Slot X 2 Optional)

Expansion / Internal Interface

PCIe Slot	PCIe [x8] slot x 1, cannot use w/ NIM
Mini-PCIe Slot	Default Mini-Card socket (full-size) x1 (Optional) Mini-Card socket (full-size) with SIM socket x 1
IPMI	—
KB Mouse	—
USB	USB 3.0 x 2

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	GPIO Programmable Button x 1
TPM	Optional TPM v1.2 / TPM v2.0
GPIO	4 bits input, 4bits output
Fan	System Fan x 1
MTBF (Hours)	142412 Hours
Color	Black

Environmental Parameters and Dimension

Power Requirement	100W Flex ATX PSU
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz / operation (2.5" HDD) 1.5 Grms/ 5 ~ 500Hz / non operation
Shock	10 G peak acceleration (11 m sec. duration), operation 20 G peak acceleration (11 m sec. duration), non-operation
Dimension (W X D X H)	16.93" x 12.01" x 1.73" (430mm x 305mm x 44mm)

I/O Interface

Front Panel

SFP+ with LED x 2
RJ45 Ethernet Port with LED x 5
USB 3.0 x 2
RJ45 Console x 1
Software Programmable Button x 1
Parallel LCM Display and 4 Keypad x 1
LED for Power/HDD/ Status/ Bypass x 5
NIM Slot x 1
Bypass LED x 2
Power LED x1
HDD LED x1
Status LED x1

Rear Panel

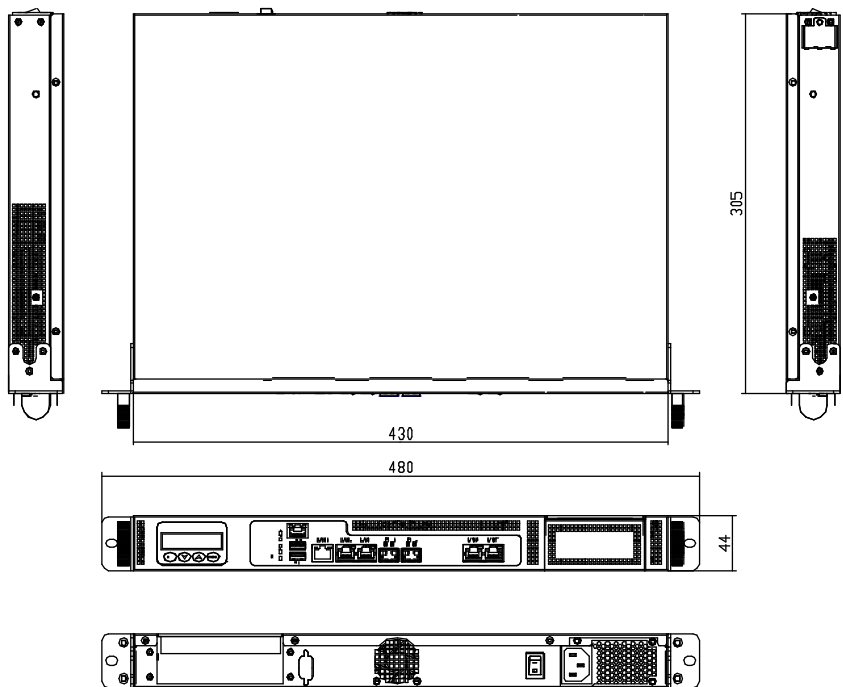
Power Switch x 1
AC Power Input x 1
Rear Expansion Slot x 1

Chapter 2

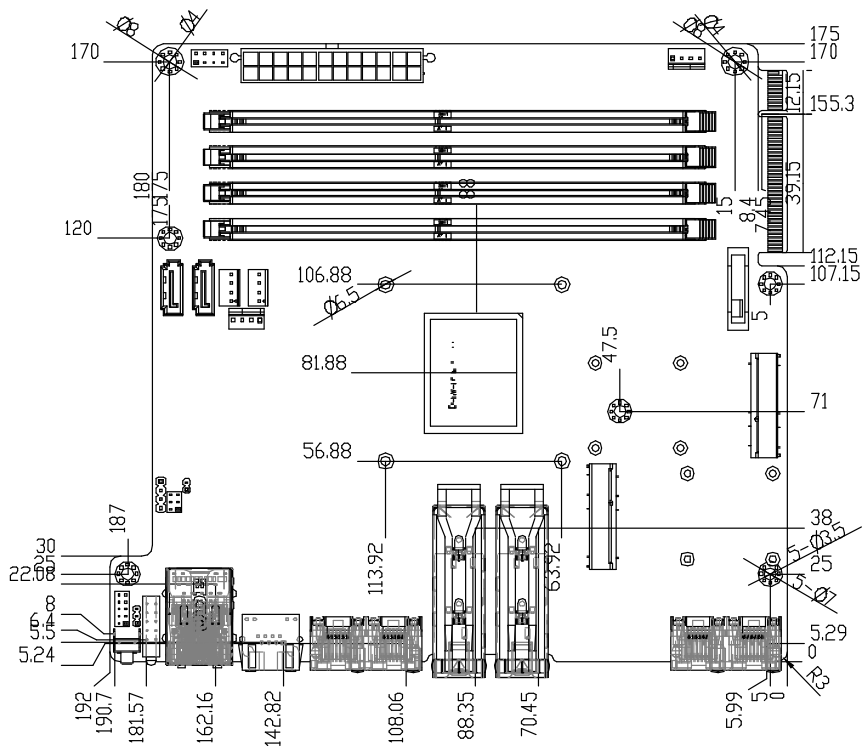
Hardware Information

2.1 Dimensions

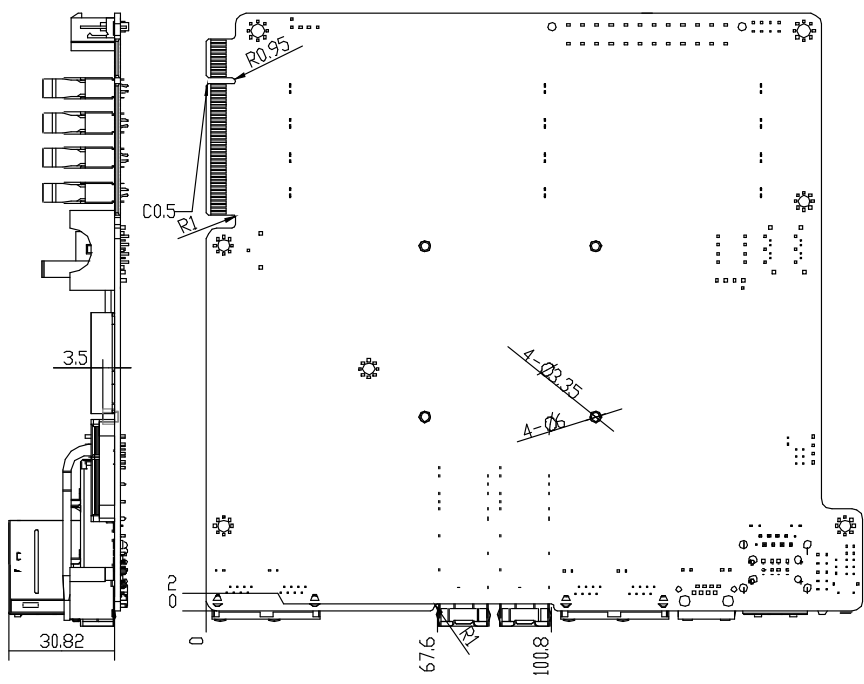
System



Component Side

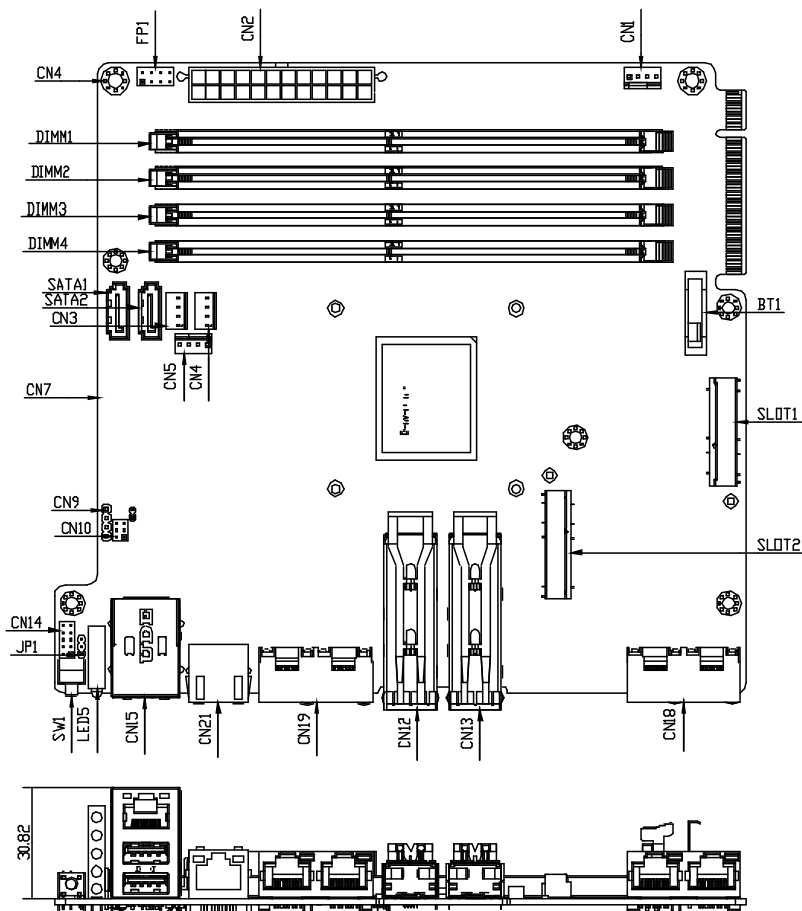


Solder Side

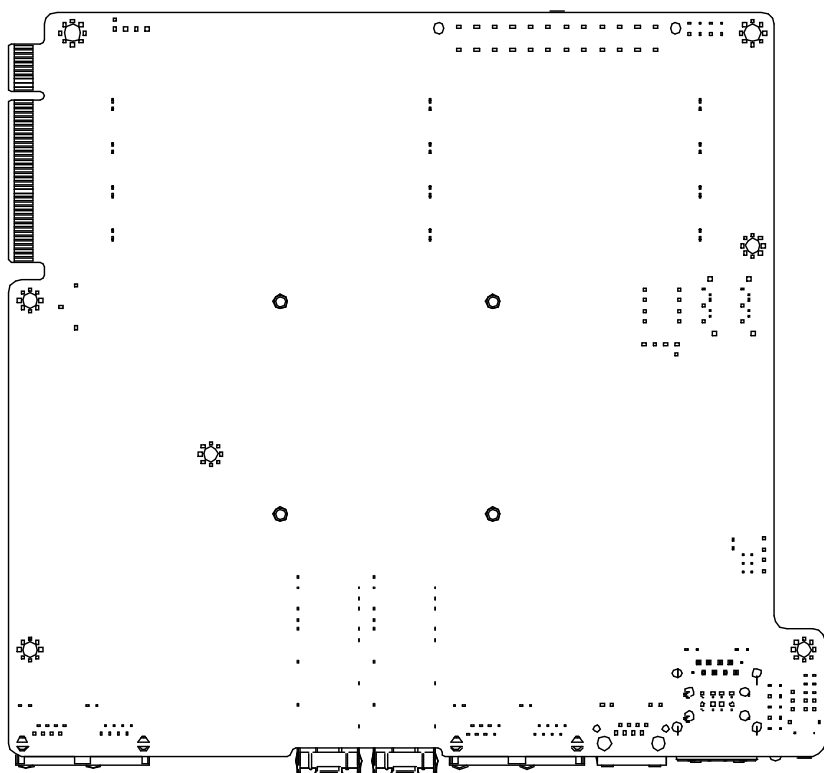


2.2 Jumpers and Connectors

Component Side



Solder Side



2.3 Jump Settings

2.3.1 Auto Power Button (JP1)

Normal	1-2
Auto power on	2-3

2.3.2 Clear CMOS (CN10)

Normal	1-3,2-4
Clear CMOS	3-5,4-6

2.4 Connector Pin Assignments

2.4.1 Front Panel (FP1)

Pin	Signal	Pin	Signal
1	FB_PWSIN#	2	GND
3	RESET	4	GND
5	Power LED+	6	Power LED-
7	HDD LED+	8	HDD LED-

2.4.2 CASEOPEN Pin Header (CN8)

Pin	Signal	Pin	Signal
1	CaseOpen	2	GND

2.4.3 LCM KeyPad Header (CN9)

Pin	Signal	Pin	Signal
1	Down	2	Up
3	Right	4	Left

2.4.4 Digital IO Pin Header (CN14)

Pin	Signal	Pin	Signal
1	DIO bit1	2	DIO bit2
3	DIO bit3	4	DIO bit4
5	DIO bit5	6	DIO bit6

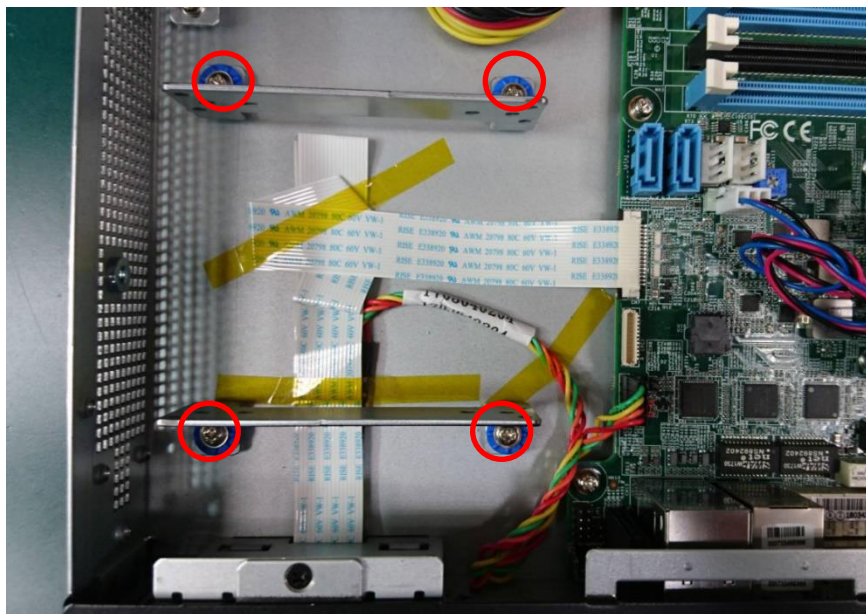
7	DIO bit7	8	DIO bit8
9	+5V	10	GND

2.5 Installing the 2.5"x2 Hard Disk Driver

1. Unscrew the upper lid



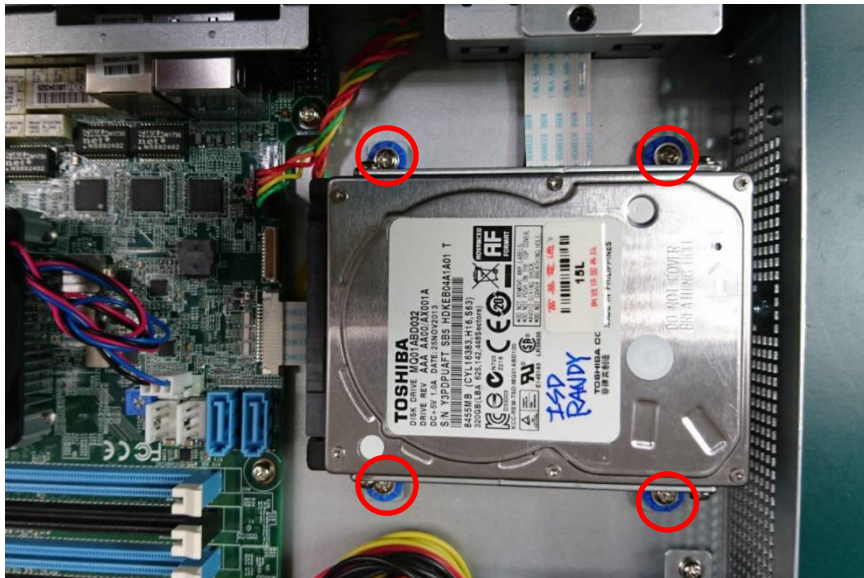
2. Remove the four screws



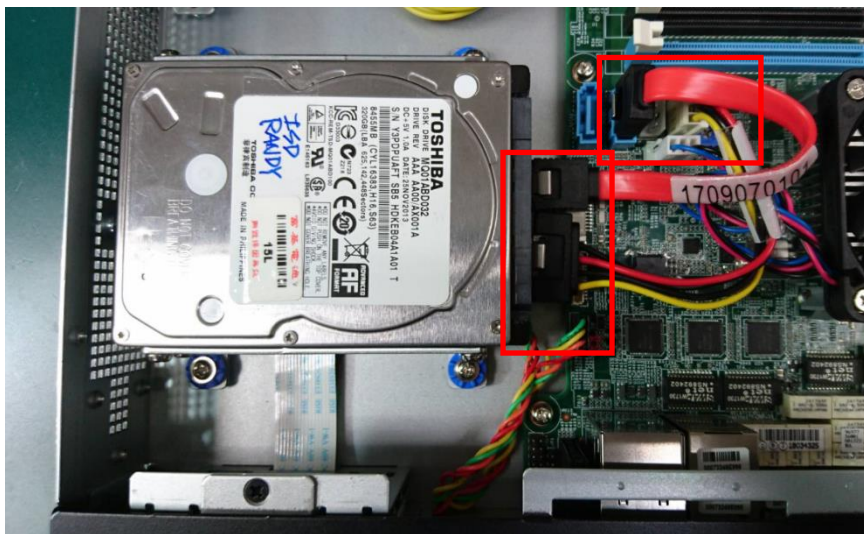
- Secure the HDD to the HDD bracket with eight screws



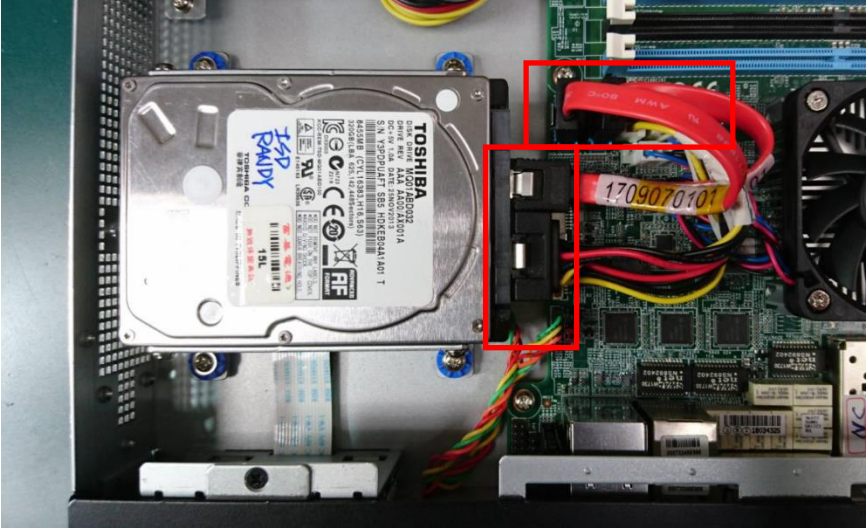
- Secure the HDD bracket to the chassis with four screws



- Connect the SATA and power cables to the lower hard disk



6. Connect the SATA and power cables to the upper hard disk



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

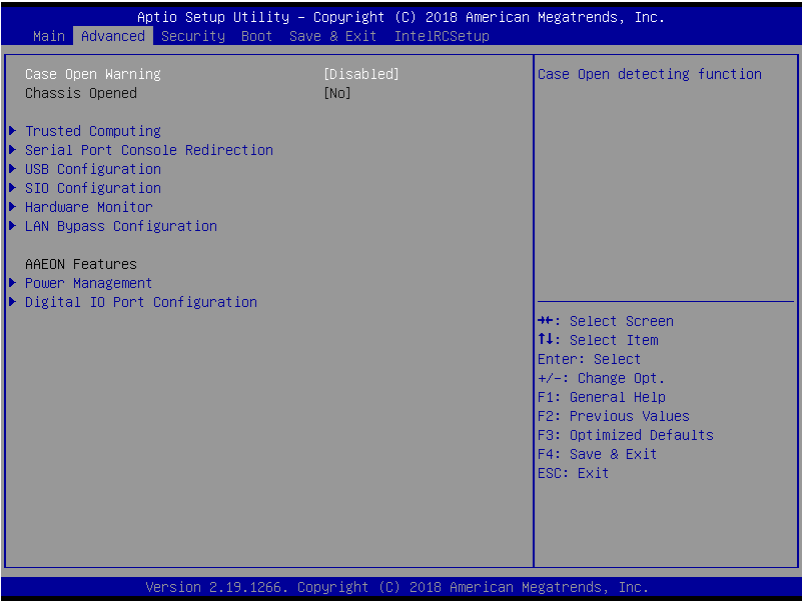
Save & Exit – Save your changes and exit the program

IntelRCSetup – For host bridge parameters

3.3 Setup Submenu: Main



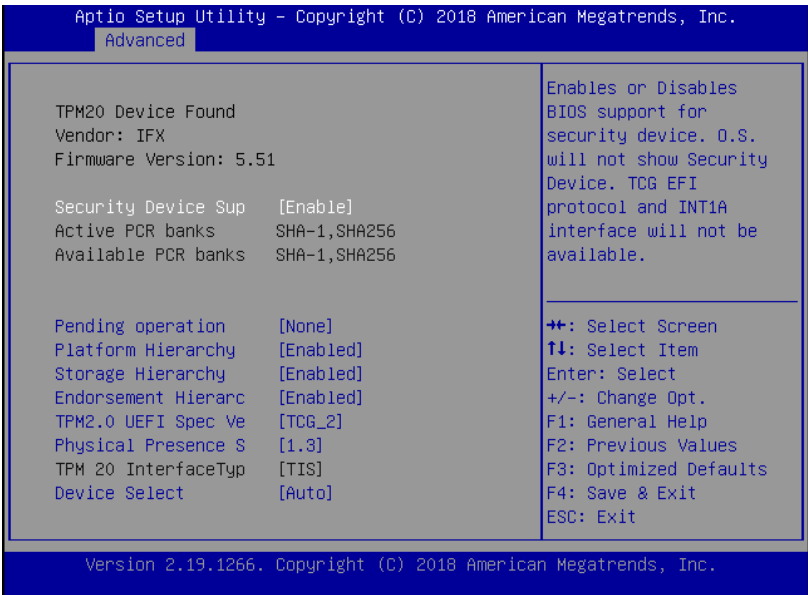
3.4 Setup Submenu: Advanced



Options summary:

Case Open Warning	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Clear	
Case Open detecting function		

3.4.1 Advanced: Trusted Computing

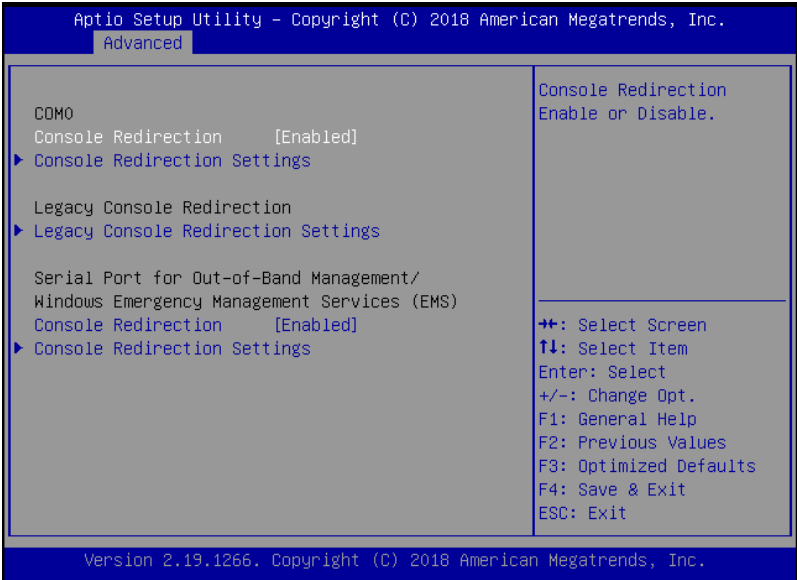


Options summary:

Security Device Sup	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default

Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec	TCG_1_2	
Version	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support,		
TCG_1_2 : the Compatible mode for Win8/Win10		
TCG_2 : Support new TCG2 protocol and event		
Physical Presence	1.2	
Spec Version	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

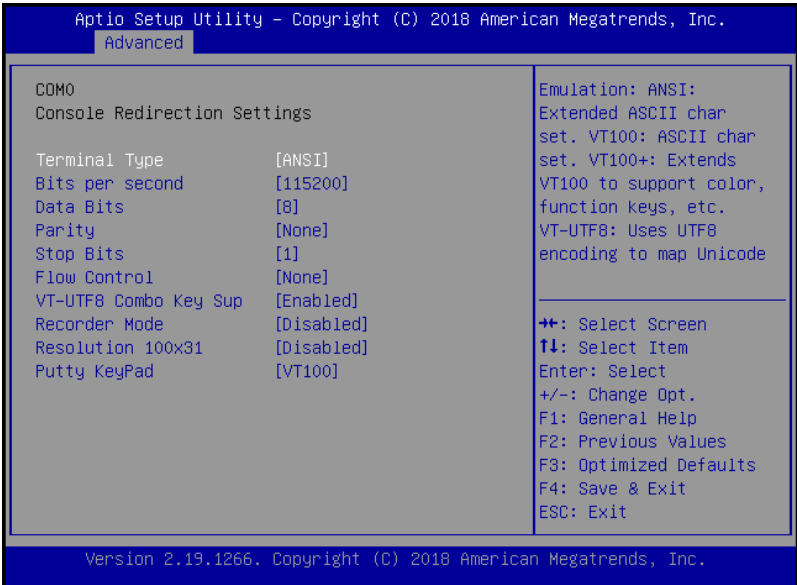
3.4.2 Advanced: Serial Port Console Redirection



Options summary:

COM0		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Console Redirection Settings		
Legacy Console Redirection		
Legacy Console Redirection Settings		
Serial Port for Out-of-Band Management / Windows Emergency Management Services		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Console Redirection Settings		

3.4.2.1 COM0 Console Redirection

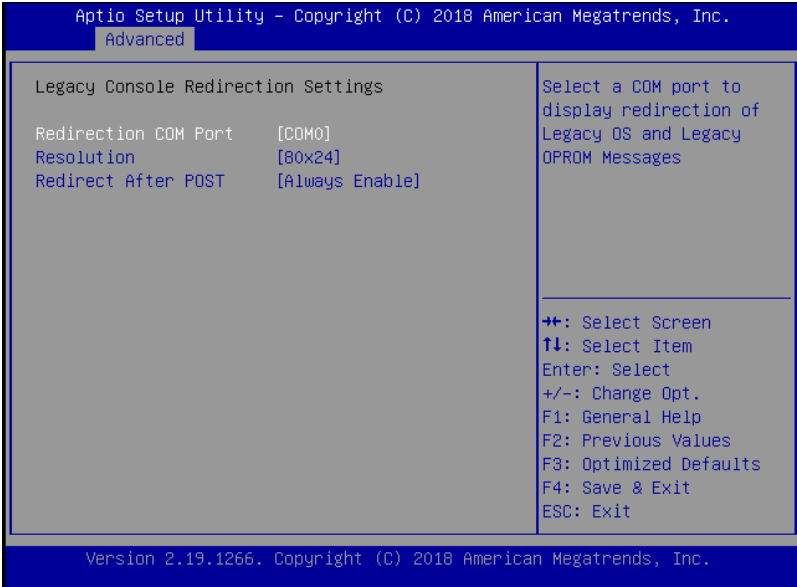


Options summary:

Terminal Type	VT100	
	VY100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation :		
ANSI : Extended ASCII char set.		
VT100 : ASCII char set.		
VT100+ : Extends VT100 to support color, function keys, etc.		
VT-UTF8 : Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	
	57600	
	11520	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data bit	7	

	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

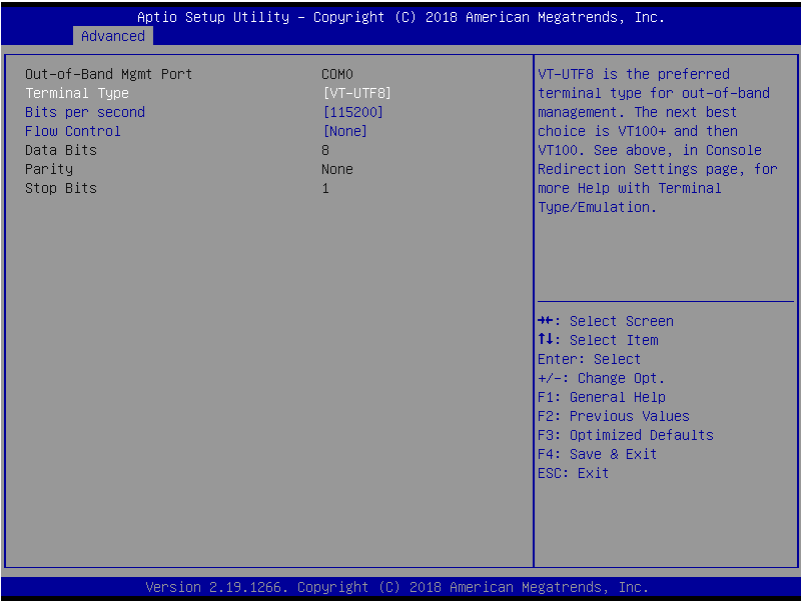
3.4.2.2 Legacy Console Redirection Settings



Options summary:

Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPRM Messages.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection.		
Redirection After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When BootLoader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is		

3.4.2.3 Console Redirection Settings

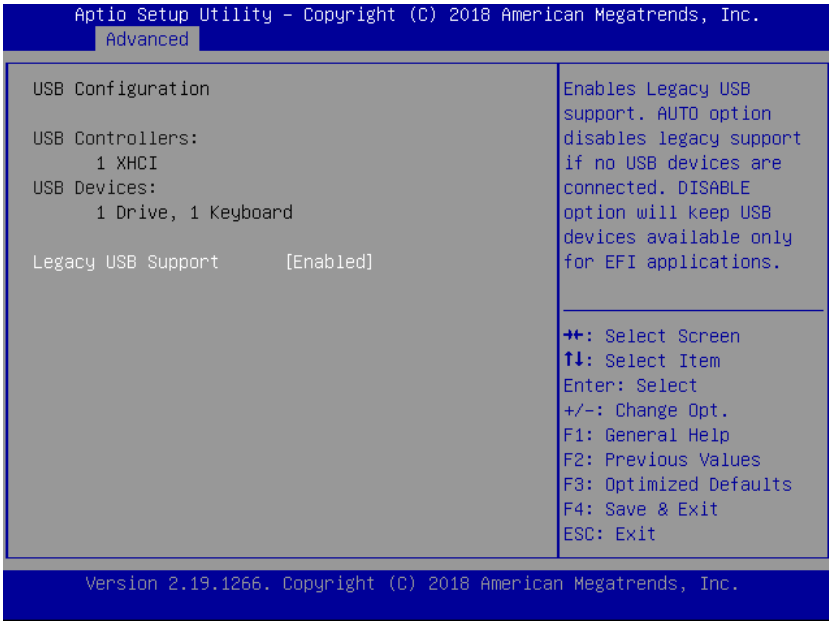


Options summary:

Terminal Type	VT100	
	VT100+	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits per second	9600	
	19200	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software Xon/Xoff	

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

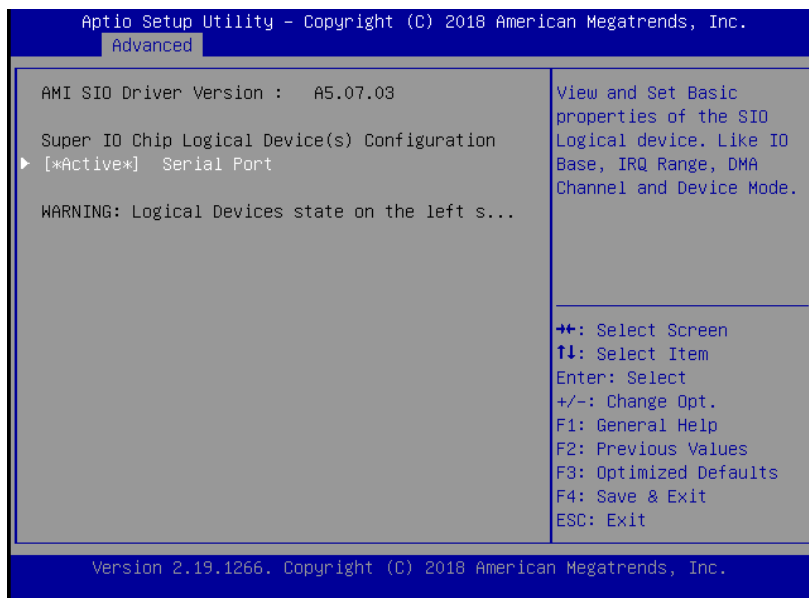
3.4.3 Advanced: USB Configuration



Options summary:

Legacy USB Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

3.4.4 Advanced: SIO Configuration



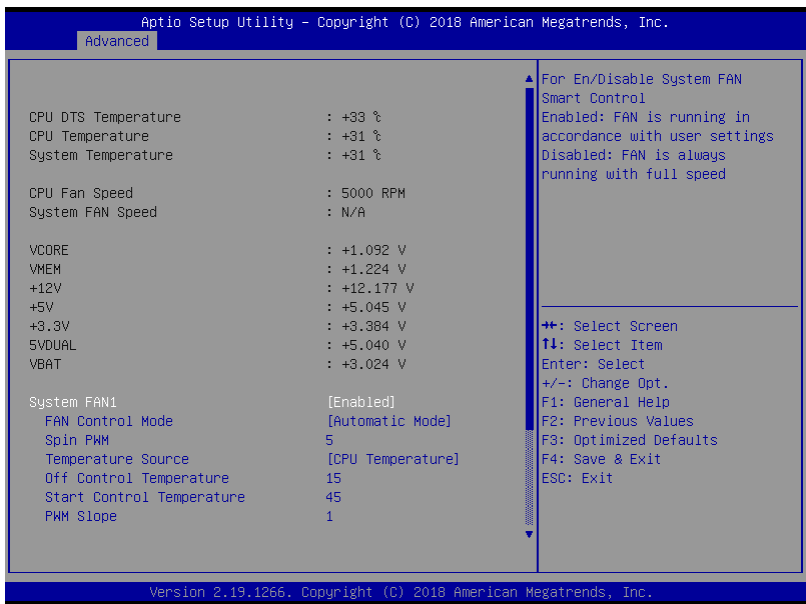
3.4.4.1 Serial Port Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.5 Advanced: Hardware Monitor

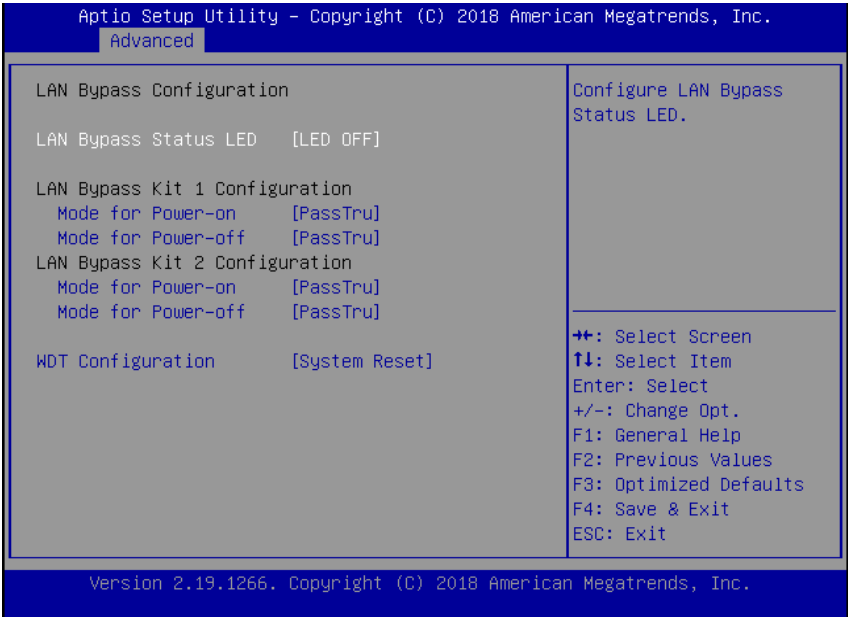


Options summary:

System Fan1	Enabled	Optimal Default, Failsafe Default
	Disabled	
For En/Disable System FAN1 Smart Control\nEnabled: FAN is running in accordance with user settings\nDisabled: FAN is always running with full speed		
FAN Control Mode	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Manual Mode: Depends on PWM Duty\nAutomatic Mode: FAN Speed is depends on CPU Temperature		
Spin PWM	5	Optimal Default, Failsafe Default
The PWM Duty of FAN Spin\nRange:[0 - 255]		
Temperature Source	CPU Temperature	Optimal Default, Failsafe Default
	System Temperature	
Reference Temperature Input Selection.		
n0x00 : TMPIN1		
n0x01 : TMPIN2		
n0x02 : TMPIN3		

Off Control Temperature	15	Optimal Default, Failsafe Default
Temperature Limit Value of Fan Off\nNote: Some fans have the minimum speed even if the PWM value is 0		
Start Control Temperature	45	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Start Control		
PWM Slope	1	Optimal Default, Failsafe Default
Slope PWM value/Degree C for FAN Speed Control\nRange:[1-15]		
System Fan2	Enabled	Optimal Default, Failsafe Default
	Disabled	
For En/Disable System FAN1 Smart Control\nEnabled: FAN is running in accordance with user settings\nDisabled: FAN is always running with full speed		
FAN Control Mode	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Manual Mode: Depends on PWM Duty\nAutomatic Mode: FAN Speed is depends on CPU Temperature		
Spin PWM	5	Optimal Default, Failsafe Default
The PWM Duty of FAN Spin\nRange:[0 - 255]		
Temperature Source	CPU Temperature	Optimal Default, Failsafe Default
	System Temperature	
Reference Temperature Input Selection. n0x00 : TMPIN1 n0x01 : TMPIN2 n0x02 : TMPIN3		
Off Control Temperature	15	Optimal Default, Failsafe Default
Temperature Limit Value of Fan Off\nNote: Some fans have the minimum speed even if the PWM value is 0		
Start Control Temperature	45	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Start Control		
PWM Slope	1	Optimal Default, Failsafe Default
Slope PWM value/Degree C for FAN Speed Control\nRange:[1-15]		

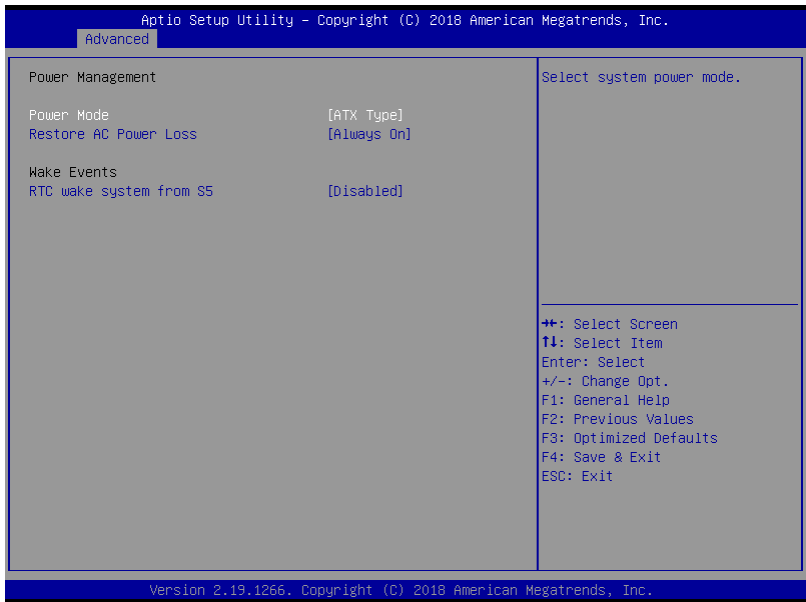
3.4.6 Advanced: LAN Bypass Configuration



Options summary:

Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
LAN Bypass Status LED		
Mode for Power-on	ByPass	Optimal Default, Failsafe Default
	PassTru	
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through)		
Mode for Power-off	ByPass	Optimal Default, Failsafe Default
	PassTru	
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through)		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure LAN kit behavior when WDT is triggered. (Bypass/Pass Through)		

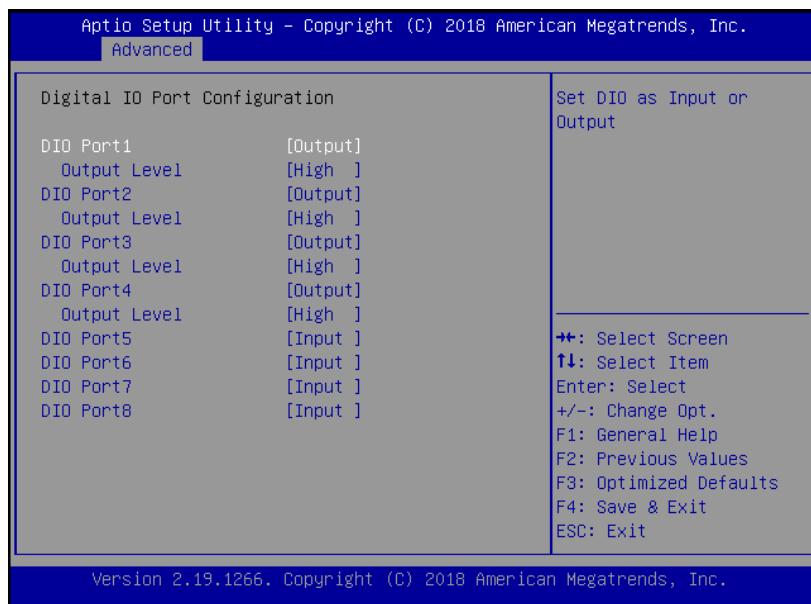
3.4.7 Advanced: Power Management



Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time : System will wake on the hr :: min :: sec		
Specified Dynamic Time : System will wake on the current time + Increase minutes(s).		

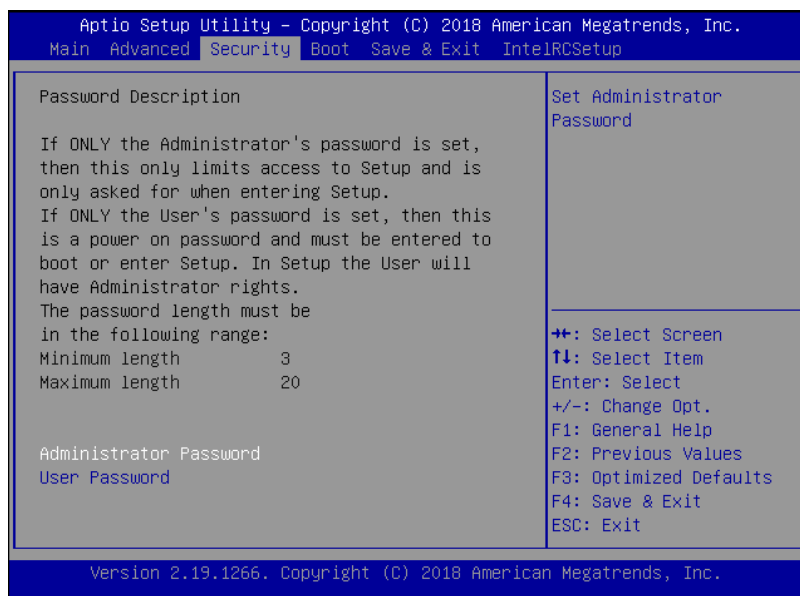
3.4.8 Advanced: Digital IO Port Configuration



Options summary:

DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		

3.5 Setup submenu: Security



Change User/Administrator Password

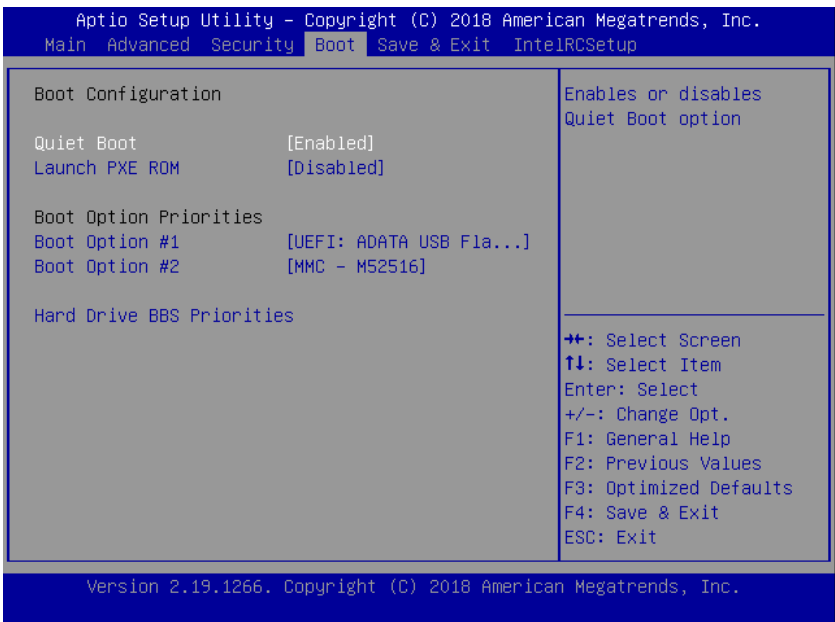
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.6 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable Quiet Boot option.		
Launch PXE Rom	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		
Boot Option #1	UEFI OS (Lilee System SSM 1GB 0910)	Optimal Default, Failsafe Default
	Disabled	
Sets the system boot order.		

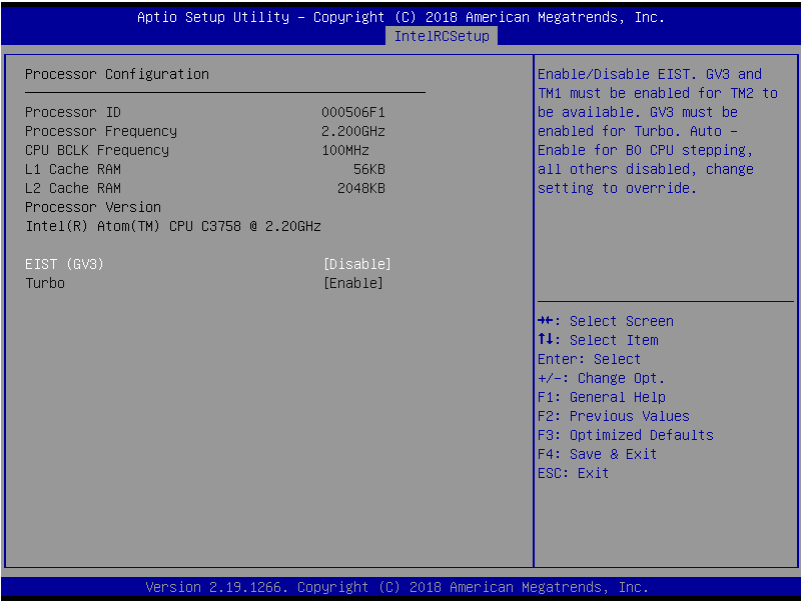
3.7 Setup submenu: Save & Exit



3.8 Setup submenu: IntelRCSetup



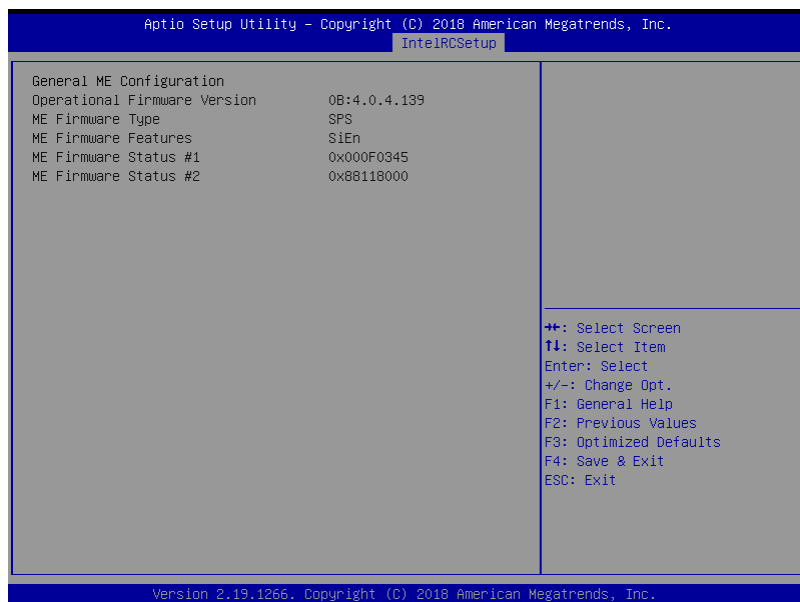
3.8.1 IntelRCSetup: Processor Configuration



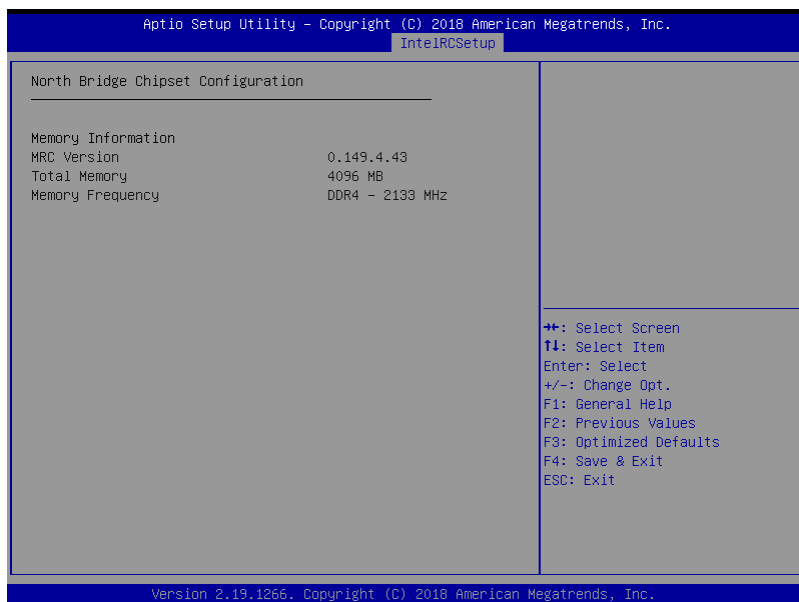
Options summary:

EIST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable EIST. GV3 and TM1 must be enabled for TM2 to be available. GV3 must be enabled for Turbo. Auto - Enable for B0 CPU stepping, all others disabled, change setting to override.		
Turbo Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable CPU Turbo capability. This option only applies to ES2 and above.		

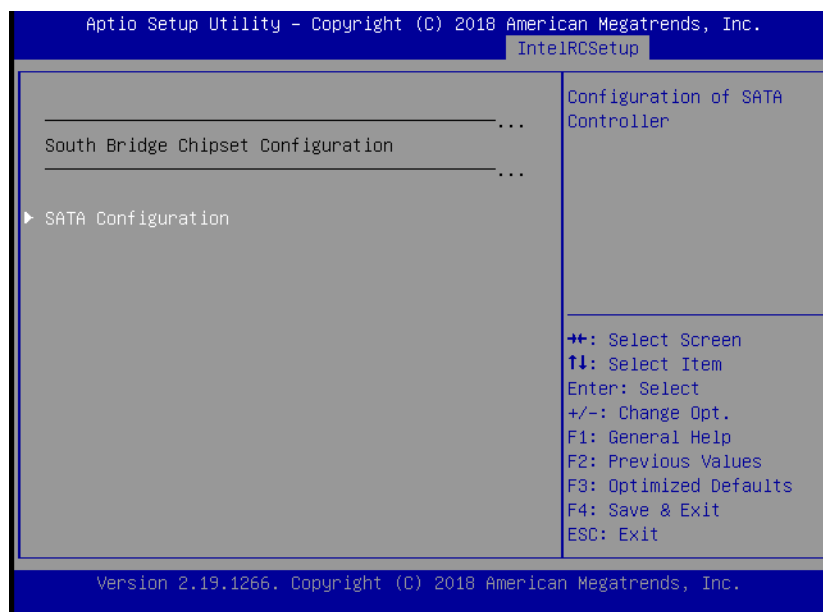
3.8.2 IntelRCSetup: Server ME Configuration



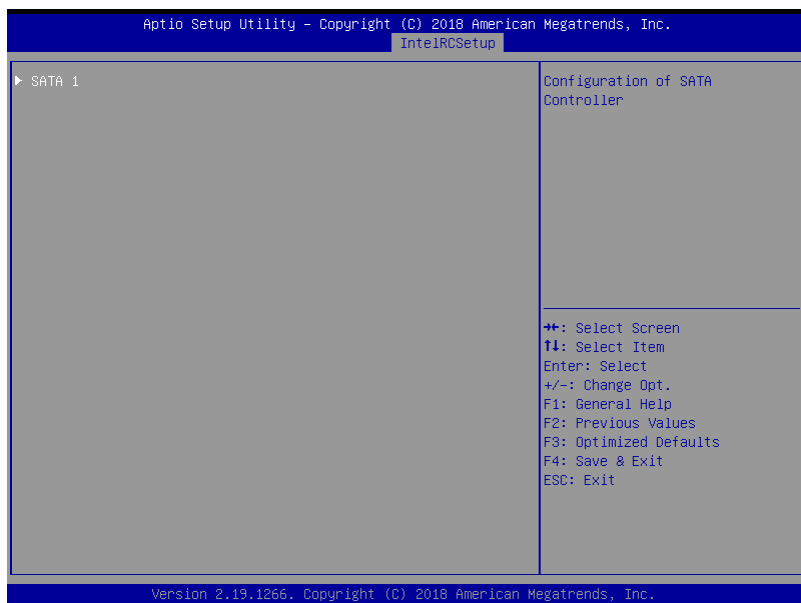
3.8.3 IntelRCSetup: North Bridge Chipset Configuration



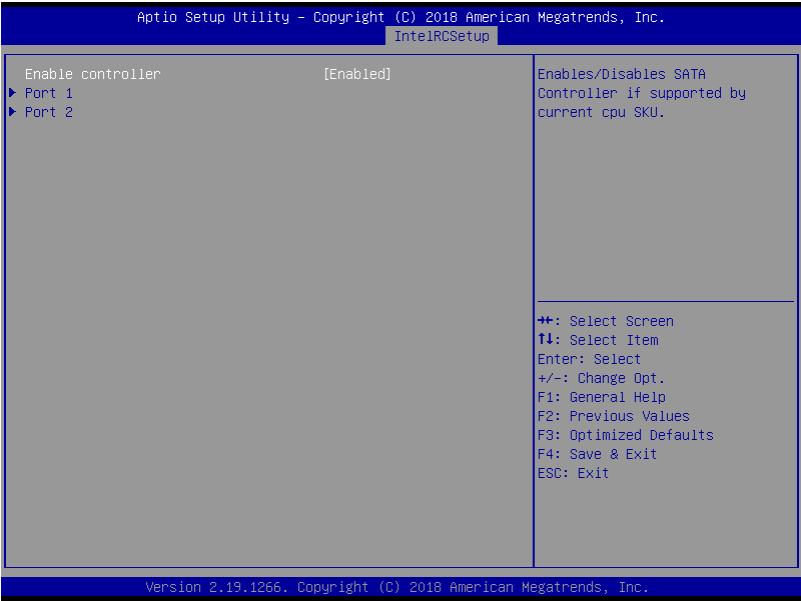
3.8.4 IntelRCSetup: South Bridge Chipset Configuration



3.8.4.1 SATA Configuration



3.8.4.1.1 SATA 1

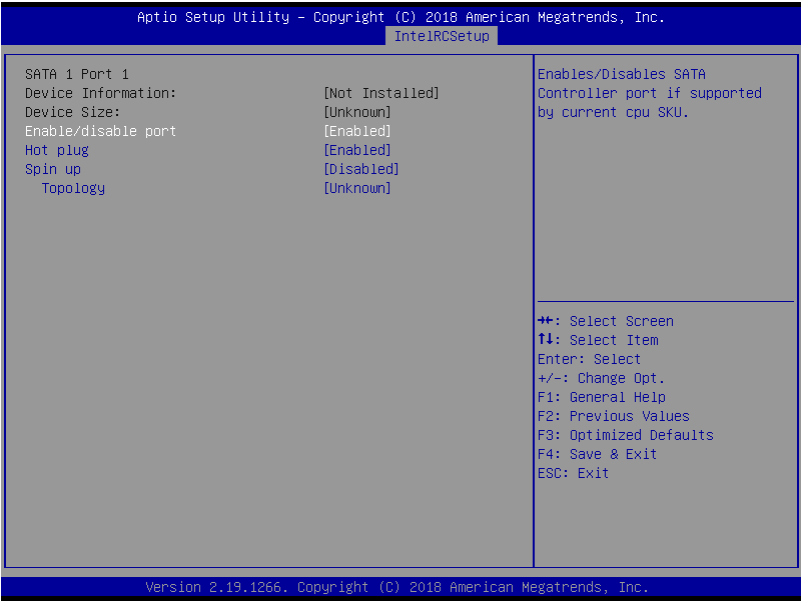


Options summary:

Enable controller	Enabled	Optimal Default, Failsafe Default
	Disabled	

Enable or disable the Chipset SATA Controller. The Chipset SATA Controller support the 2 black internal SATA ports (up to 3Gb/s supported per port).

3.8.4.1.1.1 SATA 1 Port 1/2



Options summary:

Enable/disable port	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables/Disables SATA Controller port if supported by current cpu SKU.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Hot Plug		
Spin up	Disabled	Optimal Default, Failsafe Default
	Enabled	
Spin up		
Topology	Unknown	Optimal Default, Failsafe Default
	ISATA	
	Direct Connect	
	Flex	
	M2	
Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2.		

Chapter 4

Drivers Installation

4.1 Driver Installation

Please download the driver from the AAEON website -

<http://www.aaeon.com/en/p/desktop-network-appliance-fws-7360>. It contains all the drivers and utilities you need to set up your product. Follow the steps below to install the drivers.

For Linux:

Step 1 – Open the Step 1 – LAN\Linux folder

Step 2 – Double click ixgbe-5.1.3.tar.gz

Step 3 – Double click igb-5.3.5.7.tar.gz

Step 4 – Follow the README instructions

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIODData   //This parameter is represented from Note2
#define void    IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN  //This parameter is represented from Note9
#define byte   EnableReg  //This parameter is represented from Note10
#define byte   EnableBit  //This parameter is represented from Note11
#define byte   EnableVal  //This parameter is represented from Note12
#define byte   StatusLDN  // This parameter is represented from Note13
#define byte   StatusReg  // This parameter is represented from Note14
#define byte   StatusBit  // This parameter is represented from Note15
*****

```

```
*****  
VOID Main() {  
    // Procedure : AaeonWDTConfig  
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)  
    // (boolean)Unit : Select time unit(0: second, 1: minute).  
    AaeonWDTConfig();  
  
    // Procedure : AaeonWDTEnable  
    // This procedure will enable the WDT counting.  
    AaeonWDTEnable();  
}  
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID SIOEnterMBPnPMode(){
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****

```

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){

Byte TmpValue;

SIOEnterMBPnPMode();

SIOSelectLDN(byte LDN);

IOWriteByte(SIOIndex, Register);

TmpValue = IOReadByte(SIOData);

TmpValue &= ~(1 << BitNum);

TmpValue |= (Value << BitNum);

IOWriteByte(SIOData, TmpValue);

SIOExitMBPnPMode();

}

VOID SIOByteSet(byte LDN, byte Register, byte Value){

SIOEnterMBPnPMode();

SIOSelectLDN(LDN);

IOWriteByte(SIOIndex, Register);

IOWriteByte(SIOData, Value);

SIOExitMBPnPMode();

}

Appendix B

I/O Information

B.1 I/O Address Map

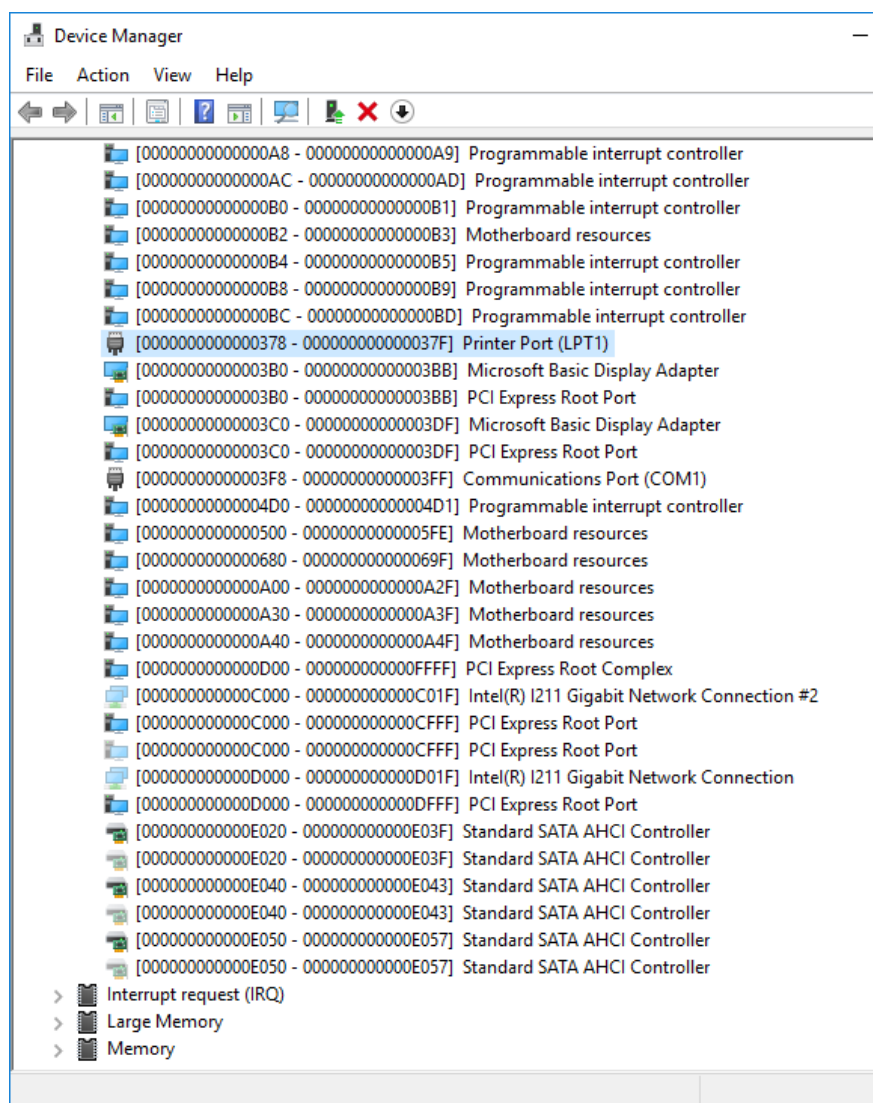
Device Manager

File Action View Help

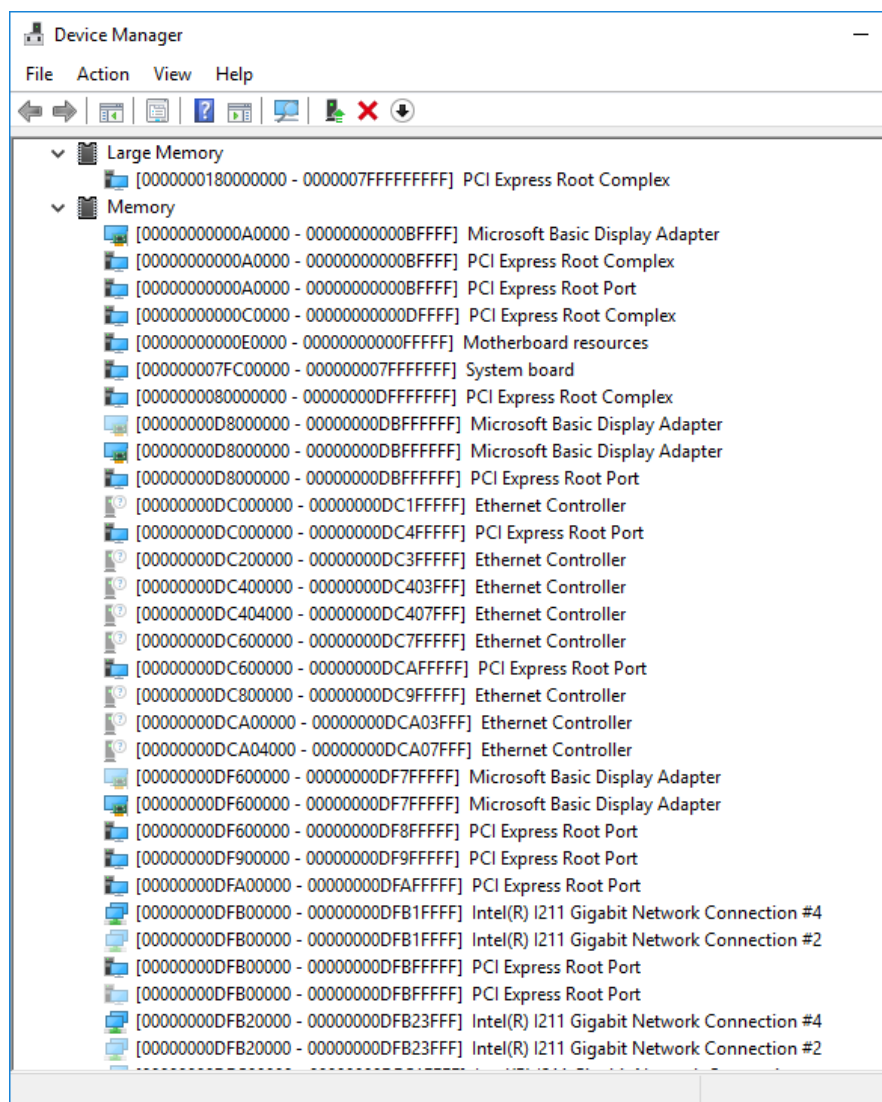
← → ↻ ? 🖨

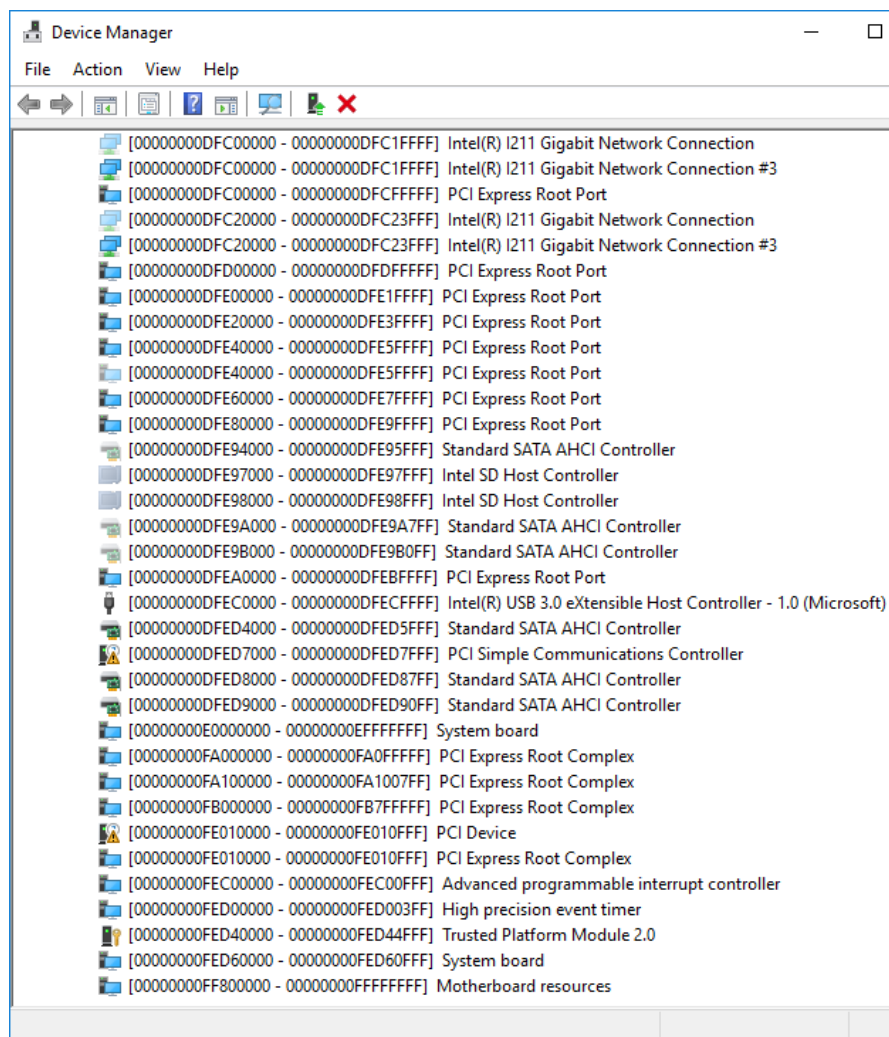
▼ **Input/output (IO)**

- 📁 [0000000000000000 - 000000000000CF7] PCI Express Root Complex
- 📁 [0000000000000020 - 0000000000000021] Programmable interrupt controller
- 📁 [0000000000000024 - 0000000000000025] Programmable interrupt controller
- 📁 [0000000000000028 - 0000000000000029] Programmable interrupt controller
- 📁 [000000000000002C - 000000000000002D] Programmable interrupt controller
- 📁 [000000000000002E - 000000000000002F] Motherboard resources
- 📁 [0000000000000030 - 0000000000000031] Programmable interrupt controller
- 📁 [0000000000000034 - 0000000000000035] Programmable interrupt controller
- 📁 [0000000000000038 - 0000000000000039] Programmable interrupt controller
- 📁 [000000000000003C - 000000000000003D] Programmable interrupt controller
- 📁 [0000000000000040 - 0000000000000043] System timer
- 📁 [000000000000004E - 000000000000004F] Motherboard resources
- 📁 [0000000000000050 - 0000000000000053] System timer
- 📁 [0000000000000060 - 0000000000000060] Standard PS/2 Keyboard
- 📁 [0000000000000061 - 0000000000000061] Motherboard resources
- 📁 [0000000000000063 - 0000000000000063] Motherboard resources
- 📁 [0000000000000064 - 0000000000000064] Standard PS/2 Keyboard
- 📁 [0000000000000065 - 0000000000000065] Motherboard resources
- 📁 [0000000000000067 - 0000000000000067] Motherboard resources
- 📁 [0000000000000070 - 0000000000000070] Motherboard resources
- 📁 [0000000000000070 - 0000000000000077] System CMOS/real time clock
- 📁 [0000000000000080 - 0000000000000080] Motherboard resources
- 📁 [0000000000000092 - 0000000000000092] Motherboard resources
- 📁 [00000000000000A0 - 00000000000000A1] Programmable interrupt controller
- 📁 [00000000000000A4 - 00000000000000A5] Programmable interrupt controller
- 📁 [00000000000000A8 - 00000000000000A9] Programmable interrupt controller
- 📁 [00000000000000AC - 00000000000000AD] Programmable interrupt controller
- 📁 [00000000000000B0 - 00000000000000B1] Programmable interrupt controller
- 📁 [00000000000000B2 - 00000000000000B3] Motherboard resources
- 📁 [00000000000000B4 - 00000000000000B5] Programmable interrupt controller
- 📁 [00000000000000B8 - 00000000000000B9] Programmable interrupt controller
- 📁 [00000000000000BC - 00000000000000BD] Programmable interrupt controller
- 🖨 [0000000000000378 - 000000000000037F] Printer Port (LPT1)



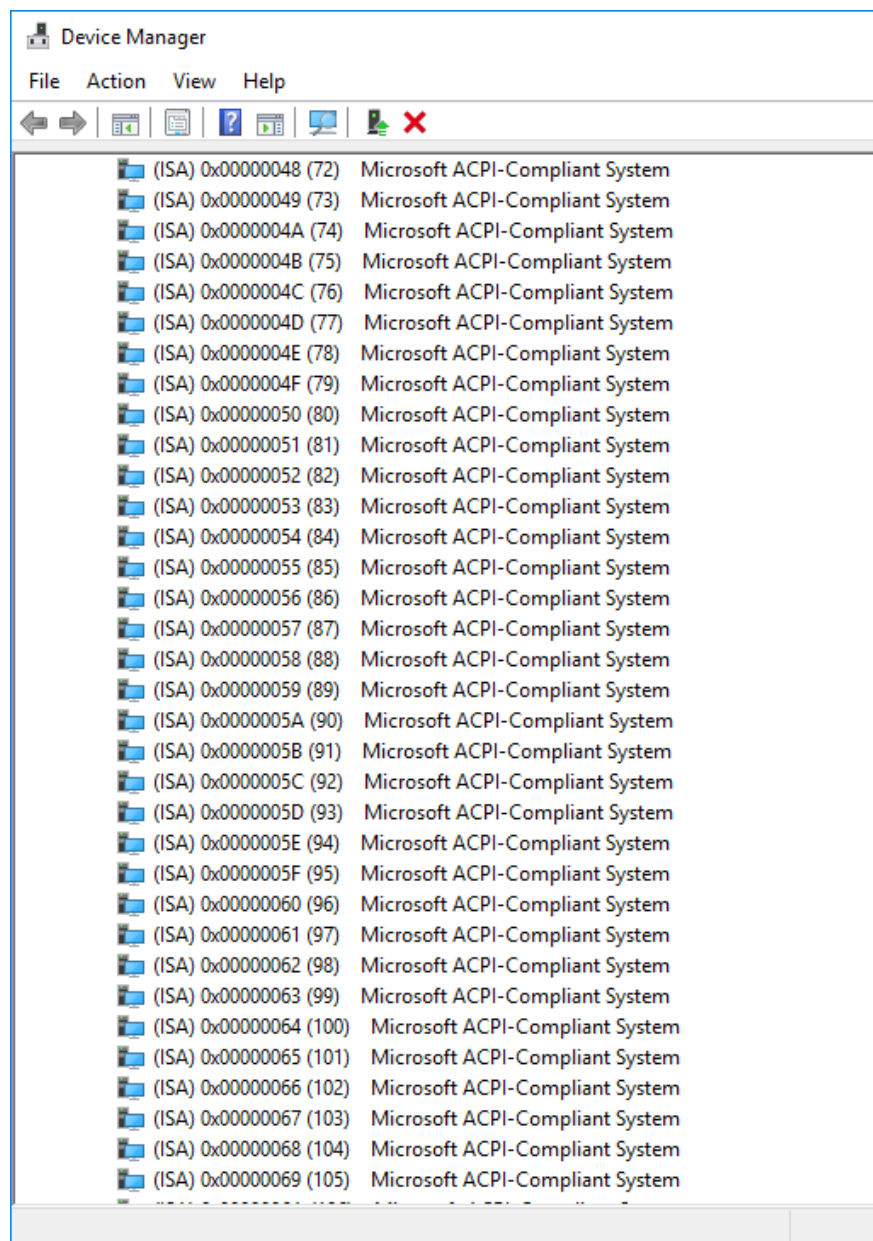
B.2 Memory Address Map

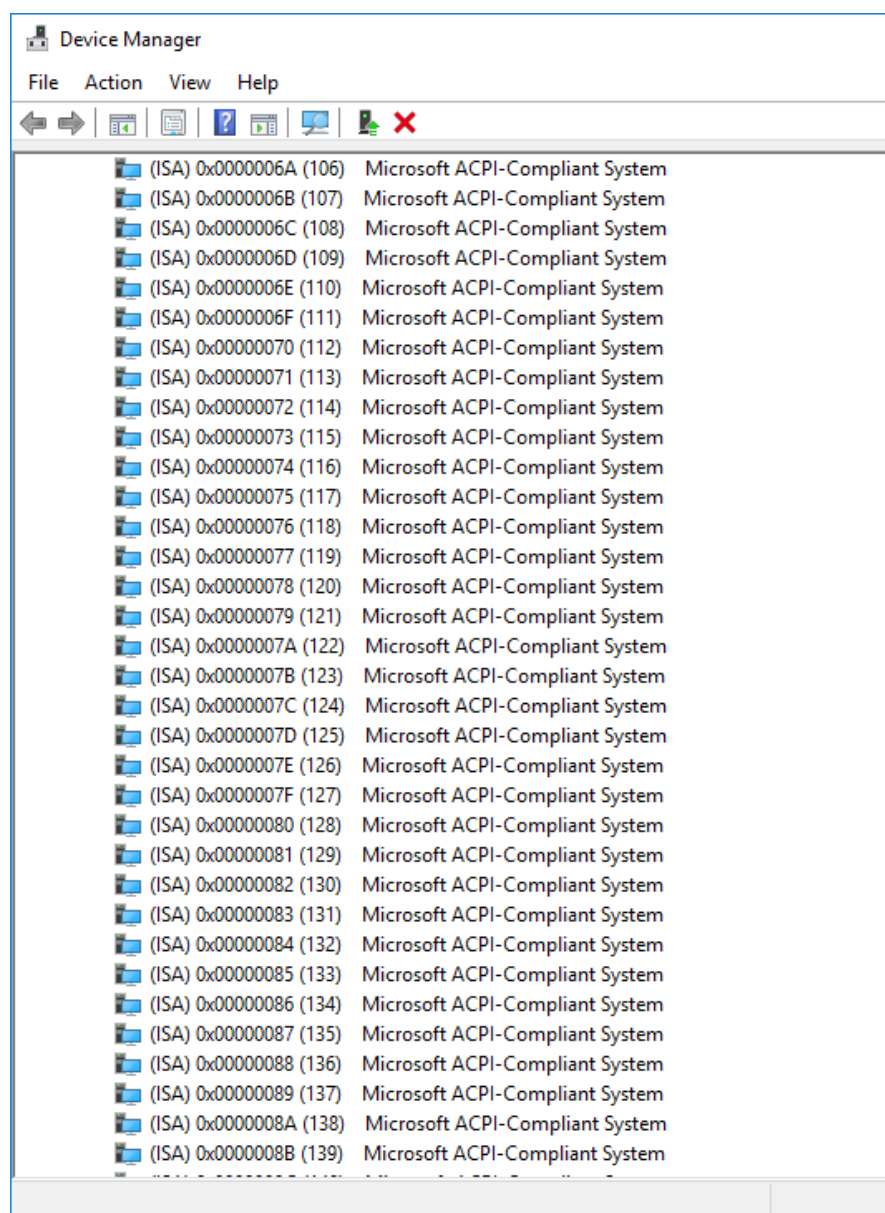


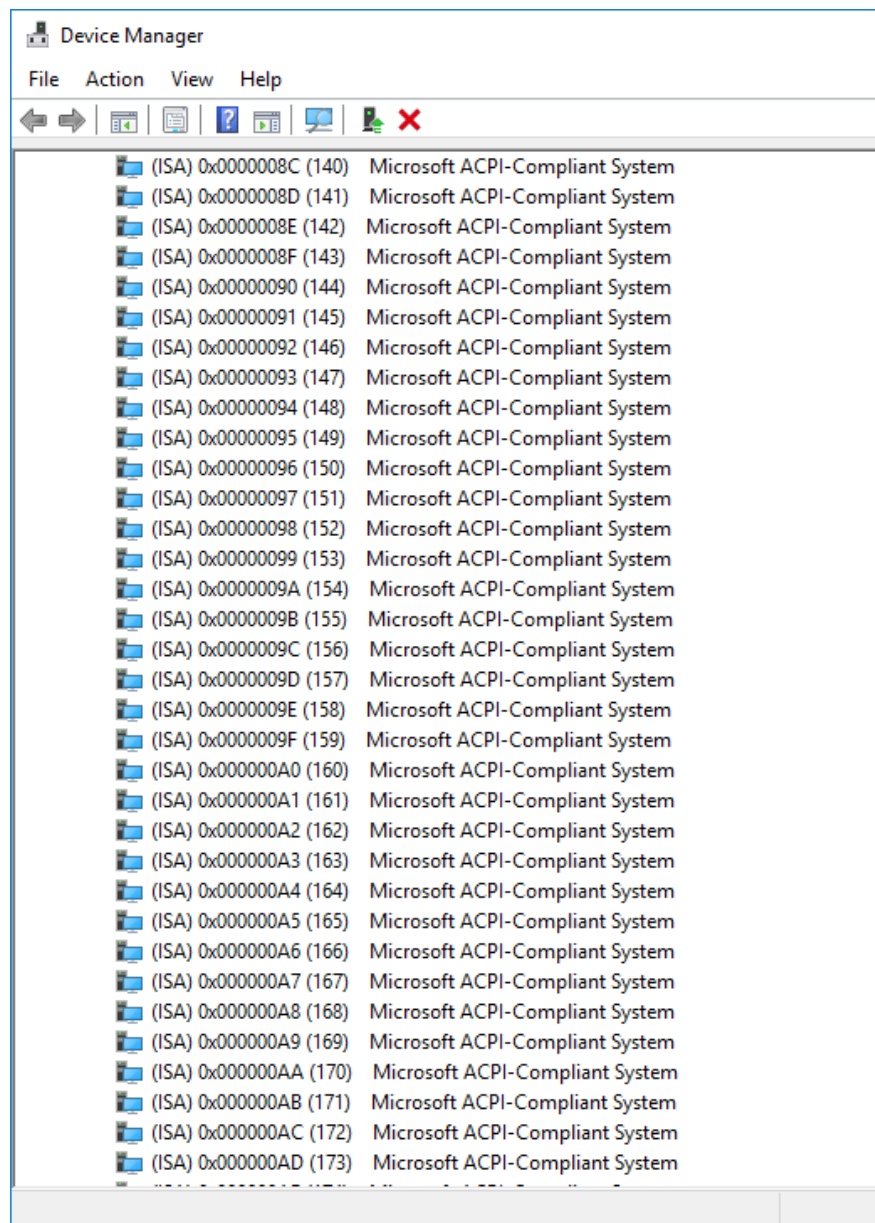


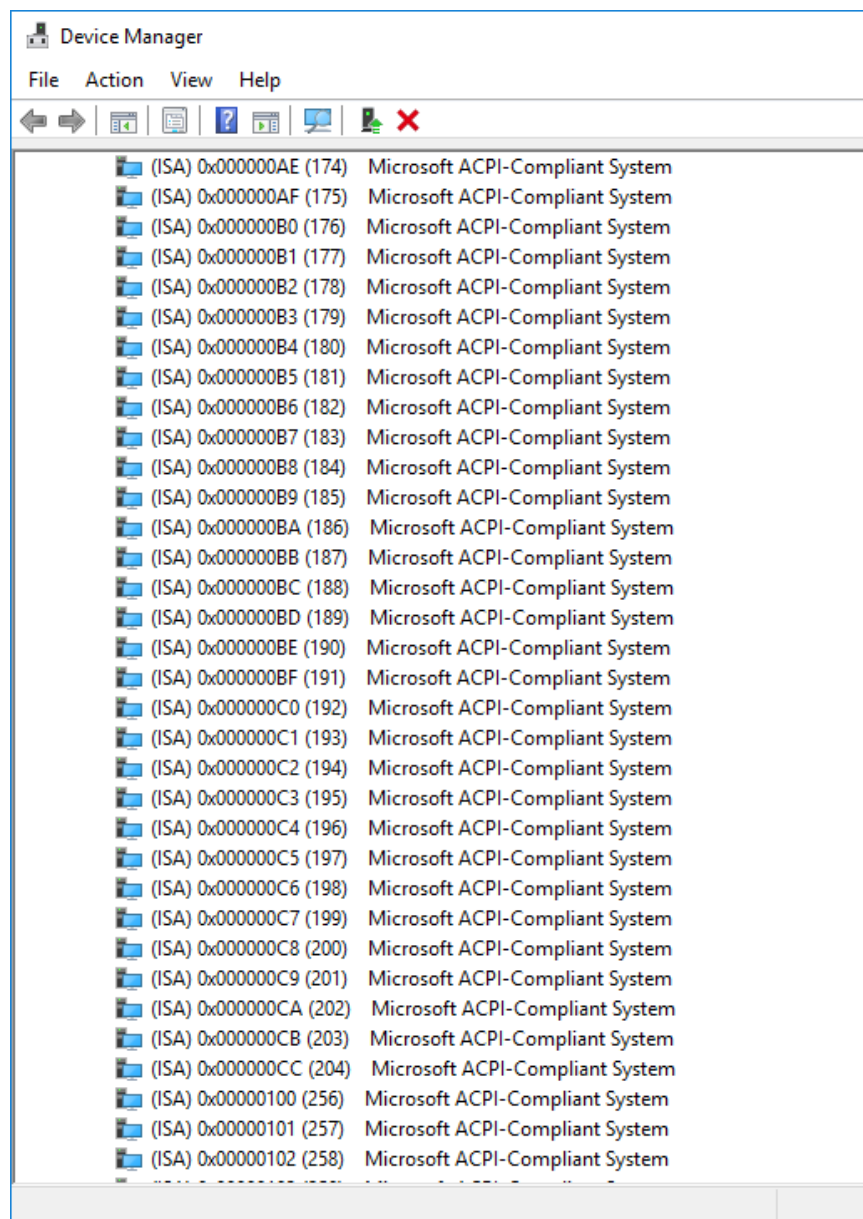
B.3 IRQ Mapping Chart

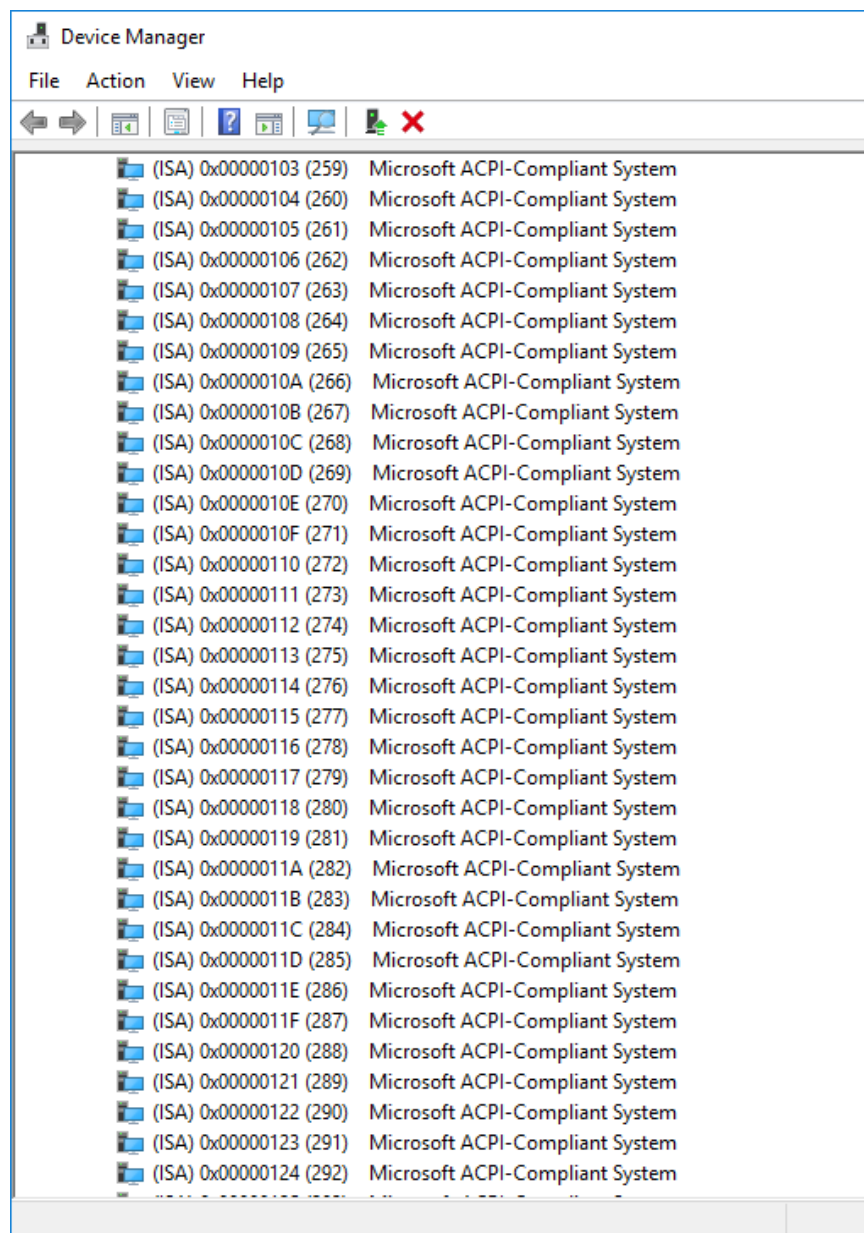
Device Manager		
File Action View Help		
▼ Interrupt request (IRQ)		
(ISA) 0x00000000 (00)	System timer	
(ISA) 0x00000001 (01)	Standard PS/2 Keyboard	
(ISA) 0x00000004 (04)	Communications Port (COM1)	
(ISA) 0x00000008 (08)	System CMOS/real time clock	
(ISA) 0x0000000A (10)	Ethernet Controller	
(ISA) 0x0000000A (10)	Ethernet Controller	
(ISA) 0x0000000A (10)	Intel(R) I211 Gigabit Network Connection #2	
(ISA) 0x0000000A (10)	Microsoft Basic Display Adapter	
(ISA) 0x0000000A (10)	PCI Express Root Port	
(ISA) 0x0000000A (10)	Standard SATA AHCI Controller	
(ISA) 0x0000000B (11)	Ethernet Controller	
(ISA) 0x0000000B (11)	Ethernet Controller	
(ISA) 0x0000000B (11)	Intel SD Host Controller	
(ISA) 0x0000000B (11)	Intel(R) I211 Gigabit Network Connection	
(ISA) 0x0000000C (12)	PS/2 Compatible Mouse	
(ISA) 0x00000036 (54)	Microsoft ACPI-Compliant System	
(ISA) 0x00000037 (55)	Microsoft ACPI-Compliant System	
(ISA) 0x00000038 (56)	Microsoft ACPI-Compliant System	
(ISA) 0x00000039 (57)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003A (58)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003B (59)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003C (60)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003D (61)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003E (62)	Microsoft ACPI-Compliant System	
(ISA) 0x0000003F (63)	Microsoft ACPI-Compliant System	
(ISA) 0x00000040 (64)	Microsoft ACPI-Compliant System	
(ISA) 0x00000041 (65)	Microsoft ACPI-Compliant System	
(ISA) 0x00000042 (66)	Microsoft ACPI-Compliant System	
(ISA) 0x00000043 (67)	Microsoft ACPI-Compliant System	
(ISA) 0x00000044 (68)	Microsoft ACPI-Compliant System	
(ISA) 0x00000045 (69)	Microsoft ACPI-Compliant System	
(ISA) 0x00000046 (70)	Microsoft ACPI-Compliant System	
(ISA) 0x00000047 (71)	Microsoft ACPI-Compliant System	

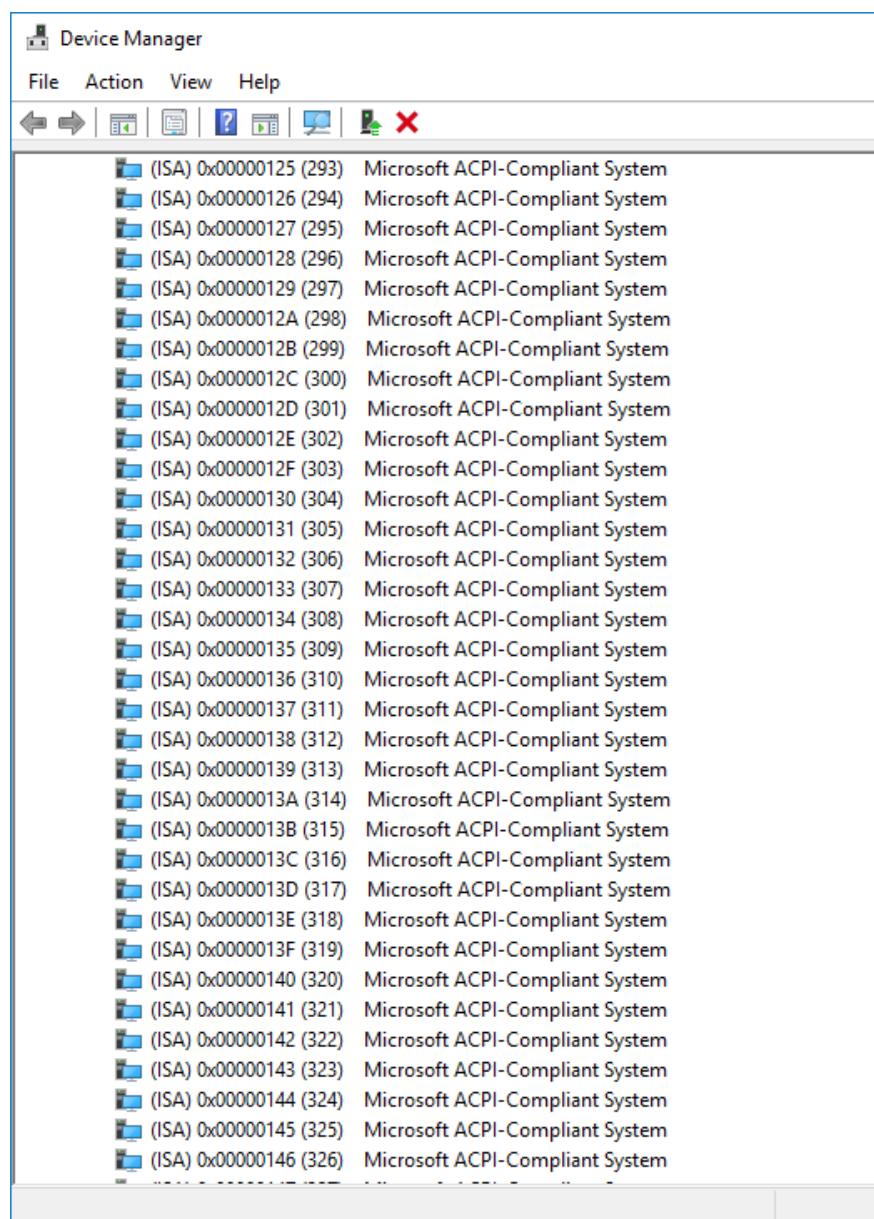


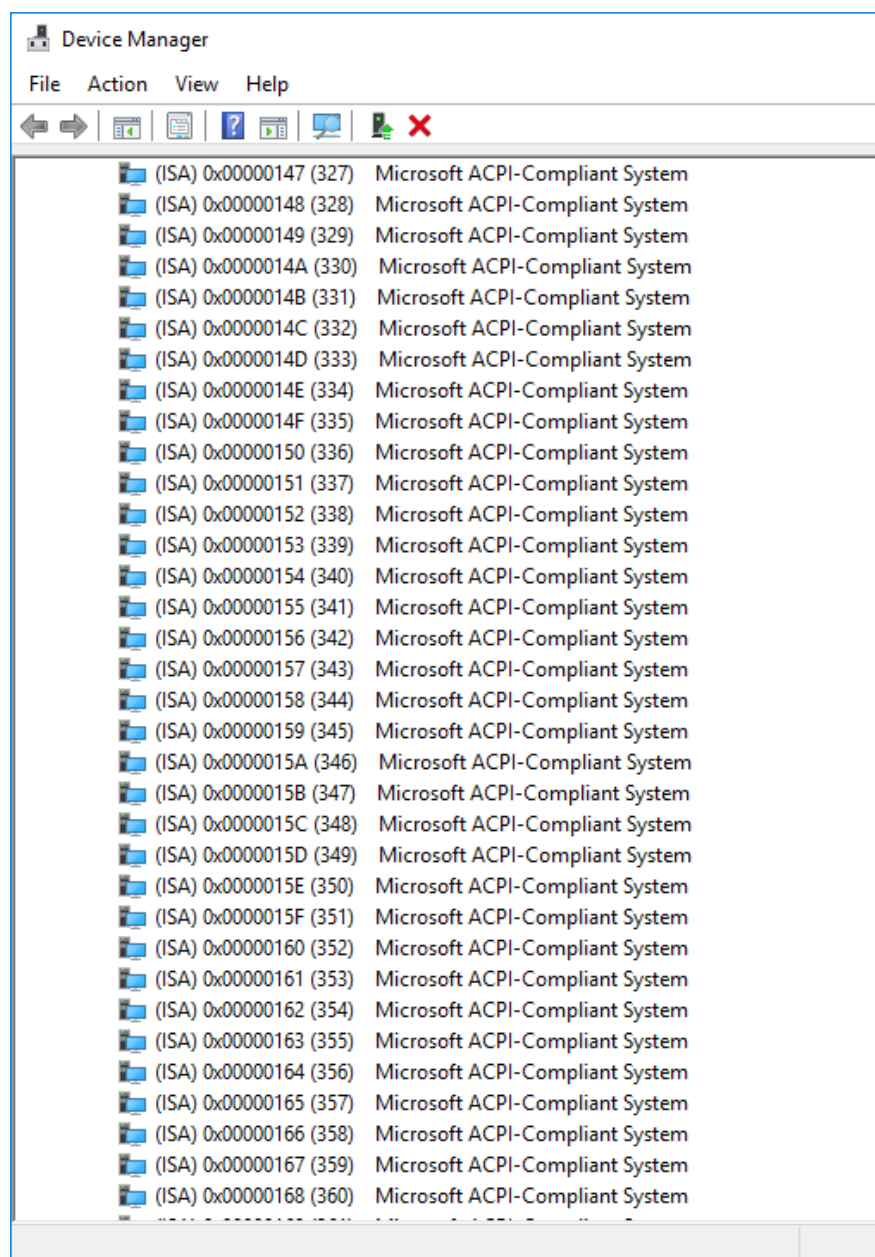


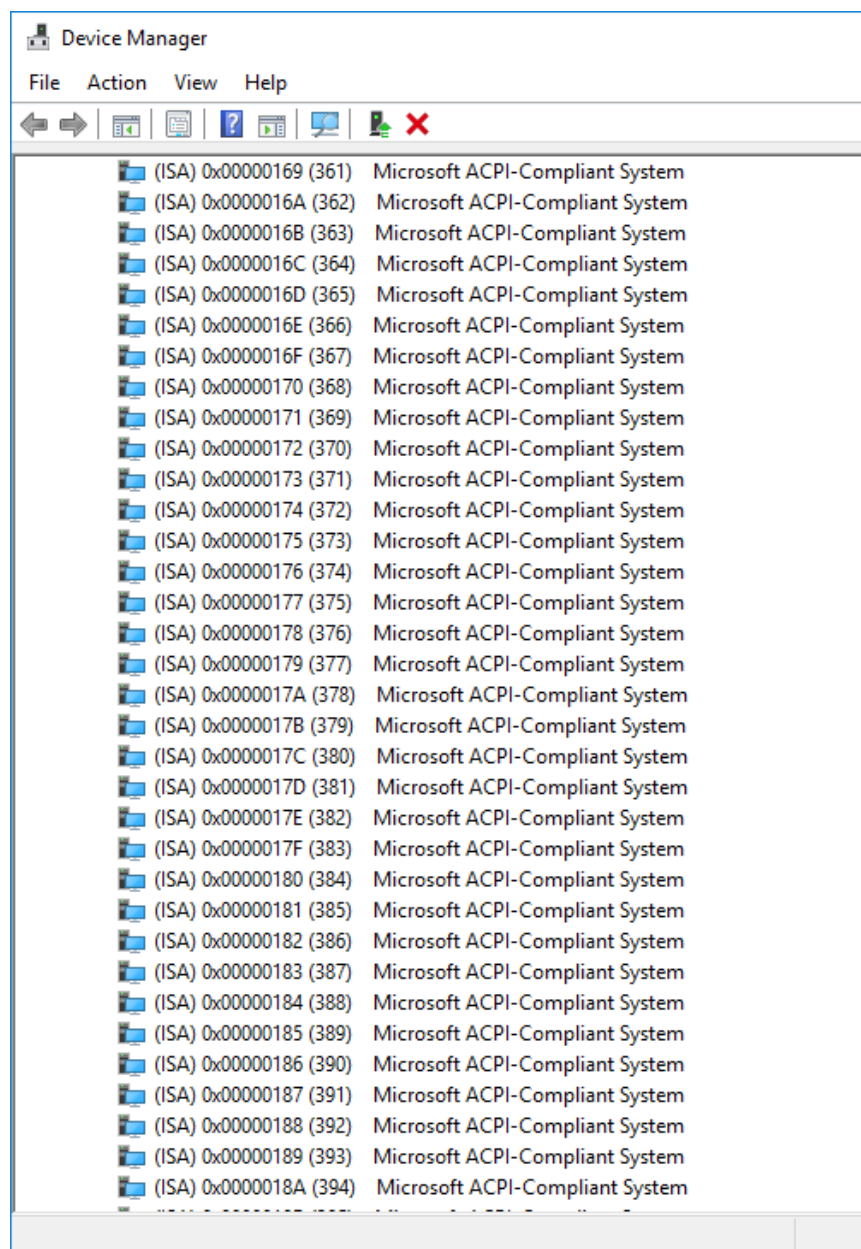


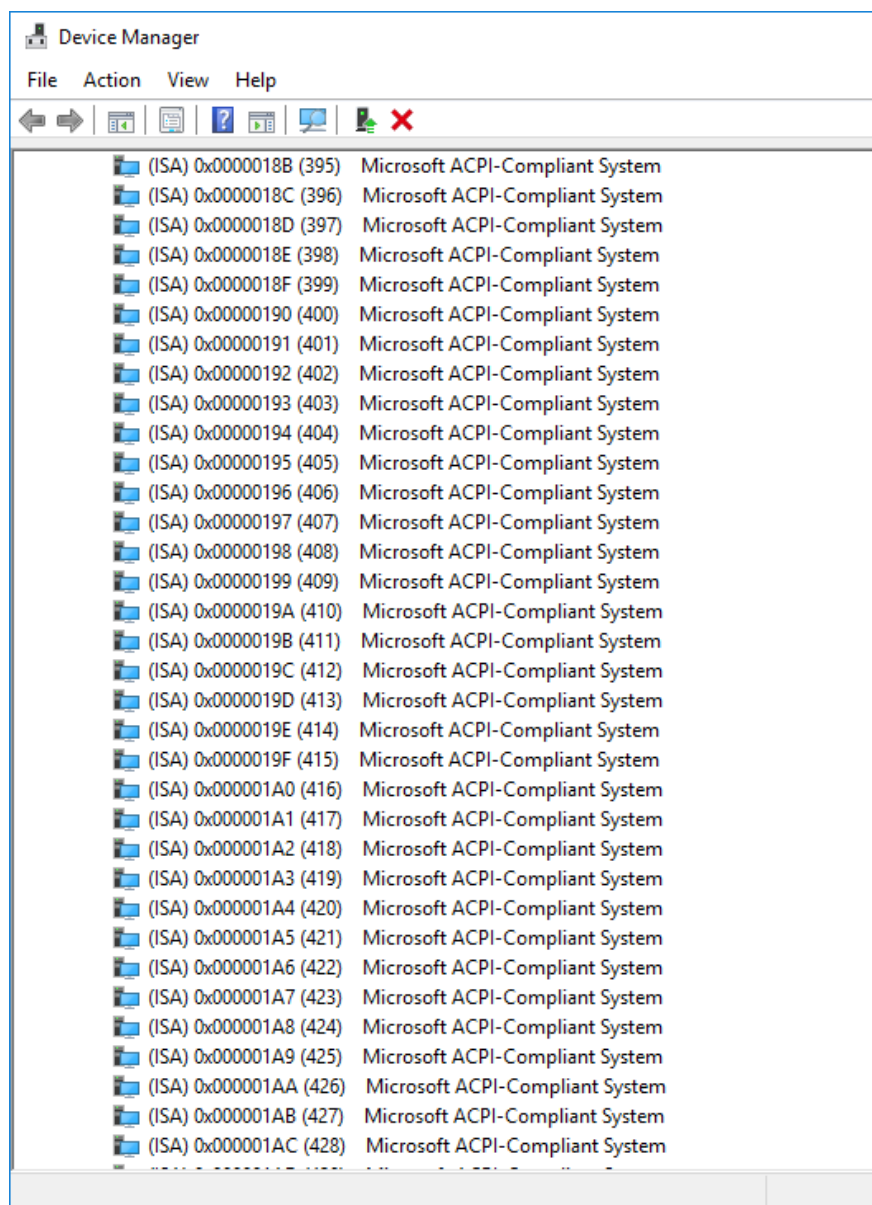


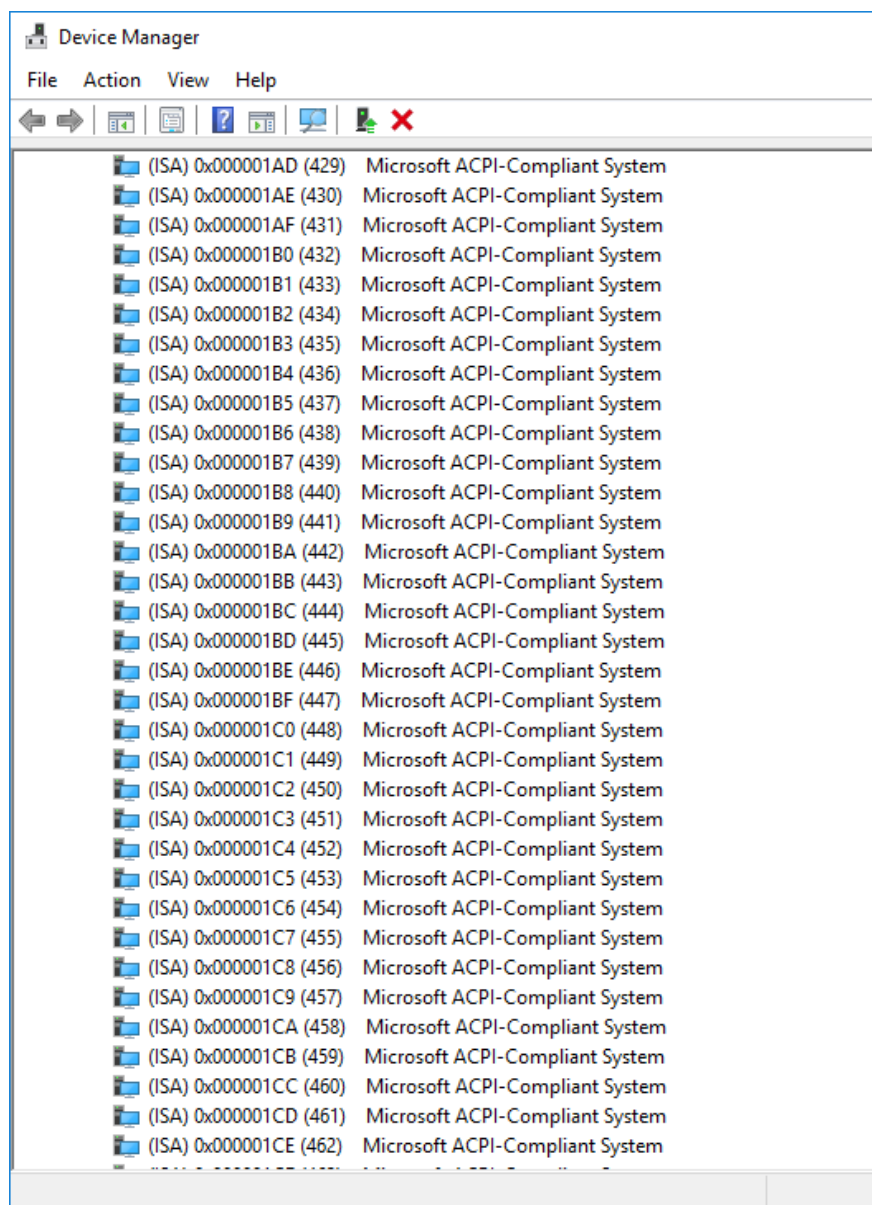


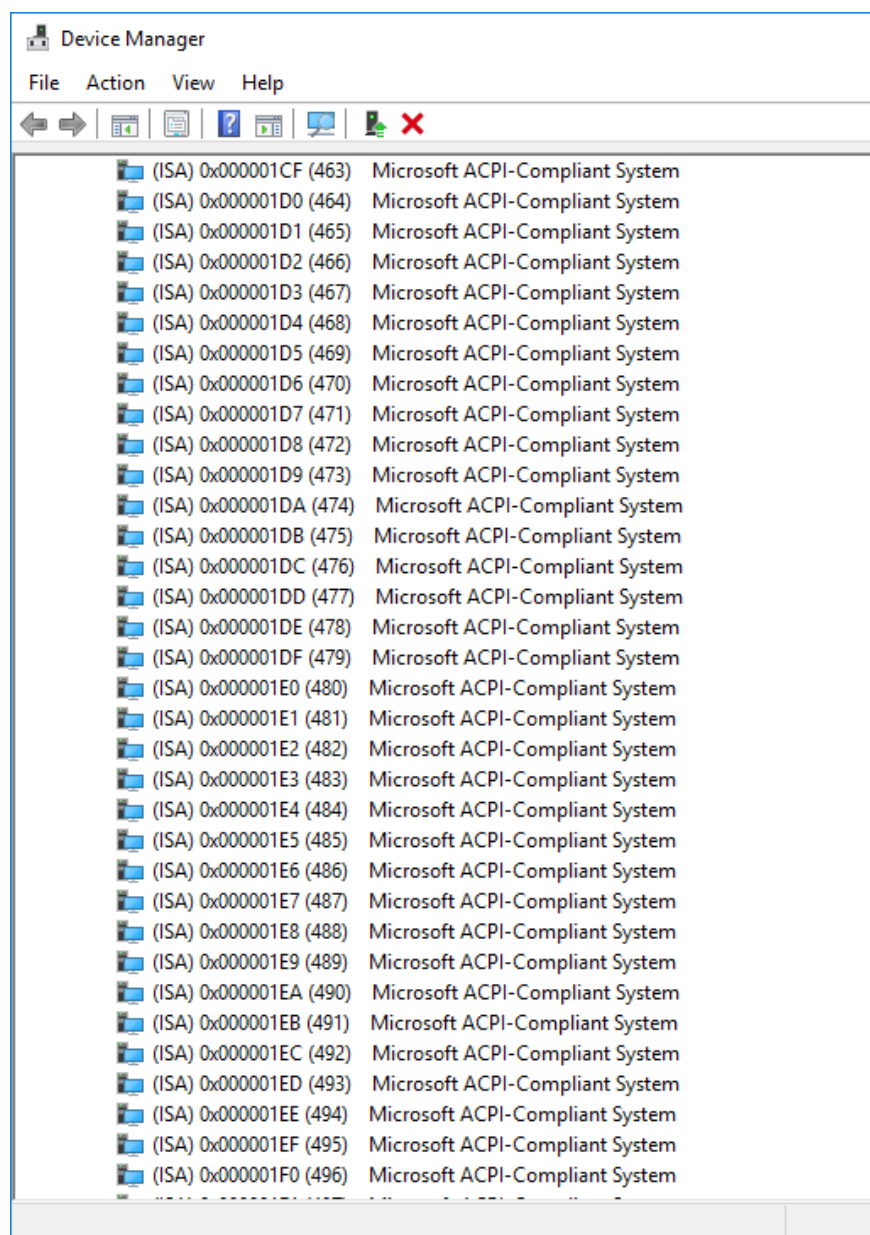


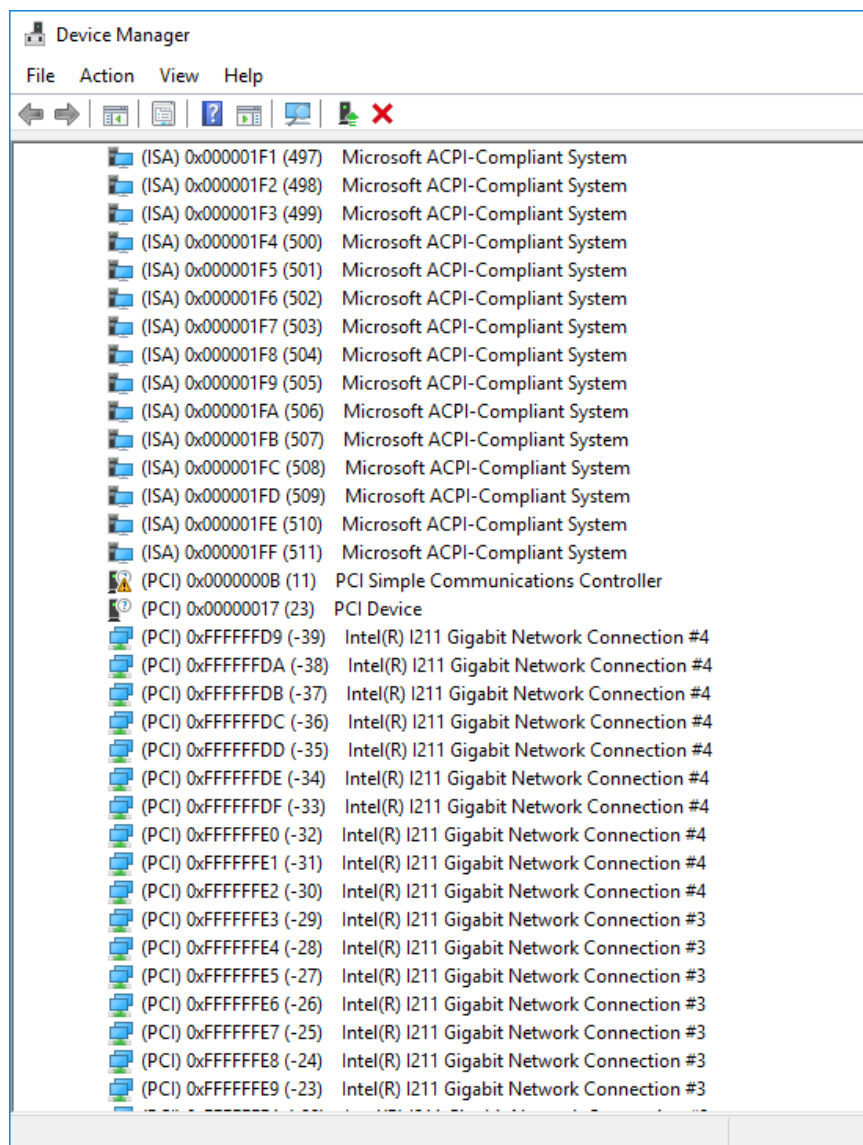


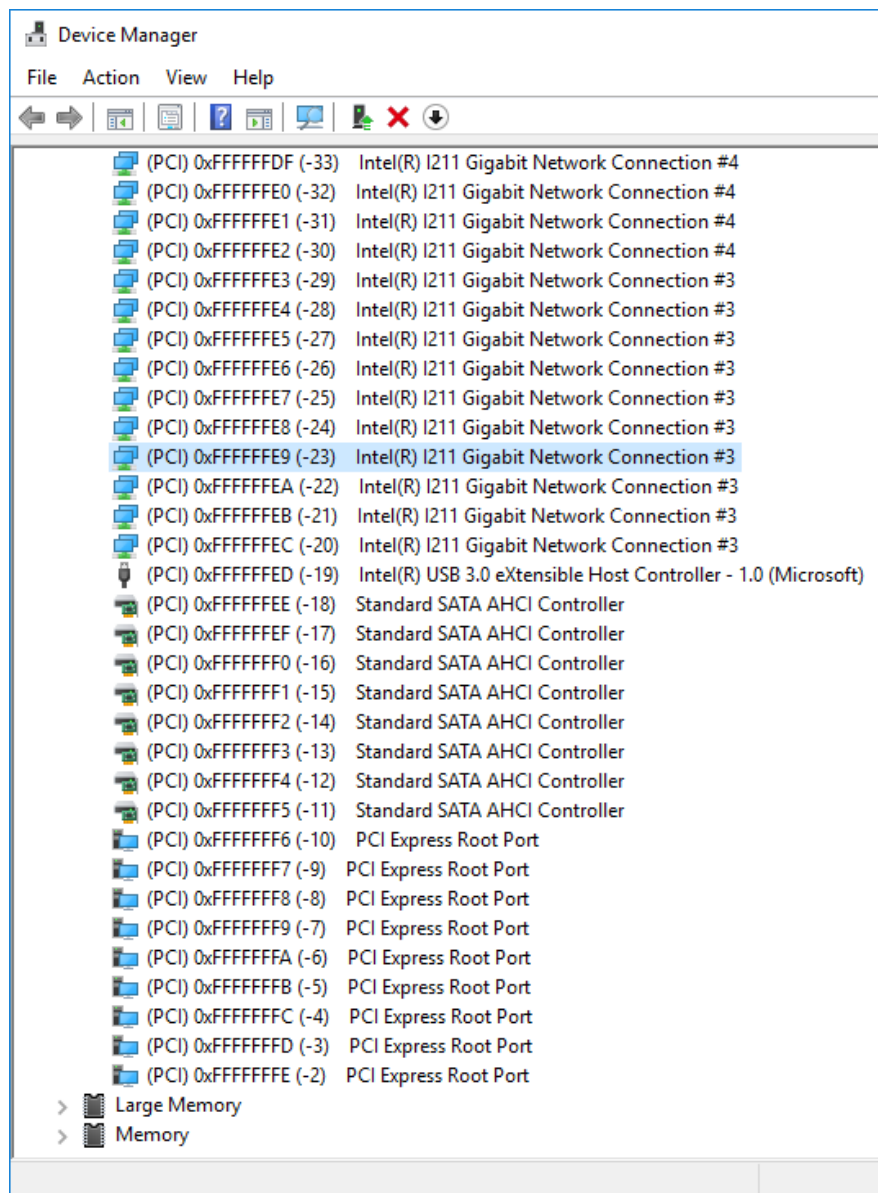












Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

C.1.1 Introduction

The FWS-7360 provides an LED indicator which can change the LED status by AAEON SDK. The user is able to program the LED status to express different status.

C.1.2 Status LED Configuration

Table 1 : Turth Table of Status LED			
STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table 2 : Status LED relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

C.1.3 Sample Code

```

*****
#define Byte CPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define Byte OFFSET //This parameter is represented from Note2
*****

bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
//LED Off
//BIT2=0, BIT1=0, BIT0=0
bData = bData & 0xF8;
break;
}
case 1:
{
//Red LED On
//BIT2=0, BIT1=0, BIT0=1
bData = (bData & 0xF8) | 0x01;
break;
}
case 2:
{
//Red LED Blink
//BIT2=0, BIT1=1, BIT0=0
bData = (bData & 0xF8) | 0x02;
break;
}
case 3:
{
//Red LED Fast Blink
//BIT2=0, BIT1=1, BIT0=1
bData = (bData & 0xF8) | 0x03;
break;
}
case 4:
{
//Green LED On

```

```
//BIT2=1, BIT1=1, BIT0=1
bData = (bData & 0xF8) | 0x07;
break;
}
case 5:
{
    //Green LED Blink
    //BIT2=1, BIT1=0, BIT0=1
    bData = (bData & 0xF8) | 0x05;
    break;
}
case 6:
{
    //Green LED Fast Blink
    //BIT2=1, BIT1=1, BIT0=0
    bData = (bData & 0xF8) | 0x06;
    break;
}
default:
    break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*****
```

C.2 LAN Bypass

C.2.1 Introduction

The FWS-7360 provides a LAN Bypass kit and allows uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

C.2.2 LAN Bypass Configuration

Table 1 : ID Select table of LAN kit

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table 2 : LAN Bypass relative register table

Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refert to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3 : LAN Bypass relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

C.2.3 Sample Code

```

*****
#define ByteCPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define ByteOFFSET              //This parameter is represented from Note2
*****

// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
    bData = bData | 0x08;
else
    bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
    bData = bData | 0x04;
else
    bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
    bData = bData | 0x02;
else
    bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
    bData = bData | 0x01;
else
    bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH) // Pass Through
    bData = bData & 0xBF;
else // Bypass
    bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH) // Pass Through
    bData = bData & 0xDF;
else // Bypass

```

```
bData = bData | 0x20;
```

```
// WDT Action (Reg01h bit4)
```

```
if(SET_WDT_RESET)      // Reset
```

```
    bData = bData & 0xEF;
```

```
else                    // Bypass
```

```
    bData = bData | 0x10;
```

```
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);
```

```
// Apply Settings (Reg01h bit7)
```

```
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
```

```
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
```

```
Sleep(500);
```

```
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
```

```
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
```

```
*****
```

C.3 Software Reset button (General Propose Input)

C.3.1 Introduction

The FWS-7360 provides a general propose input button which gets its status by the AAEON SDK.

C.3.2 LAN Bypass Configuration

Table 2 : LAN Bypass relative register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1 : Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

C.3.3 Sample Code

```

*****
#define Word      BTN_STS      //This parameter is represented from Note1
#define ByteBTN_STS_R      //This parameter is represented from Note2
*****

Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
    BYTE  TmpValue;

    TmpValue = inportb (IoAddr);
    return  (TmpValue & (1 << BitNum))
}
*****
VOID  Main(){
    Byte RstBtn;

    RstBtn = GET_Value (BTN_STS, BTN_STS_R); // Active Low
}
*****

```