EPIC-KBS9-PUC

BOX PC

User's Manual 1st Ed

Last Updated: April 2, 2019

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● EPIC-KBS9-PUC	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	4" EPIC Board
CPU	6th/7th Generation Intel® Core™ i7/i5/i3/Celeron® S-series (Supports 35~65W)
Chipset	H110/H170/Q170 (6W)
Memory Type	DDR4 (Non-ECC) SODIMM x 2, 2133MHz, up to 32G
Max. Memory Capacity	Up to 32G
BIOS	AMI
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V with lockable DC jack
Power Supply Type	ATX
Power Consumption (Typical)	--
Dimension (L x W x H)	216mm x 180mm x 65mm (unit size) 380mm x 350mm x 180mm (with packaging)
Operating Temperature	32°F ~ 122°F (0°C ~ 50°C)
Storage Temperature	-4°F ~ 176°F (-20°C ~ 80°C)
Operation Humidity	0 ~ 90% @ 40°C, non-condensing
MTBF (Hours)	--

System

- **Certification** — CE/FCC Class A
- **Anti-vibration** — 1 Grms/ 5~500 Hz/ operation—with mSATA

Display

- **VGA/LCD Controller** — 6th/7th Generation Intel® Core™ i3/i5/i7/Celeron®
- **Video Output** — HDMI (Rear), VGA (Internal Only)
- **Backlight Inverter Supply** — --

I/O

- **Ethernet** — Intel® i211 10/100/1000Base-TX x 2 or 4 ports
- **Audio** — --
- **USB Port** — USB3.0 x 2 (Real IO)
USB2.0 x 2 (Internal)
- **Serial Port** — COM x 2 (All Internal), RS-232/422/485
- **Parallel Port** — --
- **HDD Interface** — SATA 3.0 x 2
- **FDD Interface** — --
- **SSD** — Full size mSATA x1 (Default) or
2.5" HDD x1 (Optional)
- **Expansion Slot** — Mini-PCIe slot (Share with mSATA as above)
PCIe[x4] Slot x 1 (Q170 and H170 SKU)
- **DIO** — 8-bit

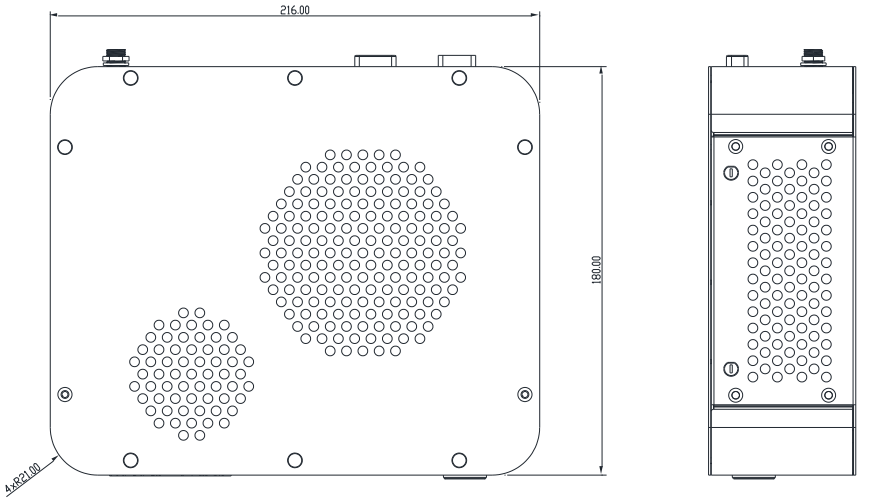
I/O	
● TPM	--
● Touch	--

Chapter 2

Hardware Information

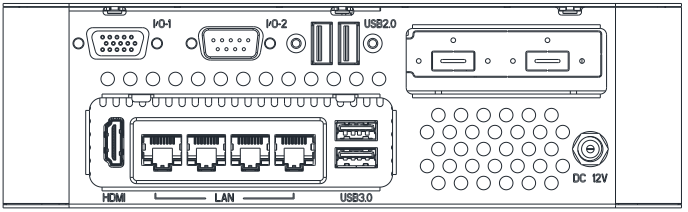
2.1 Dimensions

Top and Side

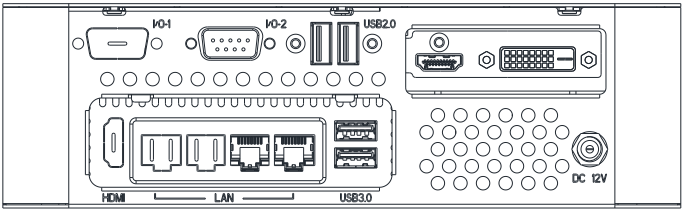


Front

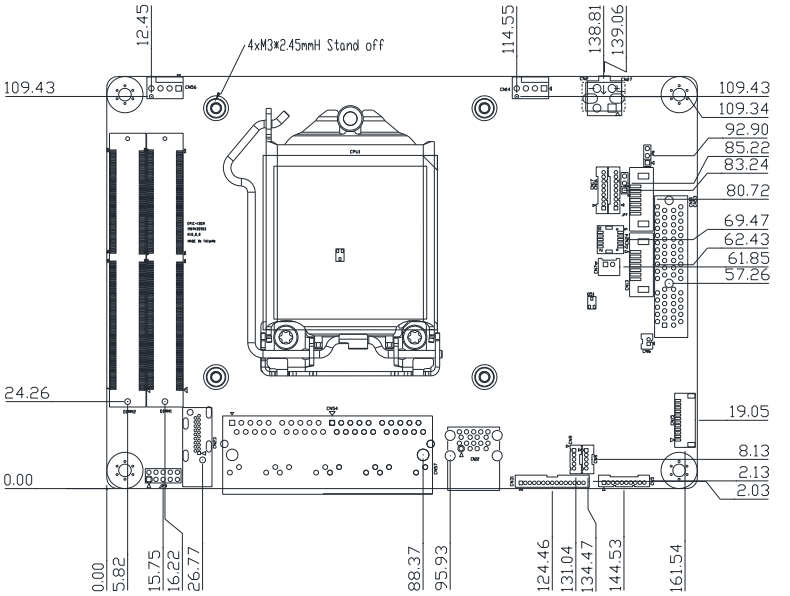
Rear EPIC-KBS9-PUC-A10-0002

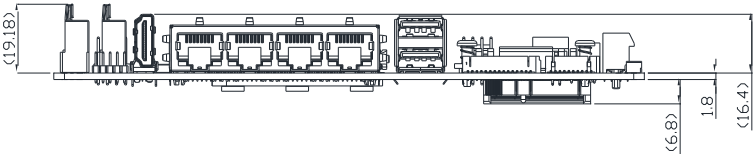


Rear EPIC-KBS9-PUC-A10-0001

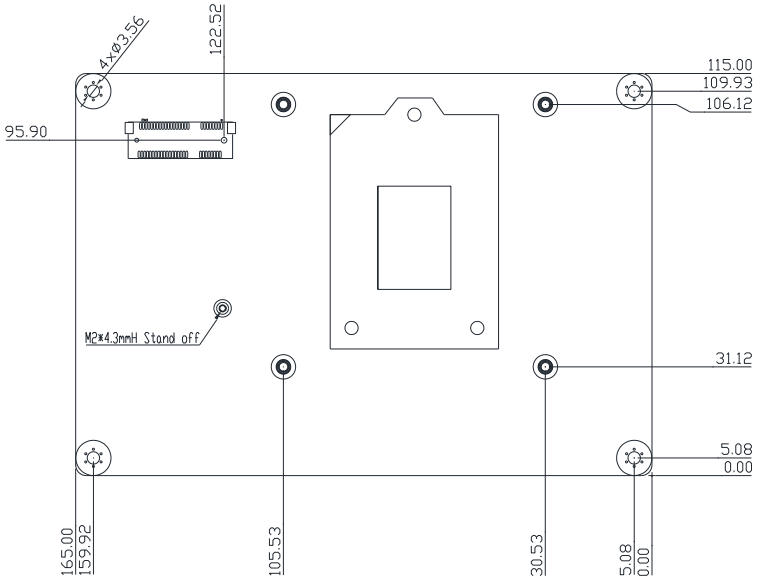


Board Component Side



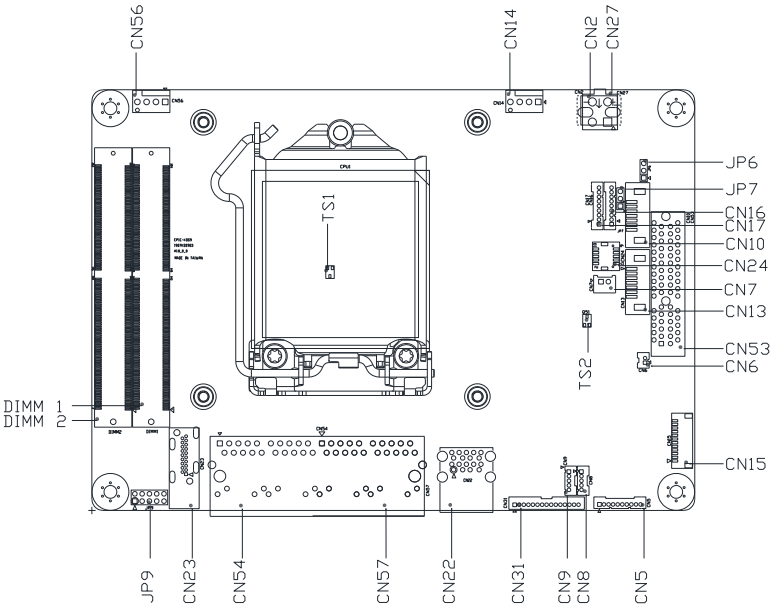


Board Solder Side

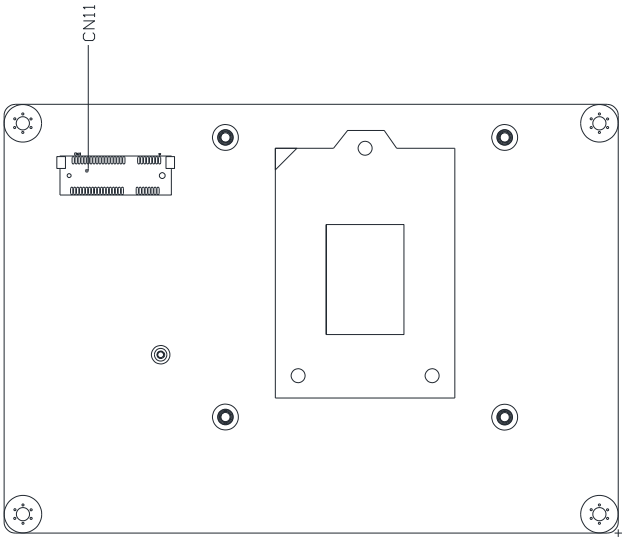


2.2 Jumpers and Connectors

Component Side



Solder Side

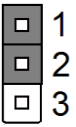


2.3 List of Jumpers

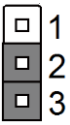
Please refer to the table below for all of the board's jumpers that you can configure for your application.

Label	Function
JP6	Clear CMOS Jumper
JP7	AT/ATX Mode Selection
JP9	Front Panel PIN Header

2.3.1 Clear CMOS Jumper (JP6)

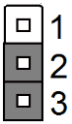


Normal (Default)

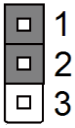


Clear CMOS

2.3.2 AT/ATX mode Selection (JP7)

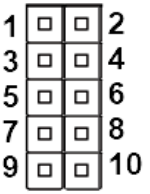


AT mode



ATX mode (Default)

2.3.3 Front Panel PIN Header (JP9)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	EXT_PWRBTN#	IN	
3	HDD_LED-	OUT	GND
4	HDD_LED+	OUT	+3.3V
5	SPKR-	OUT	GND
6	SPKR+	OUT	+5V
7	GND	GND	
8	PWR_LED+	OUT	+3.3V
9	GND	GND	
10	HWRST#	IN	

2.4 List of Connectors

The table below lists all of the board's connectors, configurable for your application.

Label	Function
CN2	External +12V Input [Default]
CN5	Audio Port
CN6	RTC Battery Connector
CN7	+5V Output for SATA HDD
CN8	USB 2.0 Port
CN9	USB 2.0 Port
CN10	SATA Port
CN11	Mini-Card / mSATA Connector
CN13	SATA Port
CN14	CPU FAN Connector
CN15	LPC Port
CN16	COM Port
CN17	COM Port
CN22	USB 2.0/3.0 Port 1~Port 2
CN23	HDMI
CN24	DIO
CN27	External +12V Input [Reserved]
CN31	CRT
CN53	PCIE x 4 Slot
CN54	LAN (RJ-45) Port 1~Port 4
CN56	System FAN Connector
CN57	LAN (RJ-45) Port 1~Port 2 [Reserved]
DIMM1	DDR4 SO-DIMM
DIMM2	DDR4 SO-DIMM

2.4.1 External +12V Input (CN2)

Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	

2.4.2 Audio Port (CN5)

Pin	Pin Name	Signal Type	Signal Level
1	MIC_L		
2	MIC_R		
3	GND		
4	LIN_L		
5	LIN_R		
6	GND	GND	
7	LOUT_L		
8	GND	GND	
9	LOUT_R		
10	+V5A_AUD	PWR	+5V

2.4.3 RTC Battery Connector (CN6)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	+3.3V
2	GND	GND	

2.4.4 +5V Output for SATA HDD (CN7)

Pin	Pin Name	Signal Type	Signal Level
1	+V5S	PWR	+5V
2	GND	GND	

2.4.5 USB 2.0 Port (CN8)

Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB	PWR	+5V
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.6 USB 2.0 Port (CN9)

Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB	PWR	+5V
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.7 SATA Port (CN10)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.8 Mini-Card/mSATA Connector (CN11)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB/+3.3V	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PRW	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V

Pin	Pin Name	Signal Type	Signal Level
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-/mSATARX+	DIFF	
24	+3.3VSB/+3.3V	PWR	+3.3V
25	PCIE_RX+/mSATARX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-/mSATATX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+/mSATATX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB/+3.3V	PWR	+3.3V
40	GND	GND	
41	+3.3VSB/+3.3V	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB/+3.3V	PWR	+3.3V

2.4.9 SATA Port (CN13)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.10 CPU FAN Connector (CN14)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+V12S/+V5S	PWR	+12V/+5V
3	TACH	IN	
4	PWM	OUT	

※ +12V/+5V can be set by BOM(R768-+12V/R766-+5V) [Default:+12V]

2.4.11 LPC Port (CN15)

Pin	Pin Name	Signal Type	Signal Level
1	LAD0	IN/OUT	+3.3V
2	LAD1	IN/OUT	+3.3V
3	LAD2	IN/OUT	+3.3V
4	LAD3	IN/OUT	+3.3V
5	+V3.3S	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA/ I2C_SDA	IN/OUT	
11	SMB_CLK/ I2C_CLK	OUT	
12	SMB_ALERT/ INT_SERIRQ	IN	+3.3V

2.4.12 COM Port (CN16)

Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

※ COM RS-232/422/485 can be set by BIOS setting. Default is RS-232.

※ COM RI/+5V/+12V function can be set by BOM(R1971-RI/R1972-+12V/R1973-+5V)

2.4.13 COM Port (CN17)

Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

※ COM RS-232/422/485 can be set by BIOS setting. Default is RS-232.

※ COM RI/+5V/+12V function can be set by BOM(R1968-RI/R1970-+12V/R1969-+5V)

2.4.14 USB 2.0/3.0 Port 1~Port 2 (CN22)

Pin	Pin Name	Signal Type	Signal Level
1	+V5SB	PWR	+5V
2	USB3_D-	DIFF	
3	USB3_D+	DIFF	
4	GND	GND	
5	USB3_SSRX–	DIFF	
6	USB3_SSRX+	DIFF	
7	GND	GND	
8	USB3_SSTX–	DIFF	
9	USB3_SSTX+	DIFF	
10	+V5SB	PWR	+5V
11	USB4_D-	DIFF	
12	USB4_D+	DIFF	
13	GND	GND	
14	USB4_SSRX–	DIFF	
15	USB4_SSRX+	DIFF	
16	GND	GND	
17	USB4_SSTX–	DIFF	
18	USB4_SSTX+	DIFF	

2.4.15 HDMI (CN23)

Pin	Pin Name	Signal Type	Signal Level
1	HDMI_TX2+	DIFF	
2	GND	GND	
3	HDMI_TX2-	DIFF	
4	HDMI_TX1+	DIFF	
5	GND	GND	
6	HDMI_TX1-	DIFF	
7	HDMI_TX0+	DIFF	
8	GND	GND	
9	HDMI_TX0-	DIFF	
10	HDMI_CLK+	DIFF	
11	GND	GND	
12	HDMI_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	PWR	+5V
19	HDMI_HPD		

2.4.16 DIO (CN24)

Pin	Pin Name	Signal Type	Signal Level
1	DIO0		
2	DIO1		
3	DIO2		
4	DIO3		
5	DIO4		
6	DIO5		
7	DIO6		
8	DIO7		
9	+V5S	PWR	+5V
10	GND	GND	

2.4.17 External +12V Input [Reserved] (CN27)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	GND	GND	
3	+12V	PWR	+12V
4	+12V	PWR	+12V

2.4.18 CRT (CN31)

Pin	Pin Name	Signal Type	Signal Level
1	RED		
2	GREEN		
3	BLUE		
4	NC		
5	GND	GND	
6	GND	GND	
7	GND	GND	
8	GND	GND	
9	+V5S_DISP_CON	PWR	+5V
10	GND	GND	
11	NC		
12	DATA		
13	HSY		
14	VSY		
15	CLK		

2.4.19 PCIE [x4] Slot (CN53)

Standard specification

2.4.20 LAN (RJ-45) Port1~4 (CN54)

Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.21 System FAN Connector (CN56)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+V12S/+V5S	PWR	+12V/+5V
3	TACH	IN	
4	PWM	OUT	

※ +12V/+5V can be set by BOM (R2146-+12V/R2145-+5V) [Default:+12V]

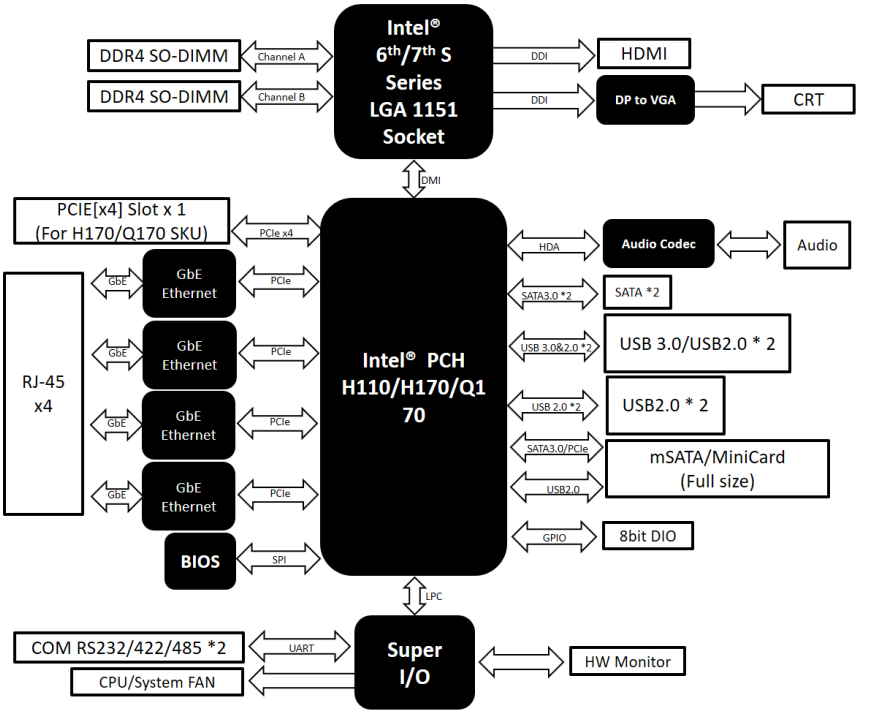
2.4.22 LAN (RJ-45) Port1~2 [Reserved] (CN57)

Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.23 DDR4 SO-DIMM Slot (DIMM1 & DIMM2)

Standard specification

2.5 Block Diagram



Chapter 3

BIOS Setup

3.1 System Test and Initialization

The EPIC-KBS9-PUC board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System Configuration Verification routines check the current system configuration stored on the CMOS memory and BIOS NVRAM. If the system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup System Configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The EPIC-KBS9-PUC CMOS memory has an integral lithium battery backup for data retention. You will need to replace the complete unit when it runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in a battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

To enter setup, power on the computer and press <Del>or <ESC> immediately. The following are short descriptions of each submenu:

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot options for legacy network devices

Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

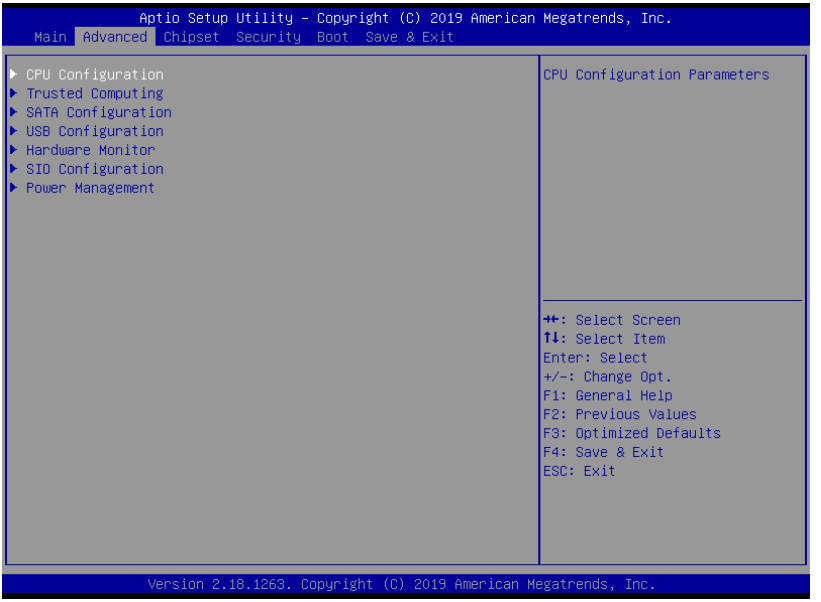
Boot – Enable/ Disable quiet Boot Option

Save & Exit –Save your changes and exit the program

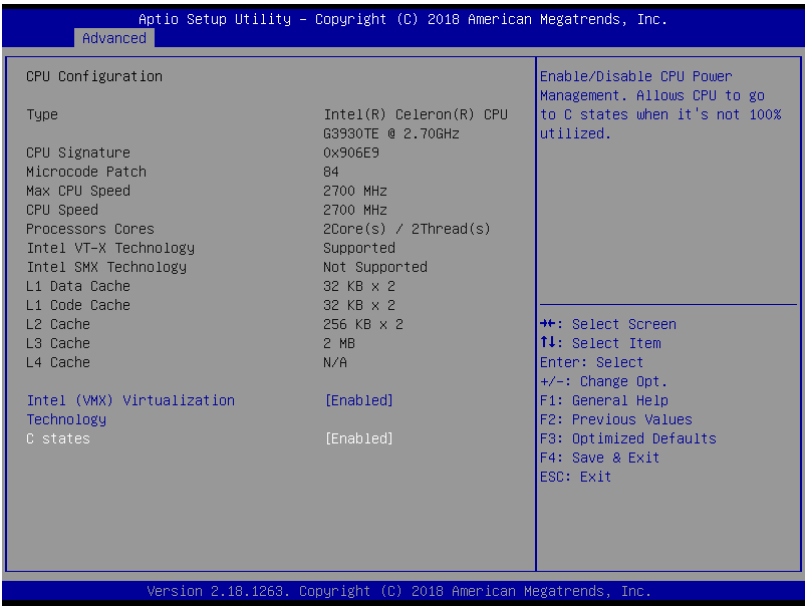
3.3 Setup Submenu: Main

Date and Time can be set here. Press <Tab> to switch between elements.

3.4 Setup Submenu: Advanced

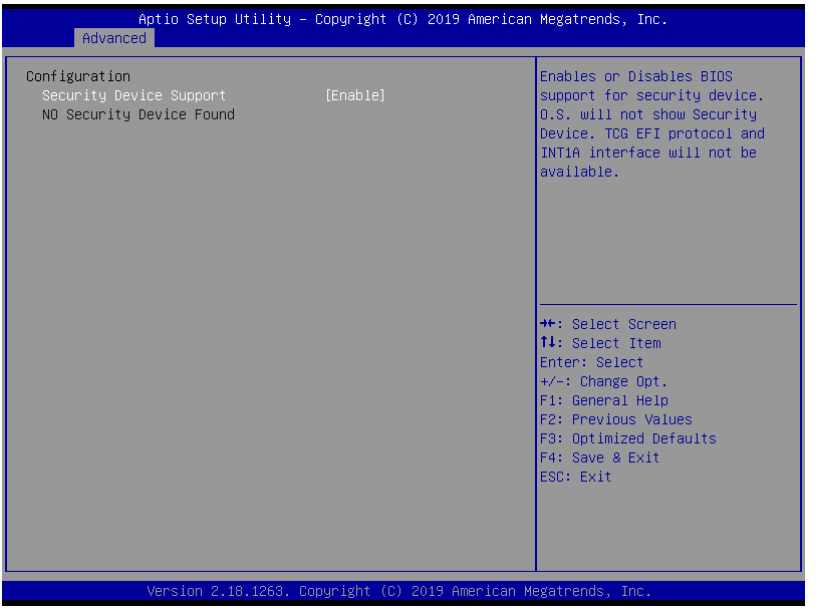


3.4.1 CPU Configuration



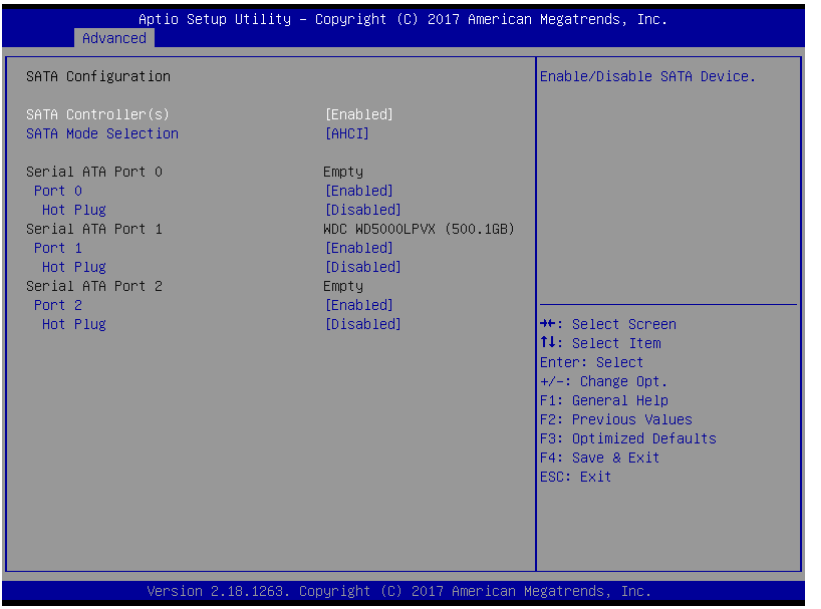
Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
C states	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disable for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.		

3.4.2 Trusted Computing



Options Summary		
Security Device Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable Security Device. **NOTE:** Your Computer will reboot during restart in order to change State of the Device.		

3.4.3 SATA Configuration

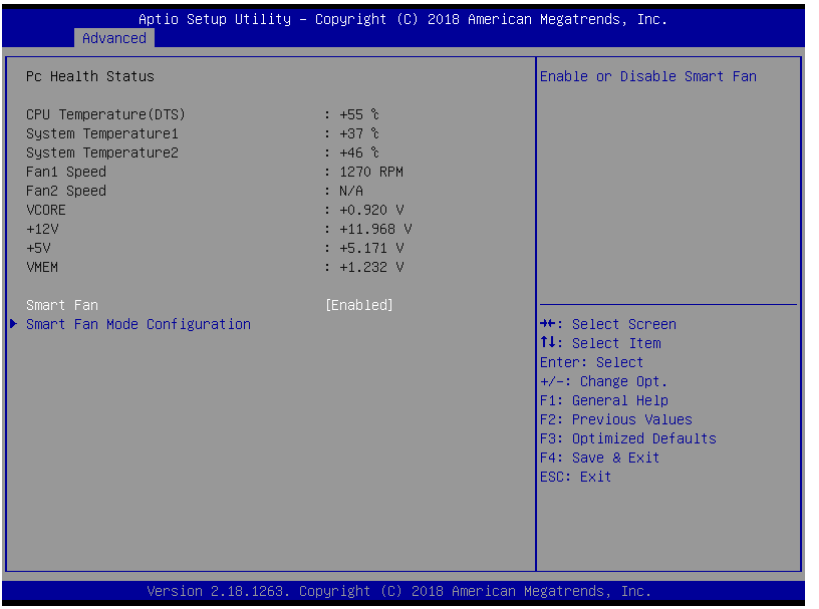


Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable SATA Device.		
SATA Mode	AHCI Mode	Optimal Default, Failsafe Default
	RAID Mode	
Determines how SATA controller(s) operate.		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

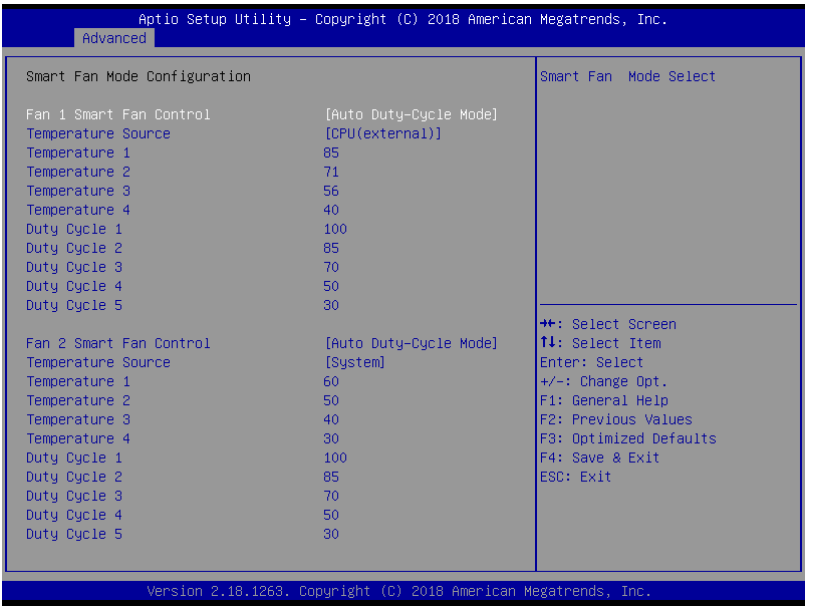
3.4.4 USB Configuration

Options Summary		
Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		
USB Port 0/1 function routing	FCH USB port 8/9	Optimal Default, Failsafe Default
	FCH USB port 0/1	

3.4.5 Hardware Monitor

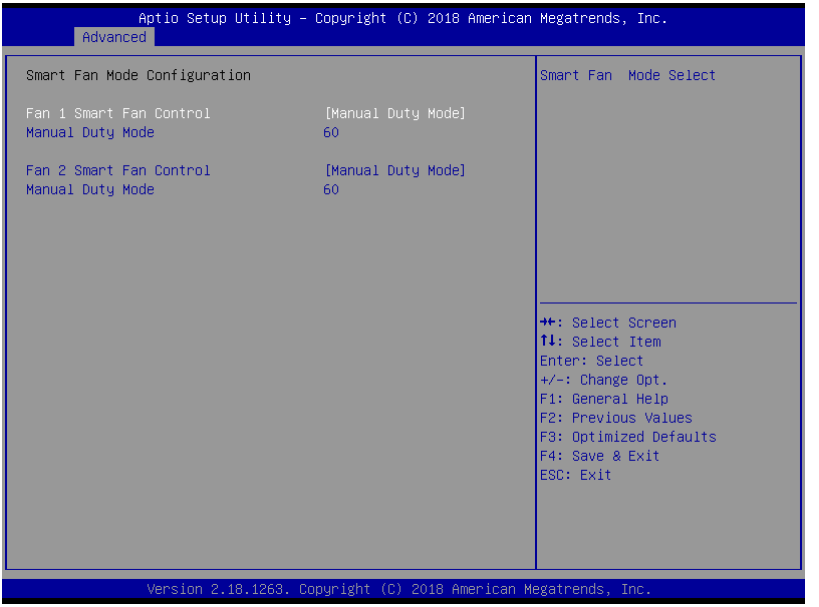


3.4.5.1 Smart Fan Mode Configuration



Smart Fan Mode Configuration Menu – Auto Duty Cycle Mode Selected

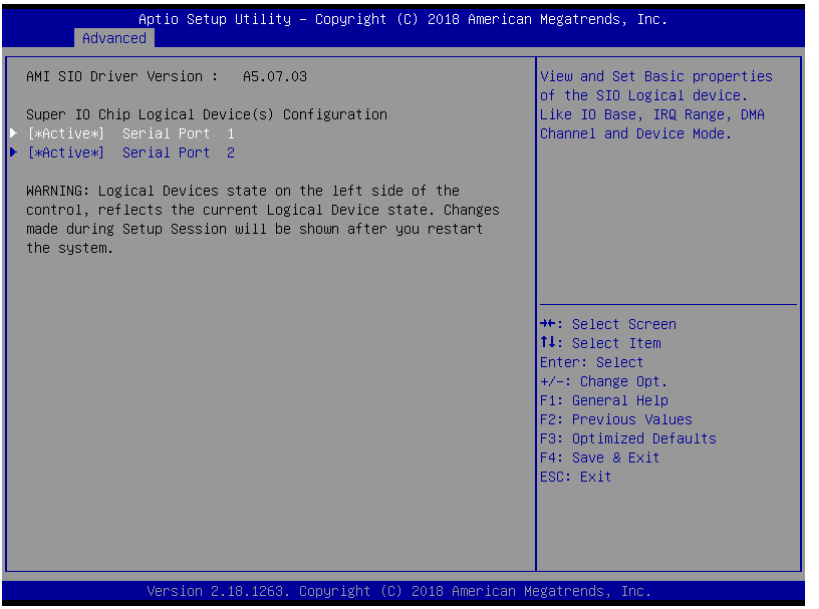
Options Summary		
Fan1 Smart Fan control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Fan2 Smart Fan control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default



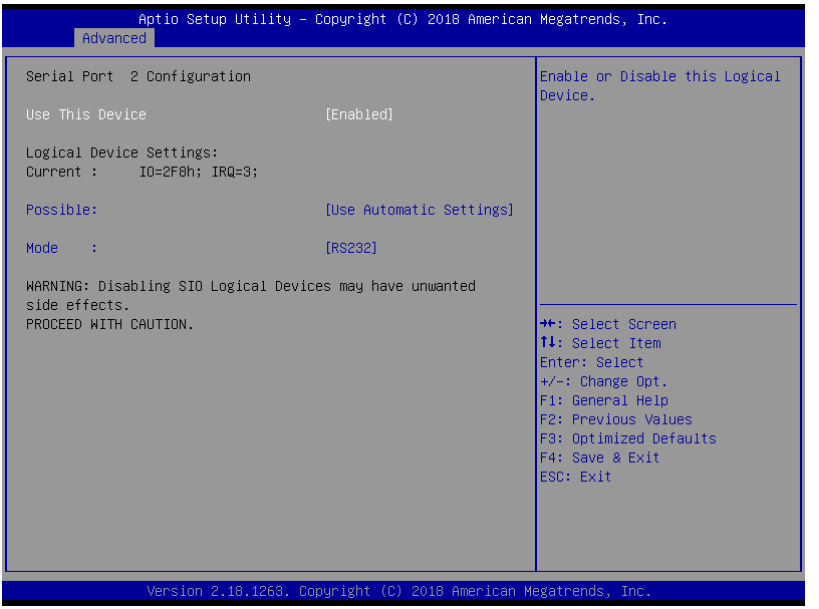
Smart Fan Mode Configuration Menu – Manual Duty Mode Selected

Options Summary		
Manual Setting	60	Optimal Default, Failsafe Default
Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number:		

3.4.6 SIO Configuration

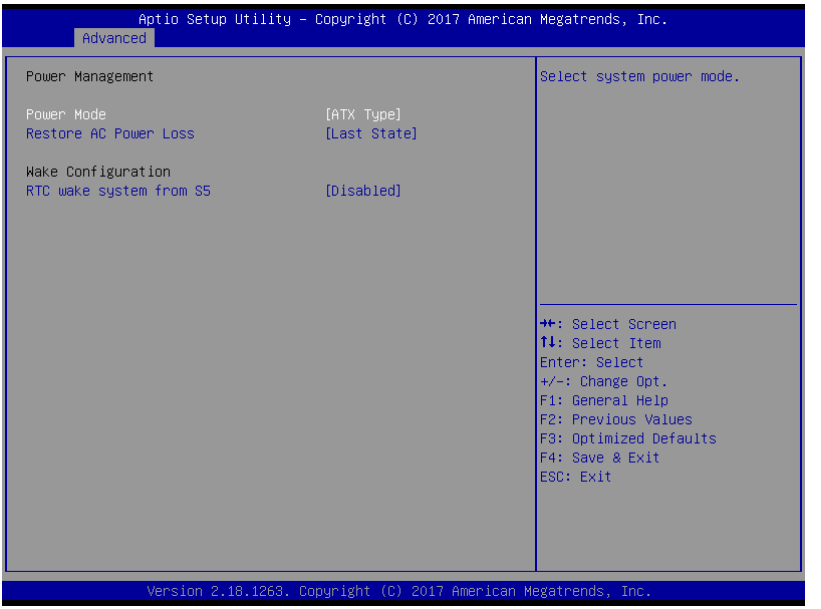


3.4.6.1 Serial Port Configuration



Options Summary		
Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232/422/485 selection		

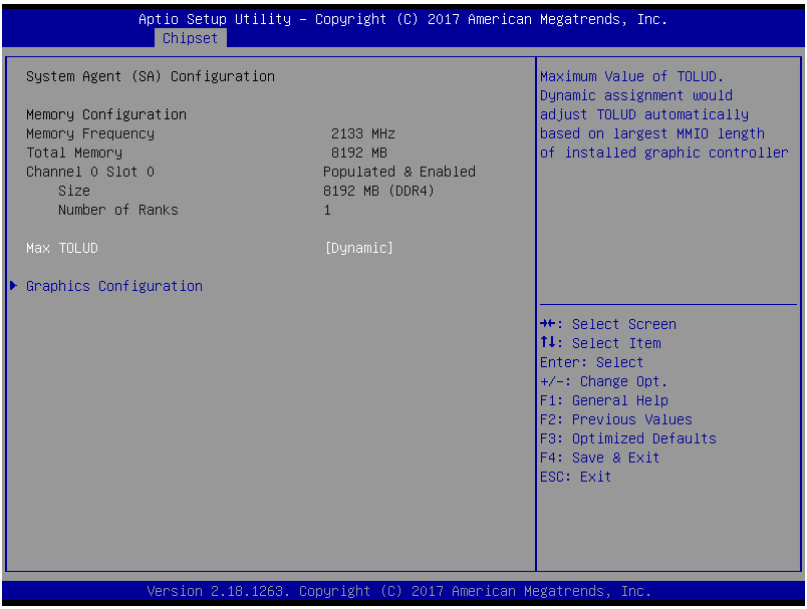
3.4.7 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power LOSS	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

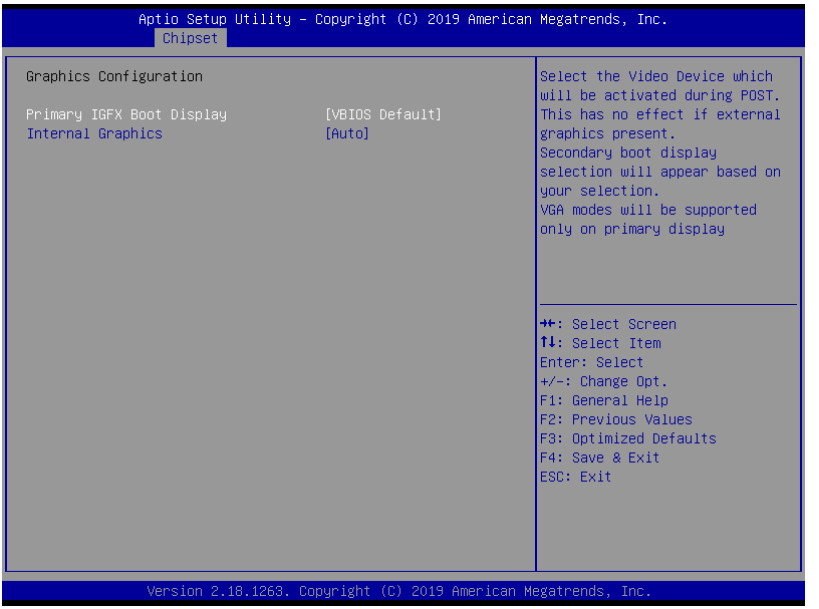
3.5 Setup Submenu: Chipset

3.5.1 System Agent (SA) Configuration



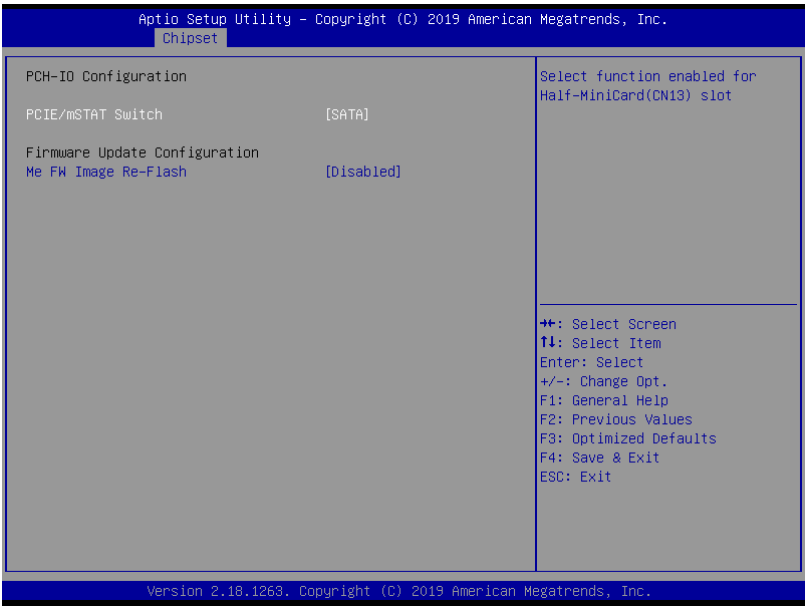
Options Summary		
Max TOLUD	Dynamic	Optimal Default, Failsafe Default
	1 GB	
	1.25 GB	
	1.5 GB	
	1.75 GB	
	2 GB	
	2.25 GB	
	2.5 GB	
	2.75 GB	
	3 GB	
	3.25 GB	
Maximum Value of TOLUD Dynamic assignment will adjust TOLUD automatically based on largest MMIO length of installed graphic controller.		

3.5.1.1 Graphics Configuration



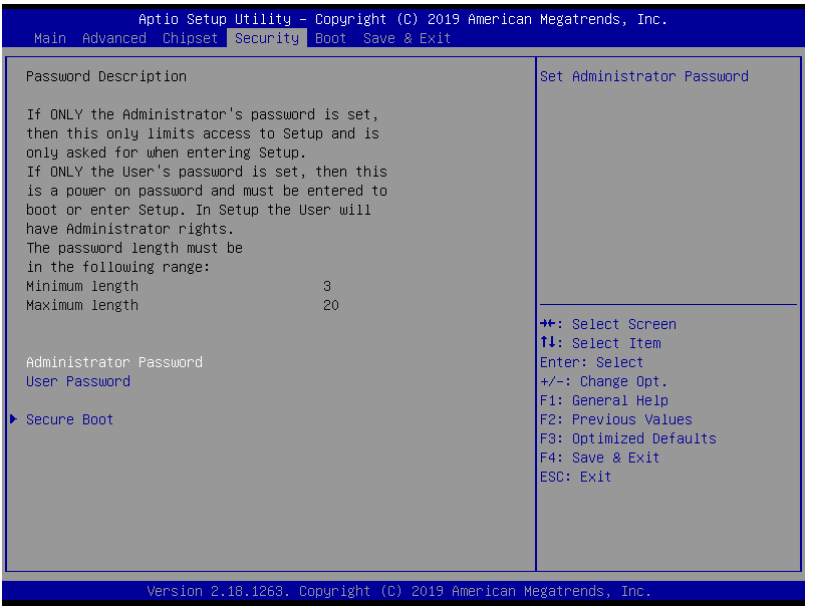
Options Summary		
Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	CRT	
	HDMI	
Select the Video Device which will be activated during POST. This has no effect if external graphic present. Secondary boot display selection will appear based on your selection.		
Internal Graphics	AUTO	Optimal Default, Failsafe Default
	Disabled	
	Enabled	
Keep IGFX enabled based on the setup options.		

3.5.2 PCH-IO Configuration



Options Summary		
PCIE/mSATA Switch	PCIE	Optimal Default, Failsafe Default
	SATA	
Select function enabled for Half-MiniCard(CN13) slot		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Auto	
Enable/Disable Me FW Image Re-Flash function.		

3.6 Setup Submenu: Security



Set User/Supervisor Password

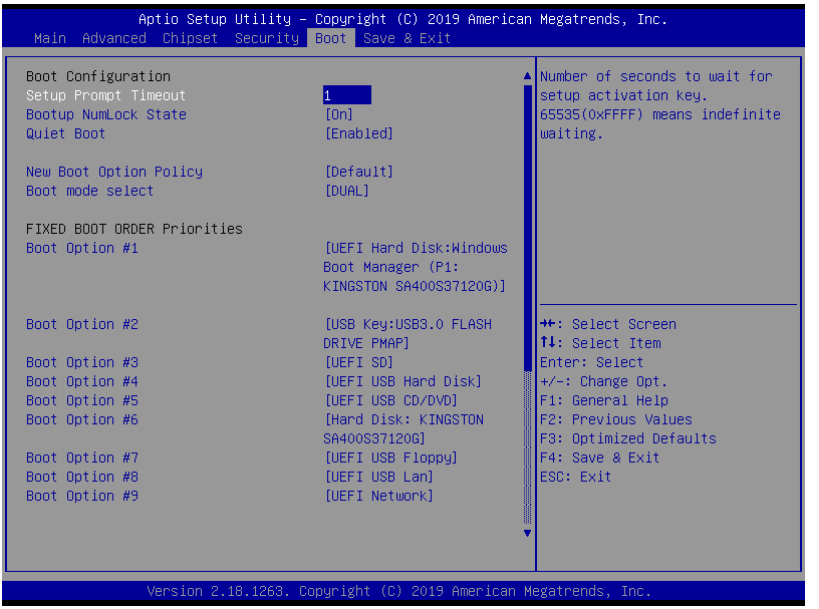
You can set an Administrator Password in this menu. If an Administrator Password is set, you will be able to then set a User Password. User Password limits access to many of the features in the Setup utility.

To set a password, select the password you want to set and then press <Enter>. A dialog box will appear in which you can set a password that is between 3 and 20 letters or numbers long. Press <Enter> when you are finished and type the password again into the dialog box to confirm. The password will be required when booting or when entering the Setup utility.

Removing the Password

Highlight this item and press <Enter>. In the dialog box that appears, type the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup Submenu: Boot

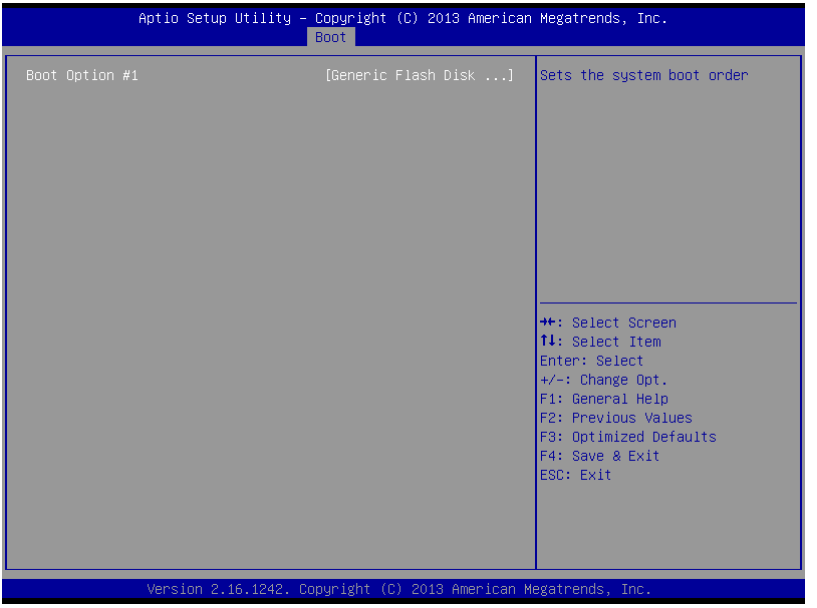


Options Summary		
Setup Prompt Timeout	1	Optimal Default, Failsafe Default
Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.		
Bootup NumLock State	On	Optimal Default, Failsafe Default
	Off	
Select the keyboard NumLock state		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable showing boot logo.		
New Boot Option Policy	Default	Optimal Default, Failsafe Default
	Place First	
	Place Last	
Controls the placement of newly detected UEFI boot options		

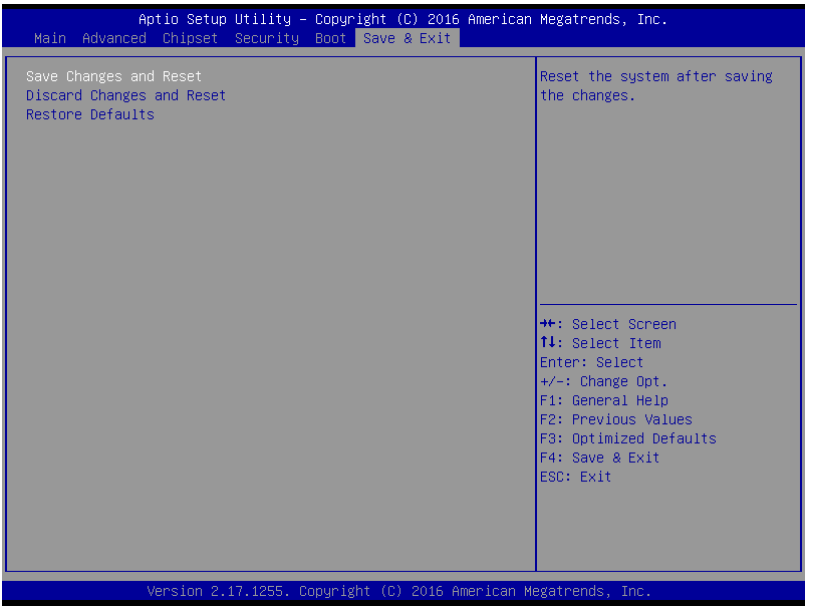
Table continues on next page.

Options Summary		
Boot mode select	LEGACY	Optimal Default, Failsafe Default
	UEFI	
	DUAL	
Select boot mode LEGACY/UEFI		

3.7.1 BBS Priorities



3.8 Setup Submenu: Save & Exit



Chapter 4

Driver Installation

4.1 Driver Installation

Drivers for the EPIC-KBS9-PUC can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/epic-boards-epic-kbs9-puc

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 – Chipset** folder and select your SKU and OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step 2 - Graphic** folder and select your SKU and OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Open the **Step 3 – LAN** folder and select your SKU and OS
2. Open the .**exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Serial Port Drivers

1. Open the **Step 4 – Serial Port Driver (Optional)** folder and select your SKU and OS
2. Open the **FintekSerial.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Mating Connectors

A.1 List of Mating Connectors and Cables

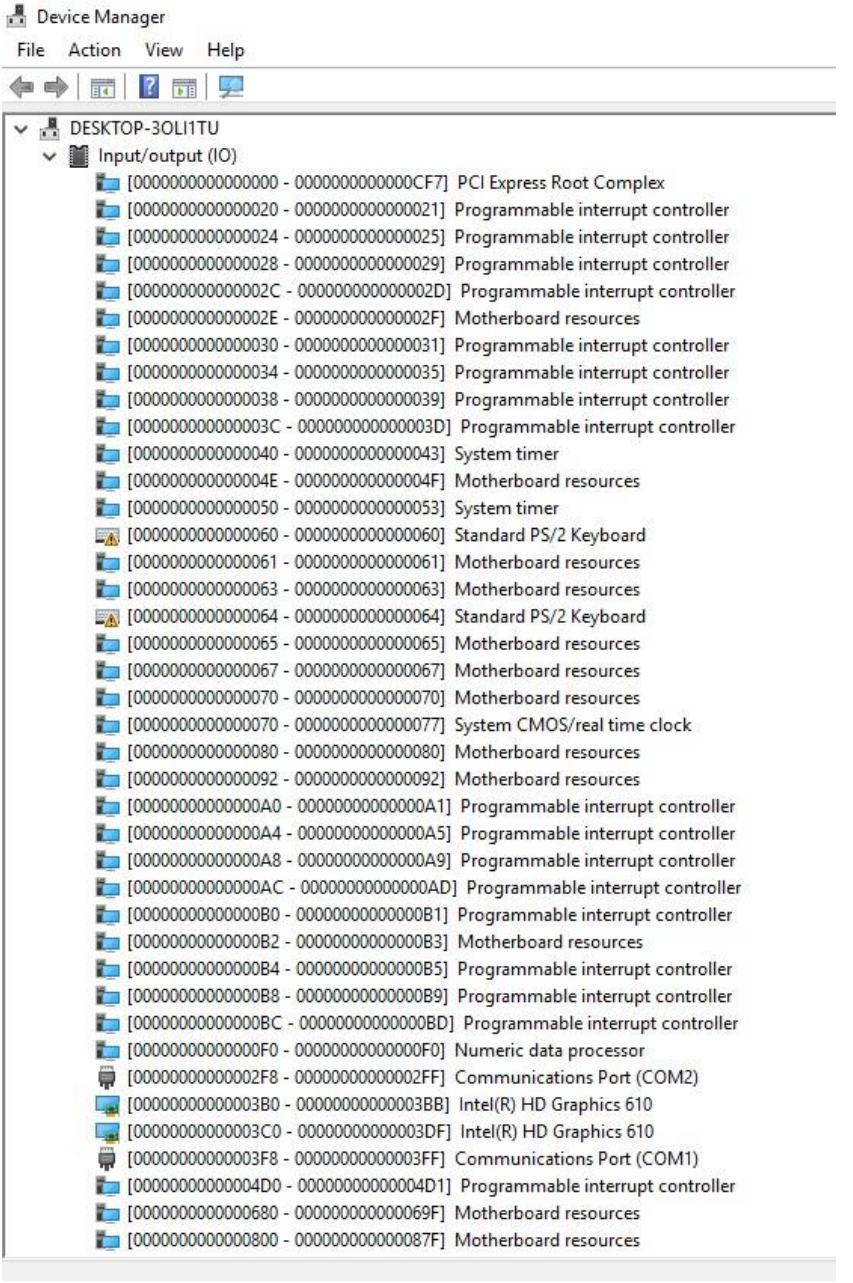
The table notes mating connectors and available cables.

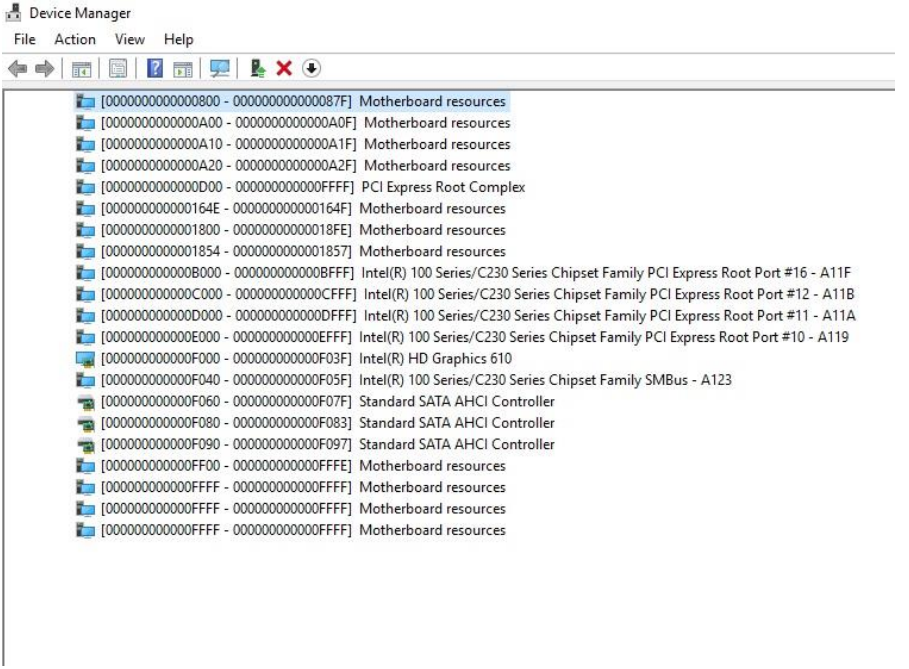
Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model No.		
CN2	External +12V Input	Molex	19211-0003	Power cable	170204010R
CN5	Audio Port	Molex	51021-1000	Audio Cable	1709100254
CN6	Battery Connector	Molex	51021-0200	Battery Cable	175011301K
CN7	+5V Output for SATA HDD	JST	PHR-2	SATA Power Cable	1702150155
CN8	USB 2.0 Port	Molex	51021-0500	USB Cable	1700050207
CN9	USB 2.0 Port	Molex	51021-0500	USB Cable	1700050207
CN10	SATA Port	Molex	887505318	SATA Cable	1709070500
CN13	SATA Port	Molex	887505318	SATA Cable	1709070500
CN14	CPU FAN Connector	Molex	47054-1000	FAN	17592KBS90
CN15	LPC Connector	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN16	COM Port	Molex	51021-0900	COM Cable	1701090150
CN17	COM Port	Molex	51021-0900	COM Cable	1701090150
CN24	DIO	JCTC	11002H00-2x5P	N/A	N/A
CN27	External +12V Input [Reserved]	Molex	3901-2040	N/A	N/A
CN31	CRT	JWT	A1251H02-15	VGA Cable	1704150153
CN56	System FAN Connector	Molex	47054-1000	FAN	17592KBS90

Appendix B

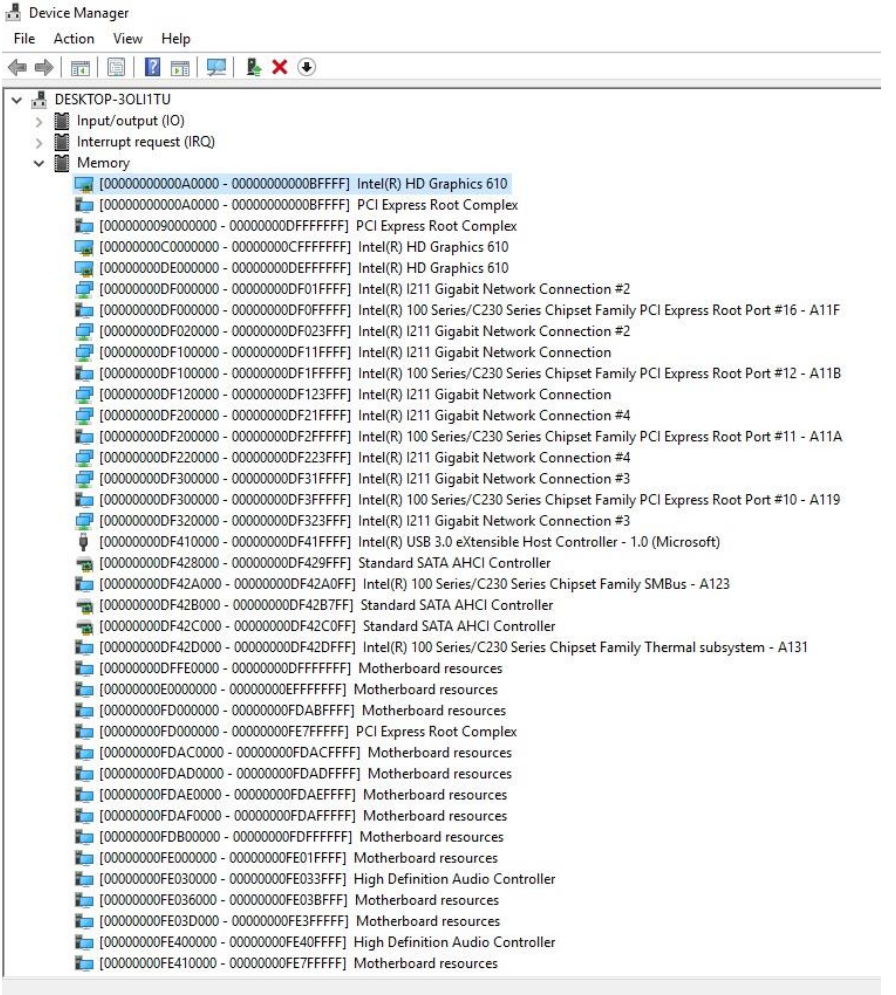
I/O Information

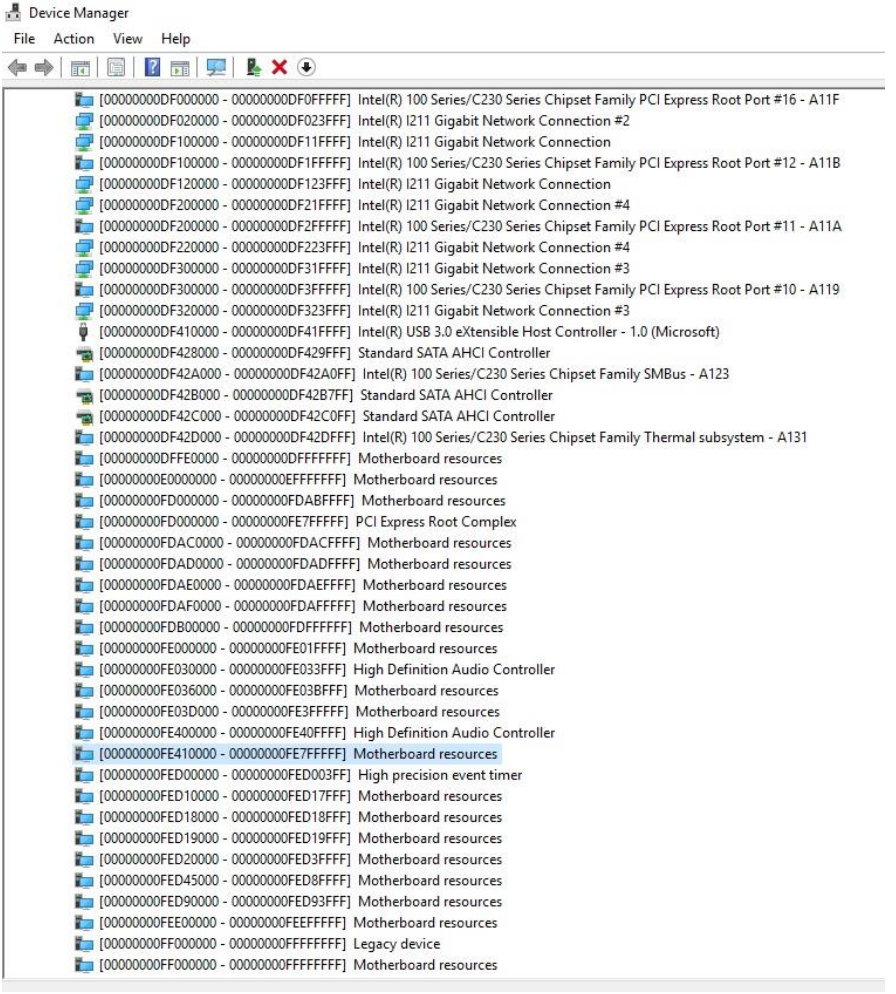
B.1 I/O Address Map



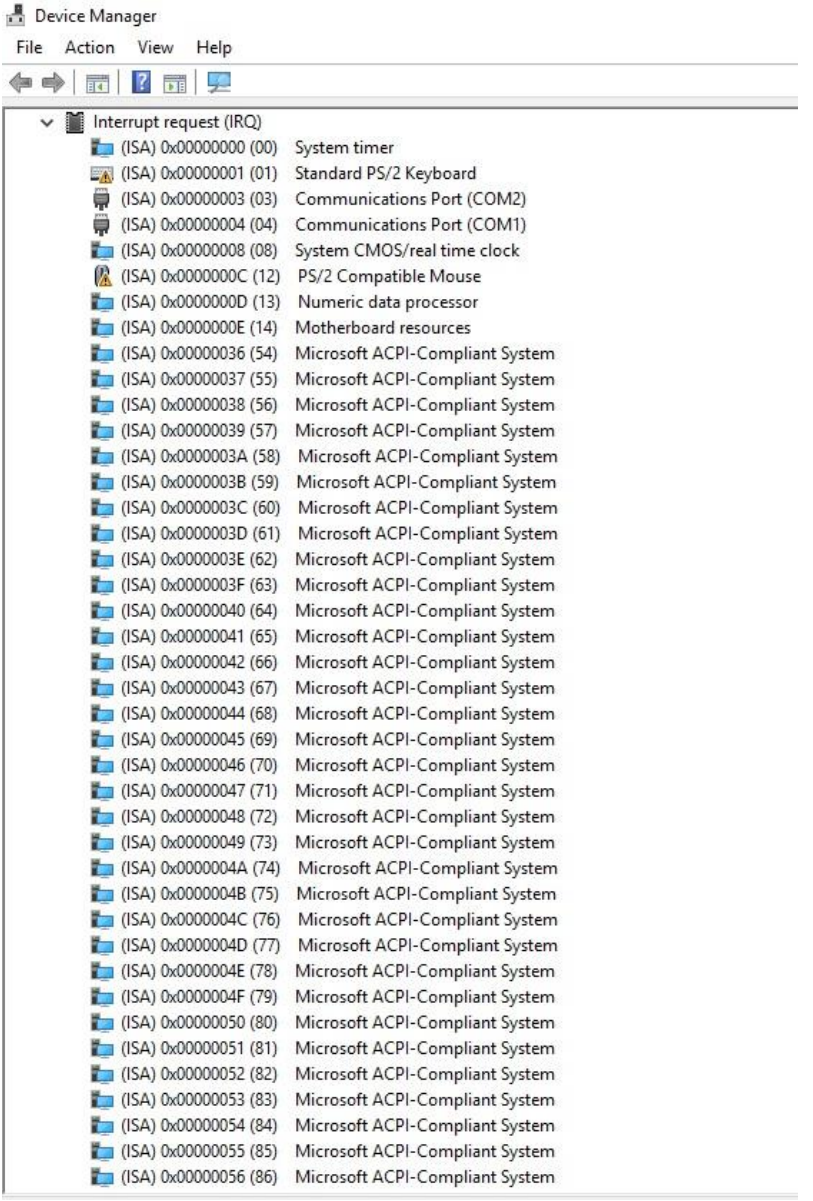

Device Manager
File Action View Help
[0000000000000800 - 000000000000087F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 00000000000018FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[000000000000B000 - 000000000000BFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #16 - A11F
[000000000000C000 - 000000000000CFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #12 - A11B
[000000000000D000 - 000000000000DFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #11 - A11A
[000000000000E000 - 000000000000EFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #10 - A119
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics 610
[000000000000F040 - 000000000000F05F] Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources

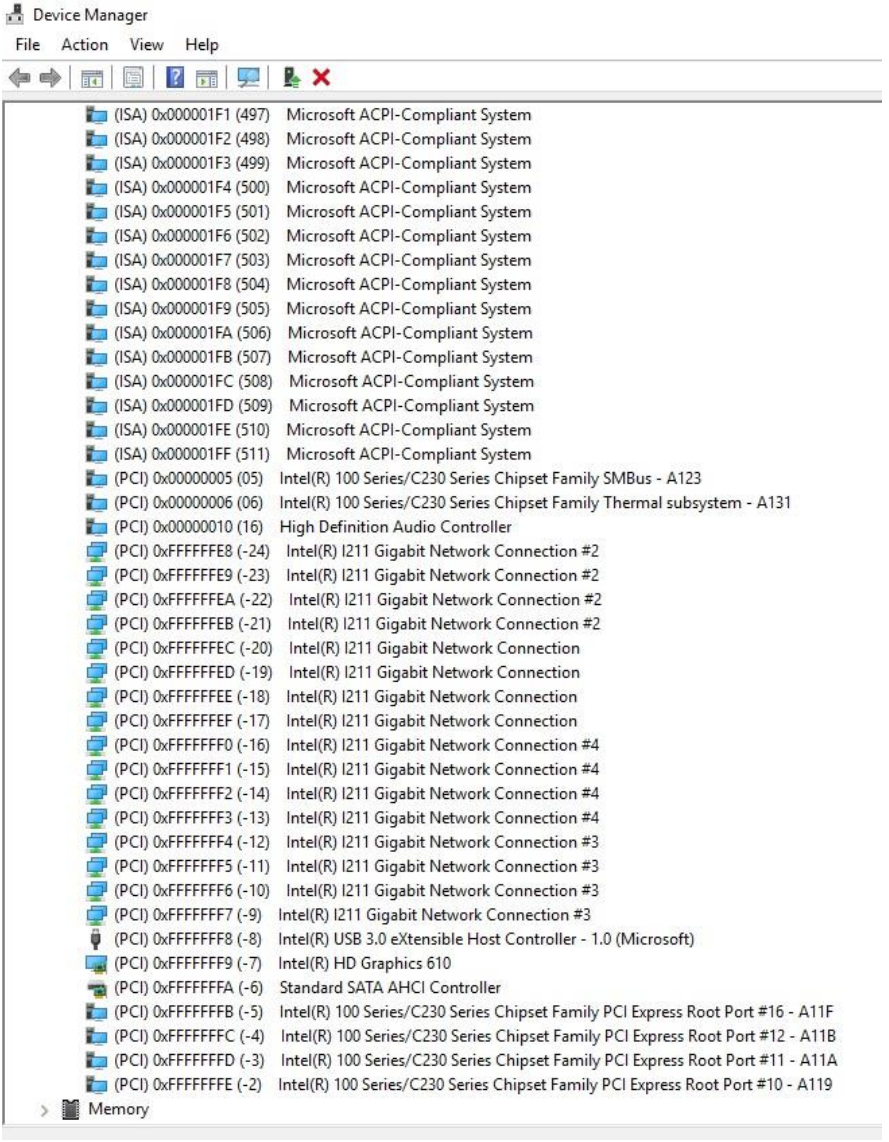
B.2 Memory Address Map




Device Manager
File Action View Help
[00000000DF000000 - 00000000DF0FFFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #16 - A11F
[00000000DF020000 - 00000000DF023FFF] Intel(R) I211 Gigabit Network Connection #2
[00000000DF100000 - 00000000DF11FFFF] Intel(R) I211 Gigabit Network Connection
[00000000DF100000 - 00000000DF1FFFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #12 - A11B
[00000000DF120000 - 00000000DF123FFF] Intel(R) I211 Gigabit Network Connection
[00000000DF200000 - 00000000DF21FFFF] Intel(R) I211 Gigabit Network Connection #4
[00000000DF200000 - 00000000DF2FFFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #11 - A11A
[00000000DF220000 - 00000000DF223FFF] Intel(R) I211 Gigabit Network Connection #4
[00000000DF300000 - 00000000DF31FFFF] Intel(R) I211 Gigabit Network Connection #3
[00000000DF300000 - 00000000DF3FFFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #10 - A119
[00000000DF320000 - 00000000DF323FFF] Intel(R) I211 Gigabit Network Connection #3
[00000000DF410000 - 00000000DF41FFFF] Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
[00000000DF428000 - 00000000DF429FFF] Standard SATA AHCI Controller
[00000000DF42A000 - 00000000DF42A0FF] Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[00000000DF42B000 - 00000000DF42B7FF] Standard SATA AHCI Controller
[00000000DF42C000 - 00000000DF42C0FF] Standard SATA AHCI Controller
[00000000DF42D000 - 00000000DF42DFFF] Intel(R) 100 Series/C230 Series Chipset Family Thermal subsystem - A131
[00000000DFFE0000 - 00000000DFFFFFFF] Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF] Motherboard resources
[00000000FD000000 - 00000000FDABFFFF] Motherboard resources
[00000000FD000000 - 00000000FE7FFFFF] PCI Express Root Complex
[00000000FDAC0000 - 00000000FDACFFFF] Motherboard resources
[00000000FDAD0000 - 00000000FDADFFFF] Motherboard resources
[00000000FDAE0000 - 00000000FDAEFFFF] Motherboard resources
[00000000FDAF0000 - 00000000FDAFFFFF] Motherboard resources
[00000000FDB00000 - 00000000FDFFFFFF] Motherboard resources
[00000000FE000000 - 00000000FE01FFFF] Motherboard resources
[00000000FE030000 - 00000000FE033FFF] High Definition Audio Controller
[00000000FE036000 - 00000000FE03BFFF] Motherboard resources
[00000000FE03D000 - 00000000FE3FFFFF] Motherboard resources
[00000000FE400000 - 00000000FE40FFFF] High Definition Audio Controller
[00000000FE410000 - 00000000FE7FFFFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED10000 - 00000000FED17FFF] Motherboard resources
[00000000FED18000 - 00000000FED18FFF] Motherboard resources
[00000000FED19000 - 00000000FED19FFF] Motherboard resources
[00000000FED20000 - 00000000FED3FFFF] Motherboard resources
[00000000FED45000 - 00000000FED8FFFF] Motherboard resources
[00000000FED90000 - 00000000FED93FFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF] Legacy device
[00000000FF000000 - 00000000FFFFFFFF] Motherboard resources

B.3 IRQ Mapping Chart




Device Manager
File Action View Help
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000005 (05) Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
(PCI) 0x00000006 (06) Intel(R) 100 Series/C230 Series Chipset Family Thermal subsystem - A131
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0xFFFFFFE8 (-24) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFE9 (-23) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEA (-22) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEB (-21) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEC (-20) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFED (-19) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEE (-18) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEF (-17) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF0 (-16) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFF1 (-15) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFF2 (-14) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFF3 (-13) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFF4 (-12) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF5 (-11) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF6 (-10) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF7 (-9) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF8 (-8) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFF9 (-7) Intel(R) HD Graphics 610
(PCI) 0xFFFFFFFA (-6) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFB (-5) Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #16 - A11F
(PCI) 0xFFFFFFFC (-4) Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #12 - A11B
(PCI) 0xFFFFFFFD (-3) Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #11 - A11A
(PCI) 0xFFFFFFFE (-2) Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #10 - A119
Memory

Appendix C

Digital I/O Ports

Pad Configuration DW0 (PAD_CFG_DW0_GPP_A_0)— Offset 400h

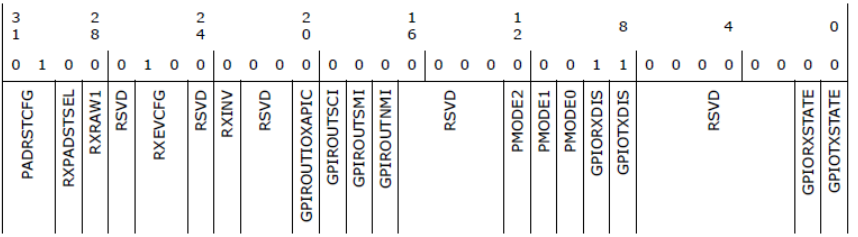
This register applies to GPP_A0.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4400xx00h



Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when a host reset (with or without power cycle) is initiated or a global reset is initiated, except that the reset does not assert when in S3/S4/S5. 10 = PLTRST# 11 = Reserved
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally

Bit Range	Default & Access	Field Name (ID): Description
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge 2h = Drive '0' 3h = Reserved (implement as setting 0h)
24	0h RO	Reserved.
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RO	Reserved.
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0h RW	**GPIO Input Route SMI (GPIROUTSMI):** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0h RW	**GPIO Input Route NMI (GPIROUTNMI):** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:13	0h RO	Reserved.
12	-- RW	**Pad Mode bit 2 (PMODE2):** See Pad Mode Bit 0 description.
11	-- RW	**Pad Mode bit 1 (PMODE1):** See Pad Mode Bit 0 description.

Bit Range	Default & Access	Field Name (ID): Description
10	-- RW	**Pad Mode bit 0 (PMODE0):** This bit is used in conjunction with Pad Mode bit 1 and 2 . This three-bit field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad 3h = native function 3, if applicable, controls the Pad 4h = enable GPIO blink/PWM capability if applicable (note that not all GPIOs have blink/PWM capability) Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad

C.2 Digital I/O Sample Code

```
UINT32     SOC_GPIO_BASE_ADDRESS=0xFDAE06A8,SOC_GPIO_VAL=0;
for (i = 0; i < 8; i++)
{
        SOC_GPIO_VAL=MmioRead32(SOC_GPIO_BASE_ADDRESS+8*i);
        if (SetupData.SOCGPPGx_Oe[i]==0)//GPIO set to input
          {
              SOC_GPIO_VAL |= BIT8;//Set bit 8
              SOC_GPIO_VAL &= (~BIT9);//Clear bit 9
          }
        else if (SetupData.SOCGPPGx_Oe[i]==1)//GPIO set to output
           {
              SOC_GPIO_VAL |= BIT9;//Set bit 9
              SOC_GPIO_VAL &= (~BIT8);//Clear bit 8
              if(SetupData.SOCGPPGx_Val[i]==0)
                  SOC_GPIO_VAL &= (~BIT0);//Clear bit 0 ==>Output LOW
              else
                   SOC_GPIO_VAL |= BIT0;//Set bit 0 ==>Output HIGH
            }
}
```

Appendix D

Watchdog Timer Programming

D.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s **Pulse width is must longer then 16ms.**
Signal Polarity	0x05	2	0	0: low active 1: high active **Must set this bit to 0**
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse **Must set this bit to 1**
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

D.2 Watchdog Sample Program

```
*****************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg         0x00   // Device configuration register
      #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
      #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
      #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
      #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
      #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
      #define   PolarityVal    0x00     // Low active for WDTRST#
      #define   UnitBit        0x03     // Unit for timer (Bit3)
      #define   ModeBit        0x04     // WDTRST# mode (Bit4)
      #define   ModeVal        0x01     // 0:level 1: pulse
      #define   EnableBit      0x05     // WDT timer enable (Bit5)
      #define   EnableVal      0x01     // 1: enable
      #define   StatusBit      0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*****************************************************************************

*****************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig(Counter, Unit);

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*****************************************************************************

*****************************************************************************
// Procedure : AaeonWDTEnable
```

```
VOID    AaeonWDTEnable (){
          WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
          // Disable WDT counting
          WDTEnableDisable(0);
          // Clear Watchdog Timeout Status
          WDTClearTimeoutStatus();
          // WDT relative parameter setting
          WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
          If (Value == 1)
              WDTSetBit(TimerReg, EnableBit, 1);
          else
              WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
          // Watchdog Timer counter setting
         WDTWriteByte(CounterReg, Counter);
        // WDT counting unit setting
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
          // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
```

```
VOID   WDTWriteByte(byte Register, byte Value){
       IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
       return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
       byte TmpValue;

       TmpValue = WDTReadByte(Register);
       TmpValue &= ~(1 << Bit);
       TmpValue |= Val << Bit;
       WDTWriteByte(Register, TmpValue);
}

*******************************************************************************
```