**COM-TGUC6 C10**

COM Express Module

**User’s Manual 1st Ed**

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##### Packing List

Before setting up your product, please make sure the following items have been shipped:

|  |  |
| --- | --- |
| **Item** | **Quantity** |
| * COM-TGUC6 C10 | 1 |

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

##### About this Document

This User’s Manual contains all the essential information, such as detailed descriptions and explanations on the product’s hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

##### Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system’s hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
17. If any of the following situations arises, please the contact our service personnel:
18. Damaged power cord or plug
19. Liquid intrusion to the device
20. Exposure to moisture
21. Device is not working as expected or in a manner as described in this manual
22. The device is dropped or damaged
23. Any obvious signs of damage displayed on the device
24. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE’S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

##### FCC Statement

|  |  |
| --- | --- |
|  | This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation. |

***Caution:***

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer’s instructions and your local government’s recycling or disposal directives.*

***Attention:***

*Il y a un risque d’explosion si la batterie est remplacée de façon incorrecte.*

*Ne la remplacer qu’avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

**China RoHS Requirements (CN)**

|  |  |
| --- | --- |
| 产品中有毒有害物质或元素名称及含量 | |
| AAEON 主板/子板/背板 | QO4-381 Rev.A2 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 部件名称 | 有毒有害物质或元素 | | | | | |
| 铅  (Pb) | 汞  (Hg) | 镉  (Cd) | 六价铬(Cr(VI)) | 多溴联苯(PBB) | 多溴二苯醚(PBDE) |
| 印刷电路板  及其电子组件 | × | ○ | ○ | ○ | ○ | ○ |
| 外部信号  连接器及线材 | × | ○ | ○ | ○ | ○ | ○ |
| 本表格依据 SJ/T 11364 的规定编制。  ○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。  ×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。  环保使用期限(EFUP (Environmental Friendly Use Period)) : 10年  备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。 | | | | | | |

**China RoHS Requirement (EN)**

|  |  |
| --- | --- |
| Name and content of hazardous substances in product | |
| AAEON Main Board/Daughter Board/Backplane | QO4-381 Rev.A2 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Part Name | Hazardous Substances | | | | | |
| 铅  (Pb) | 汞  (Hg) | 镉  (Cd) | 六价铬(Cr(VI)) | 多溴联苯(PBB) | 多溴二苯醚(PBDE) |
| PCB Assemblies | × | ○ | ○ | ○ | ○ | ○ |
| Connector and Cable | × | ○ | ○ | ○ | ○ | ○ |
| The table is prepared in accordance with the provisions of SJ/T 11364.  ○：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.  ×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).  EFUP (Environment Friendly Use Period) value: 10 years  Notes: This product defined period of use is under normal condition. | | | | | | |

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**Chapter 1**

# Chapter 1 - Product Specifications

## 1.1 Specifications

| **System** |  |
| --- | --- |
| **Form Factor** | COM Express Compact Size, Type 6 |
| **CPU** | 11th Generation Intel® Core™ Processors:  Intel® Core™ i7-1185G7E (4C/8T, 1.8 GHz, 15W)  Intel® Core™ i5-1145G7E (4C/8T, 1.5 GHz, 15W)  Intel® Core™ i3-1115G4E (2C/4T, 2.20 GHz, 15W)  Intel® Celeron® Processor 6000 Series:  Intel® Celeron® 6305E Processor (2C/2T 1.80 GHz, 15W) |
| **Chipset** | Integrated with Intel® SoC |
| **Memory** | DDR4 3200MHz Dual Channel SODIMM x 2, up to 64GB (In-Band ECC by SKU) |
| **Onboard Storage** | - |
| **BIOS** | AMI UEFI |
| **Wake on LAN** | Yes |
| **Watchdog Timer** | 255 Levels |
| **Dimension** | 3.74" x 3.74" (95mm x 95mm) |
| **Security** | TPM 2.0 |
| **OS Support** | Windows® 10 (64-bit)  Linux Ubuntu 20.04.2/Kernel 5.8 |

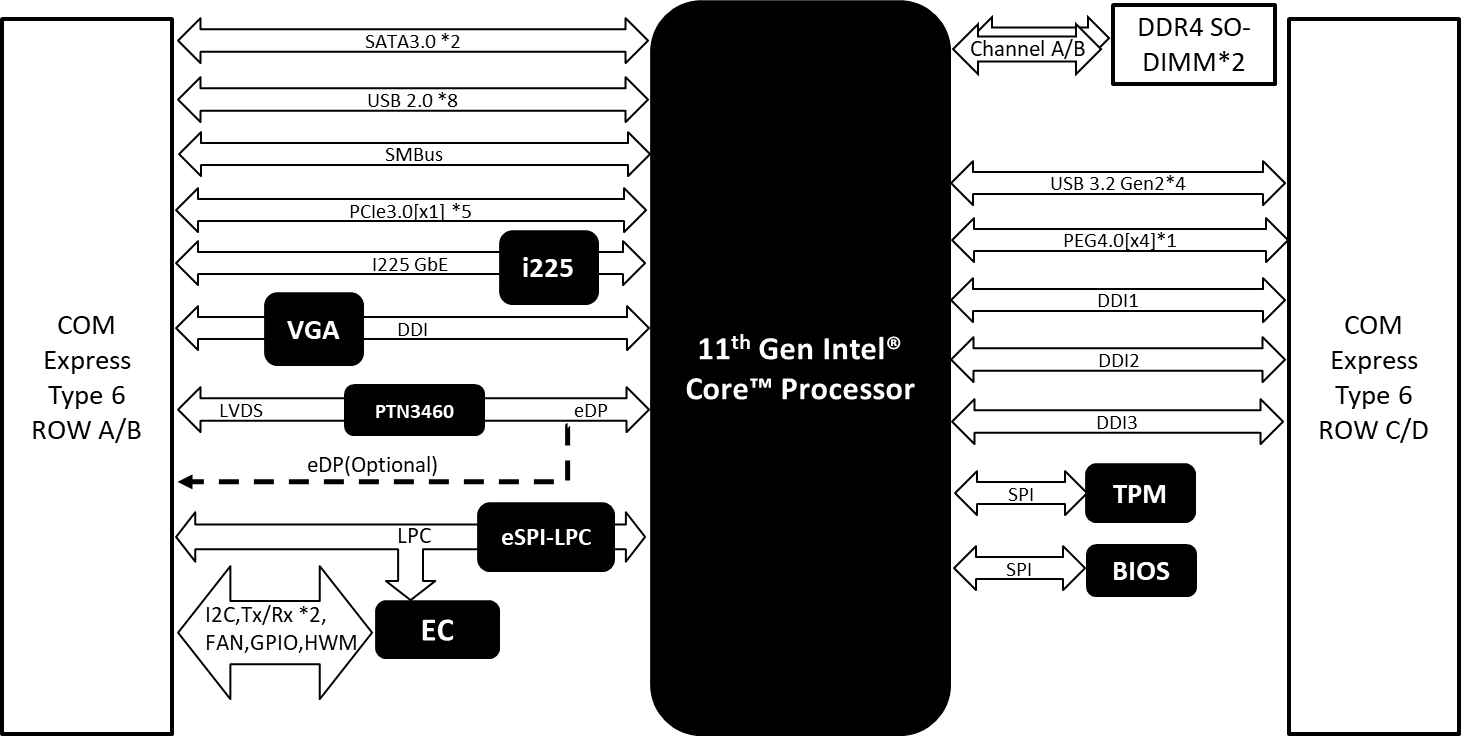
|  |  |
| --- | --- |
| **Power** |  |
| **Power Requirement** | +12V and +5VSB for ATX, +12V for AT |
| **Power Type** | AT/ATX |
| **Power Consumption (Typical)** | Intel® Core™ i7-1185G7E, 3.22A @+12V |

| **Display** |  |
| --- | --- |
| **Graphics Controller** | Intel® Iris® Xe Graphics  Intel® UHD Graphics |
| **Video Output** | 4 Simultaneous Displays:  DDI x 3, up to 3840 x 2160  18/24-bit Single/Dual-Channel LVDS/eDP x 1,  up to 1920 x 1080/3840 x 2160  VGA x 1, up to 1920 x 1080 |

|  |  |
| --- | --- |
| **I/O** |  |
| **Ethernet** | Intel® Ethernet Controller I225/I226, 2.5GbE x 1 |
| **Audio** | High Definition Audio Interface |
| **USB Port** | USB 2.0 x 8  USB 3.2 Gen 2 x 4 |
| **Serial Port** | 2-Wire UART x 2 (Tx/Rx) |
| **HDD Interface** | SATA 6Gb/s x 2 |
| **Expansion** | PEG 4.0 [x4] x 1  PCIe 3.0 [x1] x 5  LPC x 1 |
| **GPIO** | 8-bit |
| **SMBus/I2C** | I2C x 1  SMBus x 1 |

|  |  |
| --- | --- |
| **Environmental** |  |
| **Operating Temperature** | 32°F ~ 140°F (0°C ~ 60°C) |
| **Storage Temperature** | -40°F ~ 185°F (-40°C ~ 85°C) |
| **Operating Humidity** | 0% ~ 90% relative humidity, non-condensing |
| **EMC** | CE/FCC Class A |
| **Weight** | 0.44 lb. (0.20Kg) |

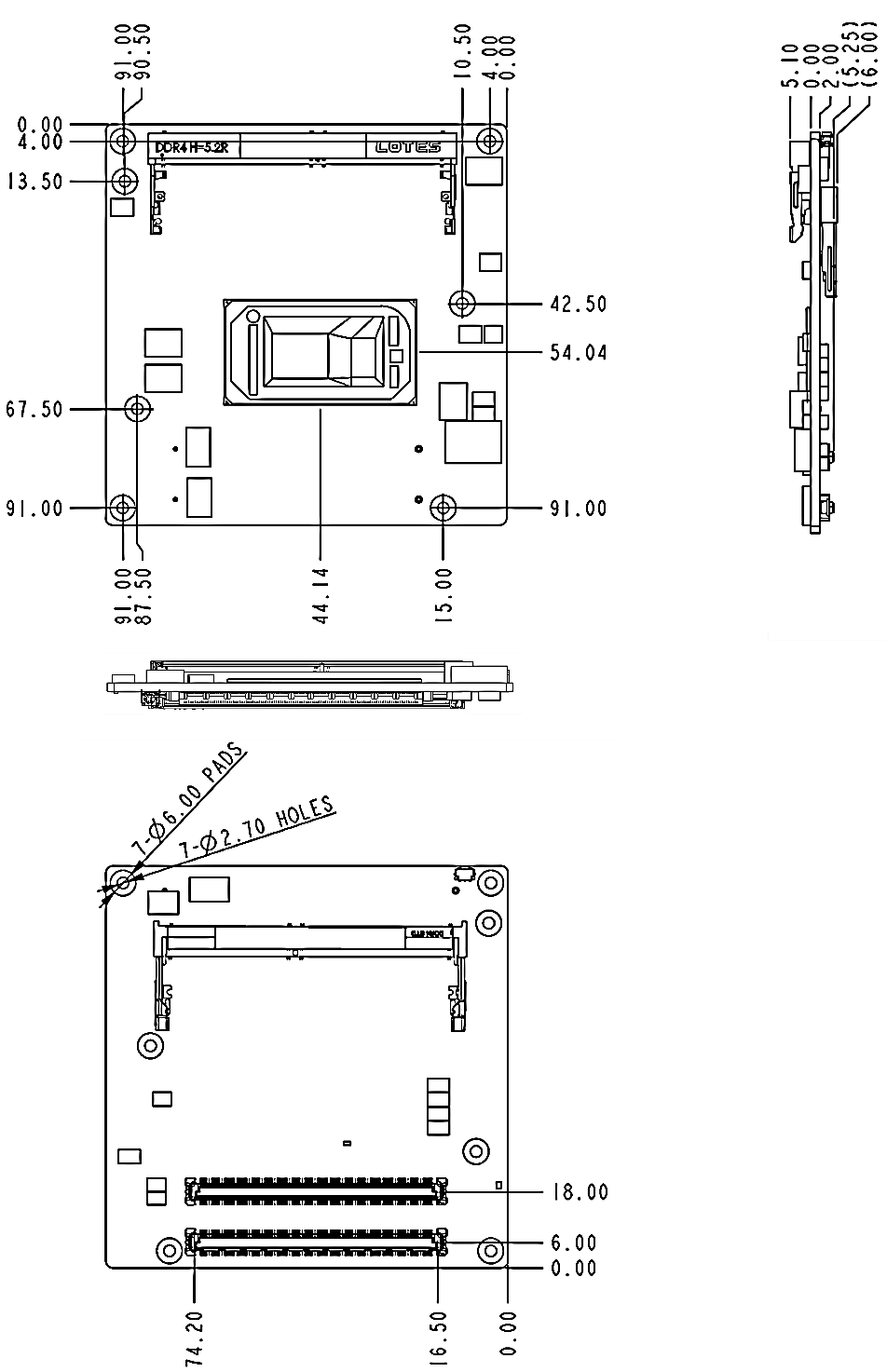
## 1.2 Block Diagram



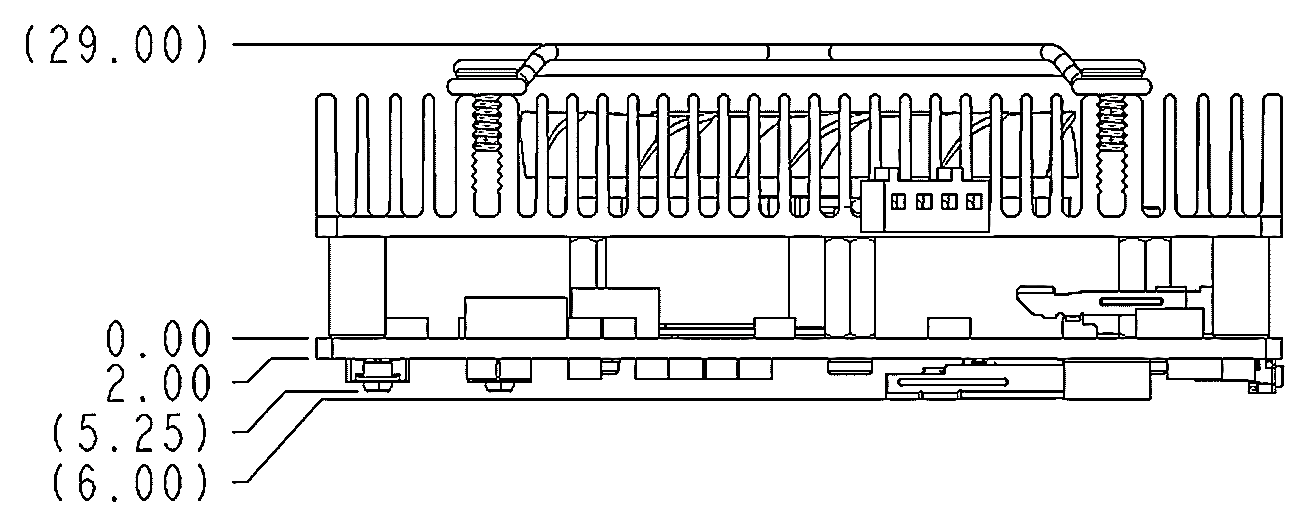
**Chapter 2**

# Chapter 2 – Hardware Information

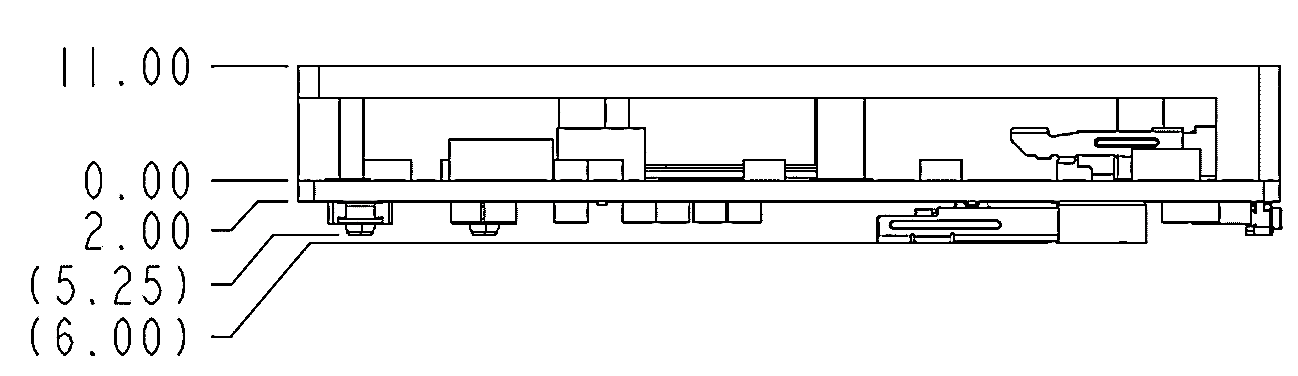
## 2.1 Dimensions

****

**With Active Cooling (Part No: COM-TGUC6-FAN01)**

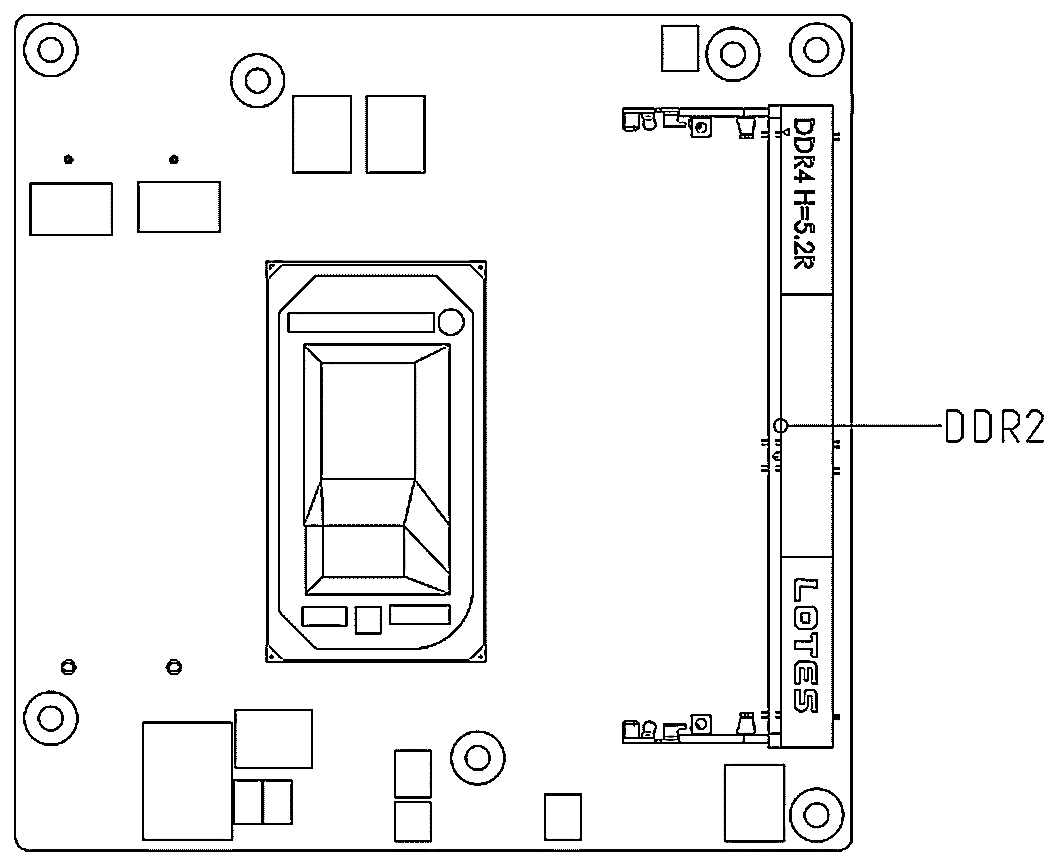
****

**With Heat Spreader (Part No: COM-TGUC6-HSP01)**

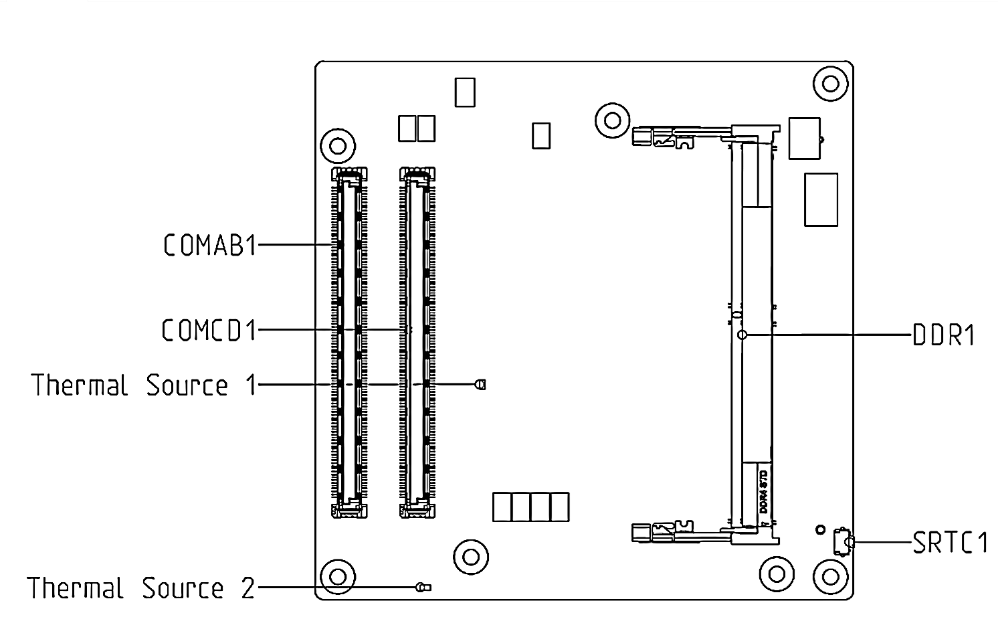
****

## 2.2 Jumpers and Connectors

**Component Side**



**Solder Side**



## 2.3 List of Connectors

Please refer to the table below for all of the board’s connectors that you can configure for your application

|  |  |
| --- | --- |
| **Label** | **Function** |
| **COMAB1** | ROW A/B |
| **COMCD1** | ROW C/D |
| **DDR1** | DDR4 SODIMM Connector |
| **DDR2** | DDR4 SODIMM Connector |
| **SRTC1** | Push Button for RTC reset |

### 2.3.1 COM Row A/B Connector (COMAB1)

| **Row A** | | **Row B** | | | |
| --- | --- | --- | --- | --- | --- |
| **Pin** | **Signal** | | **Pin** | **Signal** |
| **A1** | GND (FIXED) | | **B1** | GND (FIXED) |
| **A2** | GBE0\_MDI3- | | **B2** | GBE0\_ACT# |
| **A3** | GBE0\_MDI3+ | | **B3** | **LPC\_FRAME#** |
| **A4** | GBE0\_LINK100# | | **B4** | **LPC\_AD0** |
| **A5** | GBE0\_LINK1000# | | **B5** | **LPC\_AD1** |
| **A6** | GBE0\_MDI2- | | **B6** | **LPC\_AD2** |
| **A7** | GBE0\_MDI2+ | | **B7** | **LPC\_AD3** |
| **A8** | GBE0\_LINK# | | **B8** | **NA** |
| **A9** | GBE0\_MDI1- | | **B9** | **NA** |
| **A10** | GBE0\_MDI1+ | | **B10** | **LPC\_CLK** |
| **A11** | GND (FIXED) | | **B11** | GND (FIXED) |
| **A12** | GBE0\_MDI0- | | **B12** | PWRBTN# |
| **A13** | GBE0\_MDI0+ | | **B13** | SMB\_CK |
| **A14** | **NA** | | **B14** | SMB\_DAT |
| **A15** | SUS\_S3# | | **B15** | SMB\_ALERT# |
| **A16** | SATA0\_TX+ | | **B16** | SATA1\_TX+ |
| **A17** | SATA0\_TX- | | **B17** | SATA1\_TX- |
| **A18** | SUS\_S4# | | **B18** | SUS\_STAT# |
| **A19** | SATA0\_RX+ | | **B19** | SATA1\_RX+ |
| **A20** | SATA0\_RX- | | **B20** | SATA1\_RX- |
| **A21** | GND (FIXED) | | **B21** | GND (FIXED) |
| **A22** | **NA** | | **B22** | **NA** |
| **A23** | **NA** | | **B23** | **NA** |
| **A24** | SUS\_S5# | | **B24** | PWR\_OK |
| **A25** | **NA** | | **B25** | **NA** |
| **A26** | **NA** | | **B26** | **NA** |
| **A27** | BATLOW# | | **B27** | WDT |
| **A28** | (S)ATA\_ACT# | | **B28** | **NA** |
| **A29** | AC/HDA\_SYNC | | **B29** | HDA\_SDIN1 |
| **A30** | AC/HDA\_RST# | | **B30** | HDA\_SDIN0 |
| **A31** | GND (FIXED) | | **B31** | GND (FIXED) |
| **A32** | HDA\_BITCLK | | **B32** | SPKR |
| **A33** | HDA\_SDOUT | | **B33** | I2C\_CK |
| **A34** | BIOS\_DIS0# | | **B34** | I2C\_DAT |
| **A35** | THRMTRIP# | | **B35** | THRM# |
| **A36** | USB6- | | **B36** | USB7- |
| **A37** | USB6+ | | **B37** | USB7+ |
| **A38** | USB\_6\_7\_OC# | | **B38** | USB\_4\_5\_OC# |
| **A39** | USB4- | | **B39** | USB5- |
| **A40** | USB4+ | | **B40** | USB5+ |
| **A41** | GND (FIXED) | | **B41** | GND (FIXED) |
| **A42** | USB2- | | **B42** | USB3- |
| **A43** | USB2+ | | **B43** | USB3+ |
| **A44** | USB\_2\_3\_OC# | | **B44** | USB\_0\_1\_OC# |
| **A45** | USB0- | | **B45** | USB1- |
| **A46** | USB0+ | | **B46** | USB1+ |
| **A47** | VCC\_RTC | | **B47** | **NA** |
| **A48** | **RSMRST\_OUT#** | | **B48** | **NA** |
| **A49** | **NA** | | **B49** | SYS\_RESET# |
| **A50** | LPC\_SERIRQ | | **B50** | CB\_RESET# |
| **A51** | GND (FIXED) | | **B51** | GND (FIXED) |
| **A52** | **NA** | | **B52** | **NA** |
| **A53** | **NA** | | **B53** | **NA** |
| **A54** | GPI0 | | **B54** | GPO1 |
| **A55** | PCIE\_TX4+ | | **B55** | PCIE\_RX4+ |
| **A56** | PCIE\_TX4- | | **B56** | PCIE\_RX4- |
| **A57** | GND | | **B57** | GPO2 |
| **A58** | PCIE\_TX3+ | | **B58** | PCIE\_RX3+ |
| **A59** | PCIE\_TX3- | | **B59** | PCIE\_RX3- |
| **A60** | GND (FIXED) | | **B60** | GND (FIXED) |
| **A61** | PCIE\_TX2+ | | **B61** | PCIE\_RX2+ |
| **A62** | PCIE\_TX2- | | **B62** | PCIE\_RX2- |
| **A63** | GPI1 | | **B63** | GPO3 |
| **A64** | PCIE\_TX1+ | | **B64** | PCIE\_RX1+ |
| **A65** | PCIE\_TX1- | | **B65** | PCIE\_RX1- |
| **A66** | GND | | **B66** | WAKE0# |
| **A67** | GPI2 | | **B67** | WAKE1# |
| **A68** | PCIE\_TX0+ | | **B68** | PCIE\_RX0+ |
| **A69** | PCIE\_TX0- | | **B69** | PCIE\_RX0- |
| **A70** | GND (FIXED) | | **B70** | GND (FIXED) |
| **A71** | LVDS\_A0+ | | **B71** | LVDS\_B0+ |
| **A72** | LVDS\_A0- | | **B72** | LVDS\_B0- |
| **A73** | LVDS\_A1+ | | **B73** | LVDS\_B1+ |
| **A74** | LVDS\_A1- | | **B74** | LVDS\_B1- |
| **A75** | LVDS\_A2+ | | **B75** | LVDS\_B2+ |
| **A76** | LVDS\_A2- | | **B76** | LVDS\_B2- |
| **A77** | LVDS\_VDD\_EN | | **B77** | LVDS\_B3+ |
| **A78** | LVDS\_A3+ | | **B78** | LVDS\_B3- |
| **A79** | LVDS\_A3- | | **B79** | LVDS\_BKLT\_EN |
| **A80** | GND (FIXED) | | **B80** | GND (FIXED) |
| **A81** | LVDS\_A\_CK+ | | **B81** | LVDS\_B\_CK+ |
| **A82** | LVDS\_A\_CK- | | **B82** | LVDS\_B\_CK- |
| **A83** | LVDS\_I2C\_CK | | **B83** | LVDS\_BKLT\_CTRL |
| **A84** | LVDS\_I2C\_DAT | | **B84** | VCC\_5V\_SBY |
| **A85** | GPI3 | | **B85** | VCC\_5V\_SBY |
| **A86** | **NA** | | **B86** | VCC\_5V\_SBY |
| **A87** | EDP\_HPD | | **B87** | VCC\_5V\_SBY |
| **A88** | PCIE\_CLK\_REF+ | | **B88** | BIOS\_DIS1# |
| **A89** | PCIE\_CLK\_REF- | | **B89** | VGA\_RED |
| **A90** | GND (FIXED) | | **B90** | GND (FIXED) |
| **A91** | SPI\_POWER | | **B91** | VGA\_GRN |
| **A92** | **NA** | | **B92** | VGA\_BLU |
| **A93** | GPO0 | | **B93** | VGA\_HSYNC |
| **A94** | **NA** | | **B94** | VGA\_VSYNC |
| **A95** | **NA** | | **B95** | VGA\_I2C\_CK |
| **A96** | TPM\_PP | | **B96** | VGA\_I2C\_DAT |
| **A97** | **NA** | | **B97** | **NA** |
| **A98** | SER0\_TX | | **B98** | **NA** |
| **A99** | SER0\_RX | | **B99** | **NA** |
| **A100** | GND (FIXED) | | **B100** | GND (FIXED) |
| **A101** | SER1\_TX | | **B101** | FAN\_PWMOUT |
| **A102** | SER1\_RX | | **B102** | FAN\_TACHIN |
| **A103** | LID# | | **B103** | SLEEP# |
| **A104** | VCC\_12V | | **B104** | VCC\_12V |
| **A105** | VCC\_12V | | **B105** | VCC\_12V |
| **A106** | VCC\_12V | | **B106** | VCC\_12V |
| **A107** | VCC\_12V | | **B107** | VCC\_12V |
| **A108** | VCC\_12V | | **B108** | VCC\_12V |
| **A109** | VCC\_12V | | **B109** | VCC\_12V |
| **A110** | GND (FIXED) | | **B110** | GND (FIXED) |

### 2.4.2 COM Row C/D Connector (COMCD1)

| **Row C** | | | **Row D** | | |
| --- | --- | --- | --- | --- | --- |
| **Pin** | **Signal** | **Pin** | | **Signal** |
| **C1** | GND (FIXED) | **D1** | | GND (FIXED) |
| **C2** | GND | **D2** | | GND |
| **C3** | USB\_SSRX0- | **D3** | | USB\_SSTX0- |
| **C4** | USB\_SSRX0+ | **D4** | | USB\_SSTX0+ |
| **C5** | GND | **D5** | | GND |
| **C6** | USB\_SSRX1- | **D6** | | USB\_SSTX1- |
| **C7** | USB\_SSRX1+ | **D7** | | USB\_SSTX1+ |
| **C8** | GND | **D8** | | GND |
| **C9** | USB\_SSRX2- | **D9** | | USB\_SSTX2- |
| **C10** | USB\_SSRX2+ | **D10** | | USB\_SSTX2+ |
| **C11** | GND (FIXED) | **D11** | | GND (FIXED) |
| **C12** | USB\_SSRX3- | **D12** | | USB\_SSTX3- |
| **C13** | USB\_SSRX3+ | **D13** | | USB\_SSTX3+ |
| **C14** | GND | **D14** | | GND |
| **C15** | **NA** | **D15** | | DDI1\_CTRLCLK\_AUX+ |
| **C16** | **NA** | **D16** | | DDI1\_CTRLDATA\_AUX- |
| **C17** | RSVD | **D17** | | RSVD10 |
| **C18** | **GND** | **D18** | | RSVD10 |
| **C19** | **NA** | **D19** | | **NA** |
| **C20** | **NA** | **D20** | | **NA** |
| **C21** | GND (FIXED) | **D21** | | GND(FIXED) |
| **C22** | **NA** | **D22** | | **NA** |
| **C23** | **NA** | **D23** | | **NA** |
| **C24** | DDI1\_HPD | **D24** | | **GND** |
| **C25** | **NA** | **D25** | | **GND** |
| **C26** | **NA** | **D26** | | DDI1\_PAIR0+ |
| **C27** | RSVD | **D27** | | DDI1\_PAIR0- |
| **C28** | RSVD | **D28** | | RSVD10 |
| **C29** | **NA** | **D29** | | DDI1\_PAIR1+ |
| **C30** | **NA** | **D30** | | DDI1\_PAIR1- |
| **C31** | GND(FIXED) | **D31** | | GND(FIXED) |
| **C32** | DDI2\_CTRLCLK\_AUX+ | **D32** | | DDI1\_PAIR2+ |
| **C33** | DDI2\_CTRLDATA\_AUX- | **D33** | | DDI1\_PAIR2- |
| **C34** | DDI2\_DDC\_AUX\_SEL | **D34** | | DDI1\_DDC\_AUX\_SEL |
| **C35** | RSVD | **D35** | | RSVD10 |
| **C36** | DDI3\_CTRLCLK\_AUX+ | **D36** | | DDI1\_PAIR3+ |
| **C37** | DDI3\_CTRLDATA\_AUX- | **D37** | | DDI1\_PAIR3- |
| **C38** | DDI3\_DDC\_AUX\_SEL | **D38** | | **GND** |
| **C39** | DDI3\_PAIR0+ | **D39** | | DDI2\_PAIR0+ |
| **C40** | DDI3\_PAIR0- | **D40** | | DDI2\_PAIR0- |
| **C41** | GND(FIXED) | **D41** | | GND(FIXED) |
| **C42** | DDI3\_PAIR1+ | **D42** | | DDI2\_PAIR1+ |
| **C43** | DDI3\_PAIR1- | **D43** | | DDI2\_PAIR1- |
| **C44** | DDI3\_HPD | **D44** | | DDI2\_HPD |
| **C45** | RSVD10 | **D45** | | **GND** |
| **C46** | DDI3\_PAIR2+ | **D46** | | DDI2\_PAIR2+ |
| **C47** | DDI3\_PAIR2- | **D47** | | DDI2\_PAIR2- |
| **C48** | RSVD10 | **D48** | | **GND** |
| **C49** | DDI3\_PAIR3+ | **D49** | | DDI2\_PAIR3+ |
| **C50** | DDI3\_PAIR3- | **D50** | | DDI2\_PAIR3- |
| **C51** | GND(FIXED) | **D51** | | GND(FIXED) |
| **C52** | PEG\_RX0+ | **D52** | | PEG\_TX0+ |
| **C53** | PEG\_RX0- | **D53** | | PEG\_TX0- |
| **C54** | **NA** | **D54** | | PEG\_LANE\_RV# |
| **C55** | PEG\_RX1+ | **D55** | | PEG\_TX1+ |
| **C56** | PEG\_RX1- | **D56** | | PEG\_TX1- |
| **C57** | **NA** | **D57** | | TYPE2# |
| **C58** | PEG\_RX2+ | **D58** | | PEG\_TX2+ |
| **C59** | PEG\_RX2- | **D59** | | PEG\_TX2- |
| **C60** | GND(FIXED) | **D60** | | GND(FIXED) |
| **C61** | PEG\_RX3+ | **D61** | | PEG\_TX3+ |
| **C62** | PEG\_RX3- | **D62** | | PEG\_TX3- |
| **C63** | **GND** | **D63** | | **GND** |
| **C64** | **GND** | **D64** | | **GND** |
| **C65** | **NA** | **D65** | | **NA** |
| **C66** | **NA** | **D66** | | **NA** |
| **C67** | RSVD | **D67** | | GND |
| **C68** | **NA** | **D68** | | **NA** |
| **C69** | **NA** | **D69** | | **NA** |
| **C70** | GND (FIXED) | **D70** | | GND(FIXED) |
| **C71** | **NA** | **D71** | | **NA** |
| **C72** | **NA** | **D72** | | **NA** |
| **C73** | GND | **D73** | | GND |
| **C74** | **NA** | **D74** | | **NA** |
| **C75** | **NA** | **D75** | | **NA** |
| **C76** | GND | **D76** | | GND |
| **C77** | **GND** | **D77** | | **GND** |
| **C78** | **NA** | **D78** | | **NA** |
| **C79** | **NA** | **D79** | | **NA** |
| **C80** | GND (FIXED) | **D80** | | GND(FIXED) |
| **C81** | **NA** | **D81** | | **NA** |
| **C82** | **NA** | **D82** | | **NA** |
| **C83** | **GND** | **D83** | | **GND** |
| **C84** | GND | **D84** | | GND |
| **C85** | **NA** | **D85** | | **NA** |
| **C86** | **NA** | **D86** | | **NA** |
| **C87** | GND | **D87** | | GND |
| **C88** | **NA** | **D88** | | **NA** |
| **C89** | **NA** | **D89** | | **NA** |
| **C90** | GND (FIXED) | **D90** | | GND(FIXED) |
| **C91** | **NA** | **D91** | | **NA** |
| **C92** | **NA** | **D92** | | **NA** |
| **C93** | GND | **D93** | | GND |
| **C94** | **NA** | **D94** | | **NA** |
| **C95** | **NA** | **D95** | | **NA** |
| **C96** | GND | **D96** | | GND |
| **C97** | **GND** | **D97** | | **GND** |
| **C98** | **NA** | **D98** | | **NA** |
| **C99** | **NA** | **D99** | | **NA** |
| **C100** | GND (FIXED) | **D100** | | GND(FIXED) |
| **C101** | **NA** | **D101** | | **NA** |
| **C102** | **NA** | **D102** | | **NA** |
| **C103** | GND | **D103** | | GND |
| **C104** | VCC\_12V | **D104** | | VCC\_12V |
| **C105** | VCC\_12V | **D105** | | VCC\_12V |
| **C106** | VCC\_12V | **D106** | | VCC\_12V |
| **C107** | VCC\_12V | **D107** | | VCC\_12V |
| **C108** | VCC\_12V | **D108** | | VCC\_12V |
| **C109** | VCC\_12V | **D109** | | VCC\_12V |
| **C110** | GND (FIXED) | **D110** | | GND(FIXED) |

**Chapter 3**

# Chapter 3 - AMI BIOS Setup

## 3.1 System Test and Initialization

The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

* You are starting your system for the first time.
* You have changed the hardware attached to your system.
* The CMOS memory has lost power and the configuration information has been erased.

The COM-TGUC6 C10 CMOS memory uses a backup battery for data retention. The battery must be replaced if it runs out of power.

## 3.2 AMI BIOS Setup

The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off.

To enter Setup, power on the computer and press <Del> immediately.

The function of each menu is as follows:

**Main –** Date and time can be set here. Use <Tab> to switch between date elements.

**Advanced –** Enable/disable boot option for legacy network devices.

**System I/O** – System I/O information and configuration.

**Security** – Password for setup administrator can be set here.

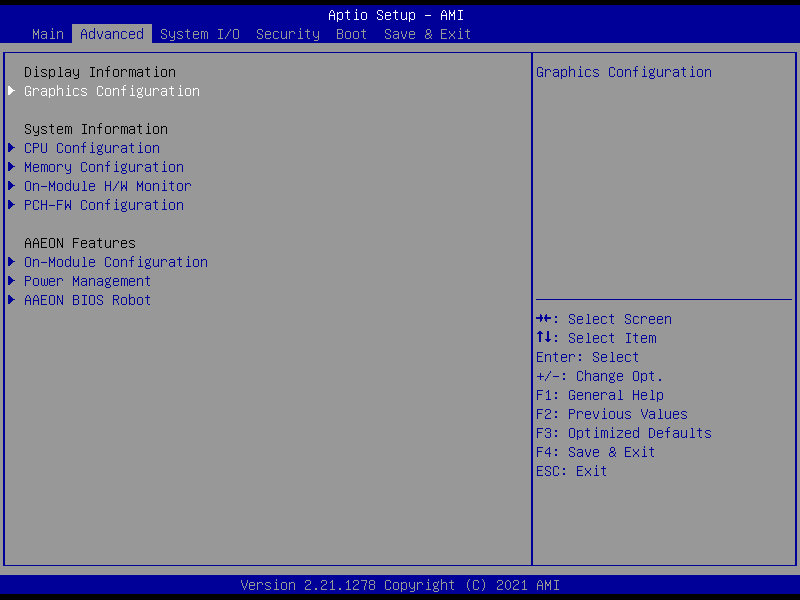
**Boot** – Enable/disable Quiet Boot option.

**Save & Exit** – Save changes and exit Setup.

## 3.3 Setup Submenu: Main



## 3.4 Setup Submenu: Advanced

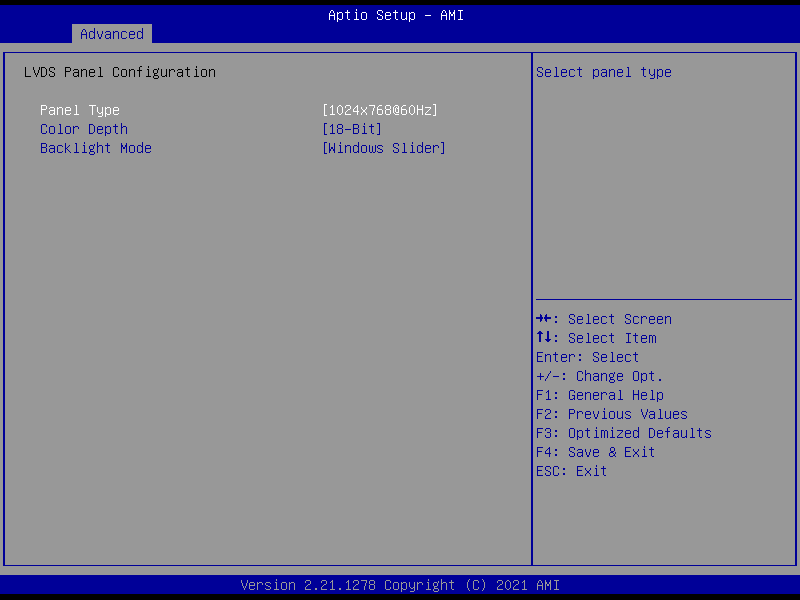


### 3.4.1 Graphics Configuration



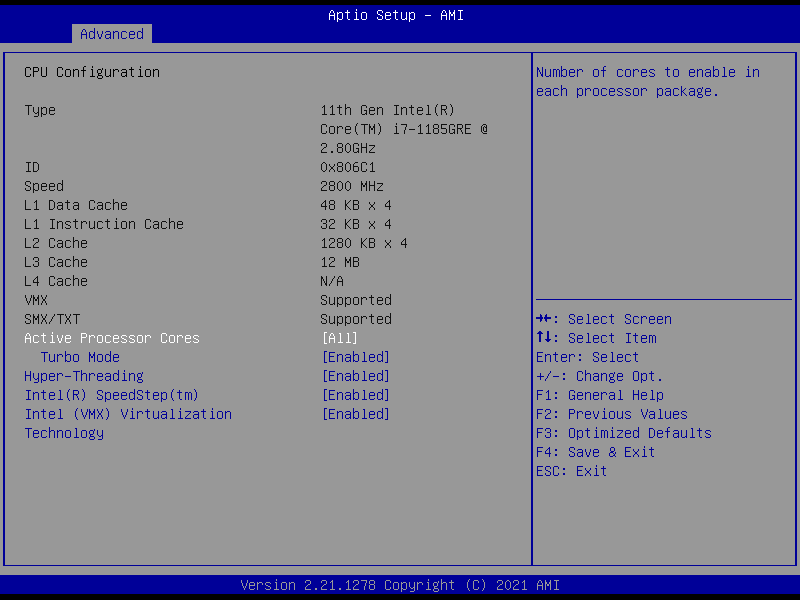
| **Options Summary** | | |
| --- | --- | --- |
| **VBT Select** | LVDS On |  |
| eDP On |  |
| eDP/LVDS Off | Optimal Default, Failsafe Default |
| Select VBT for GOP Driver. | | |

#### 3.4.1.1 LVDS Panel Configuration



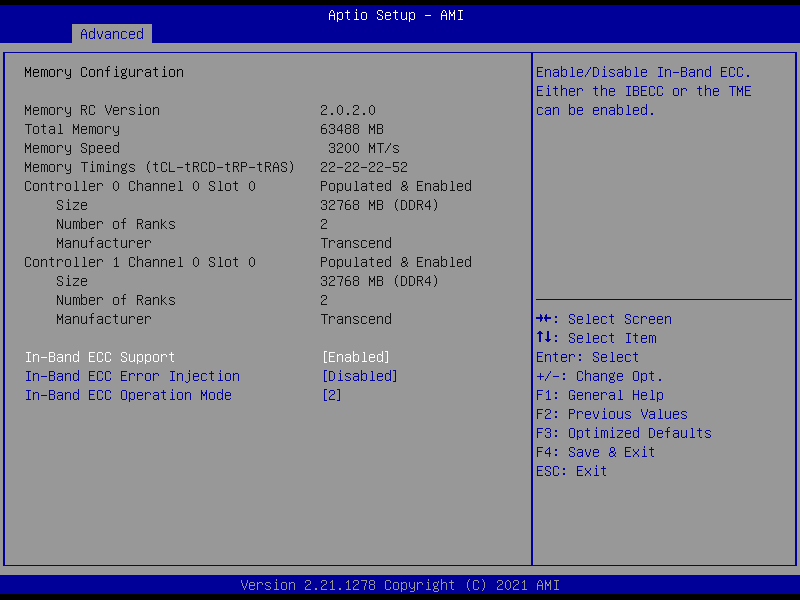
| **Options Summary** | | |
| --- | --- | --- |
| **Panel Type** | 640x480@60Hz |  |
| 800x480@60Hz |  |
| 800x600@60Hz |  |
| 1024x600@60Hz |  |
| 1024x768@60Hz | Optimal Default, Failsafe Default |
| 1280x768@60Hz |  |
| 1280x800@60Hz |  |
| 1280x1024@60Hz |  |
| 1366x768@60Hz |  |
| 1440x900@60Hz |  |
| 1600x1200@60Hz |  |
| 1920x1080@60Hz |  |
| 1920x1200@60Hz |  |
| Select panel type. | | |
| **Color Depth** | 18-Bit | Optimal Default, Failsafe Default |
| 24-Bit |  |
| 36-Bit |  |
| 48-Bit |  |
| Select panel type. | | |
| **Backlight Mode** | BIOS & Application |  |
| Windows Slider | Optimal Default, Failsafe Default |
| Select backlight control signal type. | | |

### 3.4.2 CPU Configuration



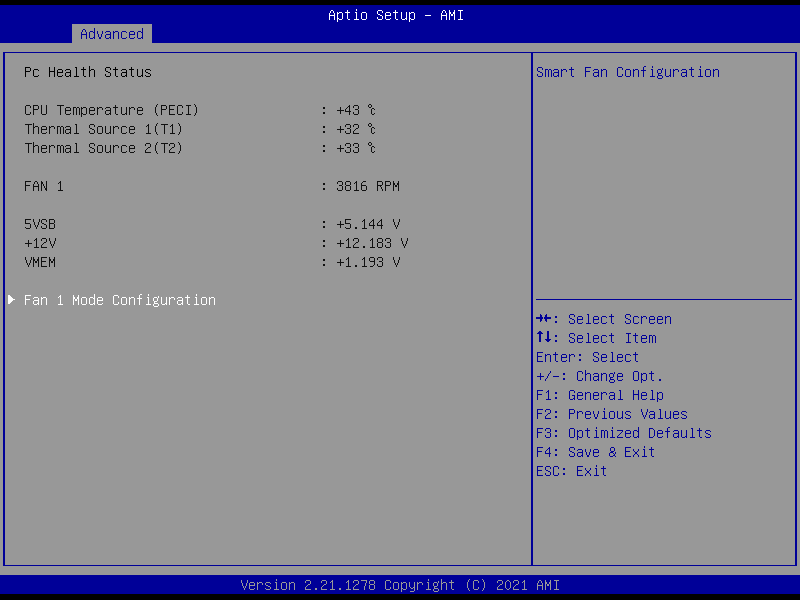
| **Options Summary** | | |
| --- | --- | --- |
| **Active Processor Cores** | All | Optimal Default, Failsafe Default |
| 1 |  |
| 2 |  |
| 3 |  |
| Number of cores to enable in each processor package. | | |
| **Turbo Mode** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled. | | |
| **Hyper-Threading** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Hyper-Threading Technology. | | |
| **Intel(R) SpeedStep(tm)** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Allows more than two frequency ranges to be supported. | | |
| **Intel (VMX) Virtualization Technology** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. | | |

### 3.4.3 Memory Configuration



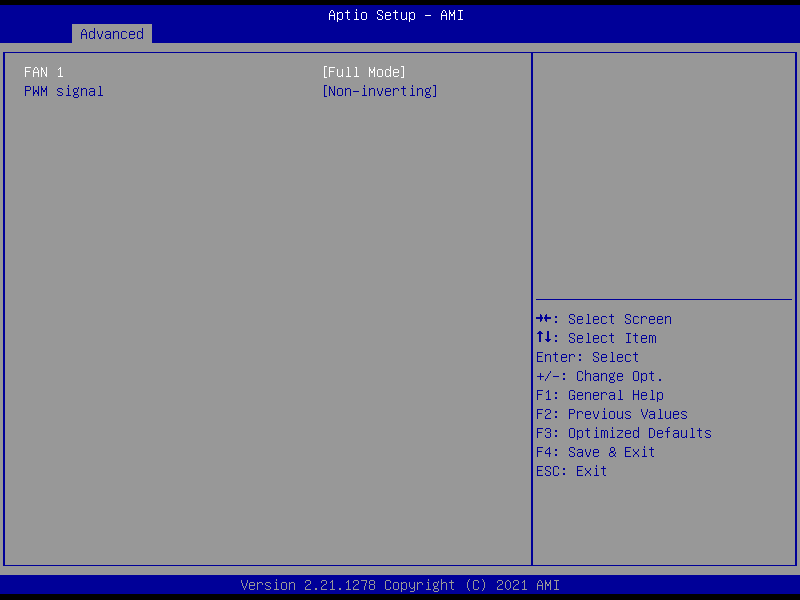
| **Options Summary** | | |
| --- | --- | --- |
| **In-Band ECC Support** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable/Disable In-Band ECC. Either the IBECC or the TME can be enabled. | | |
| **In-Band ECC Error Injection** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions. | | |
| **In-Band ECC Error Operation Mode** | 0 |  |
| 1 |  |
| 2 | Optimal Default, Failsafe Default |
| 0: Functional Mode protects requests based on the address range.  1: Makes all requests non-protected and ignore range checks. 2: Makes all requests protected and ignore range checks. | | |

### 3.4.4 On-Module H/W Monitor

****

#### 3.4.4.1 Smart Fan Mode Configuration

**FAN 1: Full Mode**



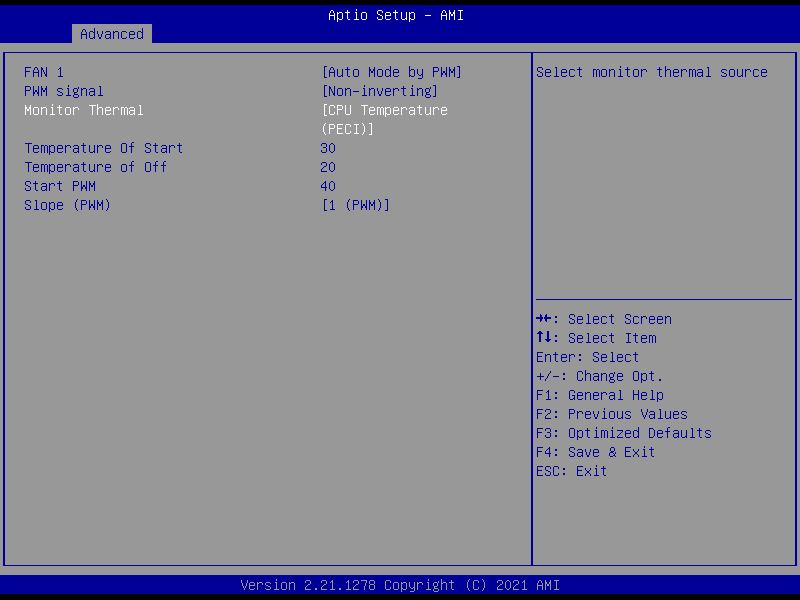
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **FAN 1** | Full Mode | Optimal Default, Failsafe Default |
| Manual Mode by PWM |  |
| Auto Mode by PWM |  |
| Smart Fan Mode Select. | | |
| **PWM signal** | Non-inverting | Optimal Default, Failsafe Default |
| Inverting |  |
| Select output PWM of inverting or non-inverting signal. | | |

**FAN 1: Manual Mode by PWM**



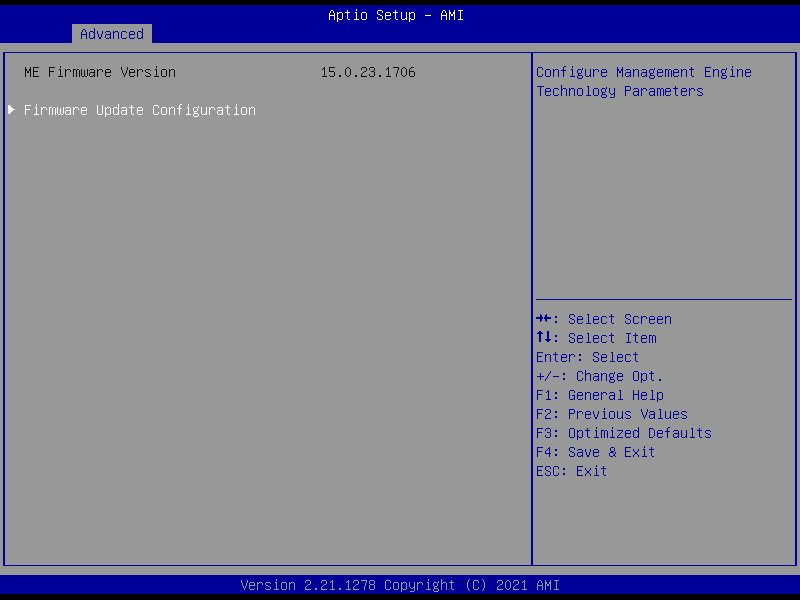
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Manual Setting** | 70 | Optimal Default, Failsafe Default |
| Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number: | | |

**FAN 1: Auto Mode by PWM**

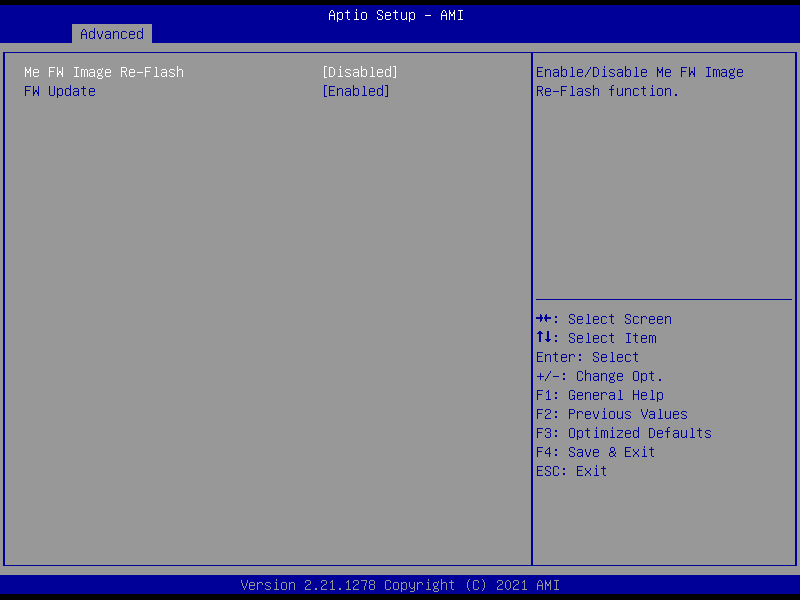


| **Options Summary** | | |
| --- | --- | --- |
| **Monitor Thermal** | CPU Temperature (PECI) | Optimal Default, Failsafe Default |
| Thermal Source 1(T1) |  |
| Thermal Source 2(T2) |  |
| Select monitor thermal source. | | |
| **Temperature of Start** | 30 | Optimal Default, Failsafe Default |
| Temperature of Start. | | |
| **Temperature of Off** | 20 | Optimal Default, Failsafe Default |
| Temperature of Off. | | |
| **Start PWM** | 40 | Optimal Default, Failsafe Default |
| Start PWM | | |
| **Slope (PWM)** | 0 (PWM) |  |
| 1 (PWM) | Optimal Default, Failsafe Default |
| 2 (PWM) |  |
| 4 (PWM) |  |
| 8 (PWM) |  |
| 16 (PWM) |  |
| 32 (PWM) |  |
| 64 (PWM) |  |
| Slope (PWM) | | |

### 3.4.5 PCH-FW Configuration

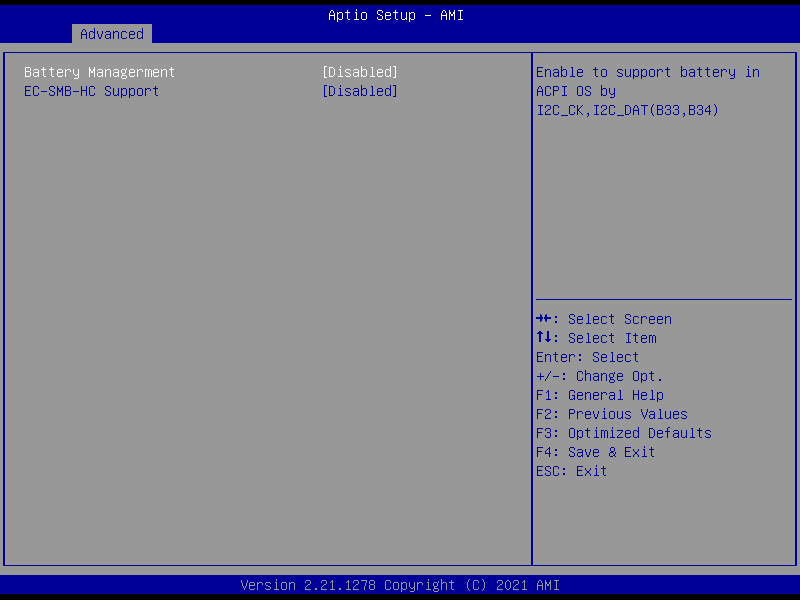
****

#### 3.4.6.1 Firmware Update Configuration

****

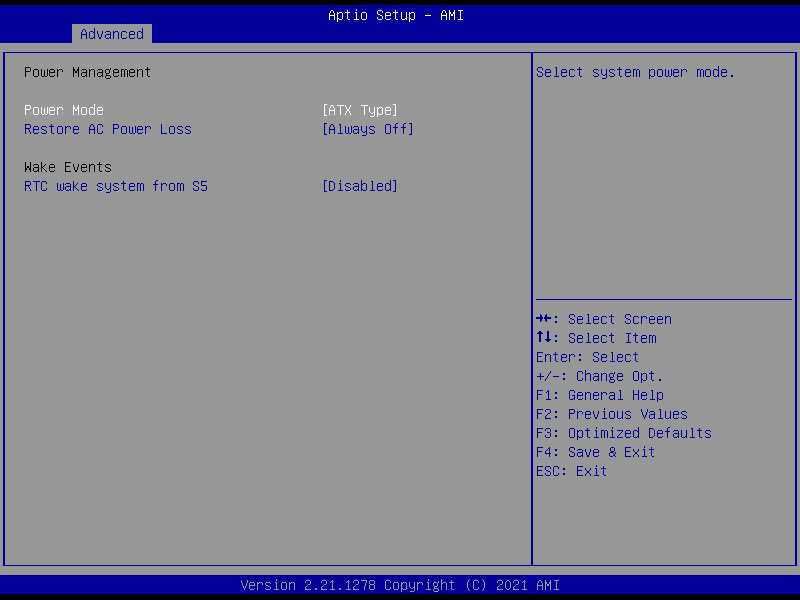
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Me FW Image Re-Flash** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enable/ Disable Me FW Image Re-Flash Function. | | |
| **FW Update** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable/Disable ME FW Update Function | | |

### 3.4.6 On-Module Configuration



|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Battery Management** | Disabled | Optimal Default, Failsafe Default |
| One Battery |  |
| Enable to support battery in ACPI OS by I2C\_CK, I2C\_DAT (B33, B34). | | |
| **EC-SMB-HC Support** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| SMBus Host Controller Interface via Embedded Controller. | | |

### 3.4.7 Power Management

****

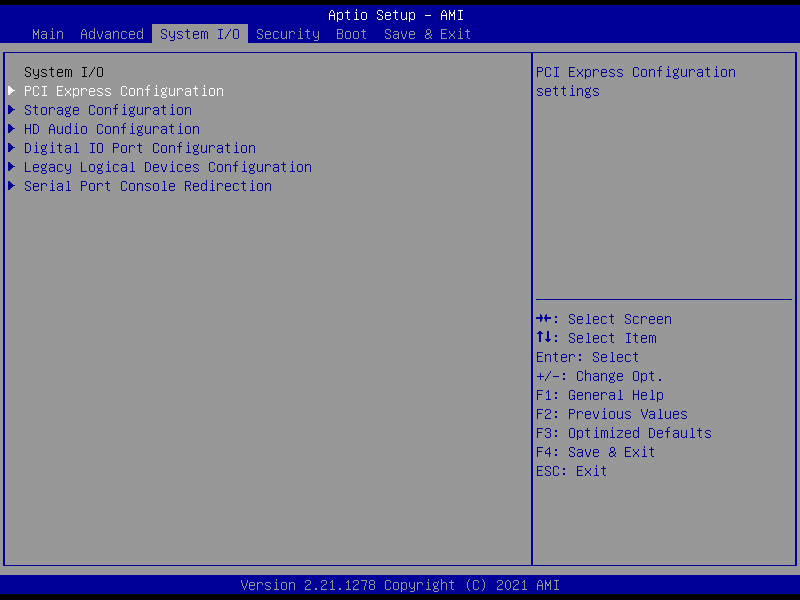
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Power Mode** | ATX Type | Optimal Default, Failsafe Default |
| AT Type |  |
| Select system power mode. | | |
| **Restore AC Power Loss** | Last State |  |
| Always On |  |
| Always Off | Optimal Default, Failsafe Default |
| SIO Restore AC Power Loss: To decide the behavior after system power cut then resupply. **Note:** The CMOS battery must be present. | | |
| **RTC wake system from S5** | Disabled | Optimal Default, Failsafe Default |
| Fixed Time |  |
| Dynamic Time |  |
| Bypass |  |
| Fixed Time: System will wake on the hr::mn::sec Specified.  Dynamic Time: System will wake on the current time + Increase minute(s).  Bypass: BIOS will not control RTC wake function during system shutdown. | | |

### 3.4.8 AAEON BIOS Robot

****

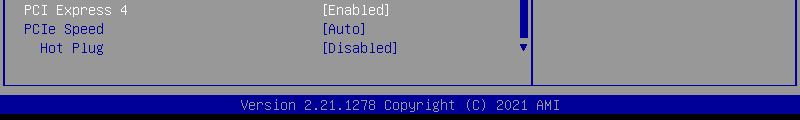
| **Options Summary** | | |
| --- | --- | --- |
| **Sends watch dog before BIOS POST** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enabled - Robot set Watch Dog Timer (WDT) right after power on, before BIOS start POST process. And then Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero. | | |
| **Sends watch dog before booting OS** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enabled - Robot set Watch Dog Timer (WDT) after POST completion before BIOS transfer control to OS. **Warning**: Before enabling this function, a program in OS must be in responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself. | | |
| **Delayed POST (PEI phase)** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this before 'Send watch dog'. | | |
| **Delayed POST**  **(DXE phase)** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. **Note**: Robot does this after 'Send watch dog before BIOS POST'. | | |
| **Reset system once** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enabled - Robot resets system for one time on each boot. This will send a soft or hand reset to onboard devices, thus puts devices to more stable state. | | |

## 3.5 Setup Submenu: System I/O



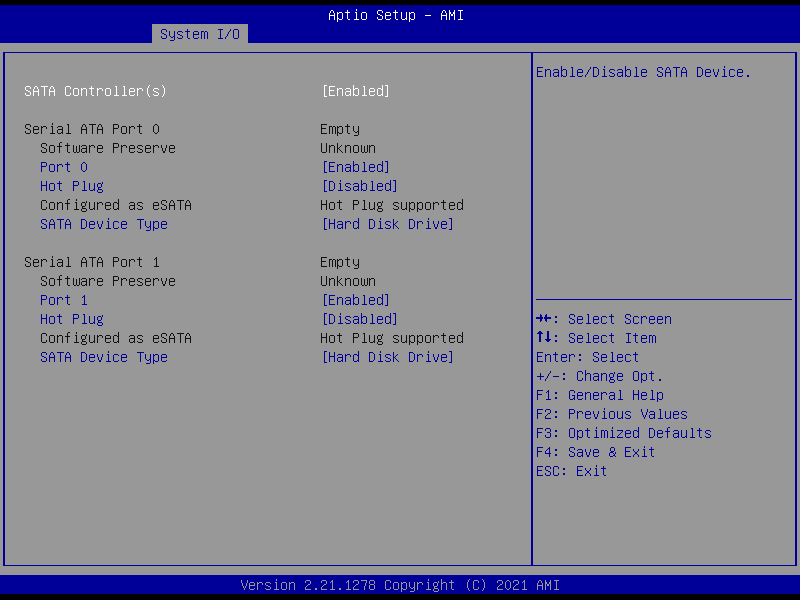
### 3.5.1 PCI Express Configuration





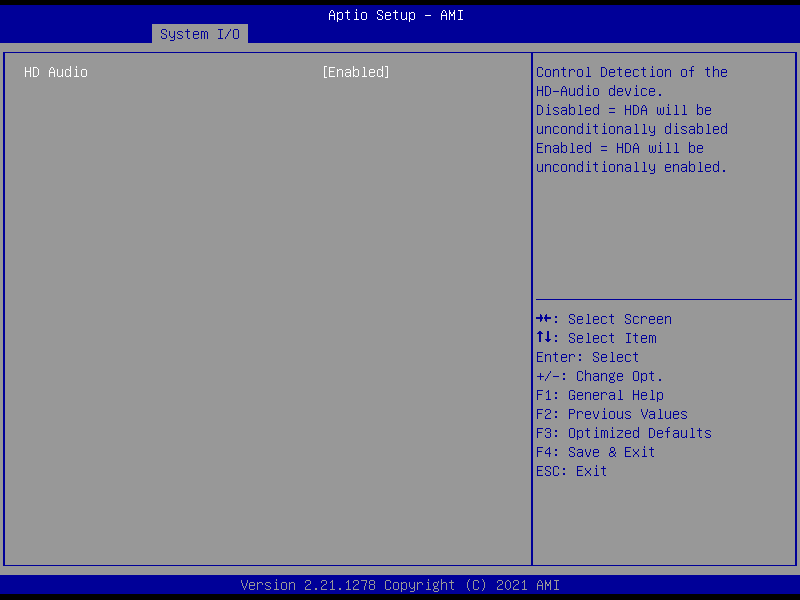
| **Options Summary** | | |
| --- | --- | --- |
| **PCI Express Root Port 1** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Gen4 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |
| **PCIe 0\_3 Select** | PCIE Controller are four 1 | Optimal Default, Failsafe Default |
| PCIE Controller are one 2 and two 1 |  |
| PCIE Controller are two 2 |  |
| PCIE Controller is one 4 |  |
| PCIE Controller Selection. | | |
| **PCI Express 0** | Disable |  |
| Enable | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |
| **PCI Express 1** | Disable |  |
| Enable | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |
| **PCI Express 2** | Disable |  |
| Enable | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed**  **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |
| **PCI Express 3** | Disable |  |
| Enable | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |
| **PCI Express 4** | Disable |  |
| Enable | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| **PCIe Speed** | Auto | Optimal Default, Failsafe Default |
| Gen1 |  |
| Gen2 |  |
| Gen3 |  |
| Configure PCIe Speed. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| PCI Express Hot Plug Enable/Disable. | | |

### 3.5.2 Storage Configuration



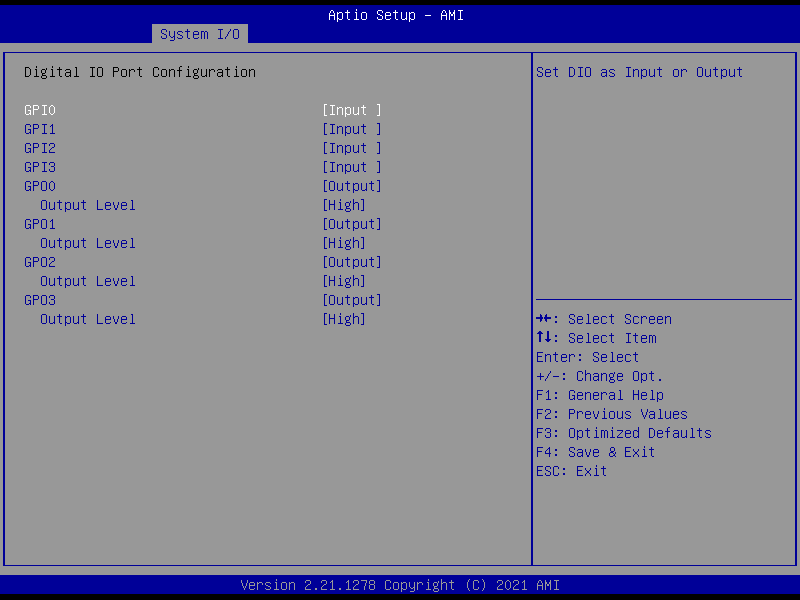
| **Options Summary** | | |
| --- | --- | --- |
| **SATA Controller(s)** | Enabled | Optimal Default, Failsafe Default |
| Disabled |  |
| Enable/Disable SATA Device. | | |
| **Port 0** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable SATA Port. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Designates this port as Hot Pluggable. | | |
| **SATA Device Type** | Hard Disk Drive | Optimal Default, Failsafe Default |
| Solid State Drive |  |
| Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. | | |
| **Port 1** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable SATA Port. | | |
| **Hot Plug** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Designates this port as Hot Pluggable. | | |
| **SATA Device Type** | Hard Disk Drive | Optimal Default, Failsafe Default |
| Solid State Drive |  |
| Identify the SATA port is connected to Solid State Drive or Hard Disk Drive. | | |

### 3.5.3 HD Audio Configuration

****

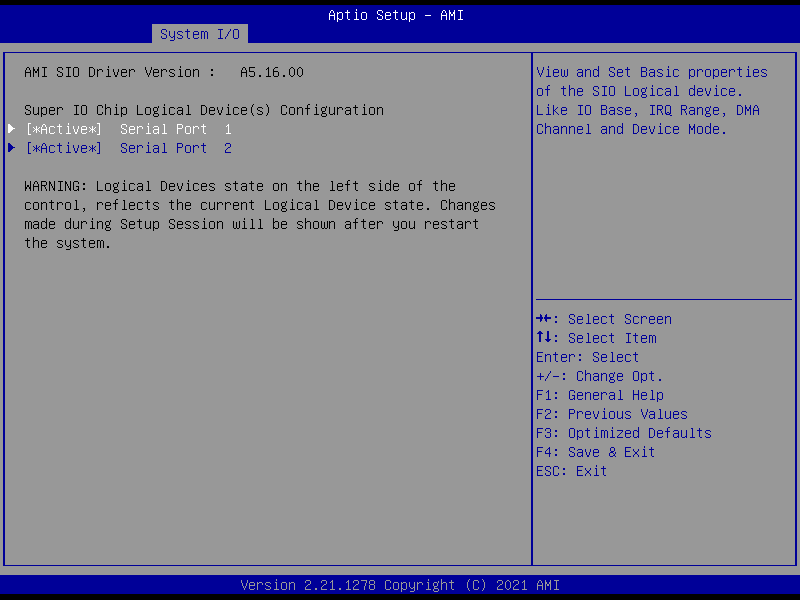
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **HD Audio** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Control Detection of the HD-Audio device.  Disabled = HDA will be unconditionally disabled.  Enabled = HDA will be unconditionally enabled. | | |

### 3.5.4 Digital IO Port Configuration

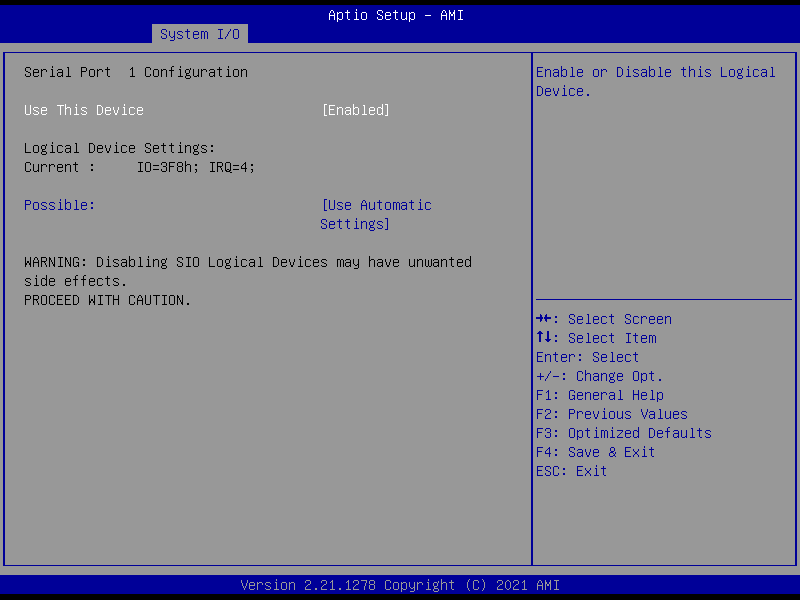


| **Options Summary** | | |
| --- | --- | --- |
| **GPI\*** | Input | Optimal Default, Failsafe Default |
| Output |  |
| Set DIO as Input or Output. | | |
| **GPO\*** | Input |  |
| Output | Optimal Default, Failsafe Default |
| Set DIO as Input or Output. | | |
| **Output Level** | Low |  |
| High | Optimal Default, Failsafe Default |
| Set output level when DIO pin is output. | | |

### 3.5.5 Legacy Logical Devices Configuration

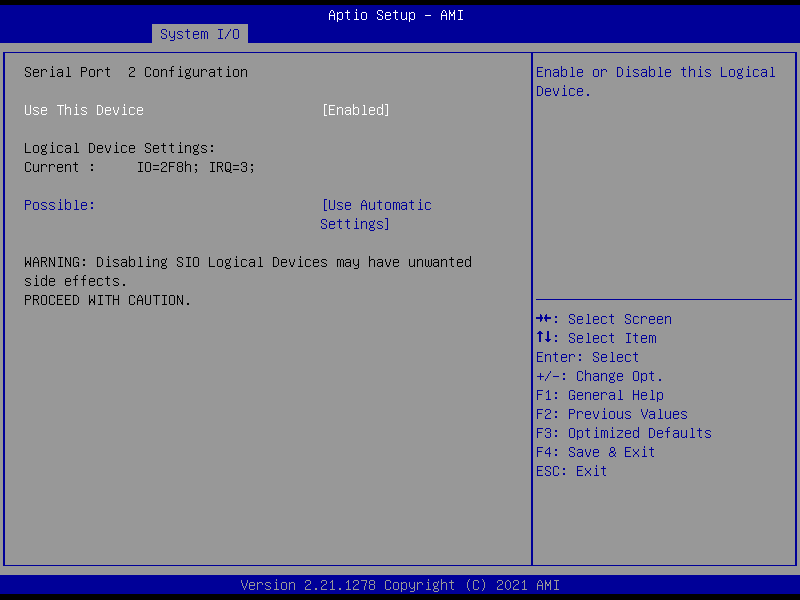


#### 3.5.5.1 Serial Port 1 Configuration



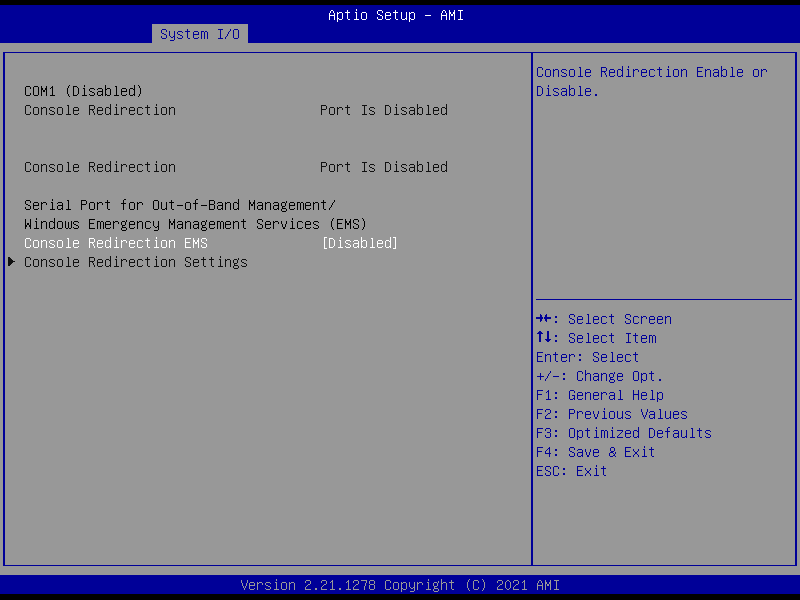
| **Options Summary** | | |
| --- | --- | --- |
| **Use This Device** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable this Logical Device. | | |
| **Possible:** | Use Automatic Settings | Optimal Default, Failsafe Default |
| IO=3F8h; IRQ=4; DMA; |  |
| IO=2C8h; IRQ=11; DMA; |  |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |

#### 3.5.5.2 Serial Port 2 Configuration



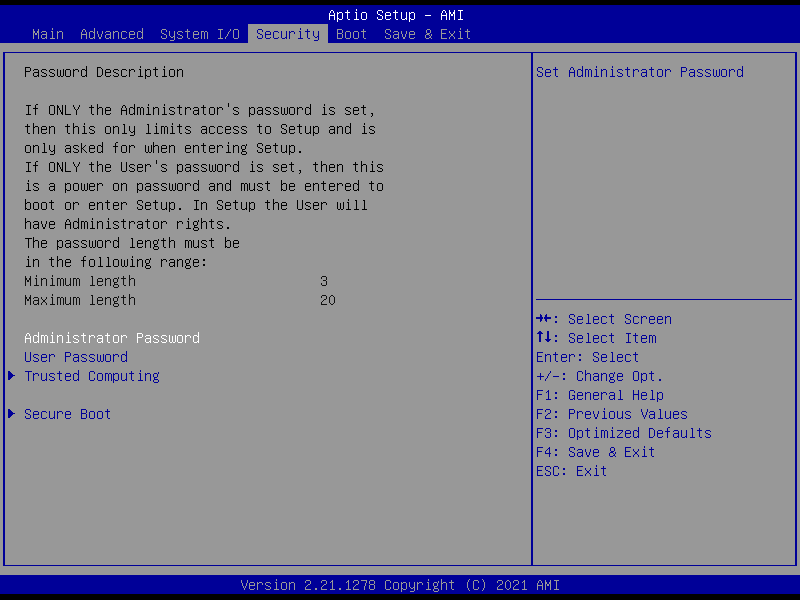
| **Options Summary** | | |
| --- | --- | --- |
| **Use This Device** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable this Logical Device. | | |
| **Possible:** | Use Automatic Settings | Optimal Default, Failsafe Default |
| IO=2F8h; IRQ=3 DMA; |  |
| IO=2D8h; IRQ=10; DMA; |  |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |

### 3.5.6 Serial Port Console Redirection



| **Options Summary** | | |
| --- | --- | --- |
| **Console Redirection EMS** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Console Redirection Enable or Disable. | | |

## 3.6 Setup Submenu: Security



**Change Administrator/User Password**

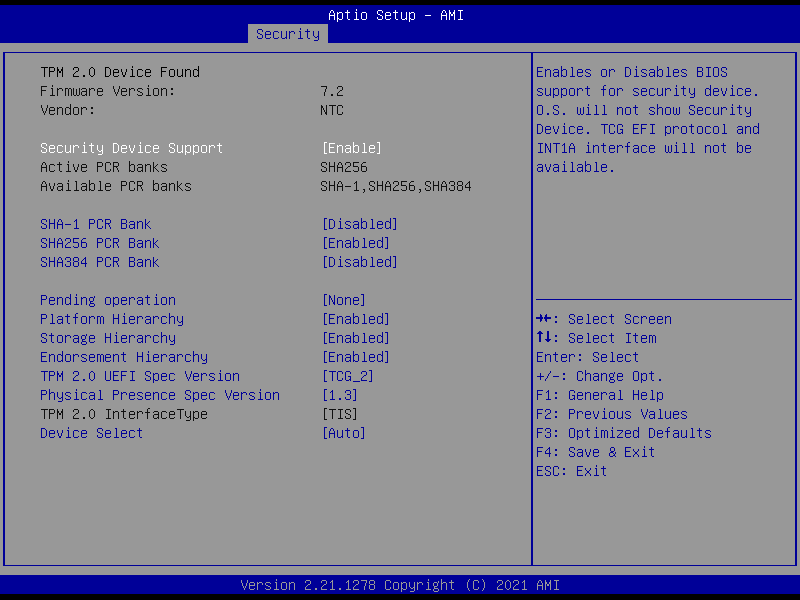
You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility.

Select the password you want to set and press <Enter>. A dialog box will appear which lets you set the password. Passwords must be between 3 and 20 letters or numbers. Press <Enter> and re-enter the password into the next dialog box that appears. Press <Enter> after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

**Remove Password**

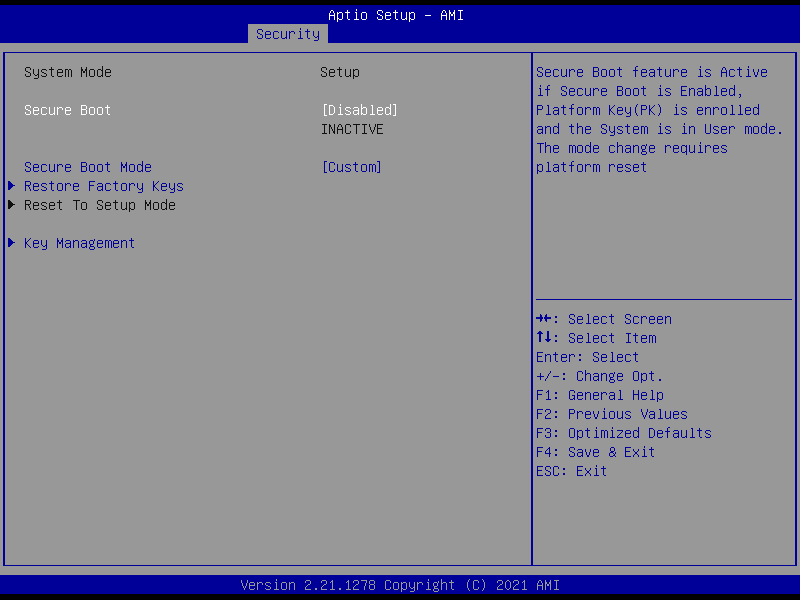
Highlight this item and type in the current password. At the next dialog box press <Enter> to disable password protection.

### 3.6.1 Trusted Computing



| **Options Summary** | | |
| --- | --- | --- |
| **Security Device Support** | Disable | Optimal Default, Failsafe Default |
| Enable |  |
| Enables or Disables BIOS support for security device. O.S. will not show Security Device.  TGU EFI protocol and INT1A interface will not be available. | | |
| **SHA-1 PCR Bank** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enable or Disable SHA-1 PCR Bank. | | |
| **SHA256 PCR Bank** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable SHA256 PCR Bank. | | |
| **SHA384 PCR Bank** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Enable or Disable SHA384 PCR Bank. | | |
| **Pending operation** | None | Optimal Default, Failsafe Default |
| TPM Clear |  |
| Schedule an Operation for the Security Device. Note: Your Computer will reboot during restart in order to change State of Security Device. | | |
| **Platform Hierarchy** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Platform Hierarchy. | | |
| **Storage Hierarchy** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Storage Hierarchy. | | |
| **Endorsement Hierarchy** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Endorsement Hierarchy. | | |
| **TPM 2.0 UEFI Spec Version** | TCG\_1\_2 |  |
| TCG\_2 | Optimal Default, Failsafe Default |
| Select the TCG2 Spec Version Support. TCG\_1\_2: The Compatible mode for Win8/Win10. TCG\_2: Support new TCG2 protocol and event format for win10 or later. | | |
| **Physical Presence Spec Version** | 1.2 |  |
| 1.3 | Optimal Default, Failsafe Default |
| Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3. | | |
| **Device Select** | TPM 1.2 |  |
| TPM 2.0 |  |
| Auto | Optimal Default, Failsafe Default |
| TPM 1.2 will restrict support to TPM 1.2 devices.  TPM 2.0 will restrict support to TPM 2.0 devices.  Auto will support both with the default set to TPM 2.0 devices if not found.  TPM 1.2 devices will be enumerated. | | |

### 3.6.2 Secure Boot



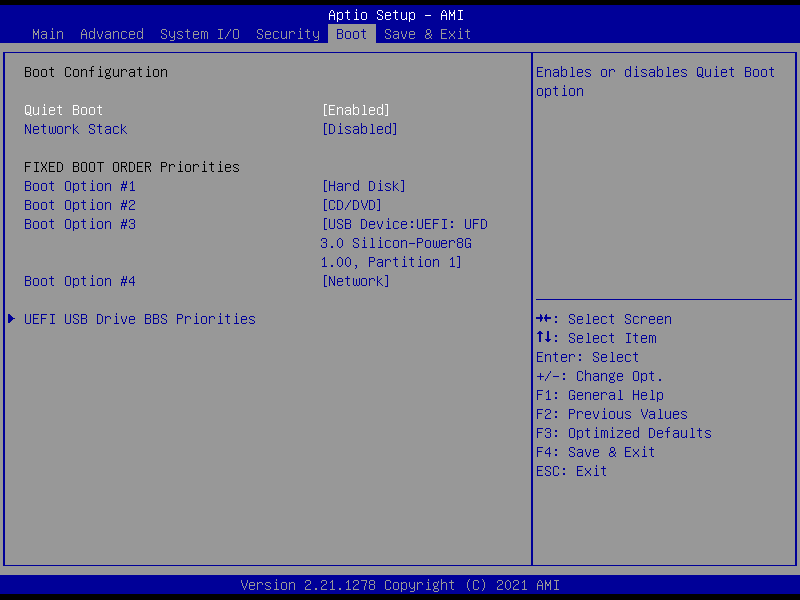
|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Secure Boot** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. | | |
| **Secure Boot Mode** | Standard |  |
| Custom | Optimal Default, Failsafe Default |
| Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. | | |

#### 3.6.2.1 Key Management



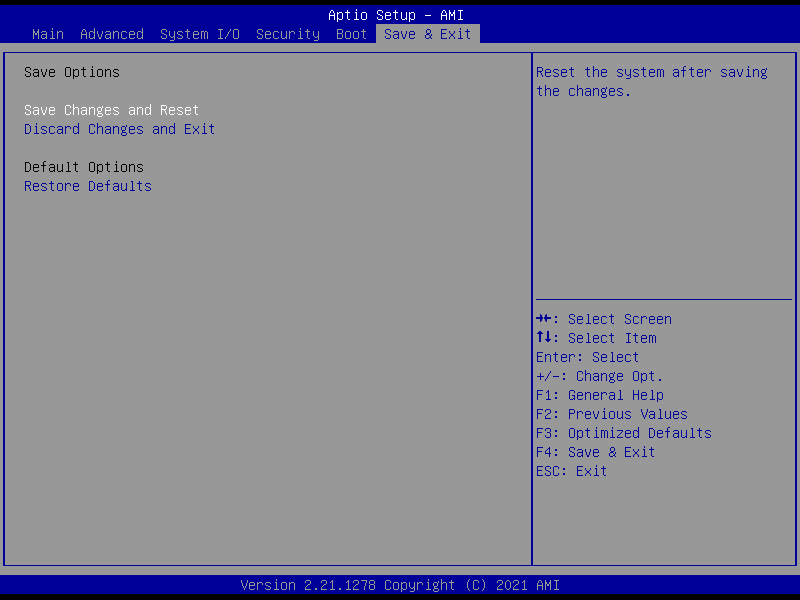
| **Options Summary** | | |
| --- | --- | --- |
| **Factory Key Provision** | Disabled | Optimal Default, Failsafe Default |
| Enabled |  |
| Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. | | |

## 3.7 Setup Submenu: Boot



|  |  |  |
| --- | --- | --- |
| **Options Summary** | | |
| **Quiet Boot** | Disabled |  |
| Enabled | Optimal Default, Failsafe Default |
| Enables or Disables Quite Boot option. | | |
| **Network Stack** | Disabled | Optimal Default, Failsafe Default |
| UEFI |  |
| Enable/Disable UEFI Network Stack. | | |

## 3.8 Setup Submenu: Save & Exit



**Chapter 4**

# Chapter 4 – Drivers Installation

## 4.1 Drivers Download and Installation

Drivers for the COM-TGUC6 can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/>

Download the driver(s) you need and follow the steps below to install them.

**Audio Driver (Windows 10)**

1. Open thefolder where you unzipped the **Audio Drivers**
2. Run the **Setup.exe** in the folder
3. Follow the instructions
4. Drivers will be installed automatically

**Chipset Driver (Windows 10)**

1. Open thefolder where you unzipped the **Chipset Drivers**
2. Run the**SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

**Graphics Driver (Windows 10)**

1. Open thefolder where you unzipped the **Graphics Drivers**
2. Run the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

**LAN Drivers (Windows 10)**

1. Open thefolder where you unzipped the **LAN Drivers**
2. Read the ReadMe.txt file before proceeding. **Caution:** Be sure to install the driver package before installing the Intel® PROSet package.
3. Open the **Wired\_driver\_26.3\_x64** folder
4. Run the **Wired\_driver\_26.3\_x64.exe** file in the folder
5. Follow the instructions, drivers will be installed automatically.
6. After installing the LAN driver, install Intel® PROSet package (optional)
7. Open the **Wired\_PROSet\_26.3\_x64** folder
8. Run the **Wired\_PROSet\_26.3\_x64.exe** file in the folder
9. Follow the instructions
10. Drivers will be installed automatically

**Intel® Active Management Technology Drivers (Windows 10)**

1. Open thefolder where you unzipped the **Intel AMT Drivers**
2. Drivers must be installed manually, refer to Windows guidance to complete steps.

**Intel® Management Engine Interface Drivers (Windows 10)**

1. Open thefolder where you unzipped the **Intel MEI Drivers**
2. Drivers must be installed manually, refer to Windows guidance to complete steps.

**Peripheral Driver (Linux)**

1. Open thefolder where you unzipped the **Peripheral Drivers**
2. Follow the instructions contained within the user guides to install the related drivers.

**Appendix A**

# Appendix A - Watchdog Timer

## A.1 Watchdog Timer Initial Program

|  |  |  |
| --- | --- | --- |
| **Table 1: Embedded BRAM Relative Register Table** | | |
|  | **Default Value** | **Note** |
| **Index** | **0x284(Note1)** | BRAM Index Register |
| **Data** | **0x285(Note2)** | BRAM Data Register |
| **Logical Device Number** | **0xA8(Note3)** | Watch dog Logical Device Number |
| **Function and Device Number** | **0x00(Note4)** | Watch dog Function/Device Number |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Table 2: Watchdog Relative Register Table** | | | | |
|  | **Option Register** | **BitNum** | **Value** | **Note** |
| **Timer Counter** | **0x00**(Note5) |  | (Note10) | Time of watchdog timer  (0~255) |
| **Counting Unit** | **0x01**(Note6) | **0**(Note7) | **0**(Note11) | Select time unit.  0: second  1: minute |
| **Watchdog RST pulse width** | **0x01**(Note8) | **[3:2]**(Note9) | **0**(Note12) | 0: 20ms  1: 60ms  2: 100ms  3: 250ms |

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Embedded BRAM relative definition (Please reference to Table 1)

**#define byte** EcBRAMIndex //This parameter is represented from **Note1**

**#define byte** EcBRAMData //This parameter is represented from **Note2**

**#define byte** BRAMLDNReg //This parameter is represented from **Note3**

**#define byte** BRAMFnDataReg //This parameter is represented from **Note4**

**#define** **void** EcBRAMWriteByte(**byte** Offset, **byte** Value);

**#define byte** EcBRAMReadByte(**byte** Offset);

**#define** **void** IOWriteByte(**byte** Offset, **byte** Value);

**#define byte** IOReadByte(**byte** Offset);

// Watch Dog relative definition (Please reference to Table 2)

**#define byte** TimerReg //This parameter is represented from **Note5**

**#define byte** TimerVal // This parameter is represented from **Note10**

**#define byte** UnitReg //This parameter is represented from **Note6**

**#define byte** UnitBit //This parameter is represented from **Note7**

**#define byte** UnitVal //This parameter is represented from **Note11**

**#define byte** RSTReg //This parameter is represented from **Note8**

**#define byte** RSTBit //This parameter is represented from **Note9**

**#define byte** RSTVal //This parameter is represented from **Note12**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

VOID **Main**(){

// Procedure : AaeonWDTConfig

// (byte)Timer : Time of WDT timer.(0x00~0xFF)

// (boolean)Unit : Select time unit(0: second, 1: minute).

AaeonWDTConfig();

// Procedure : AaeonWDTEnable

// This procudure will enable the WDT counting.

AaeonWDTEnable();

}

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Procedure : AaeonWDTEnable

VOID **AaeonWDTEnable ()**{

WDTEnableDisable(**1**);

}

// Procedure : AaeonWDTConfig

VOID **AaeonWDTConfig ()**{

// Disable WDT counting

WDTEnableDisable(**0**);

// WDT relative parameter setting

WDTParameterSetting();

}

VOID **WDTEnableDisable(byte Value)**{

ECBRAMWriteByte(TimerReg , Value);

}

VOID **WDTParameterSetting()**{

Byte TempByte;

// Watchdog Timer counter setting

ECBRAMWriteByte(TimerReg , TimerVal);

// WDT counting unit setting

TempByte = ECBRAMReadByte(UnitReg);

TempByte |= (UnitVal << UnitBit);

ECBRAMWriteByte(UnitReg , TempByte);

// WDT RST pulse width setting

TempByte = ECBRAMReadByte(RSTReg);

TempByte |= (RSTVal << RSTBit);

ECBRAMWriteByte(RSTReg , TempByte);

}

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

VOID **ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value)**{

IOWriteByte(EcBRAMIndex, 0x10);

IOWriteByte(EcBRAMData, BRAMLDNReg);

IOWriteByte(EcBRAMIndex, 0x11);

IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);

IOWriteByte(EcBRAMData, Value);

IOWriteByte(EcBRAMIndex, 0x12);

IOWriteByte(EcBRAMData, 0x30); //Write start

}

Byte **ECBRAMReadByte(byte OPReg)**{

IOWriteByte(EcBRAMIndex, 0x10);

IOWriteByte(EcBRAMData, BRAMLDNReg);

IOWriteByte(EcBRAMIndex, 0x11);

IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x12);

IOWriteByte(EcBRAMData, 0x10); //Read start

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);

Return IOReadByte(EcBRAMData, Value);

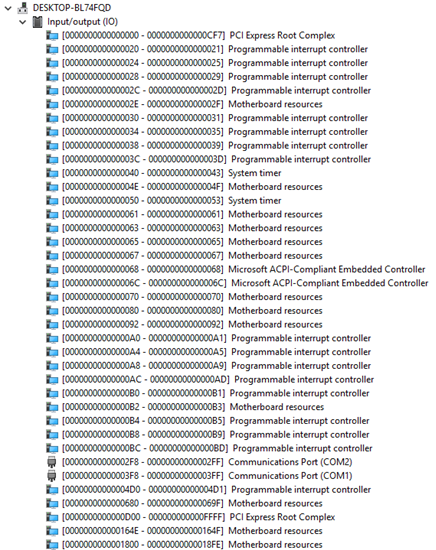
}

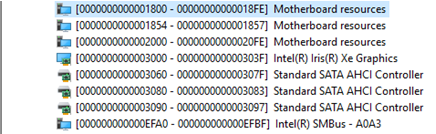
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

**Appendix B**

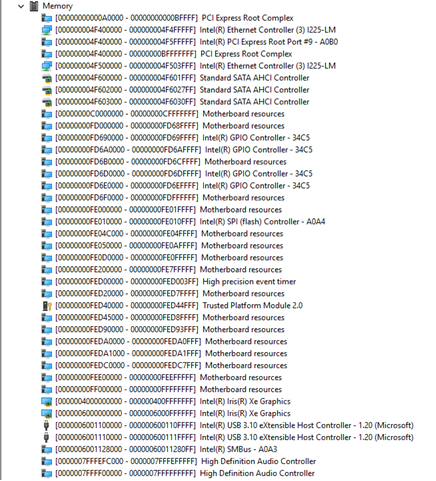
# Appendix B - I/O Information

## B.1 I/O Address Map





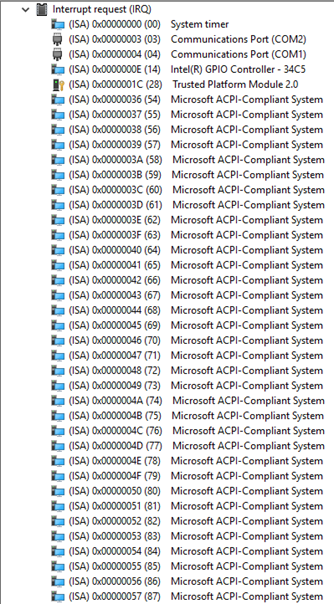
## B.2 Memory Address Map

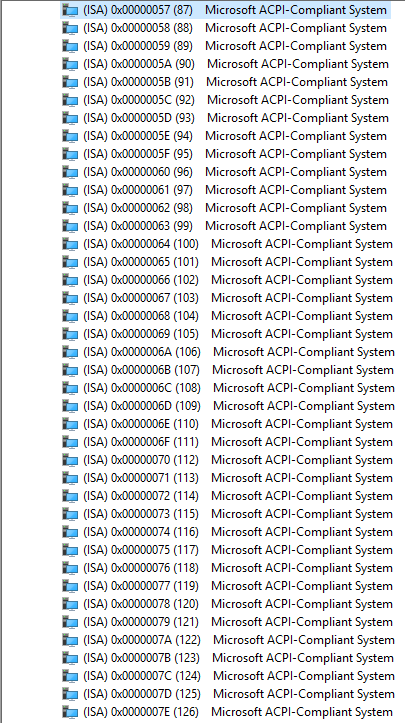


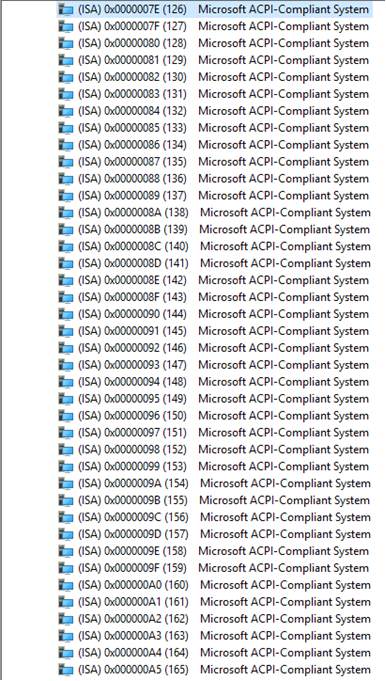
## B.3 Large Memory Address Map

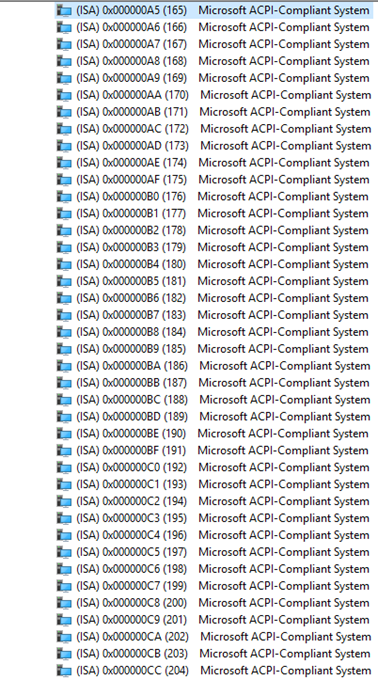


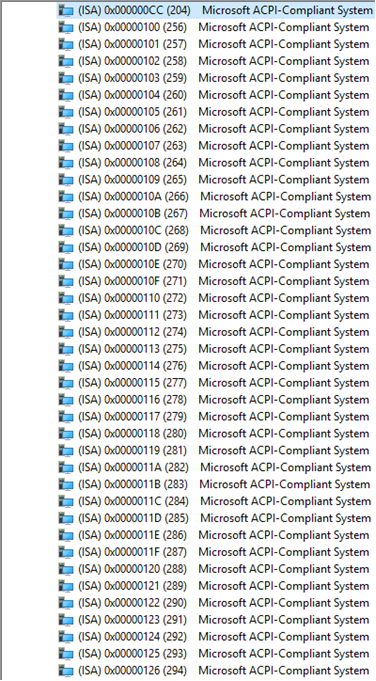
## B.4 IRQ Mapping Chart

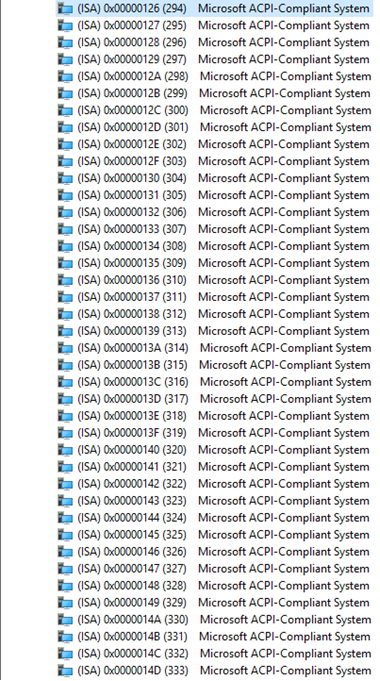


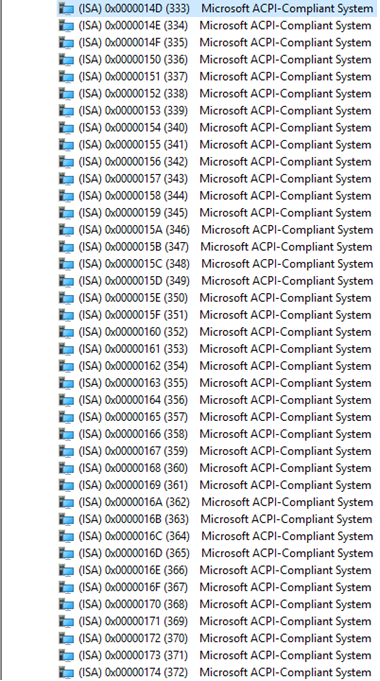


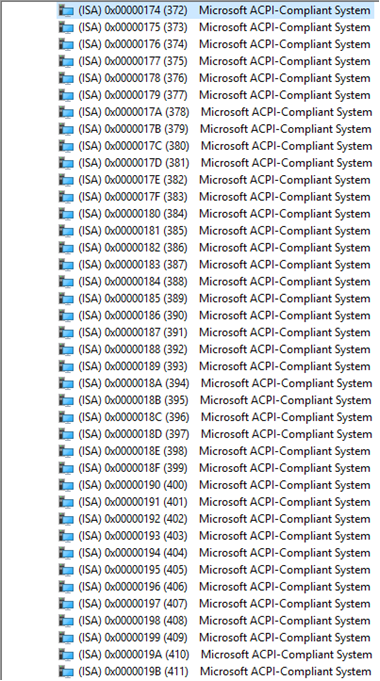


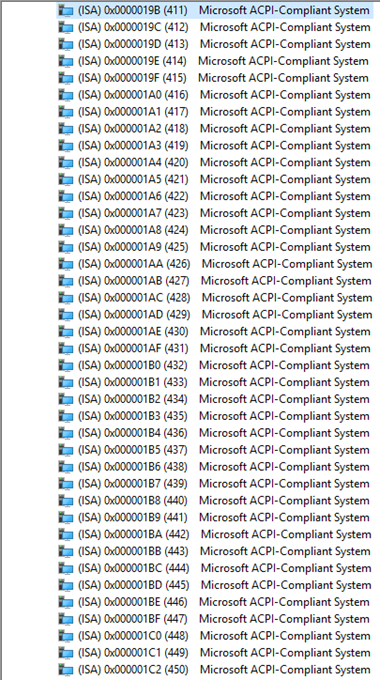


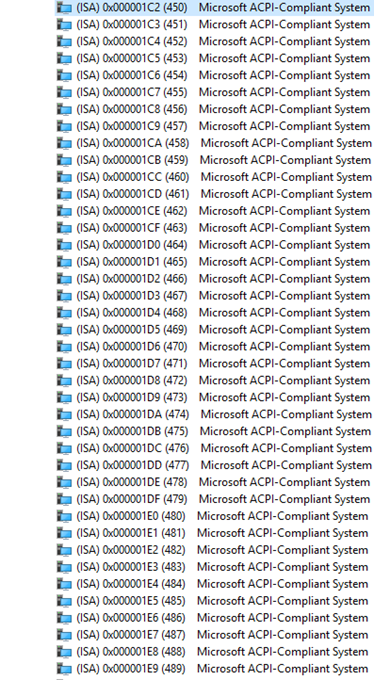


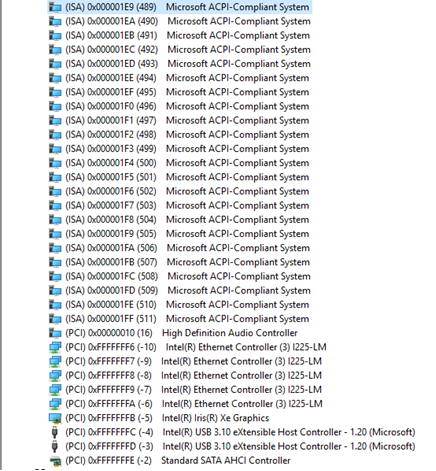












**Appendix C**

# Appendix C – Programming Digital I/O

## C.1 Digital I/O Programming

The COM-TGUC6 C10 utilizes an AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration, which you can use to develop a customized program to fit your application.

## C.2 Digital I/O Register

|  |  |  |
| --- | --- | --- |
| **Table 1: Embedded BRAM Relative Register Table** | | |
|  | **Default Value** | **Note** |
| **Index** | **0x284**(Note1) | BRAM Index Register |
| **Data** | **0x285**(Note2) | BRAM Data Register |
| **Logical Device Number** | **0xA2**(Note3) | Watchdog Logical Device Number |
| **IO Direction**  **Function and Device Number** | **0x00**(Note4) | DIO Input/ Output Function/Device Number |
| **IO Vaule/Status**  **Function and Device Number** | **0x01**(Note5) | DIO Output Data Function/Device Number |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Table 2: Digital I/O Relative Register Table** | | | | |
|  | **Register** | | | |
|  | **Option Register** | **BitNum** | **Value** | **Note** |
| **GPI0 Pin Status** | **0x00**(Note6) | **0**(Note7) | (Note15) | GPA2 |
| **GPI1 Pin Status** | **0x00**(Note6) | **1**(Note8) | (Note16) | GPA3 |
| **GPI2 Pin Status** | **0x00**(Note6) | **2**(Note9) | (Note17) | GPA4 |
| **GPI3 Pin Status** | **0x00**(Note6) | **3**(Note10) | (Note18) | GPA5 |
| **GPO0 Pin Status** | **0x00**(Note6) | **4**(Note11) | (Note19) | GPJ0 |
| **GPO1 Pin Status** | **0x00**(Note6) | **5**(Note12) | (Note20) | GPJ1 |
| **GPO2 Pin Status** | **0x00**(Note6) | **6**(Note13) | (Note21) | GPJ2 |
| **GPO3 Pin Status** | **0x00**(Note6) | **7**(Note14) | (Note22) | GPJ3 |

## C.3 Digital I/O Sample Program

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Embedded BRAM relative definition (Please reference to Table 1)

**#define byte** EcBRAMIndex //This parameter is represented from **Note1**

**#define byte** EcBRAMData //This parameter is represented from **Note2**

**#define byte** BRAMLDNReg //This parameter is represented from **Note3**

**#define byte** BRAMFnData0Reg //This parameter is represented from **Note4**

**#define byte** BRAMFnData1Reg //This parameter is represented from **Note5**

**#define** **void** EcBRAMWriteByte(**byte** Offset, **byte** Value);

**#define byte** EcBRAMReadByte(**byte** Offset);

**#define** **void** IOWriteByte(**byte** Offset, **byte** Value);

**#define byte** IOReadByte(**byte** Offset);

// Digital Input Status relative definition (Please reference to Table 2)

**#define byte** DIO0ToDIO7Reg // This parameter is represented from **Note6**

**#define byte** DIO0Bit // This parameter is represented from **Note7**

**#define byte** DIO1Bit // This parameter is represented from **Note8**

**#define byte** DIO2Bit // This parameter is represented from **Note9**

**#define byte** DIO3Bit // This parameter is represented from **Note10**

**#define byte** DIO4Bit // This parameter is represented from **Note11**

**#define byte** DIO5Bit // This parameter is represented from **Note12**

**#define byte** DIO6Bit // This parameter is represented from **Note13**

**#define byte** DIO7Bit // This parameter is represented from **Note14**

**#define byte** DIO0Val // This parameter is represented from **Note15**

**#define byte** DIO1Val // This parameter is represented from **Note16**

**#define byte** DIO2Val // This parameter is represented from **Note17**

**#define byte** DIO3Val // This parameter is represented from **Note18**

**#define byte** DIO4Val // This parameter is represented from **Note19**

**#define byte** DIO5Val // This parameter is represented from **Note20**

**#define byte** DIO6Val // This parameter is represented from **Note21**

**#define byte** DIO7Val // This parameter is represented from **Note22**

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VOID **Main**(){

Boolean PinStatus ;

// Procedure : AaeonReadPinStatus

// Input :

// Example, Read Digital I/O Pin 3 status

// Output :

// InputStatus :

// 0: Digital I/O Pin level is low

// 1: Digital I/O Pin level is High

PinStatus = AaeonReadPinStatus(**DIO0ToDIO7Reg, DIO3Bit**);

// Procedure : AaeonSetOutputLevel

// Input :

// Example, Set Digital I/O Pin 6 level

AaeonSetOutputLevel(**DIO0ToDIO7Reg, DIO6Bit, DIO6Val**);

}

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Boolean **AaeonReadPinStatus(byte OptionReg, byte BitNum)**{

Byte TempByte;

TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);

If (TempByte & BitNum == 0)

Return 0;

Return 1;

}

VOID **AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value)**{

Byte TempByte;

TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);

TempByte |= (Value << BitNum);

ECBRAMWriteByte(OptionReg, BitNum, Value);

}

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VOID **ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value)**{

IOWriteByte(EcBRAMIndex, 0x10);

IOWriteByte(EcBRAMData, BRAMLDNReg);

IOWriteByte(EcBRAMIndex, 0x11);

IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);

IOWriteByte(EcBRAMData, Value);

IOWriteByte(EcBRAMIndex, 0x12);

IOWriteByte(EcBRAMData, 0x30); //Write start

}

Byte **ECBRAMReadByte(byte FnDataReg, byte OPReg)**{

IOWriteByte(EcBRAMIndex, 0x10);

IOWriteByte(EcBRAMData, BRAMLDNReg);

IOWriteByte(EcBRAMIndex, 0x11);

IOWriteByte(EcBRAMData, FnDataReg);

IOWriteByte(EcBRAMIndex, 0x12);

IOWriteByte(EcBRAMData, 0x10); //Read start

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);

Return IOReadByte(EcBRAMData, Value);

}

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