

# VPC-5600S

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Mobile NVR

User's Manual 3<sup>rd</sup> Ed

## Copyright Notice

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## Packing List

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Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● VPC-5600S	1
● Product DVD with drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

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This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

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Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：  
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。  
二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

## China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products  
AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

**Note:** The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

# Table of Contents

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<b>Chapter 1 - Product Specifications</b> .....	<b>1</b>
1.1 Specifications .....	2
<b>Chapter 2 – Hardware Information</b> .....	<b>4</b>
2.1 Dimensions .....	5
2.2 Jumpers and Connectors.....	9
2.3 List of Jumpers .....	11
2.3.1 COM1 Ring/+5V/+12V Selection (CN15).....	12
2.3.2 Clear CMOS (CN10) .....	12
2.3.3 ATX/AT Selection (CN14).....	12
2.3.4 Can Bus UART/USB Selection (CN16).....	12
2.3.5 Can Bus Program Firmware (CN18).....	13
2.4 List of Connectors.....	14
2.4.1 Front Plane Connector (CN5).....	16
2.4.2 COM4 RS-232 Serial Port Connector (COM1).....	16
2.4.3 COM3 RS-232 Serial Port Connector (COM2).....	16
2.4.4 COM1 & COM2 RS-232/422/485 Serial Port Connector (COM3) .	17
2.4.5 Digital I/O Connector (CN20).....	17
2.4.6 Power In & Remote Button (CN19).....	18
2.4.7 CAN Bus 2.0B Connector (CN22) .....	18
2.4.8 Power on/off delay select (Sw3).....	19
2.5 2.5" HDD Installation.....	20
2.6 mSATA Drive Installation .....	22
2.7 GPS & RAM Installation.....	26
<b>Chapter 3 - AMI BIOS Setup</b> .....	<b>33</b>
3.1 System Test and Initialization .....	34
3.2 AMI BIOS Setup .....	35

3.3	Setup submenu: Main .....	36
3.4	Setup submenu: Advanced .....	37
3.4.1	Advanced: CPU Configuration .....	38
3.4.2	Advanced: PCH-FW Configuration .....	39
3.4.3	Advanced: SATA Drives .....	40
3.4.4	Advanced: Trusted Computing .....	41
3.4.5	Advanced: Hardware Monitor .....	43
3.4.6	Advanced: SIO Configuration .....	44
3.4.6.1	SIO Configuration: Serial Port Configuration .....	45
3.4.6.2	SIO Configuration: Serial Port 1 Configuration .....	46
3.4.6.3	SIO Configuration: Serial Port 2 Configuration .....	47
3.4.6.4	SIO Configuration: Serial Port 3 Configuration .....	48
3.4.6.5	SIO Configuration: Serial Port 4 Configuration .....	49
3.4.6.6	SIO Configuration: Serial Port 5 Configuration .....	50
3.4.6.7	SIO Configuration: Serial Port 6 Configuration .....	51
3.4.7	Advanced: Digital IO Port Configuration .....	52
3.4.8	Advanced: Power Management .....	53
3.5	Setup submenu: Chipset .....	54
3.5.1	Chipset: System Agent (SA) Configuration .....	55
3.5.1.1	System Agent (SA) Configuration: Graphics Configuration .....	56
3.6	Setup submenu: Security .....	57
3.7	Setup submenu: Boot .....	58
3.8	Setup submenu: Save & Exit .....	59
<b>Chapter 4 – Drivers Installation .....</b>		<b>60</b>
4.1	Product CD/DVD .....	61
<b>Appendix A - Watchdog Timer Programming .....</b>		<b>63</b>
A.1	Watchdog Timer Initial Program .....	64
<b>Appendix B - I/O Information .....</b>		<b>69</b>

B.1	I/O Address Map .....	70
B.2	IRQ Mapping Chart.....	71
<b>Appendix C – Digital I/O Ports.....</b>		<b>72</b>
C.1	DI/O Programming .....	73
C.2	Digital I/O Register .....	74
C.3	Digital I/O Sample Program.....	75

# Chapter 1

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Product Specifications

## 1.1 Specifications

### System

- **Form Factor** In-Vehicle NVR
- **Processor** Intel® 7th Gen. Core™ i3/i5/i7 Processor  
(Default: i3-7100U)
- **Chipset** —
- **Main Memory** Up to 32GB, DDR4 260-pin SODIMM
- **Display** HDMI x 1, DP x 1
- **Ethernet** 10/100/1000Base-TX x 6 (Max. 10)
- **PoE Ethernet Port** 4 ports (Max. 8 ports)
- **RAID support** 0/1
- **Expansion Slot** Mini-Card slot x 3 (USB2.0 x 2 + PCIe & USB 2.0 x 1) Built-in CAN 2.0B x 1
- **GPS, G Sensor** Onboard (GPS/GLONASS, G Sensor)
- **Front I/O Panel** Power Button x 1  
3G/4G/WIFI LED x 3  
USB3.0 x 4  
SIM slot x 2  
GbE port (RJ-45) x 2  
PoE LAN x 4 (IEEE 802.3 at/af), Max. 8 ports
- **Rear I/O Panel** DC-In power x 1 Remote Power x 1  
8bit DIO x 1, 4-ch digital input (Wet/dry contact with Isolation Protection 3,000 VDC) ,  
4-ch digital output (Compatible 5 V/TTL, 31 mA max. per channel)  
DC 12V Output x 1 RS-232/422/485 x 2  
HDMI x 1, DP x 1

CanBus connector x 1, USB3.0 x 4, Audio  
Line-out x 1, Mic-In x 1

## Storage

- HDD Tray 2.5" HDD Bay x 2
- CF/CFast/mSATA Slot mSATA Slot x 1

## Environmental

- Operating Temperature -4°F ~ 158°F (-20°C ~ 70°C);  
Project base, -40°C ~ 85°C
- Storage Temperature -40°F ~ 185°F (-40°C ~ 85°C)
- Storage Humidity 10%~80% @40°C, non-condensing
- Vibration/Shock MIL-STD-810G
- Certification CE & FCC Class A, EMARK

## Power Requirement

- Power Supply DC 10-36V

## Mechanical

- Removable HDD Tray Hot swappable 2.5" HDD/SSD x 2 (Project base) via extension module
- Internal System HDD Bay 2.5" HDD x 2
- Dimension 6.85" x 7.87" x 2.52" (174mm x 200mm x 64mm)
- Gross Weight 5.7 lb (2.6 kg)
- Note —



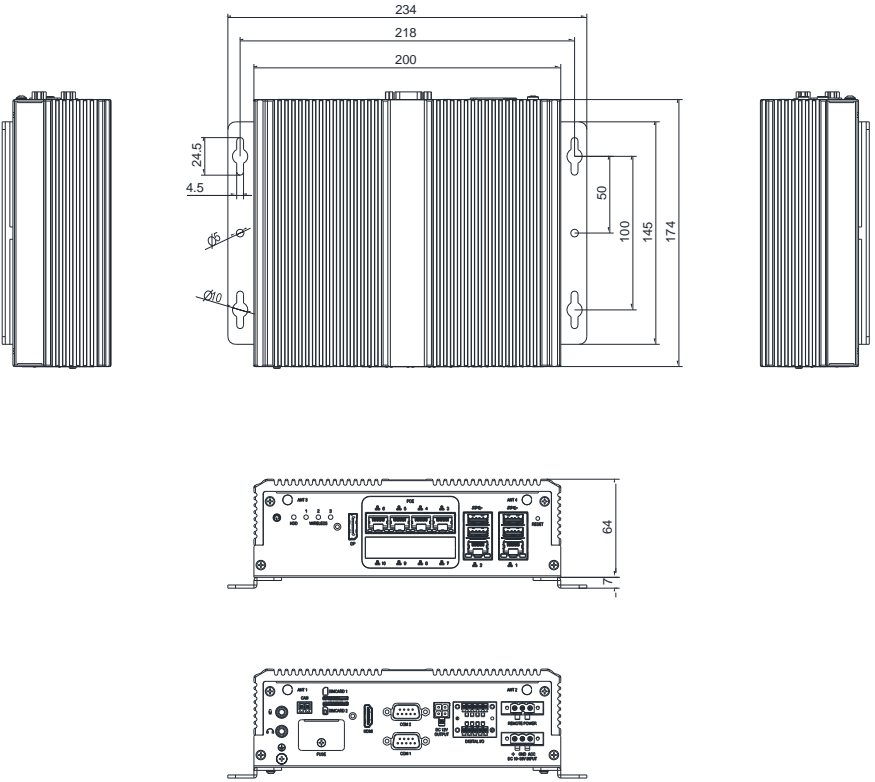
# Chapter 2

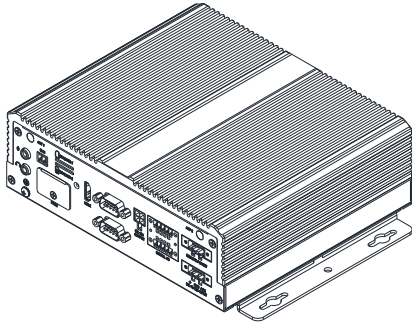
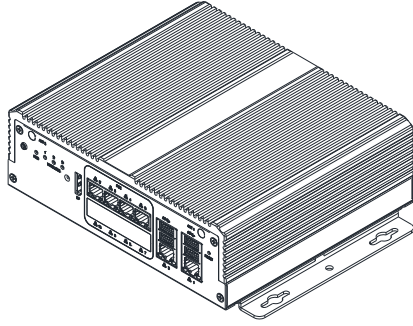
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Hardware Information

## 2.1 Dimensions

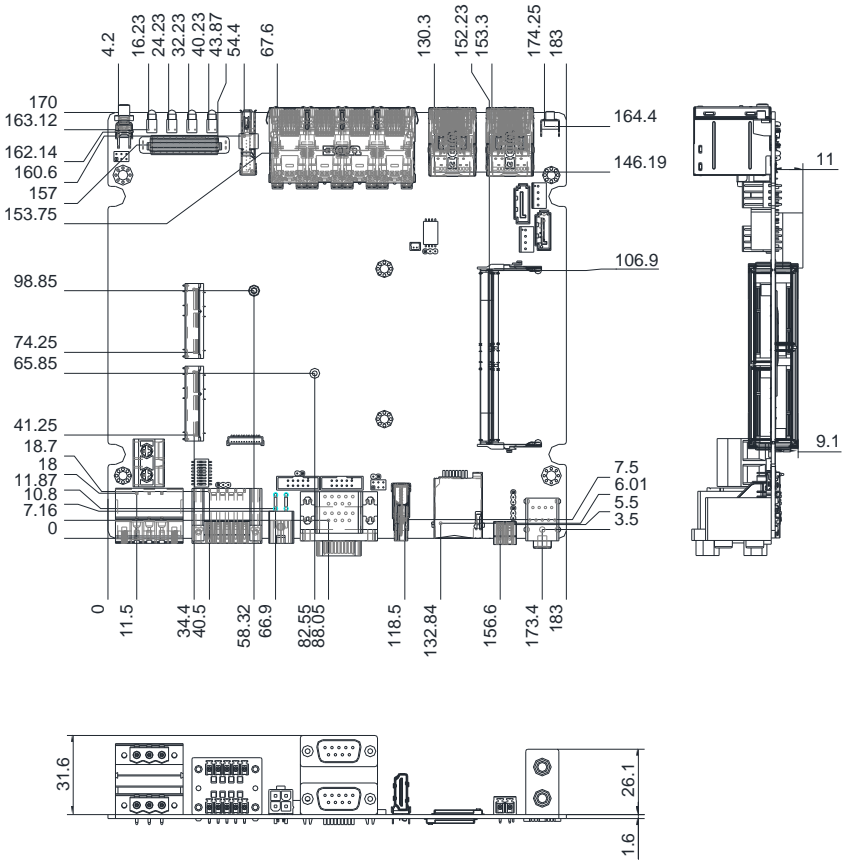
### Chassis



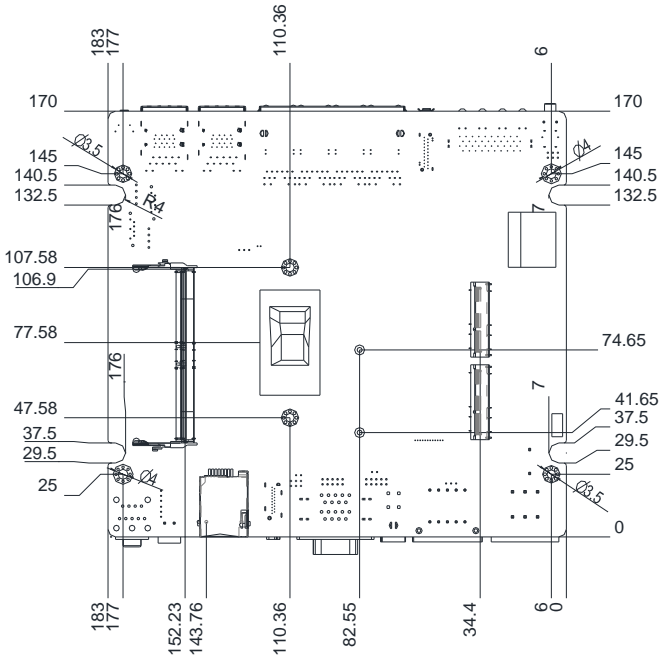


# Board

## Component side

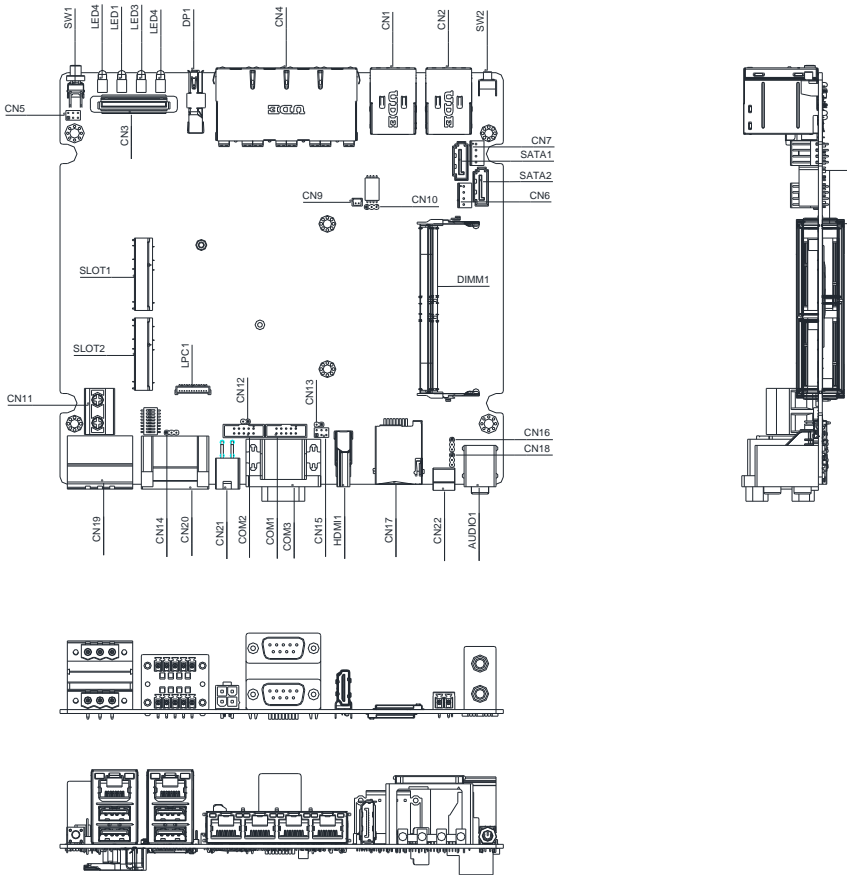


Solder side

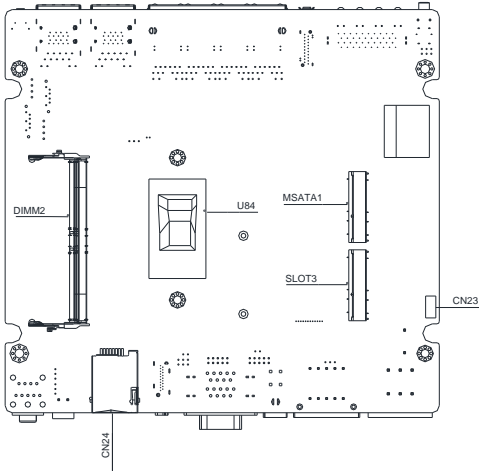


## 2.2 Jumpers and Connectors

### Component side



### Solder side



## 2.3 List of Jumpers

---

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN10	Clear CMOS
CN14	ATX/AT Selection
CN15	COM1 Ring/+5V/+12V Selection
CN16	Can Bus UART/USB Selection
CN18	Can Bus Program Firmware



### 2.3.1 COM1 Ring/+5V/+12V Selection (CN15)

---

Pin	Function
1-2	+5 V
3-4	Ring (Default)
5-6	+12 V

### 2.3.2 Clear CMOS (CN10)

---

Pin	Function
1-2	Clear
2-3	Protected (Default)

### 2.3.3 ATX/AT Selection (CN14)

---

Pin	Function
1-2	ATX
2-3	AT (Default)

### 2.3.4 Can Bus UART/USB Selection (CN16)

---

Pin	Function
1-2	UART
2-3	USB (Default)

### 2.3.5 Can Bus Program Firmware (CN18)

---

Pin	Function
1-2	Protected (Default)
2-3	Program

## 2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
SW1	Power Button
SW3	Software Reset
SW4	Power on/off delay selection
VGA1	CRT Port
SW1	Power Button
CN5	Front Panel Connector
CN3	Board to Board Connector
DP1	Display Port
CN4	LAN3~LAN6(With POE Function)
CN1	USB3 & USB4 Connector with LAN2(10/100/1000 Base-Tx Ethernet) Connector
CN2	USB1 & USB2Connector with LAN1(10/100/1000 Base-Tx Ethernet) Connector
SW2	Software Reset
CN19	Power In & Remote Button
CN20	Digital I/O Connector
CN21	+12V Output
COM1	COM4 RS-232 Serial Port Connector
COM2	COM3 RS-232 Serial Port Connector
COM3	COM1 & COM2 RS-232/422/485 Serial Port Connector
HDMI1	HDMI
CN17	SIM Card(With SLOT2)
CN24	SIM Card(With SLOT3)

CN22	CAN Bus 2.0B Connector
AUDIO1	Audio Connector
CN11	Fuse Connector
SW3	Power on/off delay select
DIMM1	DIMM2 Slot
DIMM2	DIMM1 Slot
SLOT1	Mini Card Connector(only USB) half size
SLOT2	Mini Card Connector(PCIe+USB) full size
SLOT3	Mini Card Connector(only USB) full size
MSATA1	mini-SATA Connector
SATA1	Primary Serial ATA Connector
SATA2	Secondary Serial ATA Connector
LED4	SATA LED
LED1~LED3	Mini Card WLED (SLOT1 w/LED1,SLOT2 w/LED2,SLOT3 w/LED3)

### 2.4.1 Front Plane Connector (CN5)

---

Pin	Signal	Pin	Signal
1	PWR_SW#	2	FPANSWH#
3	GND	4	HWRST#
5	GND	6	FPANSWH#

### 2.4.2 COM4 RS-232 Serial Port Connector (COM1)

---

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

### 2.4.3 COM3 RS-232 Serial Port Connector (COM2)

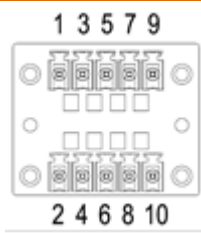
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Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

## 2.4.4 COM1 & COM2 RS-232/422/485 Serial Port Connector (COM3)

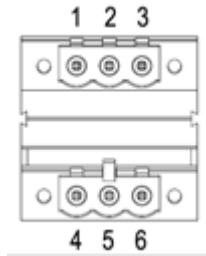
Pin	Signal	Pin	Signal
1	DCD (RS485 Data-/RS422 TX-)	2	RXD (RS422 RX-)
3	TXD (RS485 Data+/RS422 TX+)	4	DTR (RS422 RX+)
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

## 2.4.5 Digital I/O Connector (CN20)



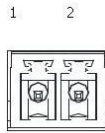
Pin	Signal	Pin	Signal
1	GND	2	+GP_V
3	GPI0	4	GPO0
5	GPI1	6	GPO1
7	GPI2	8	GPO2
9	GPI3	10	GPO3

## 2.4.6 Power In & Remote Button (CN19)



Pin	Signal	Pin	Signal
1	ACC	2	GND_PRI
3	PWR_IN	4	REMOTE_SW
5	GND	6	PS_ON#

## 2.4.7 CAN Bus 2.0B Connector (CN22)



Pin	Signal	Pin	Signal
1	CAN DATA +	2	CAN DATA-

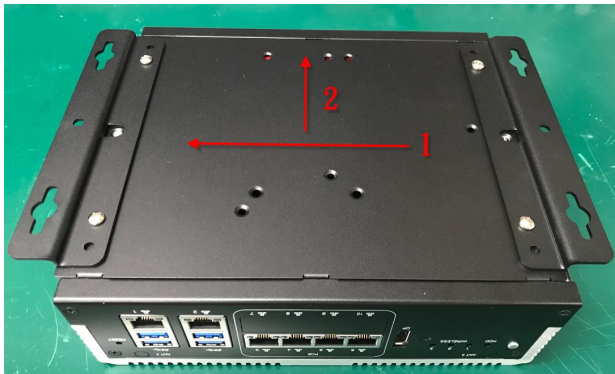
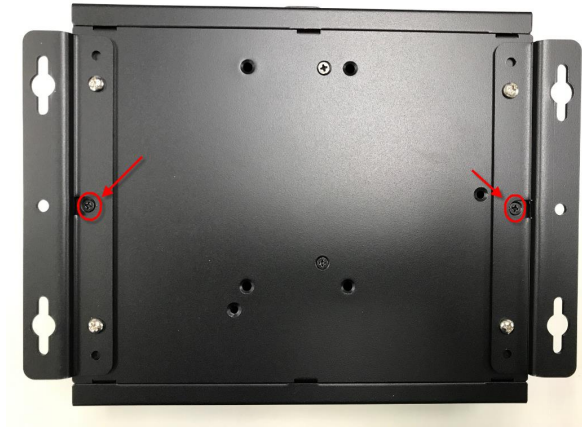
## 2.4.8 Power on/off delay select (Sw3)

Switch Pin Number	Power On Delay			Time (Sec)	Power Off Delay			Time (Sec)	Remarks
	6	7	8		5	4	3		
Control Table	off	off	off	5	off	off	off	180	
	off	off	on	10	off	off	on	300	
	off	on	off	15	off	on	off	900	
	off	on	on	30	off	on	on	1800	
	on	off	off	Null	on	off	off	2 Day	
	on	off	on	Null	on	off	on	Null	
	on	on	off	Null	on	on	off	Null	
	on	on	on	Null	on	on	on	Null	



## 2.5 2.5" HDD Installation

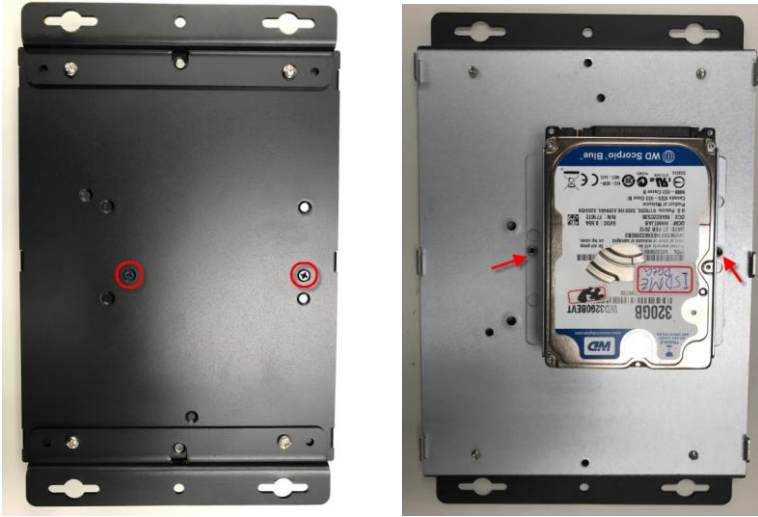
1. Loosen the screws and remove the bottom cover



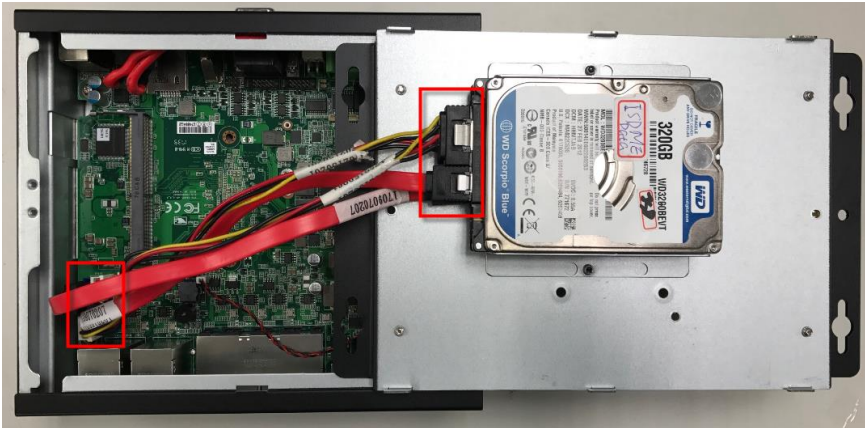
2. Attach the brackets to the HDD.



3. Install the HDD onto the bottom cover



4. Attach the cables to the motherboard

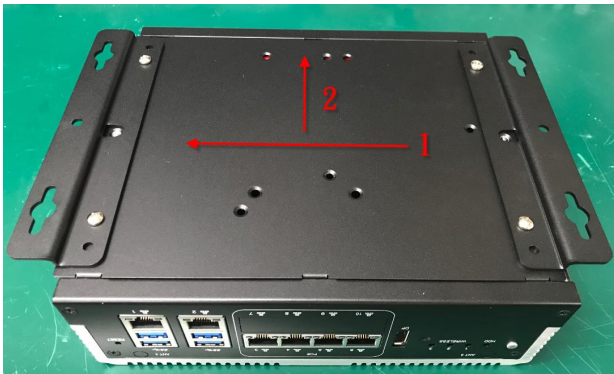
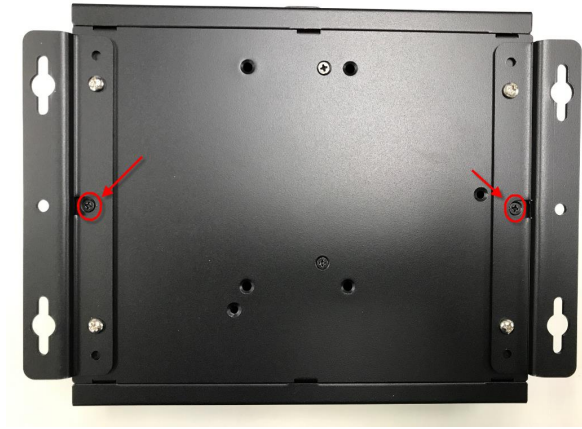


5. Replace the bottom cover and tighten the screws.

## 2.6 mSATA Drive Installation

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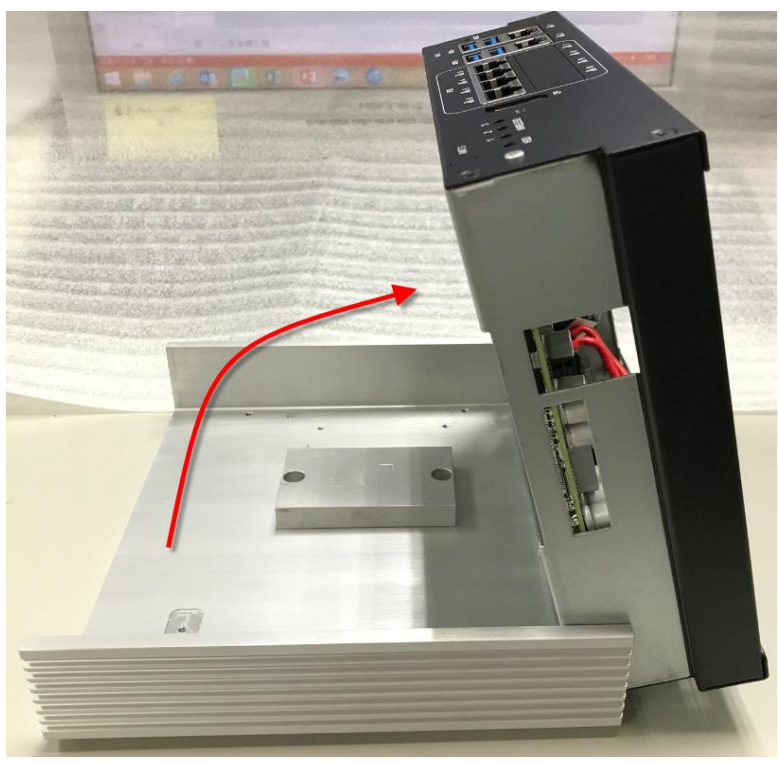
1. Loosen the screws and remove the bottom cover



2. Remove the screws from 6 locations



3. Remove the top cover





4. Install the mSATA drive onto the motherboard and tighten the screw

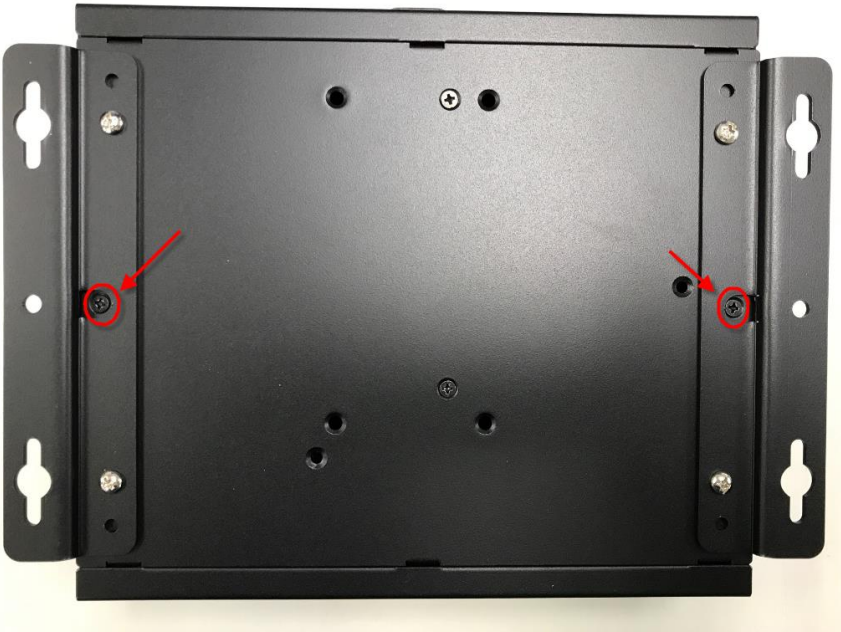


5. Replace the top cover and tighten the screws
6. Replace the bottom cover and tighten the screws

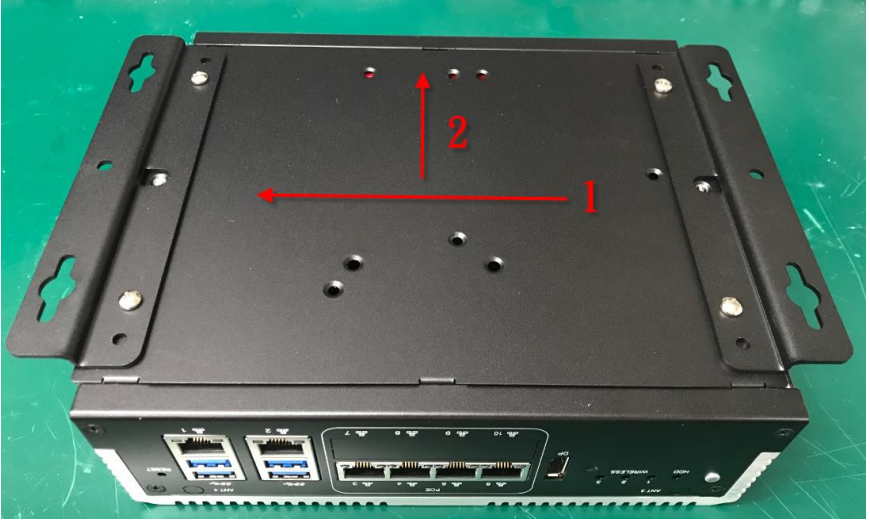
## 2.7 GPS & RAM Installation

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1. Unscrew the bottom cover.



2. Remove the bottom cover.





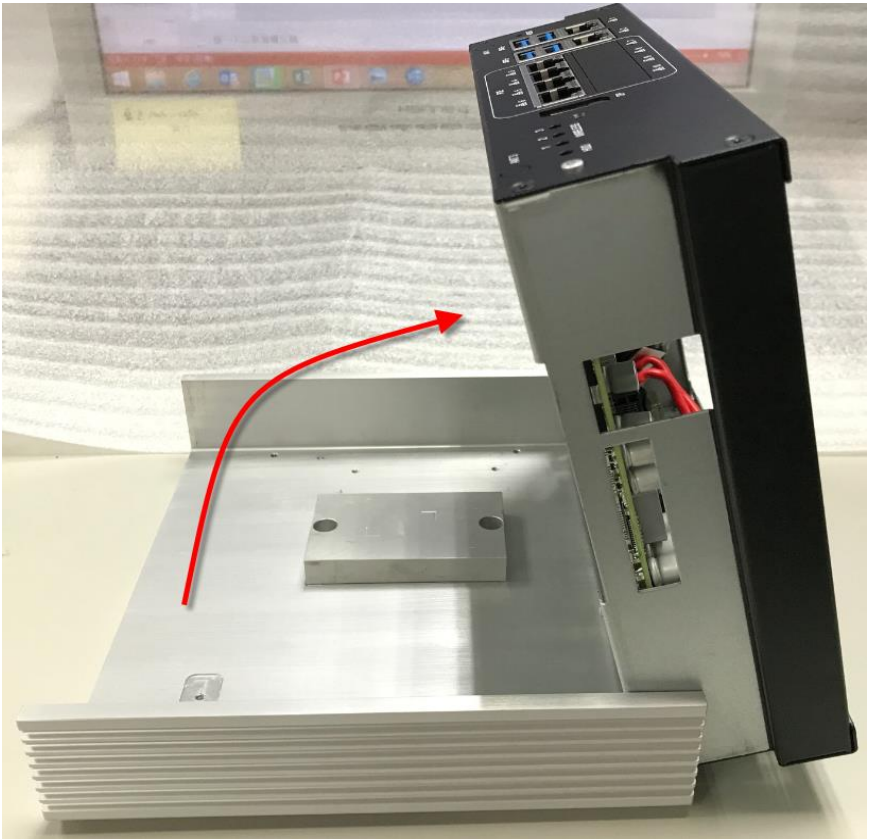
3. Remove these six screws.



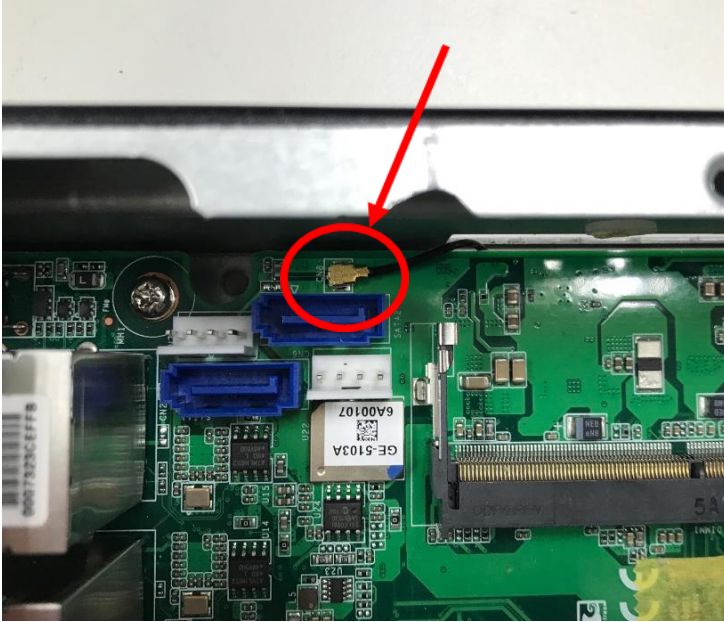
4. Lift up the case.



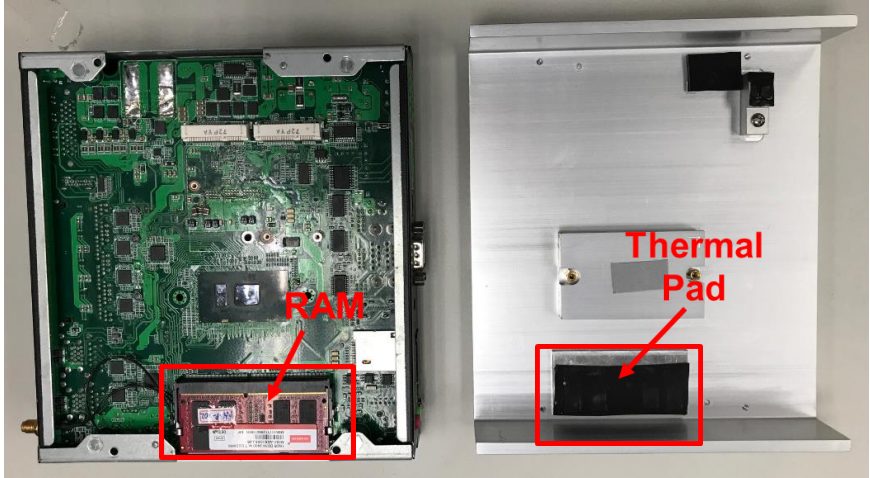
5. Pick up the case.



6. Install the GPS cable and WiFi Screw.



7. Install the RAM and thermal pad.



# Chapter 3

---

AMI BIOS Setup



## 3.1 System Test and Initialization

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The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

## 3.2 AMI BIOS Setup

---

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Enable/ Disable boot option for legacy network devices

**Chipset** – For hosting bridge parameters

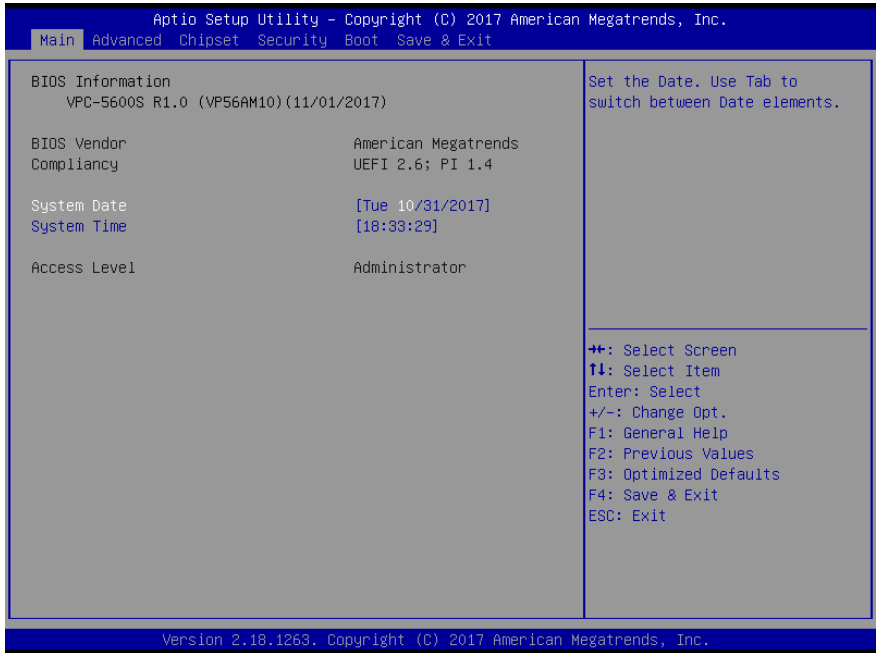
**Security** – The setup administrator password can be set here

**Boot** – Enable/ Disable quiet Boot Option

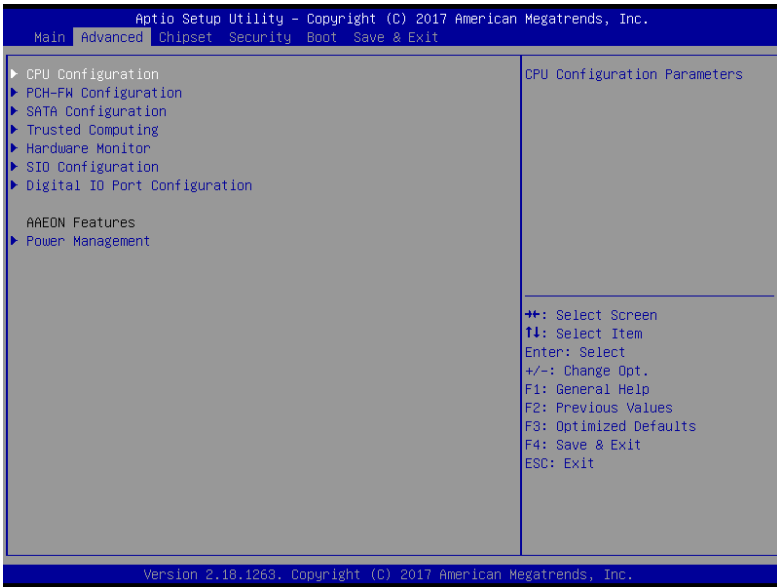
**Save & Exit** – Save your changes and exit the program



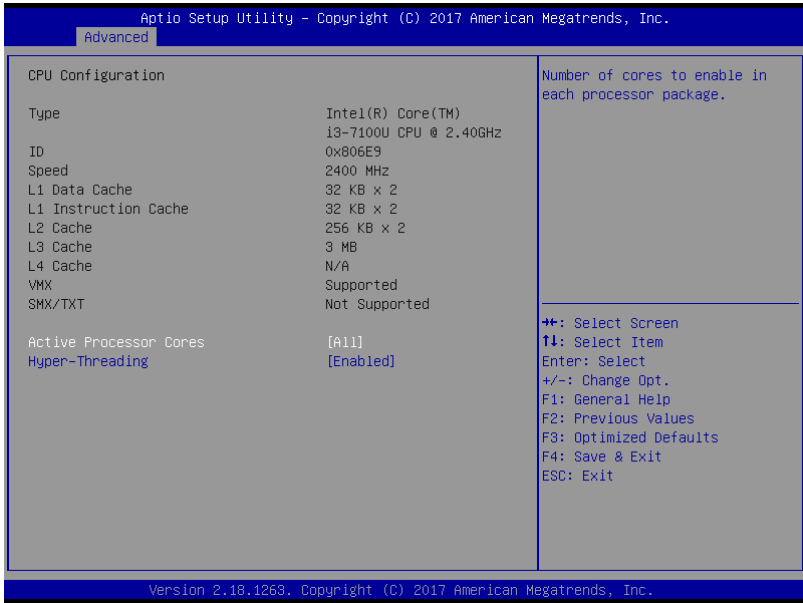
### 3.3 Setup submenu: Main



### 3.4 Setup submenu: Advanced



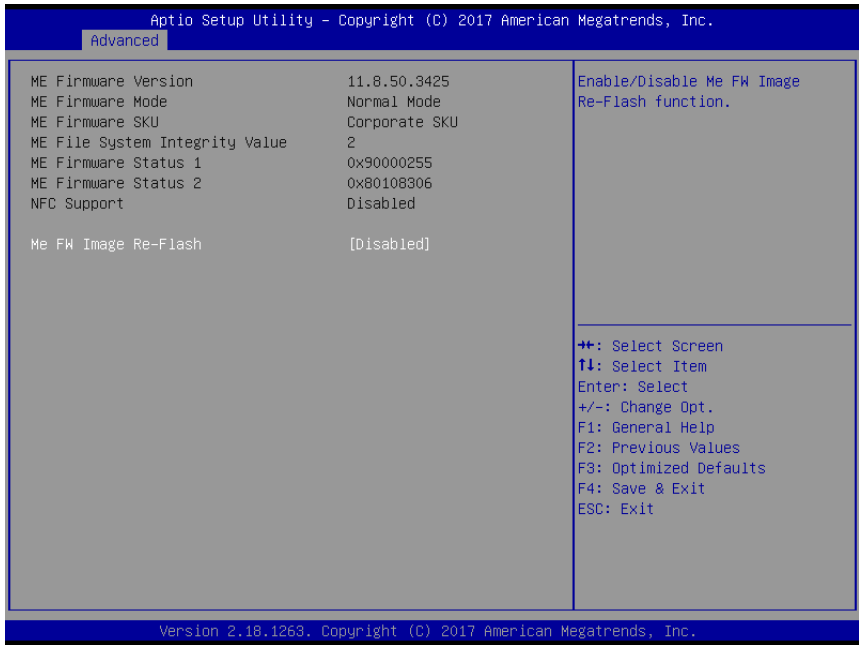
### 3.4.1 Advanced: CPU Configuration



Options summary:

Active Processor Cores	All
	1
Number of cores to enable in each processor package.	
Hyper-Threading	Disabled
	Enabled
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).	

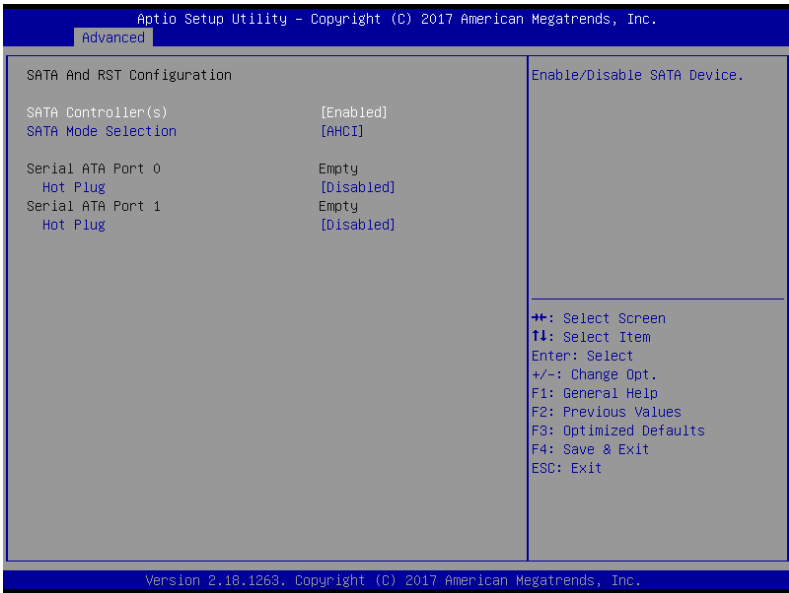
### 3.4.2 Advanced: PCH-FW Configuration



Options summary:

ME FW Image Re-Flash	Disabled
	Enabled
Enable/Disable Me FW Image Re-Flash function.	

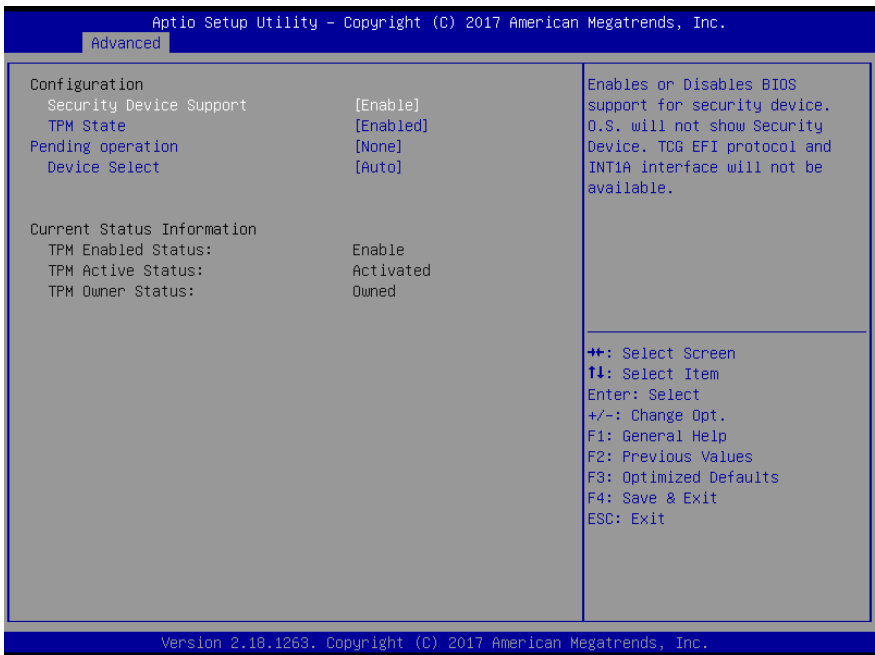
### 3.4.3 Advanced: SATA Drives



Options summary:

SATA Controller(s)	Disabled
	Enabled
Enable/Disable SATA Device.	
Hot Plug	Disabled
	Enabled
Designates this port as Hot Pluggable.	

### 3.4.4 Advanced: Trusted Computing



Options summary:

Security Device Support	Disabled
	<b>Enabled</b>
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.	
TPM State	Disabled
	<b>Enabled</b>
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.	
Pending operation	<b>None</b>
	TPM Clear
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.	
Device Select	TPM 1.2
	TPM 2.0
	<b>Auto</b>

TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

### 3.4.5 Advanced: Hardware Monitor

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

Advanced

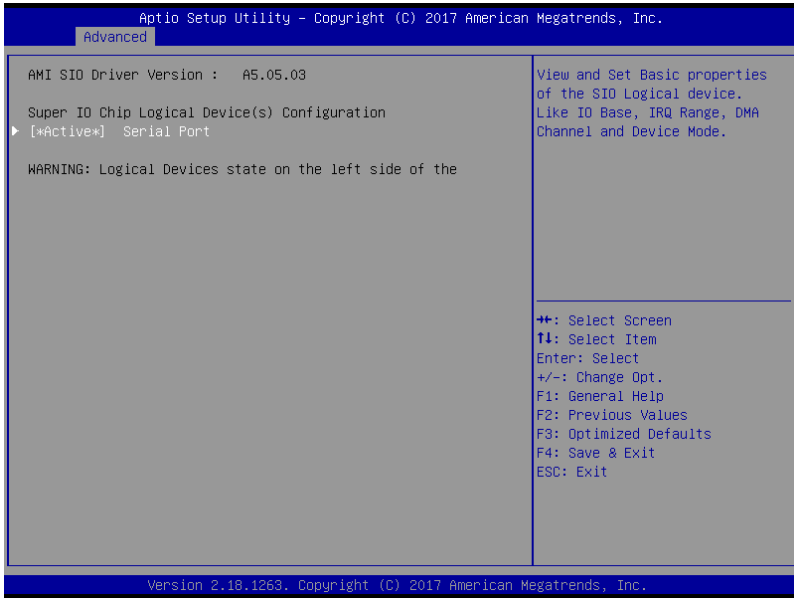
CPU Temperature(DTS)	: +100 %
System Temperature	: +52 %
VCORE	: +0.712 V
+1.2V	: +1.232 V
+5V	: +5.045 V
+12V	: +12.232 V
+5VSB	: +5.112 V
+3.3V	: +3.376 V
VBAT	: +3.104 V

++: Select Screen  
↑↓: Select Item  
Enter: Select  
+/-: Change Opt.  
F1: General Help  
F2: Previous Values  
F3: Optimized Defaults  
F4: Save & Exit  
ESC: Exit

Version 2.18.1263. Copyright (C) 2017 American Megatrends, Inc.



### 3.4.6 Advanced: SIO Configuration



### 3.4.6.1 SIO Configuration: Serial Port Configuration

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

Advanced

AMI SIO Driver Version : A5.07.03

Super IO Chip Logical Device(s) Configuration

- ▶ [\*Active\*] Serial Port 1
- ▶ [\*Active\*] Serial Port 2
- ▶ [\*Active\*] Serial Port 3
- ▶ [\*Active\*] Serial Port 4
- ▶ [\*Active\*] Serial Port 5
- ▶ [\*Active\*] Serial Port 6

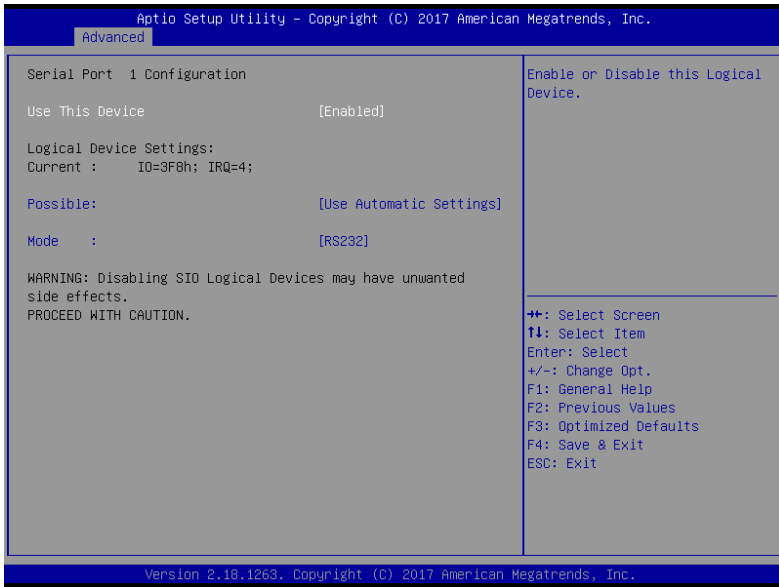
WARNING: Logical Devices state on the left side of the control, reflects the current Logical Device state. Changes made during Setup Session will be shown after you restart the system.

View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.

++: Select Screen  
↑: Select Item  
Enter: Select  
+/-: Change Opt.  
F1: General Help  
F2: Previous Values  
F3: Optimized Defaults  
F4: Save & Exit  
ESC: Exit

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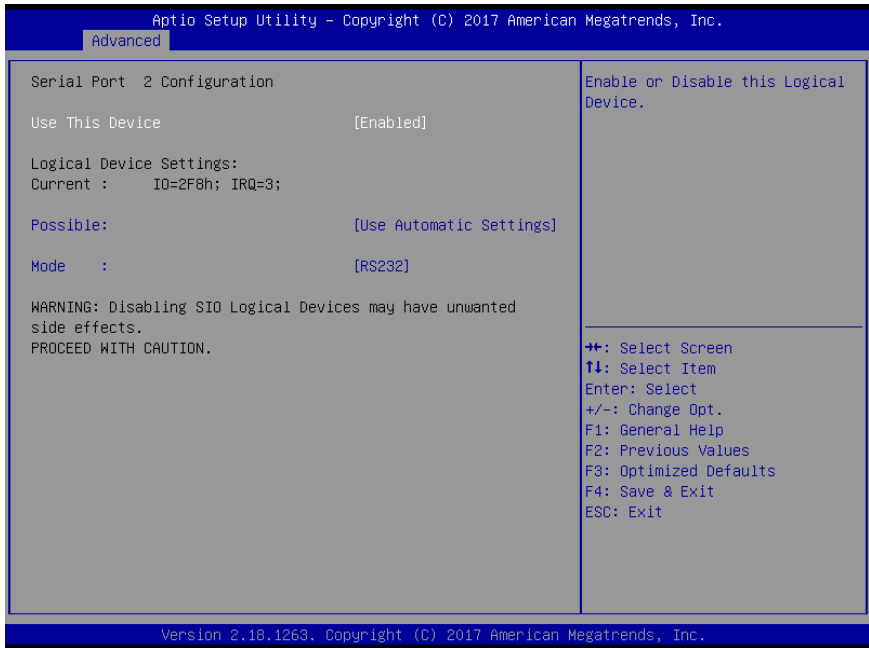
### 3.4.6.2 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	
Mode	<b>RS232</b>
	RS422
	RS485
UART RS232, 422, 485 selection.	

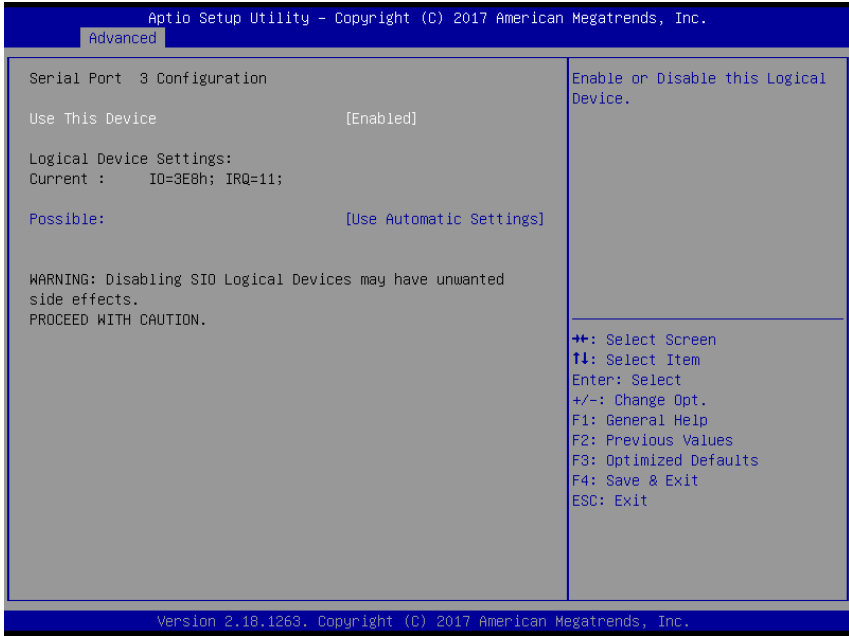
### 3.4.6.3 SIO Configuration: Serial Port 2 Configuration



Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	
Mode	<b>RS232</b>
	RS422
	RS485
UART RS232, 422, 485 selection.	

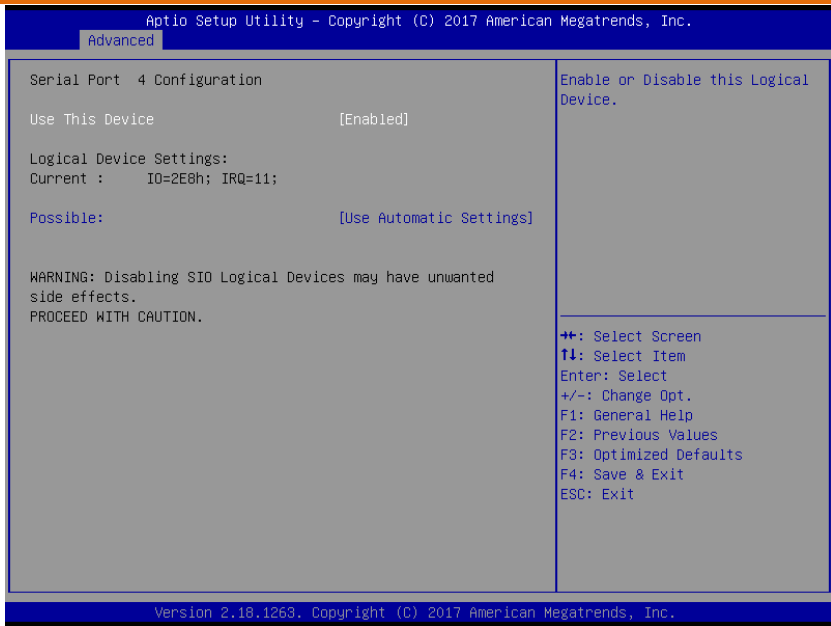
### 3.4.6.4 SIO Configuration: Serial Port 3 Configuration



Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

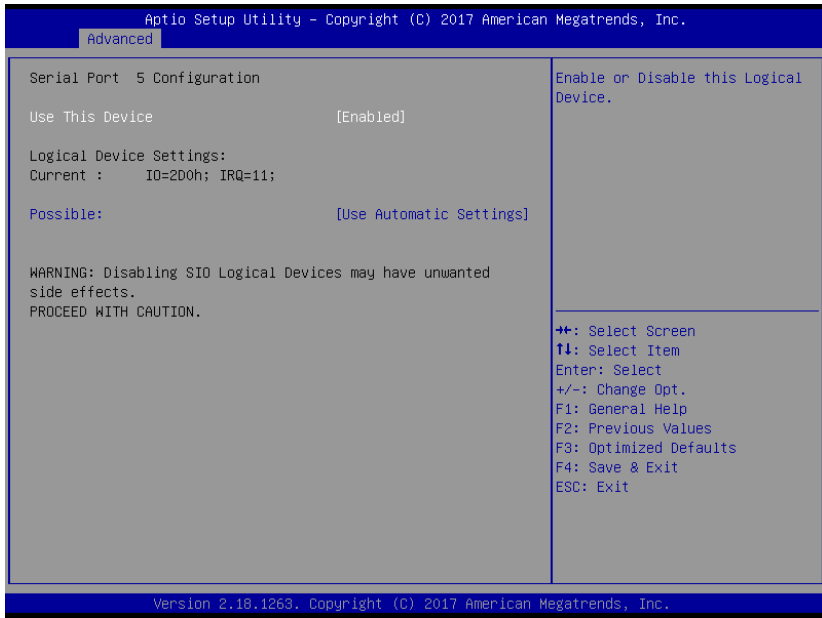
### 3.4.6.5 SIO Configuration: Serial Port 4 Configuration



Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

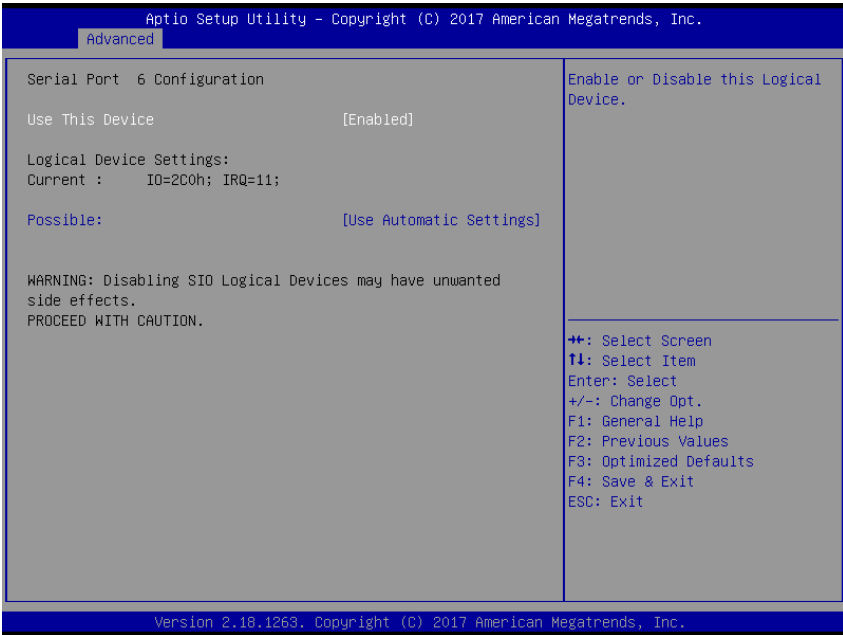
### 3.4.6.6 SIO Configuration: Serial Port 5 Configuration



Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

### 3.4.6.7 SIO Configuration: Serial Port 6 Configuration

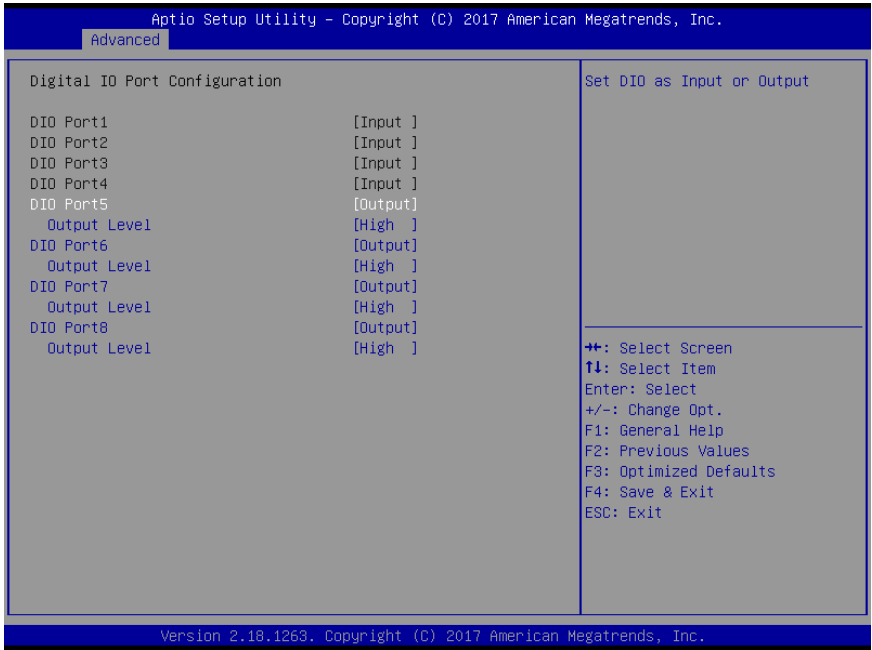


Options summary:

Use This Device	Disabled
	<b>Enabled</b>
Enable or Disable this Logical Device.	
Possible:	<b>Use Automatic Settings</b>
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	



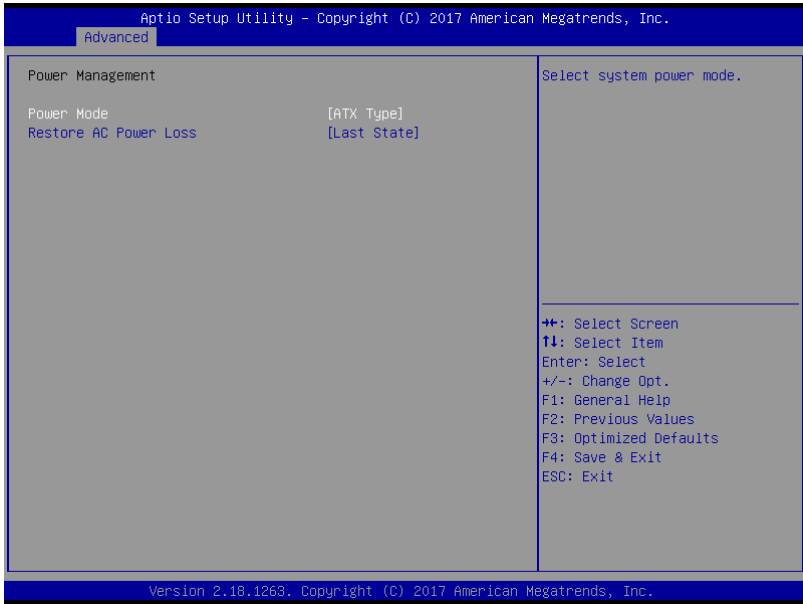
### 3.4.7 Advanced: Digital IO Port Configuration



Options summary:

DIO Port5~8	Output
	Input
Set DIO as Input or Output.	
Output Level	Low
	High
Set output level when DIO pin is output.	

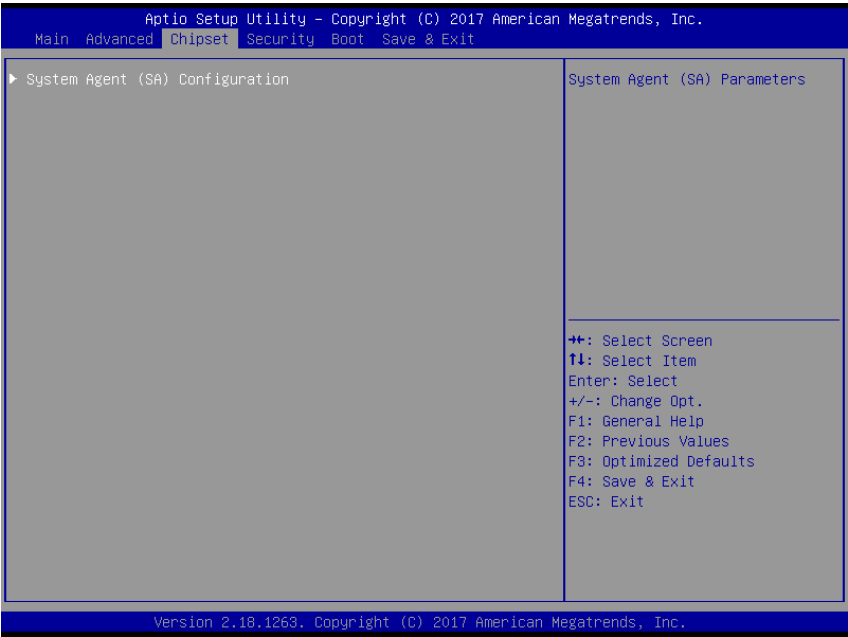
### 3.4.8 Advanced: Power Management



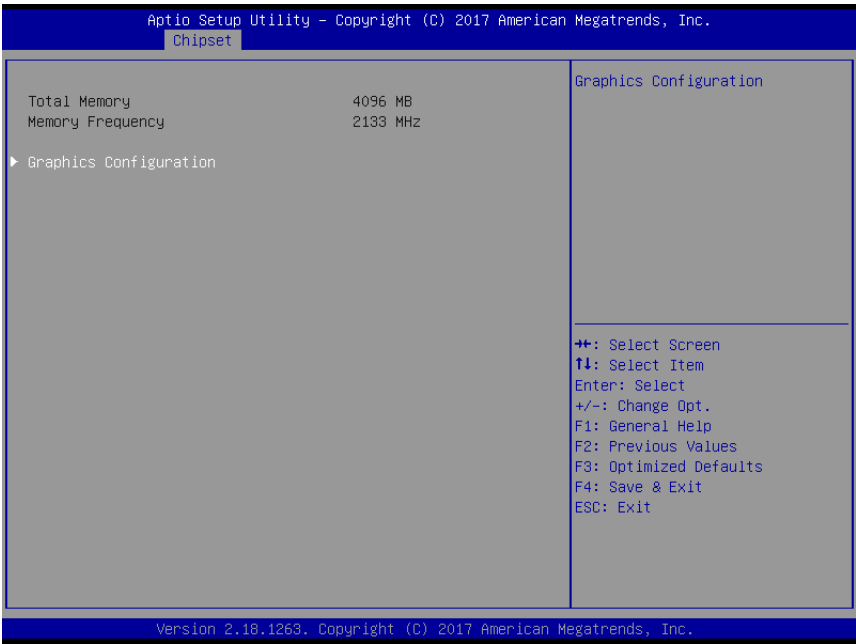
Options summary:

Power Mode	<b>ATX Type</b>
	AT Type
Select Power Supply Mode.	
Restore AC Power Loss	Power Off
	Power On
	<b>Last State</b>
Select AC power state when power is re-applied after a power failure.	

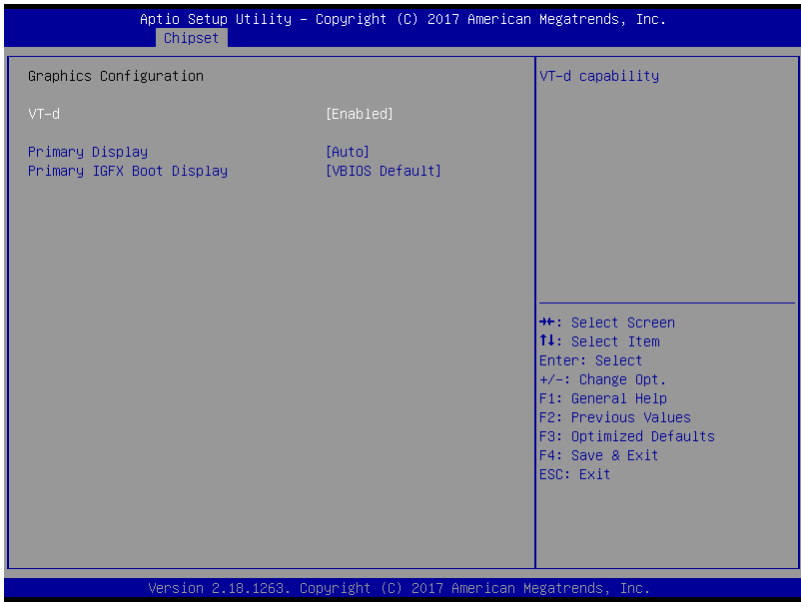
### 3.5 Setup submenu: Chipset



### 3.5.1 Chipset: System Agent (SA) Configuration



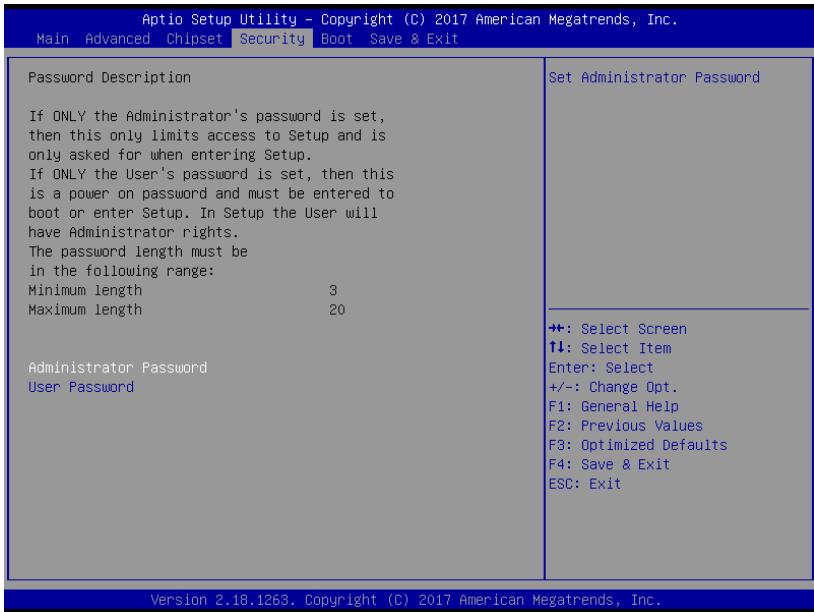
### 3.5.1.1 System Agent (SA) Configuration: Graphics Configuration



Options summary:

VT-d	<b>Enabled</b>
	Disabled
VT-d capability.	
Primary Display	<b>Auto</b>
	IGFX
	PEG
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.	
Primary IGFX Boot Display	<b>VBIOS Default</b>
	HDMI
	DP
<p>Select the Video Device which will be activated during POST.          This has no effect if external graphics present.          Secondary boot display selection will appear based on your selection.          VGA modes will be supported only on primary display</p>	

## 3.6 Setup submenu: Security



### Change User/Supervisor Password

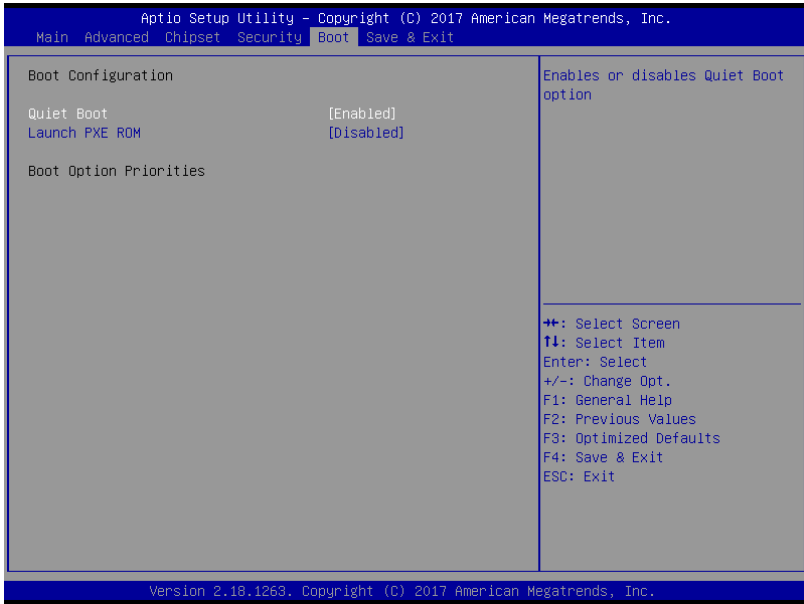
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

### Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

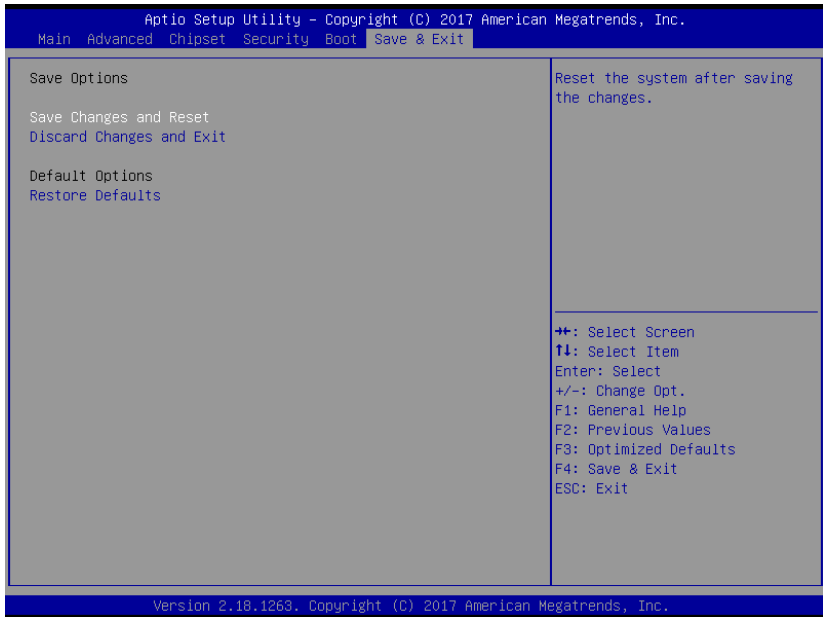
### 3.7 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Launch PXE ROM	Disabled
	Enabled
Controls the execution of UEFI and Legacy PXE OpROM	

### 3.8 Setup submenu: Save & Exit





# Chapter 4

---

Drivers Installation

## 4.1 Product CD/DVD

---

The VPC-5600S comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

### Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

### Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphic** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 3 – Install LAN Drivers

1. Open the **Step 3 – LAN** folder and select your OS
2. Open the **setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 4 – Install Audio Driver

1. Open the **Step 4 - Audio** folder and select your OS
2. Open the **.exe** file in the folder

3. Follow the instructions
4. Drivers will be installed automatically

#### Step 5 – Install USB 3.0 Driver

1. Open the **Step 5 – USB3.0** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

#### Step 6 – Install ME Driver

1. Open the **Step 6 - ME** folder followed by **MEISetup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

#### Step 9 – Install Serial Port Driver (Optional)

1. Open the **Step 7 - Serial Port Driver (Optional)** folder and select your OS
2. Open the **.exe** or **.bat** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

# Appendix A

---

## Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN // This parameter is represented from Note20
#define byte   WDTRstReg // This parameter is represented from Note21
#define byte   WDTRstBit // This parameter is represented from Note22
#define byte   WDTRstVal // This parameter is represented from Note23
*****

```

```
*****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModelLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```



```
*****
VOID SIOEnterMBPnPMode0{
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIODData, 0x02);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIODData, LDN);
}
*****
```

# Appendix B



---

I/O Information



## B.1 I/O Address Map

---

### Input/output (IO)

- >  [0000000000000000 - 000000000000CF7] PCI Express Root Complex
- >  [000000000000D00 - 000000000000FFFF] PCI Express Root Complex

## B.2 IRQ Mapping Chart

Interrupt request (IRQ)	
 (ISA) 0x00000000 (00)	System timer
 (ISA) 0x00000003 (03)	Fintek Communications Port (COM2)
 (ISA) 0x00000004 (04)	Fintek Communications Port (COM1)
 (ISA) 0x00000008 (08)	System CMOS/real time clock
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM3)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM4)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM5)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM6)
 (ISA) 0x0000000E (14)	Motherboard resources
 (PCI) 0x0000000B (11)	Mobile 6th/7th Generation Intel(R) Processor Family I/O Thermal subsystem - 9D31
 (PCI) 0x0000000B (11)	Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
 (PCI) 0x00000010 (16)	High Definition Audio Controller
 (PCI) 0x00000010 (16)	Intel(R) Serial IO I2C Host Controller - 9D60
 (PCI) 0xFFFFFFFF0 (-16)	Intel(R) Management Engine Interface
 (PCI) 0xFFFFFFFF1 (-15)	Realtek PCIe GBE Family Controller
 (PCI) 0xFFFFFFFF2 (-14)	Realtek PCIe GBE Family Controller #2
 (PCI) 0xFFFFFFFF3 (-13)	Realtek PCIe GBE Family Controller #4
 (PCI) 0xFFFFFFFF4 (-12)	Realtek PCIe GBE Family Controller #3
 (PCI) 0xFFFFFFFF5 (-11)	Realtek PCIe GBE Family Controller #6
 (PCI) 0xFFFFFFFF6 (-10)	Realtek PCIe GBE Family Controller #5
 (PCI) 0xFFFFFFFF7 (-9)	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
 (PCI) 0xFFFFFFFF8 (-8)	Intel(R) HD Graphics 620
 (PCI) 0xFFFFFFFF9 (-7)	Standard SATA AHCI Controller
 (PCI) 0xFFFFFFFFFA (-6)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #5 - 9D14
 (PCI) 0xFFFFFFFFFB (-5)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #4 - 9D13
 (PCI) 0xFFFFFFFFFC (-4)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #3 - 9D12
 (PCI) 0xFFFFFFFFFD (-3)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #2 - 9D11
 (PCI) 0xFFFFFFFFFE (-2)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #1 - 9D10

# Appendix C

---

Digital I/O Ports

## C.1 DI/O Programming

---

VPC-5600S utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

- (1) Enter the MB PnP Mode
- (2) Modify the data of configuration registers
- (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

## C.2 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A(Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A(Note10)	2(Note11)		GPIO82
DIO-4 Pin Status	0x06(Note12)	0x8A(Note13)	3(Note14)		GPIO83
DIO-5 Pin Status	0x06(Note15)	0x8A(Note16)	4(Note17)		GPIO84
DIO-6 Pin Status	0x06(Note18)	0x8A(Note19)	5(Note20)		GPIO85
DIO-7 Pin Status	0x06(Note21)	0x8A(Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A(Note25)	7(Note26)		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89(Note32)	1(Note33)	(Note34)	GPIO81
DIO-3 Output Data	0x06(Note35)	0x89(Note36)	2(Note37)	(Note38)	GPIO82
DIO-4 Output Data	0x06(Note39)	0x89(Note40)	3(Note41)	(Note42)	GPIO83
DIO-5 Output Data	0x06(Note43)	0x89(Note44)	4(Note45)	(Note46)	GPIO84
DIO-6 Output Data	0x06(Note47)	0x89(Note48)	5(Note49)	(Note50)	GPIO85
DIO-7 Output Data	0x06(Note51)	0x89(Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89(Note56)	7(Note57)	(Note58)	GPIO87

### C.3 Digital I/O Sample Program

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```



```

*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte DOutput1LDN // This parameter is represented from Note27
#define byte DOutput1Reg // This parameter is represented from Note28
#define byte DOutput1Bit // This parameter is represented from Note29
#define byte DOutput1Val // This parameter is represented from Note30
#define byte DOutput2LDN // This parameter is represented from Note31
#define byte DOutput2Reg // This parameter is represented from Note32
#define byte DOutput2Bit // This parameter is represented from Note33
#define byte DOutput2Val // This parameter is represented from Note34
#define byte DOutput3LDN // This parameter is represented from Note35
#define byte DOutput3Reg // This parameter is represented from Note36
#define byte DOutput3Bit // This parameter is represented from Note37
#define byte DOutput3Val // This parameter is represented from Note38
#define byte DOutput4LDN // This parameter is represented from Note39
#define byte DOutput4Reg // This parameter is represented from Note40
#define byte DOutput4Bit // This parameter is represented from Note41
#define byte DOutput4Val // This parameter is represented from Note42
#define byte DOutput5LDN // This parameter is represented from Note43
#define byte DOutput5Reg // This parameter is represented from Note44
#define byte DOutput5Bit // This parameter is represented from Note45
#define byte DOutput5Val // This parameter is represented from Note46
#define byte DOutput6LDN // This parameter is represented from Note47
#define byte DOutput6Reg // This parameter is represented from Note48
#define byte DOutput6Bit // This parameter is represented from Note49
#define byte DOutput6Val // This parameter is represented from Note50
#define byte DOutput7LDN // This parameter is represented from Note51
#define byte DOutput7Reg // This parameter is represented from Note52
#define byte DOutput7Bit // This parameter is represented from Note53
#define byte DOutput7Val // This parameter is represented from Note54
#define byte DOutput8LDN // This parameter is represented from Note55
#define byte DOutput8Reg // This parameter is represented from Note56
#define byte DOutput8Bit // This parameter is represented from Note57
#define byte DOutput8Val // This parameter is represented from Note58
*****

```

```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean  AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```

*****
VOID  SIOEnterMBPnPMode0{
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

```

*****
Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID  ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****

```