

# VPC-5600S

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Mobile NVR

User's Manual 11<sup>th</sup> Ed

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## Packing List

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Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● VPC-5600S	1
● Wall Mount Bracket	2
● SATA Cable	2
● SATA Power Cable	2

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

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This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

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Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## 产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

# China RoHS Requirement (EN)

## Hazardous and Toxic Materials List

AAEON System

QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBS)	Polybrominated ethers (PBDES)
PCB and Components	X	○	○	○	○	○
Wires & Connectors for Ext.Connections	X	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	X	○	○	○	○	○
HDD Drive	X	○	○	○	○	○
LCD Module	X	X	○	○	○	○
Optical Drive	X	○	○	○	○	○
Touch Control Module	X	○	○	○	○	○
PSU	X	○	○	○	○	○
Battery	X	○	○	○	○	○

This form is prepared in compliance with the provisions of SJ/T 11364.

○: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

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# Chapter 1

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Product Specifications

## 1.1 Specifications

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### System

Form Factor	In-Vehicle NVR
Processor	7th Generation Intel® Core™ i3-7100U Processor
Chipset	—
Main Memory	260-pin DDR4 SODIMM, up to 32GB
Display	HDMI x 1 DP x 1
Ethernet	LAN x 2 + PoE x 4 (RTL8111E 10/100/1000 Base)
PoE Ethernet Port	PoE x 4 sharing 60W Power Budget
RAID support	RAID 0, 1
Expansion Slot	mSATA Slot x 1 (Optional: if mSATA slot is in use, only 1 SATA slot is available)
GPS, G-Sensor	Onboard (GPS/GLONASS), G Sensor
Front I/O Panel	Power Button x 1 3G/4G/Wi-Fi LED x 3 USB 3.0 x 4 GbE x 2 PoE LAN x 4 (IEEE 802.3 at/af) DP x 1 Reset Button x 1
Rear I/O Panel	DC-In x 1 Remote Power x 1 8-bit DIO x 1, 4-CH Digital Input (Wet/dry contact with Isolation Protection 3,000 VDC) 4-CH Digital Output (Compatible 5 V/TTL, 31 mA max. per Channel) DC 12V/1A Output x 1

## System

<b>Rear I/O Panel (Cont.)</b>	RS-232/422/485 x 2
	HDMI x 1
	CanBus Connector x 1
	Audio Line-out x 1, Mic-In x 1
	SIM Slot x 2

## Storage

<b>HDD Tray</b>	2.5" SATA SSD x 2
<b>CF/CFast/mSATA Slot</b>	mSATA Slot x 1 (Optional: if mSATA slot is in use, only 1 SATA slot is available)

## Environmental

<b>Operating Temperature</b>	-4°F ~ 158°F (-20°C ~ 70°C)
<b>Storage Temperature</b>	-40°F ~ 185°F (-40°C ~ 85°C)
<b>Storage Humidity</b>	10% ~ 80% @40°C, non-condensing
<b>Vibration/Shock</b>	MIL-STD-810G
<b>Certification</b>	CE & FCC Class A, E-Mark

## Power Requirements

<b>Power Supply</b>	10 ~ 36V DC, with Ignition Pin
---------------------	--------------------------------

## Mechanical

<b>Removable HDD Tray</b>	-
<b>Internal System HDD Bay</b>	2.5" SATA HDD x 2
<b>Dimension</b>	6.85" x 7.87" x 2.52" (174mm x 200mm x 64mm)
<b>Gross Weight</b>	5.7 lb. (2.6Kg)

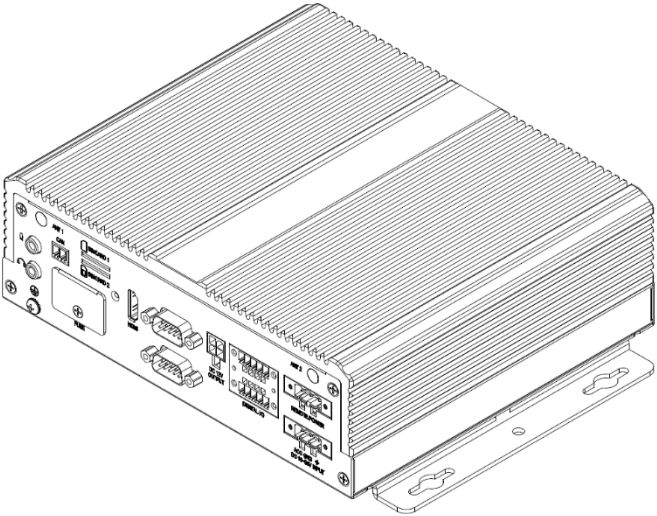
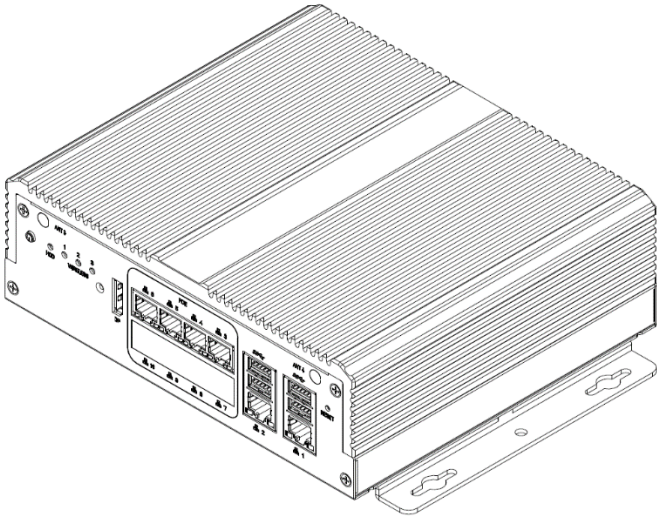


# Chapter 2

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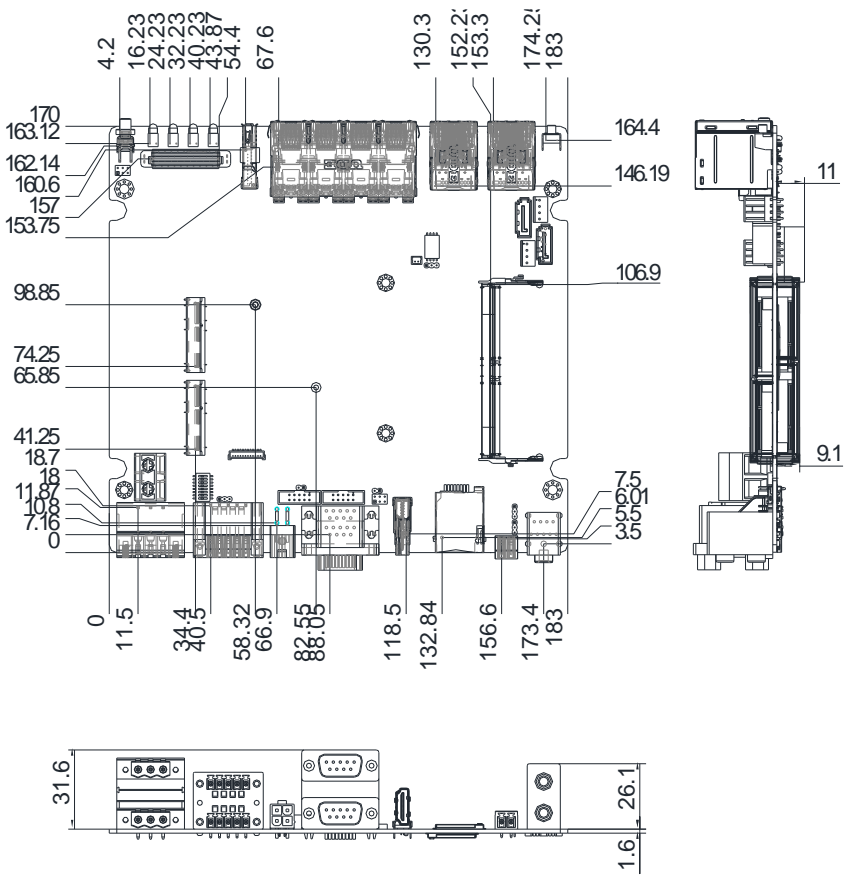
Hardware Information



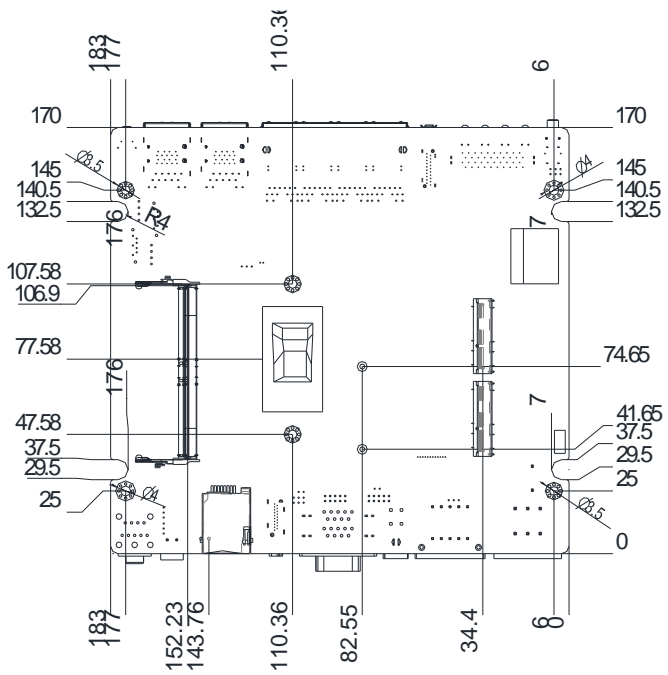


Board

Component side

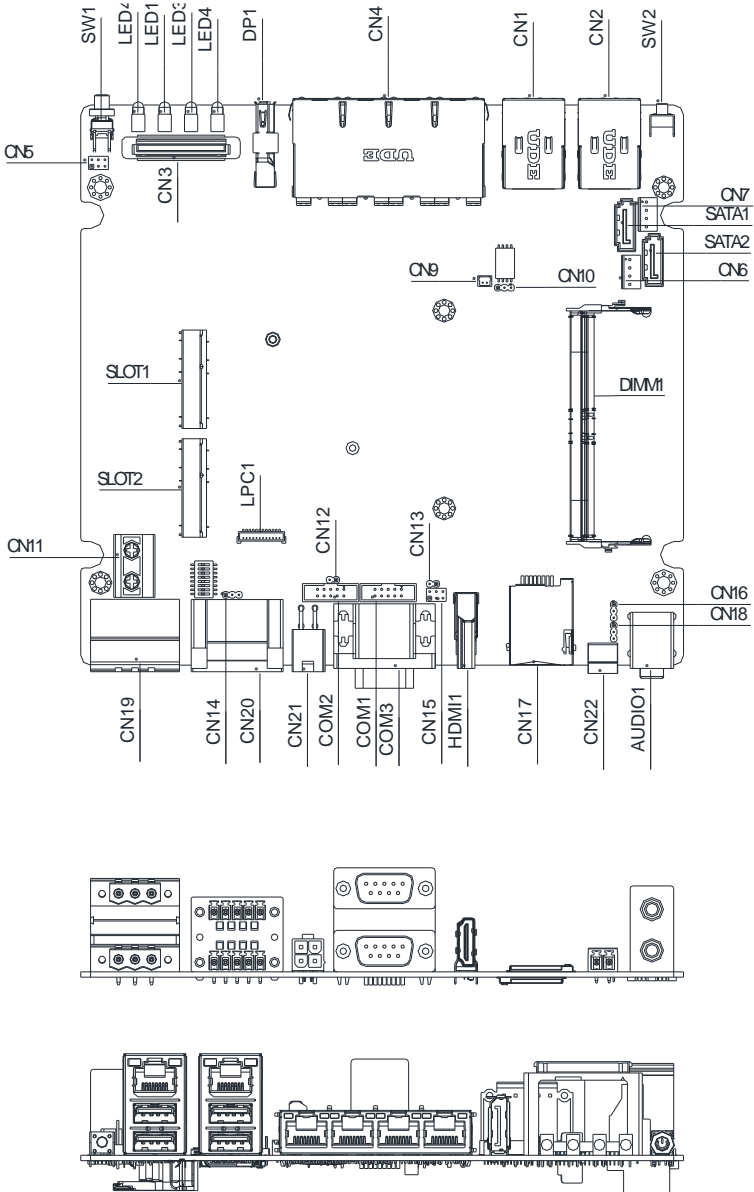


Solder side

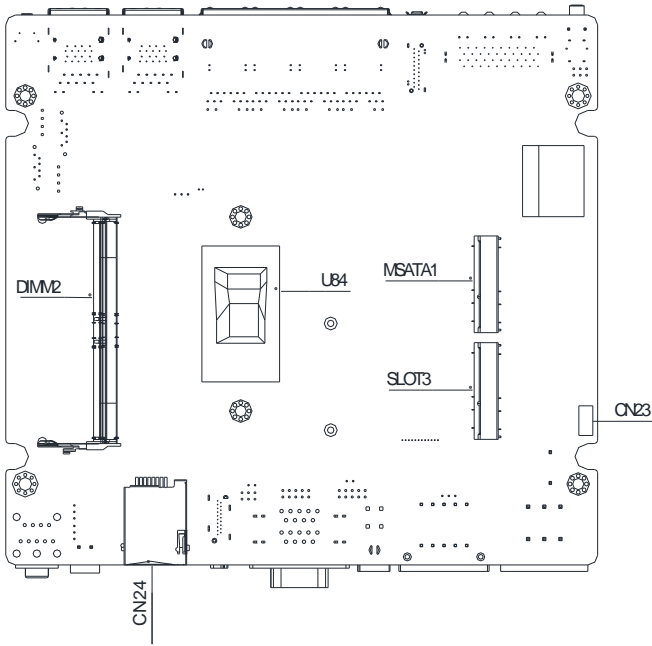


## 2.2 Jumpers and Connectors

### Component side



Solder side



## 2.3 List of Jumpers

---

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN10	Clear CMOS
CN14	ATX/AT Selection
CN15	COM 1 Ring/+5V/+12V Selection
CN16	CANBus UART/USB Selection
CN18	CANBus Program Firmware

### 2.3.1 Clear CMOS (CN10)

---

Pin Selection	Function
1-2	Clear
2-3	Protected (Default)

### 2.3.2 ATX/AT Selection (CN14)

---

Pin Selection	Function
1-2	ATX
2-3	AT (Default)



### 2.3.3 COM 1 Ring/+5V/+12V Selection (CN15)

---

Pin Selection	Function
1-2	+5V
3-4	Ring (Default)
5-6	+12V

### 2.3.4 CANBus UART/USB Selection (CN16)

---

Pin Selection	Function
1-2	UART
2-3	USB (Default)

### 2.3.5 CANBus Program Firmware (CN18)

---

Pin Selection	Function
1-2	Protected (Default)
2-3	Program

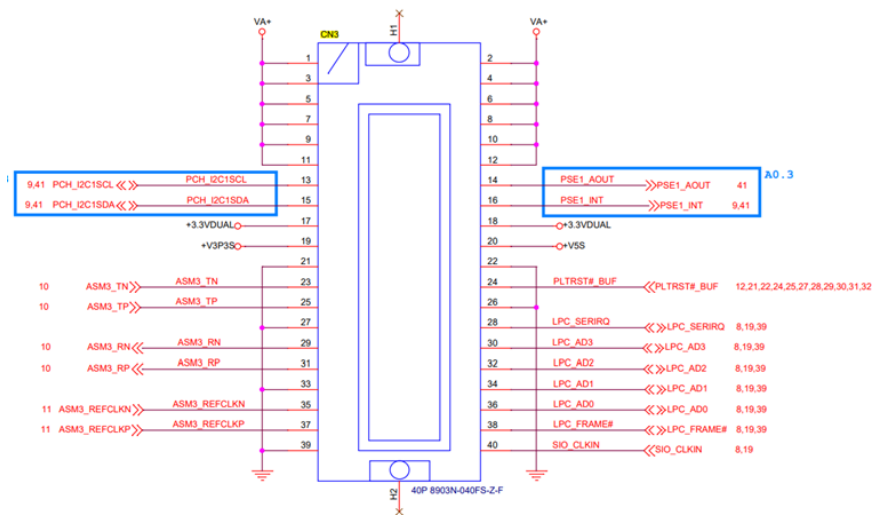
## 2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
AUDIO1	Audio Connector
CN1	USB 3.2 Gen 1 (3 ~ 4) + LAN 2
CN2	USB 3.2 Gen 1 (1 ~ 2) + LAN 1
CN3	Board to Board Connector
CN4	LAN 3 ~ LAN 6 (With PoE Function)
CN5	Front Panel Connector
CN11	Fuse Connector
CN17	SIM Card (With Slot 2)
CN19	Power In & Remote Button
CN20	Digital I/O Connector
CN21	+12V Output
CN22	CANBus 2.0B Connector
CN24	SIM Card (With Slot 3)
COM1	COM 4 RS-232 Serial Port Connector
COM2	COM 3 RS-232 Serial Port Connector
COM3	COM 1/COM 2 RS-232/422/485 Connector
DIMM1	DIMM 2 Slot
DIMM2	DIMM 1 Slot
DP1	Display Port
HDMI1	HDMI
LED1	Mini Card WLED (Slot 1)
LED2	Mini Card WLED (Slot 2)
LED3	Mini Card WLED (Slot 3)

Label	Function
LED4	SATA LED
MSATA1	mSATA Connector (Optional)
SATA1	Primary SATA Connector
SATA2	Secondary SATA Connector
SLOT1	Half Size Mini Card Connector (USB only)
SLOT2	Full Size Mini Card Connector (PCIe + USB)
SLOT3	Full Size Mini Card Connector (USB only)
SW1	Power Button
SW2	Software Reset
SW3	Power On/Off Delay Select
VGA1	CRT Port

## 2.4.1 Board to Board Connector (CN3)



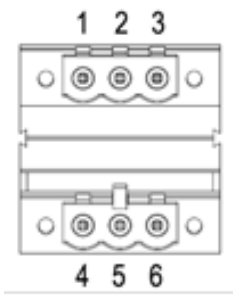
Pin	Signal	Pin	Signal
1	PWR	2	PWR
3	PWR	4	PWR
5	PWR	6	PWR
7	PWR	8	PWR
9	PWR	10	PWR
11	PWR	12	PWR
13	PCH_I2C1SCL	14	PSE1_AOUT
15	PCH_I2C1SDA	16	PSE1_INT
17	+3.3VDUAL	18	+3.3VDUAL
19	+V3P3S	20	+V5S
21	GND	22	GND
23	ASM3_TN	24	PLTRST#_BUF
25	ASM3_TP	26	GND
27	GND	28	LPC_SERIRQ

Pin	Signal	Pin	Signal
29	ASM3_RN	30	LPC_AD3
31	ASM3_RP	32	LPC_AD2
33	GND	34	LPC_AD1
35	ASM3_REFCLKN	36	LPC_AD0
37	ASM3_REFCLKP	38	LPC_FRAME#
39	GND	40	SIO_CLKIN

### 2.4.2 Front Panel Connector (CN5)

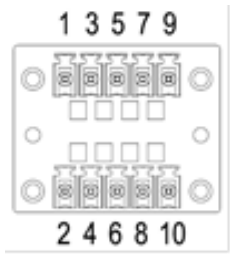
Pin	Signal	Pin	Signal
1	PWR_SW#	2	FPANSWH#
3	GND	4	HWRST#
5	GND	6	FPANSWH#

### 2.4.3 Power In & Remote Button (CN19)



d	Signal	Pin	Signal
1	PWR_IN	2	GND_PRI
3	ACC	4	REMOTE_SW
5	GND	6	PS_ON#

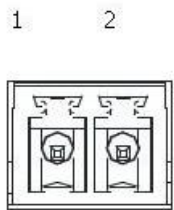
### 2.4.4 Digital I/O Connector (CN20)



Pin	Signal	Pin	Signal
1	GND	2	+GP_V
3	GPI0	4	GPO0
5	GPI1	6	GPO1
7	GPI2	8	GPO2
9	GPI3	10	GPO3

**Mating Connector:** 16522X0003 (Dinkle EC350VM-05P).

### 2.4.5 CAN Bus 2.0B Connector (CN22)



Pin	Signal	Pin	Signal
1	CAN DATA +	2	CAN DATA-

## 2.4.6 COM 4 RS-232 Serial Port Connector (COM1)

---

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

## 2.4.7 COM 3 RS-232 Serial Port Connector (COM2)

---

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

## 2.4.8 COM1 & COM2 RS-232/422/485 Connector (COM3)

---

Pin	Signal	Pin	Signal
1	DCD (RS485 Data-/RS422 TX-)	2	RXD (RS485 Data+/RS422 RX-)
3	TXD (RS422 RX+)	4	DTR (RS422 RX-)
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

## 2.4.9 Power On/Off Delay Select (SW3)

Switch Pin Number	Power On Delay			Time	Power Off Delay			Time
	6	7	8	(Sec)	5	4	3	(Sec)
Control Table	Off	Off	Off	5	Off	Off	Off	180
	Off	Off	ON	10	Off	Off	ON	300
	Off	ON	Off	15	Off	ON	Off	900
	Off	ON	ON	30	Off	ON	ON	1800
	ON	Off	Off	Null	ON	Off	Off	2 Days
	ON	Off	ON	Null	ON	Off	ON	Null
	ON	ON	Off	Null	ON	ON	Off	Null
	ON	ON	ON	Null	ON	ON	ON	Null



## 2.5 2.5" Drive Installation

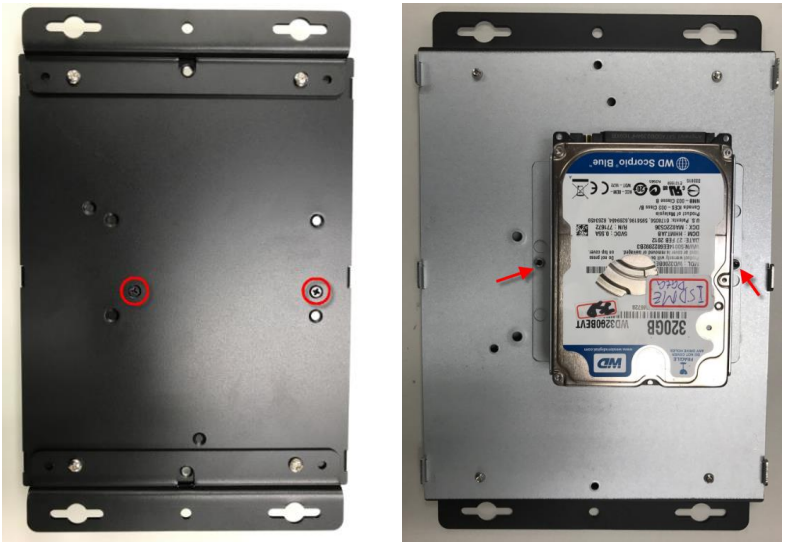
**Step 1:** Loosen the screws and remove the bottom cover.



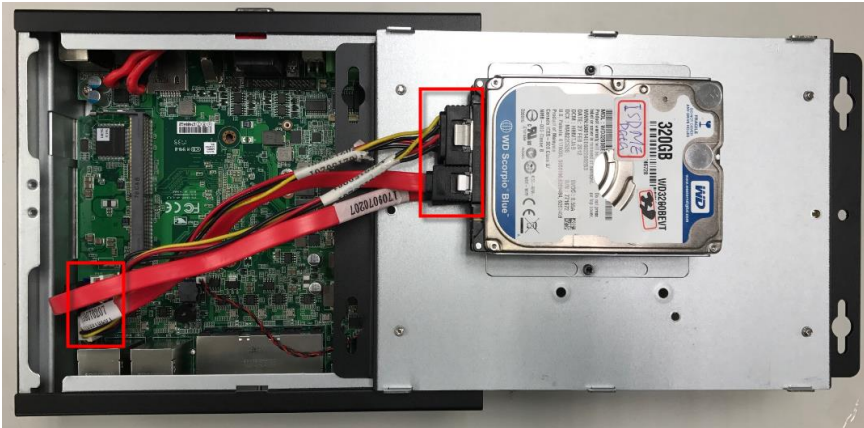
**Step 2:** Attach the brackets to the 2.5" drives. Brackets support up to two drives.



**Step 3:** Install the drive assembly onto the bottom cover.



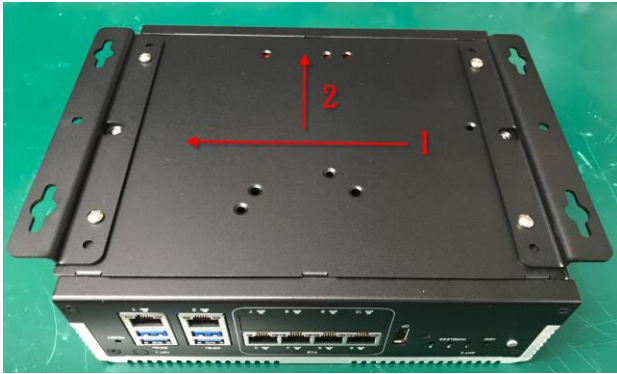
**Step 4:** Attach the cables to the motherboard.



**Step 5:** Replace the bottom cover and tighten the screws.

## 2.6 mSATA Drive Installation

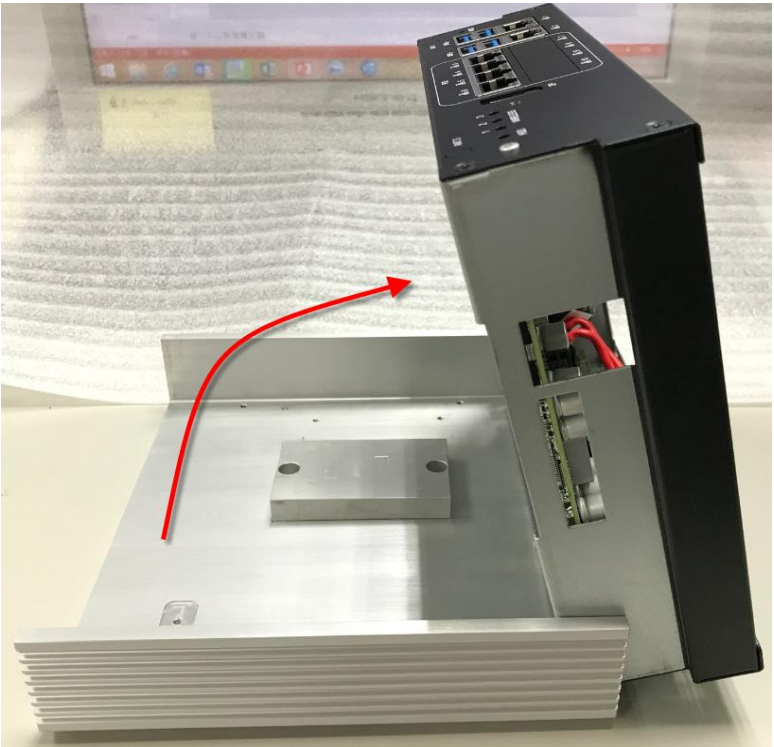
**Step 1:** Loosen the screws and remove the bottom cover



Step 2: Remove the screws from the following six (6) locations.



Step 3: Remove the top cover.





**Step 4:** Install the mSATA drive onto the motherboard and tighten the screw.



**Step 5:** Replace the top cover and tighten the screws.

**Step 6:** Replace the bottom cover and tighten the screws.

## 2.7 GPS & RAM Installation

**Step 1:** Loosen the screws and remove the bottom cover

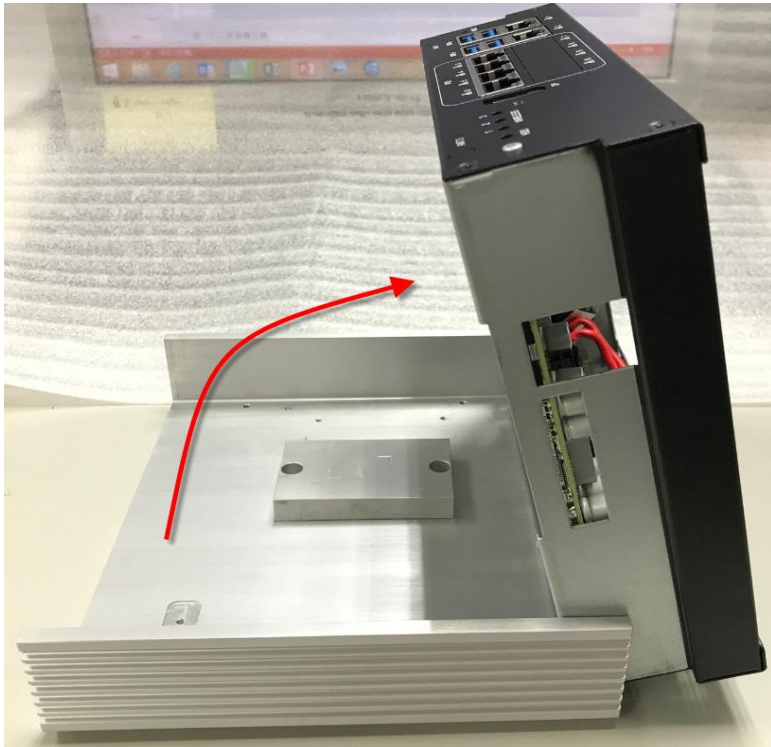


Step 2: Remove the screws from the following six (6) locations.

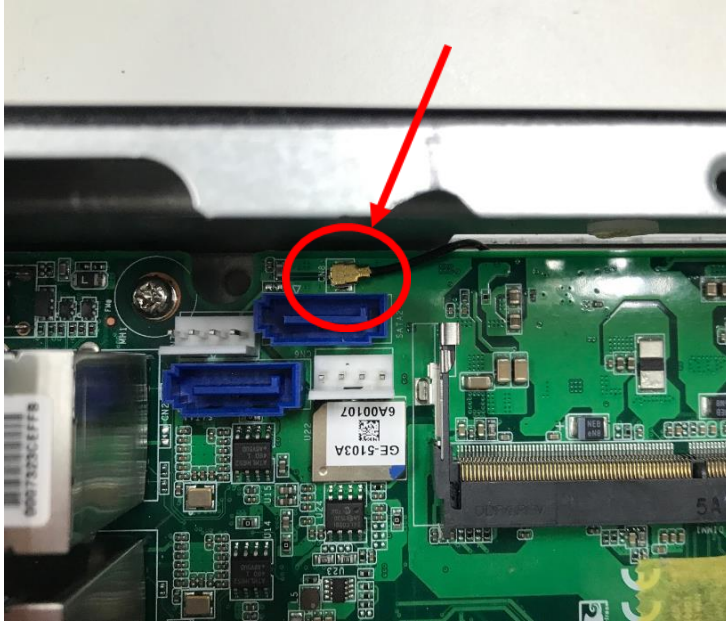




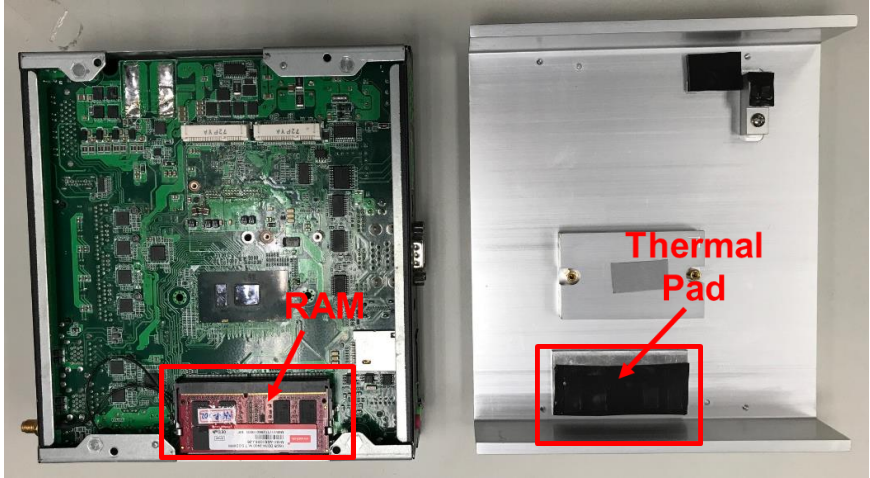
Step 3: Remove the top cover.



Step 4: Install the GPS cable and Wi-Fi antenna connector.



Step 5: Install the RAM and thermal pad.



# Chapter 3

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AMI BIOS Setup

## 3.1 System Test and Initialization

---

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

## 3.2 AMI BIOS Setup

---

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Access and configure advanced processor options and features.

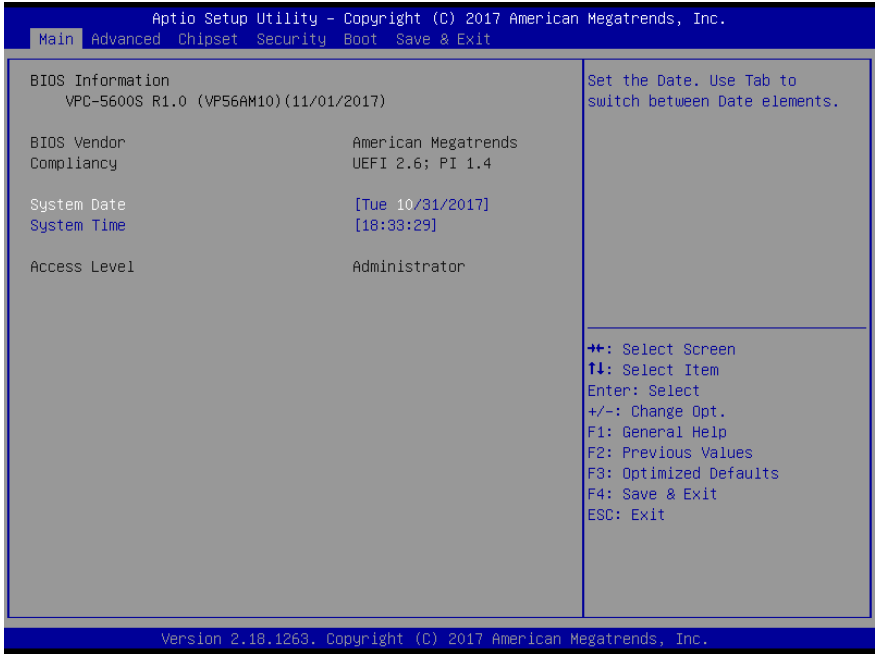
**Chipset** – Chipset and host bridge options and features

**Security** – The setup administrator password can be set here

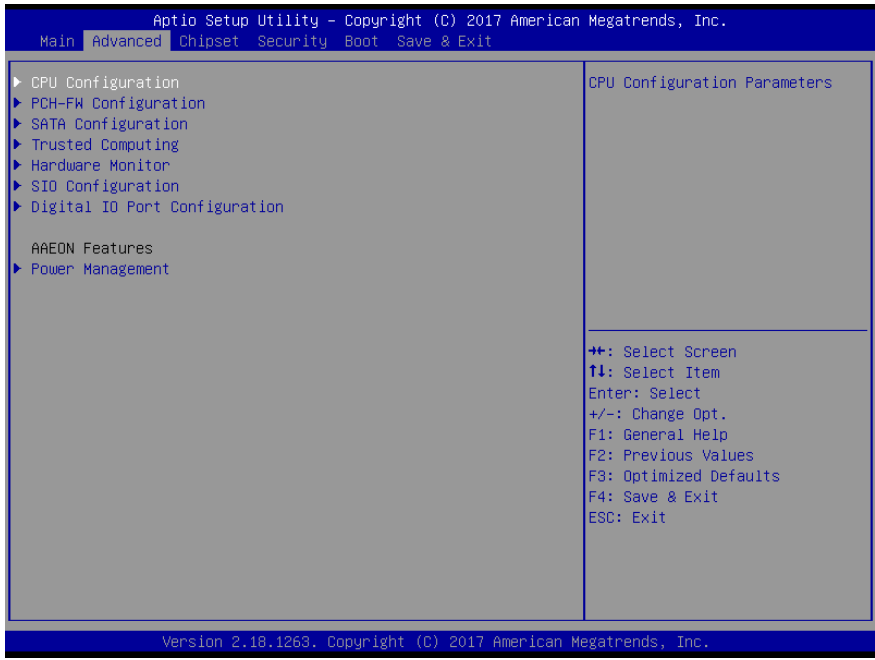
**Boot** – Set boot options including boot priority and Quiet Boot option

**Save & Exit** – Save your changes and exit the program

### 3.3 Setup Submenu: Main



### 3.4 Setup Submenu: Advanced





### 3.4.1 CPU Configuration

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

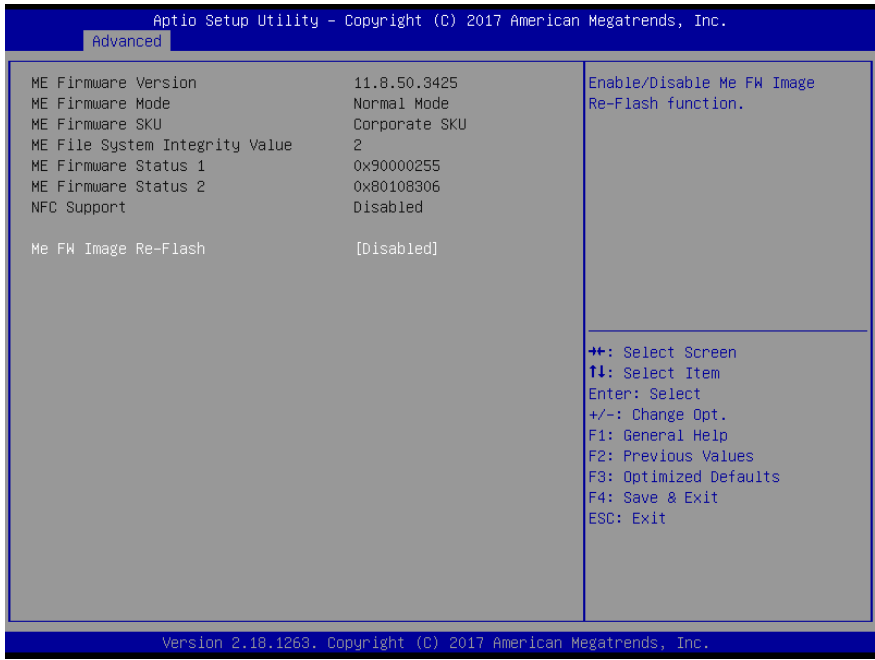
Advanced

CPU Configuration		Number of cores to enable in each processor package.
Type	Intel(R) Core(TM) i3-7100U CPU @ 2.40GHz	
ID	0x806E9	
Speed	2400 MHz	
L1 Data Cache	32 KB x 2	
L1 Instruction Cache	32 KB x 2	
L2 Cache	256 KB x 2	
L3 Cache	3 MB	
L4 Cache	N/A	
VMX	Supported	
SMX/TXT	Not Supported	
Active Processor Cores	[All]	
Hyper-Threading	[Enabled]	
		+*: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Version 2.18.1263. Copyright (C) 2017 American Megatrends, Inc.

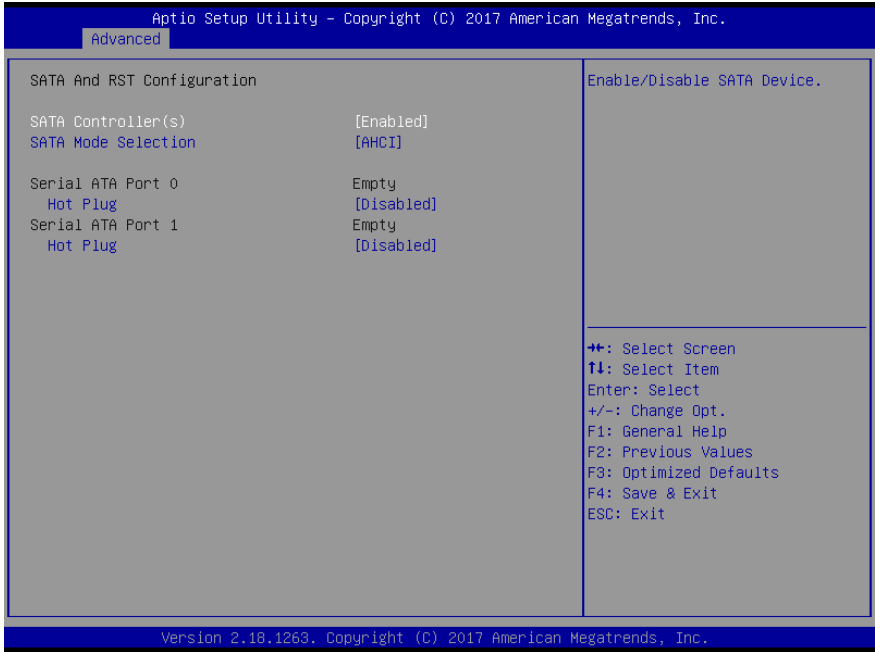
Options Summary	
Active Processor Cores	All 1
Number of cores to enable in each processor package.	
Hyper-Threading	Disabled Enabled
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).	

### 3.4.2 PCH-FW Configuration



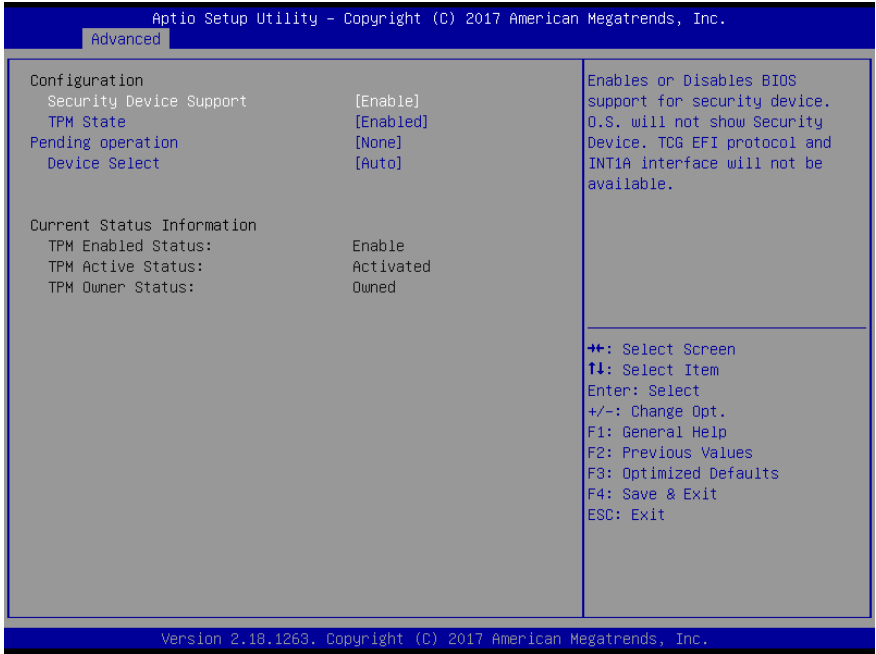
Options Summary	
ME FW Image Re-Flash	Disabled
	Enabled
Enable/Disable Me FW Image Re-Flash function.	

### 3.4.3 SATA Configuration



Options Summary	
SATA Controller(s)	Disabled
	Enabled
Enable/Disable SATA Device.	
Hot Plug	Disabled
	Enabled
Designates this port as Hot Pluggable.	

### 3.4.4 Trusted Computing



Options Summary	
Security Device Support	Disabled
	Enabled
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.	
TPM State	Disabled
	Enabled
Enable/Disable Security Device. <b>NOTE:</b> Your Computer will reboot during restart in order to change State of the Device.	
Pending operation	None
	TPM Clear
Schedule an Operation for the Security Device. <b>NOTE:</b> Your Computer will reboot during restart in order to change State of Security Device.	
Device Select	TPM 1.2
	TPM 2.0
	Auto

## Options Summary

TPM 1.2 will restrict support to TPM 1.2 devices.  
 TPM 2.0 will restrict support to TPM 2.0 devices.  
 Auto will support both with the default set to TPM 2.0 devices if not found.  
 TPM 1.2 devices will be enumerated.

### 3.4.5 Hardware Monitor

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

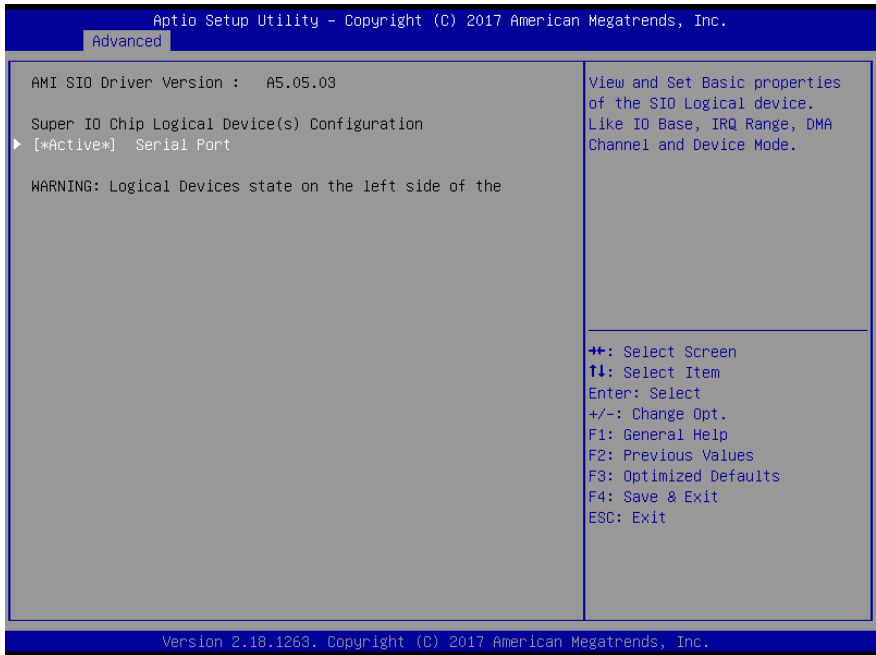
Advanced

CPU Temperature (DTS)	: +100 %
System Temperature	: +52 %
VCORE	: +0.712 V
+1.2V	: +1.232 V
+5V	: +5.045 V
+12V	: +12.232 V
+5VSB	: +5.112 V
+3.3V	: +3.376 V
VBAT	: +3.104 V

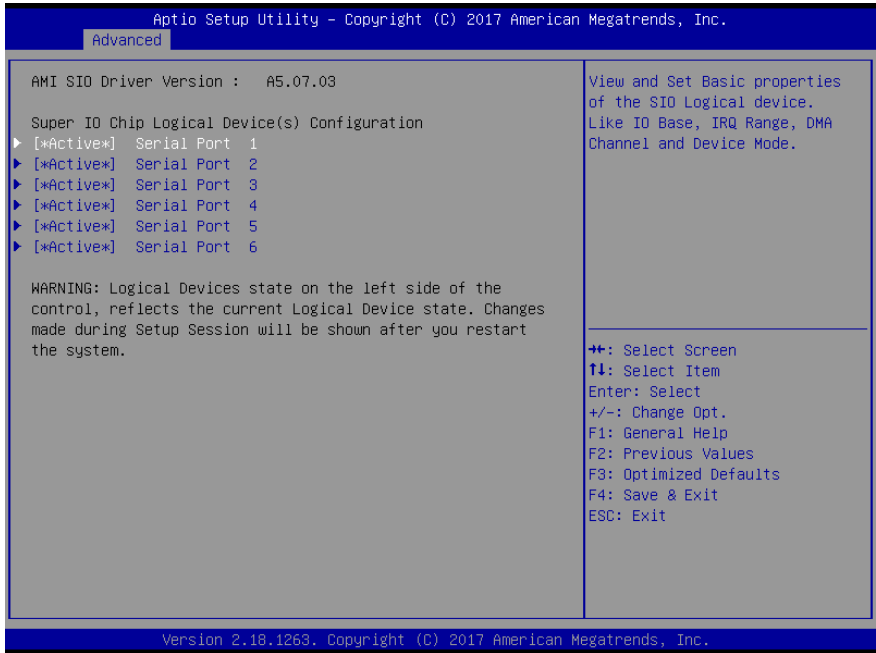
++: Select Screen  
 ↑↓: Select Item  
 Enter: Select  
 +/-: Change Opt.  
 F1: General Help  
 F2: Previous Values  
 F3: Optimized Defaults  
 F4: Save & Exit  
 ESC: Exit

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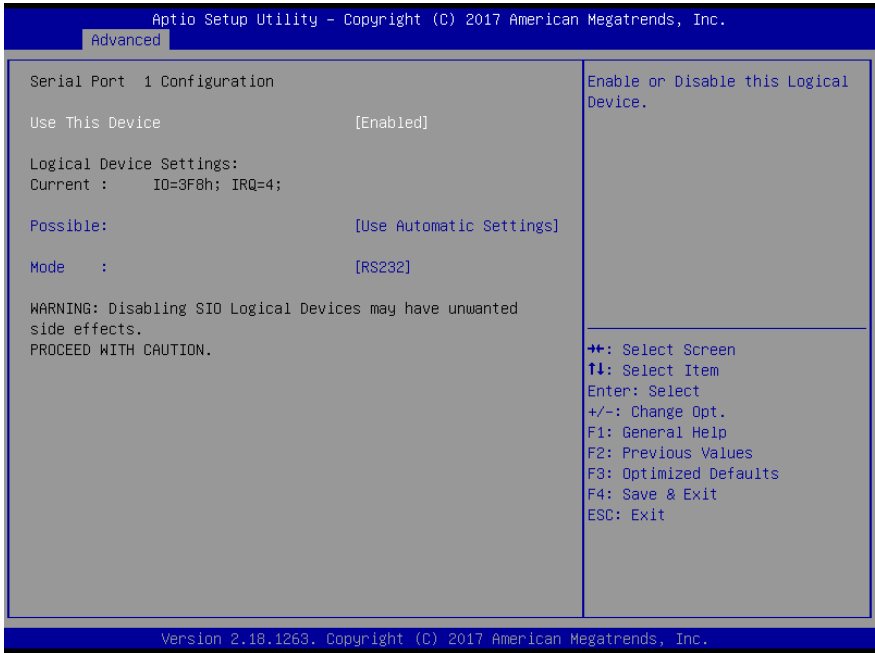
## 3.4.6 SIO Configuration



### 3.4.6.1 Serial Port Configuration



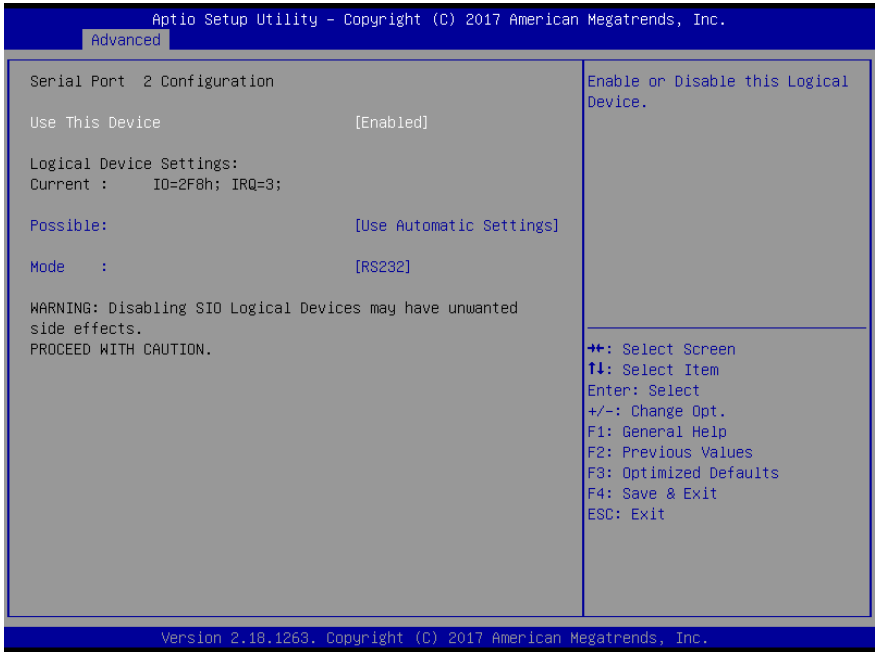
### 3.4.6.2 Serial Port 1 Configuration



Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	
Mode	RS232
	RS422
	RS485
UART RS232, 422, 485 selection.	

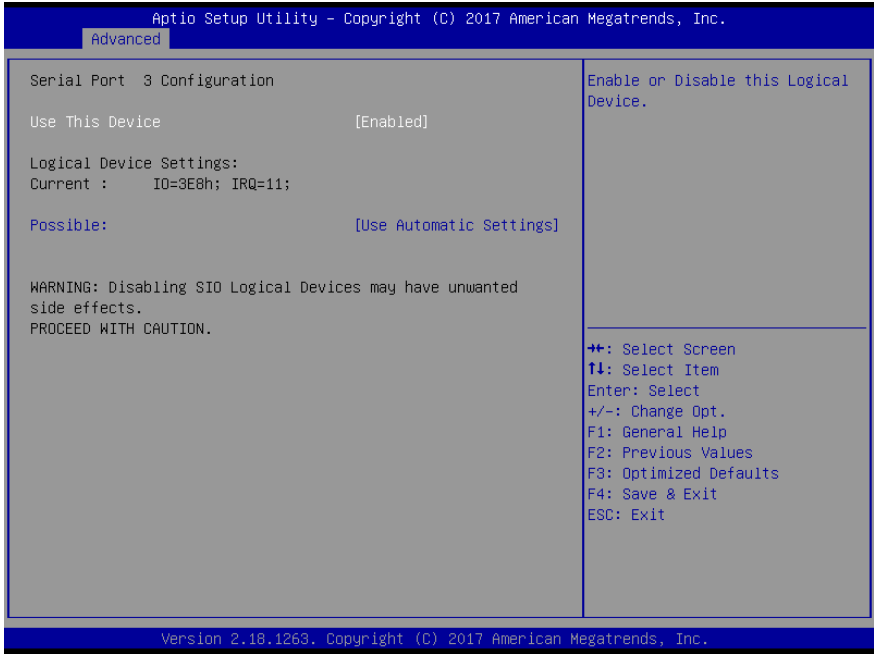


### 3.4.6.3 Serial Port 2 Configuration



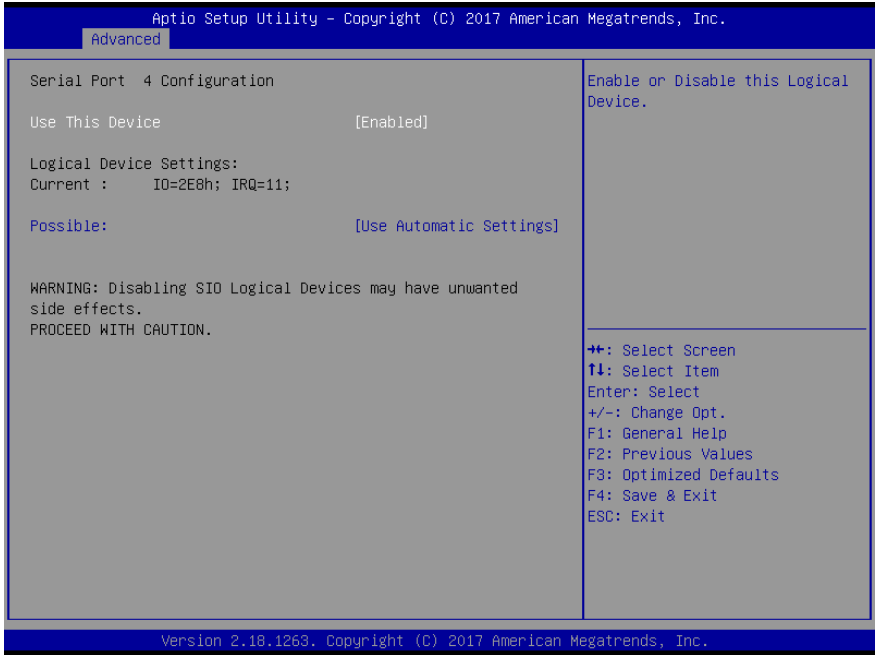
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	
Mode	RS232
	RS422
	RS485
UART RS232, 422, 485 selection.	

### 3.4.6.4 Serial Port 3 Configuration



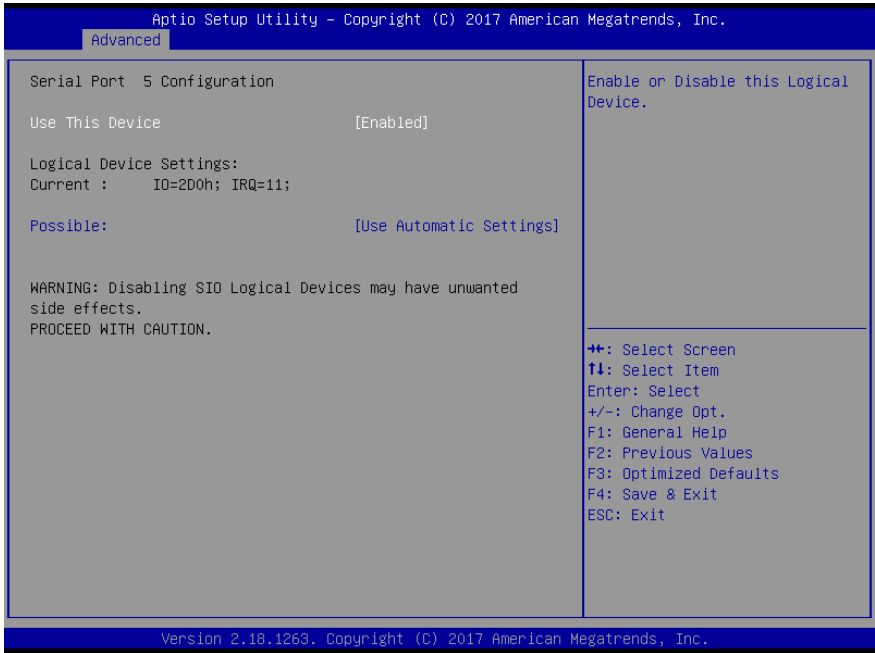
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

### 3.4.6.5 Serial Port 4 Configuration



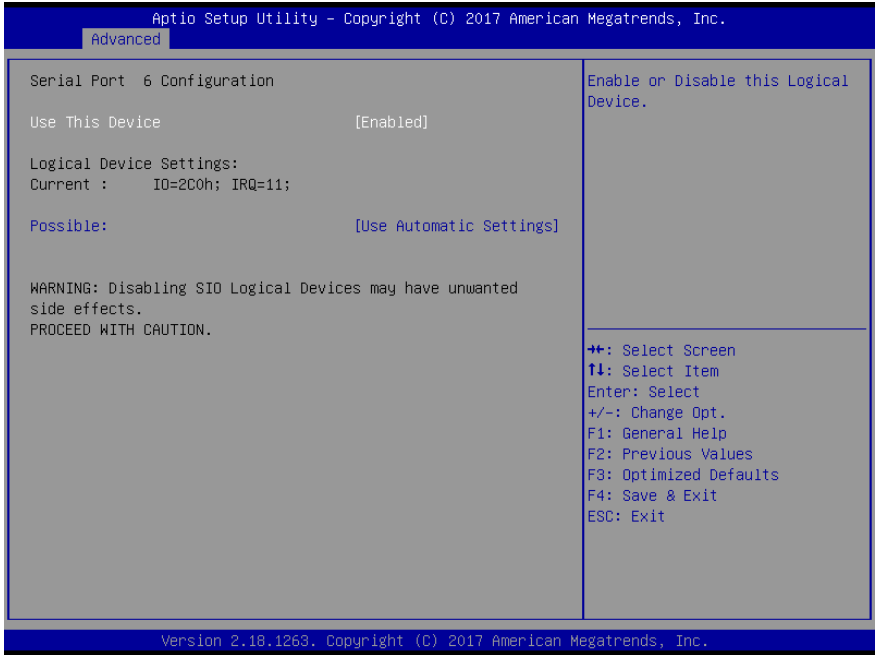
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

### 3.4.6.6 Serial Port 5 Configuration



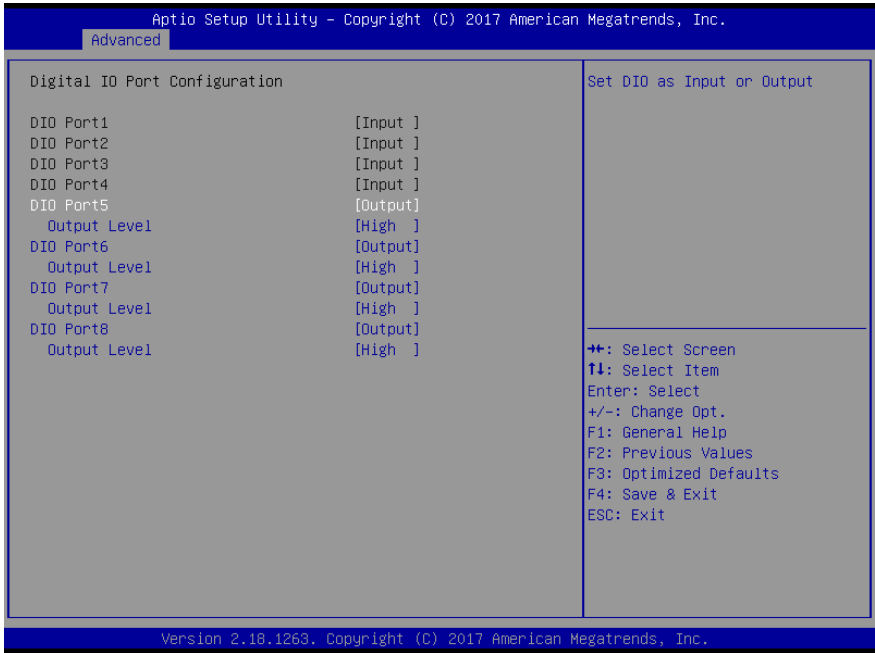
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

### 3.4.6.7 Serial Port 6 Configuration



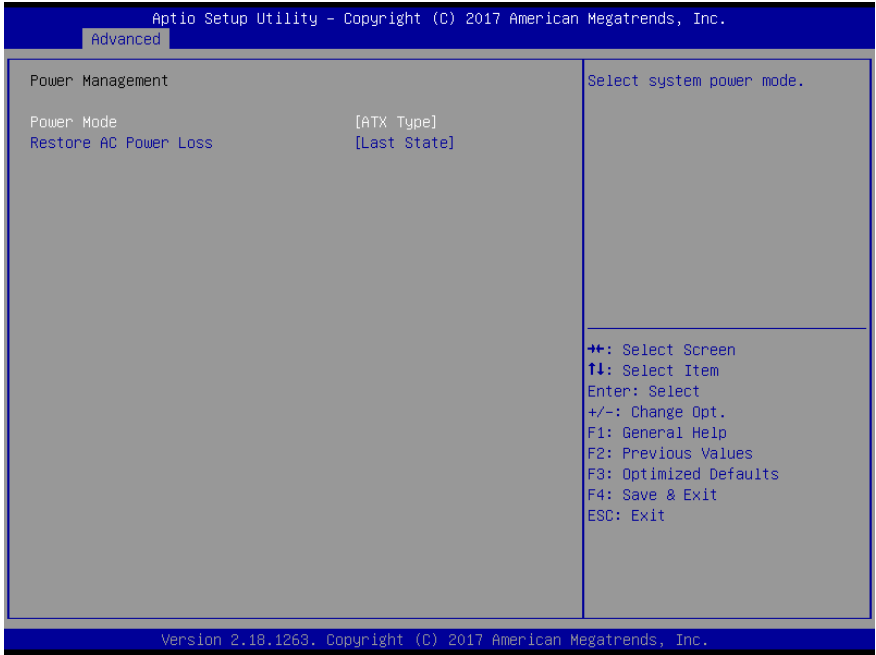
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

### 3.4.7 Digital IO Port Configuration



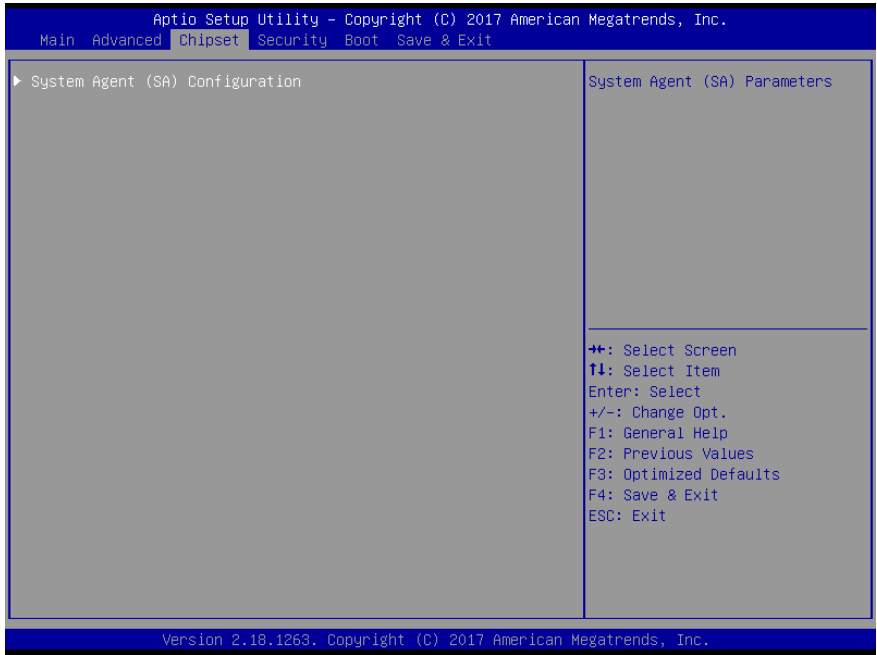
Options Summary	
DIO Port5~8	Output
	Input
Set DIO as Input or Output.	
Output Level	Low
	High
Set output level when DIO pin is output.	

### 3.4.8 Power Management



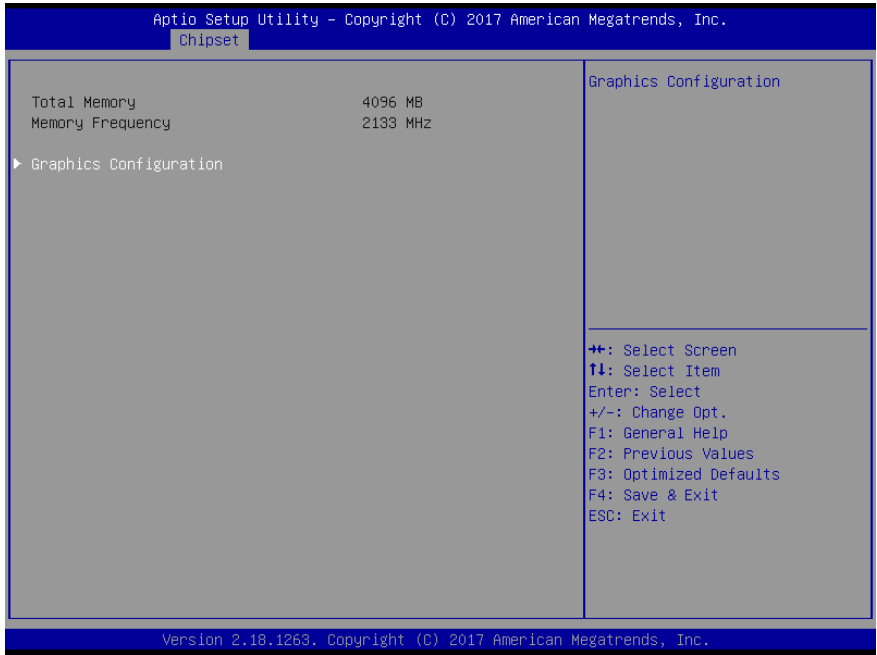
Options Summary	
Power Mode	ATX Type
	AT Type
Select Power Supply Mode.	
Restore AC Power Loss	Power Off
	Power On
	Last State
Select AC power state when power is re-applied after a power failure.	

### 3.5 Setup Submenu: Chipset

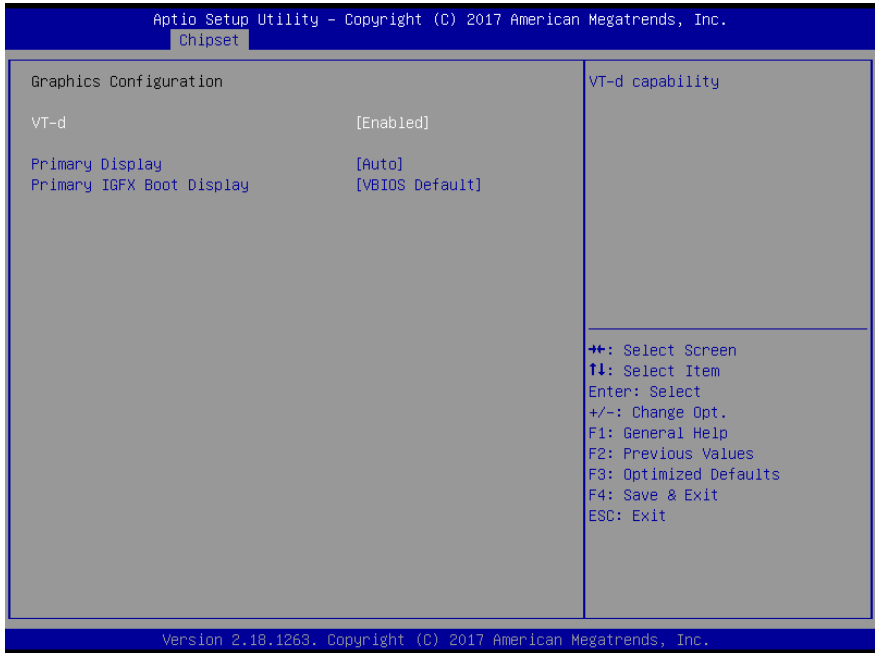




### 3.5.1 System Agent (SA) Configuration

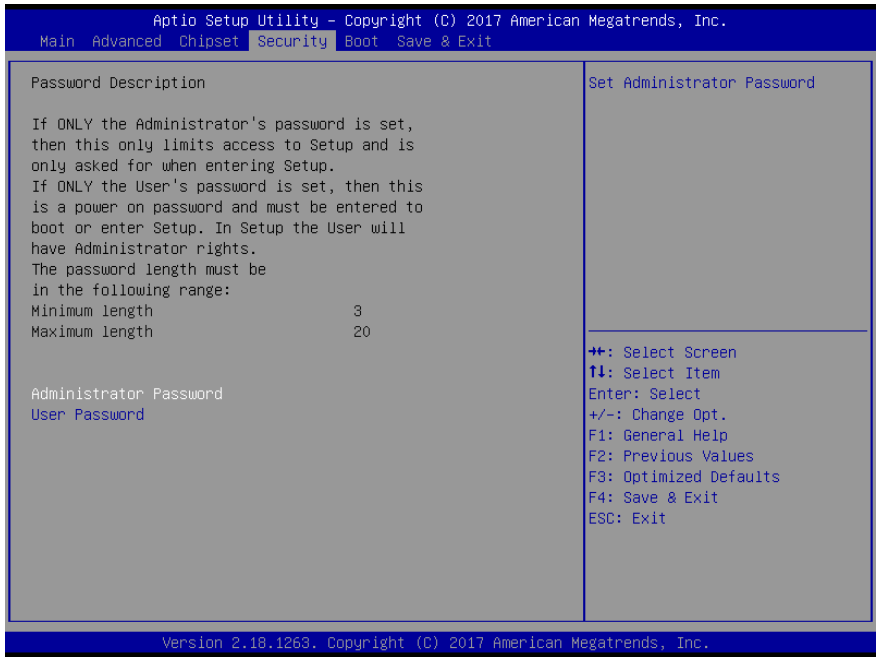


### 3.5.1.1 Graphics Configuration



Options Summary	
VT-d	Enabled
	Disabled
VT-d capability.	
Primary Display	Auto
	IGFX
	PEG
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.	
Primary IGFX Boot Display	VBIOS Default
	HDMI
	DP
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.	

## 3.6 Setup Submenu: Security



### Change User/Administrator Password

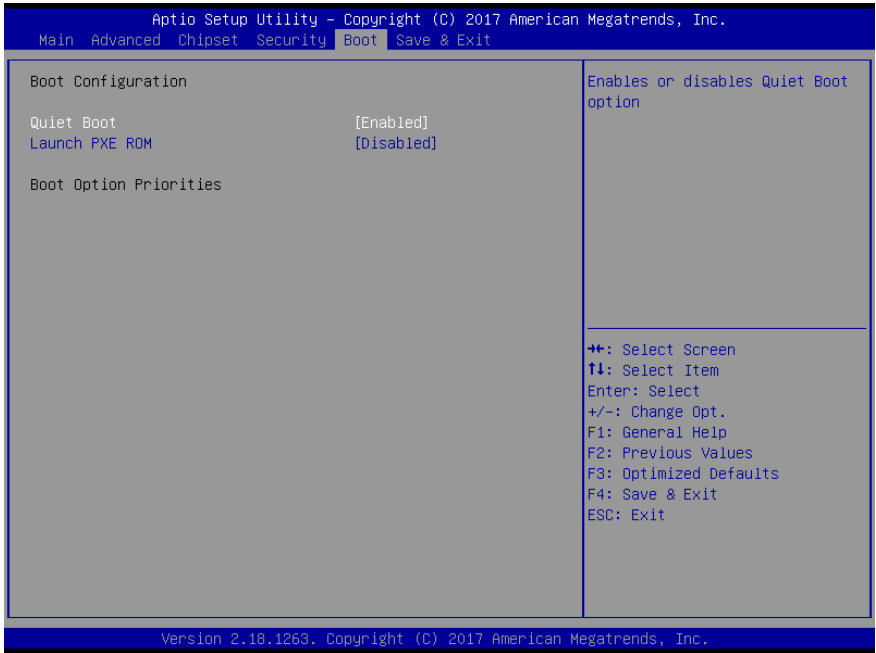
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

### Removing the Password

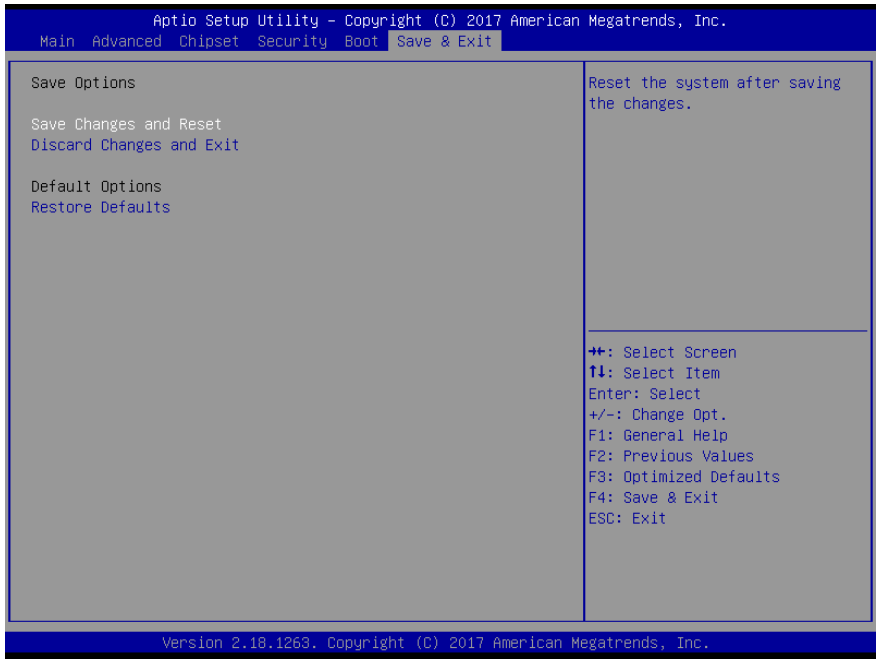
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

### 3.7 Setup Submenu: Boot



Options Summary	
Quiet Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Launch PXE ROM	Disabled
	Enabled
Controls the execution of UEFI and Legacy PXE OpROM	

### 3.8 Setup Submenu: Save & Exit



# Chapter 4

---

Drivers Installation

## 4.1 Driver Download and Installation

---

Drivers for the VPC-5600S can be downloaded from the product page on the AAEMON website by following this link:

<https://www.aaeon.com/en/p/in-vehicle-nvr-vpc-5600s>

Download the driver(s) you need and follow the steps below to install them.

### Install Chipset Drivers

1. Open the **Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

### Install Graphics Driver

1. Open the **Graphic** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Install LAN Drivers

1. Open the **LAN** folder and select your OS
2. Open the **setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Install Audio Driver

1. Open the **Audio** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Install USB 3.0 Driver

1. Open the **USB3.0** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Install ME Driver

1. Open the **ME & TXE** folder followed by **MEISetup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

### Install Serial Port Driver (Optional)

1. Open the **Serial Port Driver (Optional)** folder and select your OS
2. Open the **.exe** or **.bat** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically



# Appendix A

---

## Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

Table 1: SuperIO Relative Register Table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Watchdog Relative Register Table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN  //This parameter is represented from Note9
#define byte   EnableReg  //This parameter is represented from Note10
#define byte   EnableBit  //This parameter is represented from Note11
#define byte   EnableVal  //This parameter is represented from Note12
#define byte   StatusLDN  // This parameter is represented from Note13
#define byte   StatusReg  // This parameter is represented from Note14
#define byte   StatusBit  // This parameter is represented from Note15
#define byte   ModeLDN    // This parameter is represented from Note16
#define byte   ModeReg    // This parameter is represented from Note17
#define byte   ModeBit    // This parameter is represented from Note18
#define byte   ModeVal    // This parameter is represented from Note19
#define byte   WDTRstLDN  // This parameter is represented from Note20
#define byte   WDTRstReg  // This parameter is represented from Note21
#define byte   WDTRstBit  // This parameter is represented from Note22
#define byte   WDTRstVal  // This parameter is represented from Note23
*****

```

```
*****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModelLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID SIOEnterMBPnPMode0{
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIODData, 0x02);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIODData, LDN);
}
*****

```

# Appendix B



---

I/O Information

## B.1 I/O Address Map
























---

### Input/output (IO)

- >  [0000000000000000 - 000000000000CF7] PCI Express Root Complex
- >  [000000000000D00 - 000000000000FFFF] PCI Express Root Complex



## B.2 IRQ Mapping Chart

Interrupt request (IRQ)	
 (ISA) 0x00000000 (00)	System timer
 (ISA) 0x00000003 (03)	Fintek Communications Port (COM2)
 (ISA) 0x00000004 (04)	Fintek Communications Port (COM1)
 (ISA) 0x00000008 (08)	System CMOS/real time clock
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM3)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM4)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM5)
 (ISA) 0x0000000B (11)	Fintek Communications Port (COM6)
 (ISA) 0x0000000E (14)	Motherboard resources
 (PCI) 0x0000000B (11)	Mobile 6th/7th Generation Intel(R) Processor Family I/O Thermal subsystem - 9D31
 (PCI) 0x0000000B (11)	Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
 (PCI) 0x00000010 (16)	High Definition Audio Controller
 (PCI) 0x00000010 (16)	Intel(R) Serial IO I2C Host Controller - 9D60
 (PCI) 0xFFFFFFFF0 (-16)	Intel(R) Management Engine Interface
 (PCI) 0xFFFFFFFF1 (-15)	Realtek PCIe GBE Family Controller
 (PCI) 0xFFFFFFFF2 (-14)	Realtek PCIe GBE Family Controller #2
 (PCI) 0xFFFFFFFF3 (-13)	Realtek PCIe GBE Family Controller #4
 (PCI) 0xFFFFFFFF4 (-12)	Realtek PCIe GBE Family Controller #3
 (PCI) 0xFFFFFFFF5 (-11)	Realtek PCIe GBE Family Controller #6
 (PCI) 0xFFFFFFFF6 (-10)	Realtek PCIe GBE Family Controller #5
 (PCI) 0xFFFFFFFF7 (-9)	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
 (PCI) 0xFFFFFFFF8 (-8)	Intel(R) HD Graphics 620
 (PCI) 0xFFFFFFFF9 (-7)	Standard SATA AHCI Controller
 (PCI) 0xFFFFFFFFFA (-6)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #5 - 9D14
 (PCI) 0xFFFFFFFFFB (-5)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #4 - 9D13
 (PCI) 0xFFFFFFFFFC (-4)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #3 - 9D12
 (PCI) 0xFFFFFFFFFD (-3)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #2 - 9D11
 (PCI) 0xFFFFFFFFFE (-2)	Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #1 - 9D10

# Appendix C

---

Digital I/O Ports

## C.1 Digital I/O Programming

---

VPC-5600S utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

- (1) Enter the MB PnP Mode
- (2) Modify the data of configuration registers
- (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

## C.2 Digital I/O Register

Table 1: SuperIO Relative Register Table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Digital Input Relative Register Table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A(Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A(Note10)	2(Note11)		GPIO82
DIO-4 Pin Status	0x06(Note12)	0x8A(Note13)	3(Note14)		GPIO83
DIO-5 Pin Status	0x06(Note15)	0x8A(Note16)	4(Note17)		GPIO84
DIO-6 Pin Status	0x06(Note18)	0x8A(Note19)	5(Note20)		GPIO85
DIO-7 Pin Status	0x06(Note21)	0x8A(Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A(Note25)	7(Note26)		GPIO87

Table 3: Digital Output Relative Register Table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89(Note32)	1(Note33)	(Note34)	GPIO81
DIO-3 Output Data	0x06(Note35)	0x89(Note36)	2(Note37)	(Note38)	GPIO82
DIO-4 Output Data	0x06(Note39)	0x89(Note40)	3(Note41)	(Note42)	GPIO83
DIO-5 Output Data	0x06(Note43)	0x89(Note44)	4(Note45)	(Note46)	GPIO84
DIO-6 Output Data	0x06(Note47)	0x89(Note48)	5(Note49)	(Note50)	GPIO85
DIO-7 Output Data	0x06(Note51)	0x89(Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89(Note56)	7(Note57)	(Note58)	GPIO87

### C.3 Digital I/O Sample Program

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```

```

*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte DOutput1LDN // This parameter is represented from Note27
#define byte DOutput1Reg // This parameter is represented from Note28
#define byte DOutput1Bit // This parameter is represented from Note29
#define byte DOutput1Val // This parameter is represented from Note30
#define byte DOutput2LDN // This parameter is represented from Note31
#define byte DOutput2Reg // This parameter is represented from Note32
#define byte DOutput2Bit // This parameter is represented from Note33
#define byte DOutput2Val // This parameter is represented from Note34
#define byte DOutput3LDN // This parameter is represented from Note35
#define byte DOutput3Reg // This parameter is represented from Note36
#define byte DOutput3Bit // This parameter is represented from Note37
#define byte DOutput3Val // This parameter is represented from Note38
#define byte DOutput4LDN // This parameter is represented from Note39
#define byte DOutput4Reg // This parameter is represented from Note40
#define byte DOutput4Bit // This parameter is represented from Note41
#define byte DOutput4Val // This parameter is represented from Note42
#define byte DOutput5LDN // This parameter is represented from Note43
#define byte DOutput5Reg // This parameter is represented from Note44
#define byte DOutput5Bit // This parameter is represented from Note45
#define byte DOutput5Val // This parameter is represented from Note46
#define byte DOutput6LDN // This parameter is represented from Note47
#define byte DOutput6Reg // This parameter is represented from Note48
#define byte DOutput6Bit // This parameter is represented from Note49
#define byte DOutput6Val // This parameter is represented from Note50
#define byte DOutput7LDN // This parameter is represented from Note51
#define byte DOutput7Reg // This parameter is represented from Note52
#define byte DOutput7Bit // This parameter is represented from Note53
#define byte DOutput7Val // This parameter is represented from Note54
#define byte DOutput8LDN // This parameter is represented from Note55
#define byte DOutput8Reg // This parameter is represented from Note56
#define byte DOutput8Bit // This parameter is represented from Note57
#define byte DOutput8Val // This parameter is represented from Note58
*****

```

```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean  AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```



```

*****
VOID  SIOEnterMBPnPMode0{
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

```

*****
Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID  ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****

```