VPC-5500S

Mobile NVR

User's Manual 6th Ed

Last Updated: November 4, 2016

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● VPC-5500S	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	○	○	○	○	○	○
外部信号连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	O	O	O	O	O	O
Hard Disk	O	O	O	O	O	O
PSU	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

● CPU		Intel® Core™ i7-4700EQ, up to 3.4 GHz
		Intel® Core™ i5-4400E, up to 3.3 GHz
		Intel® Core™ i3-4100EQ, 2.4 GHz
● Chipset		QM87
● System Memory		DDR3L 1333/1600 SODIMM x 2, up to. 16 GB
● Display Interface	VGA	DB-15 x 1 for VGA
	DP	DP x 1
	HDMI	HDMI x 1
● Storage Device	HDD/SSD	SATA 6.0 Gb/s x 4
	mSATA	mSATA Socket x 1
● Network	LAN	Intel® Gigabit Ethernet x 5
	Wireless	Optional by MiniCard
● Front I/O	USB	USB 3.0 x 4
	LAN	10/100/1000 RJ-45 x 5 (PoE-enabled x 4)
	Others	SIM Socket x 2
		Power On/Off switch
● Rear I/O	USB	USB 2.0 x 2
	HDMI	HDMI x 1
	DisplayPort	DisplayPort x 1
	Audio	Line-out x 1, Mic-in x 1
	Serial Port	DB-9 for RS-232 x 2, DB-9 for
		RS-232/422/485 x 2
	VGA	15-pin D-SUB x 1
	Others	10 - 35 V DC-in, 3-pin terminal block x 1
		(ACC, V-, V+)

		3-pin terminal block for remote power support x 1 DI/O x 1 CAN Bus x 1 (read only)
● Expansion	MiniCard	Full MiniCard x 3 (2 for USB only, 1 full function)
● Indicator		Power LED (Red) x 1 HDD LED (Green) x 1 WLAN LED (Red, for mPCIe) x 3
● Power Requirement		Vehicle power: – Input voltage: 10 ~ 35V DC – Supports Ignition cold crank – Supports Ignition on/off – Supports battery protection – Supports power on/off delay
● Power Consumption		12V@4.46A
● System Cooling		Passive
● Mounting		Wall Mount
● Operating Temperature		-20 ~ 70°C (-4 ~ 158°F) with 0.5 m/s Airflow
● Storage Temperature		-40 ~ 85°C (-40 ~ 185°F)
● Anti-Vibration		3 G_{rms}/ 5~500 Hz/ operation - mSATA 1 G_{rms}/ 5~500 Hz/ operation - SSD
● Anti-Shock		50G peak acceleration (11 msec. duration) - mSATA 20G peak acceleration (11 msec. duration) - SSD
● Certification	EMC	E-Mark E13
● OS Support		Windows® 7

Windows® 8.1

Windows® Embedded Standard 7

Windows® Embedded Standard 8

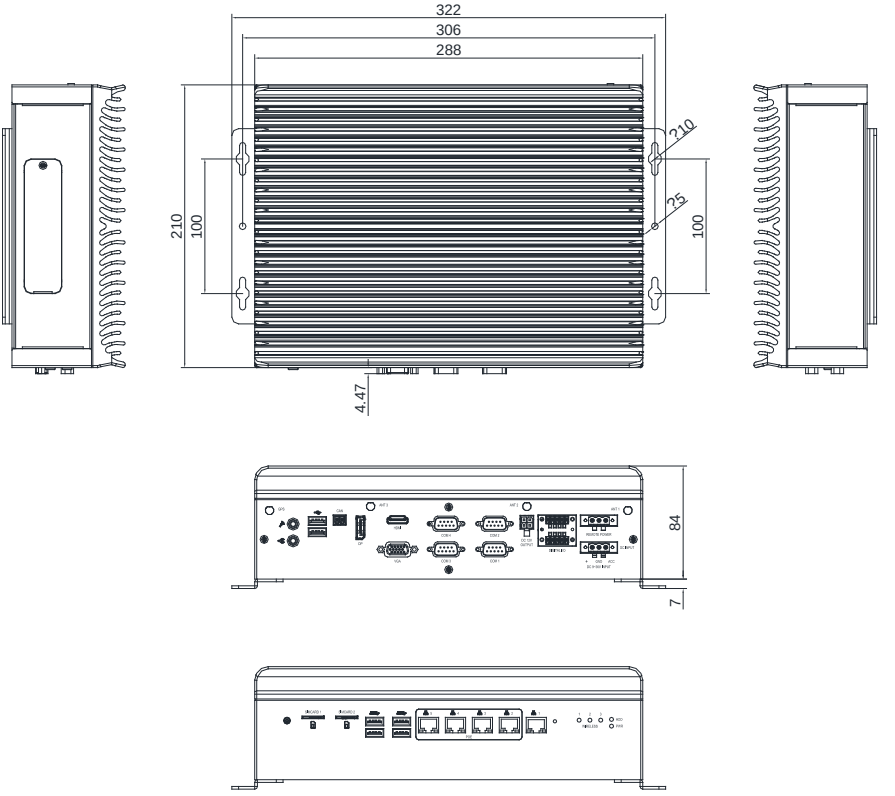
Linux by Fedora

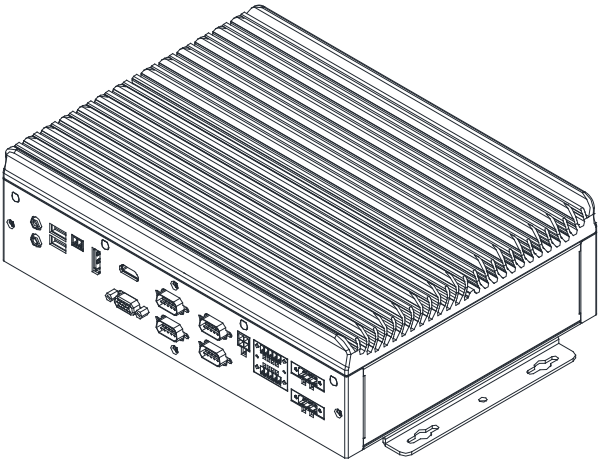
Chapter 2

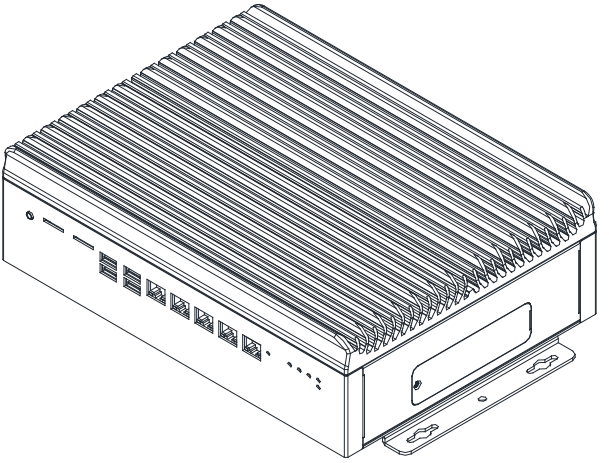
Hardware Information

2.1 Dimensions

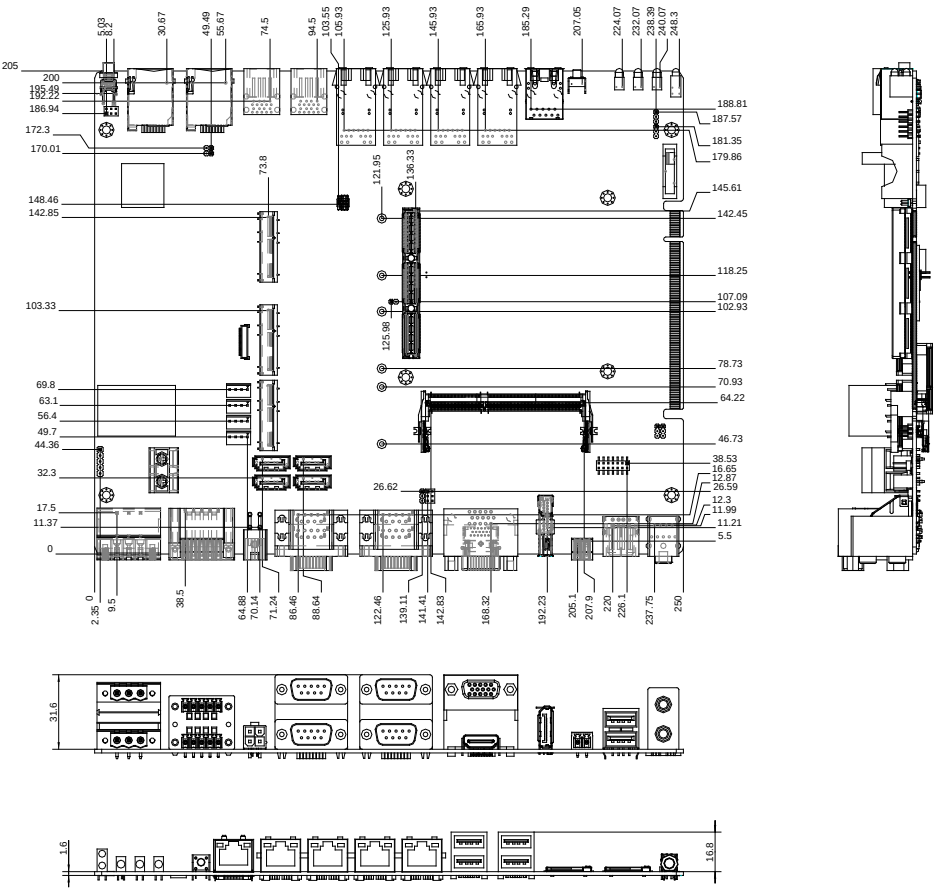
Chassis

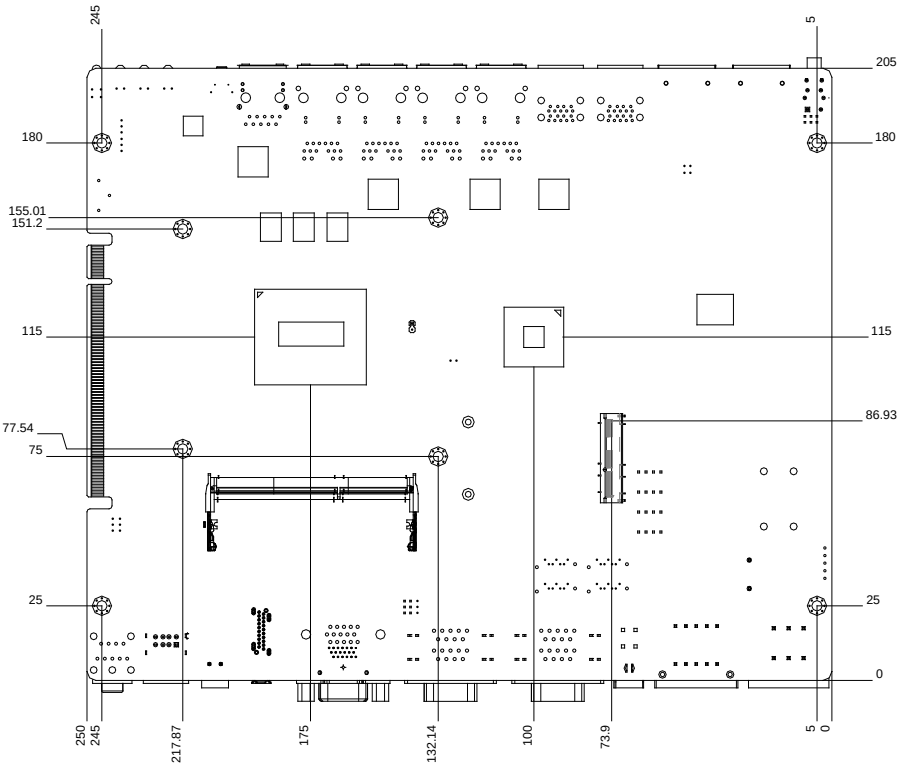






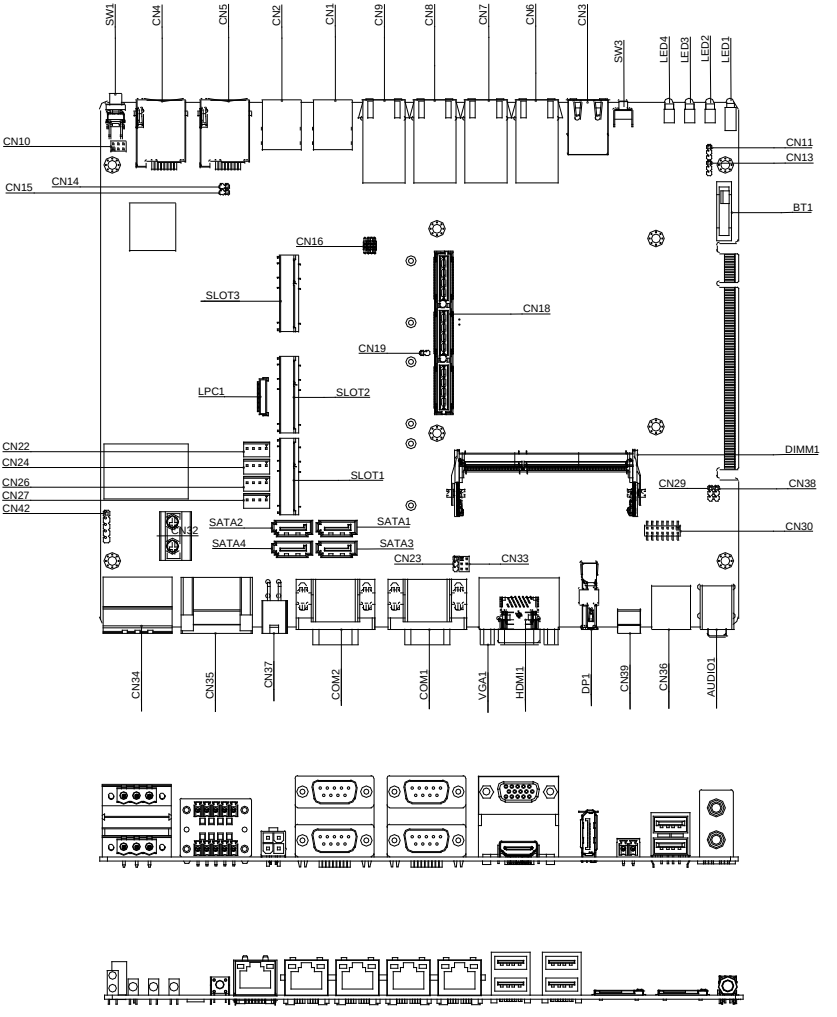
Board

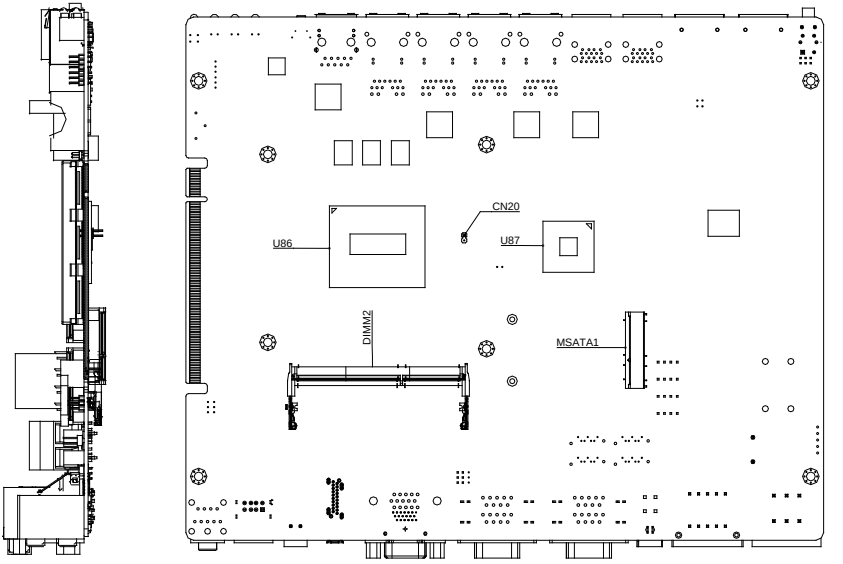

5.03
8.2
30.67
49.49
55.67
74.5
94.5
103.55
105.93
125.93
145.93
165.93
185.29
207.05
224.07
232.07
238.39
240.07
248.3
205
200
195.49
192.22
186.94
172.3
170.01
148.46
142.85
103.33
69.8
63.1
56.4
49.7
44.36
32.3
17.5
11.37
0
73.8
121.95
136.33
125.98
188.81
187.57
181.35
179.86
145.61
142.45
118.25
107.09
102.93
78.73
70.93
64.22
46.73
38.53
16.65
12.87
26.59
12.3
11.99
11.21
5.5
26.62
0
2.35
9.5
38.5
64.88
70.14
71.24
86.46
88.64
122.46
139.11
141.41
142.83
168.32
192.23
205.1
207.9
220
226.1
237.75
250
31.6
1.6
16.8



Note: Height of the cooler may vary depending on the customer's setup

2.2 Jumpers and Connectors




CN20
U86
U87
DIMM2
MSATA1

2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN11	Clear CMOS
CN13	RTC TEST
CN10	Front Plane
CN23	AT/ATX
CN33	COM3 RI Select

2.3.1 Clear CMOS Selection (CN11/CN13)

Pin (CN11/CN13)	Function
1-2 / 1-2	Default
2-3 / 2-3	Clear CMOS

2.3.2 Auto Power Button Selection (CN23)

Pin	Function
1-2	Default (ATX for Box PC)
2-3	Auto PWRBTN (AT for Box PC)

2.3.3 RI# Selection (CN33)

Pin	Function
1-2	5 V
3-4	RI (Default)
5-6	12 V

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

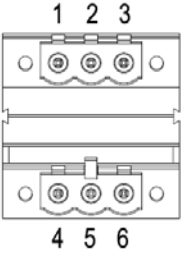
Label	Function
SW1	Power Button
CN10	Front Plane
CN4	SIM Card(With SLOT3)
CN5	SIM Card(With SLOT2)
CN6	LAN2(With POE Function)
CN7	LAN3(With POE Function)
CN8	LAN4(With POE Function)
CN9	LAN5(With POE Function)
CN2	USB3.0 Con
CN1	USB3.0 Con
CN3	LAN1
SW3	Software Reset
LED2~LED4	Mini Card WLED (SLOT1 w/LED2,SLOT2 w/LED3,SLOT3 w/LED4)
CN11	Clear CMOS
CN13	RTC TEST
BT1	BAT CON
CN40	PCIEx16 Slot (Non-standard)
CN18	PCIE104
SLOT1	Mini Card(only USB)
SLOT2	Mini Card(PCIE+USB)
SLOT3	Mini Card(only USB)
CN21	FAN CON

CN22.24.26.27	Small 4P Power
SATA1.2.3.4	SATA3 Con
DIMM1.2	DDR3L SODIMM
SW4	Power on/off delay select
AUDIO1	AUDIO Con (Front + MIC)
CN36	USB2.0 Con
CN39	CAN Bus Con
DP1	Display Port
VGA1	CRT Port
HDMI1	HDMI
CN23	AT/ATX
CN33	COM3 RI Select
COM1	COM3+COM4
COM2	COM1+COM2
CN37	+12V Output
CN35	DIO
CN34	POWER IN & Remote Button
CN32	Fuse Con
MSATA1	Msata Con

2.4.1 Front Plane Connector (CN10)

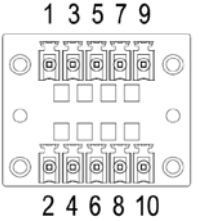
Pin	Signal	Pin	Signal
1	PWR_SW#	2	FPANSWH#
3	GND	4	HWRST#
5	GND	6	FPANSWH#

2.4.2 Power Input & Remote Button (CN34)



Pin	Signal	Pin	Signal
1	ACC	2	GND_PRI
3	PWR_IN	4	REMOTE_SW
5	GND	6	PS_ON#

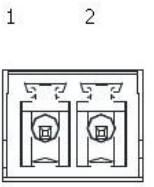
2.4.3 Digital I/O (CN35)



Pin	Signal	Pin	Signal
1	GND	2	+GP_V
3	GPI0	4	GPO0

5	GPI1	6	GPO1
7	GPI2	8	GPO2
9	GPI3	10	GPO3

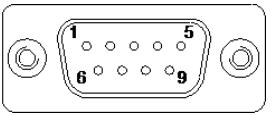
2.4.4 CAN Bus Connector (CN39)



Pin	Signal	Pin	Signal
1	CANH	2	CANL

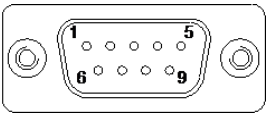
Mating Connector: DINKLE EC381V-02P

2.4.5 COM3 + COM4 (COM1) (RS232 / RS485 / RS422)



Pin	Signal	Pin	Signal
1	DCD(RS485 Data+/RS422 TX+)	2	RXD(RS422 RX-)
3	TXD(RS485 Data-/RS422 TX-)	4	DTR(RS422 RX+)
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

2.4.6 COM1 + COM2 (COM2)



Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	

2.5 Switch Pin Table

	Power on Delay			Sec	Power off Delay			Sec
SWITCH Pin Number	6	7	8		5	4	3	
Control Table	off	off	off	5	off	off	off	180
	off	off	on	10	off	off	on	300
	off	on	off	15	off	on	off	900
	off	on	on	30	off	on	on	1800
	on	off	off	Null	on	off	off	2Day
	on	off	on	Null	on	off	on	Null
	on	on	off	Null	on	on	off	Null
	on	on	on	Null	on	on	on	Null

2.6 2.5" HDD Installation

1. Remove the top cover

2. Loosen the screw on the HDD cover to remove it.

3. Attach the cushions to the HDD.

4. Place the HDD onto the tray and connect the SATA and power cable

5. Cover up the tray and make sure the flutes of the cover rests on the cushions

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

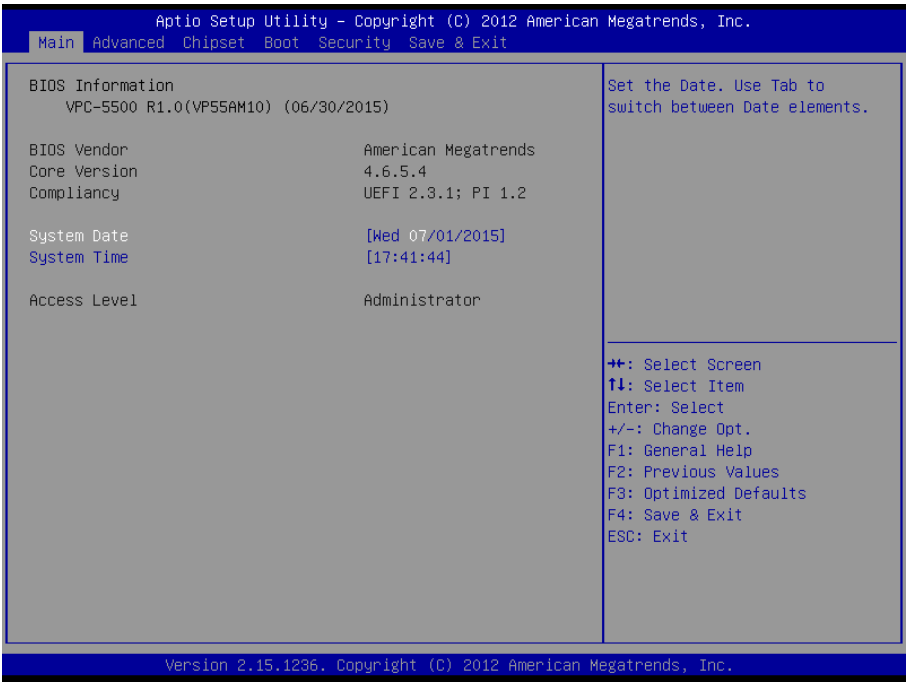
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

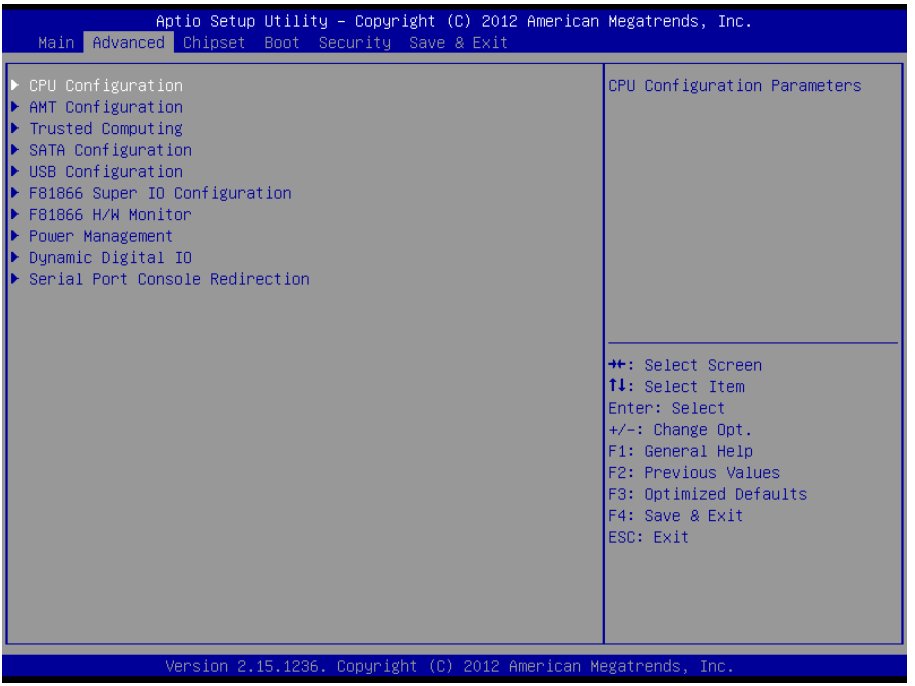
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

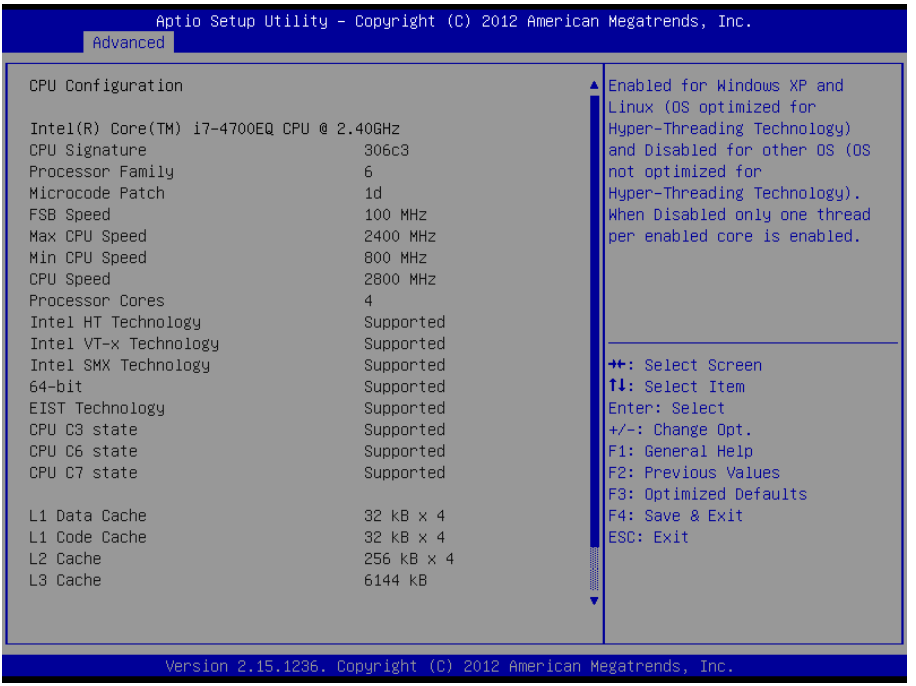
3.3 Setup submenu: Main



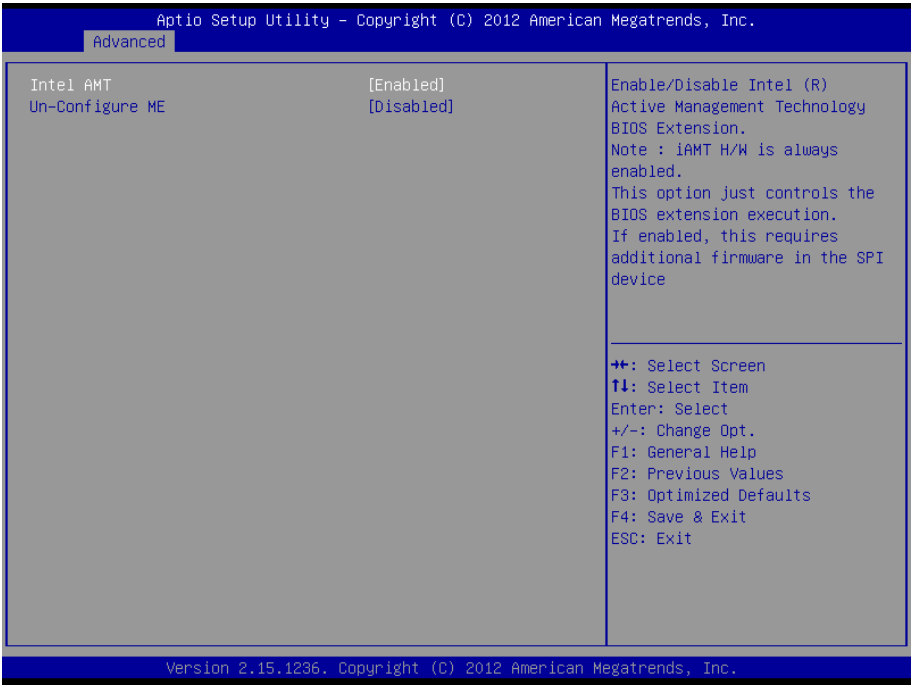
3.4 Setup submenu: Advanced



3.4.1 Advanced: CPU Configuration



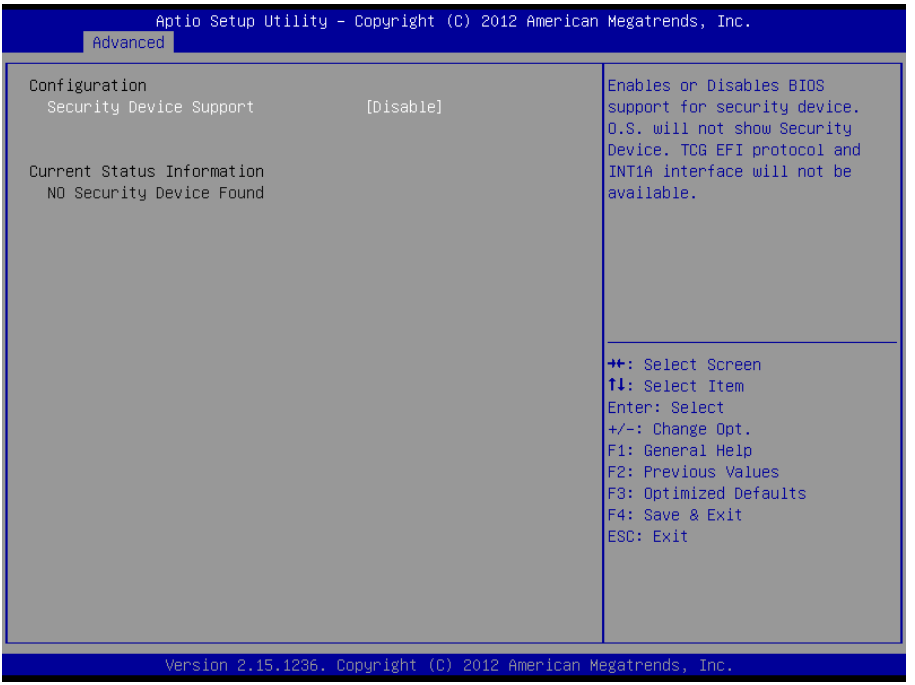
3.4.2 Advanced: AMT Configuration



Options summary:

Intel AMT	Enable	Optimal Default, Failsafe Default
	Disable	
Enable/Disable Intel (R) Active Management Technology BIOS Extension. Note : iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device		
Un-Configure ME	Disable	Optimal Default, Failsafe Default
	Enable	
OEMFlag Bit 15:Un-Configure ME without password.		

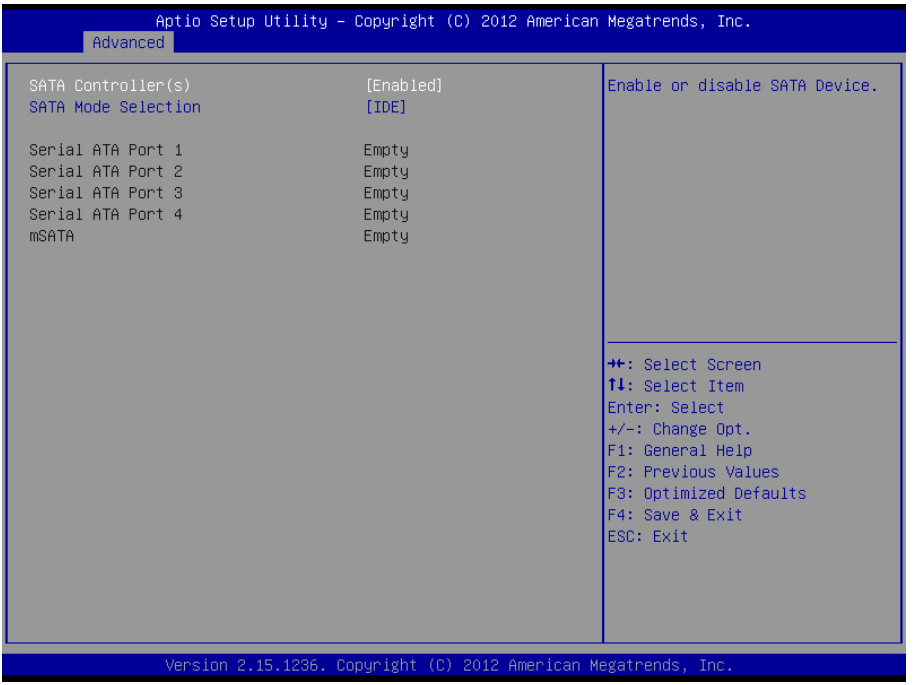
3.4.3 Advanced: Trusted Computing



Options summary:

Security Device Support	Enable	Optimal Default, Failsafe Default
	Disable	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		

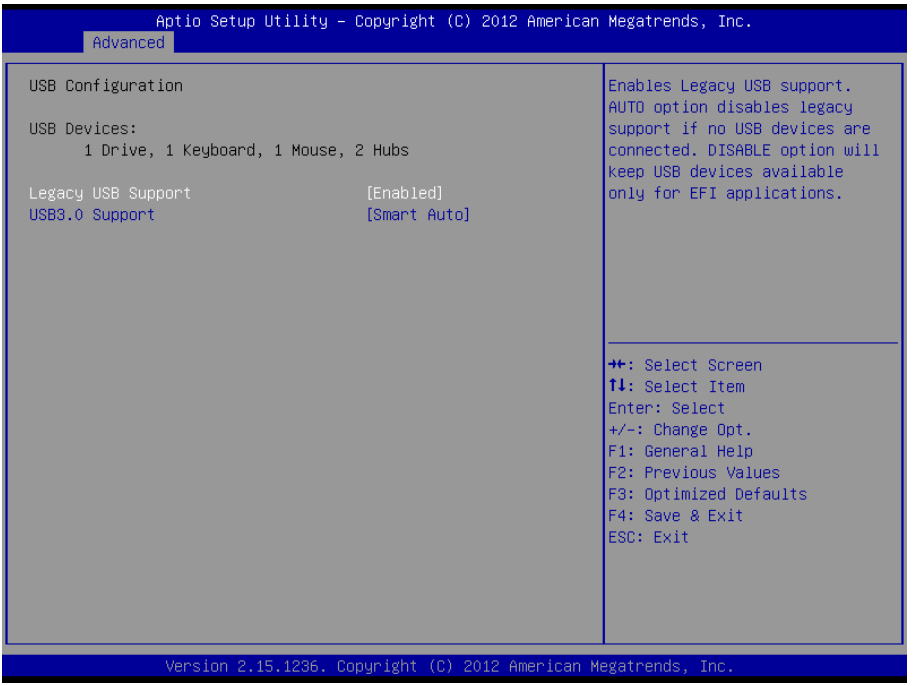
3.4.4 Advanced: SATA Configuration



Options summary:

SATA Controller(s)	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or disable SATA Device.		
SATA Mode Selection	IDE	Optimal Default, Failsafe Default
	AHCI	
Determines how SATA controller(s) operate.		

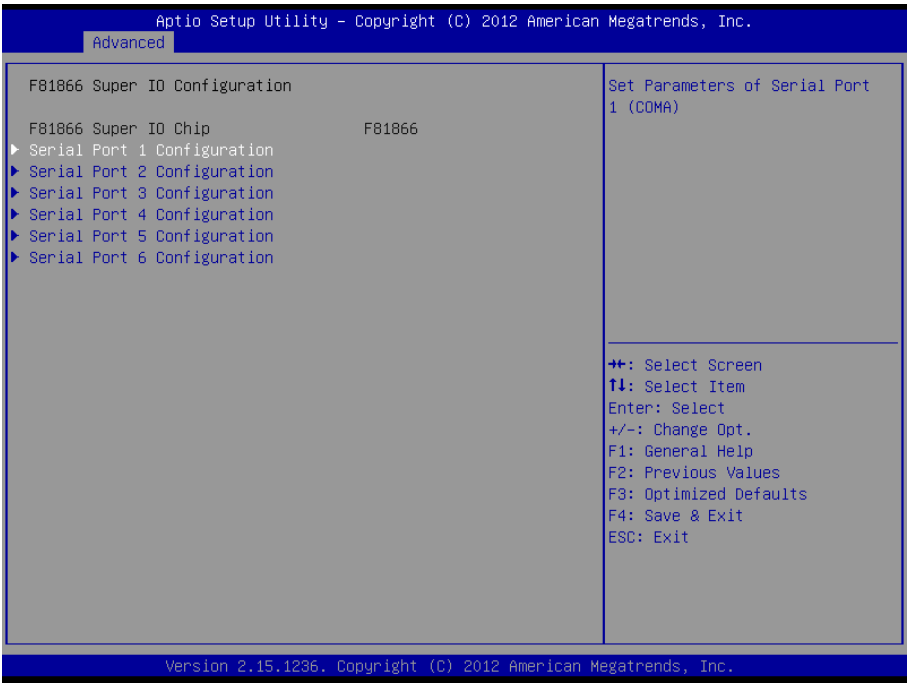
3.4.5 Advanced: USB Configuration



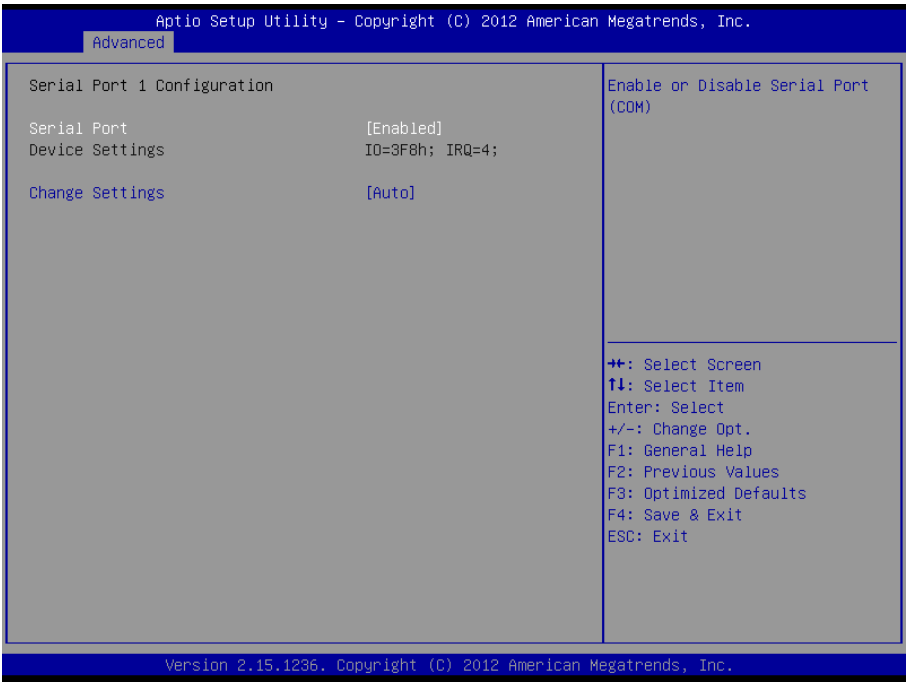
Options summary:

Legacy USB Support	Enable	Optimal Default, Failsafe Default
	Disable	
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		
USB3.0 Support	Smart Auto	Optimal Default, Failsafe Default
	Enabled	
	Disable	
Enable/Disable USB3.0 (XHCI) Controller support.		

3.4.6 Advanced: F81666 Super IO Configuration



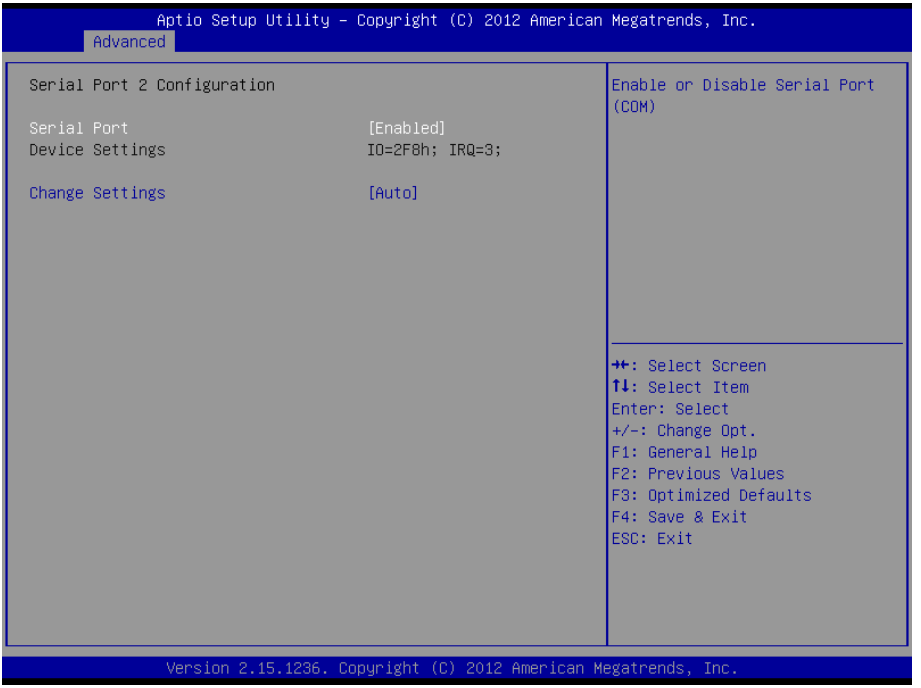
3.4.6.1 F81666 Super IO Configuration: Serial Port 1 Configuration



Options summary:

Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12; IO=2F8h; IRQ=3,4,5,6,7,10,11,12; IO=3E8h; IRQ=10; IO=2E8h; IRQ=10;	
Select an optimal setting for Super I/O device.		

3.4.6.2 F81666 Super IO Configuration: Serial Port 2 Configuration



Options summary:

Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3; IO=3F8h; IRQ=3,4; IO=2F8h; IRQ=3,4; IO=3E8h; IRQ=3,4; IO=2E8h; IRQ=3,4;	
Select an optimal setting for Super I/O device.		

3.4.6.3 F81666 Super IO Configuration: Serial Port 3 Configuration

Options summary:

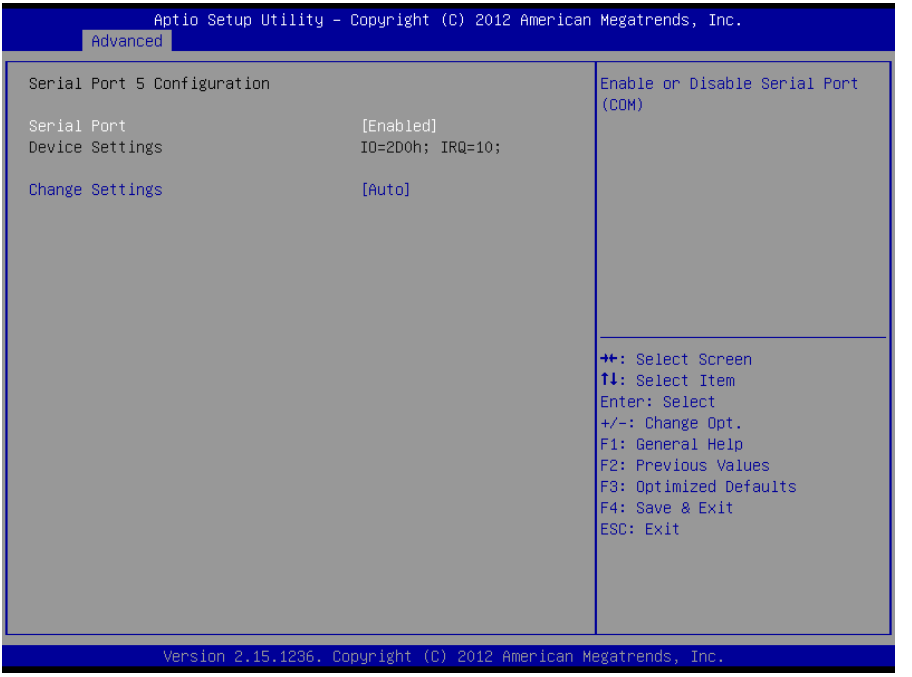
Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=10; IO=3E8h; IRQ=10; IO=2E8h; IRQ=10; IO=2D0h; IRQ=10; IO=2C0h; IRQ=10;	
Select an optimal setting for Super I/O device.		
Serial Port Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
Serial Port Mode selection. For switch RS232/422/485 mode		

3.4.6.4 F81666 Super IO Configuration: Serial Port 4 Configuration

Options summary:

Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=10; IO=3E8h; IRQ=10; IO=2E8h; IRQ=10; IO=2D0h; IRQ=10; IO=2C0h; IRQ=10;	
Select an optimal setting for Super I/O device.		
Serial Port Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
Serial Port Mode selection. For switch RS232/422/485 mode		

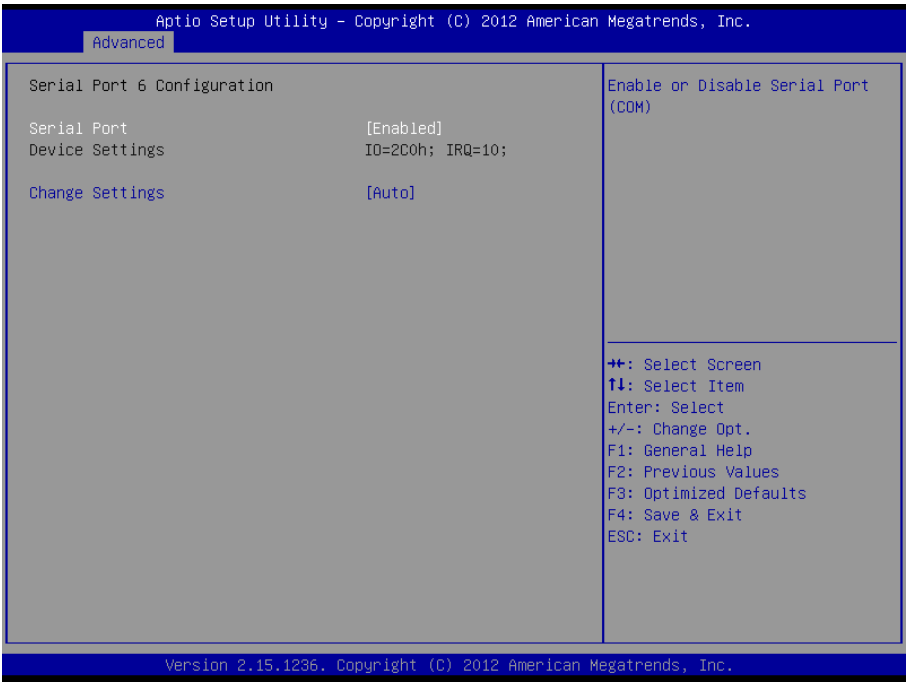
3.4.6.5 F81666 Super IO Configuration: Serial Port 5 Configuration



Options summary: (*default setting*)

Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=2F0h; IRQ=10; IO=3E8h; IRQ=10; IO=2E8h; IRQ=10; IO=2D0h; IRQ=10; IO=2C0h; IRQ=10;	
Serial Port Mode selection. For switch RS232/422/485 mode		

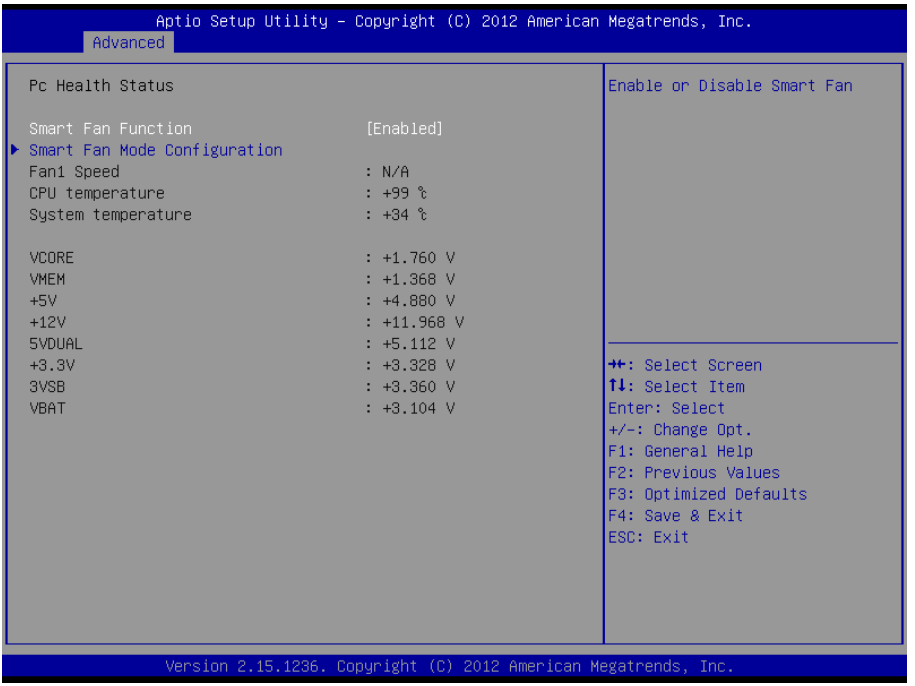
3.4.6.6 F81666 Super IO Configuration: Serial Port 6 Configuration



Options summary:

Serial Port	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Serial Port(COM)		
Change Settings	Auto	Optimal Default, Failsafe Default
	IO=2F0h; IRQ=10; IO=3E8h; IRQ=10; IO=2E8h; IRQ=10; IO=2D0h; IRQ=10; IO=2C0h; IRQ=10;	
Serial Port Mode selection. For switch RS232/422/485 mode		

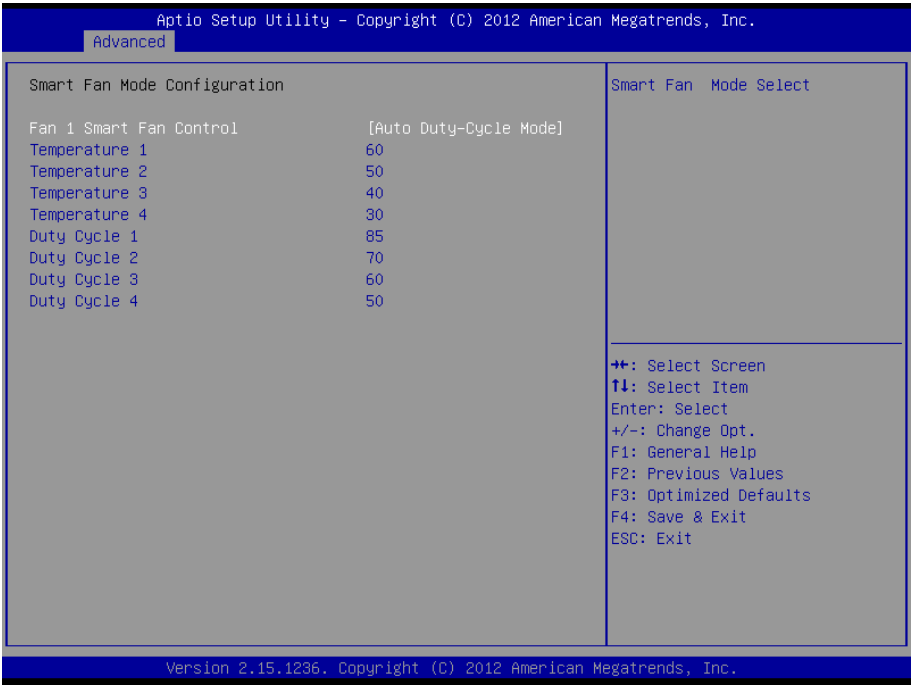
3.4.7 Advanced: H/W Monitor



Options summary:

Smart Fan Function	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable Smart Fan		

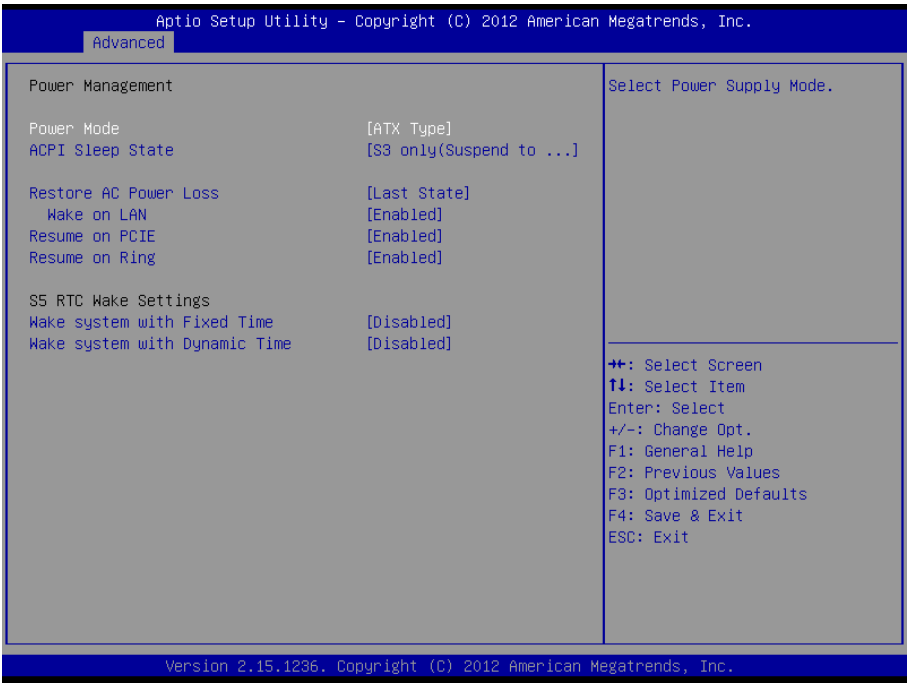
3.4.7.1 H/W Monitor: Smart Fan Mode Configuration



Options summary:

Smart Fan Mode Configuration	Manual RPM Mode	Optimal Default, Failsafe Default
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	
Smart Fan Mode Select		

3.4.8 Advanced: Power Management

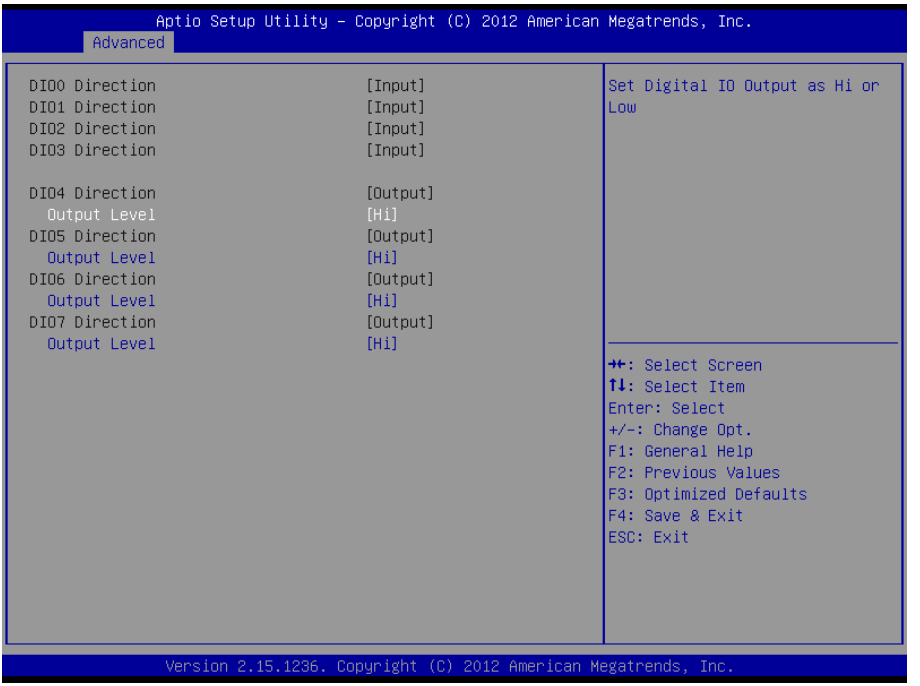


Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select Power Supply Mode.		
Restore AC Power Loss	Power off	
	Power on	
	Last State	Optimal Default, Failsafe Default
Select AC power state when power is re-applied after a power failure.		
Wake on LAN	Enable	Optimal Default, Failsafe Default
	Disable	

<table>
<tr><td colspan="3">Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)</td></tr>
<tr><td rowspan="2">Resume on PCIE</td><td>Enable</td><td rowspan="2">Optimal Default, Failsafe Default</td></tr>
<tr><td>Disable</td></tr>
<tr><td colspan="3">Enable/Disable Resume from PCIE signal</td></tr>
<tr><td rowspan="2">Resume on Ring</td><td>Enable</td><td rowspan="2">Optimal Default, Failsafe Default</td></tr>
<tr><td>Disable</td></tr>
<tr><td colspan="3">Enable/Disable Resume from RI# signal</td></tr>
<tr><td rowspan="2">Wake system with Fixed Time</td><td>Enable</td><td rowspan="2"></td></tr>
<tr><td>Disable</td><td>Optimal Default, Failsafe Default</td></tr>
<tr><td colspan="3">Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified</td></tr>
<tr><td rowspan="2">Wake system with Dynamic Time</td><td>Enable</td><td rowspan="2"></td></tr>
<tr><td>Disable</td><td>Optimal Default, Failsafe Default</td></tr>
<tr><td colspan="3">Enable or disable System wake on alarm event. When enabled, System will wake on the current time + Increase minute(s)</td></tr>
</table>

3.4.9 Advanced: Dynamic Digital IO Configuration



Options summary:

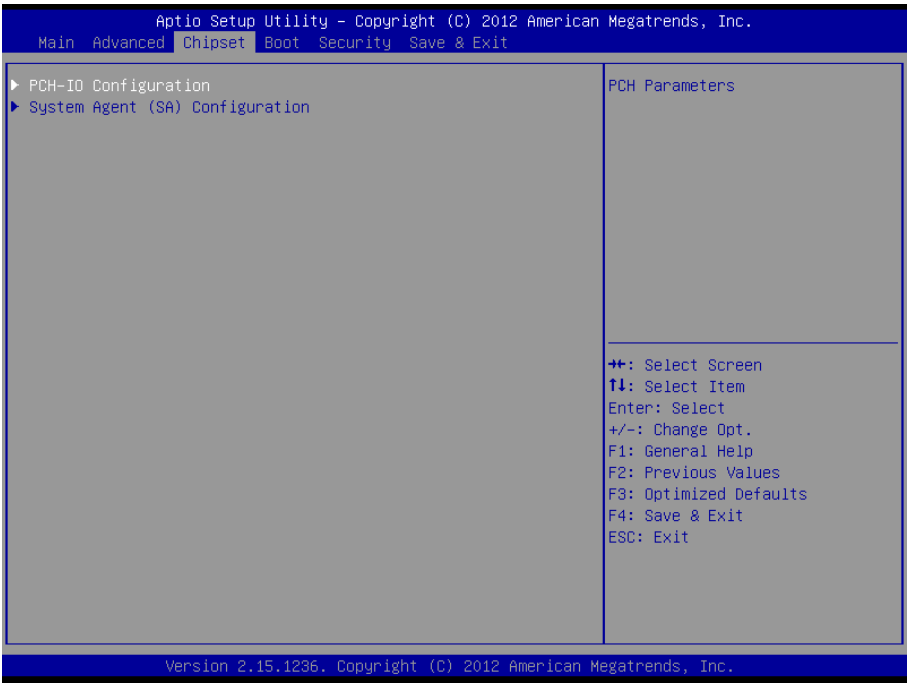
DIO[0:3]	Input	Optimal Default, Failsafe Default
	Output	
DIO[3:7][Output] Output Level	Low	Optimal Default, Failsafe Default
	Hi	
Set Digital IO Output as Hi or Low		

3.4.10 Advanced: Serial Port Console Redirection

Options summary:

Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable		

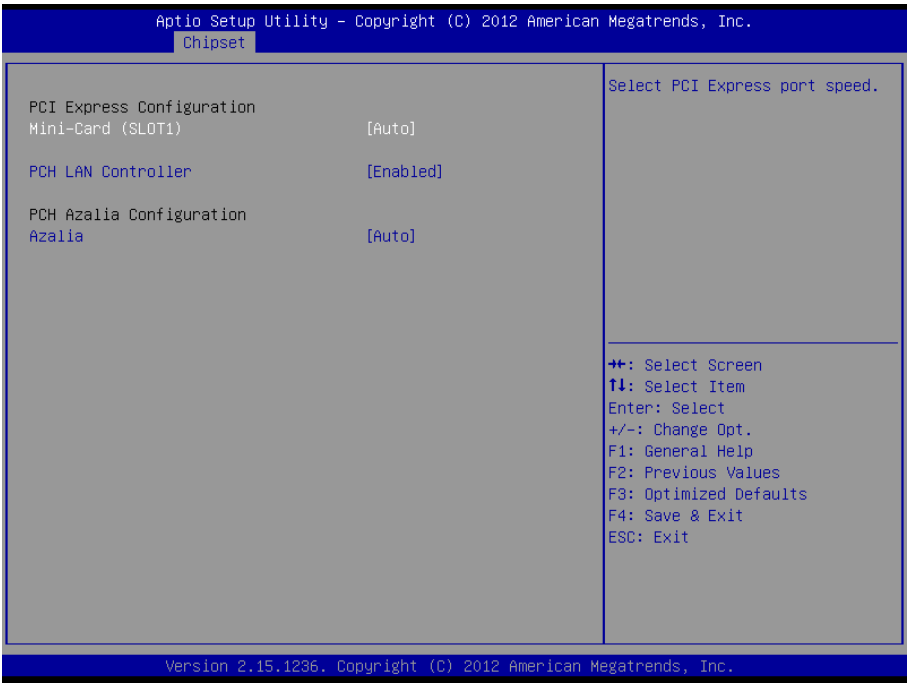
3.5 Setup submenu: Chipset



Options summary:

Touch Device	Enabled	Optimal Default, Failsafe Default
	Disabled	

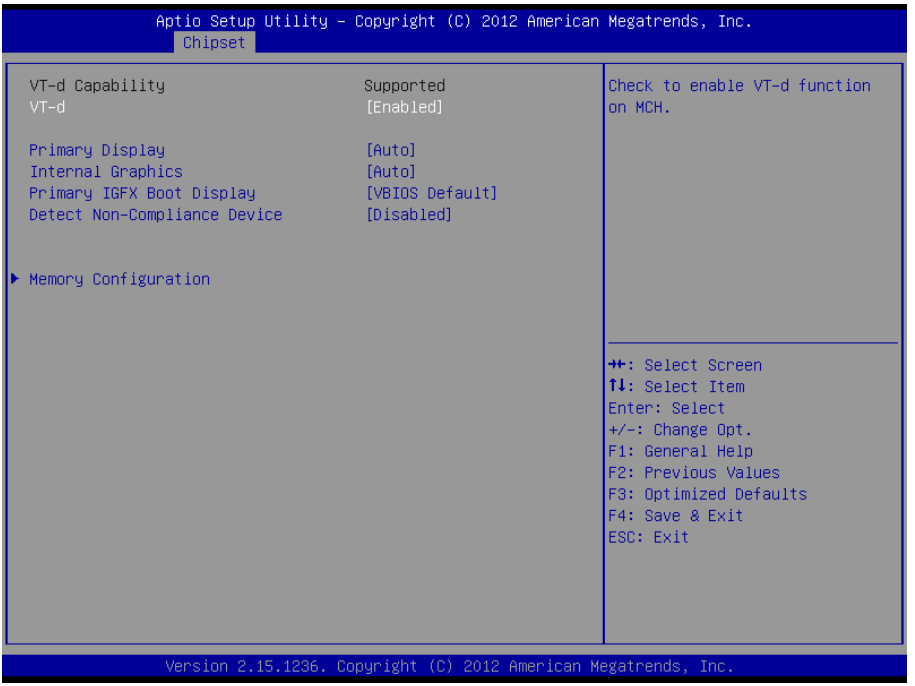
3.5.1 Chipset: RCH-IO Configuration



Options summary:

MiniCard (SLOT1)	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen1	
Select PCI Express port speed		
PCH LAN Controller	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or disable onboard NIC.		
Azalia	Disable	Optimal Default, Failsafe Default
	Enable	
	Auto	
Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally enabled Auto = Azalia will be enabled if present, disabled otherwise.		

3.5.2 Chipset: RCH-IO Configuration

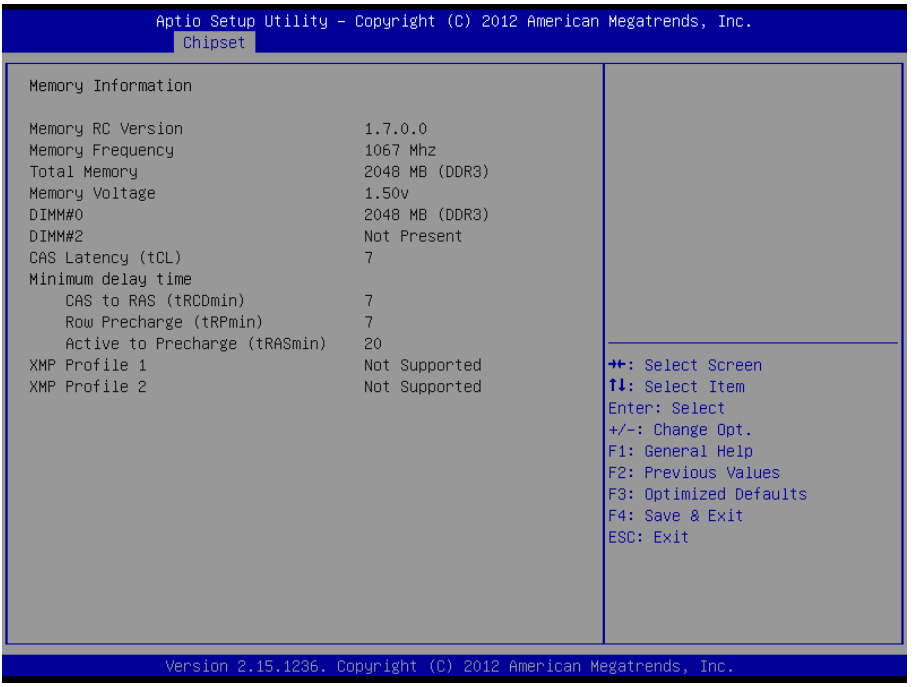


Options summary

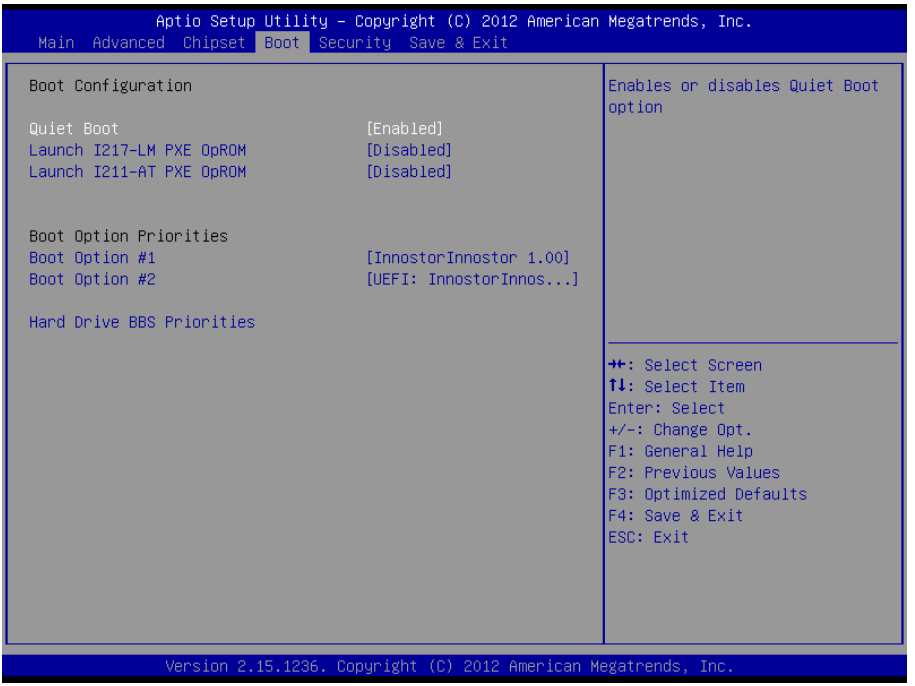
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Check to enable VT-d function on MCH.		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCIE	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display.		
Internal Graphics	Auto	Optimal Default, Failsafe Default
	Disable	
	Enable	
Keep IGD enabled based on the setup options.		
Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	CRT	

	DisplayPort	
	HDMI	
Select the Video Device which will be activated during POST. This has no effect of external graphics are present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display		
Detect Non-Compliance Device	Disable	Optimal Default, Failsafe Default
	Enable	
Detect Non-Compliance PCI Express Device in PEG		

3.5.3 Chipset: Memory Configuration



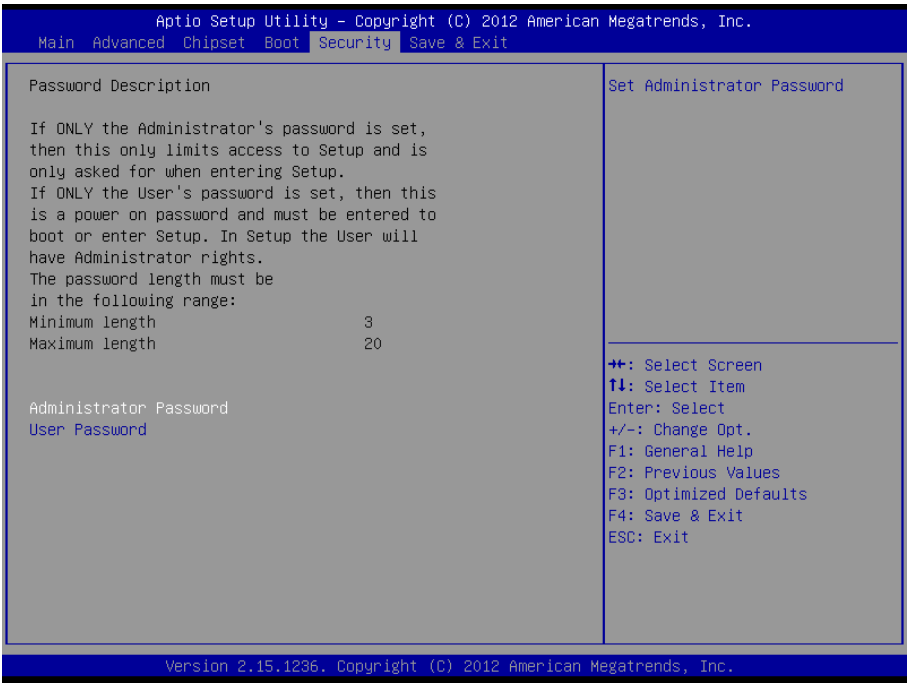
3.6 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	Default
	Enabled	
Enables or disables Quiet Boot option		
Launch I217-LM PXE OpROM	Disabled	Default
	Enabled	
Enables or Disables Legacy Boot Option for I217-LM		
Launch I211-AT PXE OpROM	Disabled	Default
	Enabled	
Enables or Disables Legacy Boot Option for I211-AT		

3.7 Setup submenu: Security



Change User/Supervisor Password

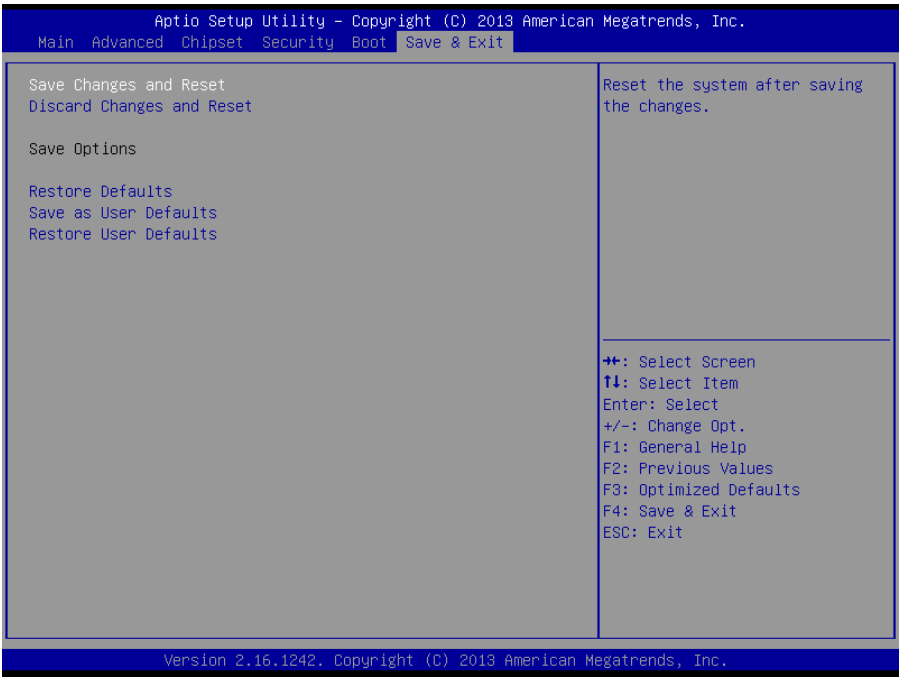
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The VPC-5500S comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step 2 - VGA** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **Step 3 – USB3.0** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **Step 4 - Audio** folder
2. Open the **.exe** file in the folder
3. Follow the instructions

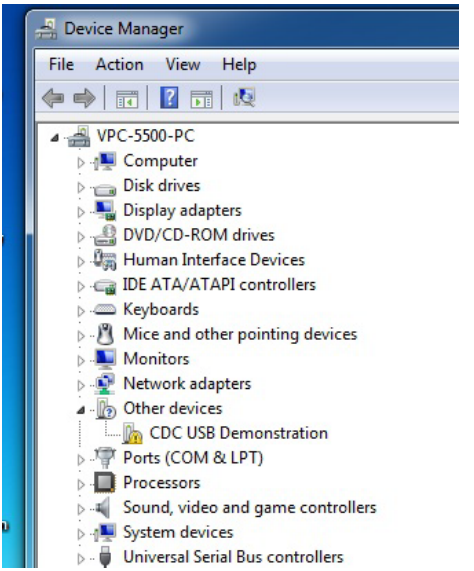
4. Drivers will be installed automatically

Step 5 – Install LAN Drivers

1. Open the **Step 5 – LAN** folder and select your OS
2. Open the **setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install CAN Bus Driver (Windows 7 only)

1. Go to Device Manager
2. Expand the "Other Devices" tree



3. Note that there is an exclamation mark at **CDD USB Demonstration**. Right click to bring up the properties dialog box.
4. Go to the Drivers tab, select Update drivers
5. Choose to let the computer search for the drivers automatically or

navigate to the drivers manually to install the drivers.

Step 7 – Install RAID AHCI Driver

Note: For Windows 7 users, please install **NDP452-KB2901907-x86-x64-AllOS-ENU.exe (Microsoft.NET Framework)** prior to installing the drivers.

1. Open the **Step 7 – RAID AHCI** folder followed by **SetupRST_13.6.0.1002.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 8 – Install ME Driver

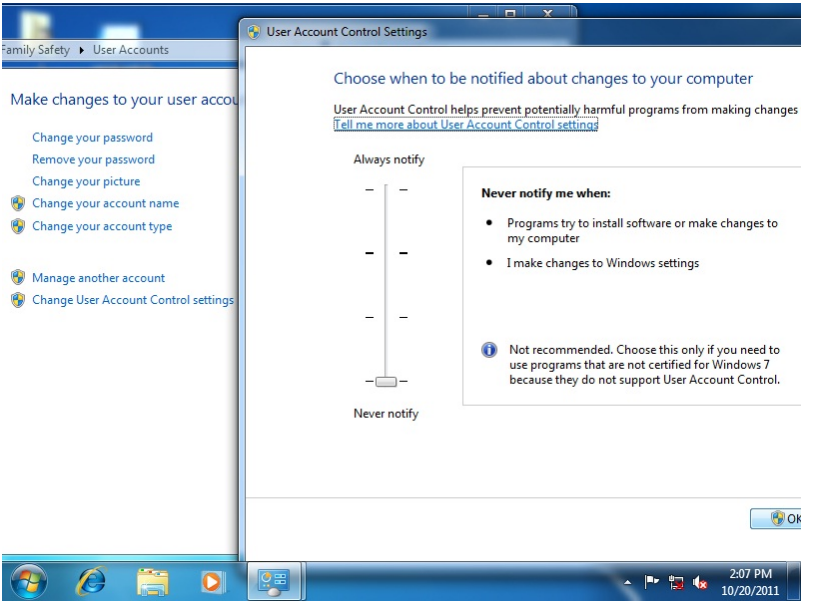
1. Open the **STEP 8 - ME** folder followed by **setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 9 – Install TPM Driver

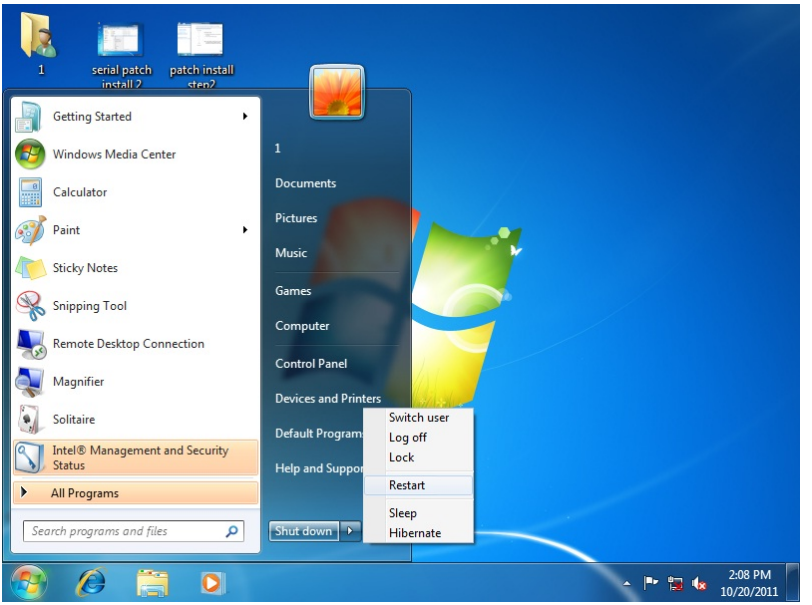
1. Open the **STEP 9 - TPM** folder followed by **setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 10 – Install UART Driver (Optional)

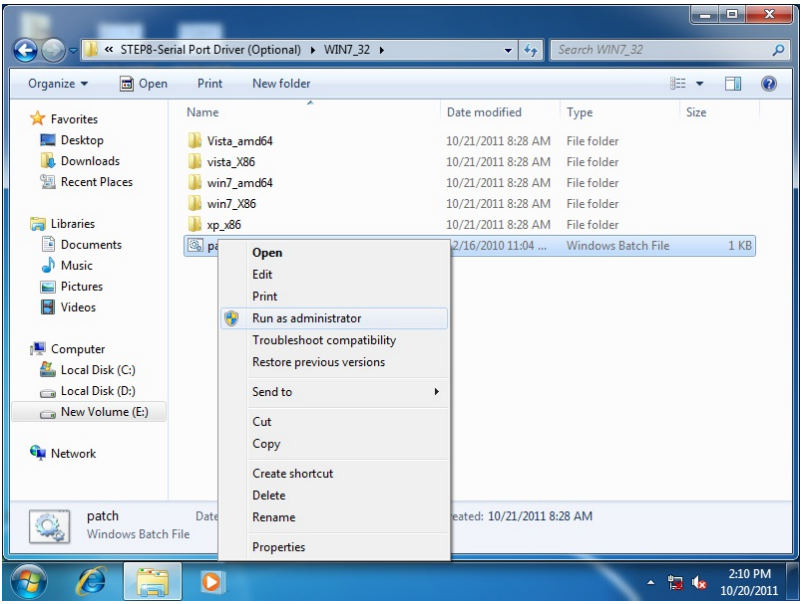
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator

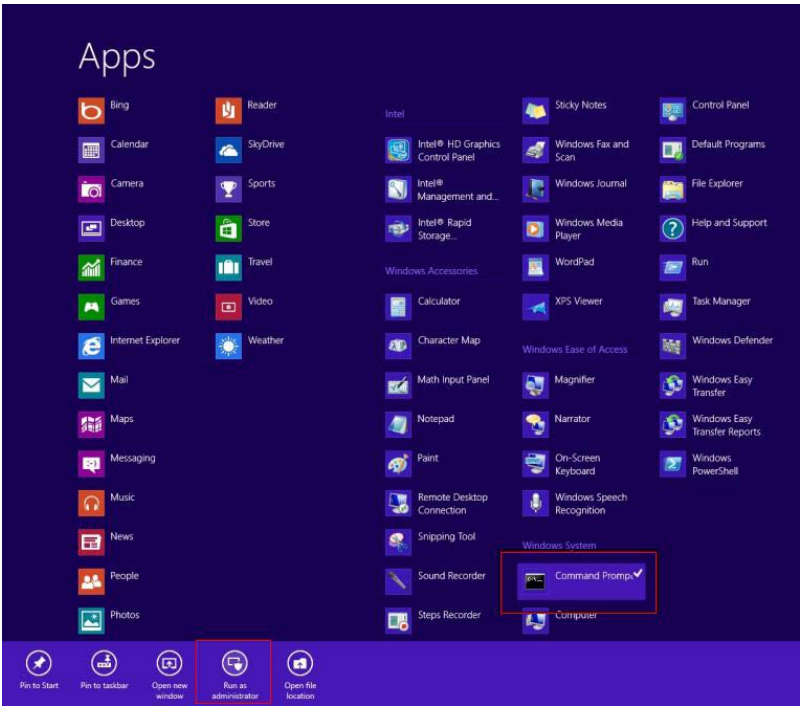


3. Run patch.bat as administrator



For Windows 8:

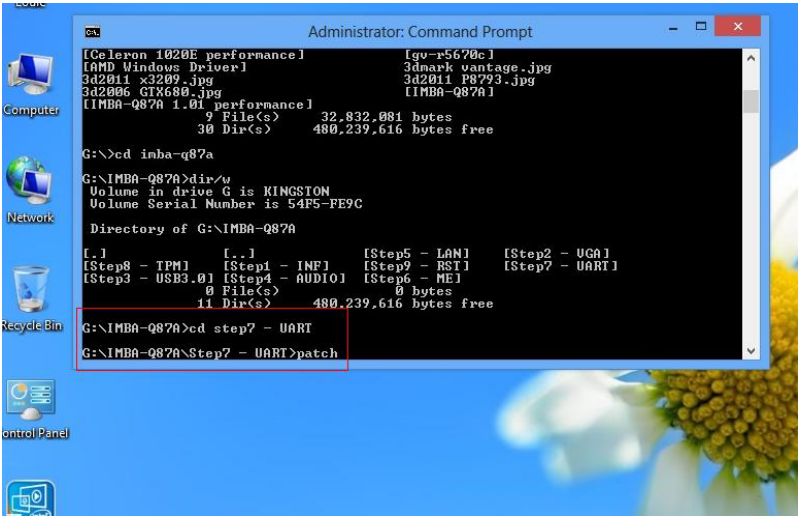
1. Open the Apps Screen, right click on the **Command Prompt** tile and select **Run as Administrator**



2. To install the driver (patch.bat), you will first have to locate the file in command prompt. To do that, first go to the directory which contains the file by entering **<drive letter>:** eg. if the driver is in D drive, enter **D:**

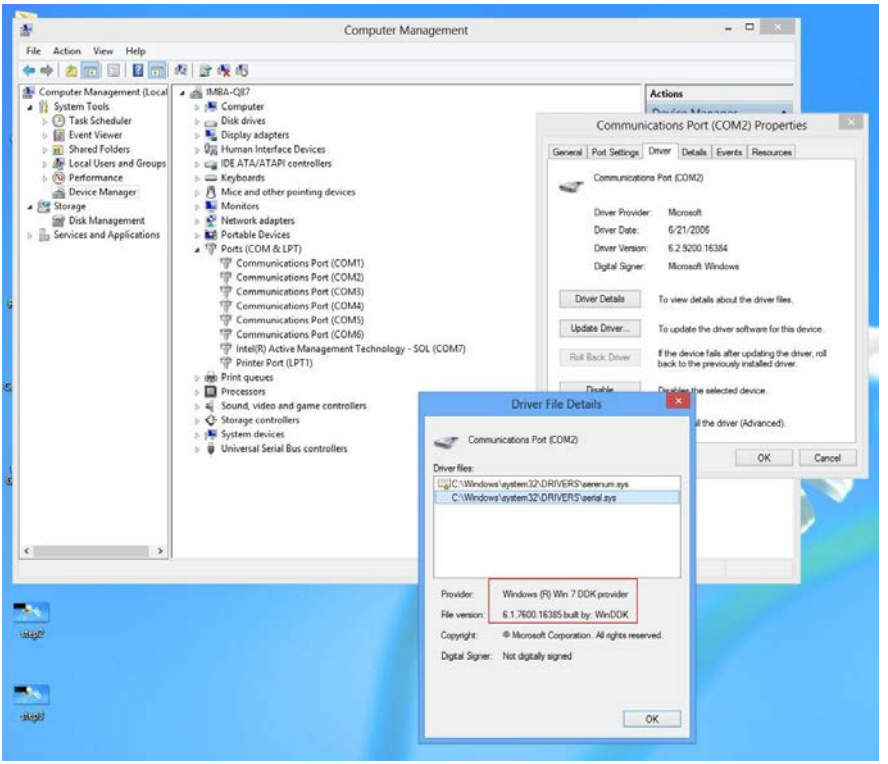
3. You are now at the directory containing the installation file. Next, go to the folder in which the file resides by entering **cd <folder>** eg: if the file is in a folder named abc, enter cd <abc>.

4. You are now at the folder where the file is located. Enter the **patch.bat** to open and install the drivers. If your file is in a subfolder, enter the cd <folder> command again to access the subfolder (screenshot below is for reference only).



5. Reboot after installation completes.

6. To confirm the installation, go to Device Manager, expand the Ports (COM & LPT) tree and double click on any of the COM ports to open its properties. Go to the Driver tab, select Driver Details and click on **serial.sys**, you should see its provider as **Windows (R) Win 7 DDK Provider**.


Computer Management
File Action View Help
Computer Management (Local
System Tools
Task Scheduler
Event Viewer
Shared Folders
Local Users and Groups
Performance
Device Manager
Storage
Disk Management
Services and Applications
IMBA-Q87
Computer
Disk drives
Display adapters
Human Interface Devices
IDE ATA/ATAPI controllers
Keyboards
Mice and other pointing devices
Monitors
Network adapters
Portable Devices
Ports (COM & LPT)
Communications Port (COM1)
Communications Port (COM2)
Communications Port (COM3)
Communications Port (COM4)
Communications Port (COM5)
Communications Port (COM6)
Intel(R) Active Management Technology - SOL (COM7)
Printer Port (LPT1)
Print queues
Processors
Sound, video and game controllers
Storage controllers
System devices
Universal Serial Bus controllers
Actions
Communications Port (COM2) Properties
General
Port Settings
Driver
Details
Events
Resources
Communications Port (COM2)
Driver Provider: Microsoft
Driver Date: 6/21/2006
Driver Version: 6.2.9200.16384
Digital Signer: Microsoft Windows
Driver Details
To view details about the driver files.
Update Driver...
To update the driver software for this device.
Roll Back Driver
If the device fails after updating the driver, roll back to the previously installed driver.
Disable
Disables the selected device.
the driver (Advanced).
OK
Cancel
Driver File Details
Communications Port (COM2)
Driver files:
C:\Windows\system32\DRIVERS\serenum.sys
C:\Windows\system32\DRIVERS\serial.sys
Provider: Windows (R) Win 7 DDK provider
File version: 6.1.7600.16385 built by: WinDDK
Copyright: © Microsoft Corporation. All rights reserved.
Digital Signer: Not digitally signed
OK

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
*********************************************************************************
```

```
*********************************************************************************
VOID    Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

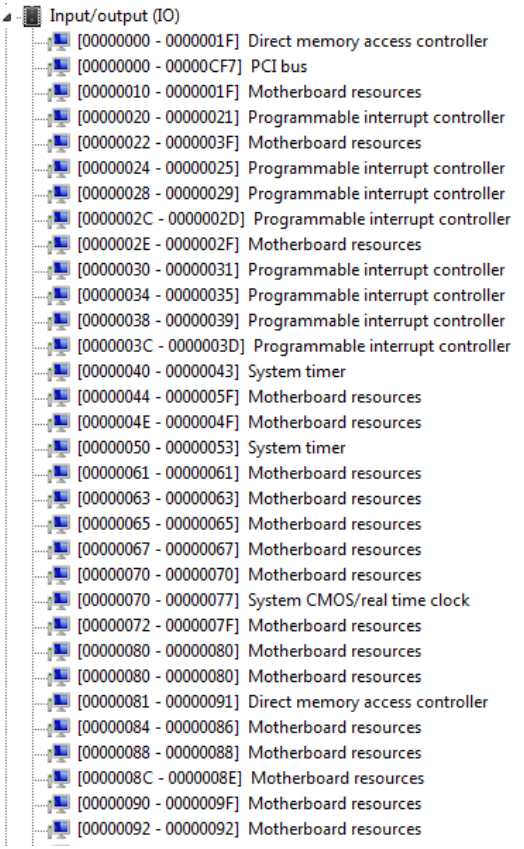
```
*****************************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig ( ){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************************
```

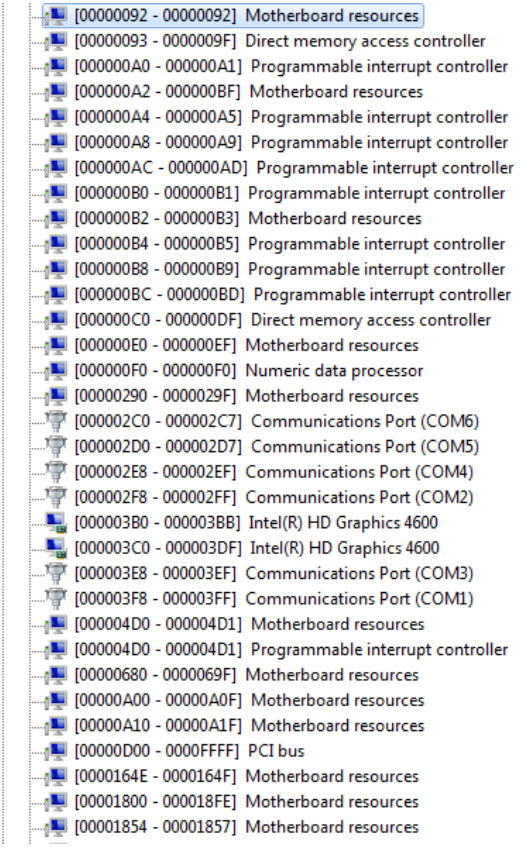
```
*********************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*********************************************************************************
```

Appendix B

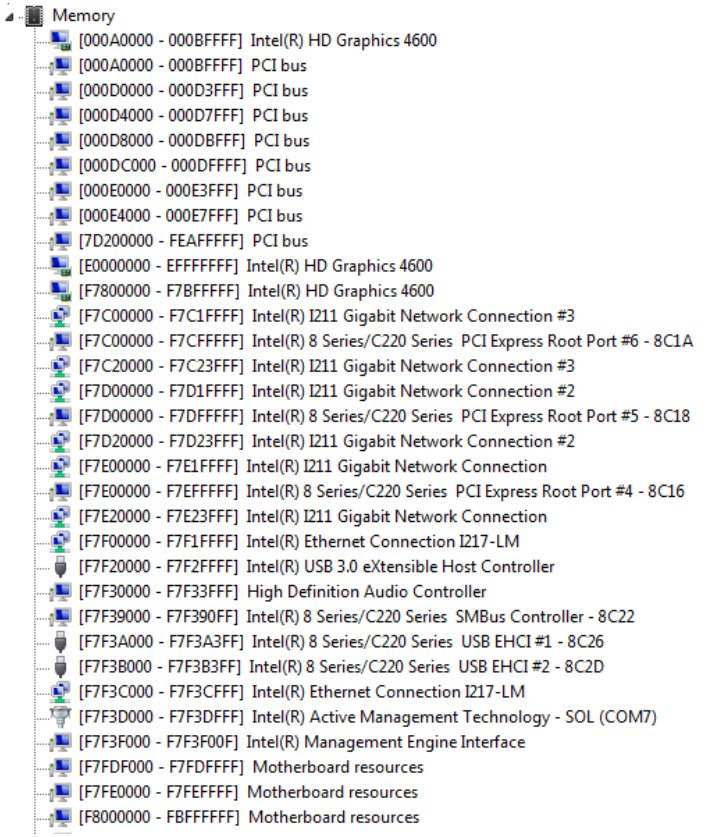
I/O Information

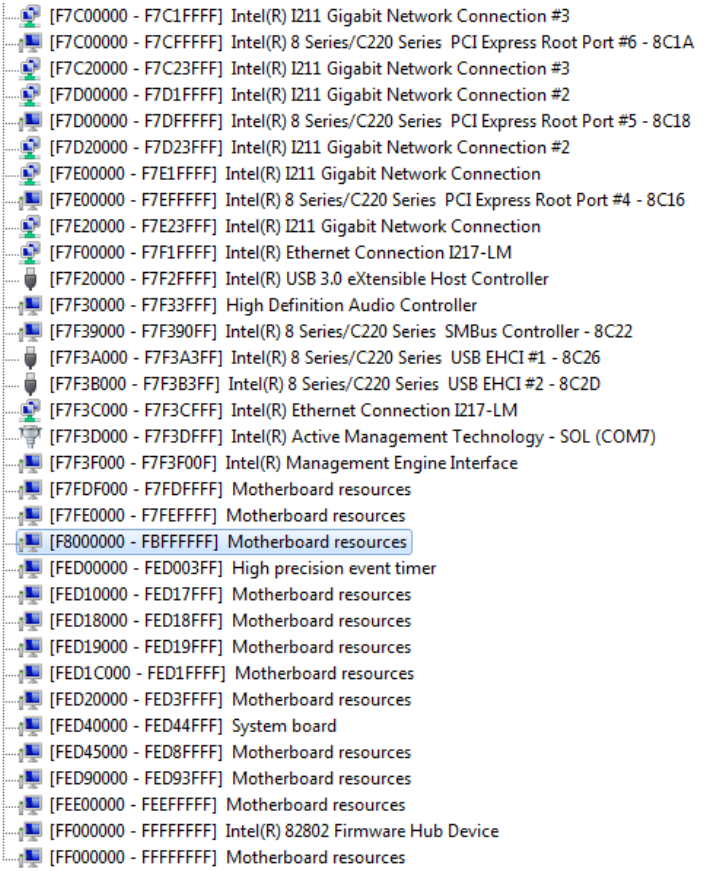
B.1 I/O Address Map



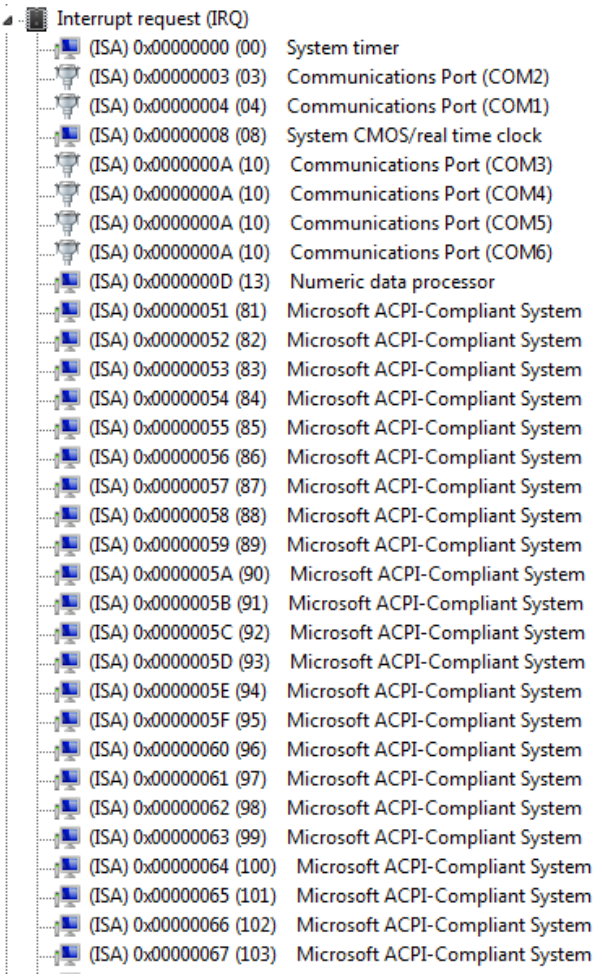

[00000092 - 00000092] Motherboard resources
[00000093 - 0000009F] Direct memory access controller
[000000A0 - 000000A1] Programmable interrupt controller
[000000A2 - 000000BF] Motherboard resources
[000000A4 - 000000A5] Programmable interrupt controller
[000000A8 - 000000A9] Programmable interrupt controller
[000000AC - 000000AD] Programmable interrupt controller
[000000B0 - 000000B1] Programmable interrupt controller
[000000B2 - 000000B3] Motherboard resources
[000000B4 - 000000B5] Programmable interrupt controller
[000000B8 - 000000B9] Programmable interrupt controller
[000000BC - 000000BD] Programmable interrupt controller
[000000C0 - 000000DF] Direct memory access controller
[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000F0] Numeric data processor
[00000290 - 0000029F] Motherboard resources
[000002C0 - 000002C7] Communications Port (COM6)
[000002D0 - 000002D7] Communications Port (COM5)
[000002E8 - 000002EF] Communications Port (COM4)
[000002F8 - 000002FF] Communications Port (COM2)
[000003B0 - 000003BB] Intel(R) HD Graphics 4600
[000003C0 - 000003DF] Intel(R) HD Graphics 4600
[000003E8 - 000003EF] Communications Port (COM3)
[000003F8 - 000003FF] Communications Port (COM1)
[000004D0 - 000004D1] Motherboard resources
[000004D0 - 000004D1] Programmable interrupt controller
[00000680 - 0000069F] Motherboard resources
[00000A00 - 00000A0F] Motherboard resources
[00000A10 - 00000A1F] Motherboard resources
[00000D00 - 0000FFFF] PCI bus
[0000164E - 0000164F] Motherboard resources
[00001800 - 000018FE] Motherboard resources
[00001854 - 00001857] Motherboard resources

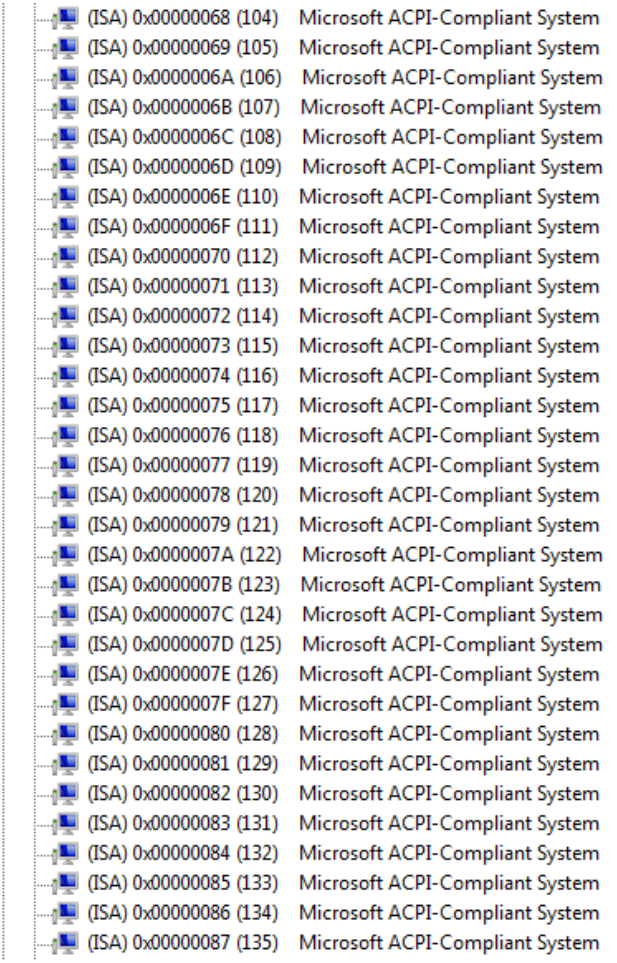
B.2 Memory Address Map

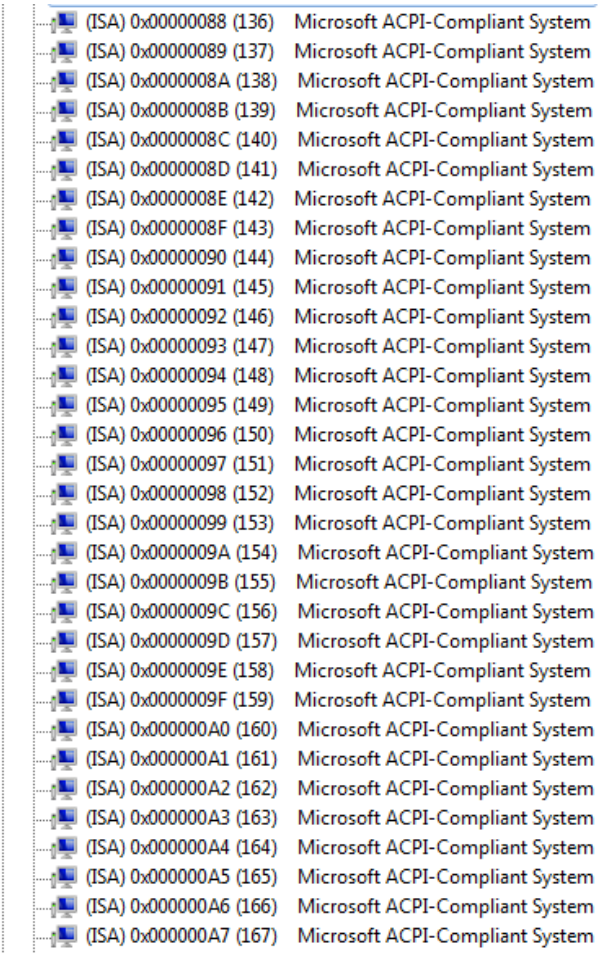


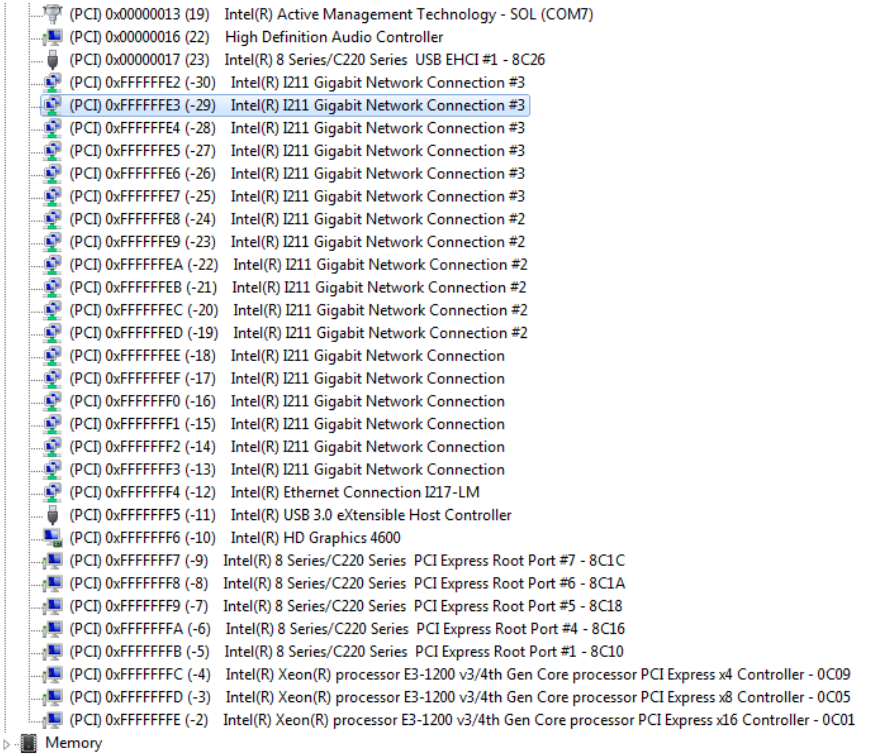

[F7C00000 - F7C1FFFF] Intel(R) I211 Gigabit Network Connection #3
[F7C00000 - F7CFFFFF] Intel(R) 8 Series/C220 Series PCI Express Root Port #6 - 8C1A
[F7C20000 - F7C23FFF] Intel(R) I211 Gigabit Network Connection #3
[F7D00000 - F7D1FFFF] Intel(R) I211 Gigabit Network Connection #2
[F7D00000 - F7DFFFFF] Intel(R) 8 Series/C220 Series PCI Express Root Port #5 - 8C18
[F7D20000 - F7D23FFF] Intel(R) I211 Gigabit Network Connection #2
[F7E00000 - F7E1FFFF] Intel(R) I211 Gigabit Network Connection
[F7E00000 - F7EFFFFF] Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
[F7E20000 - F7E23FFF] Intel(R) I211 Gigabit Network Connection
[F7F00000 - F7F1FFFF] Intel(R) Ethernet Connection I217-LM
[F7F20000 - F7F2FFFF] Intel(R) USB 3.0 eXtensible Host Controller
[F7F30000 - F7F33FFF] High Definition Audio Controller
[F7F39000 - F7F390FF] Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
[F7F3A000 - F7F3A3FF] Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26
[F7F3B000 - F7F3B3FF] Intel(R) 8 Series/C220 Series USB EHCI #2 - 8C2D
[F7F3C000 - F7F3CFFF] Intel(R) Ethernet Connection I217-LM
[F7F3D000 - F7F3DFFF] Intel(R) Active Management Technology - SOL (COM7)
[F7F3F000 - F7F3F00F] Intel(R) Management Engine Interface
[F7FDF000 - F7FDFFFF] Motherboard resources
[F7FE0000 - F7FEFFFF] Motherboard resources
[F8000000 - FBFFFFFF] Motherboard resources
[FED00000 - FED003FF] High precision event timer
[FED10000 - FED17FFF] Motherboard resources
[FED18000 - FED18FFF] Motherboard resources
[FED19000 - FED19FFF] Motherboard resources
[FED1C000 - FED1FFFF] Motherboard resources
[FED20000 - FED3FFFF] Motherboard resources
[FED40000 - FED44FFF] System board
[FED45000 - FED8FFFF] Motherboard resources
[FED90000 - FED93FFF] Motherboard resources
[FEE00000 - FEEFFFFF] Motherboard resources
[FF000000 - FFFFFFFF] Intel(R) 82802 Firmware Hub Device
[FF000000 - FFFFFFFF] Motherboard resources

B.3 IRQ Mapping Chart

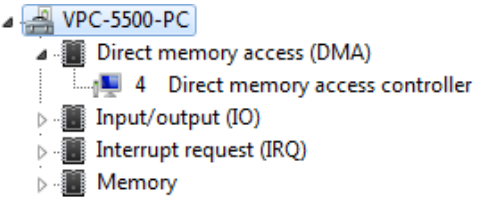



(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System


(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System


(PCI) 0x00000013 (19) Intel(R) Active Management Technology - SOL (COM7)
(PCI) 0x00000016 (22) High Definition Audio Controller
(PCI) 0x00000017 (23) Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26
(PCI) 0xFFFFFFE2 (-30) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE3 (-29) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE4 (-28) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE5 (-27) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE6 (-26) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE7 (-25) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFE8 (-24) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFE9 (-23) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEA (-22) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEB (-21) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEC (-20) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFED (-19) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFEE (-18) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEF (-17) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF0 (-16) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF1 (-15) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF2 (-14) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF3 (-13) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF4 (-12) Intel(R) Ethernet Connection I217-LM
(PCI) 0xFFFFFFF5 (-11) Intel(R) USB 3.0 eXtensible Host Controller
(PCI) 0xFFFFFFF6 (-10) Intel(R) HD Graphics 4600
(PCI) 0xFFFFFFF7 (-9) Intel(R) 8 Series/C220 Series PCI Express Root Port #7 - 8C1C
(PCI) 0xFFFFFFF8 (-8) Intel(R) 8 Series/C220 Series PCI Express Root Port #6 - 8C1A
(PCI) 0xFFFFFFF9 (-7) Intel(R) 8 Series/C220 Series PCI Express Root Port #5 - 8C18
(PCI) 0xFFFFFFFA (-6) Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
(PCI) 0xFFFFFFFB (-5) Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10
(PCI) 0xFFFFFFFC (-4) Intel(R) Xeon(R) processor E3-1200 v3/4th Gen Core processor PCI Express x4 Controller - 0C09
(PCI) 0xFFFFFFFD (-3) Intel(R) Xeon(R) processor E3-1200 v3/4th Gen Core processor PCI Express x8 Controller - 0C05
(PCI) 0xFFFFFFFE (-2) Intel(R) Xeon(R) processor E3-1200 v3/4th Gen Core processor PCI Express x16 Controller - 0C01
Memory

B.4 DMA Channel Assignments



Appendix C

Digital I/O Ports

C.1 DI/O Programming

VPC-5500S utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode
(2) Modify the data of configuration registers
(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

C.2 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A(Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A(Note10)	2(Note11)		GPIO82
DIO-4 Pin Status	0x06(Note12)	0x8A(Note13)	3(Note14)		GPIO83
DIO-5 Pin Status	0x06(Note15)	0x8A(Note16)	4(Note17)		GPIO84
DIO-6 Pin Status	0x06(Note18)	0x8A(Note19)	5(Note20)		GPIO85
DIO-7 Pin Status	0x06(Note21)	0x8A(Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A(Note25)	7(Note26)		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89(Note32)	1(Note33)	(Note34)	GPIO81
DIO-3 Output Data	0x06(Note35)	0x89(Note36)	2(Note37)	(Note38)	GPIO82
DIO-4 Output Data	0x06(Note39)	0x89(Note40)	3(Note41)	(Note42)	GPIO83
DIO-5 Output Data	0x06(Note43)	0x89(Note44)	4(Note45)	(Note46)	GPIO84
DIO-6 Output Data	0x06(Note47)	0x89(Note48)	5(Note49)	(Note50)	GPIO85
DIO-7 Output Data	0x06(Note51)	0x89(Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89(Note56)	7(Note57)	(Note58)	GPIO87

C.3 Digital I/O Sample Program

```
*******************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN   // This parameter is represented from Note3
#define byte   DInput1Reg   // This parameter is represented from Note4
#define byte   DInput1Bit   // This parameter is represented from Note5
#define byte   DInput2LDN   // This parameter is represented from Note6
#define byte   DInput2Reg   // This parameter is represented from Note7
#define byte   DInput2Bit   // This parameter is represented from Note8
#define byte   DInput3LDN   // This parameter is represented from Note9
#define byte   DInput3Reg   // This parameter is represented from Note10
#define byte   DInput3Bit   // This parameter is represented from Note11
#define byte   DInput4LDN   // This parameter is represented from Note12
#define byte   DInput4Reg   // This parameter is represented from Note13
#define byte   DInput4Bit   // This parameter is represented from Note14
#define byte   DInput5LDN   // This parameter is represented from Note15
#define byte   DInput5Reg   // This parameter is represented from Note16
#define byte   DInput5Bit   // This parameter is represented from Note17
#define byte   DInput6LDN   // This parameter is represented from Note18
#define byte   DInput6Reg   // This parameter is represented from Note19
#define byte   DInput6Bit   // This parameter is represented from Note20
#define byte   DInput7LDN   // This parameter is represented from Note21
#define byte   DInput7Reg   // This parameter is represented from Note22
#define byte   DInput7Bit   // This parameter is represented from Note23
#define byte   DInput8LDN   // This parameter is represented from Note24
#define byte   DInput8Reg   // This parameter is represented from Note25
#define byte   DInput8Bit   // This parameter is represented from Note26
*******************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*****************************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //       Example, Read Digital I/O Pin 3 status
         // Output :
         //      InputStatus :
         //              0: Digital I/O Pin level is low
         //              1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //       Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****************************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*******************************************************************************
VOID    SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*******************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************
```