VPC-3350S

Mobile NVR

User's Manual 2nd Ed

Last Updated: November 1, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
VPC-3350S	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Mobile NVR
Processor	Intel® Apollo Lake Processor
	Intel® Atom® x5 E3940 (Default)
	Intel® Pentium® N4200 (Per Project Basis)
	Intel® Celeron® N3350 (Per Project Basis)
	Intel® Atom® x7 E3950 (w/ Custom Chassis)
Chipset	—
Main Memory	Up to 8GB, DDR3L 204-pin SODIMM
Display	HDMI x 1
	DP x 1
Ethernet	Intel® i211 (colay i210)
PoE Ethernet Port	4 x ports, total power consumption max. 60W
RAID support	—
Expansion Slot	Mini-Card slot x 2 (USB2.0 + PCIe)
	SATA x 1
	Built-in CANbus (in-vehicle config., optional)
GPS, G-Sensor	Built-in GPS & G Sensor (in-vehicle config., optional)
Front I/O Panel	Power Button x 1
	Reset Button x 1
	Power/HDD LED x 2
	USB 3.0 x 2
	GbE port (RJ-45) x 1
	PoE LAN x 4 (IEEE 802.3 at/af)
	HDMI x 1

System

Front I/O Panel	CanBus connector x 1 (in-vehicle config, optional) RS-232 x 3 (in-vehicle config., optional)
Rear I/O Panel	DC-In power x 1 8-bit DIO x 1, 4-ch digital input, 4-ch digital output RS-232/422/485 x 2 DP x 1 Audio Line-out x 1 Mic-In x 1 Micro SIM slot x 2

Storage

HDD Tray	2.5" HDD/SSD Bay x 1

Environmental

Operating Temperature	-4°F ~ 158°F (-20°C ~ 70°C)
Storage Temperature	-40°F ~ 185°F (-40°C ~ 85°C)
Storage Humidity	10%~80% @40°C, non-condensing
Vibration/Shock	MIL-STD-810G
Certification	CE & FCC Class A, E-MARK (optional)

Power Requirement

Power Supply	DC 12-24V DC 9-36V with power ignition (in-vehicle config., optional)

Mechanical

Removable HDD Tray	—
Internal System HDD Bay	—
Dimension	160mm (L) x 134mm (W) x 62mm (H)
Gross Weight	1.8 kg
Note	—

Note: VPC-3350S is available in two configurations: mobile NVR and in-vehicle NVR. In-vehicle NVR shares the same specifications as mobile NVR with additional I/O ports and different power supply. If you are unsure which configuration you have, contact your AAEON sales representative for assistance.

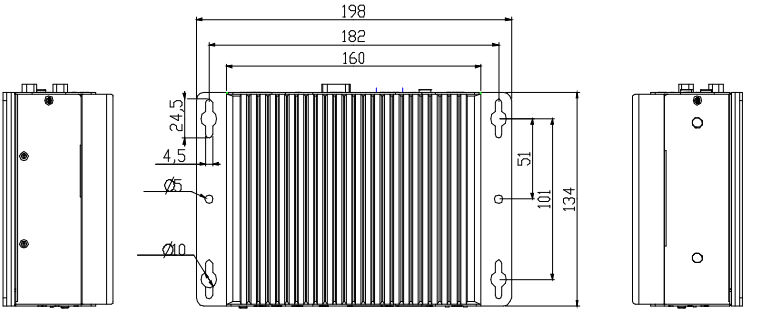
Chapter 2

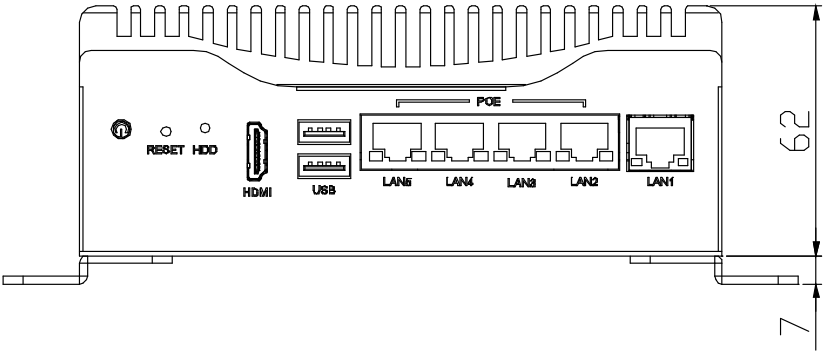
Hardware Information

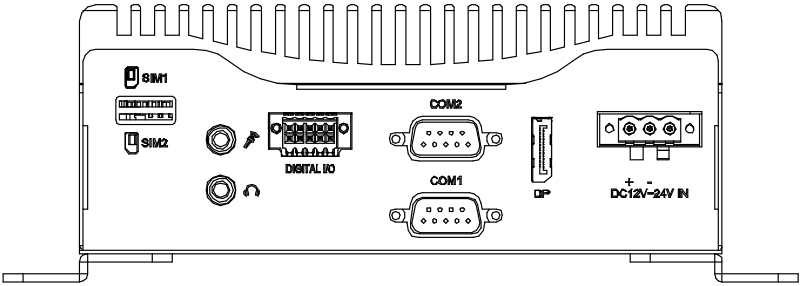
2.1 Dimensions

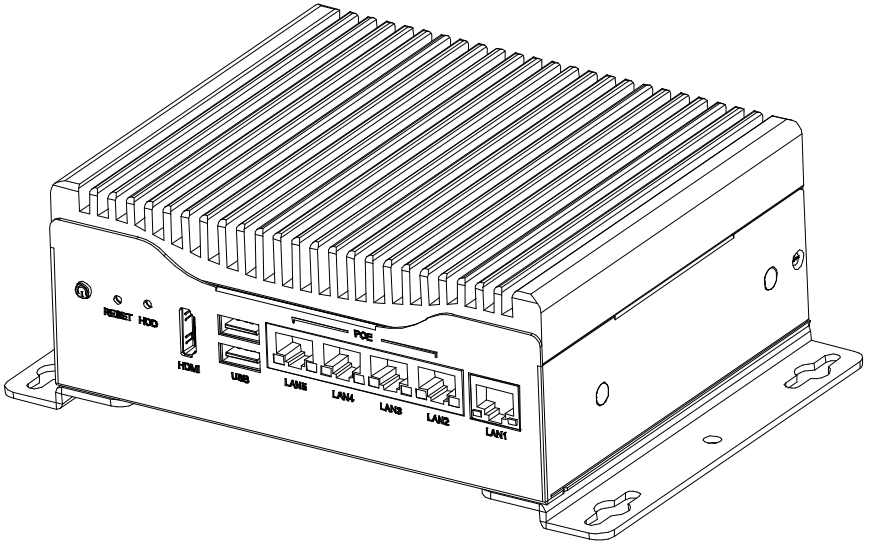
The VPC-3350S is available in two configurations, Industrial and In-vehicle. You may refer to this section for either configuration. If you have questions about your VPC-3350S or its configuration, please contact your AAEON sales representative.

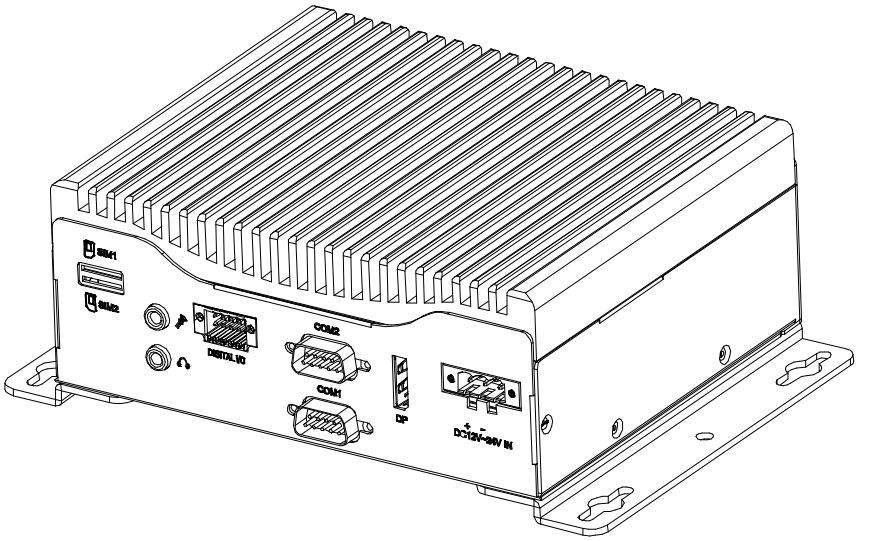
2.1.1 Industrial System



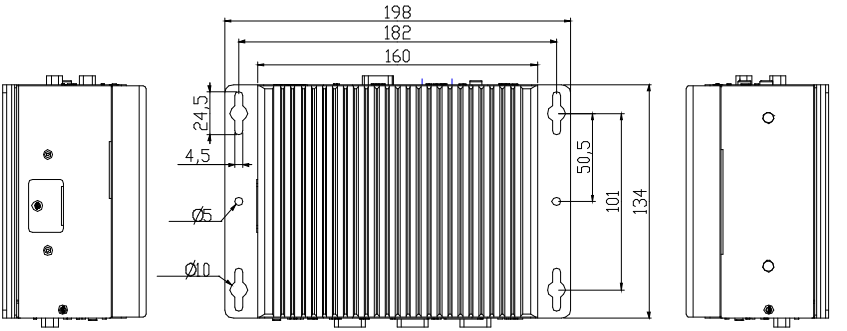

RESET
HDD
HDMI
USB
POE
LAN5
LAN4
LAN3
LAN2
LAN1
62
7

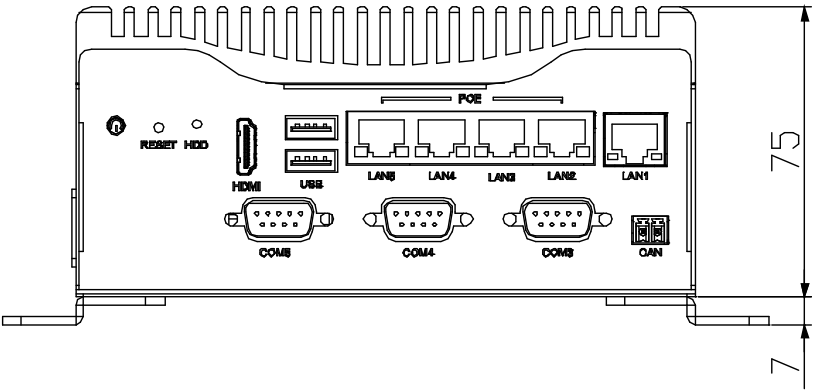

SIM1
SIM2
DIGITAL I/O
COM2
COM1
DP
+ -
DC12V~24V IN

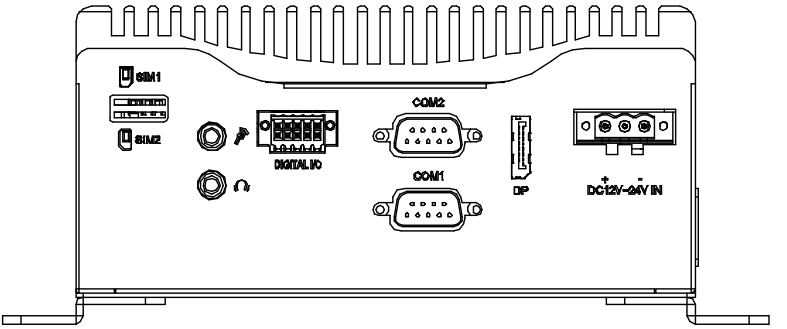

RESET
HDD
HDMI
USB
POE
LAN5
LAN4
LAN3
LAN2
LAN1

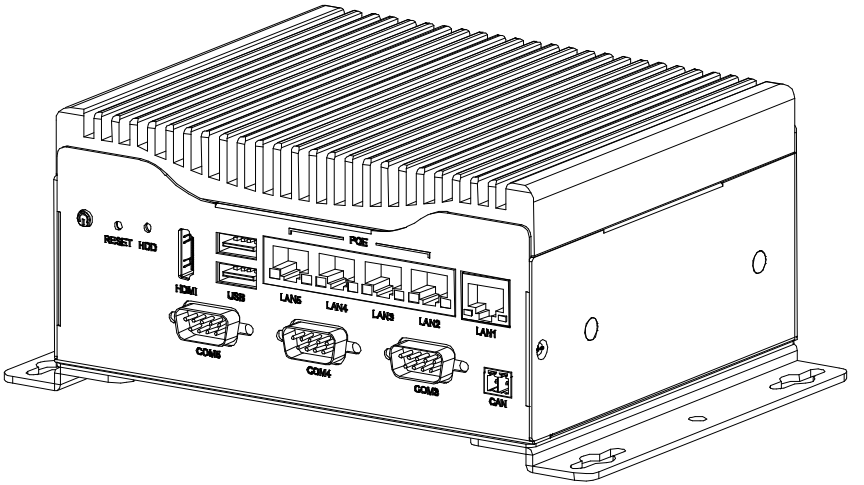

SIM1
SIM2
DIGITAL I/O
COM2
COM1
DP
+ -
DC12V-48V IN

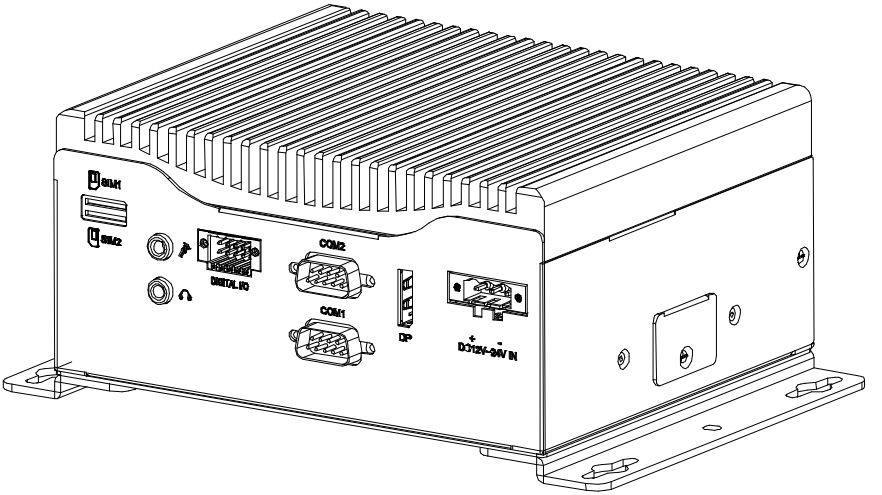
2.1.2 In-Vehicle System



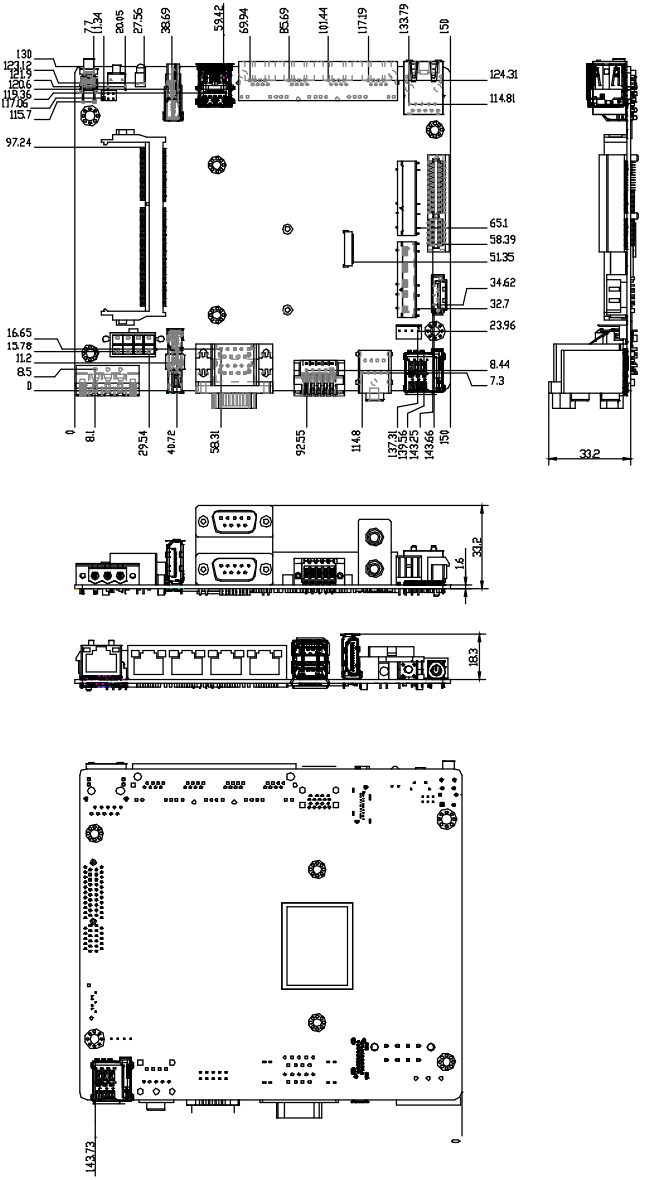





RESET
HDD
HDMI
USB
POE
LAN5
LAN4
LAN3
LAN2
LAN1
COM5
COM4
COM3
CAN

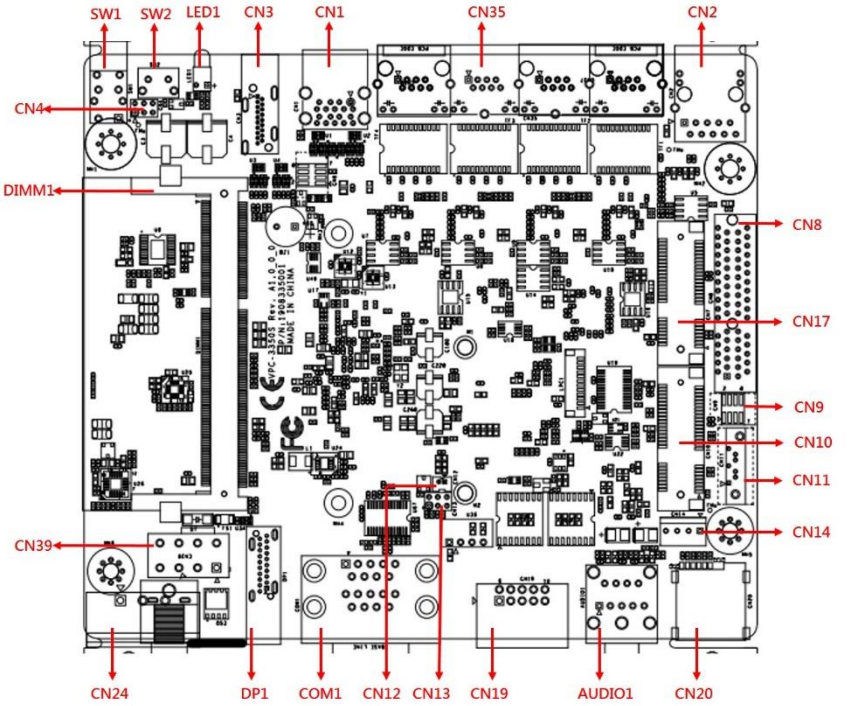

SIM1
SIM2
DIGITAL I/O
COM2
COM1
DP
D-12V~24V IN

2.1.3 Main Board

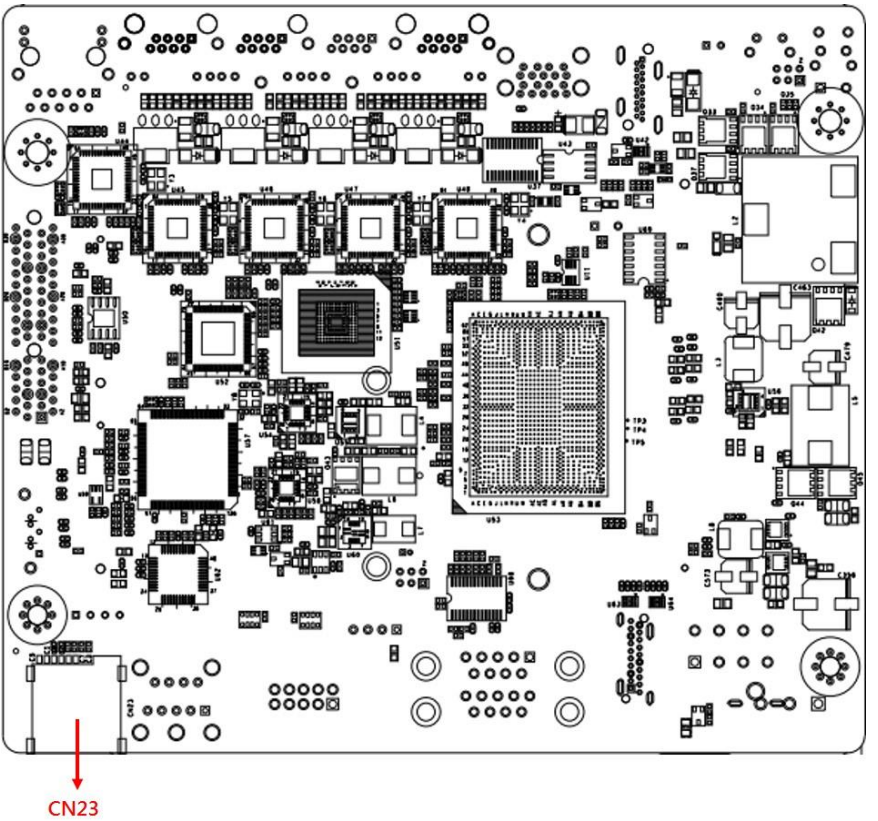


2.2 Jumpers and Connectors

Top Side



Bottom Side



2.3 List of Jumpers

Please refer to the table below for all of the system's jumpers that you can configure for your application.

Label	Function
CN13	Clear CMOS

2.3.1 Clear CMOS (CN13)

CN13 Clear CMOS uses a 6-pin configuration. Use two jumpers to connect the pins according to the chart.

Pin Selection	Function
1+3, 2+4	Normal, Default
3+5, 4+6	Clear CMOS

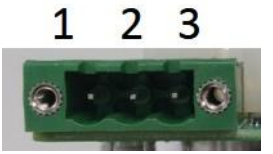
2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
AUDIO1	Front out/Microphone
CN1	Dual USB3.0
CN2	Ethernet 1 without Poe
CN3	HDMI Connector
CN4	Front Panel
CN8	For Option IO Board Connector
CN9	For Vehicle Application
CN10	Full Function Mini Card with CN23 *Option mSATA
CN11	SATA Connector
CN12	Battery Connector
CN14	SATA Power (+5V Only)
CN17	Full Function Mini Card with CN20
CN19	Digital IO Connector
CN20	SIM Slot with CN17
CN23	SIM Slot with CN10
CN24	DC Input (12~24V)
CN35	Ethernet 2.3.4.5 with Poe
CN39	Vehicle Option Power Board Application *Box PC Not use
COM1	Serial Port 1.2 with RS232/422/485 *Up COM1/Down COM2
DIMM1	DDR3L SODIMM Slot
DP1	Display Port Connector

Label	Function
LED1	SATA R/W LED
SW1	Power Button
SW2	Software Reset

2.4.1 DC Input 12~24V (CN24)



Pin	Signal	Pin	Signal
1	NA	2	GND
3	V+		

2.4.2 SATA Power Connector (CN14)

Pin	Signal	Pin	Signal
1	NA	2	GND
3	GND	4	+5V

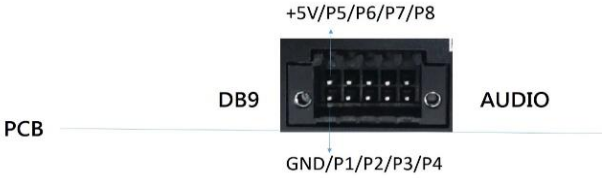
2.4.3 Serial Port 1.2 with RS232/422/485 (COM1)

Pin	Signal	Pin	Signal
1	DCD(485-/422TX-)	6	DSR
2	RXD(485+/422TX+)	7	RTS
3	TXD(422RX+)	8	CTS
4	DTR(422RX-)	9	RI
5	GND		

2.4.4 Front Panel (CN4)

Pin	Signal	Pin	Signal
1	PWR_SW# (For Car PC)	2	FPANSWH# (For Car PC)
3	GND	4	HW_RST#
5	GND	6	FPANSWH#

2.4.5 Digital IO Connector (CN19)



Pin	Signal	Pin	Signal
1	GND	6	+5V
2	GPIO Port1	7	GPIO Port5
3	GPIO Port2	8	GPIO Port6
4	GPIO Port3	9	GPIO Port7
5	GPIO Port4	10	GPIO Port8

GPIO Mapping for DIO Connector (CN19)

Pin	Signal	GPIO Mapping	Pin	Signal	GPIO Mapping
2	Bit0	Mapping SIO GP80	7	Bit4	Mapping SIO GP84
3	Bit1	Mapping SIO GP81	8	Bit5	Mapping SIO GP85
4	Bit2	Mapping SIO GP82	9	Bit6	Mapping SIO GP86
5	Bit3	Mapping SIO GP83	10	Bit7	Mapping SIO GP87

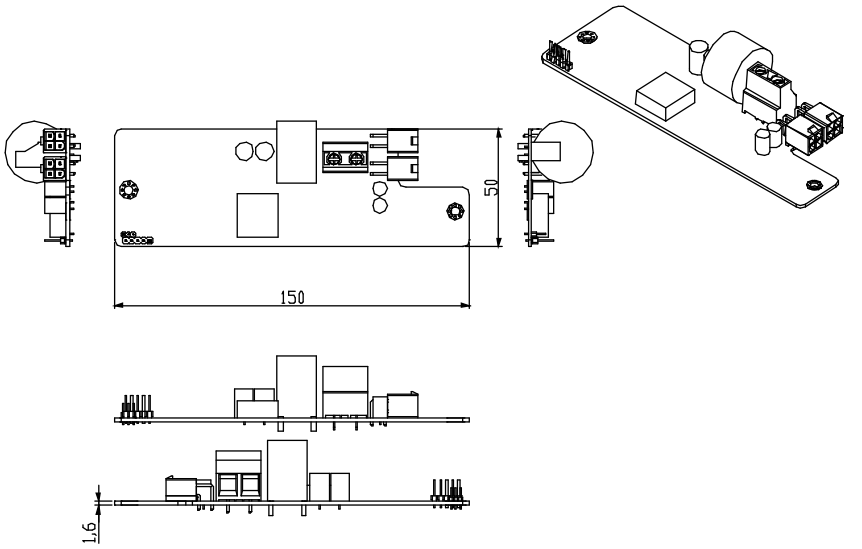
2.4.6 Software Reset (SW2) GPIO Mapping

SW2 GPIO Mapping
Mapping SIO F81866 GP76

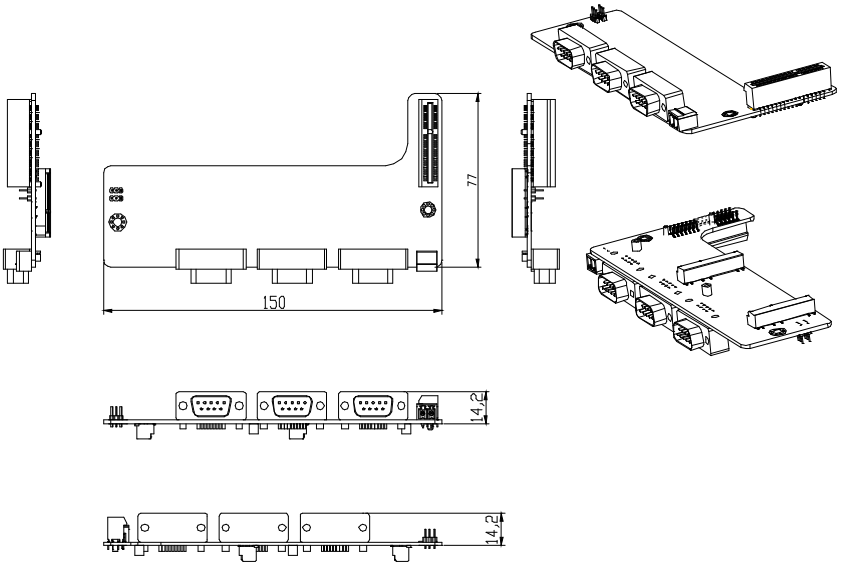
2.5 Option Board Dimensions

The VPC-3350S In-Vehicle configuration comes with two option boards, PER-T528 Power Board, and PER-T529 I/O Board. If you have any questions about the configuration of your VPC-3350S, please contact your AAEON sales representative for assistance.

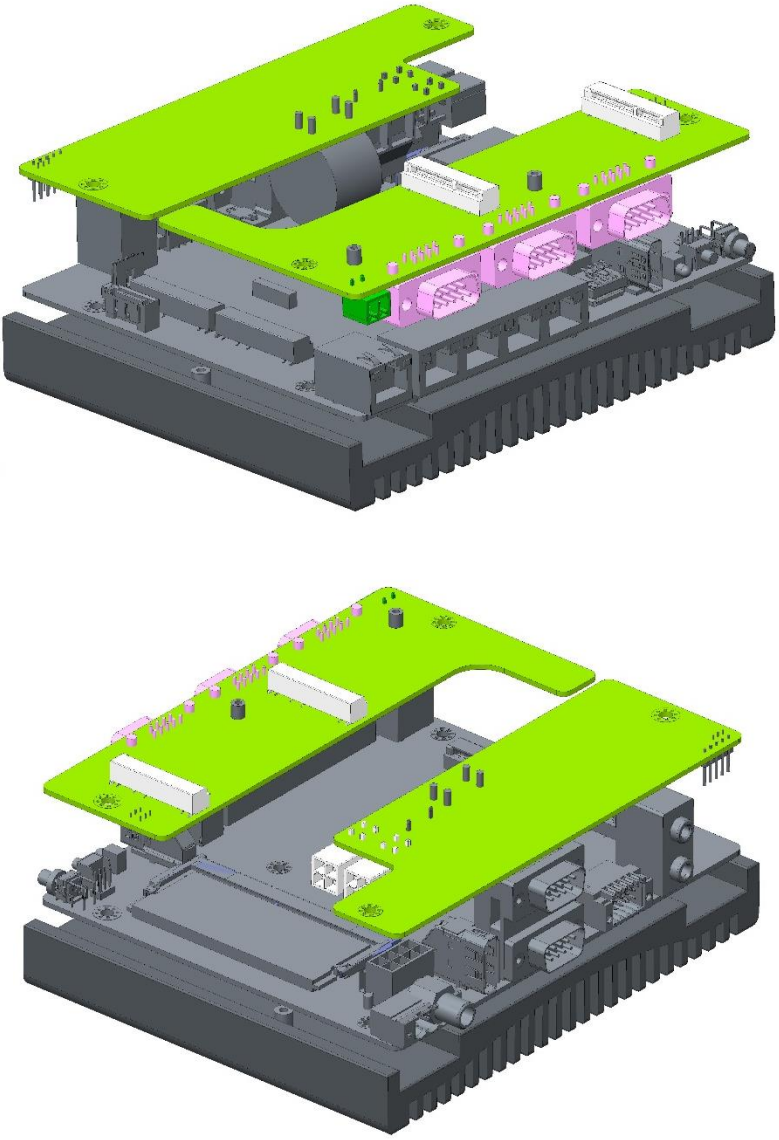
2.5.1 PER-T528 Power Board Dimensions



2.5.2 PER-T529 I/O Board Dimensions



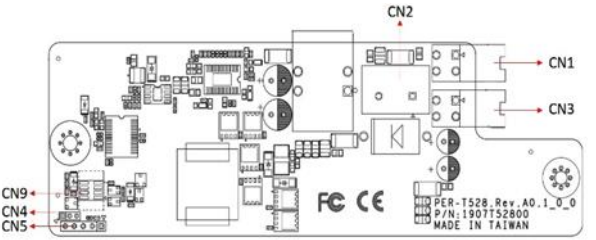
2.5.3 Option Board Assembly



2.6 Option Board Jumpers and Connectors

The VPC-3350S In-Vehicle configuration comes with two option boards, PER-T528 Power Board, and PER-T529 I/O Board. If you have any questions about the configuration of your VPC-3350S, please contact your AAEON sales representative for assistance.

2.6.1 PER-T528 Power Board Jumpers and Connectors



2.6.2 PER-T528 List of Jumpers

Label	Function
CN4	RESERVED

2.6.2.1 Reserved (CN4)

Pin Selection	Function
1-2	Reserved
2-3	Normal (Default)

2.6.3 PER-T528 List of Connectors

Label	Function
CN1	DC-Input
CN2	Fuse Slot
CN3	12VSB Output
CN5	MCU Program Header
CN9	Board To Board Cable Connector

2.6.3.1 DC-Input (CN1)

Pin	Signal	Pin	Signal
1	V-	2	V-
3	V+	4	V+

2.6.3.2 12VSB Output (CN3)

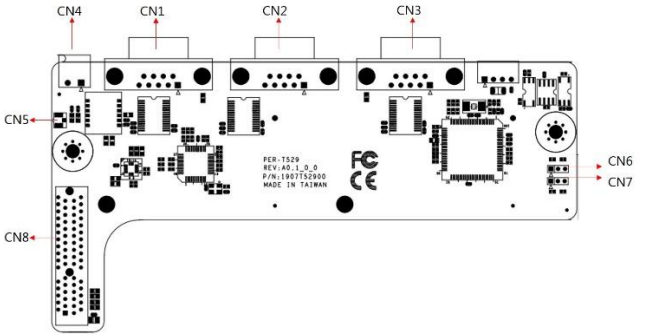
Pin	Signal	Pin	Signal
1	GND	2	GND
3	+12V	4	+12V

2.6.3.3 Board to Board Cable Connector (CN9)

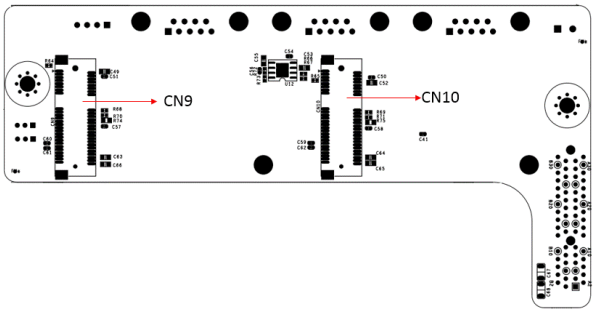
Pin	Signal	Pin	Signal
1	UART RX	5	Remote_SW#
2	PS_ON#	6	Ignition_SW
3	UART TX	7	Power Button#
4	GND	8	None

2.6.4 PER-T529 I/O Board Jumpers and Connectors

Top



Bottom



2.6.5 PER-T529 List of Jumpers

Label	Function
CN6	CAN Bus MCU Debug
CN7	CAN Bus MCU Debug

2.6.5.1 CAN Bus MCU Debug (CN6)

Pin Selection	Function
1-2	Normal (Default)
2-3	Debug

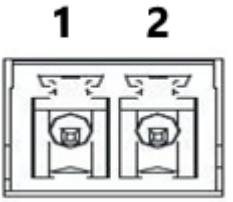
2.6.5.2 CAN Bus MCU Debug (CN7)

Pin Selection	Function
1-2	Debug
2-3	Normal (Default)

2.6.6 PER-T529 List of Connectors

Label	Function
CN1	Com Port (RS232 only)
CN2	Com Port (RS232 only)
CN3	Com Port (RS232 only)
CN4	CAN Bus Connector
CN5	GPS Antenna Connector
CN8	Board to Board Connector
CN9	Full Function mPCIE
CN10	Full Function mPCIE

2.6.6.1 CAN Bus Connector (CN4)



Pin	Signal	Pin	Signal
1	CAN DATA+		CAN DATA-

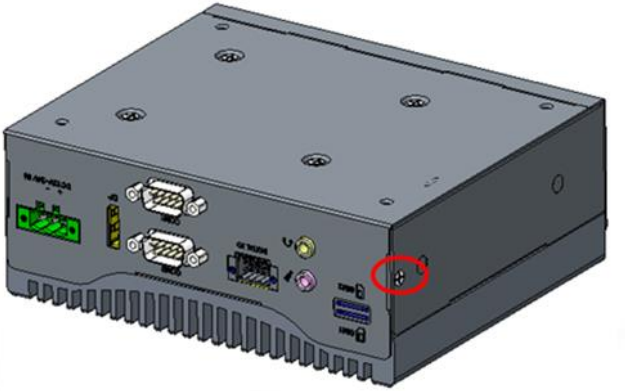
Mating Connector: DINKLE EC381V-02P

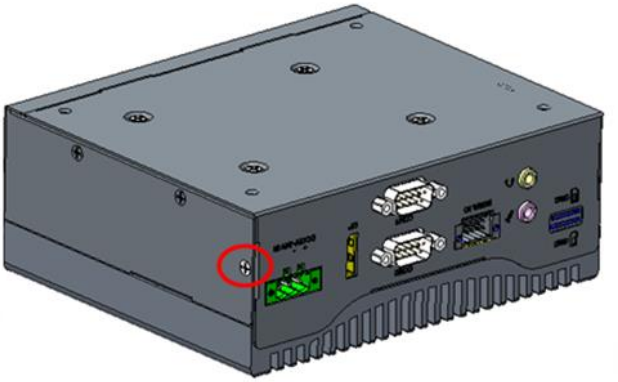
2.7 HDD/SSD 2.5" Drive Installation

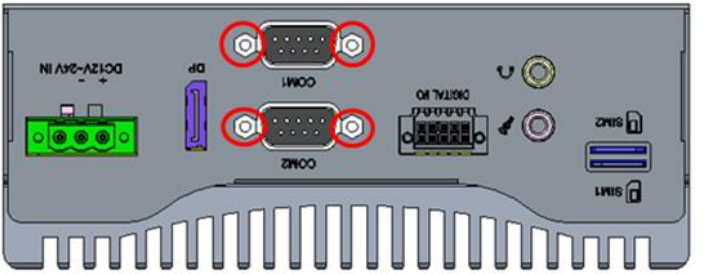
This section details the steps to install or remove the 2.5" hard drive or solid state drive (SSD). Before beginning these steps, please ensure the VPC-3350S system is shut down (not in sleep or suspended mode) and the power supply is disconnected.

Step 1 Remove the wall mount brackets.

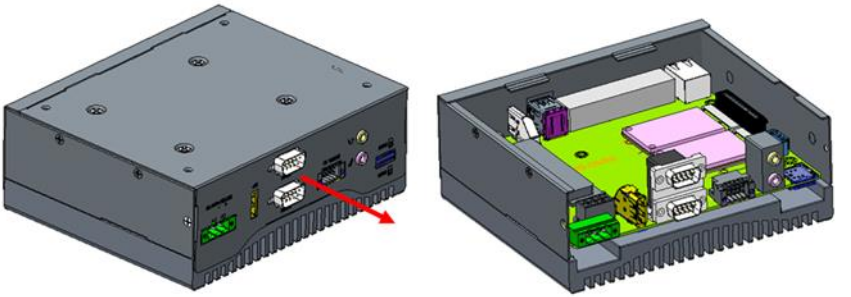
Step 2 Remove the screws securing the bottom cover. First the side screws, then the COM port fasteners.



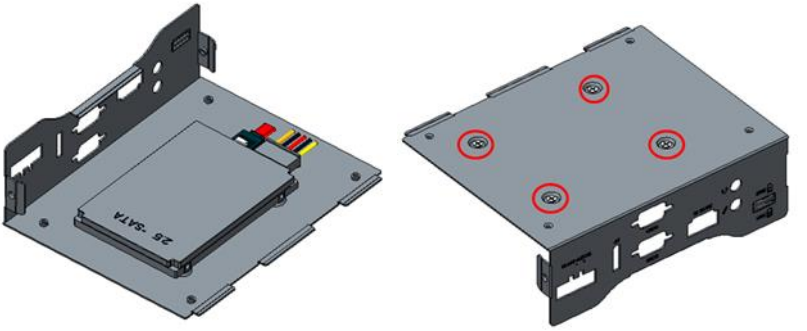




Step 3 Remove the bottom cover by sliding the cover toward the rear.



Step 4 Remove the HDD/SSD assembly by removing the screws located on the bottom of the cover. You can now remove the old drive and/or install a new one.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or display an error message. The system can usually continue the boot up sequence with non-fatal errors.

System verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If the system configuration is not found or a system configuration data error is detected, the system will load the Optimized Default Settings and re-boot with this configuration automatically.

There are four situations in which the CMOS settings will need to be setup or changed:

- Starting the system for the first time
- The system hardware has been changed
- The system configuration was reset by the Clear CMOS jumper.
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, power on the system and immediately press <Del> or <Esc>.

The function for each interface can be found below.

Main – Date and time can be set here.

Advanced – Configure major system features (CPU, Super IO, Hardware Monitor, etc.)

Chipset – Configure chipset features.

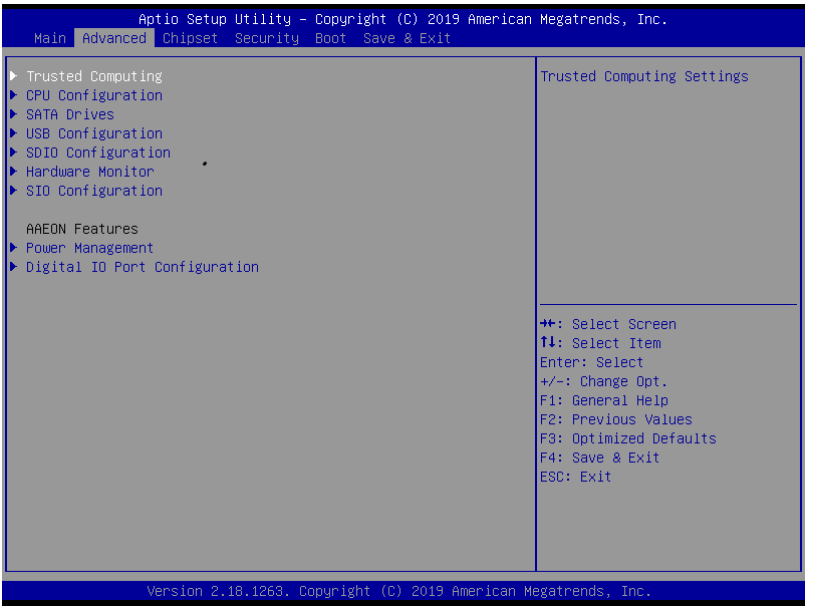
Security – The BIOS administrator and user passwords can be set here

Boot – Set boot priorities and configurations.

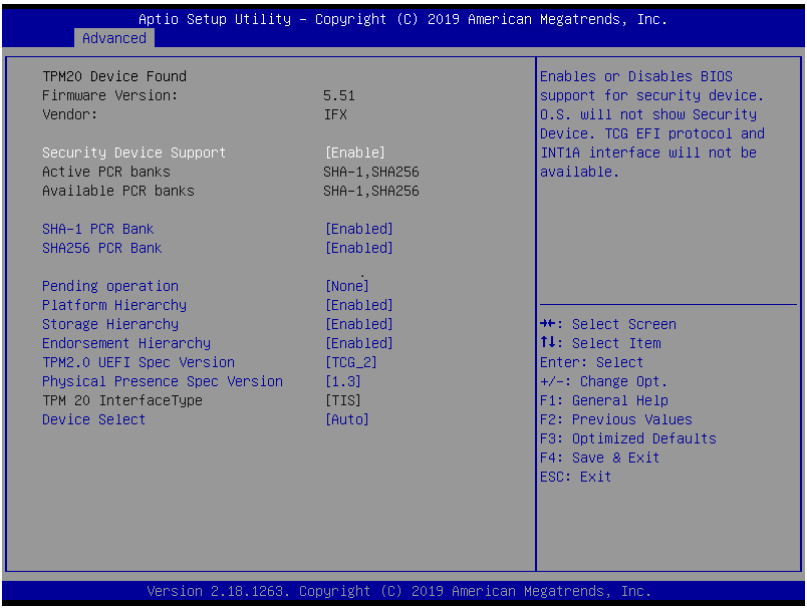
Save & Exit –Save your changes and exit system setup.

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



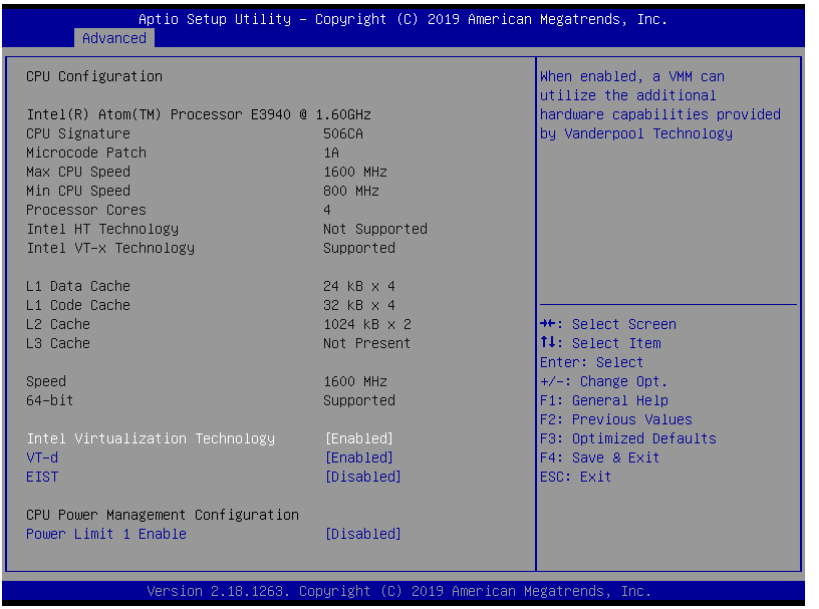
3.4.1 Advanced: Trusted Computing



Options Summary		
Security Device Support	Disabled	
	Enabled	Optimal Default, Failsafe
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable SHA256 PCR Bank.		
Pending operation	None	Optimal Default, Failsafe
	TPM Clear	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		

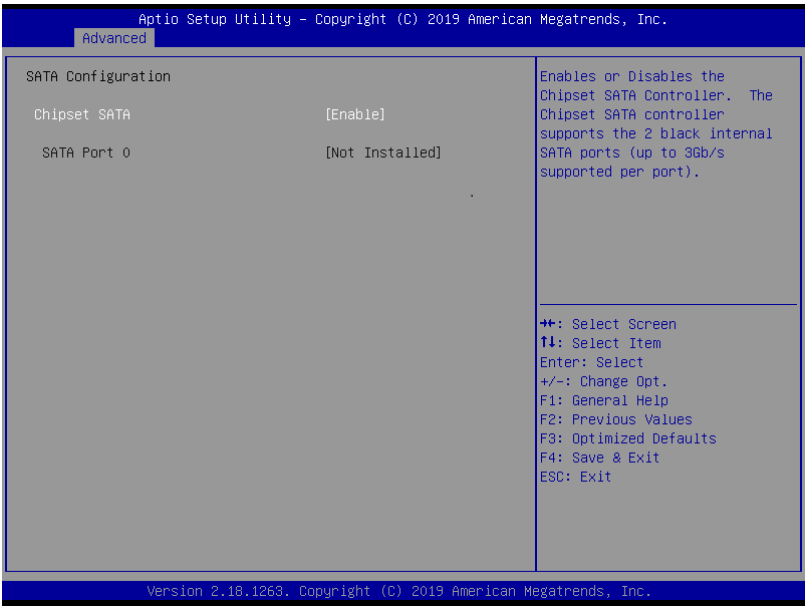
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe
Select the TCG2 Spec Version Support, TCG_1_2: Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

3.4.2 Advanced: CPU Configuration



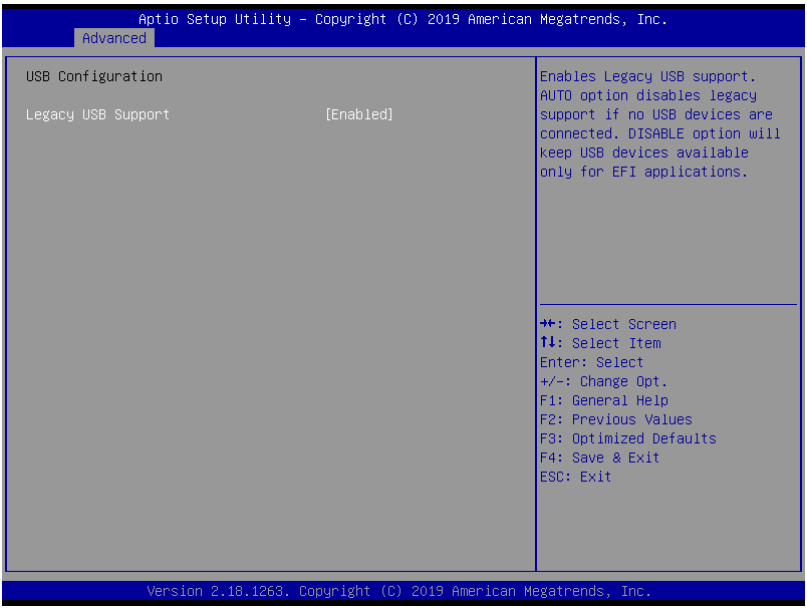
Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe
	1	
Number of cores to enable in each processor package.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		

3.4.3 Advanced: SATA Drives



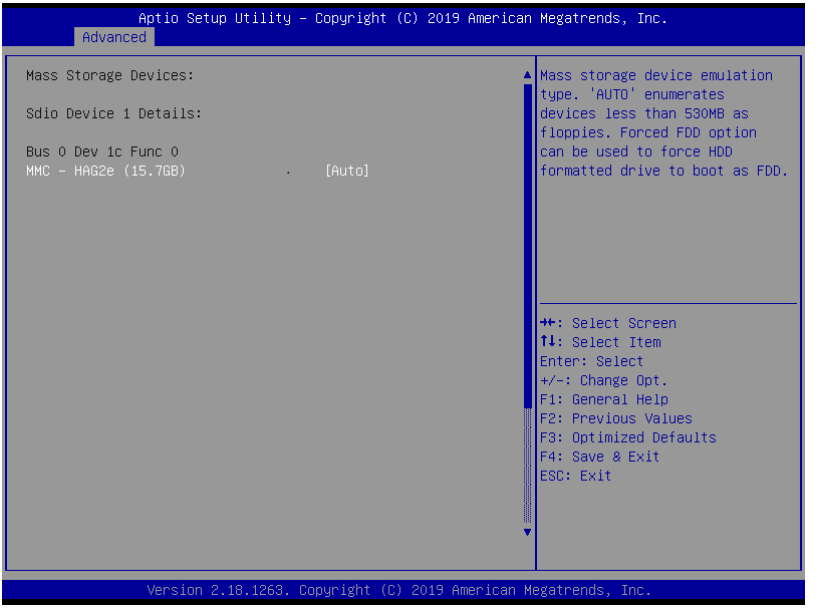
Options Summary		
Chipset SATA	Disabled	
	Enabled	Optimal Default, Failsafe
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).		

3.4.4 Advanced: USB Configuration



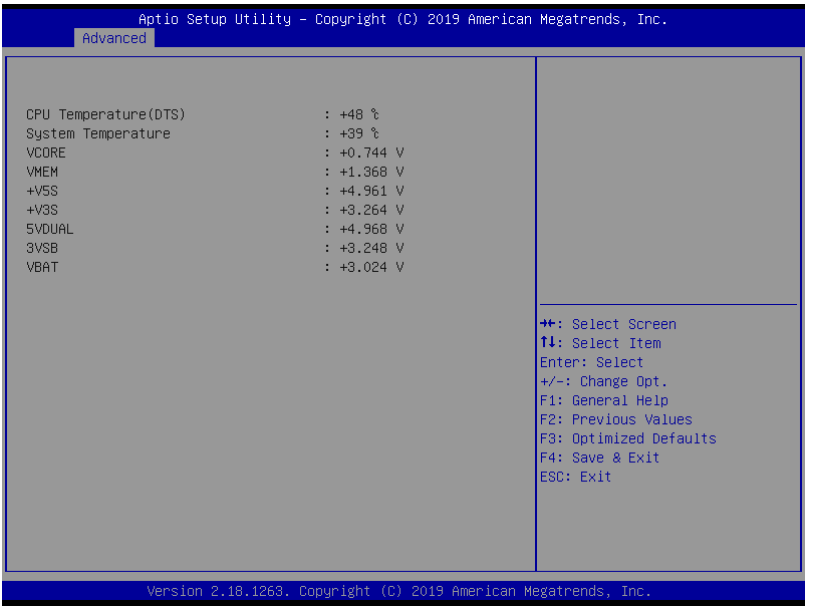
Options Summary		
Legacy USB Support	Disabled	
	Enabled	Optimal Default, Failsafe
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

3.4.5 Advanced: SDIO Configuration



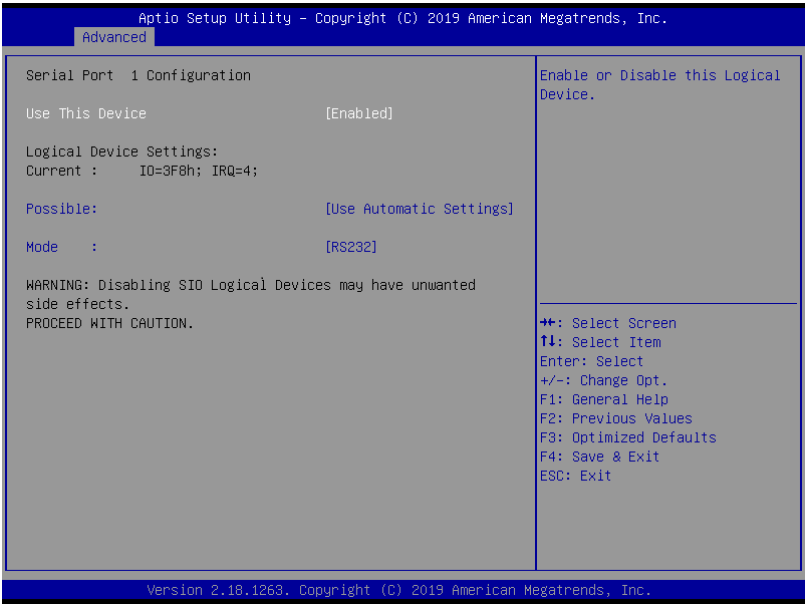
Options Summary		
Mass Storage Devices:	Auto	Optimal Default, Failsafe
	Floppy	
	Forced FDD	
	Hard Disk	
Mass storage device emulation type. 'AUTO' enumerates devices less than 530MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.		

3.4.6 Advanced: Hardware Monitor



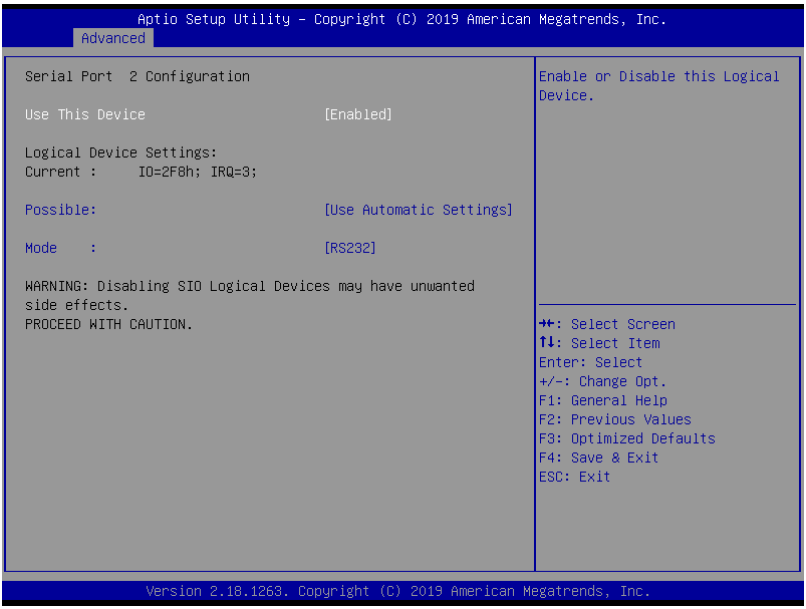
3.4.7 Advanced: SIO Configuration

3.4.7.1 Serial Port 1 Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.7.2 Serial Port 2 Configuration

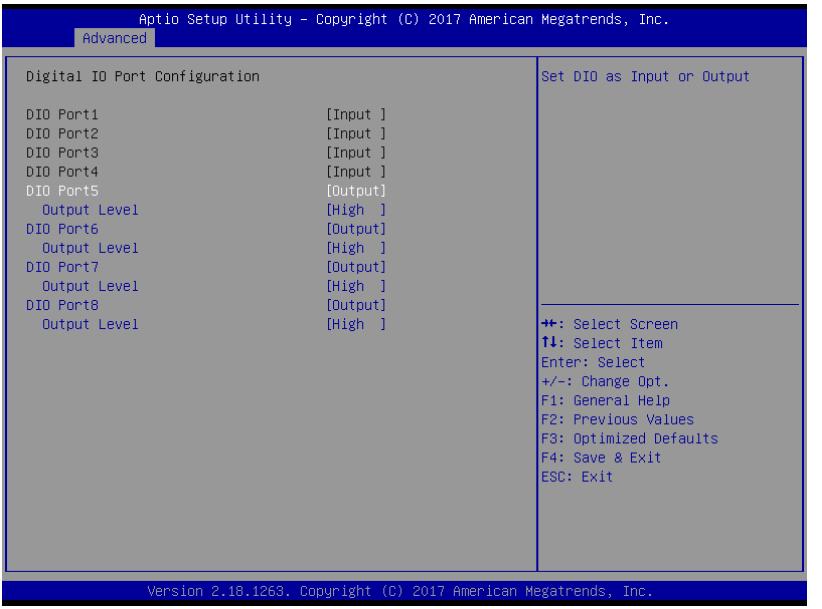


Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.8 Advanced: Power Management

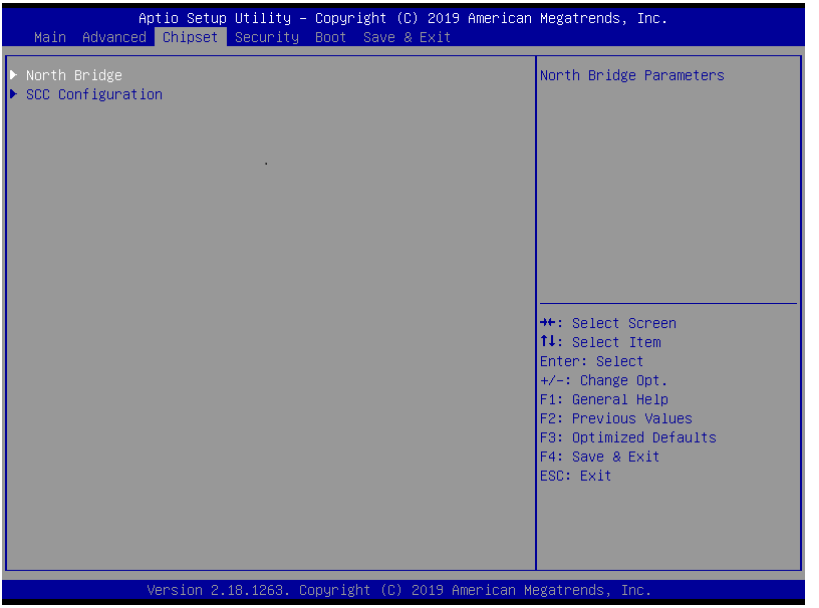
Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe
	AT Type	
Select Power Supply Mode.		
Restore AC Power Loss	Power Off	
	Power On	
	Last State	Optimal Default, Failsafe
Select AC power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

3.4.9 Advanced: Digital IO Port Configuration



Options Summary		
DIO Port5~8	Output	Optimal Default, Failsafe
	Input	
Set DIO as Input or Output.		
Output Level	Low	
	High	Optimal Default, Failsafe
Set output level when DIO pin is output.		

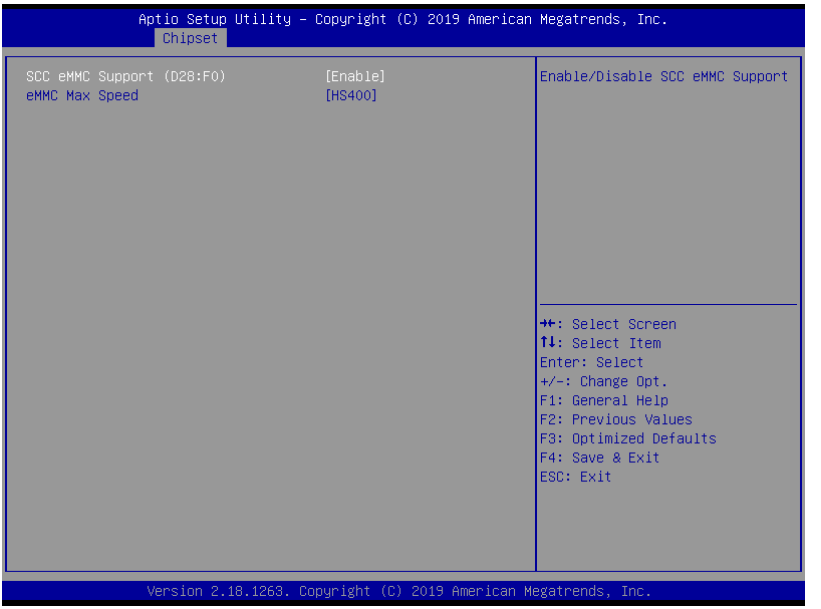
3.5 Setup submenu: Chipset



3.5.1 Chipset: North Bridge

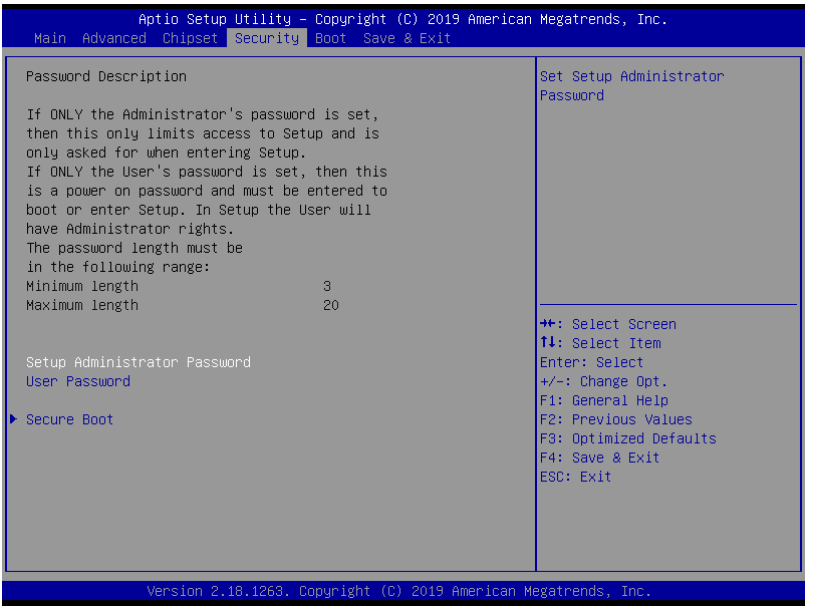
Options Summary		
Primary Display	IGD	Optimal Default, Failsafe
	PCIE	
Select which of IGD/PCI Graphics device should be Primary Display		

3.5.2 Chipset: SCC Configuration



Options Summary		
SCC eMMC Support (D28:F0)	Disabled	Optimal Default, Failsafe
	Enabled	
Enable/Disable SCC eMMC Support		
eMMC Max Speed	HS400	Optimal Default, Failsafe
	HS200	
	DDR50	
Select the eMMC max Speed allowed.		

3.6 Setup submenu: Security



Change User/Administrator Password

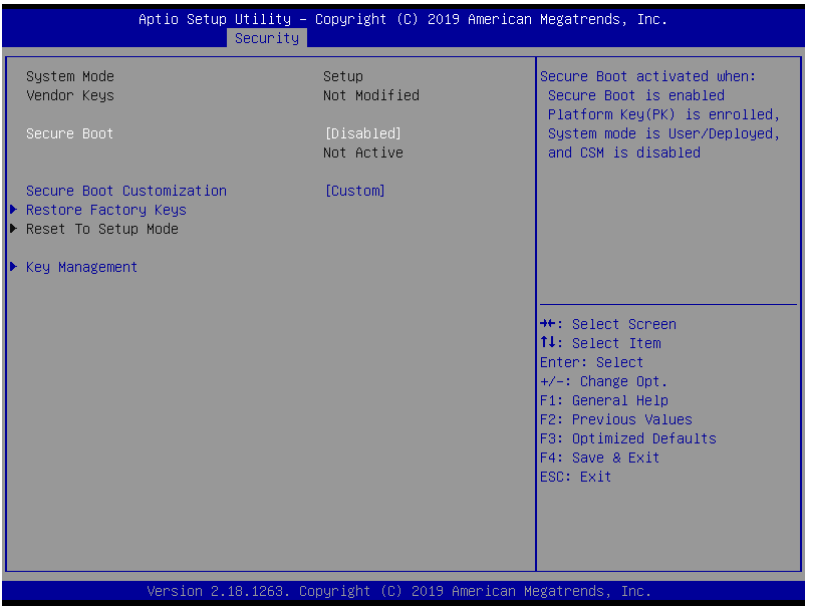
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

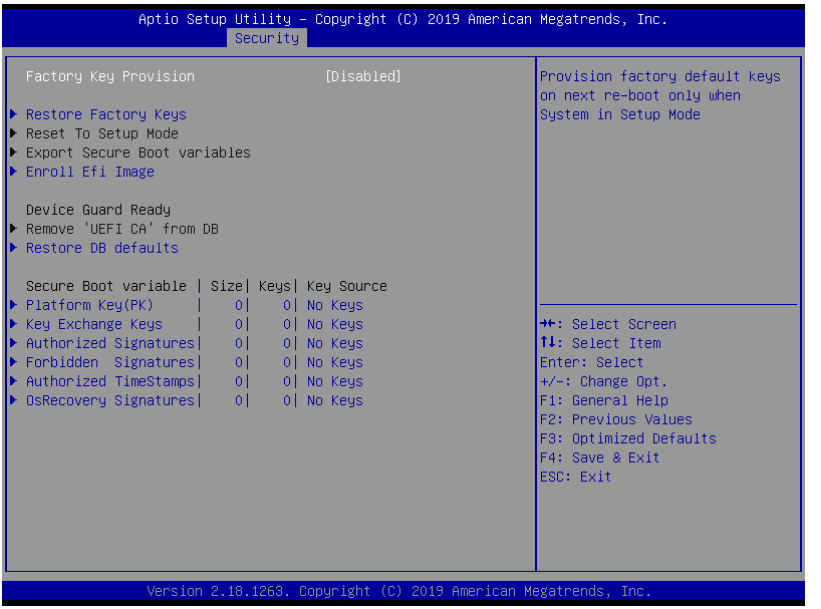
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Security: Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe
	Enabled	
Secure Boot activated when Secure Boot is enabled, Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM is disabled		
Secure Boot Customization	Custom	Optimal Default, Failsafe
	Standard	
Customizable Secure Boot mode: In Custom mode Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	Yes	Optimal Default, Failsafe
	No	
Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys		
Reset To Setup Mode	Yes	Optimal Default, Failsafe
	No	
Delete NVRAM content of all UEFI Secure Boot key databases		

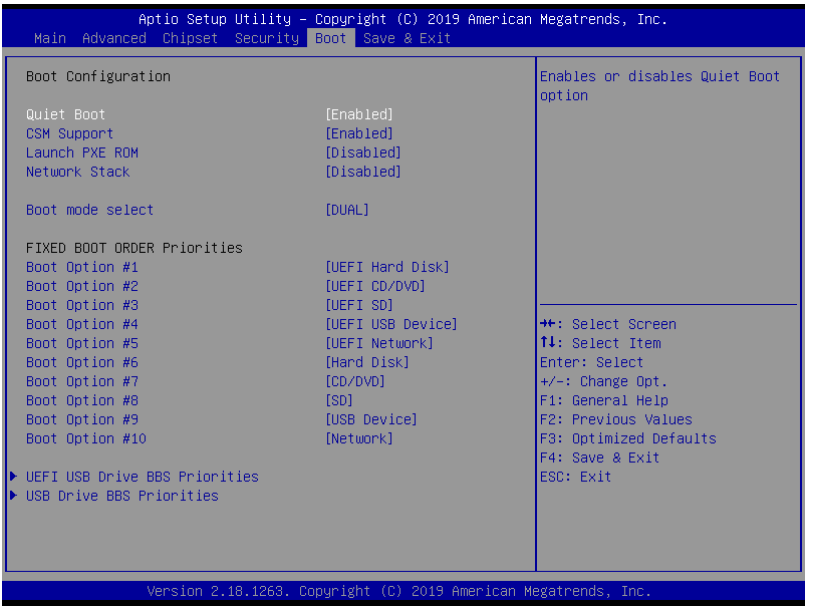
3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe
	Enabled	
Provision factory default keys on next re-boot only when System in Setup Mode		
Restore Factory Keys	Yes	Optimal Default, Failsafe
	No	
Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys		
Reset To Setup Mode	Yes	Optimal Default, Failsafe
	No	
Delete NVRAM content of all UEFI Secure Boot key databases		
Export Secure Boot variables	OK	Optimal Default, Failsafe
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		

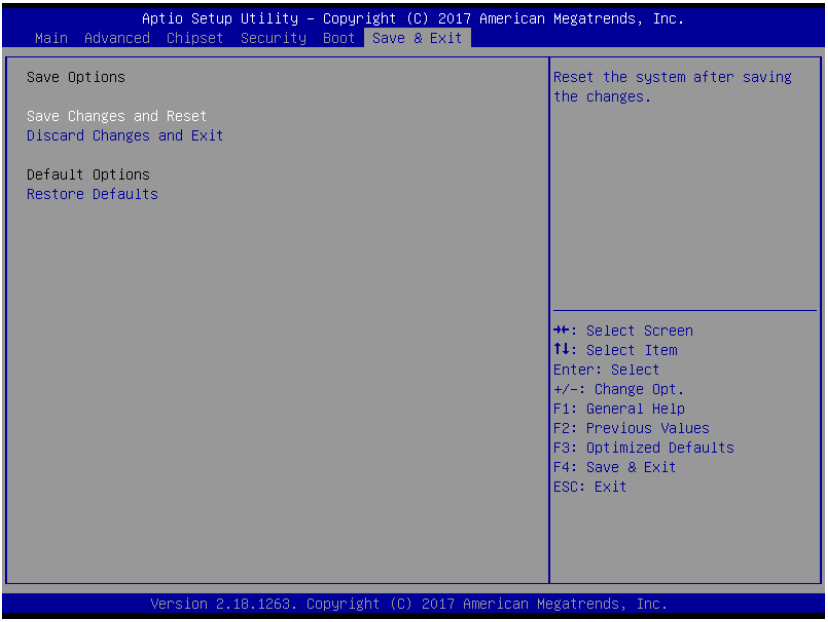
Options Summary		
Enroll Efi Image	OK	Optimal Default, Failsafe
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Remove 'UEFI CA' from DB	Yes No	Optimal Default, Failsafe
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults	Yes No	Optimal Default, Failsafe
Restore DB variable to factory defaults		
Secure Boot variable | Size| Keys| Key Source		
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed		

3.7 Setup submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe
Enables or disables Quiet Boot option.		
CSM Support	Disabled	
	Enabled	Optimal Default, Failsafe
Enable/Disable CSM Support		
Launch PXE ROM	Disabled	Optimal Default, Failsafe
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM		
Network Stack	Disabled	Optimal Default, Failsafe
	Enabled	
Enable/Disable UEFI Network Stack		

3.8 Setup submenu: Save & Exit



Chapter 4

Driver and Software Installation

4.1 Drivers Download and Installation

Drivers for the VPC-3350S can be downloaded from the product page on the AAEON website.

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Open the **Step1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Serial IO Driver

1. Open the **Step2 – Serial IO** folder and select your OS
2. Open **ReadMe.txt** and follow instructions to install driver.

Step 3 – Install Graphics Driver

1. Open the **Step3 - Graphic** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install TXE Driver

1. Open the **Step4 - TXE** folder and select your OS
2. Open the **SetupTXE.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install LAN Driver

1. Open the **Step5 - LAN** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install Serial Port Driver (optional)

1. Open the **Step6 – Serial Port Driver** folder followed by **Setup.exe** file in the folder
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

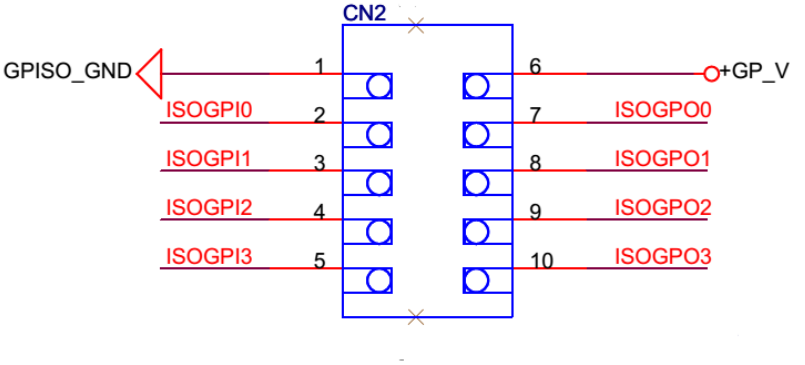
```
*****************************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************************
```

```
*********************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*********************************************************************************
```

Appendix B

Digital I/O Ports

B.1 Electrical Specifications for Digital I/O Ports



GPIO80	ISOGPI0	Input Only
GPIO81	ISOGPI1	Input Only
GPIO82	ISOGPI2	Input Only
GPIO83	ISOGPI3	Input Only
GPIO84	ISOGPO0	Output Only
GPIO85	ISOGPO1	Output Only
GPIO86	ISOGPO2	Output Only
GPIO87	ISOGPO3	Output Only

B.2 DIO Programming

The VPC-3350S utilizes FINTEK F81866D chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode

(2) Modify the data of configuration registers

(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

B.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A(Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A(Note10)	2(Note11)		GPIO82
DIO-4 Pin Status	0x06(Note12)	0x8A(Note13)	3(Note14)		GPIO83
DIO-5 Pin Status	0x06(Note15)	0x8A(Note16)	4(Note17)		GPIO84
DIO-6 Pin Status	0x06(Note18)	0x8A(Note19)	5(Note20)		GPIO85
DIO-7 Pin Status	0x06(Note21)	0x8A(Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A(Note25)	7(Note26)		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89(Note32)	1(Note33)	(Note34)	GPIO81
DIO-3 Output Data	0x06(Note35)	0x89(Note36)	2(Note37)	(Note38)	GPIO82
DIO-4 Output Data	0x06(Note39)	0x89(Note40)	3(Note41)	(Note42)	GPIO83
DIO-5 Output Data	0x06(Note43)	0x89(Note44)	4(Note45)	(Note46)	GPIO84
DIO-6 Output Data	0x06(Note47)	0x89(Note48)	5(Note49)	(Note50)	GPIO85
DIO-7 Output Data	0x06(Note51)	0x89(Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89(Note56)	7(Note57)	(Note58)	GPIO87

B.4 Digital I/O Sample Program

```
********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define  void   IOWriteByte(byte IOPort, byte Value);
#define  byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN   // This parameter is represented from Note3
#define byte   DInput1Reg   // This parameter is represented from Note4
#define byte   DInput1Bit   // This parameter is represented from Note5
#define byte   DInput2LDN   // This parameter is represented from Note6
#define byte   DInput2Reg   // This parameter is represented from Note7
#define byte   DInput2Bit   // This parameter is represented from Note8
#define byte   DInput3LDN   // This parameter is represented from Note9
#define byte   DInput3Reg   // This parameter is represented from Note10
#define byte   DInput3Bit   // This parameter is represented from Note11
#define byte   DInput4LDN   // This parameter is represented from Note12
#define byte   DInput4Reg   // This parameter is represented from Note13
#define byte   DInput4Bit   // This parameter is represented from Note14
#define byte   DInput5LDN   // This parameter is represented from Note15
#define byte   DInput5Reg   // This parameter is represented from Note16
#define byte   DInput5Bit   // This parameter is represented from Note17
#define byte   DInput6LDN   // This parameter is represented from Note18
#define byte   DInput6Reg   // This parameter is represented from Note19
#define byte   DInput6Bit   // This parameter is represented from Note20
#define byte   DInput7LDN   // This parameter is represented from Note21
#define byte   DInput7Reg   // This parameter is represented from Note22
#define byte   DInput7Bit   // This parameter is represented from Note23
#define byte   DInput8LDN   // This parameter is represented from Note24
#define byte   DInput8Reg   // This parameter is represented from Note25
#define byte   DInput8Bit   // This parameter is represented from Note26
********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*******************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //      Example, Read Digital I/O Pin 3 status
        // Output :
        //     InputStatus :
        //             0: Digital I/O Pin level is low
        //             1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //      Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*******************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************
```