



# PICO-TGU4-SEMI

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PICO-SEMI System  
User's Manual 2<sup>nd</sup> Ed

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## Packing List

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Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-TGU4-SEMI	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

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This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page on [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

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Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
18. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.**

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 此产品所标示之环保使用期限, 系指在一般正常使用状况下。</p>						

## China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
<p>O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.</p> <p>X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.</p> <p><b>Note:</b> The Environment Friendly Use Period as labeled on this product is applicable under normal usage only</p>						

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# Chapter 1

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Product Specifications

## 1.1 Specifications

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### System

Form Factor	PICO-ITX
CPU	11th Generation Intel® Core™ i7/i5/i3/Celeron SoC
CPU Frequency	Up to 4.4GHz
Chipset	11th Generation Intel® Core™ i7/i5/i3/Celeron SoC
Memory Type	LPDDR4x 3200 MHz on board memory, In-Band ECC (select SKUs)
Max. Memory Capacity	Up to 32GB
BIOS	AMI UEFI
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V ATX
Power Supply Type	Lockable DC Jack
Power Consumption (Typical)	2.89A at +12V, i7-1185G7E, LPDDR4x on board 32GB
System Cooling	Cooler
Dimension	4.80" x 3.18" x 1.98" (122mm x 80.8mm x 50.4 mm)
Gross Weight	0.84 lbs. (0.38 kg)
Operating Temperature	32°F ~ 122°F (0°C ~ 50°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	424,208
Certification	CE/FCC Class A

## Display

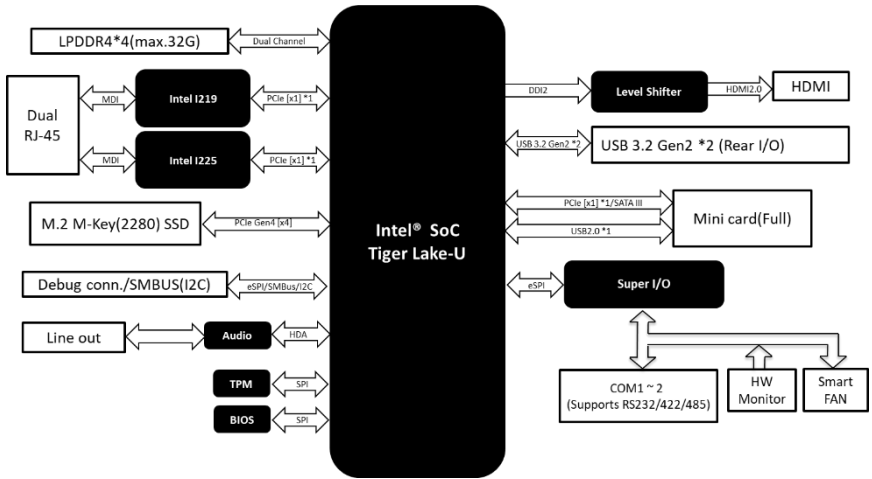
Chipset	Intel® Iris® Xe (i5/i7 support) Intel® UHD Graphics (i3/Celeron support)
Resolution	HDMI 2.0b x 1, 4k x 2k 60Hz
LCD Interface	—

## I/O

Ethernet	Intel® i225, 10/100/1000/2500Base, RJ45 x1 Intel® i219, 10/100/1000Base, RJ45 x1
USB Port	USB3.2 Gen 2 x 2
Serial Port	RS-232/422/485 x 2 (Optional)
Audio	High Definition Audio Interface, Line-out (Optional)
Expansion Slot	M.2 M Key 2280 x 1 (PCIe Gen 4 [x4] as default, SATA select by HW BOM) Full size mSATA/mPCIe or USB2.0 x 1 (mSATA as default, select by BIOS option) SMBUS/I2C/eSPI x 1 (SMBUS as default, I2C select by BOM)
SIM	—
TPM	2.0 (Optional)
Touch	—



## 1.2 Function Block Diagram



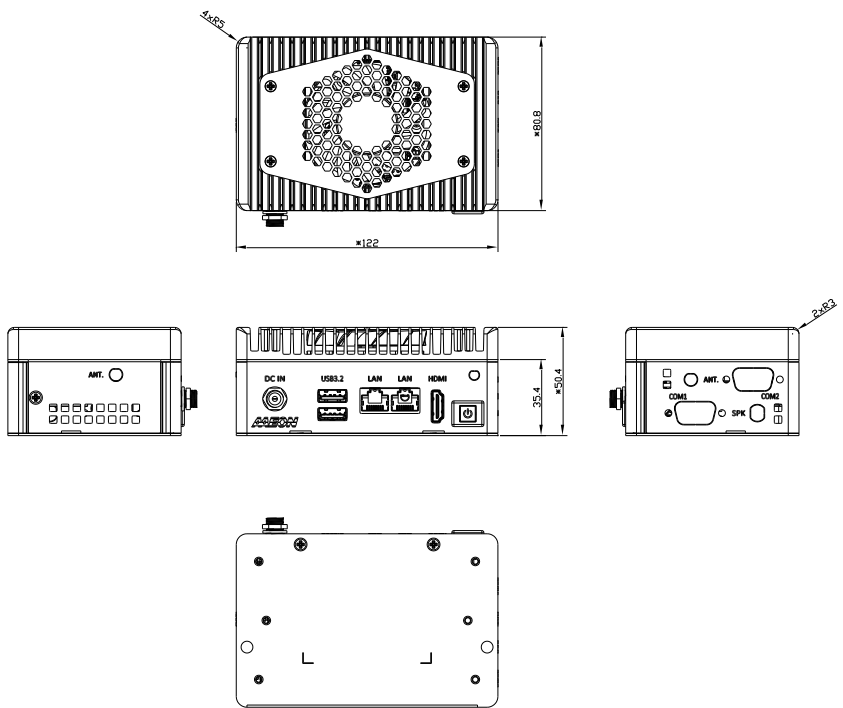
# Chapter 2

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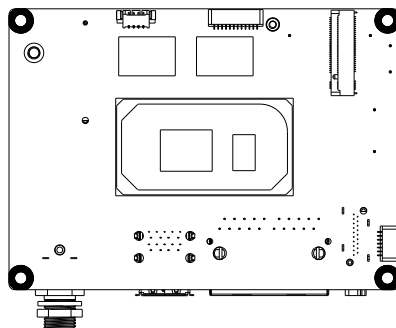
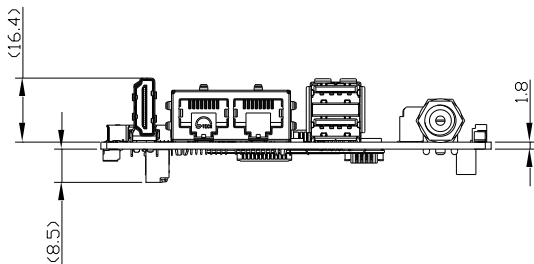
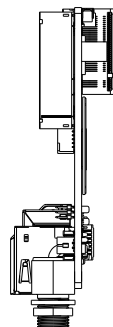
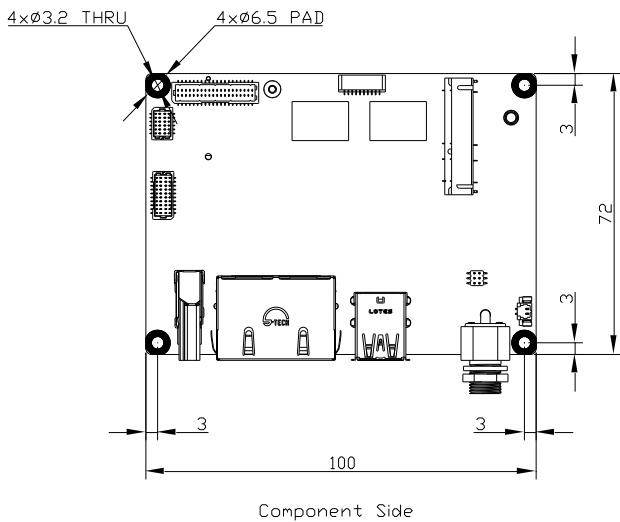
Hardware Information

## 2.1 Dimensions

### System – Lite Version

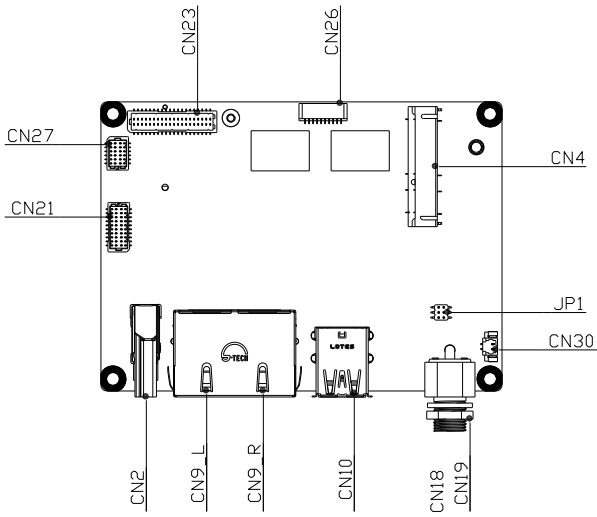


Board

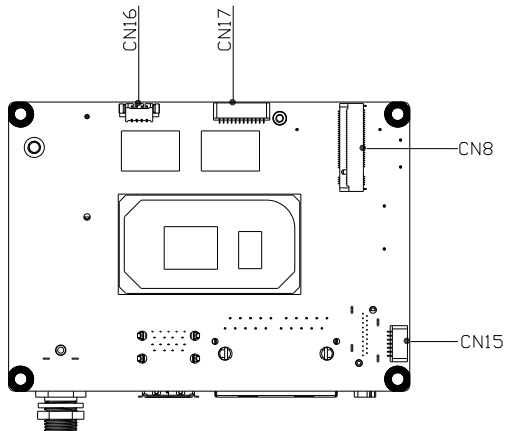


## 2.2 Jumpers and Connectors

### Component Side



### Solder Side



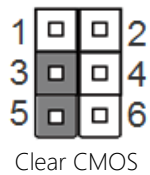
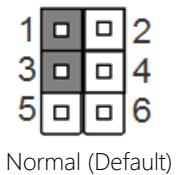
## 2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

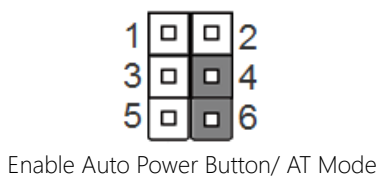
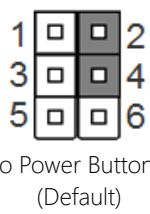
Label	Function
JP1	Clear CMOS Jumper, Auto Power Button Selection

### 2.3.1 Clear CMOS Jumper, Auto Power Button Selection (JP1)

Clear CMOS Jumper



Auto Power Button Enable/Disable Selection



**Note:** To avoid damage to the system, do not connect pins 1,3,5 with pins 2,4,6.

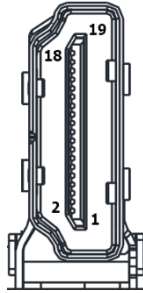
## 2.4 List of Connectors

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Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN2	HDMI Connector
CN4	Mini Card Slot (Full Size)
CN8	M.2 2280 M-Key Slot
CN9-L	Intel i225 2.5Gbps RJ-45 (Port A)
CN9-R	Intel i219 1Gbps RJ-45 (Port B)
CN10	USB3.2 Gen 2 Dual Port (Rear IO)
CN15	SPI Flash Programing Port
CN16	Smart Fan
CN17	eSPI Port (SMBus)
CN19	+12V DC Jack
CN21	USB3.2 Gen 1 Dual Port Header
CN23	Dual COM Port
CN26	Front Panel
CN27	Audio I/O Port
CN30	CMOS Battery Connector

## 2.4.1 HDMI Port (CN2)

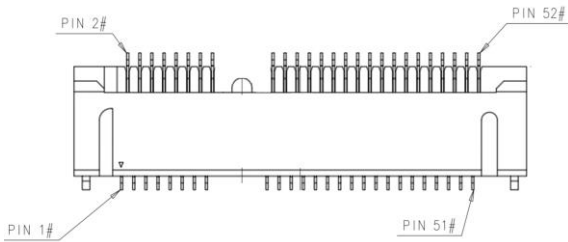


Pin	Pin Name	Signal Type	Signal Level
1	HDMI1_TX2+	DIFF	
2	GND	GND	GND
3	HDMI1_TX2-	DIFF	
4	HDMI1_TX1+	DIFF	
5	GND	GND	GND
6	HDMI1_TX1-	DIFF	
7	HDMI1_TX0+	DIFF	
8	GND	GND	GND
9	HDMI1_TX0-	DIFF	
10	HDMI1_CLK+	DIFF	
11	GND	GND	GND
12	HDMI1_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	GND



Pin	Pin Name	Signal Type	Signal Level
18	+5V	PWR	+5V
19	HDMI1_HPD		

## 2.4.2 Mini-Card Slot (Full-Size) (CN4)

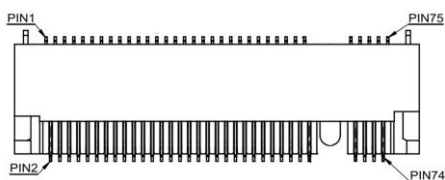


Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC	NC	
4	GND	GND	
5	NC	NC	
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
16	UIM_VPP	PWR	
17	NC	NC	
18	GND	GND	
19	NC	NC	
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
42	NC	NC	
43	GND	GND	
44	NC	NC	
45	NC	NC	
46	NC	NC	
47	NC	NC	
48	+1.5V	PWR	+1.5V
49	NC	NC	
50	GND	GND	
51	NC	NC	
52	+3.3VSB	PWR	+3.3V

### 2.4.3 M.2 2280 M-Key Slot (CN8)



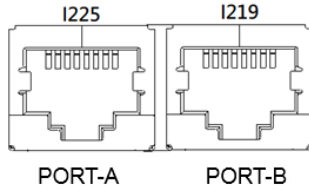
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+3.3V	PWR	+3.3V
3	GND	GND	
4	+3.3V	PWR	+3.3V
5	PCIE3_RX-	DIFF	
6	NC		
7	PCIE3_RX+	DIFF	
8	NC		

Pin	Pin Name	Signal Type	Signal Level
9	GND	GND	
10	SATA_LED	IN	+3.3V
11	PCIE3_TX-	GND	
12	+3.3V	PWR	+3.3V
13	PCIE3_TX+	GND	
14	+3.3V	PWR	+3.3V
15	GND	GND	
16	+3.3V	PWR	+3.3V
17	PCIE2_RX-	DIFF	
18	+3.3V	PWR	+3.3V
19	PCIE2_RX+	DIFF	
20	NC		
21	GND	GND	
22	NC		
23	PCIE2_TX-	DIFF	
24	NC		
25	PCIE2_TX+	DIFF	
26	NC		
27	GND	GND	
28	NC		
29	PCIE1_RX-	DIFF	
30	NC		
31	PCIE1_RX+	DIFF	
32	NC		
33	GND	GND	
34	NC		

Pin	Pin Name	Signal Type	Signal Level
35	PCIE1_TX-	DIFF	
36	NC		
37	PCIE1_TX+	DIFF	
38	DECSLP	OUT	
39	GND	GND	
40	NC		
41	PCIE0_RX-	DIFF	
42	NC		
43	PCIE0_RX+	DIFF	
44	NC		
45	GND	GND	
46	NC		
47	PCIE0_TX-	DIFF	
48	NC		
49	PCIE0_TX+	DIFF	
50	PERST#	OUT	
51	GND	GND	
52	PCIE_CLK_REQ#	IN	
53	PCIE_CLK-	DIFF	
54	PCIE_WAKE	IN	
55	PCIE_CLK+	DIFF	
56	NC		
57	GND	GND	
58	NC		
67	NC		
68	NC		

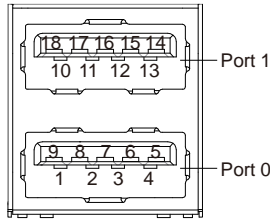
Pin	Pin Name	Signal Type	Signal Level
69	NC		
70	+3.3V	PWR	+3.3V
71	GND	GND	
72	+3.3V	PWR	+3.3V
73	GND	GND	
74	+3.3V	PWR	+3.3V
75	GND	GND	

## 2.4.4 Dual LAN (RJ-45) Intel i225 (Port A)/ Intel i219 (Port B) (CN9)



Port A (i225)		Port B (i219)	
Pin	Pin Name	Pin	Pin Name
1P1	LAN2_MDIO_P	2P1	LAN1_MDIO_P
1P2	LAN2_MDIO_N	2P2	LAN1_MDIO_N
1P3	LAN2_MDI1_P	2P3	LAN1_MDI1_P
1P4	LAN2_MDI1_N	2P4	LAN1_MDI1_N
1P5	1CT5	2P5	2CT5
1P6	1CT6	2P6	2CT6
1P7	LAN2_MDI2_P	2P7	LAN1_MDI2_P
1P8	LAN2_MDI2_N	2P8	LAN1_MDI2_N
1P9	LAN2_MDI3_P	2P9	LAN1_MDI3_P
1P10	LAN2_MDI3_N	2P10	LAN1_MDI3_N

## 2.4.5 Dual USB3.2 Gen 2 Ports (Port 1/ Port 2) (CN10)

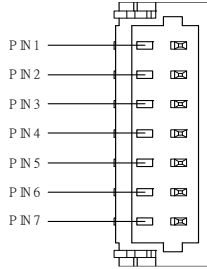


Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	GND
5	USB0_SSRX-	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	GND
8	USB0_SSTX-	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	GND
14	USB1_SSRX-	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	GND
17	USB1_SSTX-	DIFF	
18	USB1_SSTX+	DIFF	

**Note:** CN10 USB Power max current: 2.0A, 1.0A for each port

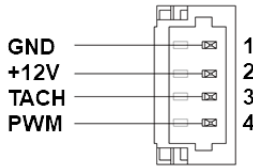


## 2.4.6 SPI Flash Programming Port (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

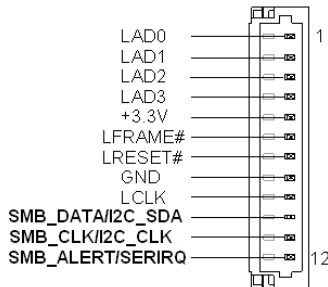
## 2.4.7 FAN Connector (CN16)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V12S	PWR	+12V
3	TACH	IN	
4	PWM	OUT	

**Note:** CN16 Smart Fan power max current: 1.0A.

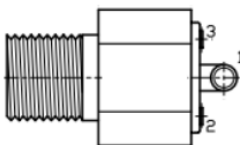
## 2.4.8 eSPI Debug Port (CN17)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V

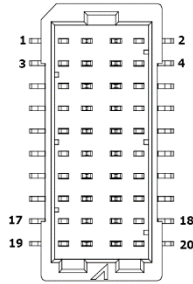
Pin	Pin Name	Signal Type	Signal Level
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA/ I2C_SDA	I/O	
11	SMB_CLK/ I2C_CLK	OUT	
12	SMB_ALERT/ SERIRQ	IN	+3.3V

## 2.4.9 +12V DC Jack (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	GND

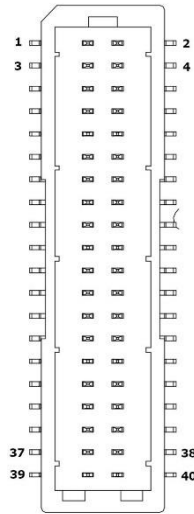
## 2.4.10 USB3.2 Gen 1 Dual Port Header (CN21)



Pin	Pin Name	Pin	Pin Name
1	5V_USB	2	5V_USB
3	USB2_9_DN	4	USB2_10_DN
5	USB2_9_DP	6	USB2_10_DP
7	GND	8	GND
9	USB3_1_RXN	10	USB3_4_RXN
11	USB3_1_RXP	12	USB3_4_RXP
13	GND	14	GND
15	USB3_1_TXN	16	USB3_4_TXN
17	USB3_1_TXP	18	USB3_4_TXP
19	GND	20	GND

**Note:** CN21 USB Power max current: 2.0A, 1.0A for each port

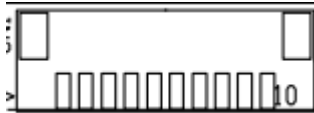
## 2.4.11 DIO 4bit/ COM Dual Port/ USB2.0 x 4 Header (CN23)



Pin	Pin Name	Pin	Pin Name
1	DIO_0	2	DIO_1
3	DIO_2	4	DIO_3
5	GND	6	5V
7	DCD_1_CON	8	DCD_2_CON
9	RX_1_CON	10	RX_2_CON
11	TX_1_CON	12	TX_2_CON
13	DTR_1_CON	14	DTR_2_CON
15	DSR_1_CON	16	DSR_2_CON
17	RTS_1_CON	18	RTS_2_CON
19	CTS_1_CON	20	CTS_2_CON
21	RI_1_CON	22	RI_2_CON
23	GND	24	GND

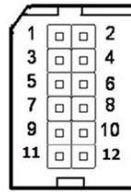
Pin	Pin Name	Pin	Pin Name
25	5V_USB	26	5V_USB
27	USB2_5_DN	28	USB2_6_DN
29	USB2_5_DP	30	USB2_6_DP
31	GND	32	GND
33	5V_USB	34	5V_USB
35	USB2_7_DN	36	USB2_8_DN
37	USB2_7_DP	38	USB2_8_DP
39	GND	40	GND

### 2.4.12 Front Panel (CN26)



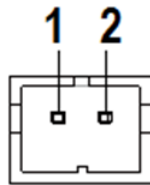
Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	BUZZER-	6	BUZZER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

### 2.4.13 Audio I/O Port (CN27)



Pin	Pin Name	Signal	Pin	Pin Name	Signal
1	LOUT_R	OUT	2	MIC_L	IN
3	LOUT_L	OUT	4	MIC_R	IN
5	JD_LOUT	IN	6	JD_MIC	IN
7	AUD_GND	GND	8	AUD_GND	GND
9	LINE_R_IN	IN	10	LIN_R	IN
11	+VDD_AUD	PWR	12	LIN_L	IN

### 2.4.14 RTC Battery Connector (CN30)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+3.3V	PWR	+3.3V

# Chapter 3

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AMI BIOS Setup



## 3.1 System Test and Initialization

---

The PICO-TGU4-SEMI uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or display an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the system will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-TGU4 CMOS memory has an integrated lithium battery backup for data retention. The battery must be replaced when it runs down.

## 3.2 AMI BIOS Setup

---

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations. These configurations are stored in the battery-backed CMOS RAM and BIOS NVRAM so the information is retained when power is turned off.

To enter BIOS Setup, turn on the system and immediately press <Del> or <ESC>.

The following BIOS menus and their functions are listed below.

**Main:** Set the date, use tab to switch between date elements.

**Advanced:** Enable/ disable boot options for legacy network devices.

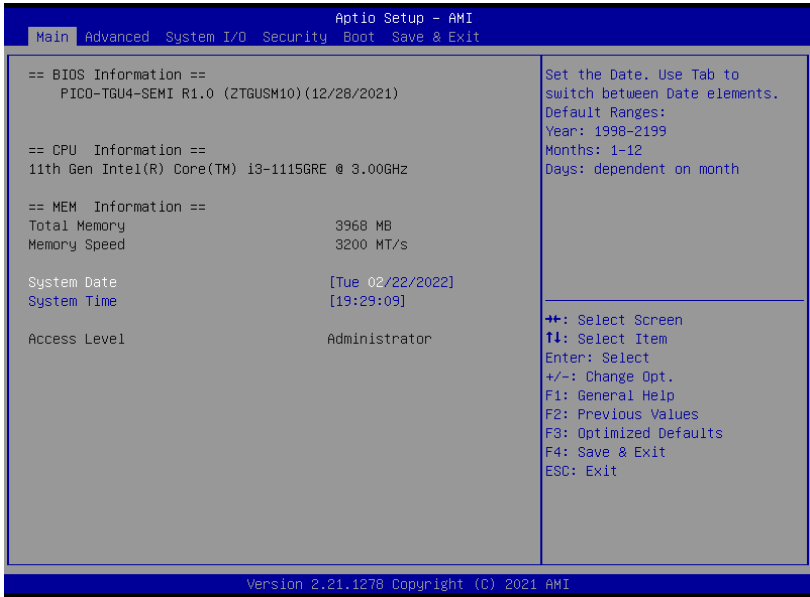
**System I/O:** Access I/O device settings, such as PCI Express, Serial Port, and Storage.

**Security:** Set setup administrator password and manage Secure Boot and Trusted Computing settings.

**Boot:** Boot Options, including Quiet Boot and BBS Priorities.

**Save & Exit:** Save changes to BIOS settings and exit BIOS program. Note: The system may need to restart for some changes to take effect.

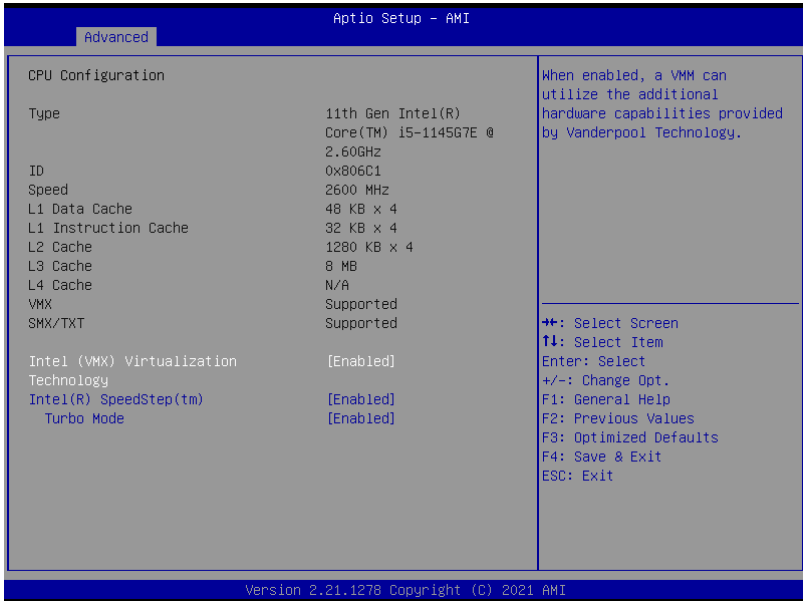
### 3.3 Setup Submenu: Main



### 3.4 Setup Submenu: Advanced



### 3.4.1 CPU Configuration



Options Summary		
Intel (VMX) Virtualization Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.		

### 3.4.2 Memory Configuration



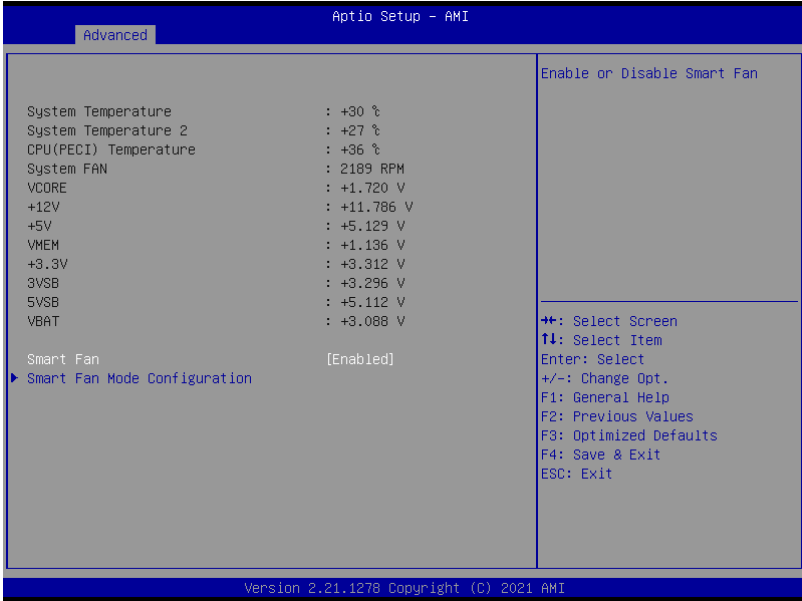
#### In-Band ECC Support

<b>In-Band ECC Support</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled In-Band ECC Support		
<b>In-Band ECC Error Injection</b>	Enabled	Optimal Default, Failsafe Default
	Disabled	
By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions.		
<b>In-Band ECC Operation Mode</b>	0	Optimal Default, Failsafe Default
	1	
	2	
0: Functional Mode protects requests based on the address range, 1: Makes all requests non protected and ignore range checks, 2: Makes all requests protected and ignore range checks		

Table Continues on Next Page...

IBECC Protect Region 0-7	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled In-Band ECC for Region 0-7		

### 3.4.3 Hardware Monitor



Options Summary		
Smart Fan	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Smart Fan		



### 3.4.3.1 Smart Fan Mode Configuration

#### Auto Duty-Cycle Mode

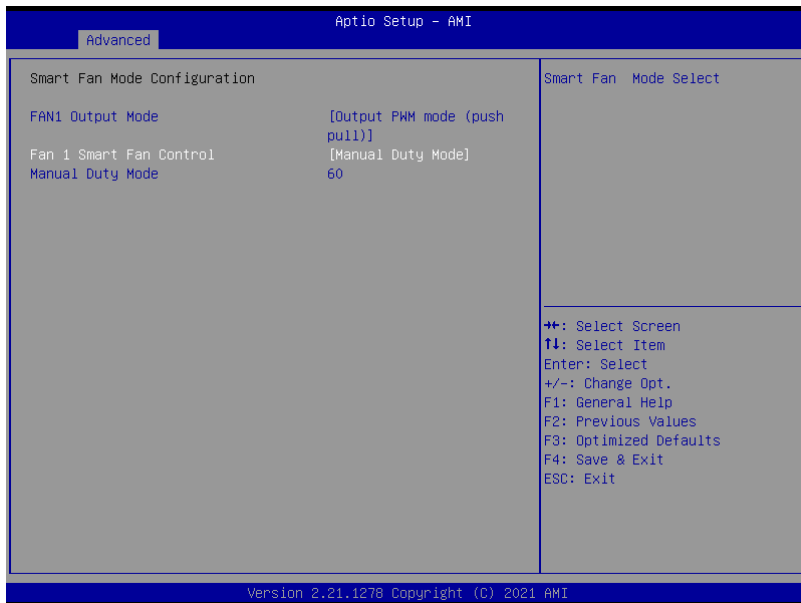
Advanced		Aptio Setup - AMI	
Smart Fan Mode Configuration		Output PWM mode (push pull) to control 4-wire fans. Linear fan application circuit to control 3-wire fan speed by fan's power terminal. Output PWM mode (open drain) to control Intel 4-wire fans.	
FAN1 Output Mode	[Output PWM mode (push pull)]	+*: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Fan 1 Smart Fan Control	[Auto Duty-Cycle Mode]		
Temperature Source	[CPU(PECI) Temperature]		
Temperature 1	60		
Temperature 2	50		
Temperature 3	40		
Temperature 4	30		
Duty Cycle 1	85		
Duty Cycle 2	70		
Duty Cycle 3	60		
Duty Cycle 4	50		
Duty Cycle 5	40		

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Options Summary		
<b>FAN1 Output Mode</b>	Output PWM mode (push pull)	Optimal Default, Failsafe Default
	Linear Fan Application	
	Output PWM mode (open drain)	
Output PWM mode (push pull) to control 4-wire fans. Linear fan application circuit to control 3-wire fan speed by fan's power terminal. Output PWM mode (open drain) to control Intel 4-wire fans.		
<b>Fan 1 Smart Fan Control</b>	Manual Duty Mode	Optimal Default, Failsafe Default
	Auto Duty-Cycle Mode	
<b>Smart Fan Mode Select</b>		
<b>Temperature Source</b>	CPU(PECI) Temperature	Optimal Default, Failsafe Default
	System Temperature 2	
	System Temperature	

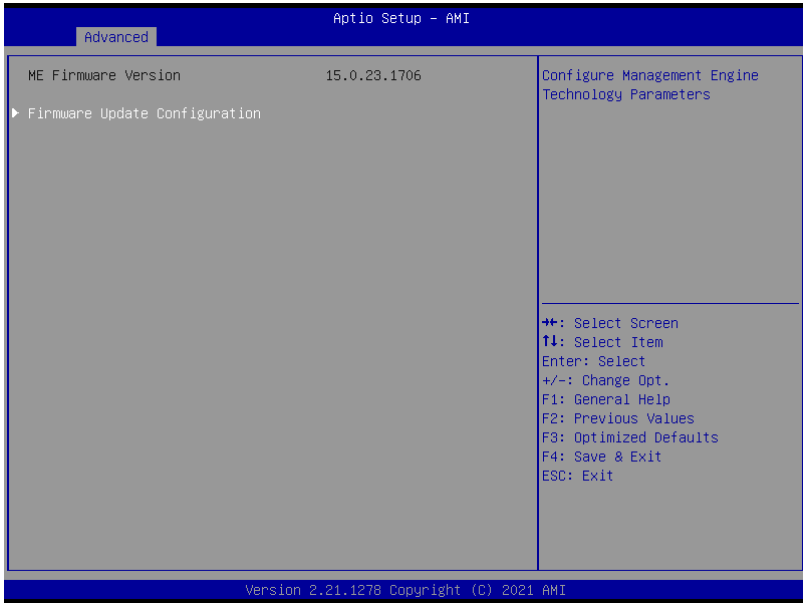
Options Summary	
Select the monitored temperature source for this fan.	
Duty Cycle	Auto fan speed control. Fan speed will follow different
Temperature	temperature by different duty cycle 1-100

## Manual Duty Mode

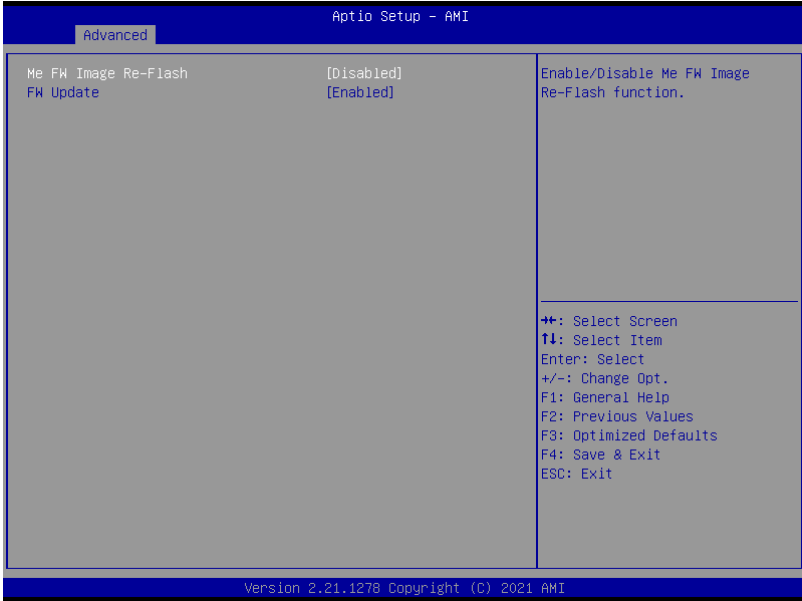


Options Summary		
Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100		

### 3.4.4 PCH-FW Configuration

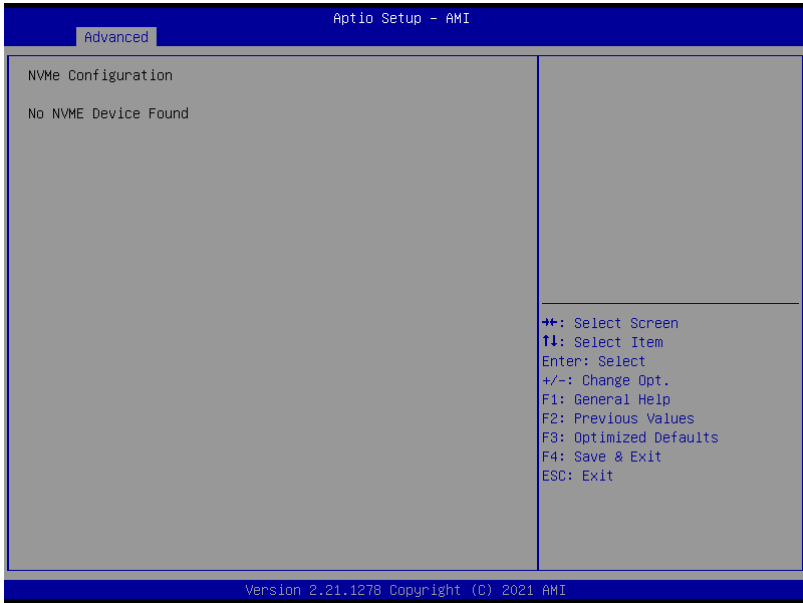


### 3.4.4.1 Firmware Update Configuration



Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable ME FW Update function.		

### 3.4.5 NVMe Configuration

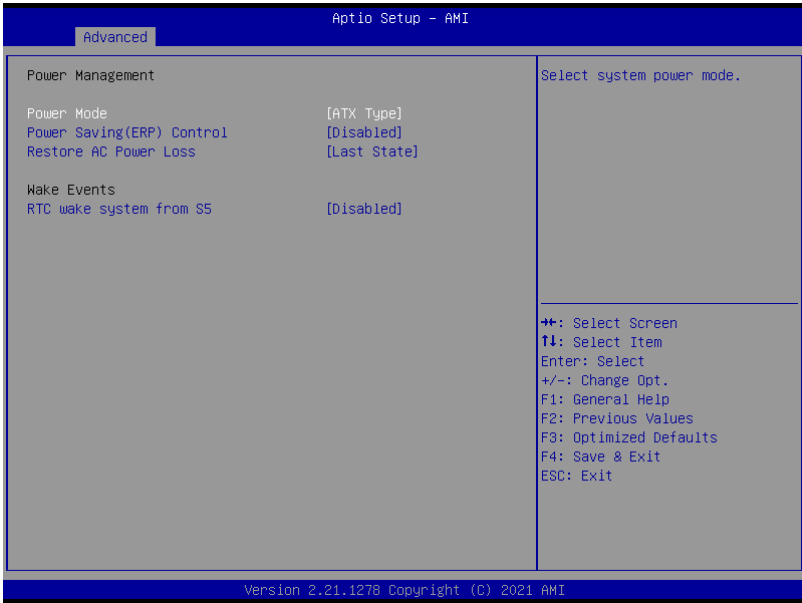


# TSN BGE Configuration



Options Summary:		
PCH TSN LAN	Enabled	Optimal Default, Failsafe Default
Contriller	Disabled	
En/Dis TSN LAN		
Enable Timed TSN PCS	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/DisTSN PCS. When enabled, TSN PCS device will appear in ACPI table		
PCH TSN Milti-Vc	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Dis PCH TSN Multi Virtual Channels		
PCH TSN Port #1 Link Speed	RefClk 24Mhz 2.5Gbps	
	RefClk 24Mhz 1Gbps	Optimal Default, Failsafe Default
	RefClk 38.4Mhz 2.5Gbps	
	RefClk 38.4Mhz 1Gbps	
PCH TSN Link Speed config		

### 3.4.6 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Power Saving(ERP) Control	Enabled	Optimal Default, Failsafe Default
	Disabled	
Configure power mode for power saving function.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
IO Restore AC power Loss		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	

Table Continues on Next Page...

### Options Summary

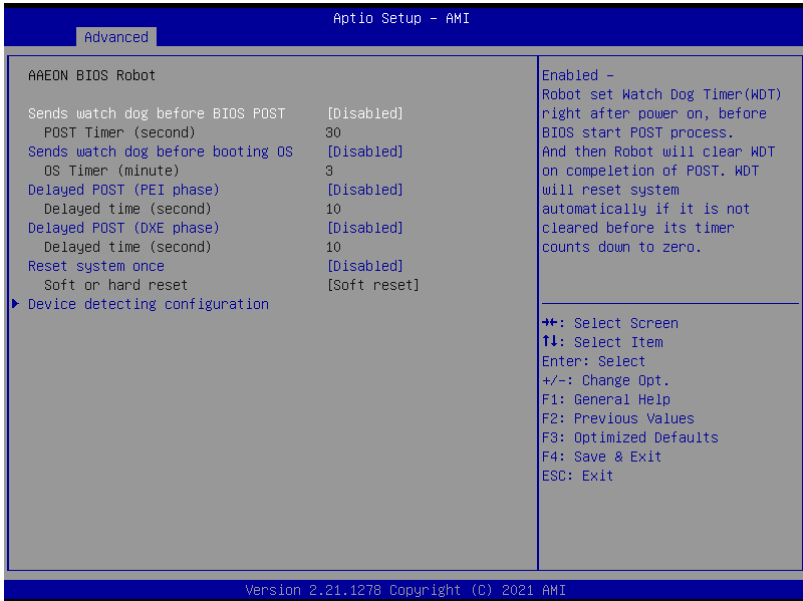
Fixed Time: System will wake on the hr::min::sec specified.

Dynamic Time: System will wake on the current time + Increase minute(s).

Bypass: BIOS will not control RTC wake function during system shutdown



### 3.4.7 AAEON BIOS Robot



Options Summary		
<b>Sends watch dog before BIOS POST</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) right after power on, before BIOS start POST process. And then Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.		
<b>POST Timer (second)</b>	30	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for POST. WARNING: Do not set to a value equal or shorter than normal POST time, otherwise system may never complete POST unless clearing BIOS settings. More than 2x normal POST time is suggested.		
<b>Sends watch dog before booting OS</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	

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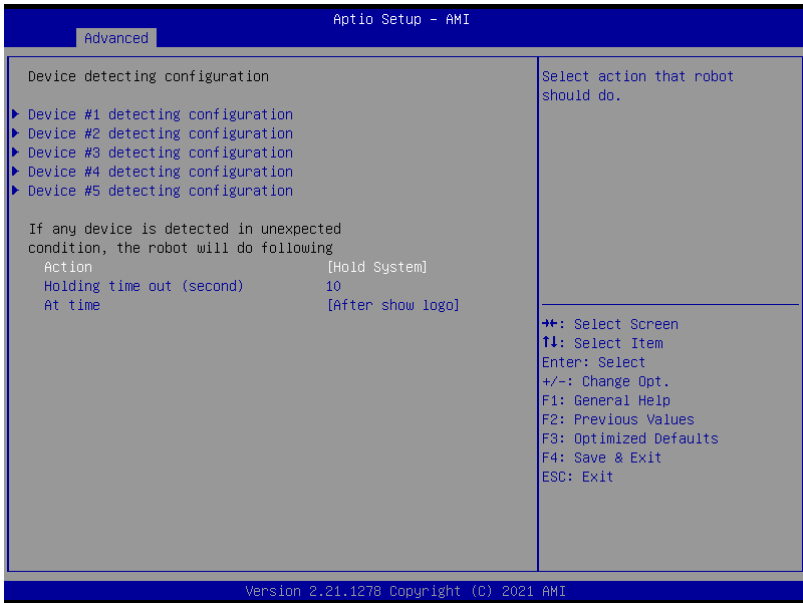
Options Summary		
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfer control to OS. WARNING: Before enabling this function, a program in OS must be in responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		
<b>OS Timer (minute)</b>	3	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for OS loading.		
<b>Delayed POST (PEI phase)</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.		
<b>Delayed time (second)</b>	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
<b>Delayed POST (DXE phase)</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this after 'Sends watch dog before BIOS POST'.		
<b>Delayed time (second)</b>	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
<b>Reset system once</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		
<b>Soft or hard reset</b>	Soft reset	Optimal Default, Failsafe Default
	Hard reset"	
Select reset type robot should send on each boot.		

### 3.4.7.1 Device Detecting Configuration



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do action after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

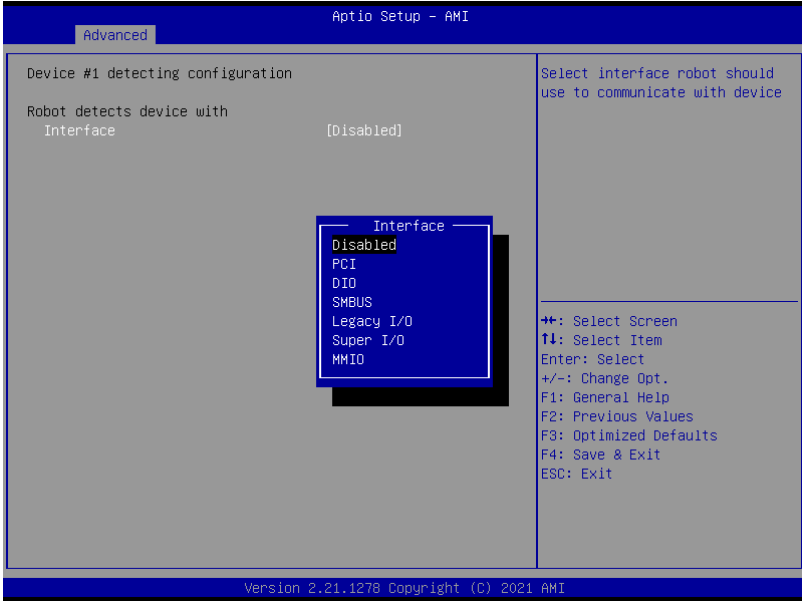
## Action: Hold System



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Holding time out (second)	10	Optimal Default, Failsafe Default
Fill hold time out here. Robot will hold system no longer then time-out value, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do action after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

### 3.4.7.1.1 Device #X Detecting Configuration

#### Interface: Disabled



Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

## Interface: PCI

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Advanced

Device #1 detecting configuration		Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.
Robot detects device with		
Interface	[PCI]	
BUS	0	
Device	0	
Function	0	
Expecting		
Device	[is not]	
In condition	[Specified register data]	
Register data is	[bitwise equal to]	
Register offset	0	
Bit offset	0	
Bit value	[Low]	

++: Select Screen  
 ↓: Select Item  
 Enter: Select  
 +/-: Change Opt.  
 F1: General Help  
 F2: Previous Values  
 F3: Optimized Defaults  
 F4: Save & Exit  
 ESC: Exit

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Options Summary		
<b>BUS</b>	0	Optimal Default, Failsafe Default
Fill BUS number to a PCI device, in hexadecimal. Range: 0 - FF		
<b>Device</b>	0	Optimal Default, Failsafe Default
Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 - FF		
<b>Function</b>	0	Optimal Default, Failsafe Default
Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 - FF		
<b>Device</b>	is	Optimal Default, Failsafe Default
	Is not	
Select that robot should or should not do action if condition met.		
<b>In condition</b>	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

*Table Continues on Next Page...*

Options Summary		
<b>Register data is</b>	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		
<b>Register offset</b>	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
<b>Bit offset</b>	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
<b>Bit value</b>	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
<b>Byte value</b>	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

## Interface: SMBUS

Advanced		Aptio Setup - AMI
Device #1 detecting configuration		Select interface robot should use to communicate with device
Robot detects device with		
Interface	[SMBUS]	++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
SMBUS Slave Address	0	
Expecting		
Device	[is not]	
In condition	[Specified register data]	
Register data is	[bitwise equal to]	
Register offset	0	
Bit offset	0	
Bit value	[Low]	

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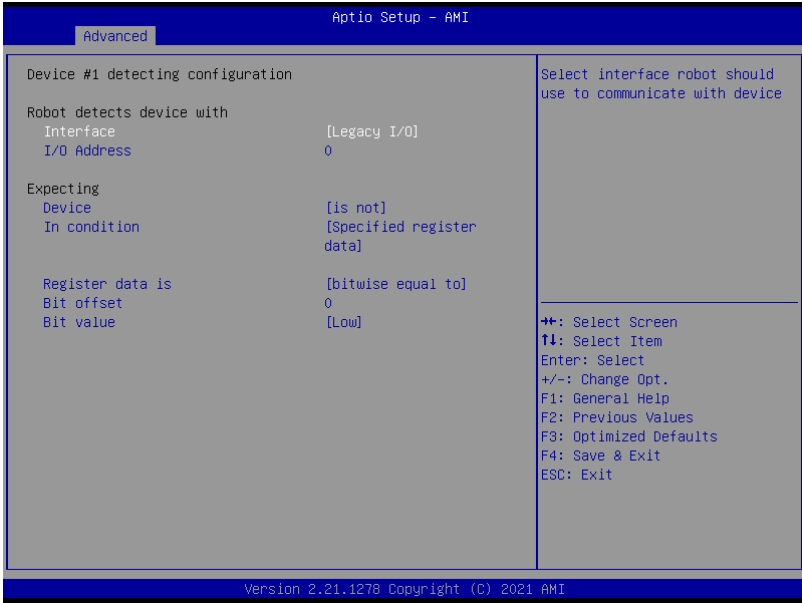
Options Summary		
<b>SMBUS Slave Address</b>	0	Optimal Default, Failsafe Default
Fill slave address to a SMBUS device, in hexadecimal. Range: 0 - FF		
<b>Device</b>	is	Optimal Default, Failsafe Default
	Is not	
Select that robot should or should not do action if condition met.		
<b>In condition</b>	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
<b>Register data is</b>	bitwise equal to	Optimal Default, Failsafe Default
	byte-wise equal to	
	byte-wise lesser than	
	byte-wise larger than	

Table Continues on Next Page...



Options Summary		
Select how robot should compare data read from register, to a value configured below.		
<b>Register offset</b>	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
<b>Bit offset</b>	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
<b>Bit value</b>	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
<b>Byte value</b>	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

## Interface: Legacy I/O



Options Summary		
<b>I/O Address</b>	0	Optimal Default, Failsafe Default
Fill I/O address device is responding to. Range: 0~FFFF		
<b>Device</b>	is	Optimal Default, Failsafe Default
	Is not	
Select that robot should or should not do action if condition met.		
<b>In condition</b>	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
<b>Register data is</b>	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		

### Interface: Super I/O

The screenshot shows the 'Advanced' tab of the 'Aptio Setup - AMI' BIOS. The 'Super I/O' section is expanded, showing the following configuration:

- Device #1 detecting configuration
- Robot detects device with:
  - Interface: [Super I/O]
  - Super I/O LDN: 0
- Expecting:
  - Device: [is not]
  - In condition: [Specified register data]
- Register data is: [bitwise equal to]
- Register offset: 0
- Bit offset: 0
- Bit value: [Low]

Navigation instructions on the right side of the screen:

- +/: Select Screen
- ↑↓: Select Item
- Enter: Select
- +/-: Change Opt.
- F1: General Help
- F2: Previous Values
- F3: Optimized Defaults
- F4: Save & Exit
- ESC: Exit

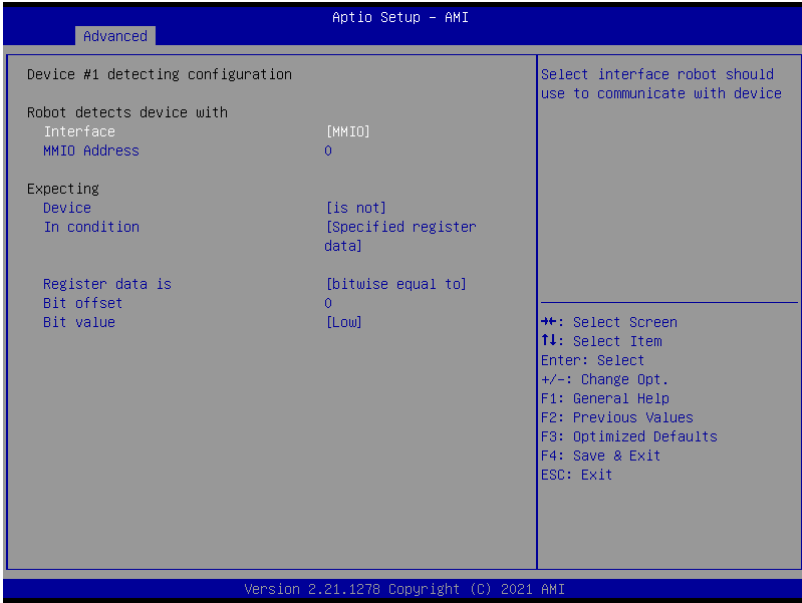
Version 2.21.1278 Copyright (C) 2021 AMI

Options Summary		
Super I/O LDN	0	Optimal Default, Failsafe Default
Fill LDN number to a Super I/O device. Range: 0~FF		
Device	is	Optimal Default, Failsafe Default
	Is not	
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

Table Continue on Next Page...

Options Summary		
<b>Register data is</b>	bitwise equal to	Optimal Default, Failsafe Default
	bitwise equal to	
	bitwise lesser than	
	bitwise larger than	
Select how robot should compare data read from register, to a value configured below.		
<b>Register offset</b>	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
<b>Bit offset</b>	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
<b>Bit value</b>	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
<b>Byte value</b>	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

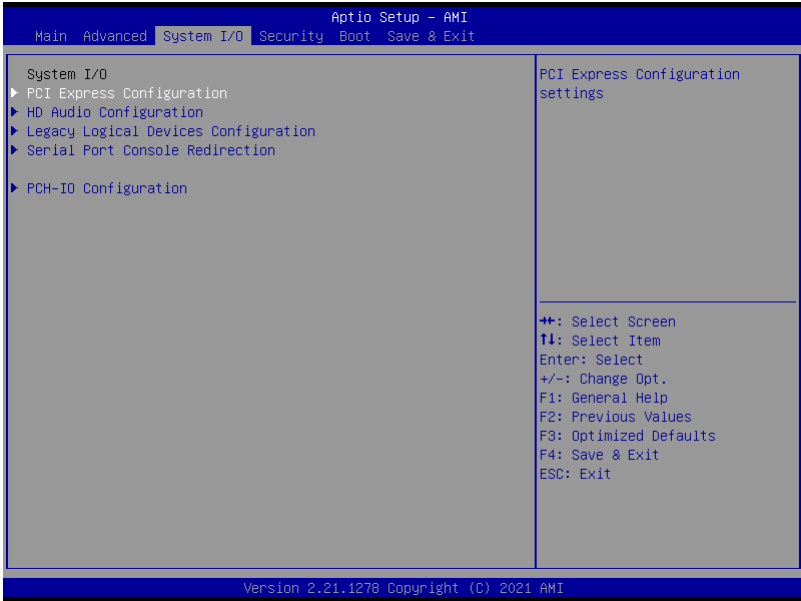
# Interface: MMIO



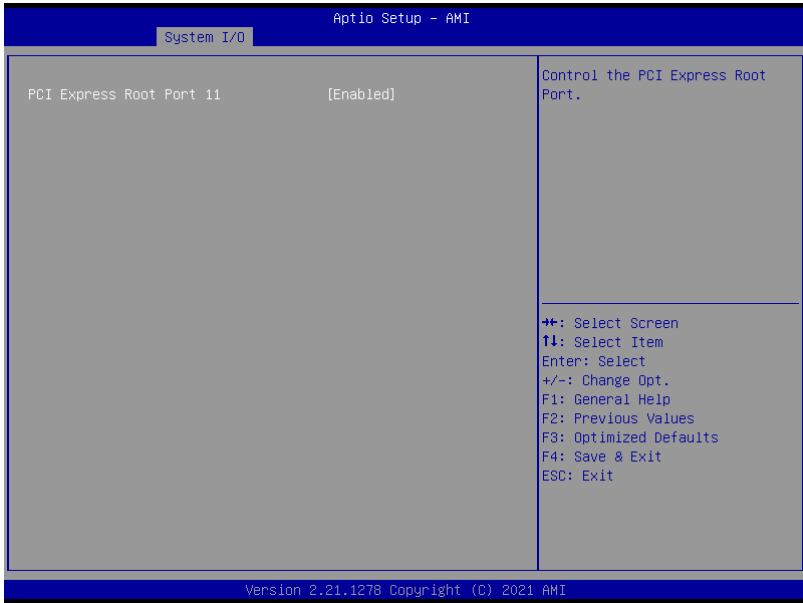
Options Summary		
<b>MMIO Address</b>	0	Optimal Default, Failsafe Default
Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF		
<b>Device</b>	is	Optimal Default, Failsafe Default
	Is not	
Select that robot should or should not do action if condition met.		
<b>In condition</b>	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. Note: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
<b>Register data is</b>	bitwise equal to	Optimal Default, Failsafe Default
	byte-wise equal to	
	byte-wise lesser than	
	byte-wise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
<b>Bit offset</b>	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
<b>Bit value</b>	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
<b>Byte value</b>	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

### 3.5 Setup Submenu: System I/O



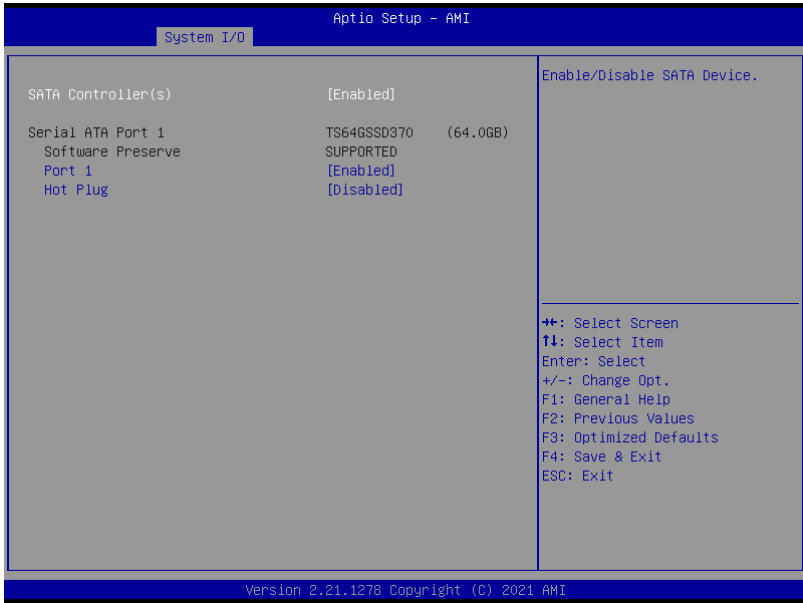
### 3.5.1 PCI Express Configuration



Options Summary		
PCI Express Root Port 11	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control the PCI Express Root Port.		

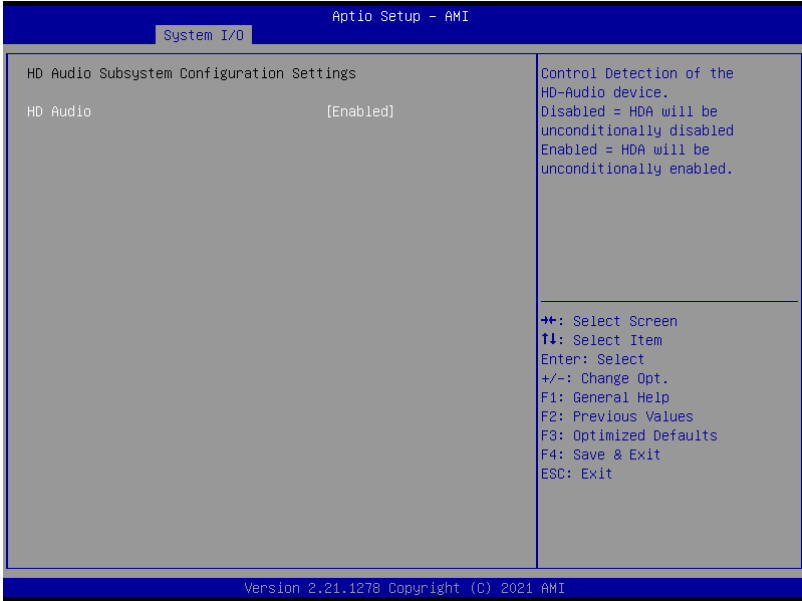


### 3.5.2 Storage Configuration



Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

### 3.5.3 HD Audio Subsystem Configuration Settings



Options Summary		
HD Audio	Disabled	Optimal Default, Failsafe Default
	Enabled	
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled		

### 3.5.4 Legacy Logical Devices Configuration

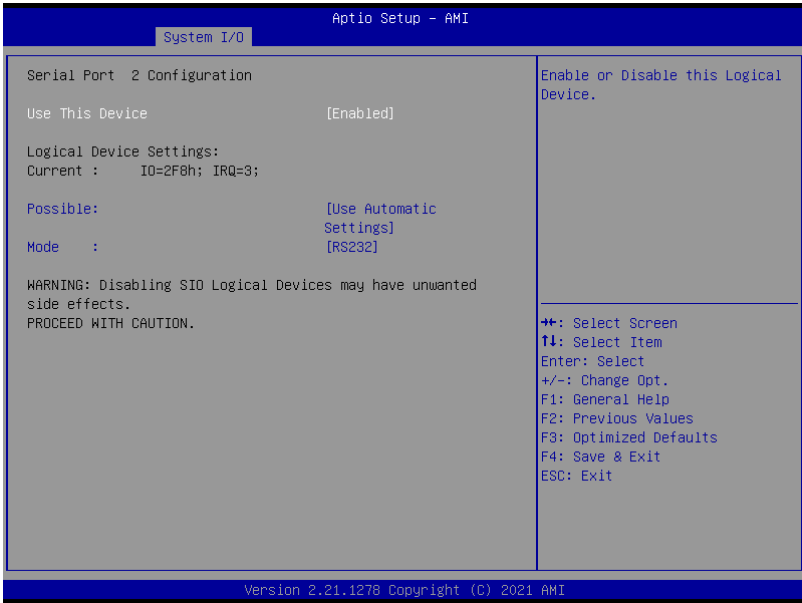


### 3.5.4.1 Serial Port 1 Configuration



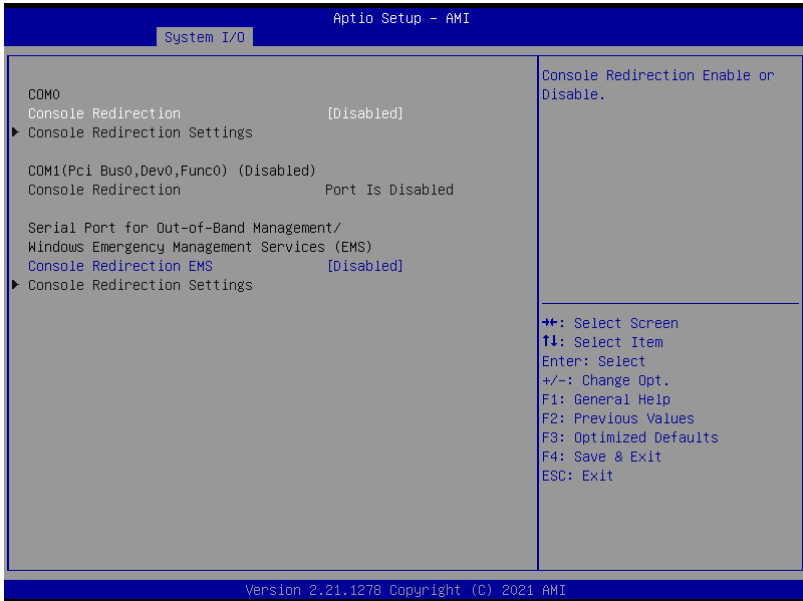
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

### 3.5.4.2 Serial Port 2 Configuration



Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

### 3.5.5 Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

### 3.5.5.1 Console Redirection Settings



Options Summary		
<b>Terminal Type</b>	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
<b>Bits Per second</b>	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

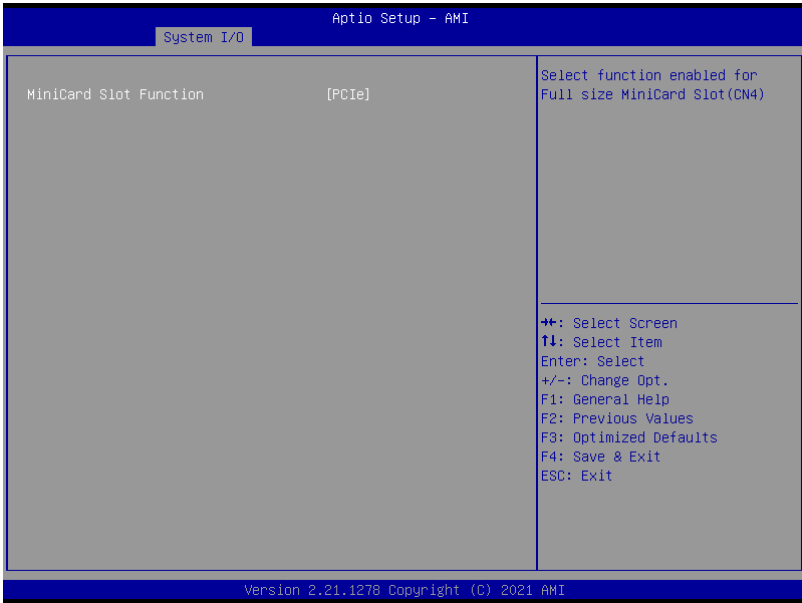
Options Summary		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
<p>A parity bit can be sent with the data bits to detect some transmission errors.            Even: parity bit is 0 if the num of 1's in the data bits is even.            Odd: parity bit is 0 if num of 1's in the data bits is odd.            Mark: parity bit is always 1.            Space: Parity bit is always 0.            Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.</p>		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
<p>Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.</p>		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
<p>Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.</p>		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
<p>Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals</p>		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
<p>With this mode enabled only text will be sent. This is to capture Terminal data.</p>		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
<p>Enables or disables extended terminal resolution</p>		

*Table Continues on Next Page...*



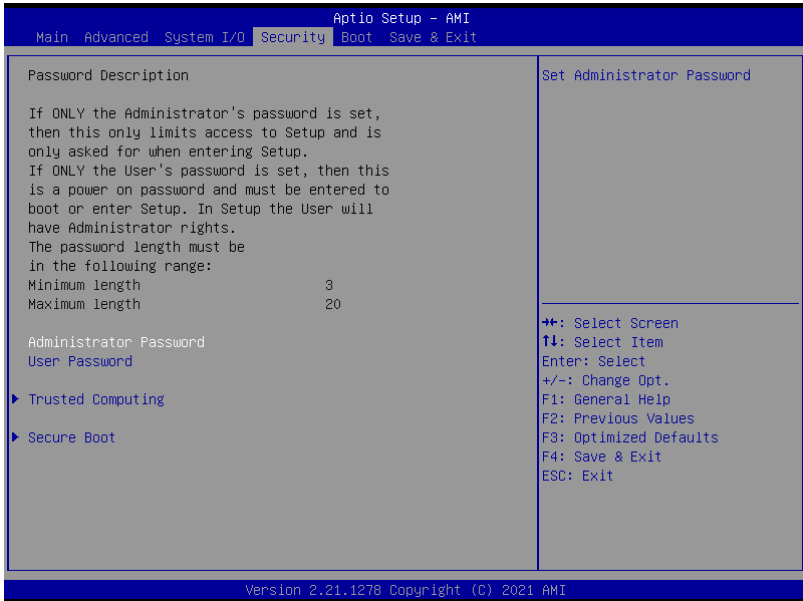
Options Summary		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

### 3.5.6 PCH-IO Configuration



Options Summary		
MiniCard Slot Function	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Full size MiniCard Slot (CN6)		

## 3.6 Setup Submenu: Security



### Change User/Administrator Password

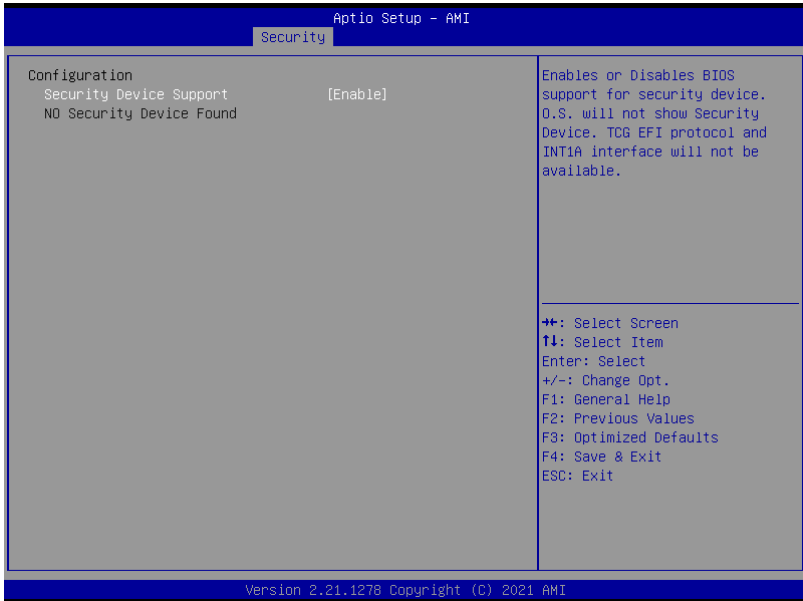
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

### Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

### 3.6.1 Trusted Computing



Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

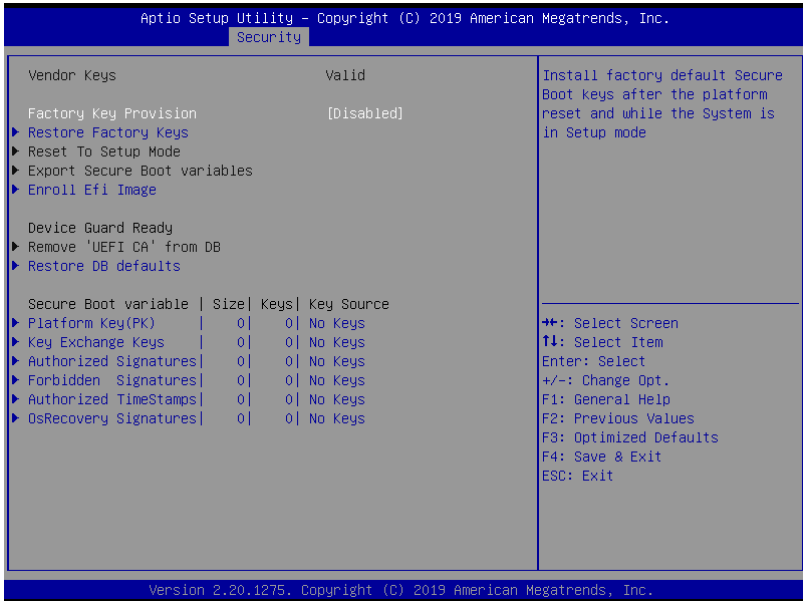
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

### 3.6.2 Secure Boot



Options Summary		
<b>Secure Boot</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
<b>Secure Boot Mode</b>	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
<b>Restore Factory Keys</b>		
Force System to User Mode. Install factory default Secure Boot key databases		
<b>Reset To Setup Mode</b>		
Delete all Secure Boot key databases from NVRAM		

### 3.6.2.1 Key Management

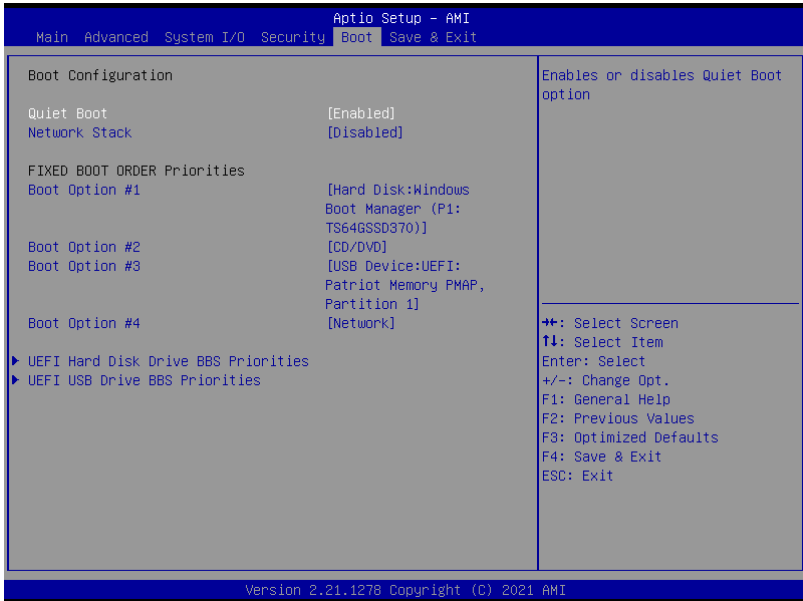


Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults		
Restore DB variable to factory defaults		
Platform Key (PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2. Authenticated UEFI Variable 3. EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

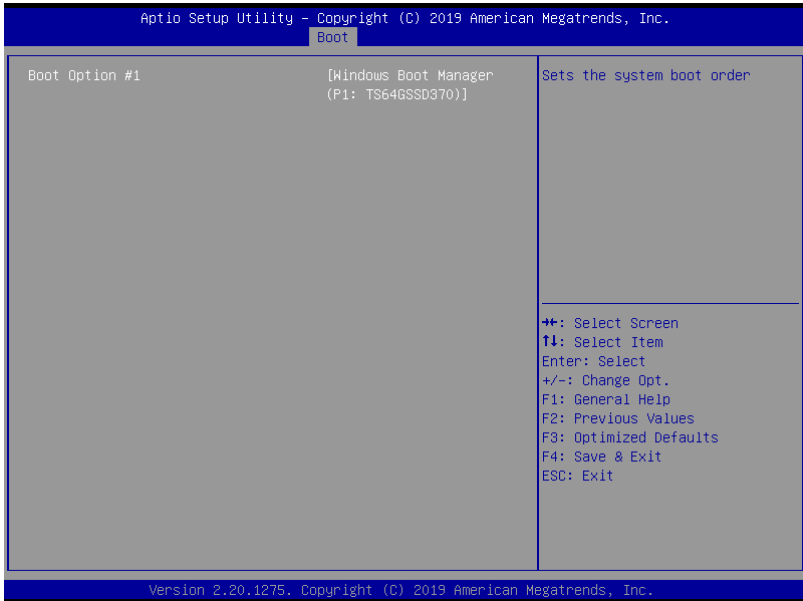


### 3.7 Setup Submenu: Boot

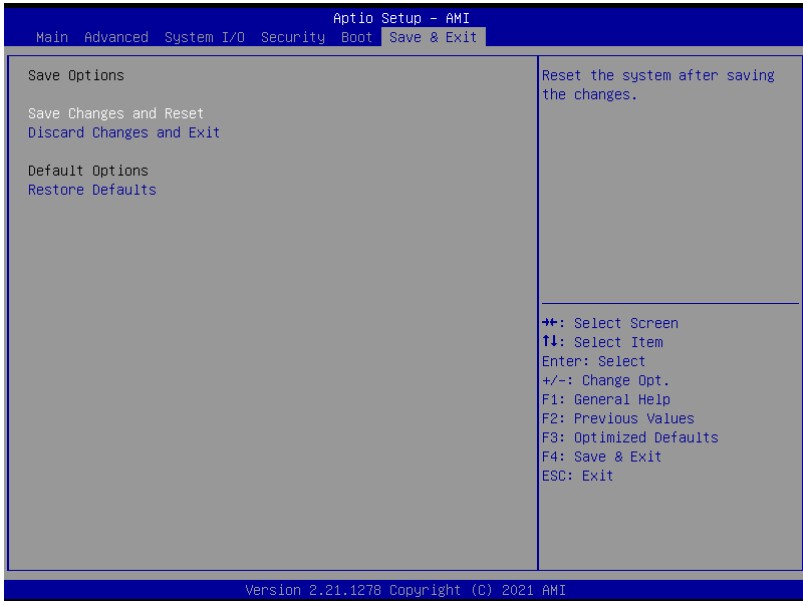


Options Summary		
Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or disable showing boot logo.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

### 3.7.1 BBS Priorities



### 3.8 Setup Submenu: Save & Exit



# Chapter 4

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Drivers Installation

## 4.1 Drivers Download and Installation

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Drivers for the PICO-TGU4 can be downloaded from the product page on the AAeon website by following this link:

<https://www.aaeon.com/en/p/pico-itx-turnkit-pico-tgu4>

Download the driver(s) you need and follow the steps below to install them.

### Step 1 – Install Chipset Driver

1. Open the **Intel Chipset** folder.
2. Run the **SetupChipset.exe** file.
3. Follow the instructions
4. Drivers will be installed automatically

### Step 2 – Install Graphics Driver

1. Open the **Intel Graphics** folder.
2. Run the **igxpın.exe** file.
3. Follow the instructions
4. Driver will be installed automatically

### Step 3 – Install Management Engine Driver

1. Open the **Intel CSME** folder.
2. Run the **SetupME.exe** file.
3. Follow the instructions
4. Driver will be installed automatically

#### Step 4 – Install Serial IO Driver

1. Open the **Serial IO** folder.
2. Run the **SetupSerialIO.exe** file
3. Follow the instructions
4. Driver will be installed automatically

#### Step 5 – Install LAN Driver

1. Open the **LAN** folder.
2. Run the **PROWinx64.exe** file
3. Follow the instructions
4. Driver will be installed automatically

#### Step 6 – Install Audio Driver

1. Open the **Realtek Audio** folder.
2. Run the **Setup.exe** file
3. Follow the instructions
4. Driver will be installed automatically

# Appendix A

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Mating Connectors

## A.1 List of Mating Connectors and Cables

The following table lists mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN16	4-pin Smart FAN	Molex	51021-0400	N/A	N/A
CN17	I2C/SMBUS/ DebugConnector	JST	SHR-12V-S-B	I2C/SMBUS Cable	1703120130
CN19	DC Jack Power Input	HUANG JI	5525C257-3 T00-R 1-7.5	N/A	N/A
CN23	COM*2/USB2.0*4/ DIO 4bit	ACES	50247-040H 0H0-001	Dual COM cable	170X000483
CN26	Front Panel Connector	JST	SHR-10V-S-B	Front Panel Cable	170X000432
CN27	Audio Connector	ACES	50247-012H 0H0-001	Audio Cable	170X000482
CN30	External RTC Connector	Molex	51021-0200	Battery Cable	175011901C



# Appendix B

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I/O Information

## B.1 I/O Address Map

The screenshot displays the I/O Address Map for a system with PCI Express Root Complex and various hardware components. The address ranges are listed in hexadecimal, and the corresponding hardware components are listed to the right.



















































Address Range	Component
[0000000000000000 - 000000000000CF7]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000060 - 0000000000000060]	Standard PS/2 Keyboard
[0000000000000061 - 0000000000000061]	Motherboard resources
[0000000000000063 - 0000000000000063]	Motherboard resources
[0000000000000064 - 0000000000000064]	Standard PS/2 Keyboard
[0000000000000065 - 0000000000000065]	Motherboard resources
[0000000000000067 - 0000000000000067]	Motherboard resources
[0000000000000070 - 0000000000000070]	Motherboard resources
[0000000000000080 - 0000000000000080]	Motherboard resources
[0000000000000092 - 0000000000000092]	Motherboard resources
[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[00000000000000B2 - 00000000000000B3]	Motherboard resources
[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
[00000000000002F8 - 00000000000002FF]	Communications Port (COM2)
[00000000000003F8 - 00000000000003FF]	Communications Port (COM1)
[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[0000000000000680 - 000000000000069F]	Motherboard resources
[0000000000000A00 - 0000000000000A0F]	Motherboard resources
[0000000000000A10 - 0000000000000A1F]	Motherboard resources
[0000000000000A20 - 0000000000000A2F]	Motherboard resources
[000000000000D00 - 000000000000FFFF]	PCI Express Root Complex
[000000000000164E - 000000000000164F]	Motherboard resources
[0000000000001800 - 00000000000018FE]	Motherboard resources
[0000000000002000 - 00000000000020FE]	Motherboard resources
[0000000000003000 - 000000000000303F]	Intel(R) Iris(R) Xe Graphics
[0000000000003060 - 000000000000307F]	Standard SATA AHCI Controller
[0000000000003080 - 0000000000003083]	Standard SATA AHCI Controller
[0000000000003090 - 0000000000003097]	Standard SATA AHCI Controller
[000000000000EFA0 - 000000000000EFBF]	Intel(R) SMBus - A0A3
[000000000000FFF8 - 000000000000FFFF]	Intel(R) Active Management Technology - SOL (COM3)

## B.2 Memory Address Map

- ▼  Large Memory
  -  [0000004000000000 - 0000007FFFFFFF] PCI Express Root Complex
- ▼  Memory
  - >  [0000000000A0000 - 0000000000BFFFFF] PCI Express Root Complex
  - >  [000000004F400000 - 00000000BFFFFFFF] PCI Express Root Complex
  -  [00000000C0000000 - 00000000CFFFFFFF] Motherboard resources
  -  [00000000FD000000 - 00000000FD68FFFF] Motherboard resources
  -  [00000000FD690000 - 00000000FD69FFFF] Intel(R) GPIO Controller - 34C5
  -  [00000000FD6A0000 - 00000000FD6AFFFF] Intel(R) GPIO Controller - 34C5
  -  [00000000FD6B0000 - 00000000FD6CFFFF] Motherboard resources
  -  [00000000FD6D0000 - 00000000FD6DFFFF] Intel(R) GPIO Controller - 34C5
  -  [00000000FD6E0000 - 00000000FD6EFFFF] Intel(R) GPIO Controller - 34C5
  -  [00000000FD6F0000 - 00000000FDFFFFFF] Motherboard resources
  - >  [00000000FE000000 - 00000000FE01FFFF] Motherboard resources
  -  [00000000FE04C000 - 00000000FE04FFFF] Motherboard resources
  -  [00000000FE050000 - 00000000FE0AFFFF] Motherboard resources
  -  [00000000FE0D0000 - 00000000FE0FFFFF] Motherboard resources
  -  [00000000FE200000 - 00000000FE7FFFFF] Motherboard resources
  -  [00000000FED00000 - 00000000FED003FF] High precision event timer
  -  [00000000FED20000 - 00000000FED7FFFF] Motherboard resources
  -  [00000000FED45000 - 00000000FED8FFFF] Motherboard resources
  -  [00000000FED90000 - 00000000FED93FFF] Motherboard resources
  -  [00000000FEDA0000 - 00000000FEDA0FFF] Motherboard resources
  -  [00000000FEDA1000 - 00000000FEDA1FFF] Motherboard resources
  -  [00000000FEDC0000 - 00000000FEDC7FFF] Motherboard resources
  -  [00000000FEE00000 - 00000000FEEFFFFFFF] Motherboard resources
  -  [00000000FF000000 - 00000000FFFFFFFF] Motherboard resources
  -  [0000004000000000 - 0000004000FFFFFF] Intel(R) Iris(Xe) Graphics
  -  [0000006000000000 - 0000006000FFFFFF] Intel(R) Iris(R) Xe Graphics
  -  [0000006001300000 - 000000600130FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
  -  [0000006001310000 - 000000600131FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
  -  [0000006001328000 - 00000060013280FF] Intel(R) SMBus - A0A3
  -  [0000007FFFCFA000 - 0000007FFFCFAFFF] USB Synopsys Controller
  -  [0000007FFFCFB000 - 0000007FFFCFBFFF] Intel(R) Management Engine Interface #1
  -  [0000007FFFCFC000 - 0000007FFFCFCFFF] High Definition Audio Controller
  -  [0000007FFFD00000 - 0000007FFFDFFFFFFF] High Definition Audio Controller
  -  [0000007FFFE00000 - 0000007FFFEFFFFFFF] USB Synopsys Controller

## B.3 IRQ Mapping Chart

▼	Interrupt request (IRQ)	
	(ISA) 0x00000000 (00)	System timer
	(ISA) 0x00000001 (01)	Standard PS/2 Keyboard
	(ISA) 0x00000003 (03)	Communications Port (COM2)
	(ISA) 0x00000004 (04)	Communications Port (COM1)
	(ISA) 0x0000000C (12)	PS/2 Compatible Mouse
	(ISA) 0x0000000E (14)	Intel(R) GPIO Controller - 34C5
	(ISA) 0x00000037 (55)	Microsoft ACPI-Compliant System
	(ISA) 0x00000038 (56)	Microsoft ACPI-Compliant System
	(ISA) 0x00000039 (57)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003A (58)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003B (59)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003C (60)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003D (61)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003E (62)	Microsoft ACPI-Compliant System
	(ISA) 0x0000003F (63)	Microsoft ACPI-Compliant System
	(ISA) 0x00000040 (64)	Microsoft ACPI-Compliant System
	(ISA) 0x00000041 (65)	Microsoft ACPI-Compliant System
	(ISA) 0x00000042 (66)	Microsoft ACPI-Compliant System
	(ISA) 0x00000043 (67)	Microsoft ACPI-Compliant System
	(ISA) 0x00000044 (68)	Microsoft ACPI-Compliant System
	(ISA) 0x00000045 (69)	Microsoft ACPI-Compliant System
	(ISA) 0x00000046 (70)	Microsoft ACPI-Compliant System
	(ISA) 0x00000047 (71)	Microsoft ACPI-Compliant System
	(ISA) 0x00000048 (72)	Microsoft ACPI-Compliant System
	(ISA) 0x00000049 (73)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004A (74)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004B (75)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004C (76)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004D (77)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004E (78)	Microsoft ACPI-Compliant System
	(ISA) 0x0000004F (79)	Microsoft ACPI-Compliant System
	(ISA) 0x00000050 (80)	Microsoft ACPI-Compliant System
	(ISA) 0x00000051 (81)	Microsoft ACPI-Compliant System
	(ISA) 0x00000052 (82)	Microsoft ACPI-Compliant System
	(ISA) 0x00000053 (83)	Microsoft ACPI-Compliant System
	(ISA) 0x00000054 (84)	Microsoft ACPI-Compliant System
	(ISA) 0x00000055 (85)	Microsoft ACPI-Compliant System
	(ISA) 0x00000056 (86)	Microsoft ACPI-Compliant System
	(ISA) 0x00000057 (87)	Microsoft ACPI-Compliant System
	(ISA) 0x00000058 (88)	Microsoft ACPI-Compliant System
	(ISA) 0x00000059 (89)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005A (90)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005B (91)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005C (92)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005D (93)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005E (94)	Microsoft ACPI-Compliant System
	(ISA) 0x0000005F (95)	Microsoft ACPI-Compliant System
	(ISA) 0x00000060 (96)	Microsoft ACPI-Compliant System
	(ISA) 0x00000061 (97)	Microsoft ACPI-Compliant System

	(ISA) 0x000001DE (478)	Microsoft ACPI-Compliant System
	(ISA) 0x000001DF (479)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E0 (480)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E1 (481)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E2 (482)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E3 (483)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E4 (484)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E5 (485)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E6 (486)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E7 (487)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E8 (488)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E9 (489)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EA (490)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EB (491)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EC (492)	Microsoft ACPI-Compliant System
	(ISA) 0x000001ED (493)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EE (494)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EF (495)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F0 (496)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F1 (497)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F2 (498)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F3 (499)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F4 (500)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F5 (501)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F6 (502)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F7 (503)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F8 (504)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F9 (505)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FA (506)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FB (507)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FC (508)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FD (509)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FE (510)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FF (511)	Microsoft ACPI-Compliant System
	(PCI) 0x00000010 (16)	High Definition Audio Controller
	(PCI) 0x00000011 (17)	USB Synopsys Controller
	(PCI) 0x00000013 (19)	Intel(R) Active Management Technology - SOL (COM3)
	(PCI) 0xFFFFFFF2 (-14)	Intel(R) Ethernet Controller I225-V
	(PCI) 0xFFFFFFF3 (-13)	Intel(R) Ethernet Controller I225-V
	(PCI) 0xFFFFFFF4 (-12)	Intel(R) Ethernet Controller I225-V
	(PCI) 0xFFFFFFF5 (-11)	Intel(R) Ethernet Controller I225-V
	(PCI) 0xFFFFFFF6 (-10)	Intel(R) Ethernet Controller I225-V
	(PCI) 0xFFFFFFF7 (-9)	Intel(R) Ethernet Connection (13) I219-LM
	(PCI) 0xFFFFFFF8 (-8)	Intel(R) Management Engine Interface #1
	(PCI) 0xFFFFFFF9 (-7)	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
	(PCI) 0xFFFFFFFA (-6)	Intel(R) Iris(R) Xe Graphics
	(PCI) 0xFFFFFFF8 (-5)	Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
	(PCI) 0xFFFFFFF4 (-4)	Standard SATA AHCI Controller
	(PCI) 0xFFFFFFF3 (-3)	Intel(R) PCI Express Root Port #1 - A0B8
	(PCI) 0xFFFFFFF2 (-2)	Intel(R) PCI Express Root Port #8 - A0B8

# Appendix C

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## Watchdog Timer Programming

## C.1 Introduction to Watchdog Timer

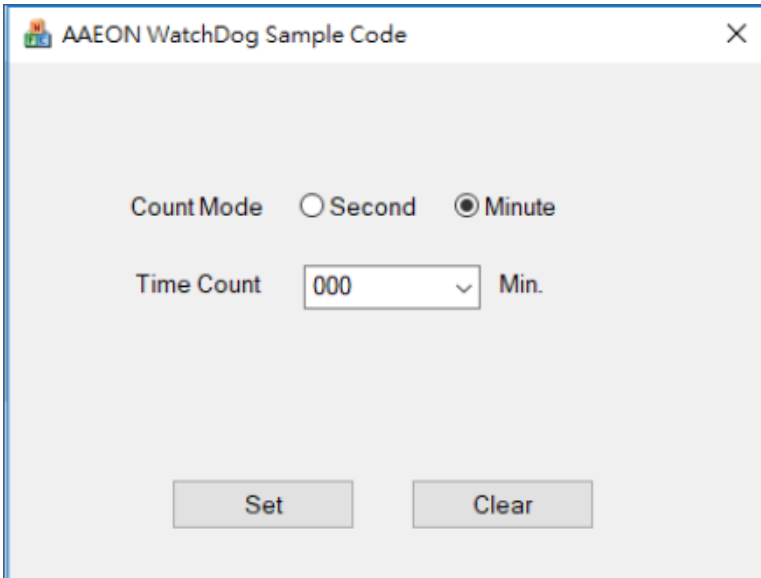
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This section details how to set up and program the Watchdog Timer for your AAEON system or board. The watchdog timer is used to automatically detect malfunctions and recover the system. During normal operation, the system will regularly send a signal to reset the watchdog timer. If the system does not reset the watchdog timer, it will timeout and force the system into recovery and/or reboot.

The following sections refer to additional software used for programming your board, such as the AAEON Framework, AAEON SDK and AAEON Windows EAPI. If you need assistance with utilizing these tools, programming your Watchdog Timer, or would like additional documentation on these resources, contact your AAEON representative or visit our support page at <https://www.aaeon.com/en/support/>

## C.2 Programing the Watchdog Timer with AAEON SDK

If you have installed the AAEON Framework, you can program the Watchdog Timer using the AAEON SDK. Simply locate where the SDK is installed, and double click the icon. The following dialog box will appear:



**Count Mode:** Set Watchdog Timer to count in minutes or seconds.

**Time Count:** The length of time (in minutes or seconds) before the Watchdog Timer will initiate a system recovery/ reboot.

**Set:** After selecting Count Mode and Time Count, this will save your changes and enable the Watchdog Timer function.

**Clear:** This will reset settings and disable the Watchdog Timer function.



### C.3 Programing Watchdog Timer with AAEON Windows EAPI

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AAEON Framework (KMDF Driver) must be installed before calling these functions.

**EapiLibInitialize()** should be the first to call before calling other EAPI functions.

**EapiLibUninitialize()** should be called to release resources before program exit.

When building C/C++ apps, Lib (Library, aaeonEAPI.lib) is needed.

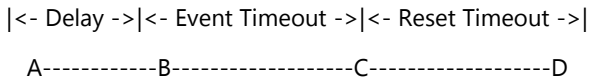
aaeonEAPI.lib is needed for C/C++ based app, make sure the lib files and executable files are in the same folder.

The following shows how to build and run codes:

There are two scenarios to invoke Watchdog Timer functions:

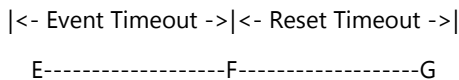
#### 1. Use **EApiWDogStart**

After EApiWDogStart



#### 2. Use **EApiWDogTrigger**

After EApiWDogTrigger



**Stage A:** Watchdog is started.

**Stage B:** Initial Delay Period.

**Stage C/F:** Event is triggered, NMI, IRQ, or PIN is Triggered. This allows for possible Software Recovery.

**Stage D/G:** System is reset.

**Stage E:** Watchdog is Triggered.

**EApiWDogStop** must be called before Stage C/F to prevent event from being generated.

EApiWDogStop must be called before Stage D/G to prevent system from being reset.

### C.3.1 Watchdog Timer Functions

#### C.3.1.1 EapiWDogGetCap()

Command Line:

```
EApiWDogGetCap(...)
    _OUTOPT uint32_t *pMaxDelay,
    _OUTOPT uint32_t *pMaxEventTimeout,
    _OUTOPT uint32_t *pMaxResetTimeout
)
```

Use this command to get maximum Supported Delay / Supported Event Timeout / Supported Reset Timeout of the watchdog timer.

Parameters	Function Parameters
*pMaxDelay	Maximum Supported Delay in milliseconds
*pMaxEvenTimeout	Maximum Supported Event Timeout in milliseconds; 0 = Unsupported
*pMaxResetTimeout	Maximum Supported Reset Timeout in milliseconds
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
pMaxDelay == NULL && pMaxResetTimeout == NULL && pMaxEventTimeout == NULL	EAPI_STATUS_INVALID_PARAMETER
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.2 EapiWDogStart()

Command Line:

```
EApiWDogStart(  
    _IN uint32_t Delay,  
    _IN uint32_t Minute,  
    _IN uint32_t EventTimeout,  
    _IN uint32_t ResetTimeout  
)
```

Use this command to start the Watchdog Timer and set the timeout values.

To stop the Watchdog Timer, issue the command **EApiWDogStop**. After issuing EApiWDogStop, the command EApiWDogStart must be called again with new values to restart.

If the hardware implementation of the watchdog timer does not allow the user to select the exact time they want, the EAPI will select the next longer time setting available.

Parameters	Function Parameters
Delay	Delay in milliseconds
Minute	Control minutes or seconds
EventTimeout	Event Timeout in milliseconds
ResetTimeout	Reset Timeout in milliseconds
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
(Delay > gMaxDelay) (EventTimeout > gMaxEventTimeout) (ResetTimeout > gMaxResetTimeout)	EAPI_STATUS_INVALID_PARAMETER
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.3 EapiWDogTrigger()

Command Line:

```
EapiWDogTrigger()
```

Use this command to trigger the Watchdog Timer.

Parameters	Function Parameters
None	
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
Watchdog Not Started	EAPI_STATUS_ERROR
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.4 EapiWDogStop()

Command Line:

```
EapiWDogStop()
```

Use this command to close the Watchdog Instance. This will disable the Watchdog Timer and clear previous settings.

Parameters	Function Parameters
None	
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.5 EapiWDogReloadTimer()

Command Line:

```
EapiWDogReloadTimer()
```

Use this command to reload the Timeout count

Parameters	Function Parameters
None	
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.6 EapiWDogGetStatus()

Command Line:

```
EapiWDogGetStatus(
    __OUTOPT uint32_t *pwdtMinute,
    __OUTOPT uint32_t *pwdtCountTime,
    __OUTOPT uint32_t *pwdtReloadTime
)
```

Use this command to get the Watchdog Timer mode, time count value and reload timer.

Parameters	Function Parameters
*pwtMinute	Get the mode of minute or second
*pwtCountTime	Get WDT time count
*pwtReloadTime	Get WDT ReloadTime
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS

### C.3.1.7 EapiWDogSetStatus()

Command Line:

```
EApiWDogSetStatus(  
    __IN uint32_t wdtMinute,  
    __IN uint32_t wdtCountTime,  
    __IN uint32_t wdtReloadTime  
)
```

Use this command to set Watchdog Timer mode, time count value and reload timer.

Parameters	Function Parameters
wdtMinute	Set the mode of minute or second
wdtCountTime	Set WDT time count
wdtReloadTime	Set WDT ReloadTime
Condition	Return Values
Library Uninitialized	EAPI_STATUS_NOT_INITIALIZED
Common Error	Common Error Code
Others	EAPI_STATUS_SUCCESS