PICO-HD01

AMD G-series Dual Core T40E/
Single Core T40R Processor
Gigabit Ethernet
5 USB 2.0, 2 COM
4-bit Digital I/O
1 Mini Card/ mSATA(Half-size)
1 SATA 3.0Gb/s

PICO-HD01 Manual Rev.A 3rd Ed.
March 4, 2015

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Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 Heatsink
- 1 SATA Power Cable
- 1 Power Cable
- 1 SATA Cable
- 1 DVD-ROM for Manual (in PDF Format) and Drivers
- 1 PICO-HD01

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

Contents

Appendix B I/O Information

Appendix C Mating Connector

Appendix D AHCI Setting

Appendix E Electrical Specifications for I/O Ports

Chapter

1

General Information

1.1 Introduction

The PICO-HD01 is the embedded board with PICO-ITX form factor AAEON developed. It supports AMD G-series T40R/ T40E processor up to 1.0 GHz. Moreover, it equips AMD A50M chipset offers a high performance computing platform with low power consumption. This new product supports DDR3 SODIMM at speeds of 1066 MHz, up to 4 GB.

One SATA 3.0Gb/s and one mSATA interfaces provide ample storages. With one Gigabit Ethernet, two COM ports, and five USB2.0, the PICO-HD01 meets the requirements of today's demanding applications.

Display requirements are met with an abundance of interfaces such as VGA, HDMI, and LVDS. In addition, the PICO-HD01 supports 18-bit Single Channel LVDS with PWM function.

With all of its integrated features, the PICO-HD01 strikes a balance of performance and price. This versatile product targets Industrial Automation, Entertainment, Networking, KIOSK/POS, Transportation, Banking, Healthcare and Digital Signage applications that require high performance and high reliability.

1.2 Features

- Onboard AMD G-Series T40R/T40E Single/Dua Processor
- AMD G-Series APU +A50M
- 204-pin SODIMM DDR3 1066MHz up to 4GB
- One Reatek RTL-8111E for 10/1000/1000Base-TX
- CRT, 18-bit Single Channel LVDS, HDMI
- HD Audio for Line-in/out & MIC
- SATA 3.0Gb/s x 1, mSATA (Half-Size) Slot x 1 Co-lay with Mini Card
- USB 2.0 x 5, COM x 2, 4-bit Digital I/O
- Expansion : Mini Card x 1
- DC 12V Operating
- Supports Mini HDMI Connector on Rear I/O

1.3 Specifications

System

● **From Factor**	PICO-ITX
● **Processor**	AMD G-series T40E/ T40R processor up to 1.0 GHz
● **System Memory**	204-pin SODIMM DDR3 1066 MHz, up to 4 GB
● **Chipset**	AMD G-series + A50M
● **I/O Chipset**	Fintek F81801U-I
● **Ethernet**	Realtek RTL-8111E, 10/100/1000Base-TX, RJ-45 x 1
● **BIOS**	AMI BIOS-32 Mb ROM
● **Wake On LAN**	Yes
● **Watchdog Timer**	Programmable 255 levels system reset
● **H/W Status Monitoring**	Vcore, +1.5V_DDR
● **Expansion Interface**	mSATA/ Mini Card (Half-size) x 1
● **Battery**	Lithium Battery
● **Power Requirement**	DC 12V, AT/ATX (Default)
● **Board Size**	3.94" x 2.76" (100mm x 72mm)
● **Gross Weight**	1.7 lb (0.77 Kg)
● **Operating Temperature**	32°F~140°F (0°C~60°C)
● **Storage Temperature**	-40°F~176°F (-40°C~80°C)
● **Operating Humidity**	0% ~ 90% relative humidity, non-condensing

Display: Supports CRT/LCD, HDMI/DVI/LCD simultaneous / dual view displays

- **Chipset** — AMD G-series Processor integrated
- **Resolution** — Up to 1366 x 768 (18-bit) @ 60 Hz for LVDS;

  Up to 1920 x 1200 @ 60 Hz for CRT and HDMI
- **LCD Interface** — 18-bit single channel LVDS with PWM function

I/O: Fintek F81801U-I

- **Storage** — SATA 3.0Gb/s x 1 , mSATA x 1 co-lay with Mini Card
- **Serial Port** — RS-232 x 1

  RS-232/422/485 x 1
- **USB** — USB2.0 x 5
- **Digital I/O** — 4-bit Programmable (2-in/ 2-out)
- **Audio** — Buzzer x 1, HD Audio Codec (Realtek ALC662) for Line-in/out & MIC x 1

Chapter

2

Quick Installation Guide

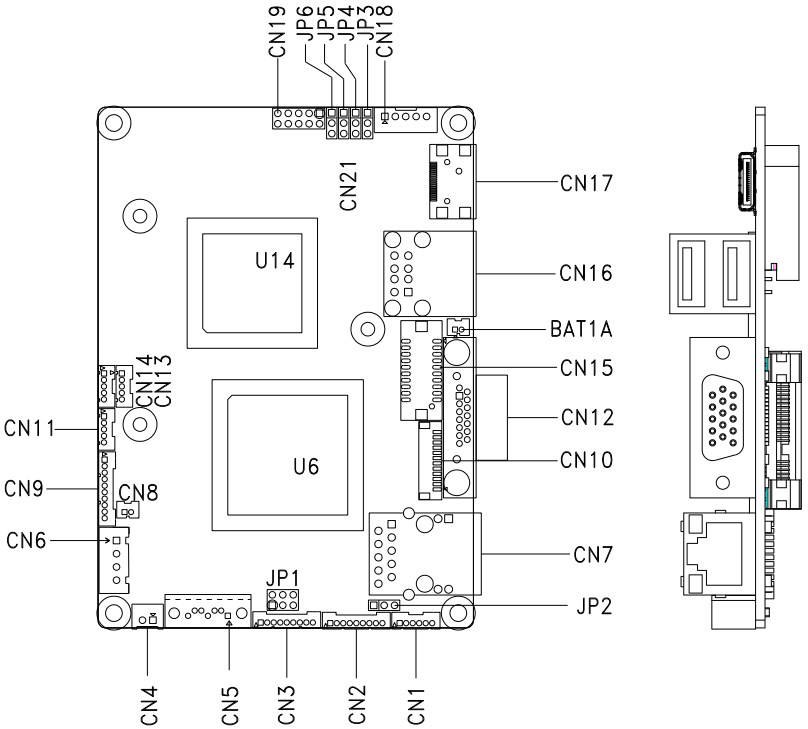
2.1 Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

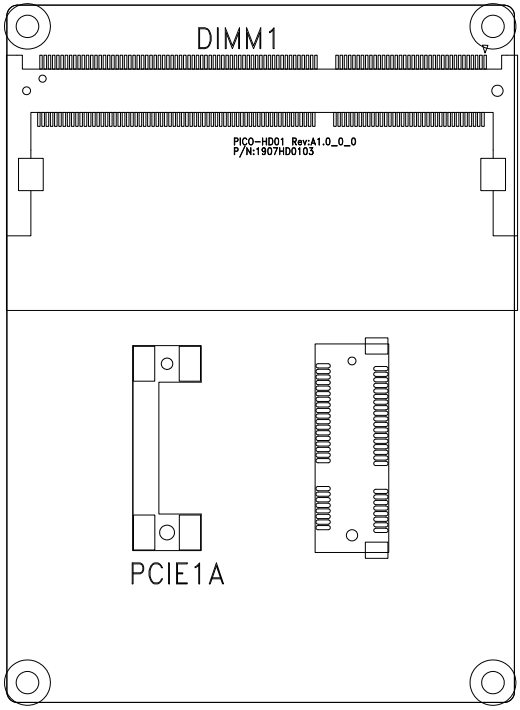
Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Location of Connectors and Jumpers

Component Side

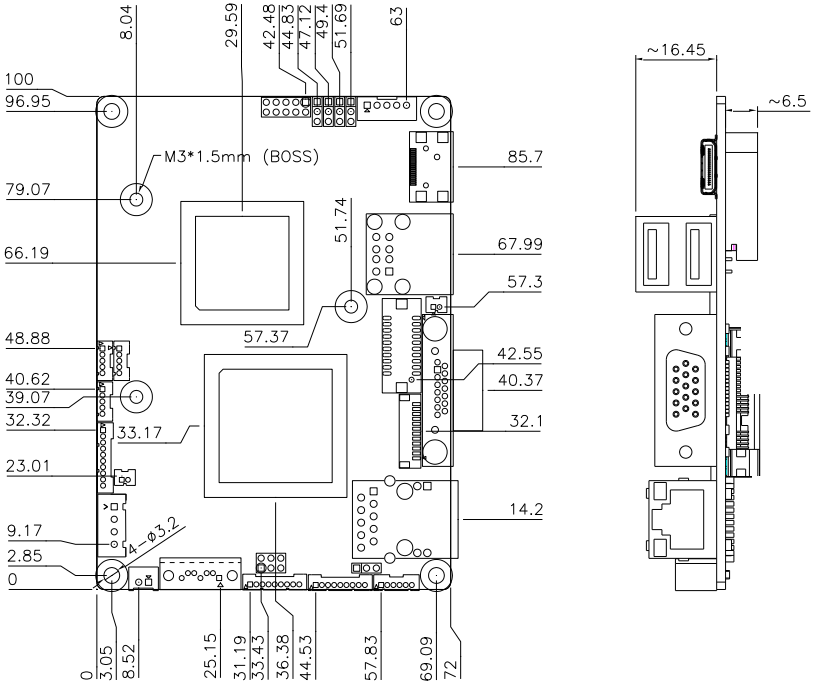


Solder Side

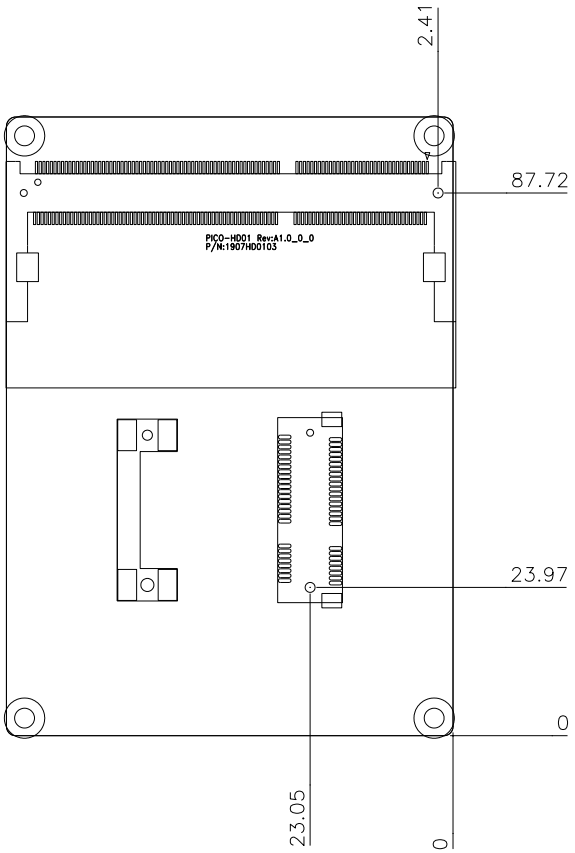


2.3 Mechanical Drawing

Component Side



Solder Side



2.4 List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Label	Function
JP1	COM2 RI/+5/+12V Selection
JP2	Clear CMOS
JP3	LVDS Inverter/ Backlight Voltage Selection
JP4	LVDS Operating Voltage Selection
JP5	LVDS Backlight Lightness Control Mode Selection
JP6	AT/ATX Power Supply Mode Selection

2.5 List of Connectors

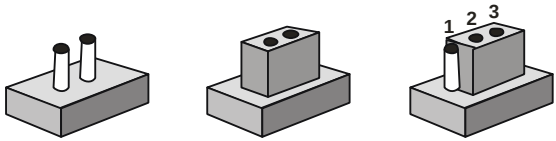
The board has a number of connectors that allow you to configure your system to suit your application. The table below shows the function of each board's connectors:

Label	Function
CN1	Digital I/O Connector
CN2	COM Port #1
CN3	COM Port #2
CN4	+5V Output For SATA HDD
CN5	SATA Port
CN6	External 12V Input
CN7	RJ-45 Ethernet
CN8	Buzzer
CN9	Audio Line In/Out and MIC Connector
CN10	LPC Expansion I/F
CN11	USB Port #5
CN12	Analog CRT Display Connector
CN13	USB Port #3
CN14	USB Port #4
CN15	18-bit LVDS Output
CN16	USB Port 1 & 2
CN17	HDMI TYPE C
CN18	LVDS Inverter/ Backlight Connector
CN19	Front Panel

2.6 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



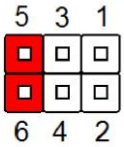
Open Closed Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

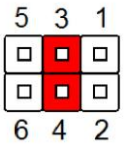
If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

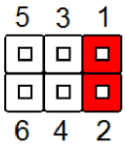
2.7 COM2 RI/+5/+12V Selection (JP1)



+5V



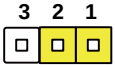
Ring (Default)



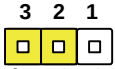
+12V

JP1	Function
1-2	+12V
3-4	Ring (Default)
5-6	+5V

2.8 Clear CMOS Selection (JP2)



Normal (Default)



Clear CMOS

JP2	Function
1-2	Normal (Default)
2-3	Clear CMOS

2.9 LVDS Backlight Inverter VCC Selection (JP3)

+12V

+5V (Default)

JP3	Function
1-2	+12V
2-3	+5V (Default)

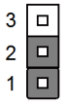
2.10 LVDS Operating Voltage Selection (JP4)

+5V

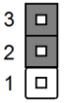
+3.3V (Default)

JP4	Function
1-2	+5V
2-3	+3.3V (Default)

2.11 LVDS Backlight Lightness Control Mode Selection (JP5)



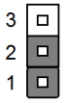
VR Mode



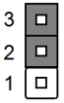
PWM Mode (Default)

JP5	Function
1-2	VR Mode
2-3	PWM Mode (Default)

2.12 AT/ATX Power Supply Mode Selection (JP6)



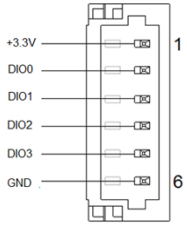
AT Mode



ATX Mode (Default)

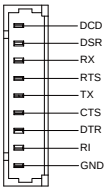
JP6	Function
1-2	AT Mode
2-3	ATX Mod (Default)

2.13 Digital IO Port Connector (CN1)



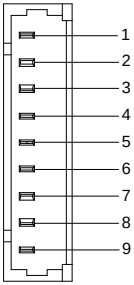
Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	+3.3V
2	DIO0	I/O	+3.3V
3	DIO1	I/O	+3.3V
4	DIO2	I/O	+3.3V
5	DIO3	I/O	+3.3V
6	GND	GND	GND

2.14 COM Port 1 Connector (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	DCDA	IN	
2	DSRA	IN	
3	RXA	IN	
4	RTSA	OUT	±9V
5	TXA	OUT	±9V
6	CTSA	IN	
7	DTRA	OUT	±9V
8	RIA	IN	
9	GND	GND	

2.15 COM Port 2 Connector (CN3)



RS-232

Pin	Pin Name	Signal Type	Signal Level
1	DCDB	IN	
2	DSRB	IN	
3	RXB	IN	

4	RTSB	OUT	±9V
5	TXB	OUT	±9V
6	CTSB	IN	
7	DTRB	OUT	±9V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

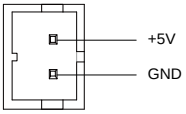
RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		

6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

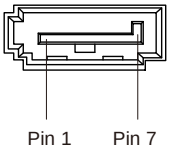
Note 1: COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.
Note 2: Pin 8 function can be set by JP1.

2.16 +5V Output For SATA HDD Connector (CN4)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	GND

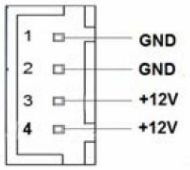
2.17 SATA Port Connector (CN5)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	

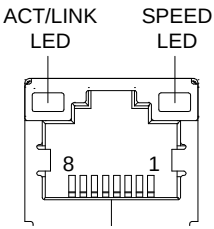
5	SATA_RX-	DIFF
6	SATA_RX+	DIFF
7	GND	GND

2.18 External +12V Input Connector (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	GND	GND	GND
3	+12V	PWR	+12V
4	+12V	PWR	+12V

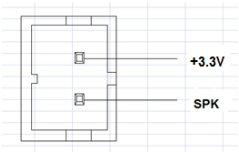
2.19 Realtek LAN (RJ-45) Port Connector (CN7)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	

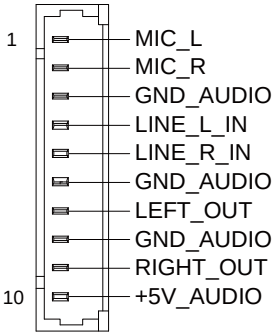
3	MDI1+	DIFF
4	MDI2+	DIFF
5	MDI2-	DIFF
6	MDI1-	DIFF
7	MDI3+	DIFF
8	MDI3-	DIFF

2.20 Buzzer Connector (CN8)



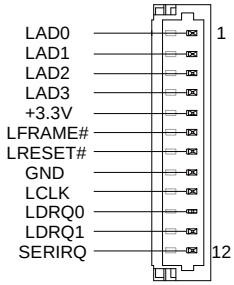
Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	+3.3V
2	SPK	OUT	

2.21 Audio Line In/Out and MIC Connector (CN9)



Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

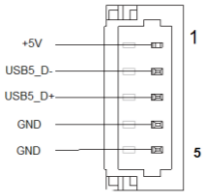
2.22 LPC Port Connector (CN10)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V

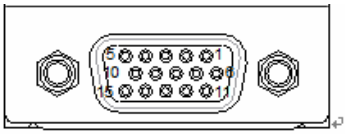
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.23 USB 2.0 Ports 5 Connector (CN11)



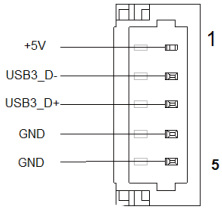
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB4_D-	DIFF	
3	USB4_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.24 VGA Port Connector (CN12)



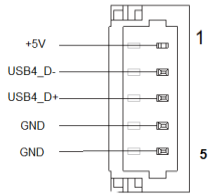
Pin	Pin Name	Signal Type	Signal Level
1	RED	OUT	
2	GREEN	OUT	
3	BLUE	OUT	
4	NC		
5	GND	GND	
6	RED_GND_RTN	GND	
7	GREEN_GND_RTN	GND	
8	BLUE_GND_RTN	GND	
9	+5V	PWR	+5V
10	CRT_PLUG#	GND	+5V
11	NC		
12	DDC_DATA	I/O	+5V
13	HSYNC	OUT	
14	VSYNC	OUT	
15	DDC_CLK	I/O	+5V

2.25 USB 2.0 Port 3 Connector (CN13)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB3_D-	DIFF	
3	USB3_D+	DIFF	
4	GND	GND	
5	GND	GND	

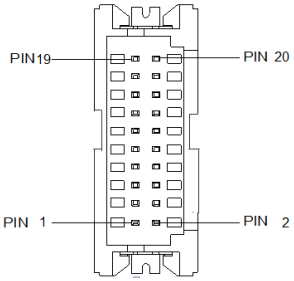
2.26 USB 2.0 Port 4 Connector (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB4_D-	DIFF	
3	USB4_D+	DIFF	

4	GND	GND
5	GND	GND

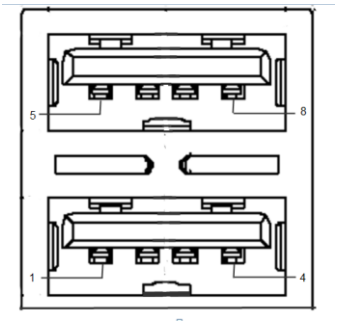
2.27 18-bits LVDS Output Connector (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR		+3.3V/+5V
4	LCD_PWR	PWR	+3.3V/+5V
5	LVDS_A_CLK-	DIFF	
6	LVDS_DA2+	DIFF	
7	LVDS_A_CLK+	DIFF	
8	LVDS_DA2-	DIFF	
9	LCD_PWR	DIFF	+3.3V/+5V
10	GND	GND	
11	LVDS_DA0+	DIFF	
12	LVDS_DA3+	DIFF	
13	LVDS_DA0-	DIFF	

14	LVDS_DA3-	DIFF	
15	GND	GND	
16	GND	GND	
17	LVDS_DA1+	DIFF	
18	DDC_DATA	I/O	+3.3V
19	LVDS_DA1-	DIFF	
20	DDC_CLK	I/O	+3.3V

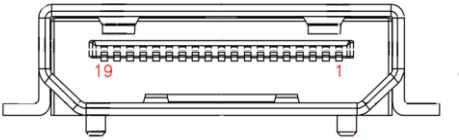
2.28 USB Port 1 and Port 2 Connector (CN16)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB1_D-	DIFF	
3	USB1_D+	DIFF	
4	GND	GND	
5	+5VSB	PWR	+5V
6	USB2_D-	DIFF	
7	USB2_D+	DIFF	

8	GND	GND	

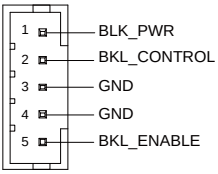
2.29 HDMI Type C Connector (CN17)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	HDMI_TX2+	DIFF	
3	HDMI_TX2-	DIFF	
4	GND	GND	
5	HDMI_TX1+	DIFF	
6	HDMI_TX1-	DIFF	
7	GND	GND	
8	HDMI_TX0+	DIFF	
9	HDMI_TX0-	DIFF	
10	GND	GND	
11	HDMI_CLK+	DIFF	
12	HDMI_CLK-	DIFF	
13	GND	GND	
14	NC	NC	
15	HDMI_DDC_CLK	I/O	+5V
16	HDMI_DDC_DATA	I/O	+5V

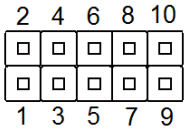
17	NC	NC	
18	DPD_HPD	IN	
19	DPD_PWR	PWR	+5V

2.30 LVDS Port Inverter / Backlight Connector (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+5V

2.31 Front Panel Connector (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	PWR_BTN-		
2	PWR_BTN+		

3	HDD_LED-		
4	HDD_LED+		
5	SPEAKER-		
6	SPEAKER+		
7	PWR_LED-		
8	PWR_LED+		
9	H/W RESET-		
10	H/W RESET+		

2.32 DDR3 SODIMM Slot (DIMM1)

Standard Specification

2.33 Mini Card Slot (PCIE1)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	

11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	

PICO-ITX Board		PICO-HD01	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

Below Table for China RoHS Requirements

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 **SJ/T 11363-2006** 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 **SJ/T 11363-2006** 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

Chapter

3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-HD01 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <F2> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

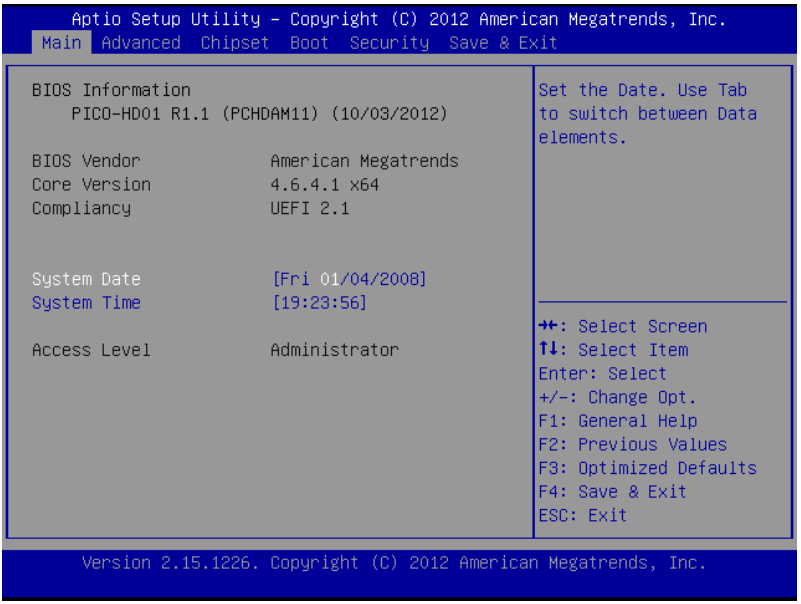
Set setup administrator password.

Save & Exit

Exit system setup after saving the changes.

Setup Menu

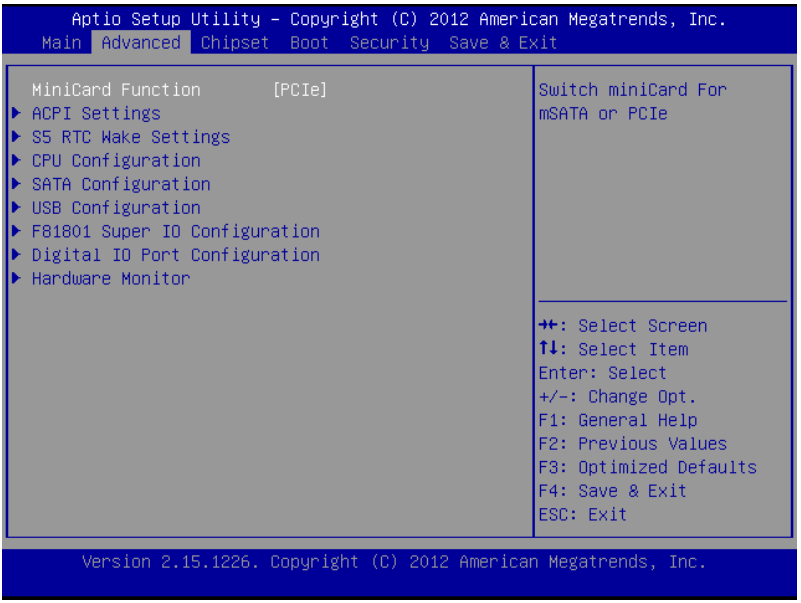
Setup submenu: Main



Options summary: (***default setting***)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

Setup submenu: Advanced

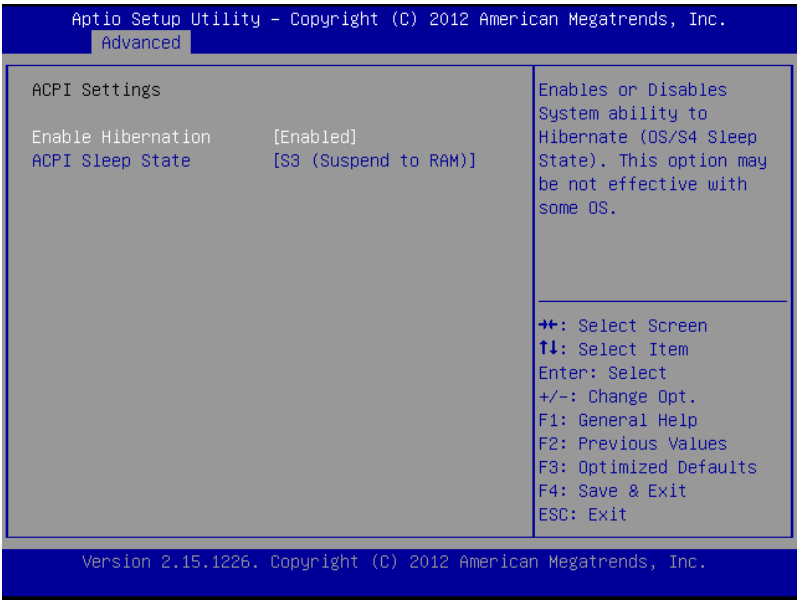


Options summary: (***default setting***)

ACPI Settings		
System ACPI Parameters		
S5 RTC Wake Settings		
Support S5 RTC Wake Function		
CPU Configuration		
CPU Configuration Parameters		
SATA Configuration		
SATA Device Options Settings		
USB Configuration		

USB Configuration Parameters		
F81801 Super IO Configuration		
F81801 Super IO Configuration Parameters		
Digital IO Port Configuration		
DIO configuration		
H/W Monitor		
Monitor hardware status		

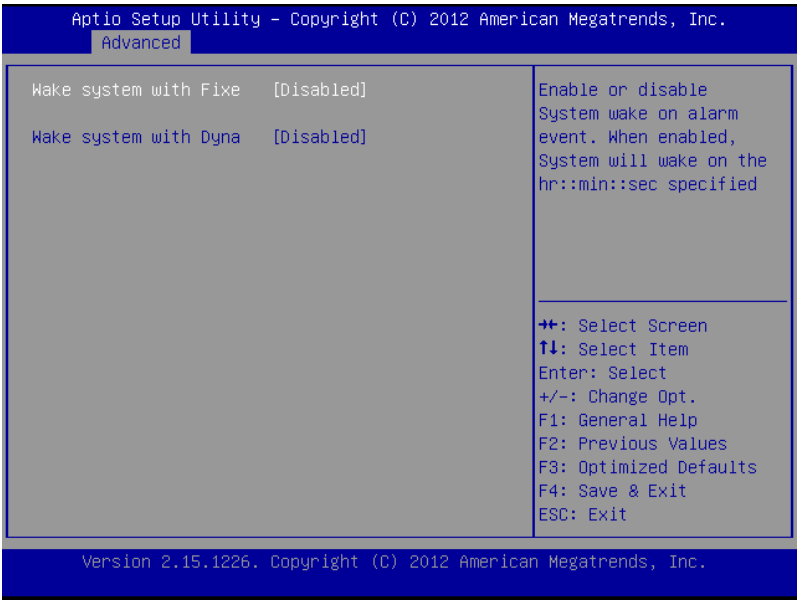
ACPI Settings



Options summary: (***default setting***)

Enable Hibernation	***Enabled***	
	Disabled	
Enabled or disabled hibernate (OS/S4 Sleep State).		
ACPI Sleep State	Suspend Disabled	
	S1 only(CPU Stop Clock)	
	S3 only(Suspend to RAM)	
	AUTO	
Select the ACPI state used for System Suspend		

S5 RTC Wake Settings

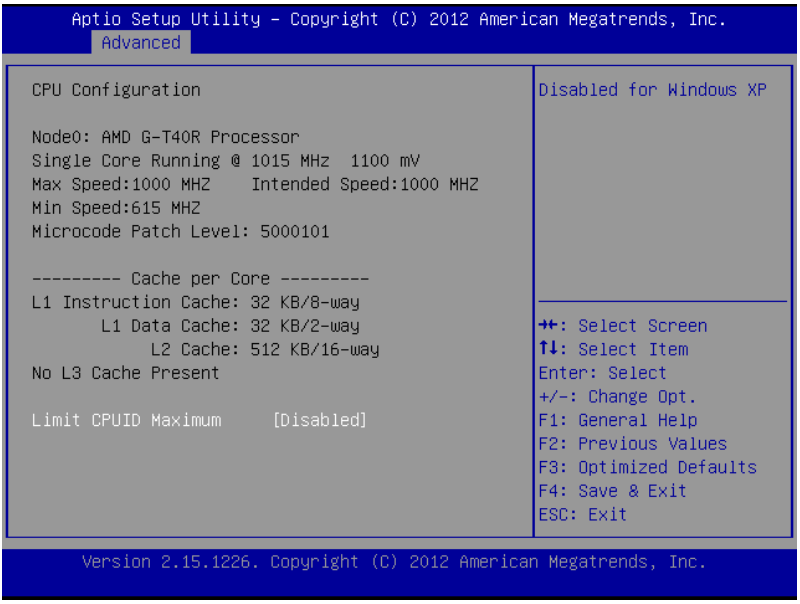


Options summary: (***default setting***)

Wake system with Fixed Time	***Disabled***	
	Enabled	
Enable or disable System wake on alarm event. Wake up time is setting by following settings.		
Wake up day	0-31	
Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0-23	

Wake up minute	0-59	
Wake up second	0-59	
Wake system with Dynamic Time	***Disabled***	
	Enabled	
Enable or disable System wake on alarm event. Wake up time is current time + Increase minutes.		
Wake up minute increase	1-5	

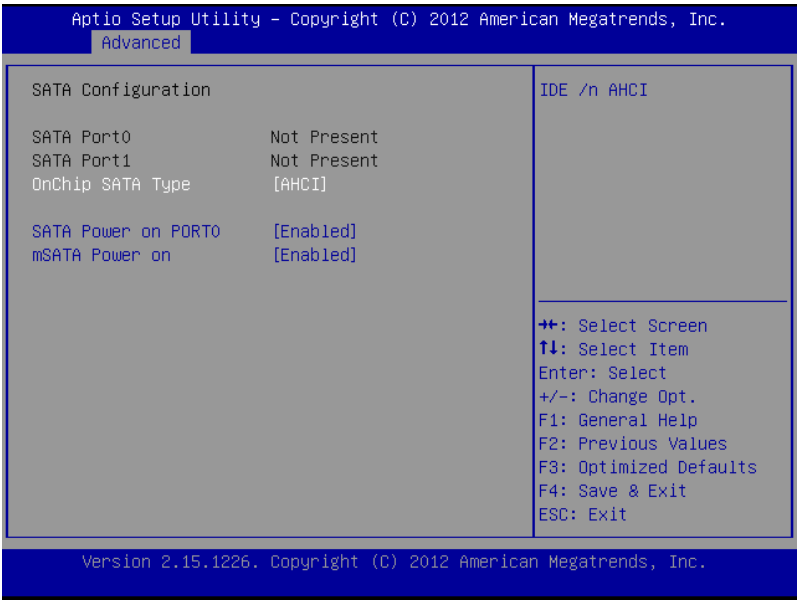
CPU Configuration



Options summary: (***default setting***)

Limit CPUID Maximum	***Disabled***	
	Enabled	
Disabled for Windows XP		

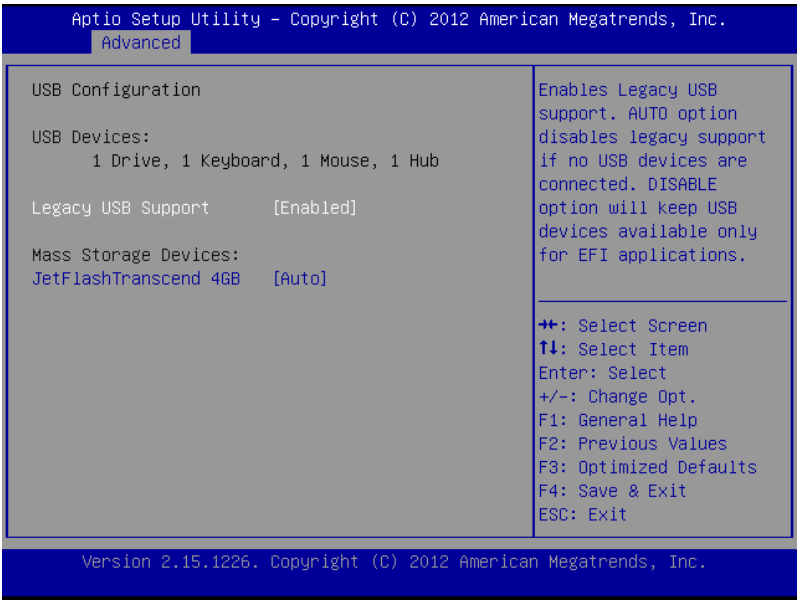
SATA Configuration



Options summary: (***default setting***)

OnChip SATA Type	IDE	
	AHCI	
Configure SATA controller operating as IDE/AHCI mode.		
SATA Power on PORT0	***Enabled***	
	Disabled	
Enable / Disable SATA port		
mSATA Power on	***Enabled***	
	Disabled	
Enable / Disable mSATA port		

USB Configuration

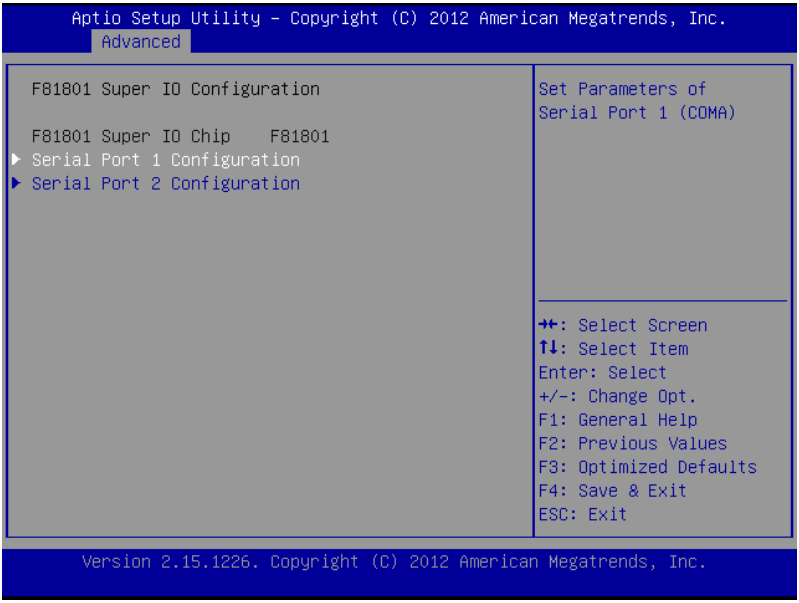


Options summary: (***default setting***)

Legacy USB Support	***Enabled***	
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application		
Device Name	**Auto**	
(Emulation Type)	Floppy	

	Forced FDD	
	Hard Disk	
	CD-ROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		

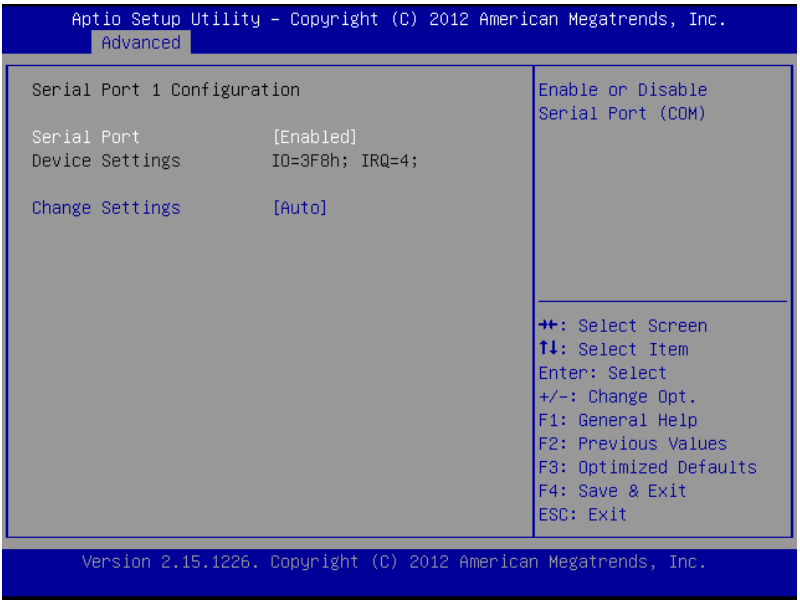
F81801 Super IO Configuration



Options summary: (***default setting***)

Serial Port 1/2 Configuration		
Set Parameters of Serial Port 1/2		

Serial Port 1 Configuration

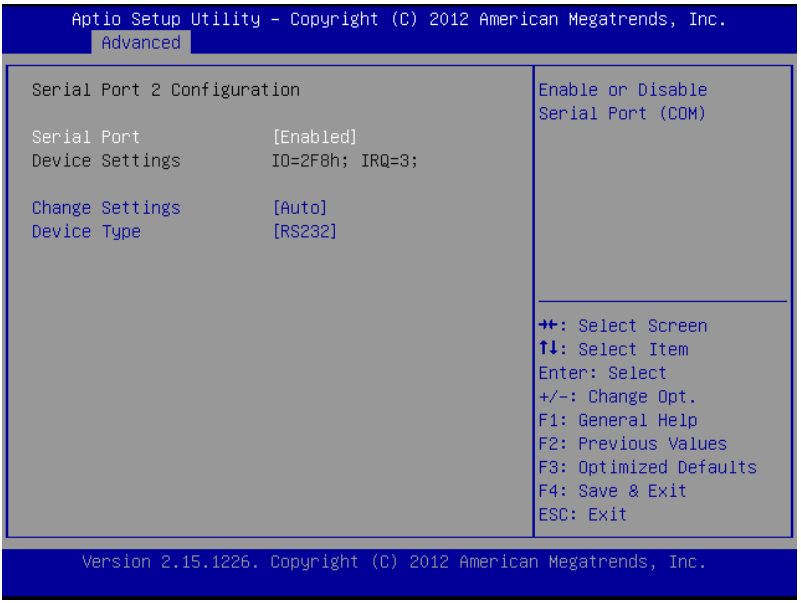


Options summary: (***default setting***)

Serial Port	Disabled	
	Enabled	
En/Disable specified serial port.		
Change Settings	***Auto***	
	IO=3F8h; IRQ=4;	
	IO=3F8h; IRQ=3,4,5,7,10,11,12;	
	IO=2F8h; IRQ=3,4,5,7,10,11,12;	

	IO=3E8h; IRQ=3,4,5,7,10,11,12;	
	IO=2E8h; IRQ=3,4,5,7,10,11,12;	
Select a resource setting for Super IO device.		

Serial Port 2 Configuration

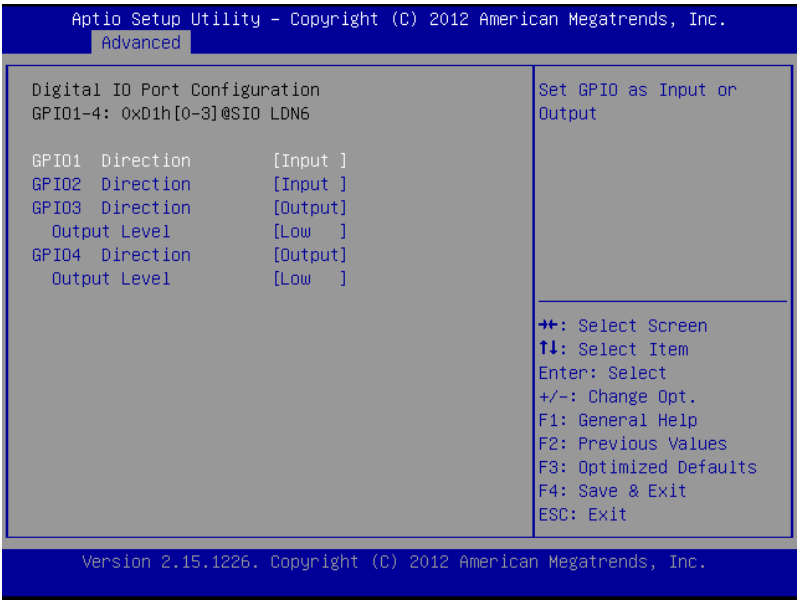


Options summary: (***default setting***)

Serial Port	Disabled	
	Enabled	
En/Disable specified serial port.		

Change Settings	***Auto***	
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4,5,7,10,11,12;	
	IO=2F8h; IRQ=3,4,5,7,10,11,12;	
	IO=3E8h; IRQ=3,4,5,7,10,11,12;	
	IO=2E8h; IRQ=3,4,5,7,10,11,12;	
Select a resource setting for Super IO device.		
Device Type	***RS232***	
	RS422	
	RS485	
Configure COM2 operated as RS232, RS422 or RS485.		

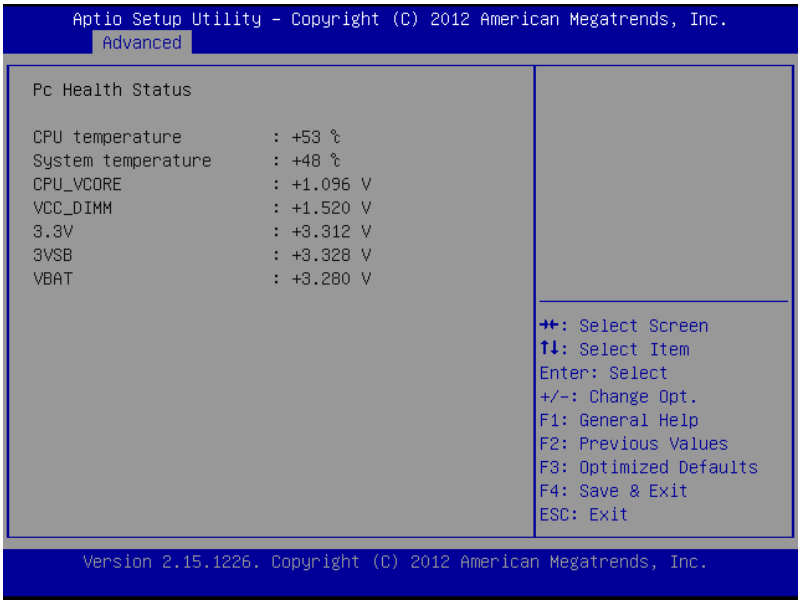
Digital IO Port Configuration



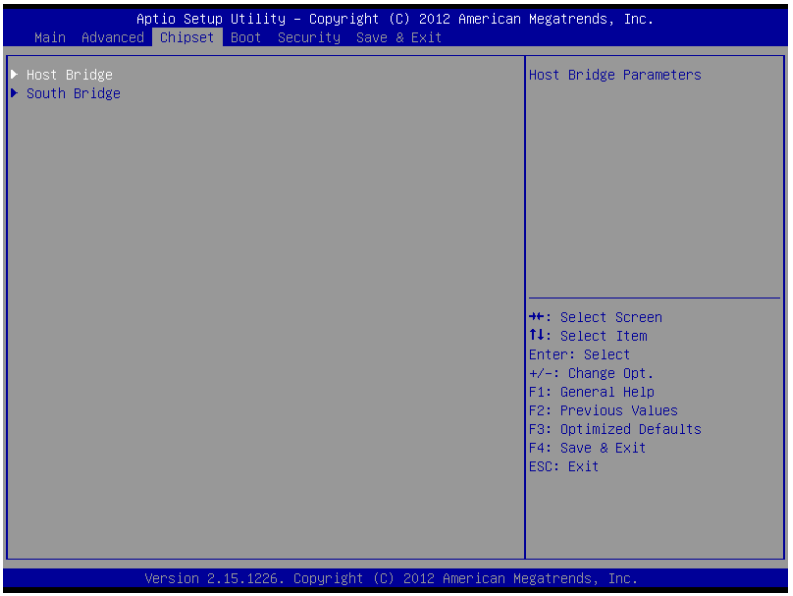
Options summary: (***default setting***)

GPIO1/GPIO2 Direction	***Input***	
	Output	
Set GPIO1/GPIO2 as Input or Output		
GPIO3/GPIO4 Direction	Input	
	Output	
Set GPIO3/GPIO4 as Input or Output		
Output Level	Hi	
	Low	
Set GPIO Level when used as Output		

H/W Monitor


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
Pc Health Status
CPU temperature : +53 °C
System temperature : +48 °C
CPU_VCORE : +1.096 V
VCC_DIMM : +1.520 V
3.3V : +3.312 V
3VSB : +3.328 V
VBAT : +3.280 V
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

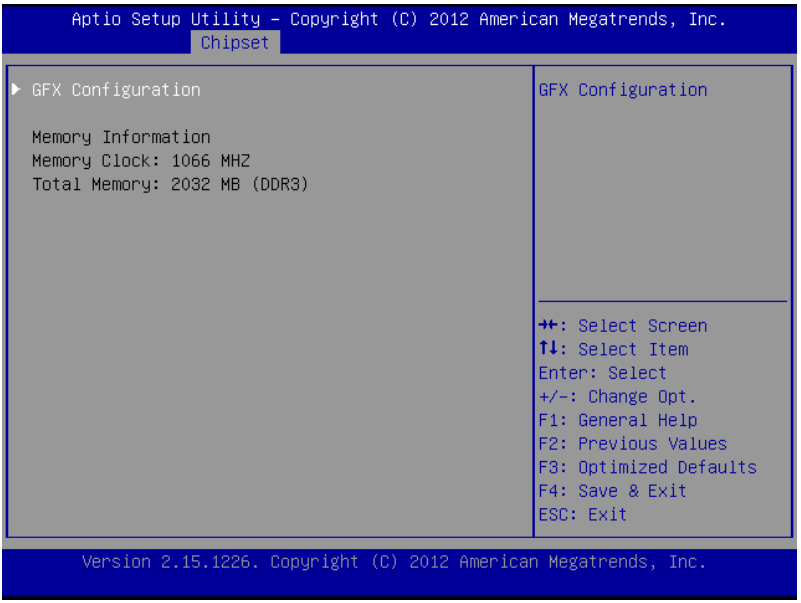
Setup submenu: Chipset



Options summary: (***default setting***)

Host Bridge		
Host Bridge Parameters		
South Bridge		
South Bridge Parameters		

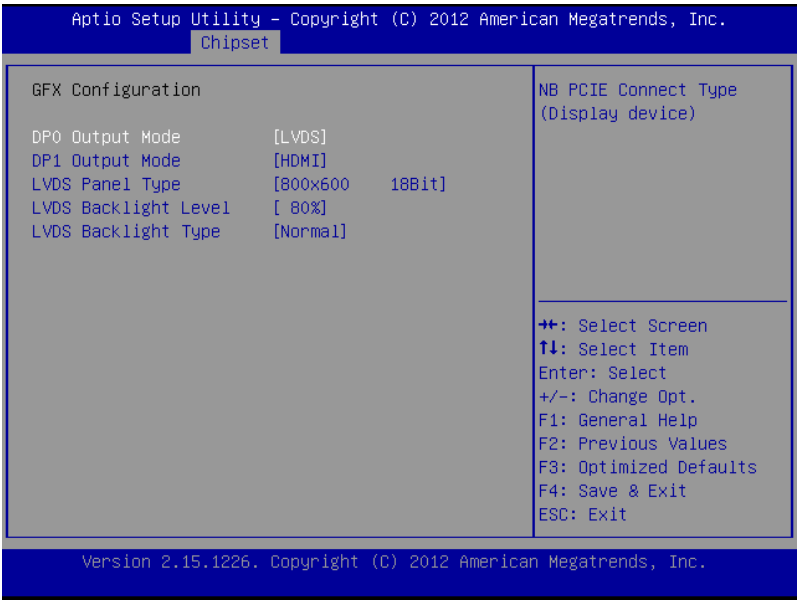
Host Bridge



Options summary: (***default setting***)

GFX Configuration		
Enter to set GFX Configuration		
Memory Information		
Show current memory information		

GFX Configuration

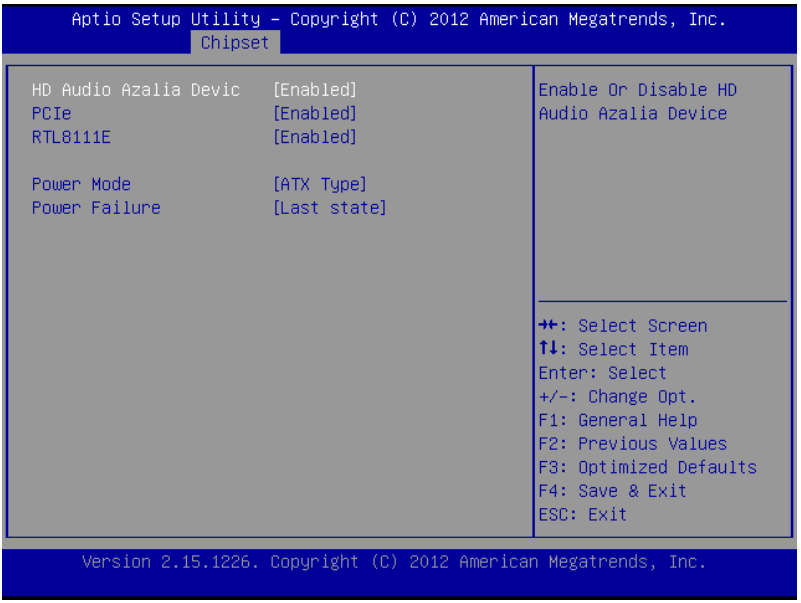


Options summary: (***default setting***)

DP0 Output Mode	***LVDS***	
	Disabled	
LVDS Enable/Disable		
DP1 Output Mode	***HDMI***	
	Disabled	
HDMI Enable/Disable		
LVDS Panel Type	640x480	
	800x600	
	1024x768	

	1280x768	
	1366x768	
Select panel native resolution. Note: Only support 18-bit panels		
LVDS Backlight Level	100%	
	90%	
	80%	
	70%	
	60%	
	50%	
	40%	
	30%	
	20%	
	10%	
	0%	
Select Backlight Level		
LVDS Backlight Type	Normal	
	Inverted	
Select Backlight control type. Inverted: Brightest for low PWM duty cycle and voltage. Normal: Brightest for high PWM duty cycle and voltage.		

South Bridge

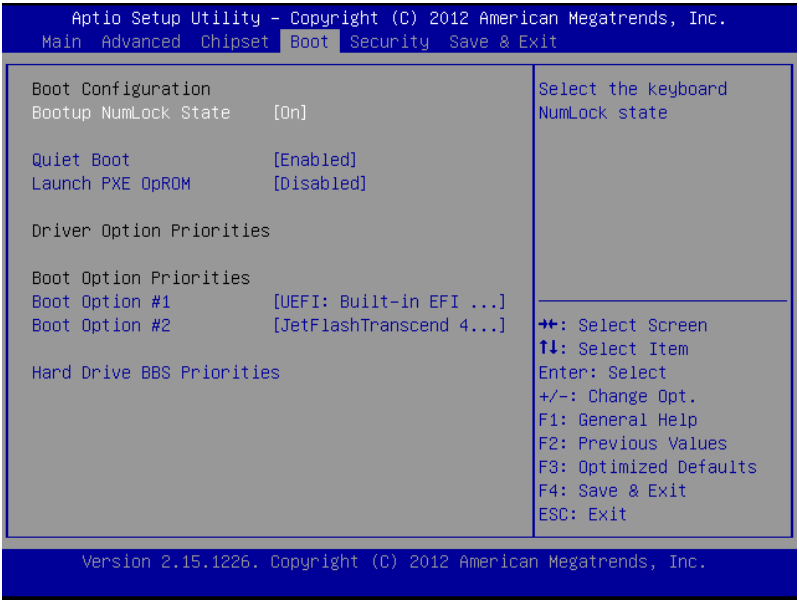


Options summary: (***default setting***)

HD Audio Azalia Device	***Enabled***	
	Disabled	
HD Audio device Enable/Disable		
PCIe	***Enable***	
	Disabled	
miniCard as PCIe Enable/Disable		
RTL8111E	***Enabled***	
	Disabled	
RTL8111E LAN Enable/Disable		

Power Mode	***ATX Type***	
	AT Type	
Select the power type used on the system		
Power Failure	Power On	
	Power Off	
	Last State	
Select AC power state when power is re-applied after a power failure.		

Boot Configuration

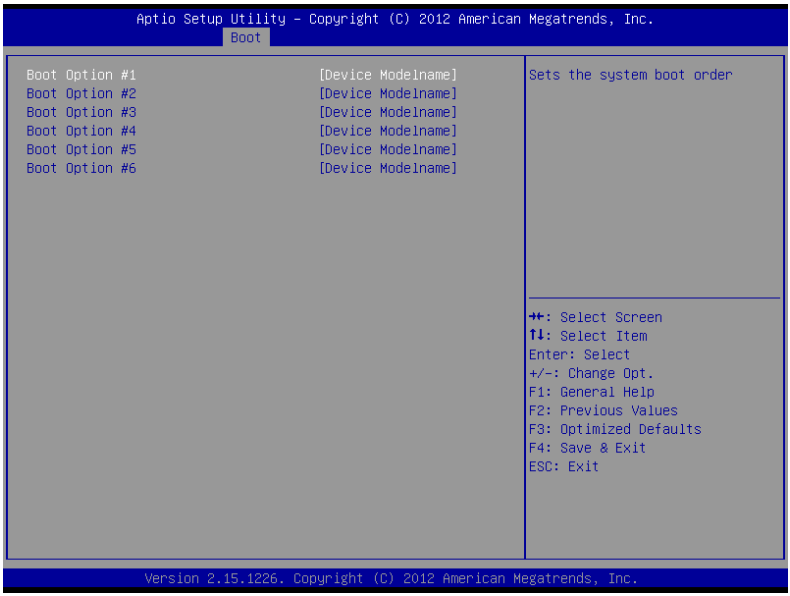


Options summary: (***default setting***)

Bootup NumLock State	***On***	

	Off	
Number Lock On/Off		
Quiet Boot	Disabled	
	Enabled	
En/Disable showing boot logo.		
Launch LAN PXE OpROM	***Disabled***	
	Enabled	
En/Disable PXE boot for RTL8111E LAN		
Boot Option #X/ XXXX Drive BBS Priorities		
The order of boot priorities.		

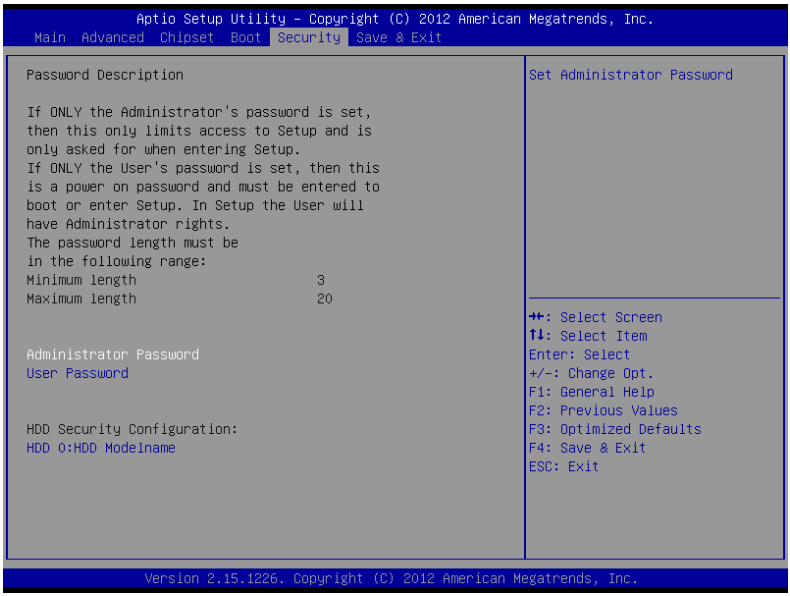
BBS Priorities



Options summary: (***default setting***)

Boot Option #x	Disabled	
	Device name	
Sets the system boot order		

Setup submenu: Security



Options summary: (***default setting***)

Administrator Password/ User Password	***Not set***	

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

Install the Password:

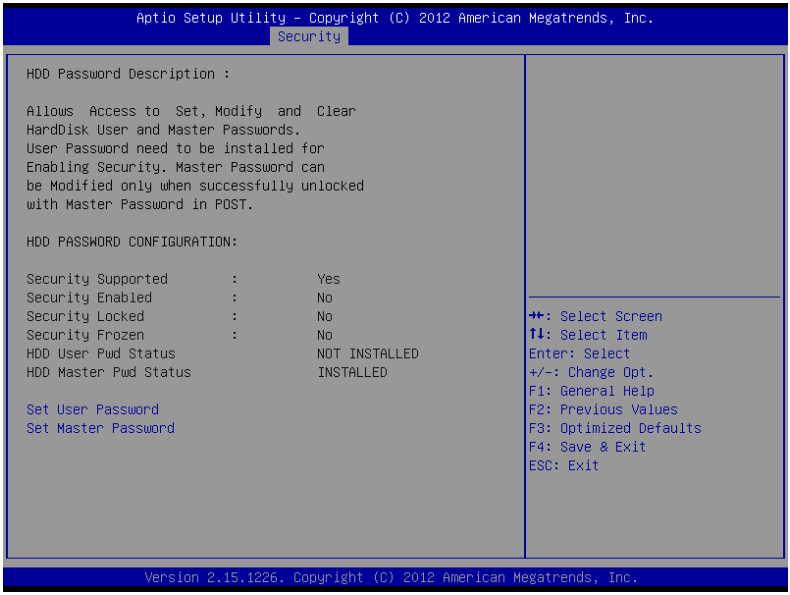
Press Enter on this item, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to

retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password:

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

HDD Security



Options summary: (***default setting***)

Set User Password/	***Not set***	
Set Master Password		

You can install a Master and User password. Before booting to OS, HDD will be set to frozen state. On S3 resume HDD will be unlocked using the HDD Password we entered while system booting.

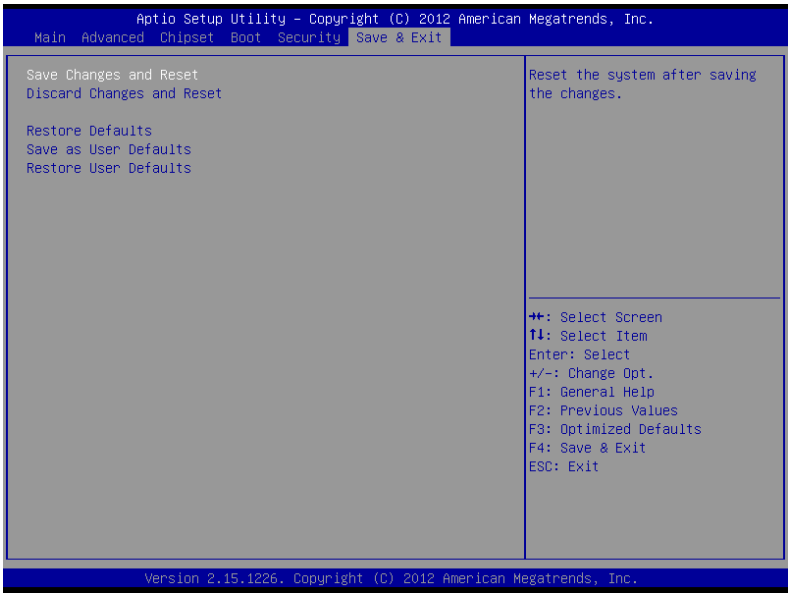
Install the Password:

Press Enter on this item, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password:

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

Setup submenu: Exit



Options summary: (***default setting***)

Save Changes and Reset		
Reset the system after saving the changes		
Discard Changes and Reset		
Reset system setup without saving any changes		
Restore Defaults		
Restore/Load Default values for all the setup options.		
Save as User Defaults		
Save the changes done so far as User Defaults		

Restore User Defaults		
Restore the User Defaults to all the setup options		

Chapter

4

Driver Installation

.

The PICO-HD01 comes with a driver disk that contains all drivers and utilities that can help you setup your product.

Insert the disk and the installation guide will start automatically. If it doesn't, please follow the sequence below to install the drivers.

Follow the sequence below to install the drivers:

Step 1 – Install Chipset Driver

Step 2 – Install AHCI Driver

Step 3 – Install LAN Driver

Step 4 – Install Audio Driver

Step 5 – Serial Port Driver (Optional)

Please refer to the instructions below for further details.

4.1 Installation:

Insert the PICO-HD01 driver disk into the disk drive. And install the drivers from Step 1 to Step 5 in order.

Step 1 – Install Chipset Driver

1. Open the ***STEP1-CHIPSET*** folder and select your OS
2. Open the ***setup.exe*** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install AHCI Driver

Please refer to the Appendix D AHCI Setting

Step 3 – Install LAN Driver

1. Open the ***STEP3-LAN*** folder and select your OS
2. Open the ***setup.exe*** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the ***STEP4-AUDIO*** folder and select your OS
2. Open the ***setup.exe*** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

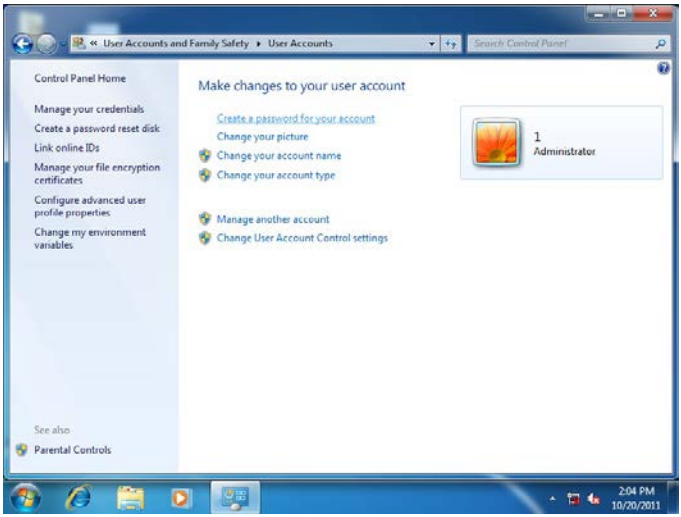
Step 5 – Serial Port Driver (Optional)

For Windows® XP:

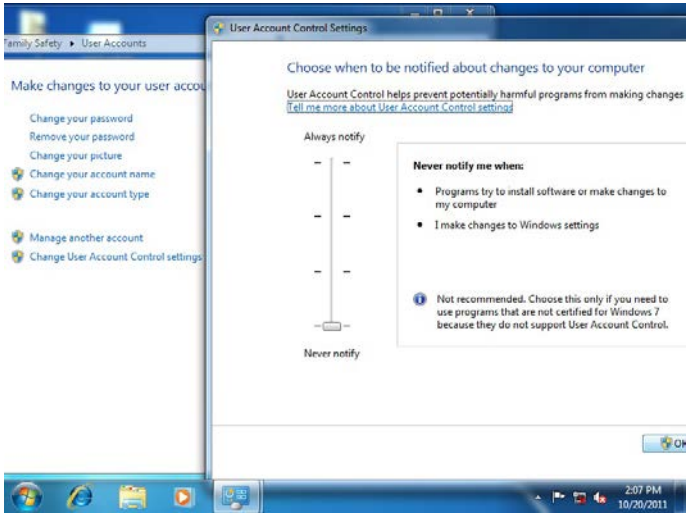
1. Open the ***STEP6-Serial Port Driver (Optional)*** and select the ***WINXP_32*** folder
2. Open ***patch.bat***
3. Follow the instructions
4. Drivers will be installed automatically

For Windows® 7:

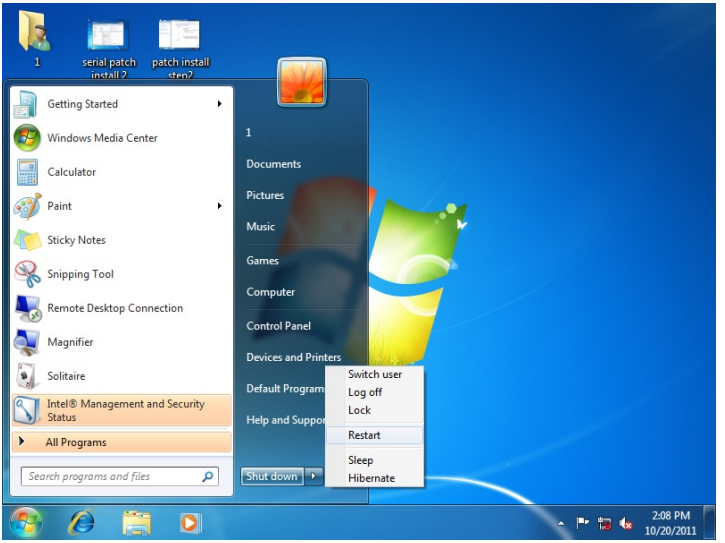
1. Create a password for Administrator account.



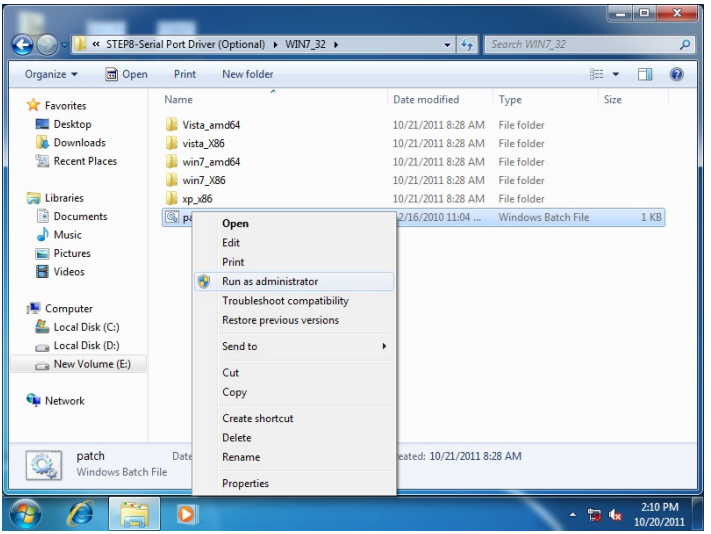
2. Change User Account Control Settings to [Never notify]



3. Reboot and Administrator login.



4. Run patch.bat as administrator.



Appendix

A

Programming the Watchdog Timer

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	**Note**
I/O Base Address	**0xA00**	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	**Offset**	**BitNum**	**Value**	**Note**
Watchdog WDTRST# Enable	**0x00**	**7**	**1**	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	**0x05**	**0:1**	**01**	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s ***Pulse width is must longer then 16ms.***
Signal Polarity	**0x05**	**2**	**0**	0: low active 1: high active ***Must set this bit to 0***
Counting Unit	**0x05**	**3**	**0**	Select time unit. 0: second 1: minute
Output Signal Type	**0x05**	**4**	**1**	0: Level 1: Pulse ***Must set this bit to 1***
Watchdog Timer Enable	**0x05**	**5**	**1**	0: Disable 1: Enable
Timeout Status	**0x05**	**6**	**1**	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	**0x06**			Time of watchdog timer (0~255)

A.2 WatchDog Sample Program

```
*************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0xA00   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
     #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
     #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
     #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
     #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
     #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
     #define   PolarityVal    0x00     // Low active for WDTRST#
     #define   UnitBit          0x03     // Unit for timer (Bit3)
     #define   ModeBit          0x04     // WDTRST# mode (Bit4)
     #define   ModeVal          0x01     // 0:level 1: pulse
     #define   EnableBit       0x05     // WDT timer enable (Bit5)
     #define   EnableVal       0x01     // 1: enable
     #define   StatusBit       0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*************************************************************************

*************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig(Counter, Unit);

        // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
```

```
        AaeonWDTEnable();
}
*****************************************************************************

*****************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
       WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (byte Counter, BOOLEAN Unit){
        // Disable WDT counting
        WDTEnableDisable(0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting(Timer, Unit);
}

VOID   WDTEnableDisable(byte Value){
        If (Value == 1)
            WDTSetBit(TimerReg, EnableBit, 1);
        else
            WDTSetBit(TimerReg, EnableBit, 0);
}

VOID   WDTParameterSetting(byte Counter, BOOLEAN Unit){
        // Watchdog Timer counter setting
       WDTWriteByte(CounterReg, Counter);
       // WDT counting unit setting
       WDTSetBit(TimerReg, UnitBit, Unit);
       // WDT output mode set to pulse
       WDTSetBit(TimerReg, ModeBit, ModeVal);
       // WDT output mode set to active low
       WDTSetBit(TimerReg, PolarityBit, PolarityVal);
       // WDT output pulse width is 25ms
```

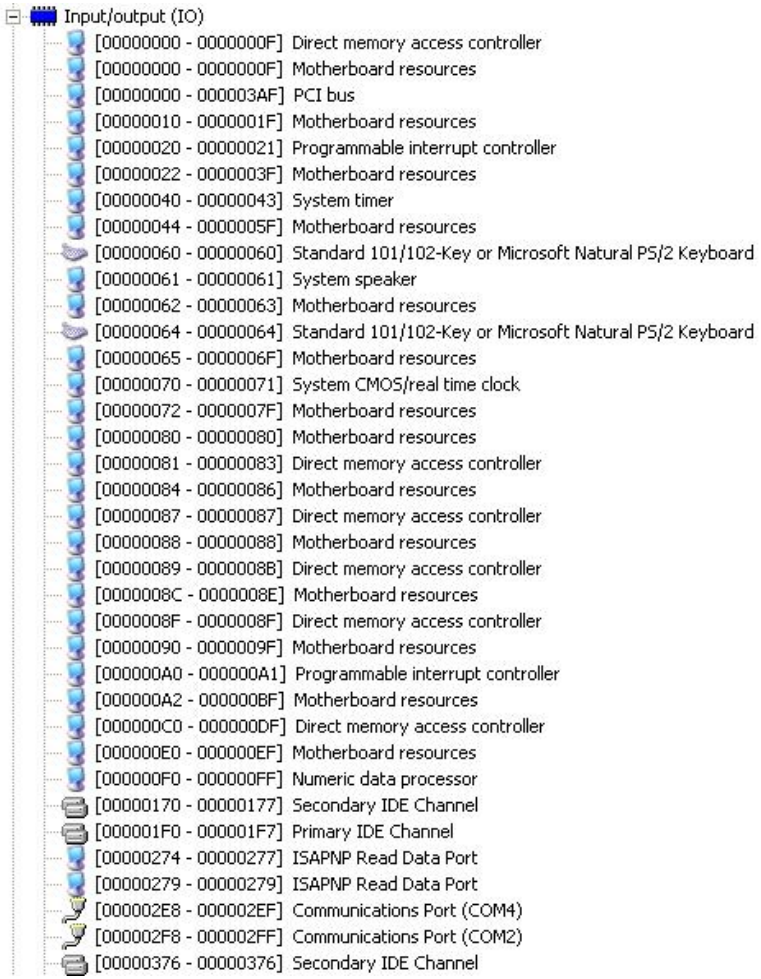
```
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
         // Watchdog WDTRST# Enable
        WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*************************************************************************

*************************************************************************
VOID   WDTWriteByte(byte Register, byte Value){
        IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
        return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
        byte TmpValue;

        TmpValue = WDTReadByte(Register);
        TmpValue &= ~(1 << Bit);
        TmpValue |= Val << Bit;
        WDTWriteByte(Register, TmpValue);
}

*************************************************************************
```

Appendix

B

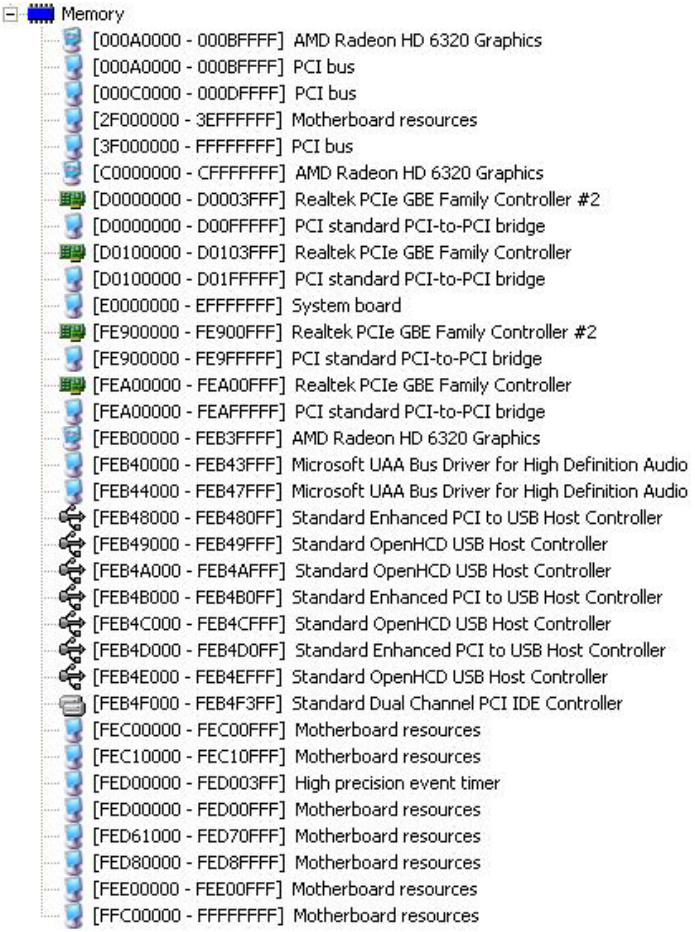
I/O Information

B.1 I/O Address Map



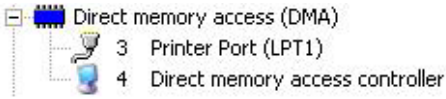
[00000378 - 0000037F] Printer Port (LPT1)
[000003B0 - 000003BB] AMD Radeon HD 6320 Graphics
[000003B0 - 000003DF] PCI bus
[000003C0 - 000003DF] AMD Radeon HD 6320 Graphics
[000003E0 - 00000CF7] PCI bus
[000003E8 - 000003EF] Communications Port (COM3)
[000003F6 - 000003F6] Primary IDE Channel
[000003F8 - 000003FF] Communications Port (COM1)
[0000040B - 0000040B] Motherboard resources
[000004D0 - 000004D1] Motherboard resources
[000004D6 - 000004D6] Motherboard resources
[00000500 - 0000050F] Motherboard resources
[00000510 - 0000051F] Motherboard resources
[00000520 - 0000052F] Motherboard resources
[00000800 - 0000089F] Motherboard resources
[00000900 - 0000090F] Motherboard resources
[00000910 - 0000091F] Motherboard resources
[00000A79 - 00000A79] ISAPNP Read Data Port
[00000B20 - 00000B3F] Motherboard resources
[00000C00 - 00000C01] Motherboard resources
[00000C14 - 00000C14] Motherboard resources
[00000C50 - 00000C51] Motherboard resources
[00000C52 - 00000C52] Motherboard resources
[00000C6C - 00000C6C] Motherboard resources
[00000C6F - 00000C6F] Motherboard resources
[00000CD0 - 00000CD1] Motherboard resources
[00000CD2 - 00000CD3] Motherboard resources
[00000CD4 - 00000CD5] Motherboard resources
[00000CD6 - 00000CD7] Motherboard resources
[00000CD8 - 00000CDF] Motherboard resources
[00000D00 - 0000FFFF] PCI bus
[0000D000 - 0000D0FF] Realtek PCIe GBE Family Controller #2
[0000D000 - 0000DFFF] PCI standard PCI-to-PCI bridge
[0000E000 - 0000E0FF] Realtek PCIe GBE Family Controller
[0000E000 - 0000EFFF] PCI standard PCI-to-PCI bridge
[0000F000 - 0000F0FF] AMD Radeon HD 6320 Graphics
[0000F100 - 0000F10F] Standard Dual Channel PCI IDE Controller
[0000F110 - 0000F113] Standard Dual Channel PCI IDE Controller
[0000F120 - 0000F127] Standard Dual Channel PCI IDE Controller
[0000F130 - 0000F133] Standard Dual Channel PCI IDE Controller
[0000F140 - 0000F147] Standard Dual Channel PCI IDE Controller
[0000F150 - 0000F15F] Standard Dual Channel PCI IDE Controller
[0000FE00 - 0000FEFE] Motherboard resources

B.2 Memory Address Map



B.3 IRQ Mapping Chart

B.4 DMA Channel Assignments



Appendix

C

Mating Connector

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model number		
CN1	Digital I/O	CATCH	1201-700-06S	AAEON DIO Extension Cable	1701060150
CN2	COM1 Port	CATCH	1201-700-09S	Serial Port Cable	1701090150
CN3	COM2 Port	CATCH	1201-700-09S	Serial Port Cable	1701090150
CN4	+5V Output for SATA HDD	CATCH	1192-700-02S	2 Pins for SATA PWR Cable	1702150155
CN5	SATA Port	ASTRON	97-0912HA-7-R	7 Pin 50cm SATA Cable	1709070500
CN6	External 12V Input	CATCH	1191-700-04S	PWR Cable	170204010S
CN7	RJ-45 Ethernet	UDE	RT7-17FAAM1A	N/A	N/A
CN8	Buzzer	CATCH	1201-700-02S	Buzzer Cable	170302010C
CN9	Audio Line In/Out and MIC Connector	CATCH	1201-700-10S	Audio Cable	1709100254
CN10	LPC Expansion I/F	CATCH	1204-700-12S	AAEON LPC Cable	1703120130

CN11	USB Port 5	CATCH	1201-700-05S	USB Port Cable	1700050207
CN12	Analog CRT Display	ASTRON	HDLH-B15-CF HN1T-1-R	N/A	N/A
CN13	USB Port 3	CATCH	1201-700-05S	USB Port Cable	1700050207
CN14	USB Port 4	CATCH	1201-700-05S	USB Port Cable	1700050207
CN15	18-bit LVDS Output	E-Call	0110-01-553-20 0	N/A	N/A
CN16	USB Port 1 and 2	TechBest	KS-002D-ANB(2.0)-L	N/A	N/A
CN17	HDMI Type C	ASTRON	360FC19-0N00 2T-R	N/A	N/A
CN18	LVDS Inverter/ Backlight Connector	CATCH	1192-700-05S	N/A	N/A
CN19	Front Panel	JVE	21B22050-XXS 10B-01G-4/2	AAEON Front Panel Cable	1701100156
BAT1	External RTC Battery Connector	CATCH	1201-700-02S	Battery Cable	175011901 M

Appendix

D

AHCI Setting

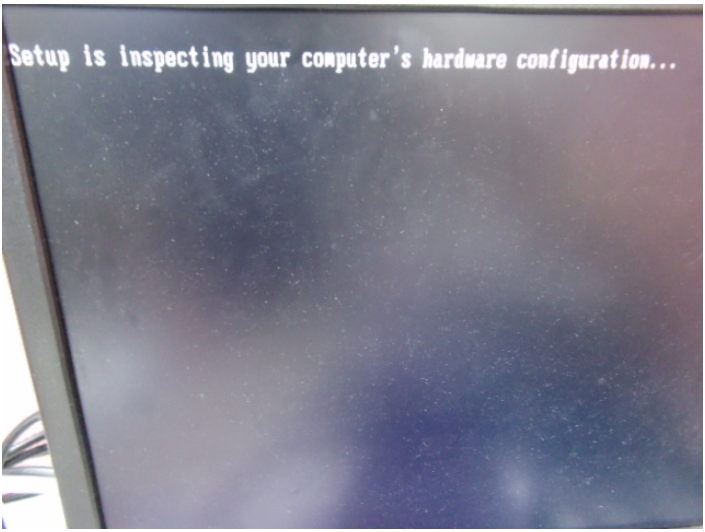
D.1 Setting AHCI

OS installation to setup AHCI Mode.

Step 1: Copy the files below from “Driver DVD -> STEP4-AHCI\WinXP\SB8xx_RAID_XP_3.2.1540.92” to Disk

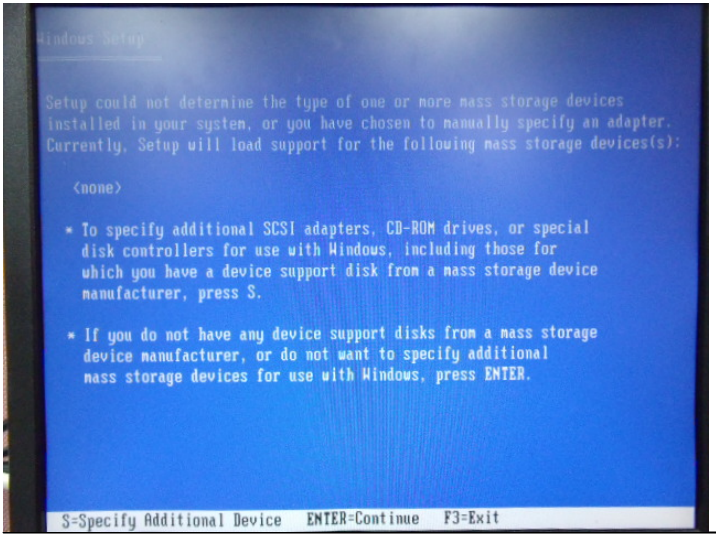
Step 2: Connect the USB Floppy to the board

Step 3: Setup OS

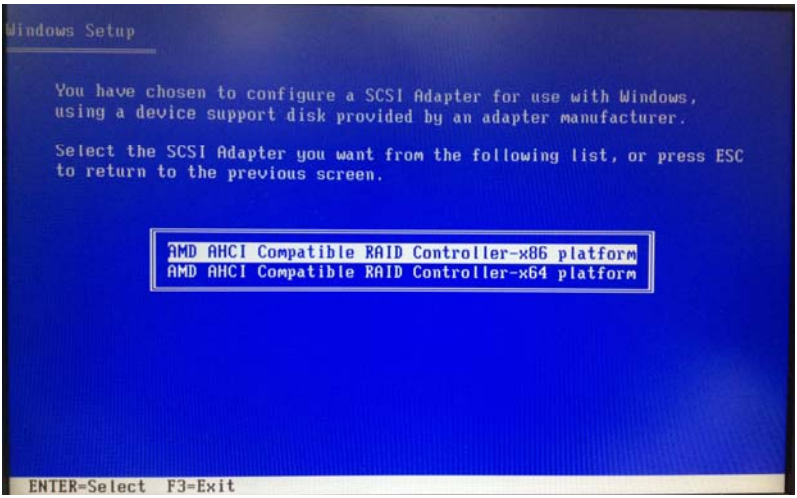


Step 4: Press "**F6**"

Step 5: Choose "**S**"

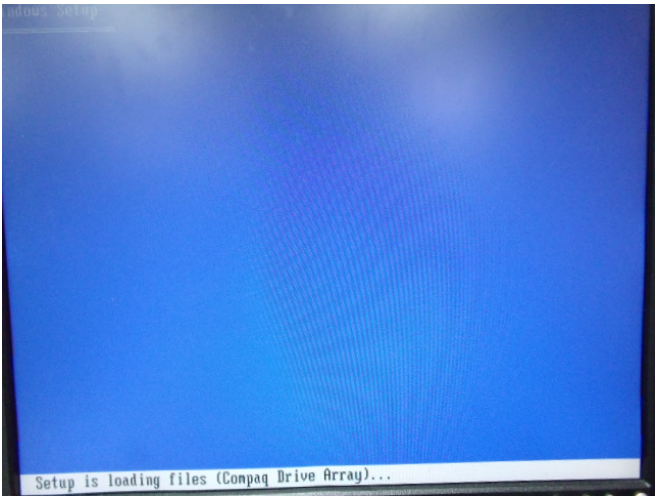


Step 6: Choose **"AMD AHCI Compatible RAID Controller-x86 platform**"



Step 7: It will show the model number you select and then press "**ENTER**

Step 8: Setup is loading files



Appendix

E

Electrical Specifications for I/O Ports

E.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification						
Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO1	I/O	0.8	2.0	0	3.3	
DIO2	I/O	0.8	2.0	0	3.3	
DIO3	I/O	0.8	2.0	0	3.3	
DIO4	I/O	0.8	2.0	0	3.3	

Note: All DIO pins are 5V tolerance in input mode.

E.2 DIO Programming

PICO-HD01 utilizes FINTEK F81801U chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DIO program is also attached based on which you can develop customized program to fit your application. There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

E.3 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	**Note**
Index	**0x2E**	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	**0x2F**)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	**Register**	**BitNum**	**Note**
GPIO1 Direction	**0x06**	**0xD0**	**0**	0:input, 1: output
GPIO2 Direction	**0x06**	**0xD0**	**1**	
GPIO3 Direction	**0x06**	**0xD0**	**2**	
GPIO4 Direction	**0x06**	**0xD0**	**3**	
GPIO1 Output Level	**0x06**	**0xD1**	**0**	0:low, 1: high
GPIO2 Output Level	**0x06**	**0xD1**	**1**	
GPIO3 Output Level	**0x06**	**0xD1**	**2**	
GPIO4 Output Level	**0x06**	**0xD1**	**3**	
GPIO1 Status	**0x06**	**0xD2**	**0**	0:low, 1: high
GPIO2 Status	**0x06**	**0xD2**	**1**	
GPIO3 Status	**0x06**	**0xD2**	**2**	
GPIO4 Status	**0x06**	**0xD2**	**3**	

E.4 Digital I/O Sample Program

```
*************************************************************************
// SuperIO relative definition (Please reference to Table 2)
#define   SIOIndex   0x2E
#define   SIOData    0x2F
#define   DIOLDN     0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define   DirReg          0xD0          // 0:input, 1: output
    #define   InputPin      0x00
    #define   OutputPin     0x01
#define   OutputReg     0xD1          // 0:low, 1: high
#define   StatusReg     0xD2          // 0:low, 1: high
    #define   PinLow        0x00
    #define   PinHigh       0x01
#define   Pin1Bit       0x00
#define   Pin2Bit       0x01
#define   Pin3Bit       0x02
#define   Pin4Bit       0x03
*************************************************************************

*************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //       Example, Read Digital I/O Pin 3 status
        // Output :
        //       InputStatus :
        //                0: Digital I/O Pin level is low
        //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(Pin3Bit);
```

```
        // Procedure : AaeonSetOutputLevel
        // Input :
        //       Example, Set Digital I/O Pin 2 to high level
        AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****************************************************************************

*****************************************************************************
Boolean   AaeonReadPinStatus(byte PinBit){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(DIOLDN, StatusReg, PinBit);
        Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte PinBit, byte Value){
        ConfigDioMode(PinBit, OutputPin);
        SIOBitSet(DIOLDN, OutputReg, PinBit, Value);
}
*****************************************************************************

*****************************************************************************VOI
D   SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;
```

```
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

```
**************************************************************************
Boolean   SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID   ConfigDioMode(byte PinBit, byte Mode){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(DIOLDN);
        IOWriteByte(SIOIndex, DirReg);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (Mode << PinBit);
        IOWriteByte(SIOData, DirReg);
        SIOExitMBPnPMode();
}
**************************************************************************
```