PICO-APL4

PICO-ITX Board

User's Manual 4th Ed

Last Updated: April 25, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
PICO-APL4	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Pico-ITX
CPU	Intel® Pentium® N4200 (4C. 1.1 GHz, up to 2.5 GHz, TDP 6W) Intel® Celeron® N3350 (2C. 1.1 GHz, up to 2.4 GHz, TDP 6W) Intel® Atom® x7-Series (4C. 1.6GHz, up to 2.00 GHz, TDP 12W)
CPU Frequency	Up to 2.4GHz
Chipset	Intel® SoC
Memory Type	Onboard DDR3L 2G (Optional to 4G)
Max. Memory Capacity	Up to 4GB
BIOS	AMI/SPI
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V, AT/ATX
Power Supply Type	Lockable & Phoenix Terminal co-lay
Power Consumption (Typical)	Intel®Pentium®N4200@1.1GHz,DDR3L 4GB 1.43A@+12V
System Cooling	Heat-spreader, heatsink & cooler (Optional)
Dimension	3.94" x 2.84" (100mm x 72mm)

System

Gross Weight	0.55 lb (0.25 kg)
Operating Temperature	32˚F ~ 140˚F (0˚C ~ 60˚C)
Storage Temperature	-40˚F ~ 176˚F (-40˚C ~ 80˚C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	191,895
Certification	CE,FCC

Display

Chipset	Intel® SoC
Resolution	HDMI 1.4b: 3840 x 2160@30Hz Internal eDP: 3840 x 2160@60Hz (Optional) DDI (Optional from BIO)
LCD Interface	eDP

I/O

Storage/SSD	SATA 6.0Gb/s x 1, 5V Power reserved M.2 2280 (B Key) x 1 eMMC 16G (optional to 32/64G)
Ethernet	Realtek 8111G x 2
USB Port	USB 3.0 x 2 Rear IO USB 2.0 x 2 (Internal, co-use with FAN connector)
Serial Port	COM1: RS-232 x 1 COM2: RS-232/422/485 x 1

I/O

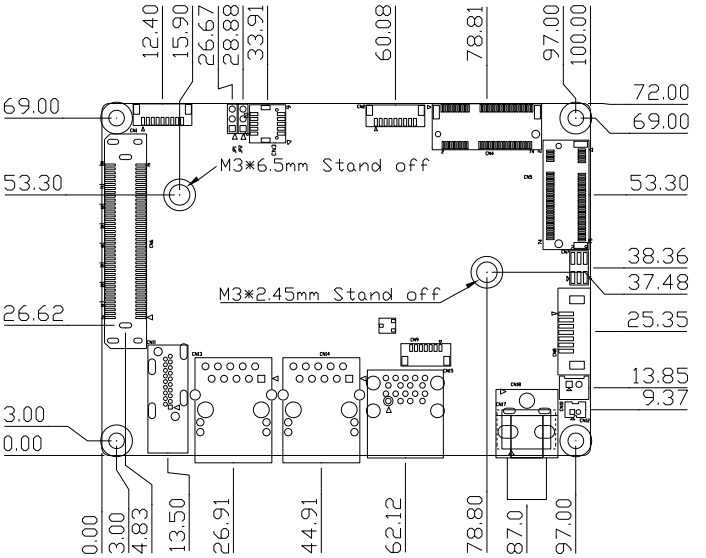
Audio	—
DIO	4-bit
Expansion Slot	M.2 2230 x 1 (E-Key) BIO x 1 (optional) I2C, Smbus
SIM	—
TPM	—
Touch	—

Chapter 2

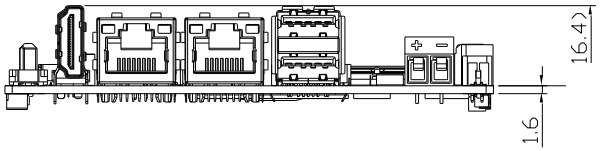
Hardware Information

2.1 Dimensions

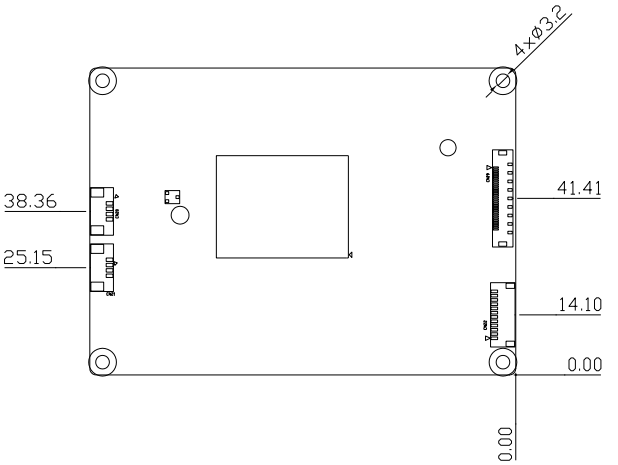
Component Side



Component Side



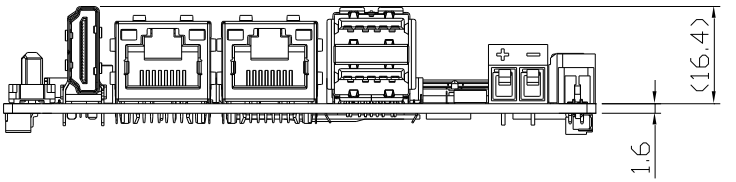
Solder Side



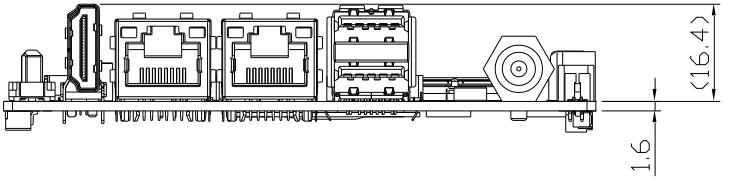
Solder Side

Rear I/O Configuration

Phoenix

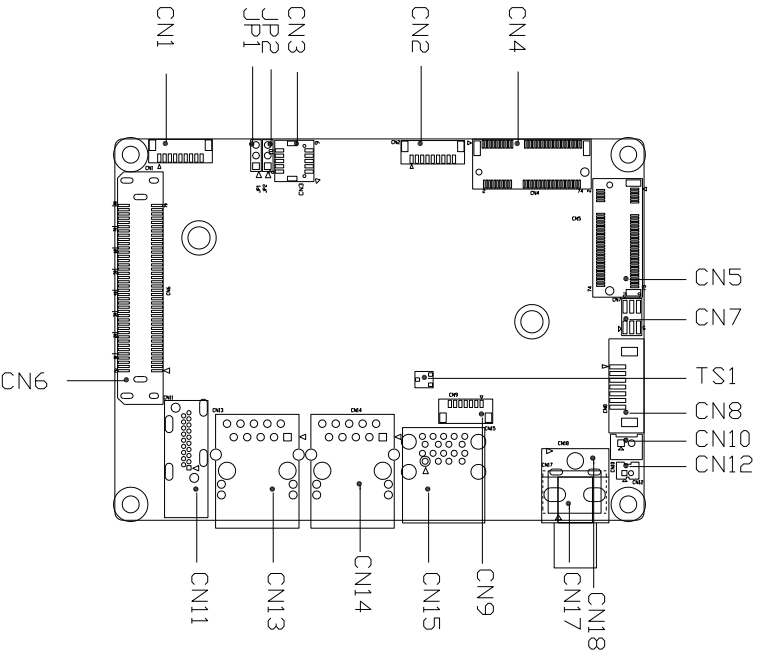


DC Jack

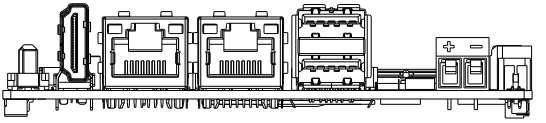


2.2 Jumpers and Connectors

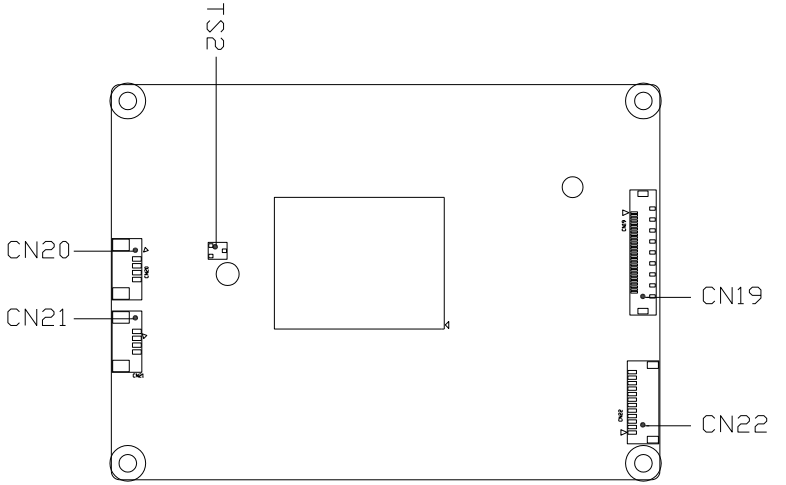
Component Side



Component Side



Solder Side



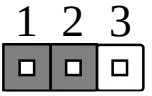
Solder Side

2.3 List of Jumpers

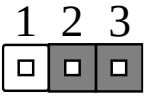
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	Auto Power Button Enable/Disable Selection
JP2	Clear CMOS Jumper

2.3.1 Auto Power Button Enable/Disable Selection (JP1)



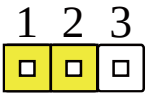
Enable/AT (Default)



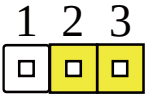
Disable/ATX

※ When disabled, the power button of CN3 (1-2) will be used to power on the system

2.3.2 Clear CMOS Jumper (JP2)



Normal (Default)



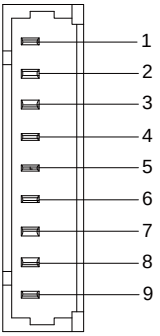
Clear CMOS

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	COM Port 2
CN2	COM Port 1
CN3	Front Panel Connector
CN4	M.2 Key-E Slot (2230)
CN5	M.2 Key-B Slot (2280)
CN6	BIO Port (Optional)
CN7	Digital I/O
CN8	SATA Port
CN9	SPI Flash Programming Port
CN10	+5V Output for SATA HDD
CN11	HDMI Port
CN12	Battery
CN13	LAN (RJ-45) Port1
CN14	LAN (RJ-45) Port2
CN15	USB 3.0 Ports 0 and 1
CN17	External Power Input
CN18	+12V DC Power Jack (Optional)
CN19	Embedded DisplayPort (Optional)
CN20	USB 2.0 Port 2
CN21	USB 2.0 Port 1

2.4.1 COM Port 2 (CN1)



RS232			
Pin	Pin Name	Signal Type	Pin Name
1	DCD2	IN	
2	DSR2	IN	
3	RX2	IN	
4	RTS2	OUT	±5V
5	TX2	OUT	±5V
6	CTS2	IN	
7	DTR2	OUT	±5V
8	RI2/+5V/+12V	IN	+5V/+12V
9	GND	GND	

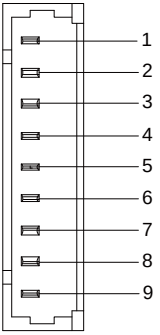
RS485			
Pin	Pin Name	Signal Type	Pin Name
1	RS485_ D2-	I/O	±5V
2	NC		
3	RS485_D2+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

RS422			
Pin	Pin Name	Signal Type	Pin Name
1	RS422_TX2-	OUT	±5V
2	NC		
3	RS422_TX2+	OUT	±5V
4	NC		
5	RS422_RX2+	IN	
6	NC		
7	RS422_RX2-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

※ COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

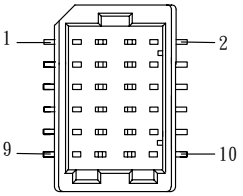
※ Pin 8 function can be changed by BOM.

2.4.2 COM Port 1 (CN2)



RS232			
Pin	Pin Name	Signal Type	Pin Name
1	DCD1	IN	
2	DSR1	IN	
3	RX1	IN	
4	RTS1	OUT	±9V
5	TX1	OUT	±9V
6	CTS1	IN	
7	DTR1	OUT	±9V
8	RI1	IN	
9	GND	GND	

2.4.3 Front Panel Connector (CN3)



Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

2.4.4 M.2 Key-E Slot (2230) (CN4)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+3.3VSB	PWR	+3.3V
3	USB_D+	DIFF	
4	+3.3VSB	PWR	+3.3V
5	USB_D-	DIFF	
6	NC		
7	GND	GND	

8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	
22	NC	
23	NC	
32	NC	
33	GND	GND
34	NC	
35	PCIE_TX+	DIFF
36	NC	

37	PCIE_TX-	DIFF	
38	NC		
39	GND	GND	
40	NC		
41	PCIE_RX+	DIFF	
42	NC		
43	PCIE_RX-	DIFF	
44	NC		
45	GND	GND	
46	NC		
47	PCIE_REF_CLK+	DIFF	
48	NC		
49	PCIE_REF_CLK-	DIFF	
50	NC		
51	GND	GND	
52	PCIE_RST#	OUT	+3.3V
53	PCIE_CLK_REQ#	IN	+3.3V
54	W_DISABLE2#	OUT	+3.3V
55	PCIE_WAKE#	IN	+3.3V
56	W_DISABLE1#	OUT	+3.3V
57	GND	GND	

58	NC		
59	NC		
60	NC		
61	NC		
62	NC		
63	GND	GND	
64	NC		
65	NC		
66	+3.3VSB	PWR	+3.3V
67	NC		
68	NC		
69	GND	GND	
70	NC		
71	NC		
72	+3.3VSB	PWR	+3.3V
73	NC		
74	+3.3VSB	PWR	+3.3V
75	GND	GND	

2.4.5 M.2 Key-B Slot (2280) (CN5)

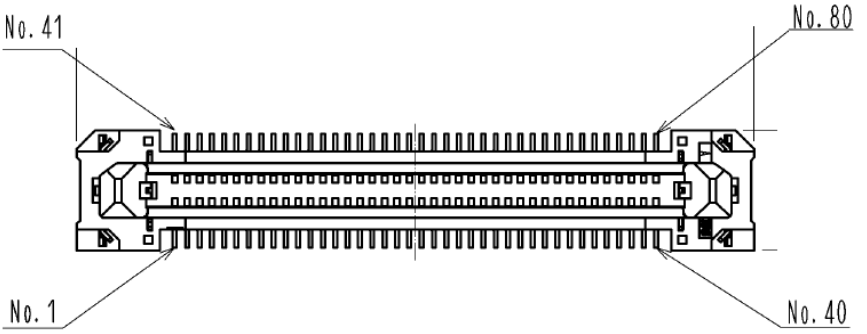
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+3.3V	PWR	+3.3V
3	GND	GND	
4	+3.3V	PWR	+3.3V
5	GND	GND	
6	NC		
7	USB_D+	DIFF	
8	NC		
9	USB_D-	DIFF	
10	SSD_DAS#	IN	+3.3V
11	NC		
20	NC		
21	GND	GND	
22	NC		
23	NC		
24	NC		
25	NC		
26	NC		
27	GND	GND	

28	NC		
29	NC		
30	NC		
31	NC		
32	NC		
33	GND	GND	
34	NC		
35	NC		
36	NC		
37	NC		
38	DEVSLP	OUT	+1.8V
39	GND	GND	
40	NC		
41	SATA_RX+	DIFF	
42	NC		
43	SATA_RX-	DIFF	
44	NC		
45	GND	GND	
46	NC		
47	SATA_TX-	DIFF	
48	NC		

49	SATA_TX+	DIFF
50	NC	
51	GND	GND
52	NC	
53	NC	
54	NC	
55	NC	
56	NC	
57	GND	GND
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	GND	GND
64	NC	
65	NC	
66	NC	
67	NC	
68	NC	
69	GND	GND

70	+3.3V	PWR	+3.3V
71	GND	GND	
72	+3.3V	PWR	+3.3V
73	GND	GND	
74	+3.3V	PWR	+3.3V
75	GND	GND	

2.4.6 BIO Port (Optional) (CN6)



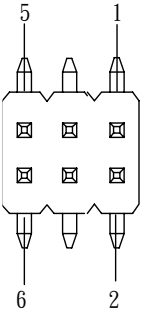
Pin	Pin Name	Signal Type	Signal Level
1	+12VSB	PWR	+12V
2	GND	GND	
3	GND	GND	
4	PCIE_TXN0	DIFF	
5	PCIE_RXN0	DIFF	
6	PCIE_TXP0	DIFF	
7	PCIE_RXP0	DIFF	

Pin	Pin Name	Signal Type	Signal Level
8	GND	GND	
9	GND	GND	
10	PCIE_TXN1	DIFF	
11	PCIE_RXN1	DIFF	
12	PCIE_TXP1	DIFF	
13	PCIE_RXP1	DIFF	
14	GND	GND	
15	GND	GND	
16	PS_ON#	OUT	
17	DDI_DDCCLK	I/O	+3.3V
18	DDI_DDCDATA	I/O	+3.3V
19	+5VSB	PWR	+5V
20	+5VSB	PWR	+5V
21	+5VSB	PWR	+5V
22	+5VSB	PWR	+5V
23	PCIE_REF_CLK0	DIFF	
24	RESET#	OUT	
25	PCIE_REF_CLK0#	DIFF	
26	GND	GND	
27	GND	GND	
28	DDI_TX1N	DIFF	
29	DDI_TX0N	DIFF	
30	DDI_TX1P	DIFF	
31	DDI_TX0P	DIFF	
32	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
33	GND	GND	
34	DDI_TX3N	DIFF	
35	DDI_TX2N	DIFF	
36	DDI_TX3P	DIFF	
37	DDI_TX2P	DIFF	
38	GND	GND	
39	GND	GND	
40	DDI_HPD	IN	+5V
41	DDI_AUXN	DIFF	
42	GND	GND	
43	DDI0_AUXP	DIFF	
44	USB3_TX_N	DIFF	
45	GND	GND	
46	USB_D0-	DIFF	
47	USB3_TX_P	DIFF	
48	GND	GND	
49	USB_D0+	DIFF	
50	USB3_RX_N	DIFF	
51	GND	GND	
52	USB3_RX_P	DIFF	
53	SMB_CLK	I/O	+3.3V
54	GND	GND	
55	SMB_DATA	I/O	+3.3V
56	WAKE#	IN	+3.3V
57	GND	GND	

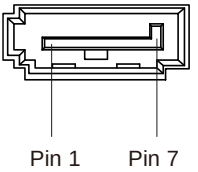
Pin	Pin Name	Signal Type	Signal Level
58	USB_OC#	IN	+3.3V
59	+5V	PWR	+5V
60	USB_OC#	IN	+3.3V
61	+5V	PWR	+5V
62	+5V	PWR	+5V
63	+5V	PWR	+5V
64	+5V	PWR	+5V
65	LPC_AD0	I/O	+3.3V
66	LPC_FRAME#	IN	+3.3V
67	LPC_AD1	I/O	+3.3V
68	SERIRQ	I/O	+3.3V
69	LPC_AD2	I/O	+3.3V
70	NC		
71	LPC_AD3	I/O	+3.3V
72	BIO_PWOK	IN	+3.3V
73	GND	GND	
74	AGND	GND	
75	LPC_CLK	OUT	+3.3V
76	NC		
77	PME#	IN	+3.3V
78	NC		
79	GND	GND	
80	GND	GND	

2.4.7 Digital I/O (CN7)



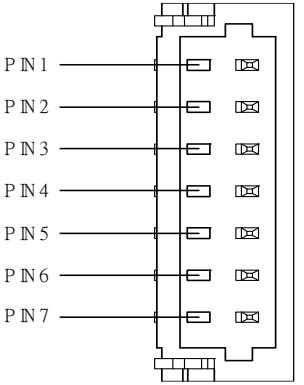
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	DIO0	I/O	+5V
3	DIO1	I/O	+5V
4	DIO2	I/O	+5V
5	DIO3	I/O	+5V
6	GND	GND	

2.4.8 SATA Port (CN8)



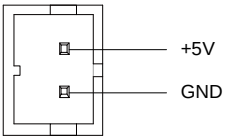
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.9 SPI Flash Programming Port (CN9)



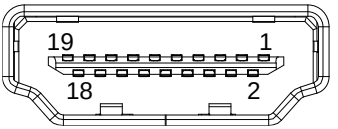
Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

2.4.10 +5V Output for SATA HDD (CN12)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

2.4.11 HDMI Port (CN11)



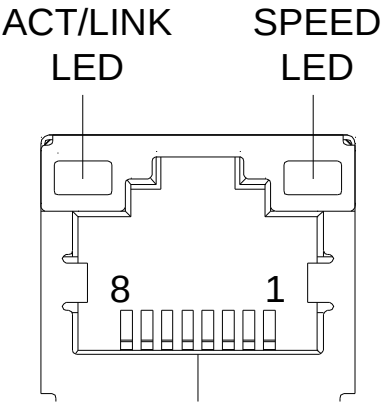
Pin	Pin Name	Signal Type	Signal level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	

Pin	Pin Name	Signal Type	Signal level
10	TMDS_CLK+	DIFF	
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.4.12 Battery (CN12)

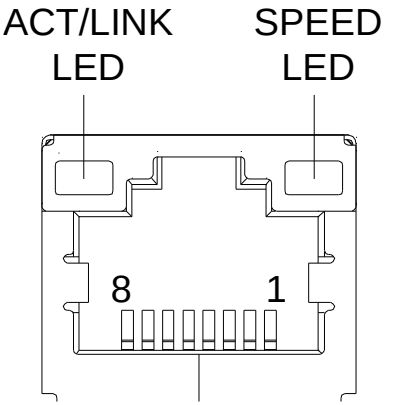
Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.13 LAN (RJ-45) Port1 (CN13)



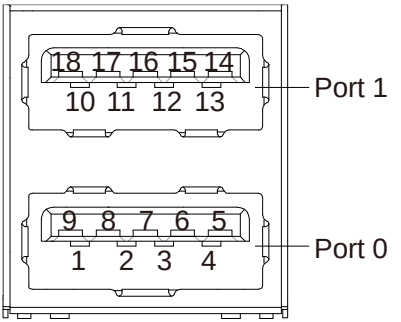
Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.14 LAN (RJ-45) Port2 (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

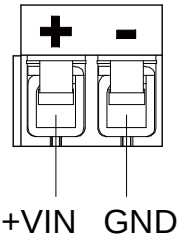
2.4.15 USB 3.0 Ports 0 and 1 (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−	DIFF	

Pin	Pin Name	Signal Type	Signal Level
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX–	DIFF	
18	USB1_SSTX+	DIFF	

2.4.16 External Power Input (CN17)



Pin	Pin Name	Signal Type	Signal Level
1	+VIN	PWR	+12V
2	GND	GND	

2.4.17 +12V DC Power Jack (Optional) (CN18)

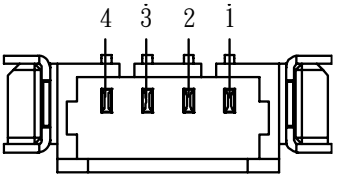
Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	
3	GND	GND	

2.4.18 Embedded DisplayPort (Optional) (CN19)

Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	+12V	PWR	+12V
3	GND	GND	
4	GND	GND	
5	EDP_TX2_N	DIFF	
6	EDP_TX2_P	DIFF	
7	GND	GND	
8	EDP_TX1_N	DIFF	
9	EDP_TX1_P	DIFF	
10	GND	GND	
11	EDP_TX0_N	DIFF	
12	EDP_TX0_P	DIFF	
13	GND	GND	
14	EDP_TX3_N	DIFF	
15	EDP_TX3_P	DIFF	
16	GND	GND	
17	EDP_AUXN	DIFF	
18	EDP_AUXP	DIFF	
19	GND	GND	
20	EDP_BKLTNESS	OUT	+3.3V

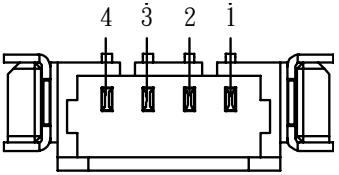
21	NC		
22	EDP_BKLTEN	OUT	+3.3V
23	EDP_HPD	IN	
24	GND	GND	
25	GND	GND	
26	GND	GND	
27	+12V	PWR	+12V
28	+12V	PWR	+12V
29	+12V	PWR	+12V
30	+12V	PWR	+12V

2.4.19 USB 2.0 Port 2 (CN20)



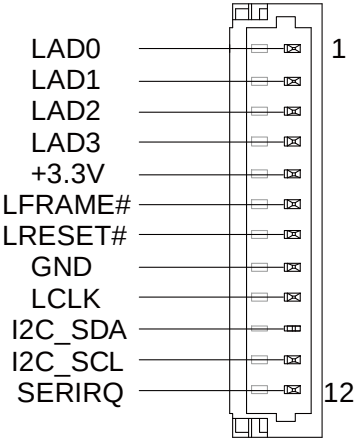
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	

2.4.20 USB 2.0 Port 1 (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	

2.4.21 LPC Port (CN22)



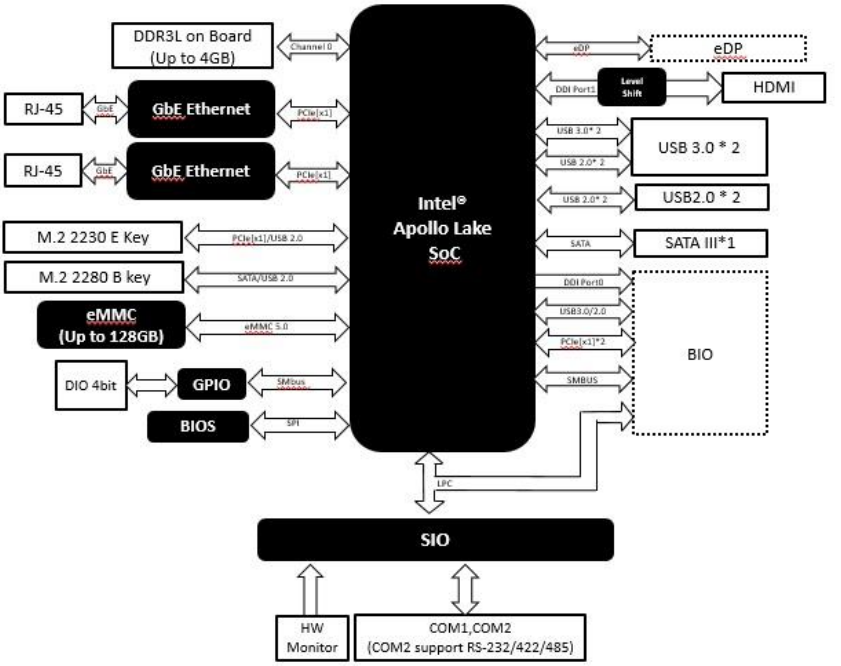
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V

5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	I2C0_SDA	I/O	+3.3V
11	I2C0_SCL	OUT	+3.3V
12	SERIRQ	I/O	+3.3V

2.5 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
COM Port 2	CN1	+5V/+12V	+5V/0.5A or +12V/0.5A
M.2 Key-E Slot (2230)	CN4	+3.3VSB	+3.3V/2A
M.2 Key-B Slot (2280)	CN5	+3.3V	+3.3V/2.5A
Digital IO Port	CN7	+5V	+5V/1A
+5V Output for SATA HDD	CN10	+5V	+5V/1A
USB Ports 0 and 1	CN15	+5VSB	+5V/1A (per channel)
USB 2.0 Ports 2	CN20	+5VSB	+5V/0.5A
USB 2.0 Ports 1	CN21	+5VSB	+5V/0.5A

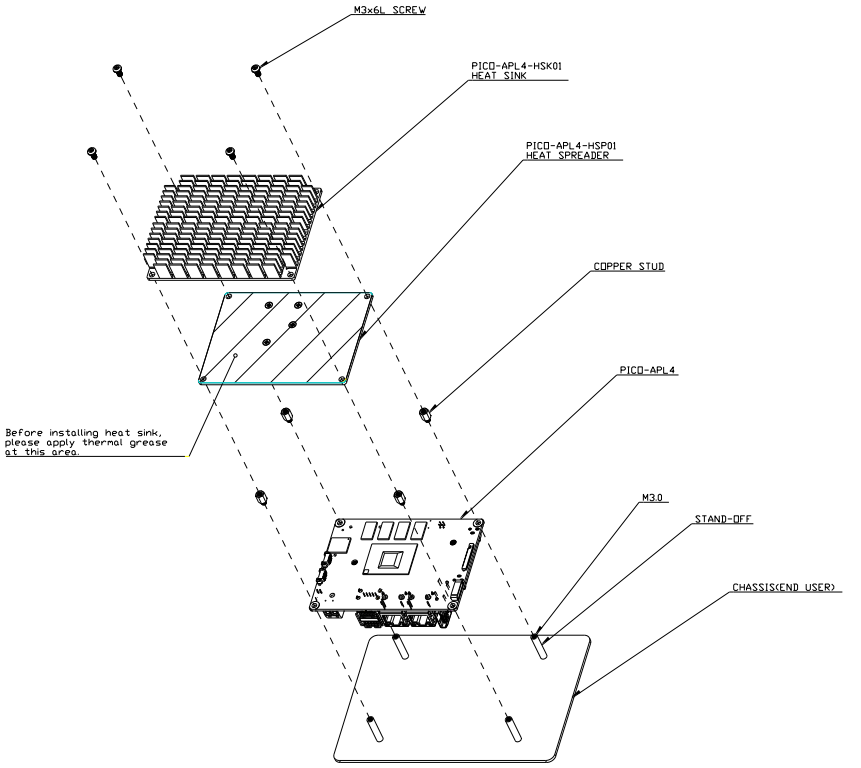
2.6 Function Block



2.7 Assembly Options

2.7.1 PICO-APL4-HSK01

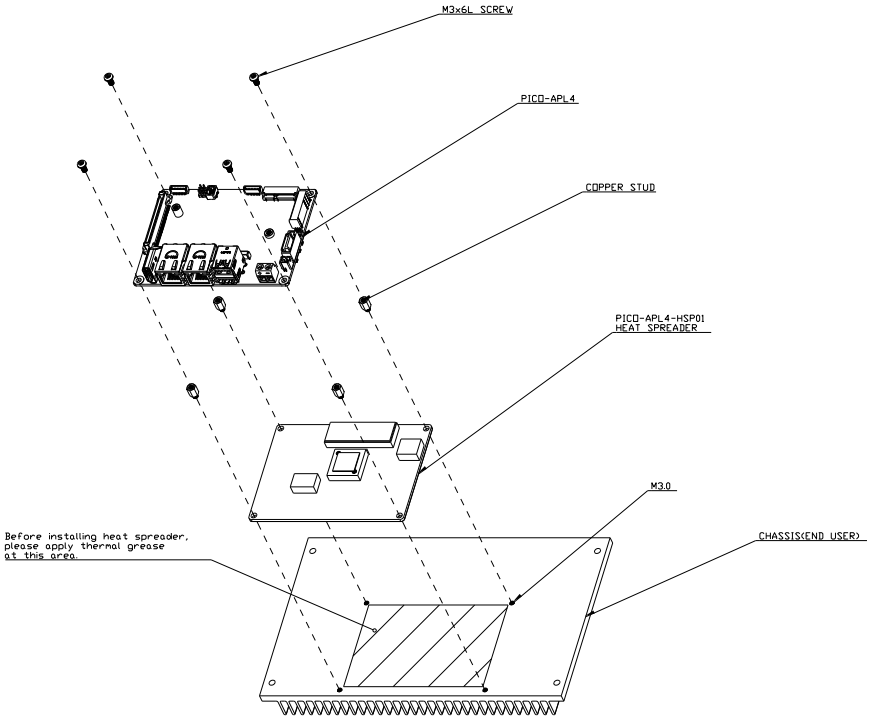
AAEON provides a heat spreader and a heatsink with both studs and screws included as options. We suggest the users have both for assembly.



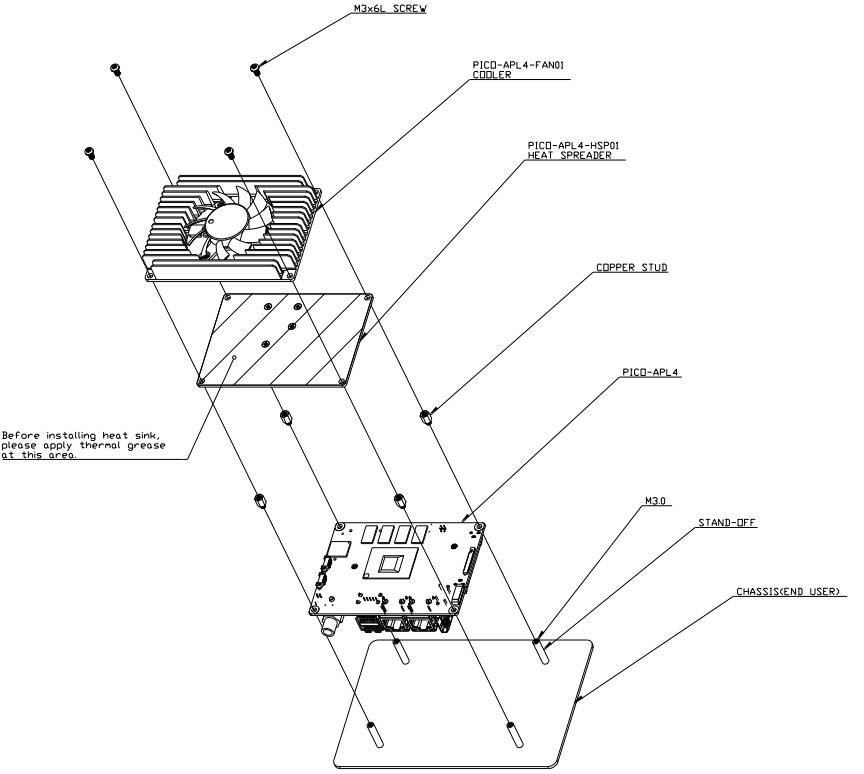
Note: AAEON suggests enabling a power limit in the BIOS setup for customers that prefer a passive cooling solution.

2.7.2 PICO-APL4-HSP01

If you only have AAEON's heat spreader and need to fix it on the chassis, please remember to put thermal grease between the chassis and heat spreader to maximize cooling efficiency.



2.7.3 PICO-APL4-FAN01



Note: The active cooling solution can be operated via +5V USB power from CN20 or CN21 without fan speed control.

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-APL4 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

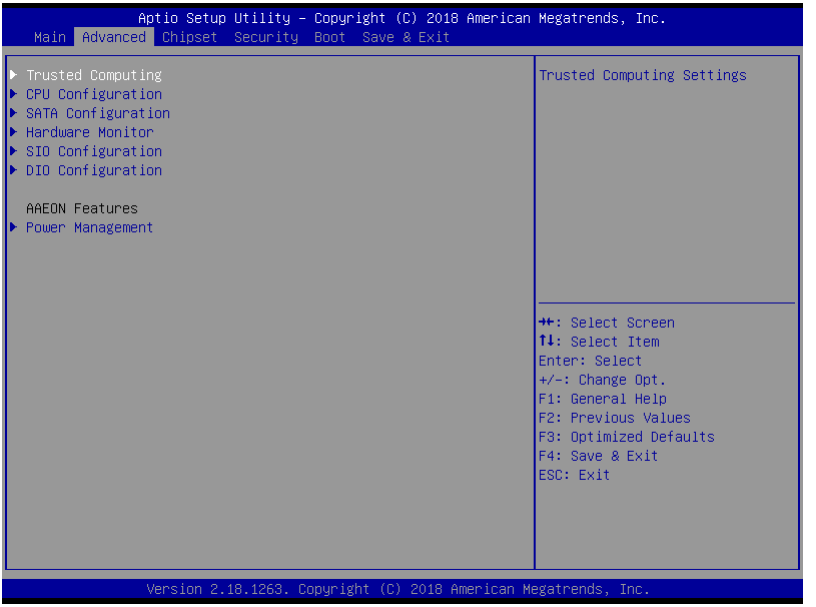
Set setup administrator password.

Save & Exit

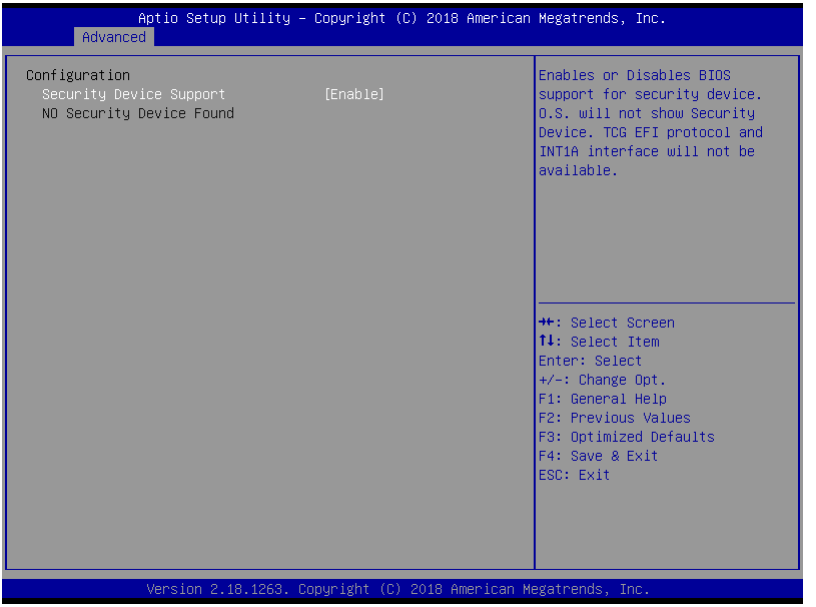
Exit system setup after saving the changes.

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



3.4.1 Trusted Computing

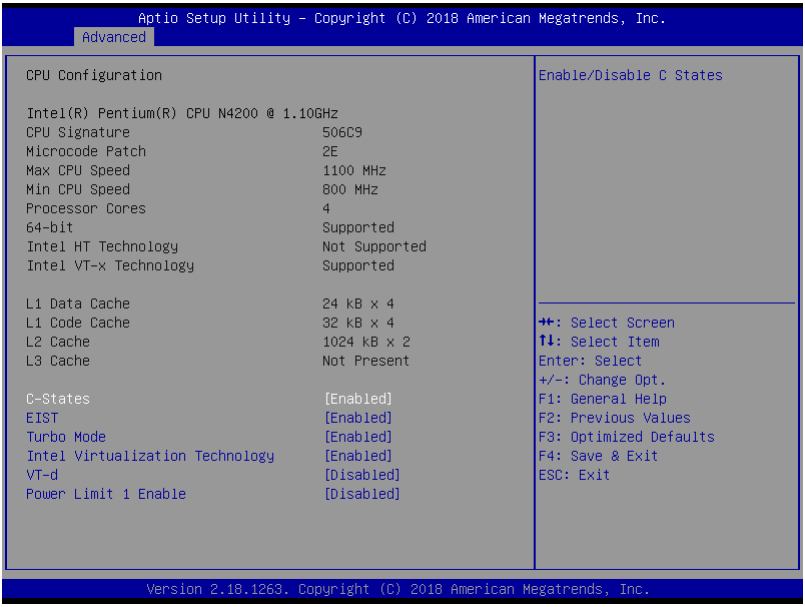


Options summary:

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.2 CPU Configuration

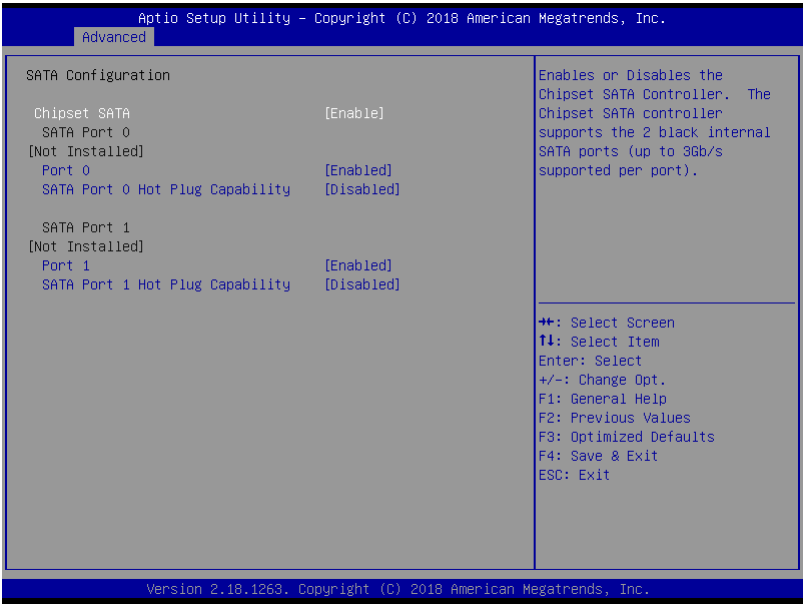


Options summary:

C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU VT-d		

Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1		

3.4.3 SATA Configuration

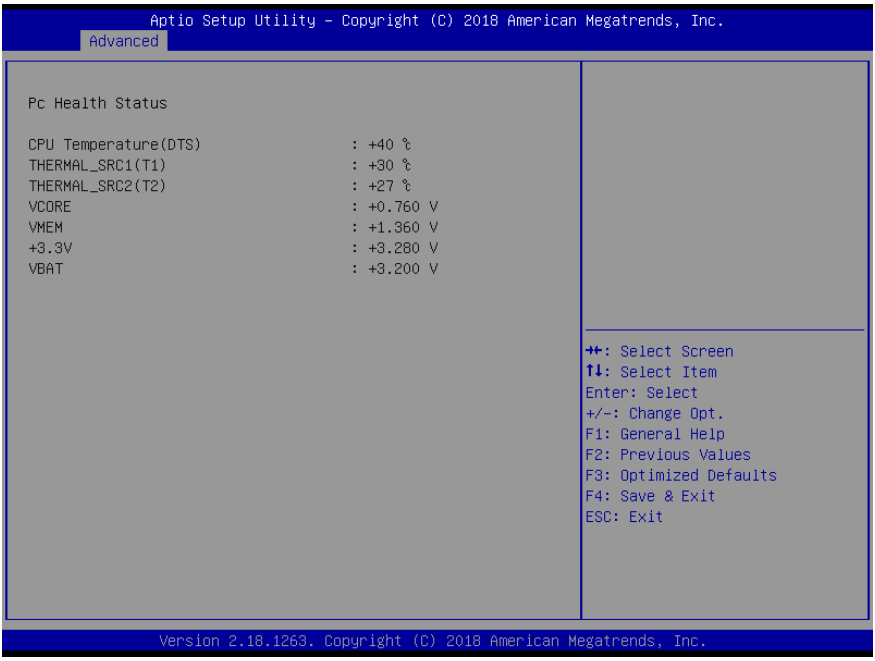


Options summary:

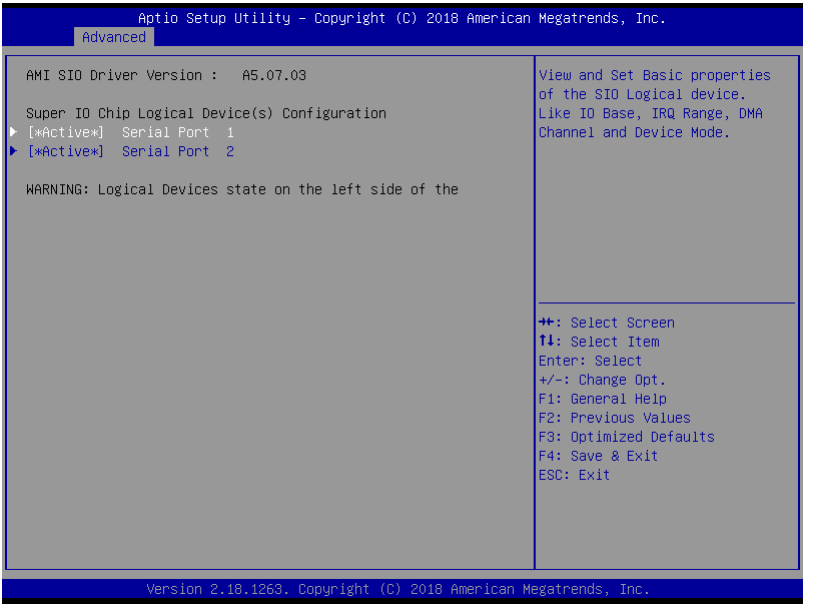
Chipset SATA	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

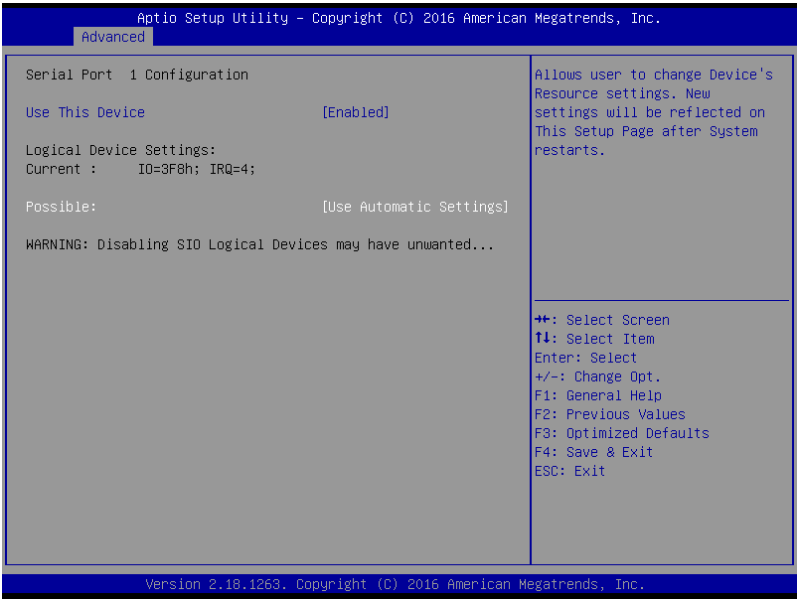
3.4.4 Hardware Monitor



3.4.5 SIO Configuration



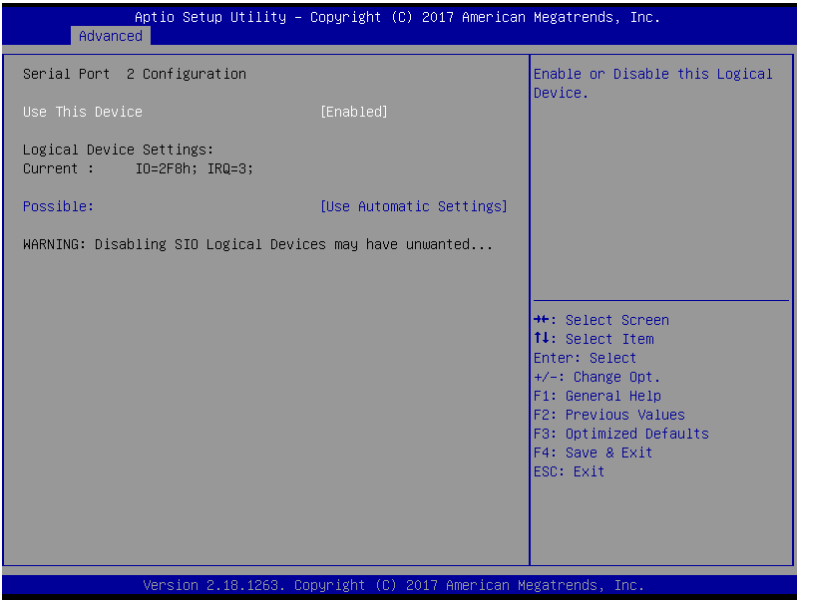
3.4.5.1 Serial Port 1 Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

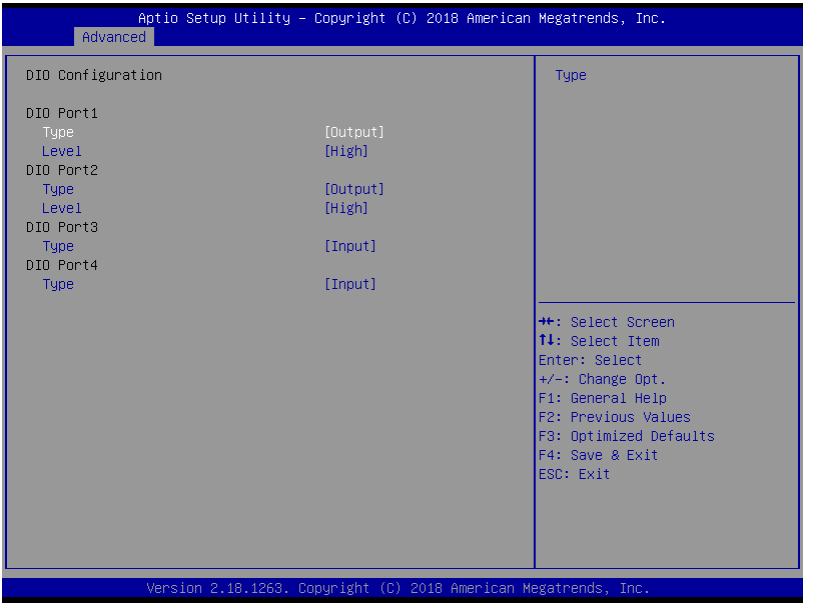
3.4.5.1 Serial Port 1 Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

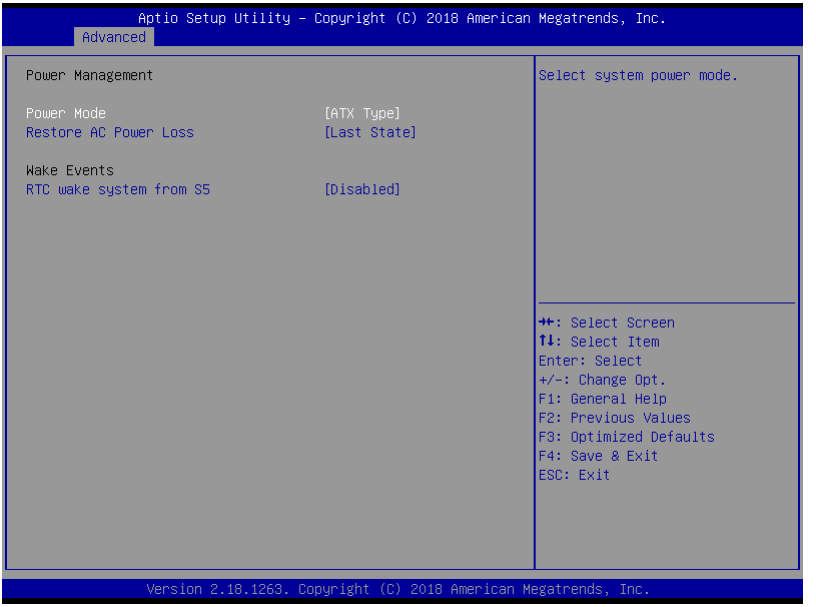
3.4.5 Digital IO Port Configuration



Options summary:

DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

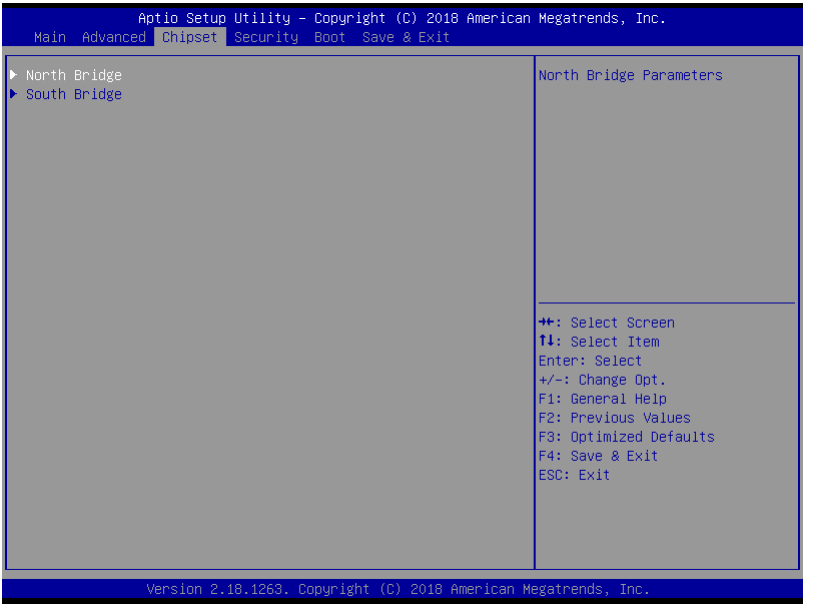
3.4.6 Power Management



Options summary:

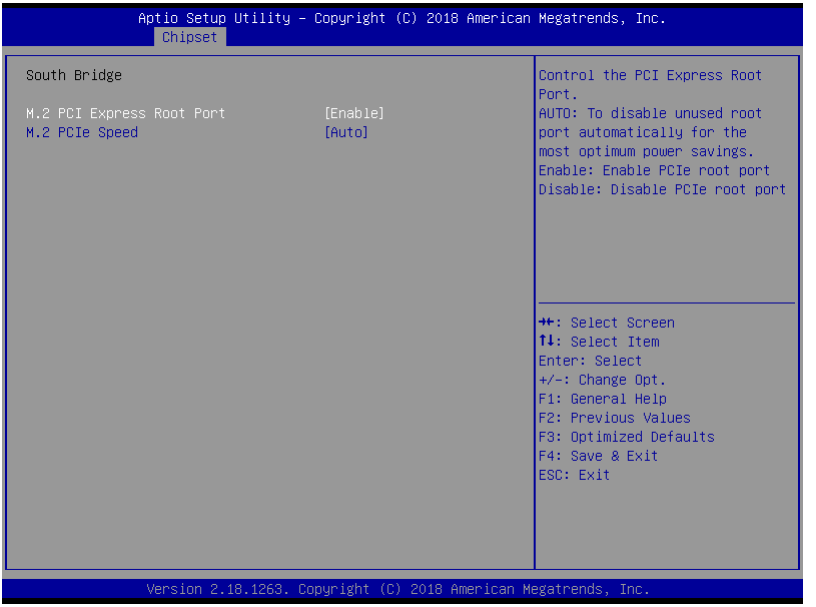
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
Fixed Time: System will wake on the hr::min::sec specified.		

3.5 Setup submenu: Chipset



3.5.1 North Bridge

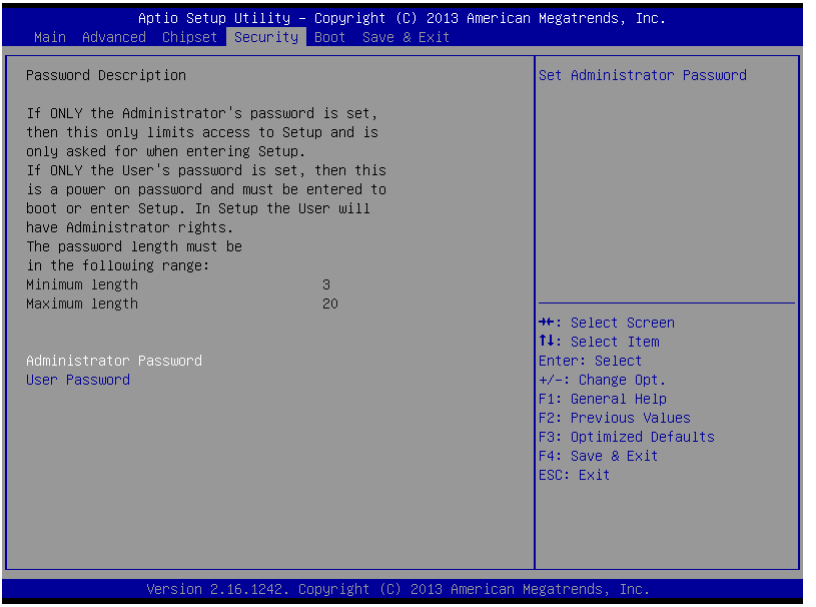
3.5.2 South Bridge



Options summary:

M.2 PCI Express Root Port	Disable	
	Enable	Optimal Default, Failsafe Default
	Auto	
Control the PCI Express Root Port. AUTO: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIe root port Disable: Disable PCIe root port		
M.2 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe Speed		

3.6 Setup submenu: Security



Change User/Supervisor Password

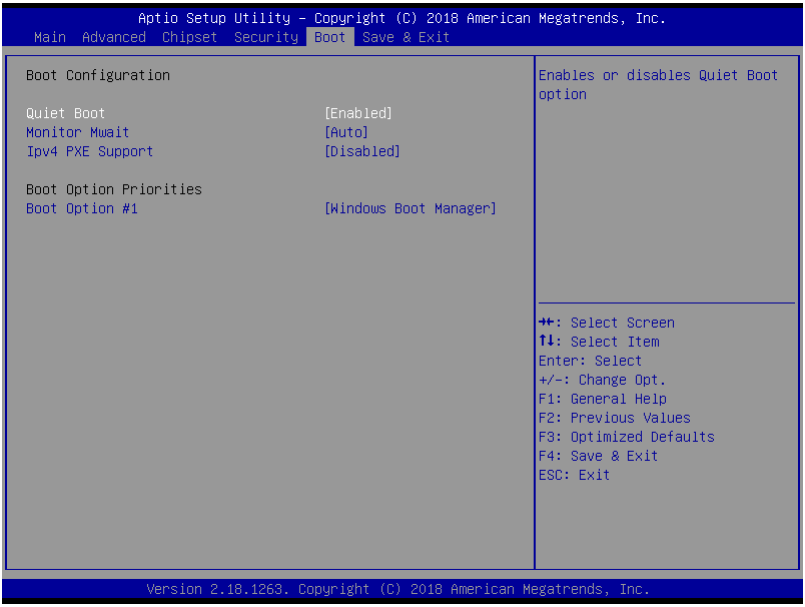
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

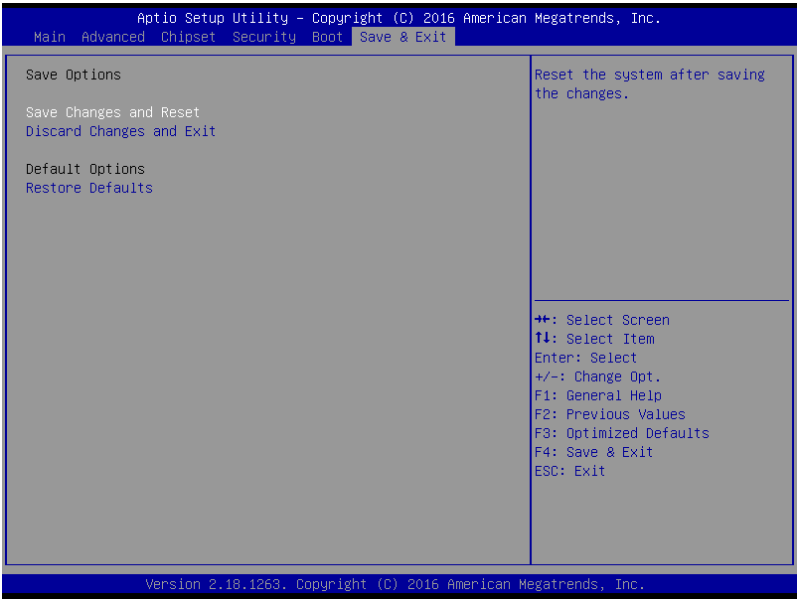
3.7 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
EnableDisable showing boot logo.		
Monitor Mwait	Disable	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the PICO-APL4 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/pico-itx-boards-pico-apl4#downloads

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Open the **STEP1 - CHIPSET** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **STEP2 - VGA** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 3 – Install LAN Driver

1. Open the **STEP3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Driver will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - AUDIO** folder and open the **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 5 – Install TXE Driver

1. Open the **STEP5 - TXE** folder and open the **SetupTXE.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 6 – Install FintekSerial_Patch_T4R8 Driver

1. Open the **STEP6-FintekSerial_Patch_T4R8** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 7 – Install GPIO Driver

1. Open the **STEP7 - GPIO** folder and open the **SetupSerialIO.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0x2E	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s *Pulse width is must longer then 16ms.*
Signal Polarity	0x05	2	0	0: low active 1: high active *Must set this bit to 0*
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse *Must set this bit to 1*
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
     #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
     #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
     #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
     #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
     #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
     #define   PolarityVal    0x00     // Low active for WDTRST#
     #define   UnitBit          0x03     // Unit for timer (Bit3)
     #define   ModeBit          0x04     // WDTRST# mode (Bit4)
     #define   ModeVal          0x01     // 0:level 1: pulse
     #define   EnableBit       0x05     // WDT timer enable (Bit5)
     #define   EnableVal       0x01     // 1: enable
     #define   StatusBit       0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*****************************************************************************

*****************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        EnterSIOconfig();
        SetWDT();
        AaeonWDTConfig(Counter, Unit);
        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
        ExitSIOconfig();
}
*****************************************************************************
```

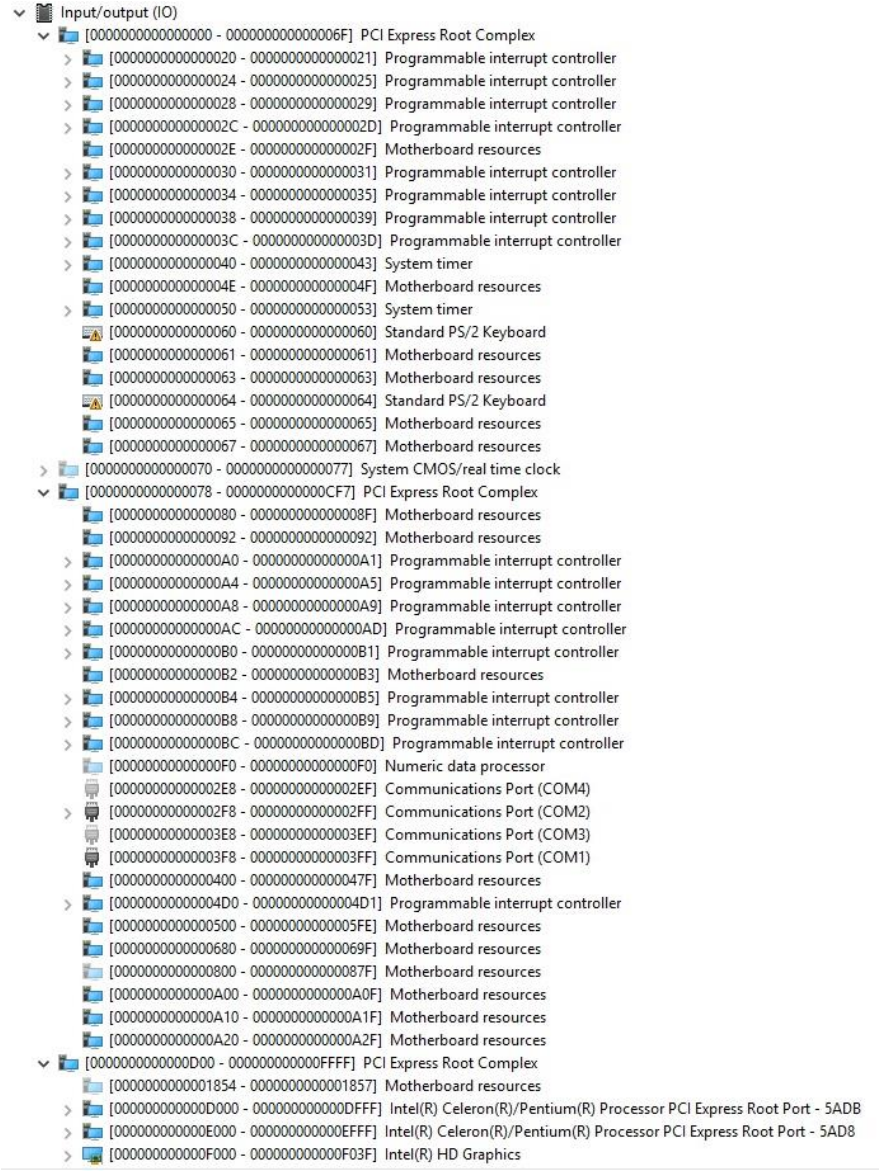
```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    EnterSIOconfig ( ){
          IOWriteByte (IoConfAddr,0x87);
          IOWriteByte (IoConfAddr,0x87);
}

VOID    ExitSIOconfig ( ){
          IOWriteByte (IoConfAddr,0xAA);
}

VOID    SetWDT ( )
          IOWriteByte (IoConfAddr,0x2B);
          IOWriteByte(IoConfAddr+1, (IOReadByte(IoConfAddr+1)&0xFC));
}

// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
          WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
          // Disable WDT counting
          WDTEnableDisable(0);
          // Clear Watchdog Timeout Status
          WDTClearTimeoutStatus();
          // WDT relative parameter setting
          WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
          If (Value == 1)
               WDTSetBit(TimerReg, EnableBit, 1);
          else
               WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
          // Watchdog Timer counter setting
          WDTWriteByte(CounterReg, Counter);
         // WDT counting unit setting
```

```
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
         // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
VOID   WDTWriteByte(byte Register, byte Value){
        IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
        return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
        byte TmpValue;

        TmpValue = WDTReadByte(Register);
        TmpValue &= ~(1 << Bit);
        TmpValue |= Val << Bit;
        WDTWriteByte(Register, TmpValue);
}

*****************************************************************************
```

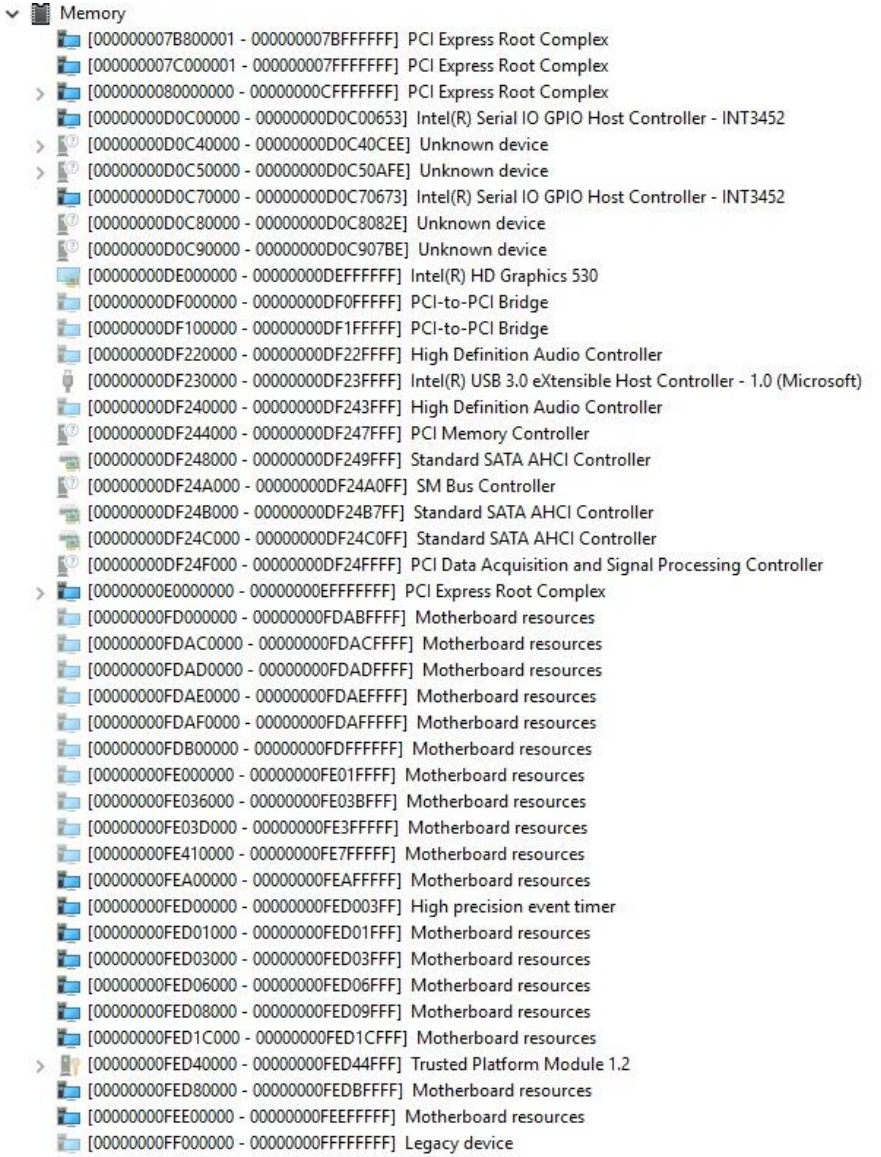
Appendix B

I/O Information

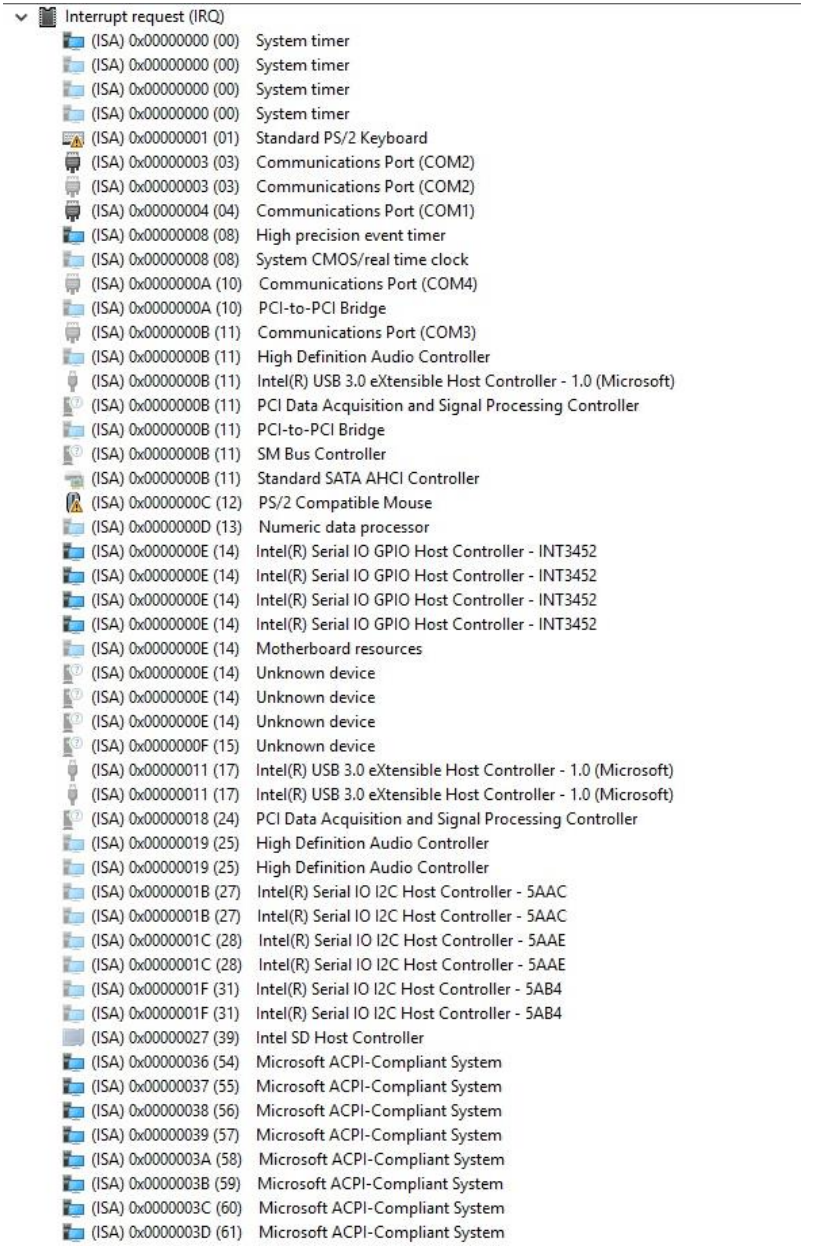
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



(ISA) 0x0000003E (62) Microsoft ACPI-Compliant System
(ISA) 0x0000003F (63) Microsoft ACPI-Compliant System
(ISA) 0x00000040 (64) Microsoft ACPI-Compliant System
(ISA) 0x00000041 (65) Microsoft ACPI-Compliant System
(ISA) 0x00000042 (66) Microsoft ACPI-Compliant System
(ISA) 0x00000043 (67) Microsoft ACPI-Compliant System
(ISA) 0x00000044 (68) Microsoft ACPI-Compliant System
(ISA) 0x00000045 (69) Microsoft ACPI-Compliant System
(ISA) 0x00000046 (70) Microsoft ACPI-Compliant System
(ISA) 0x00000047 (71) Microsoft ACPI-Compliant System
(ISA) 0x00000048 (72) Microsoft ACPI-Compliant System
(ISA) 0x00000049 (73) Microsoft ACPI-Compliant System
(ISA) 0x0000004A (74) Microsoft ACPI-Compliant System
(ISA) 0x0000004B (75) Microsoft ACPI-Compliant System
(ISA) 0x0000004C (76) Microsoft ACPI-Compliant System
(ISA) 0x0000004D (77) Microsoft ACPI-Compliant System
(ISA) 0x0000004E (78) Microsoft ACPI-Compliant System
(ISA) 0x0000004F (79) Microsoft ACPI-Compliant System
(ISA) 0x00000050 (80) Microsoft ACPI-Compliant System
(ISA) 0x00000051 (81) Microsoft ACPI-Compliant System
(ISA) 0x00000052 (82) Microsoft ACPI-Compliant System
(ISA) 0x00000053 (83) Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84) Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85) Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86) Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87) Microsoft ACPI-Compliant System
(ISA) 0x00000058 (88) Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89) Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90) Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91) Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103) Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System

(ISA) 0x000001DC (476) Microsoft ACPI-Compliant System
(ISA) 0x000001DD (477) Microsoft ACPI-Compliant System
(ISA) 0x000001DE (478) Microsoft ACPI-Compliant System
(ISA) 0x000001DF (479) Microsoft ACPI-Compliant System
(ISA) 0x000001E0 (480) Microsoft ACPI-Compliant System
(ISA) 0x000001E1 (481) Microsoft ACPI-Compliant System
(ISA) 0x000001E2 (482) Microsoft ACPI-Compliant System
(ISA) 0x000001E3 (483) Microsoft ACPI-Compliant System
(ISA) 0x000001E4 (484) Microsoft ACPI-Compliant System
(ISA) 0x000001E5 (485) Microsoft ACPI-Compliant System
(ISA) 0x000001E6 (486) Microsoft ACPI-Compliant System
(ISA) 0x000001E7 (487) Microsoft ACPI-Compliant System
(ISA) 0x000001E8 (488) Microsoft ACPI-Compliant System
(ISA) 0x000001E9 (489) Microsoft ACPI-Compliant System
(ISA) 0x000001EA (490) Microsoft ACPI-Compliant System
(ISA) 0x000001EB (491) Microsoft ACPI-Compliant System
(ISA) 0x000001EC (492) Microsoft ACPI-Compliant System
(ISA) 0x000001ED (493) Microsoft ACPI-Compliant System
(ISA) 0x000001EE (494) Microsoft ACPI-Compliant System
(ISA) 0x000001EF (495) Microsoft ACPI-Compliant System
(ISA) 0x000001F0 (496) Microsoft ACPI-Compliant System
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000019 (25) High Definition Audio Controller
(PCI) 0x00000027 (39) Intel SD Host Controller
(PCI) 0xFFFFFFF3 (-13) Intel(R) HD Graphics
(PCI) 0xFFFFFFF4 (-12) Realtek PCIe GBE Family Controller #4
(PCI) 0xFFFFFFF5 (-11) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFF6 (-10) Realtek PCIe GBE Family Controller #2
(PCI) 0xFFFFFFF7 (-9) Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFF8 (-8) Standard SATA AHCI Controller
(PCI) 0xFFFFFFF9 (-7) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD7
(PCI) 0xFFFFFFFA (-6) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD6
(PCI) 0xFFFFFFFB (-5) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
(PCI) 0xFFFFFFFC (-4) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
(PCI) 0xFFFFFFFD (-3) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
(PCI) 0xFFFFFFFE (-2) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8

Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	COM Port #2 Connector	JST	SHR-09V-S-B	Serial Port Cable	1701090122
CN2	COM Port #1 Connector	JST	SHR-09V-S-B	Serial Port Cable	1701090122
CN3	Front Panel Connector	JCTC	11002H00-5*2P	N/A	N/A
CN7	Digital I/O Connector	Harwin	M50-3000345	N/A	N/A
CN8	SATA Connector	Molex	887505318	SATA Cable	1709070500
CN10	+5Vout Connector	JST	PHR-2	2 Pins For SATA HDD Power	1702150155
CN12	External RTC Connector	Molex	51021-0200	Battery Cable	175011301C
CN17	Power Input Connector	Molex	19211-0003	Power Cable	170204010R
CN19	Embedded DisplayPort Connector	I-PEX	20453-030T	N/A	N/A
CN20	USB Port #2 Connector	Molex	51021-0400	USB Cable	1700040151
CN21	USB Port #1	Molex	51021-0400	USB Cable	1700040151

	Connector				
CN22	LPC Connector	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130

Appendix D

DIO

D.1 DIO

The PICO-APL4 provides one serial access interface, I2C Bus, to read/write internal registers. The address of Serial Bus is 0x6E (0110_1110)

The related register for configuring DIO is list as follows:

Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	Reserved	R/W	VSB3V	
5	EN_WDT10	R/W	VSB3V	Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable.
4	Reserved	R/W	VSB3V	
3	Reserved	R/W	VSB3V	
2	Reserved	R/W	VSB3V	
1	SMART_POWR_MANAGEMENT	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

GPIO2x Output Control Register – Index 20h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_OCTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function(default).
6	GP26_OCTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function(default).
5	GP25_OCTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function(default).
4	GP24_OCTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function(default).

GPIO2x Output Data Register – Index 21h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_ODATA	R/W	VSB3V	GPIO 27 output data.
6	GP26_ODATA	R/W	VSB3V	GPIO 26 output data.
5	GP25_ODATA	R/W	VSB3V	GPIO 25 output data.
4	GP24_ODATA	R/W	VSB3V	GPIO 24 output data.

GPIO2x Input Status Register – Index 22h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7	GP27_PSTS	RO	VSB3V	Read the GPIO27 data on the pin.
6	GP26_PSTS	RO	VSB3V	Read the GPIO26 data on the pin.
5	GP25_PSTS	RO	VSB3V	Read the GPIO25 data on the pin.
4	GP24_PSTS	RO	VSB3V	Read the GPIO24 data on the pin.

The following is a sample code for 8 input

```
.MODEL SMALL
.CODE
begin:
mov cl,01h
mov al,80h
call CT_I2CWriteByte
call Delay5ms

        mov al,00h
mov cl,20h
call CT_I2CWriteByte

mov cl,22h
call CT_I2CReadByte

;Input : CL - register index
```

```
; CH - device ID
;Output : AL - Value read
Ct_I2CReadByte Proc Near
mov ch,06eh
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
inc ch ; Set the slave address and
mov al, ch ; prepare for a READ command
out dx, al
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to read
out dx, al
mov dx, F040h + 06h

xor al, al ; Clear old data
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
out dx, al

mov dx, F040h + 00h ; Host Control Reegister
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready
mov dx, F040h + 06h
```

```
in al, dx

ret
Ct_I2CReadByte Endp
;Input : CL - register index
; CH - device ID
; AL - Value to write
;Output: none

Ct_I2CWriteByte Proc Near
mov ch,06eh

xchg ah, al
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
mov al, ch ; Set the slave address and
out dx, al ; prepare for a WRITE command
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to write
out dx, al
mov dx, F040h + 06h
mov al, ah
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
```

```
out dx, al
mov dx, F040h + 00h ; Host Control Register
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready ;R14
ret
Ct_I2CWriteByte Endp
; Wait until the busy bit clears, indicating that the SMBUS
; activity has concluded.
CT_Chk_SMBus_Ready Proc Near
mov dx, F040h + 01h ; Host Status Register
Check_I2C_ByteRead_ForBusy:
in al, dx
test al, 08h
jnz Check_I2C_ByteRead_ForBusy
Check_I2C_ByteRead_ForStatus:
in al, dx
test al, 07h ; HSTS[2:0]=All clearable status bits
jz Check_I2C_ByteRead_ForStatus
ret
CT_Chk_SMBus_Ready Endp
END begin
```