PICO-APL3-SEMI

PICO-SEMI System

User's Manual 1st Ed

Last Updated: June 4, 2018

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-APL3 (MB)	1
● Chassis (major parts)	1
● Bottom Cover of the Chassis	1
● Accessory Kits (with Power Button)	1
● Product DVD with Drivers and Manual	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

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Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	PICO-ITX
Processor	Intel® Pentium® Processor N4200 Intel® Celeron® Processor N3350
System Memory	Onboard DDR3L 2GB/4GB
Chipset	Intel® Pentium® N4200 / Celeron® N3350 integrated
BIOS	AMI / SPI
Wake On LAN	Yes
Watchdog Timer	255 levels
Power Requirement	+ 12 V, AT/ATX
Power Supply Type	Lockable
System Cooling	Without Heatsink
Board Size	100 x 72 mm (3.94 x 2.84")
Gross Weight	420g
Operating Temperature	32˚F ~ 122˚F (0˚C ~ 50˚C), 0.5m/s air flow
Storage Temperature	-40 ~ 80°C (-40 ~176°F)
Operation Humidity	0 ~ 90% relative humidity, non-condensing
Anti-Vibration	Radom 5~500 Hz, 2G rms - eMMC
EMC	CE/FCC Class A

Display

Chipset	Intel® Pentium® N4200 / Celeron® N3350 integrated graphic
Resolution	HDMI: 3840x2160@30Hz

I/O

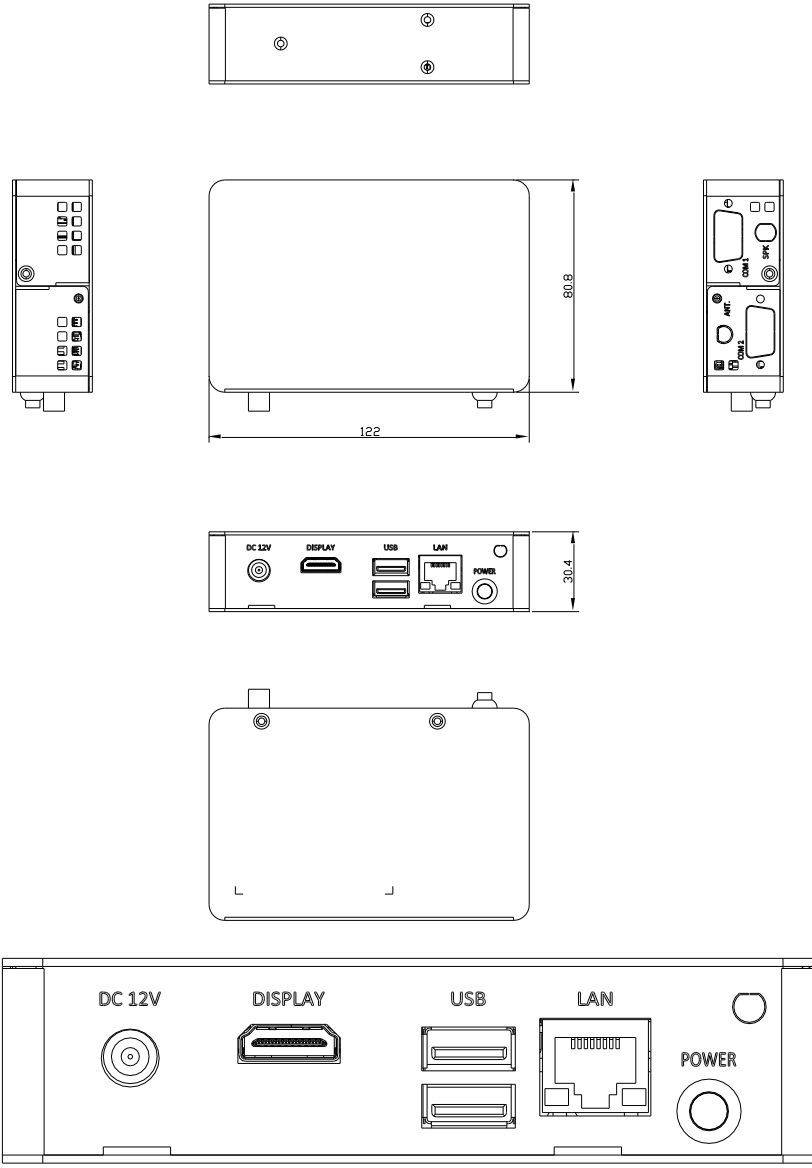
Storage	SATA III 6.0Gb/s x 1, 5V/12V Power reserved M.2 2280 (B Key) x 1 eMMC 16/32/64/128GB
Ethernet	Realtek 8111G x 1, 10/100/1000 Base-TX
USB	USB 3.0 x 2 Rear IO
Serial Port	COM1: RS-232 (Optional) COM2: RS-232 (Optional)
Audio	ALC269 (Included Amp, Optional)
DI/O	4-bit programmable (2-in/ 2-out)
Expansion Slot	M.2 2230 x 1 (E-Key)
TPM	x 1 (Optional)

Chapter 2

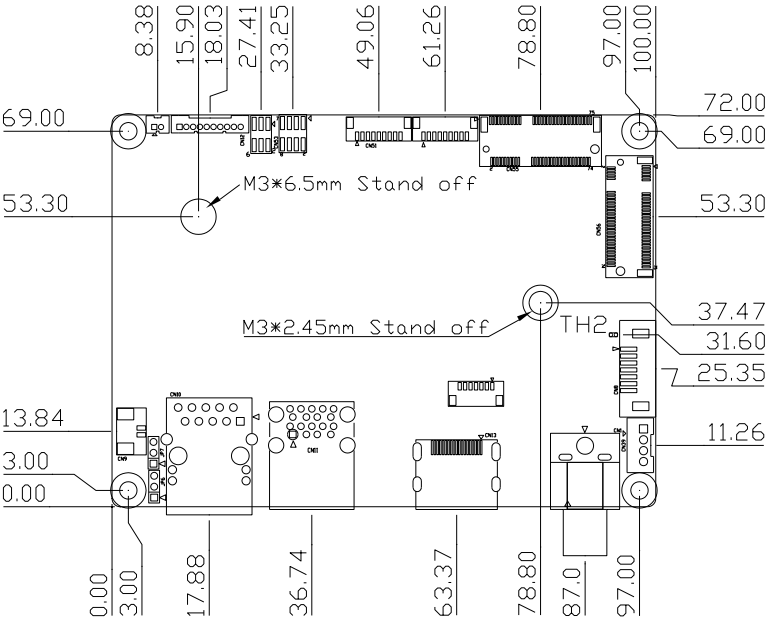
Hardware Information

2.1 Dimensions

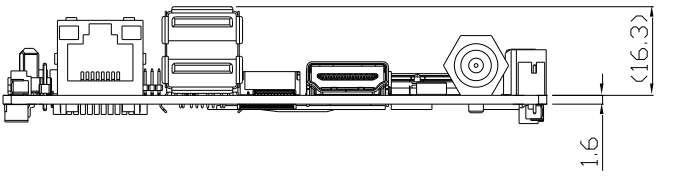
System



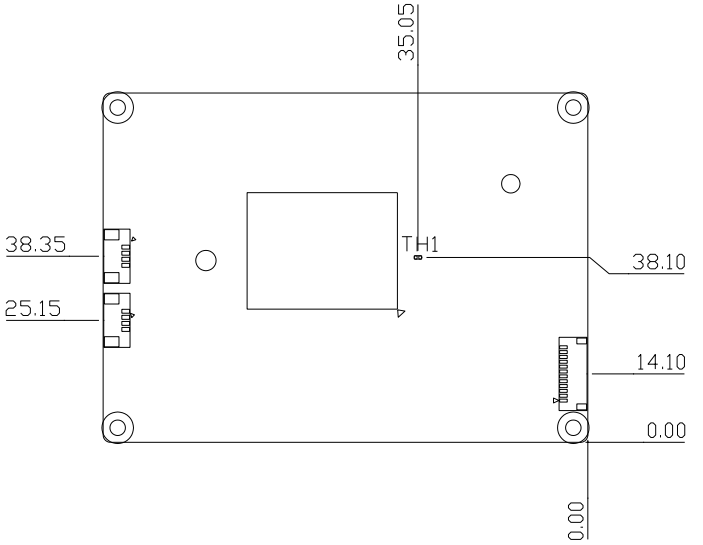
Board



Component Side



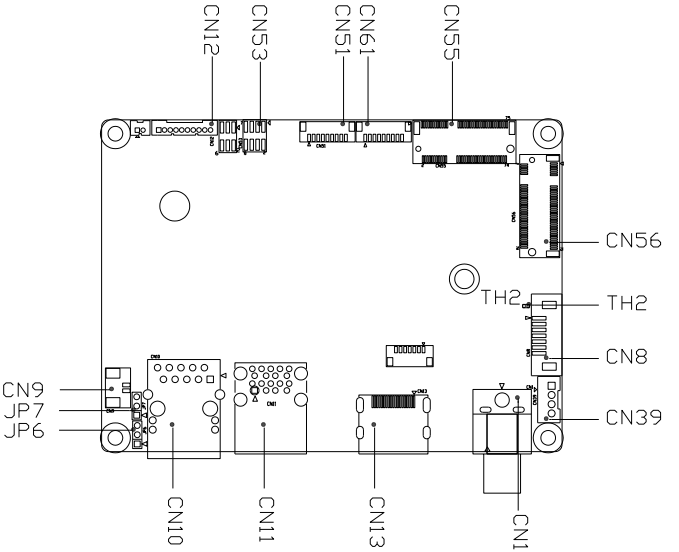
Solder Side



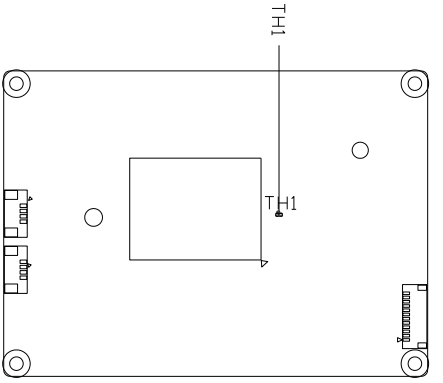
Solder Side

2.2 Jumpers and Connectors

Component Side



Solder Side

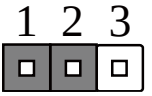


2.3 List of Jumpers

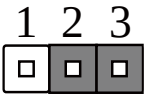
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP6	Auto Power Button Enable/Disable Selection
JP7	Clear CMOS Jumper

2.3.1 Auto Power Button Enable/Disable Selection (JP6)



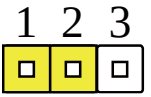
Disable



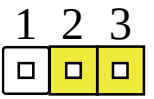
Enable (Default)

Disable Auto Power Button JP6 (1-2): Need to use power button JP6(1-2) to power on the system.

2.3.2 Clear CMOS Jumper (JP7)



Normal (Default)



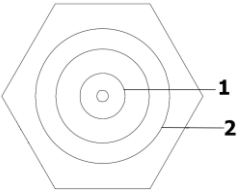
Clear CMOS

2.4 List of Connectors

Connectors on the board access links to external devices such as hard disk drives or a keyboard.

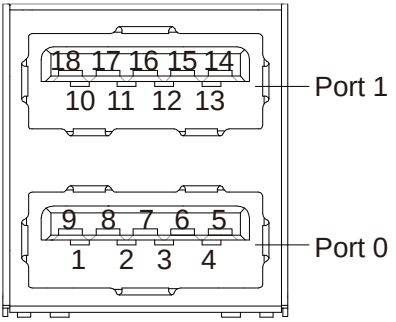
Label	Function
CN1	DC Jack
CN11	USB 3.0 Ports 0 and 1
CN9	RTC Battery
CN10	LAN (RJ-45)
CN55	M.2 E-key 2230
CN8	SATA Port
CN39	SATA PWR
CN56	M.2 B-Key 2280
CN12	Line In/ Line out/ Mic In
CN13	HDMI Port
CN53	Front Panel Header
CN51	COM port (RS-232)
CN61	COM port (RS-232)

2.4.1 External +12V Input (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	

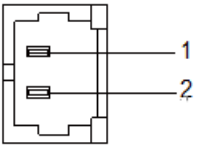
2.4.2 USB Ports 0 and 1 (CN11)



Pin	Pin Name	Signal Type	Signal Level
1	+5VA	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	

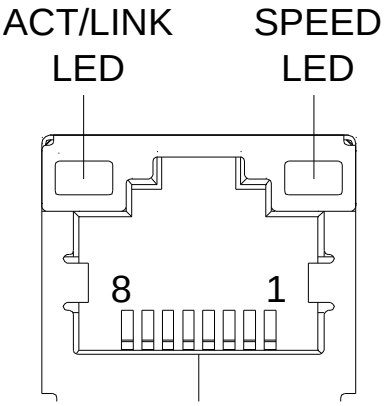
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VA	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−		
15	USB1_SSRX+		
16	GND	GND	
17	USB1_SSTX−		
18	USB1_SSTX+		

2.4.3 RTC Battery (CN9)



Pin	Pin Name	Signal Type	Signal Level
1	+BAT_RTC	PWR	3.3V
2	GND	GND	

2.4.4 LAN (RJ-45) (CN10)



Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.5 M.2 E Key (2230) (CN55)

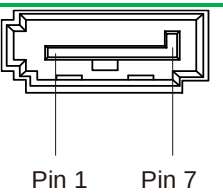
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+3.3VA	PWR	3.3V
3	USB+	DIFF	
4	+3.3VA	PWR	3.3V
5	USB-	DIFF	
6			
7	GND	GND	
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			

Pin	Pin Name	Signal Type	Signal Level
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			
33	GND	GND	
34			
35	PCIE_TXP	DIFF	
36			
37	PCIE_TXN	DIFF	
38			
39	GND	GND	
40			

Pin	Pin Name	Signal Type	Signal Level
41	PCIE_RXP	DIFF	
42			
43	PCIE_RXN	DIFF	
44			
45	GND	GND	
46			
47	CLK_PCIE_P	DIFF	
48			
49	CLK_PCIE_N	DIFF	
50			
51	GND	GND	
52	RST#	OUT	
53	PCIE_CLKREQ#	IN	
54	BT_DISABLE#	OUT	
55	PCIE_WAKE#	IN	
56	WIFI_DISABLE#	OUT	
57	GND	GND	
58			
59			
60			
61			

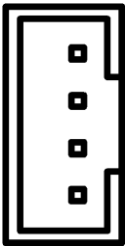
Pin	Pin Name	Signal Type	Signal Level
62			
63	GND	GND	
64			
65			
66			
67			
68			
69	GND	GND	
70			
71			
72	+3.3VA	PWR	3.3V
73			
74	+3.3VA	PWR	3.3V
75	GND	GND	

2.4.6 SATA Port (CN8)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX-	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.7 SATA Power (CN39)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	
3	GND	GND	
4	+5V	PWR	+5V

2.4.8 M.2 B-key (2280) (CN56)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+3.3V	PWR	3.3V
3	GND	GND	
4	+3.3V	PWR	3.3V
5	GND	GND	
6			
7	USB_DP	DIFF	
8			

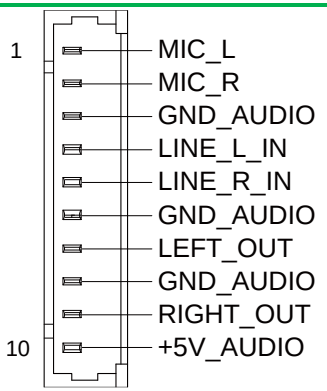
Pin	Pin Name	Signal Type	Signal Level
9	USB_DN	DIFF	
10	DAS	IN	3.3V
11	GND	GND	
12			
13			
14			
15			
16			
17			
18			
19			
20			
21	GND	GND	
22			
23			
24			
25			
26			
27			
28			
29	USB3_RX_N	Diff	

Pin	Pin Name	Signal Type	Signal Level
	(Reserved)		
30			
31	USB3_RX_P (Reserved)	Diff	
32			
33	GND	GND	
34			
35	USB3_TX_N (Reserved)	Diff	
36			
37	USB3_TX_P (Reserved)	Diff	
38			
39	GND	GND	
40			
41	SATA_RXP	DIFF	
42			
43	SATA_RXN	DIFF	
44			
45	GND	GND	
46			
47	SATA_TXN	DIFF	

Pin	Pin Name	Signal Type	Signal Level
48			
49	SATA_TXP	DIFF	
50			
51	GND	GND	
52			
53			
54			
55			
56			
57	GND	GND	
58			
59			
60			
61			
62			
63			
64			
65			
66			
67			
68			

Pin	Pin Name	Signal Type	Signal Level
69	GND	GND	
70	+3.3V	PWR	3.3V
71	GND	GND	
72	+3.3V	PWR	3.3V
73	GND	GND	
74	+3.3V	PWR	3.3V
75	GND	GND	

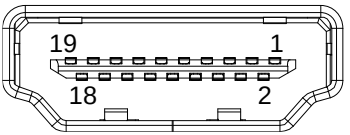
2.4.9 Audio I/O Port (C12)



Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	Audio	
2	MIC_R	Audio	
3	GND_AUDIO	AGND	
4	LINE_L_IN	Audio	
5	LINE_R_IN	Audio	

Pin	Pin Name	Signal Type	Signal Level
6	GND_AUDIO	AGND	
7	LEFT_OUT	Audio	
8	GND_AUDIO	AGND	
9	RIGHT_OUT	Audio	
10	+5V	PWR	

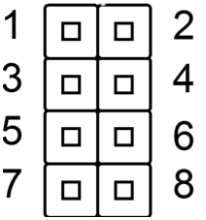
2.4.10 HDMI Port (CN13)



Pin	Pin Name	Signal Type	Signal Level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	

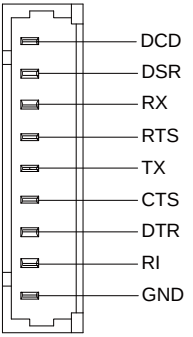
Pin	Pin Name	Signal Type	Signal Level
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.4.11 Front Panel Header (CN53)



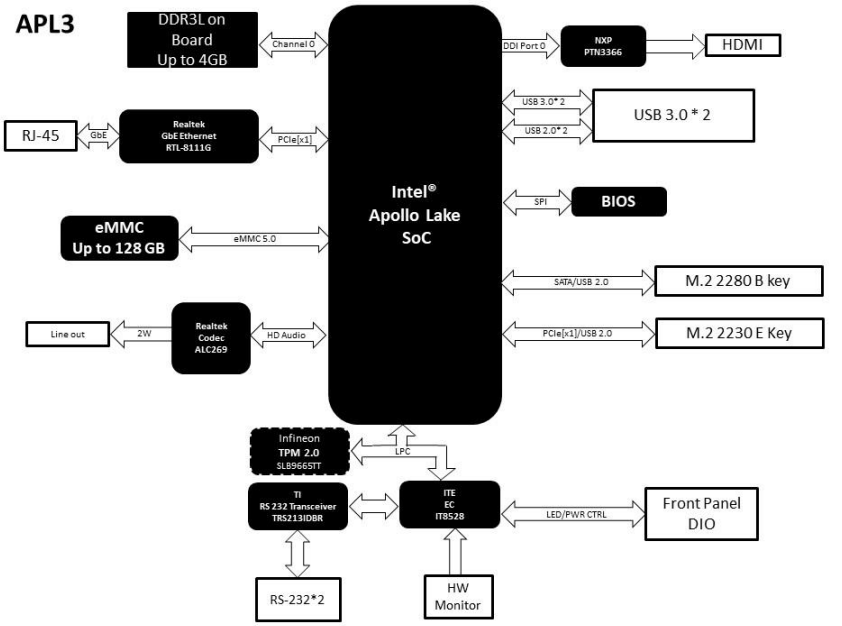
Pin 1	GND	Pin 2	PWR Button
Pin 3	FP_IDELED#	Pin 4	+3.3V
Pin 5	FP_BUZZER	Pin 6	+5V
Pin 7	GND	Pin 8	RESET Button

2.4.12 COM Port (CN51, CN61)



Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	
5	TX	OUT	
6	CTS	IN	
7	DTR	OUT	
8	RI	IN/ PWR	
9	GND	GND	

2.5 Block Diagram



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-APL3 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

Set setup administrator password.

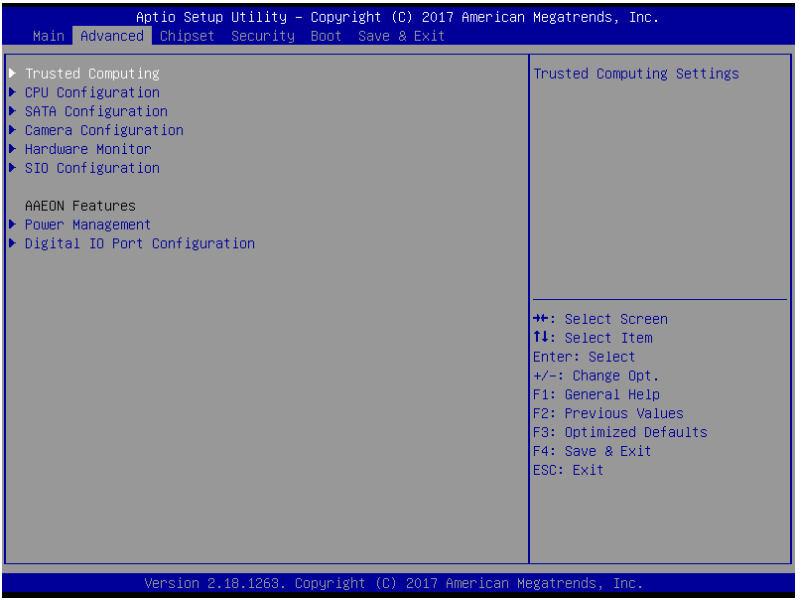
Save & Exit

Exit system setup after saving the changes.

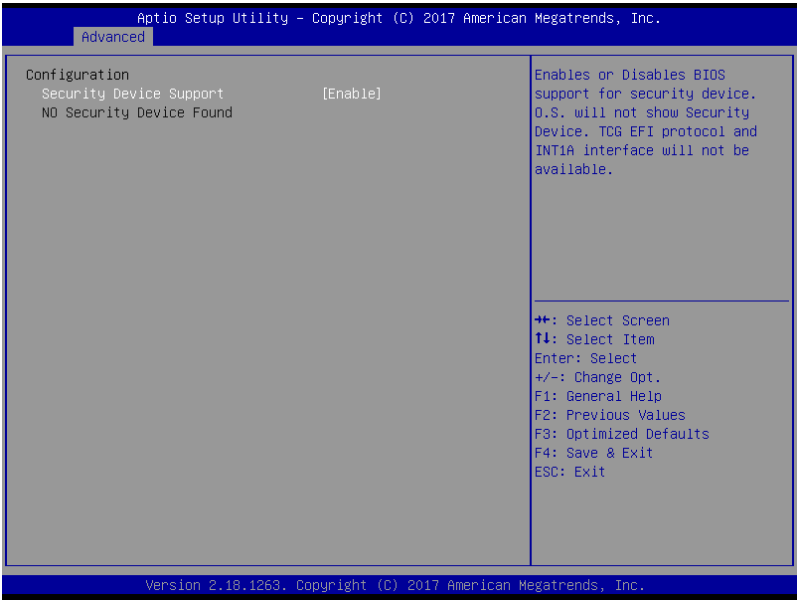
3.3 Setup Submenu: Main

Press "Delete" to enter Setup

3.4 Setup Submenu: Advanced



3.4.1 Trusted Computing

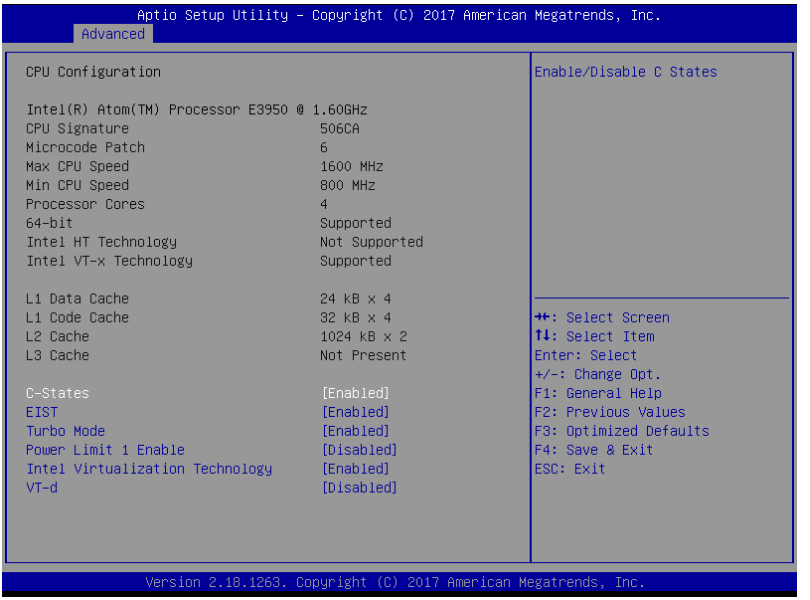


Options summary:

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		
Platform Hierarchy	Disabled	

	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.2 CPU configuration



Options summary:

C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode		
Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		

VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU VT-d		

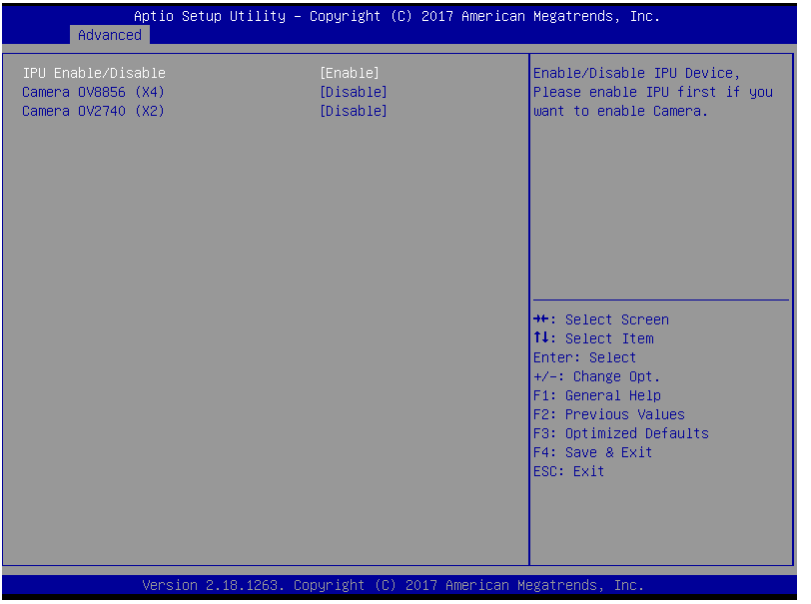
3.4.3 SATA Configuration

Options summary:

Chipset SATA	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		
Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

Port 0/1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA port		

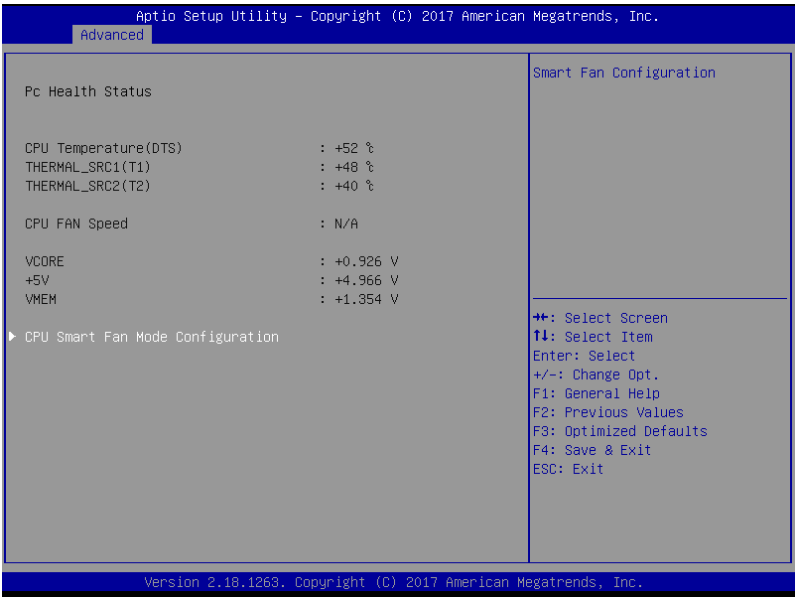
3.4.4 Camera Configuration (Optional)



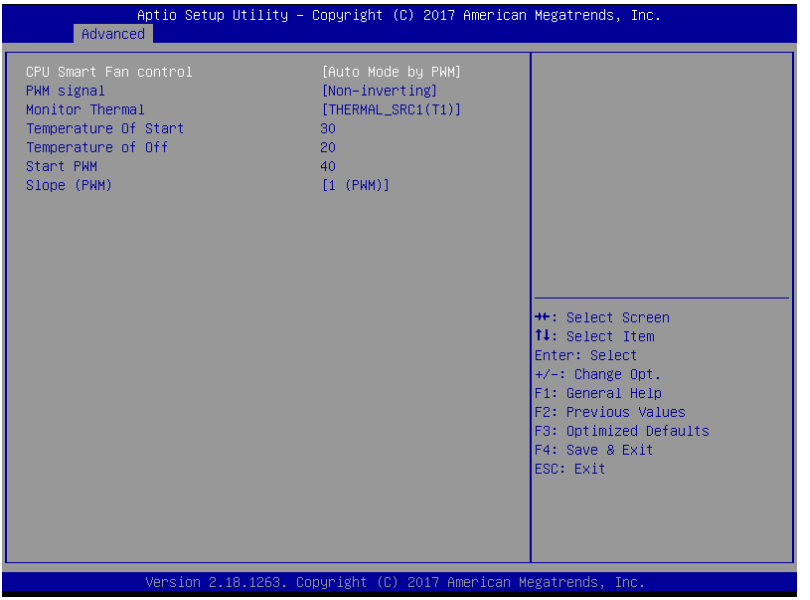
Options summary:

IPU Enable/Disable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable IPU Device, Please enable IPU first if you want to enable Camera.		
Camera OV8856(X4)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Camera OV8856		
Camera OV8856(X2)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Camera OV2740		

3.4.5 Hardware Monitor



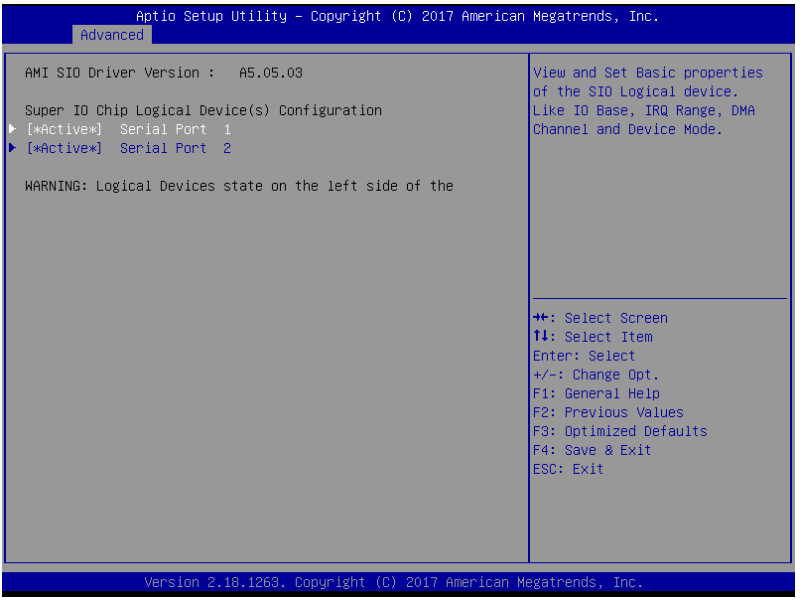
3.4.5.1 CPU Smart Fan Mode Configuration



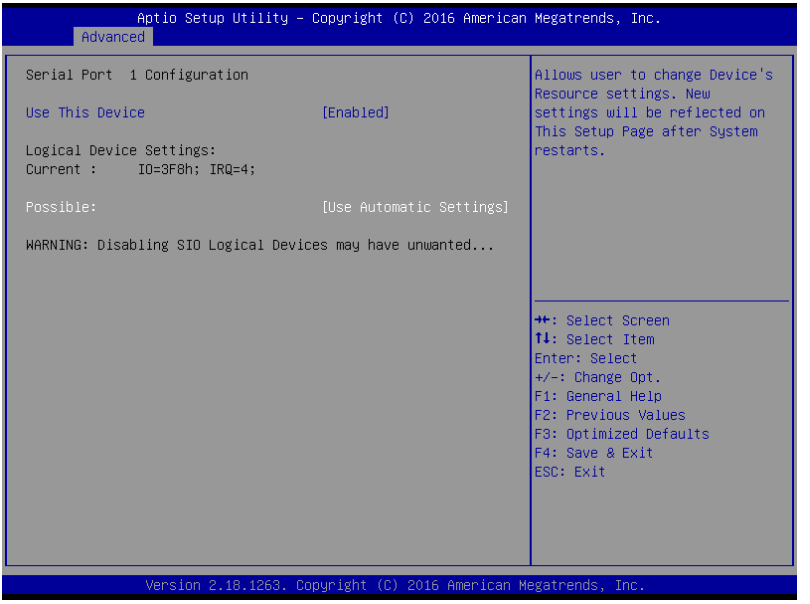
Options summary:

CPU Smart Fan Control	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
PWM signal	Non-inverting	
	Inverting	Optimal Default, Failsafe Default
Select output PWM of inverting or non-inverting signal		
Monitor Thermal	THERMAL_SRC1(T1)	Optimal Default, Failsafe Default
	THERMAL_SRC2(T2)	
Select monitor thermal source		
Temperature of Start	30	Optimal Default, Failsafe Default
Temperature Of Start		
Temperature of Off	20	Optimal Default, Failsafe Default
Temperature Of Off		
Start of PWM	40	Optimal Default, Failsafe Default
Start PWM		
Slope (PWM)	1 (PWM)	Optimal Default, Failsafe Default
Slope (PWM)		

3.4.6 SIO Configuration



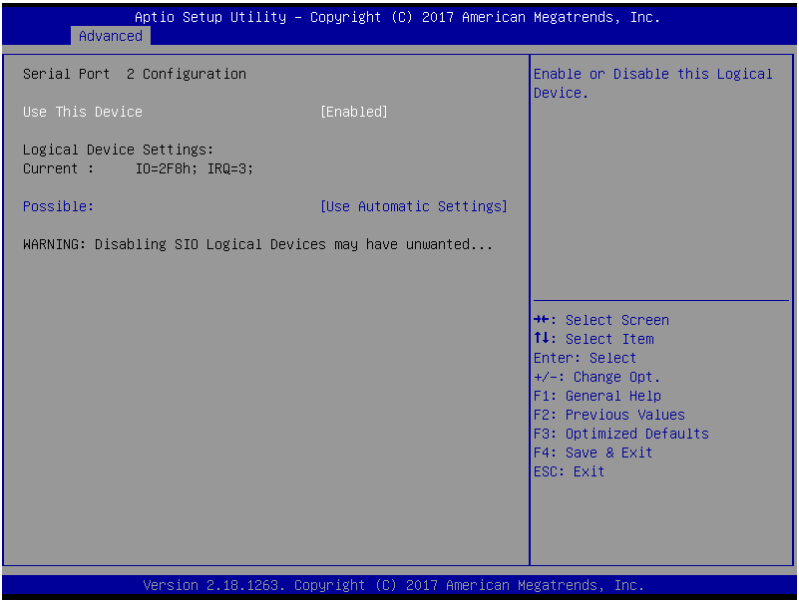
3.4.6.1 Serial Port 1 Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

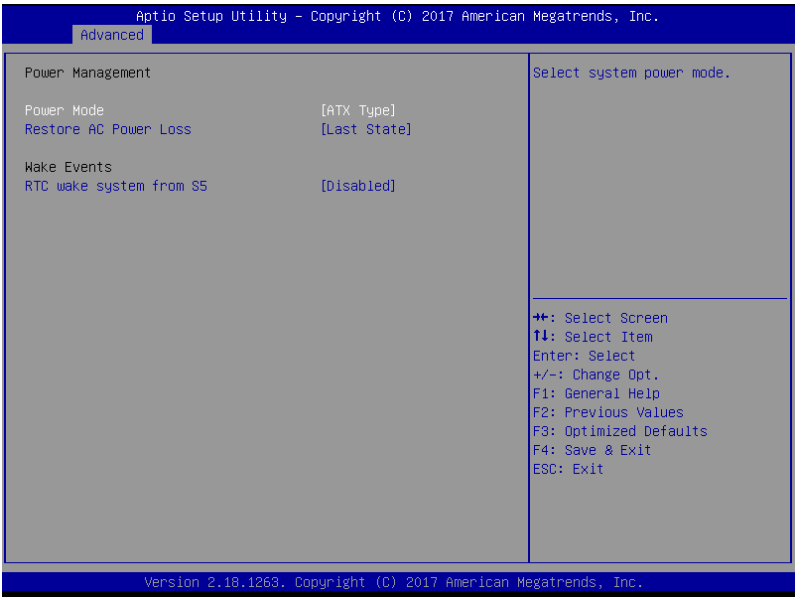
3.4.6.2 Serial Port 2 Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

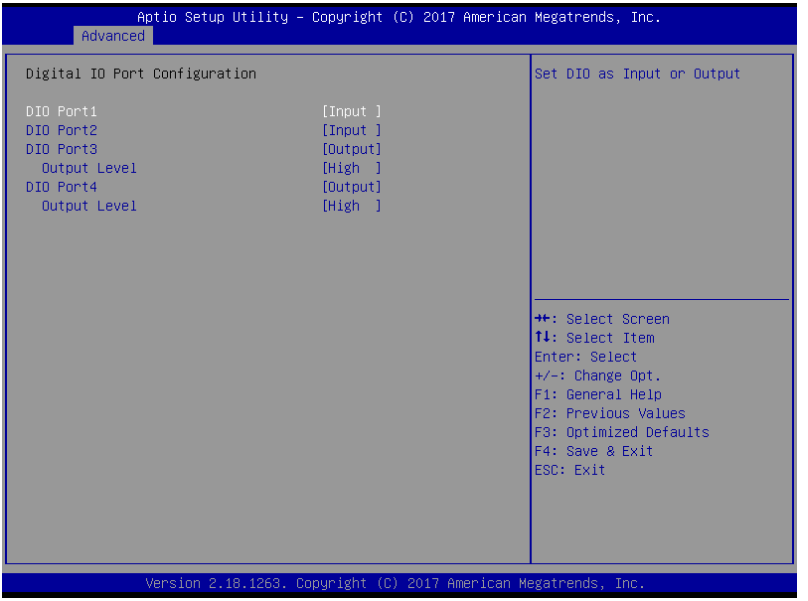
3.4.7 Power Management



Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
Fixed Time: System will wake on the hr::min::sec specified		

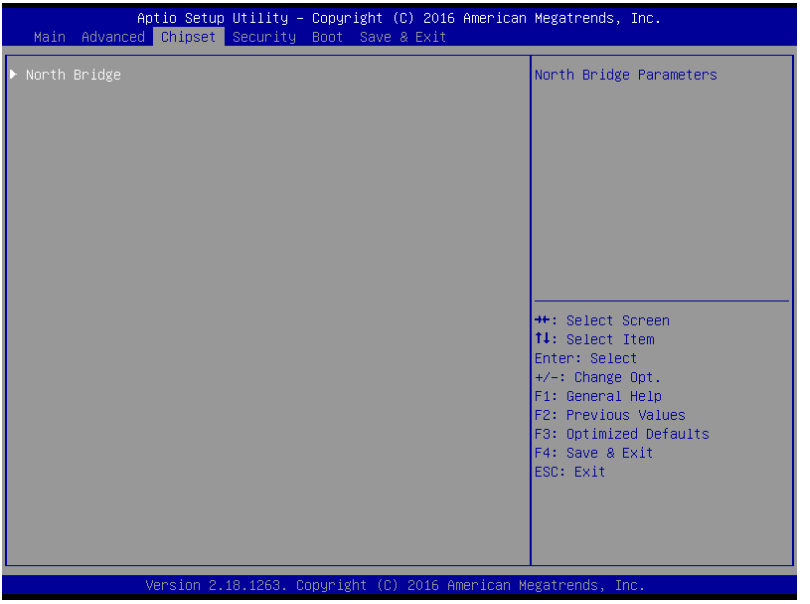
3.4.8 Digital IO Port Configuration



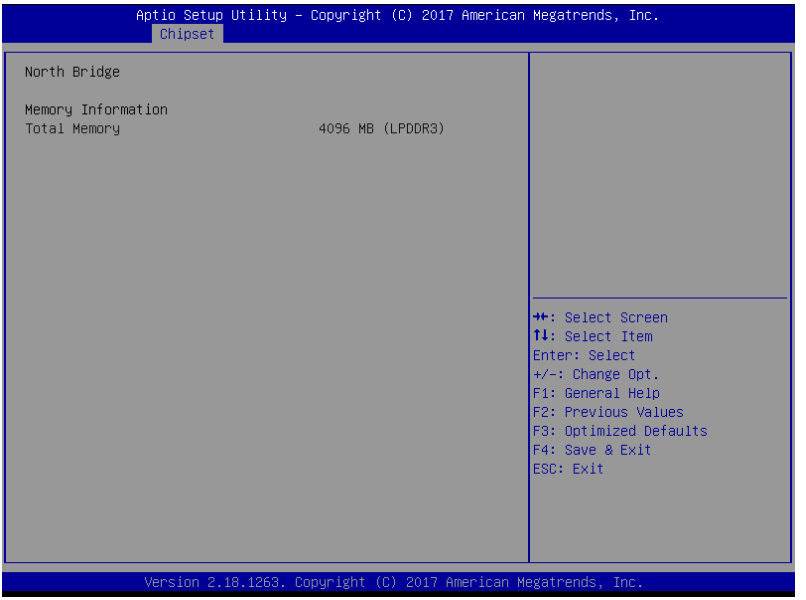
Options summary:

DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

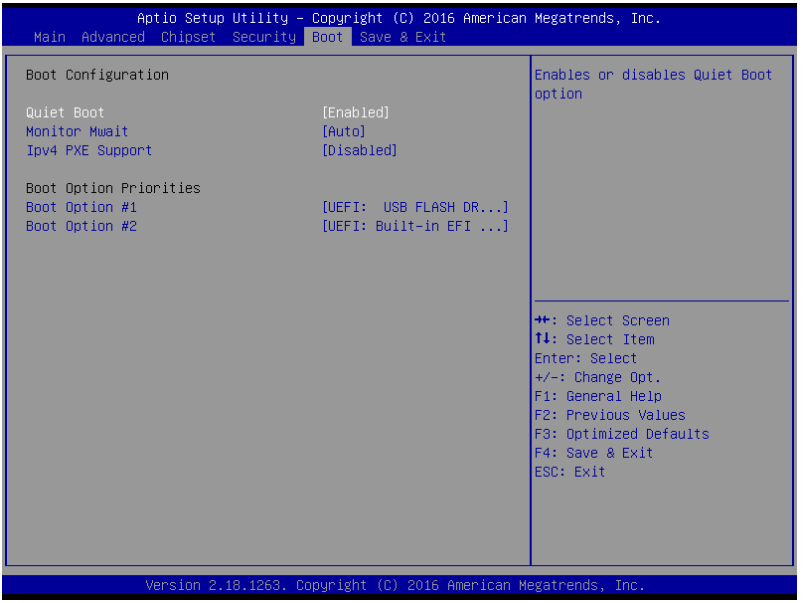
3.5 Setup submenu: Chipset



3.5.1 North Bridge



3.6 Setup submenu: Security



Change User/Supervisor Password

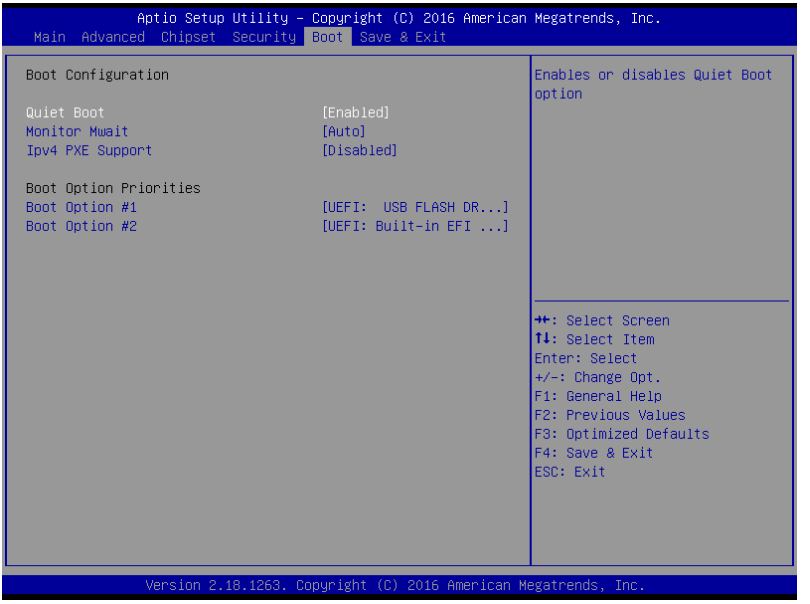
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

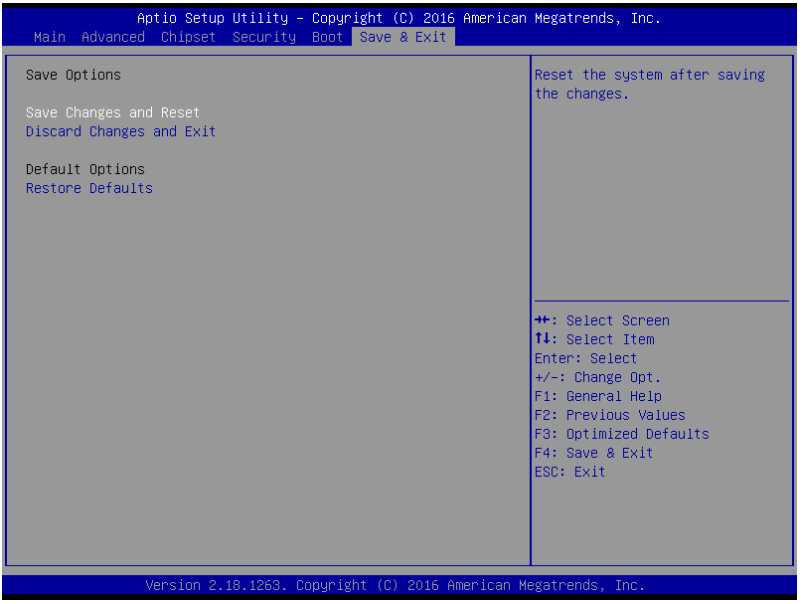
3.7 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
EnableDisable showing boot logo.		
Monitor Mwait	Disable	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The PICO-APL3-SEMI comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **STEP1 - CHIPSET** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **STEP2 - VGA** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 3 – Install LAN Driver

1. Open the **STEP3 - LAN** folder and and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - AUDIO** folder and open the **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 5 – Install TXE Driver

1. Open the **STEP5 - TXE** folder and open the **SetupTXE.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 6 – Install Serial IO Driver

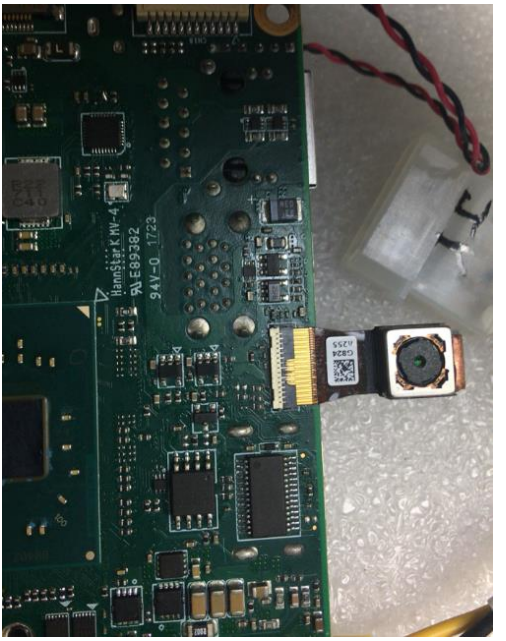
1. Open the **STEP6-Serial IO** folder and open the **SetupSerialIO.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 7 – CSI CAMERA test SOP

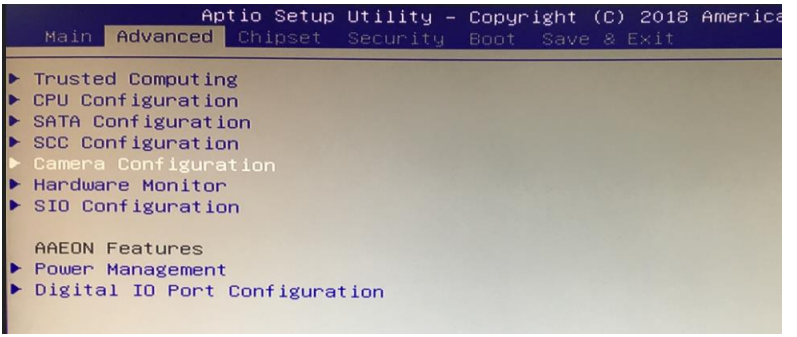
1. Install the camera

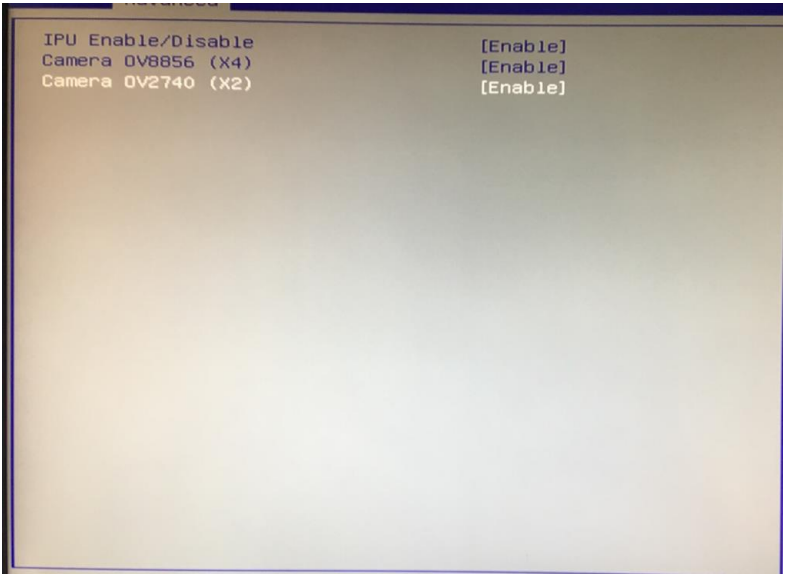
9689FG1800 to PICO-APL3 CN32

9689AG2400 to PICO-APL3 CN33

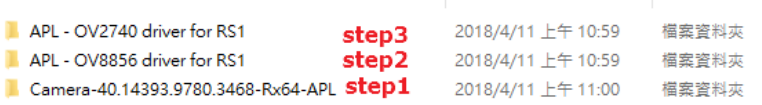


2. BIOS enable





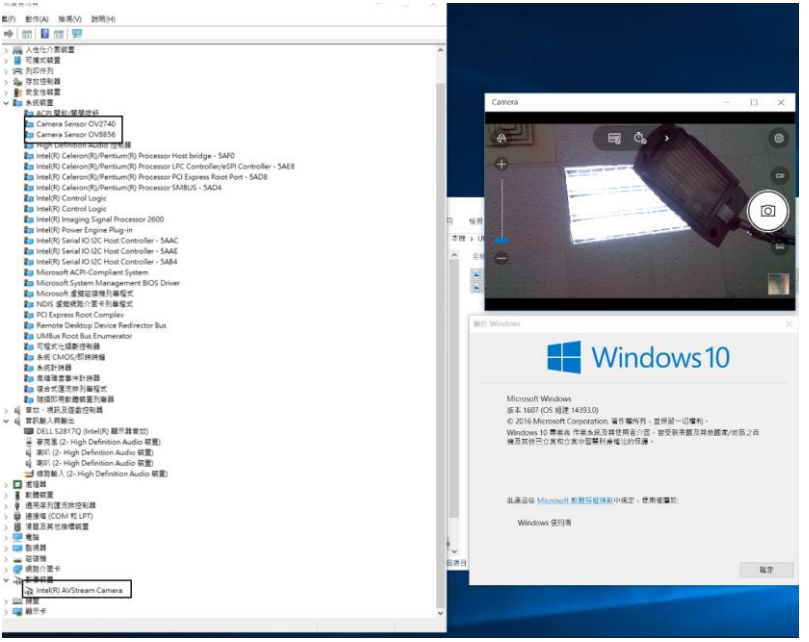
3. Install drivers manually



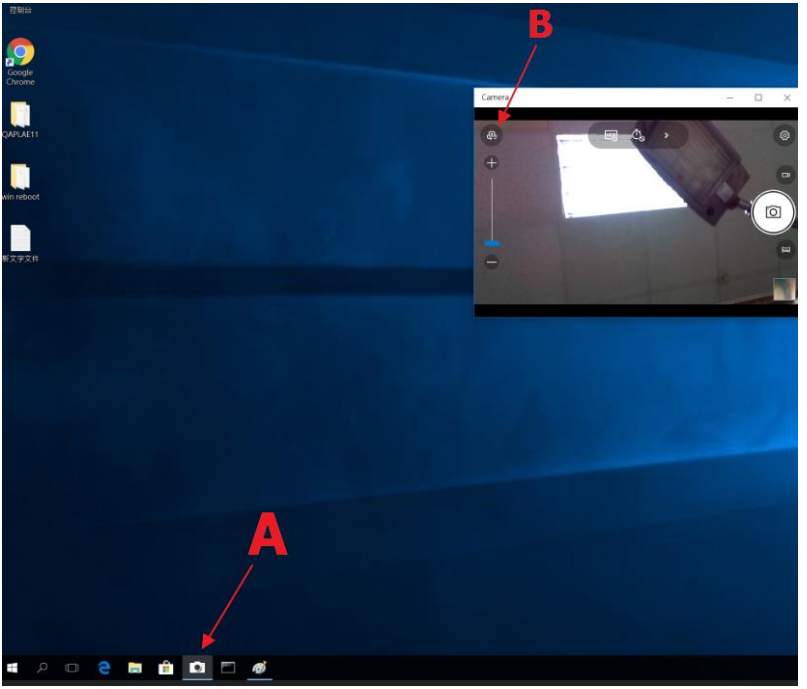
3a. Install Driver : Avstream Camera (VENID: 8086 DEVID: 5A85)

3b. Install Driver: Imaging Signal Processor 2600 (VENID: 8086 DEVID: 5A88)

3c. Install Driver: Control Logic (ACPI _HID : INT3472)



4. Test



A: Start camera app

B: Front and rear camera switch

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*****************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte EcBRAMIndex //This parameter is represented from Note1
#define byte EcBRAMData //This parameter is represented from Note2
#define byte BRAMLDNReg //This parameter is represented from Note3
#define byte BRAMFnDataReg //This parameter is represented from Note4
#define   byte   EcBRAMReadByte(byte Offset);
#define void IOWriteByte(byte Offset, byte Value);
#define byte IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte TimerReg //This parameter is represented from Note5
#define byte TimerVal // This parameter is represented from Note10
#define byte UnitReg //This parameter is represented from Note6
#define byte UnitBit //This parameter is represented from Note7
#define byte UnitVal //This parameter is represented from Note11
#define byte RSTReg //This parameter is represented from Note8
#define byte RSTBit //This parameter is represented from Note9
#define byte RSTVal //This parameter is represented from Note12
*****************************************************************************
```

```
*****************************************************************************

VOID Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();


        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
           AaeonWDTEnable();
}
*****************************************************************************
```

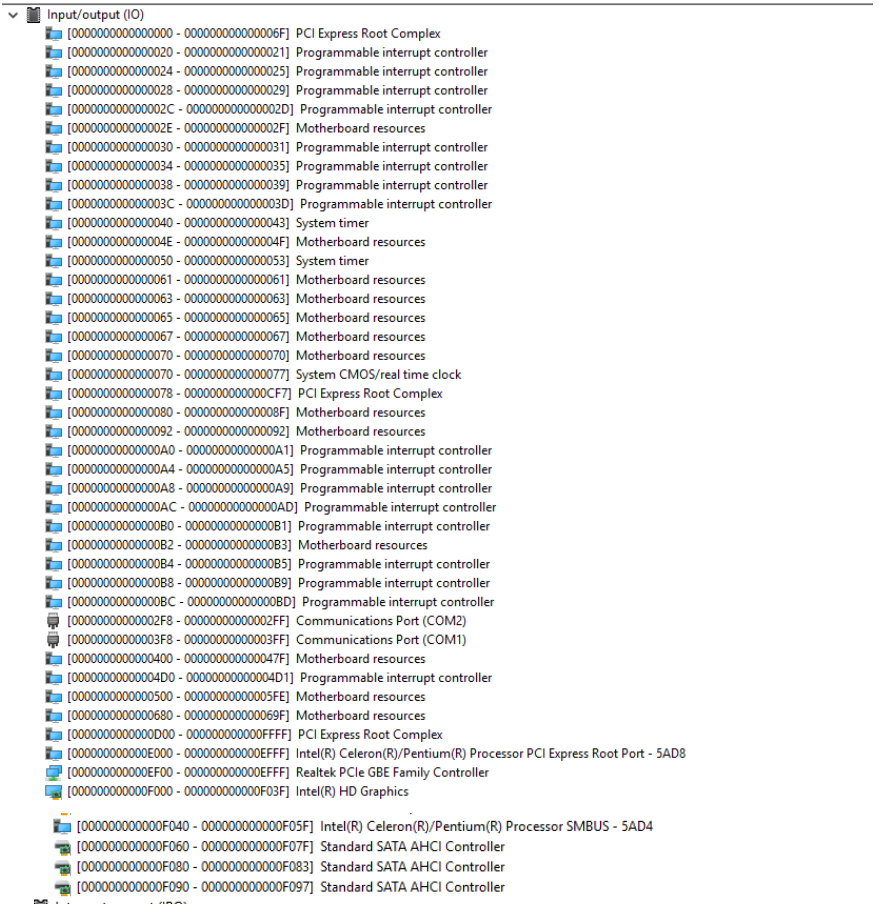
```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable (){
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (){
         // Disable WDT ounting
         WDTEnableDisable(0);
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID WDTEnableDisable(byte
       Value){ ECBRAMWriteByte(TimerReg , Value);
}

VOID
       WDTParameterSetting(){ By
       te TempByte;


          // Watchdog Timer counter setting
          ECBRAMWriteByte(TimerReg , TimerVal);
       // WDT counting unit setting
         TempByte = ECBRAMReadByte(UnitReg);
         TempByte |= (UnitVal << UnitBit);
         ECBRAMWriteByte(UnitReg , TempByte);
         // WDT RST pulse width setting
         TempByte = ECBRAMReadByte(RSTReg);
         TempByte |= (RSTVal << RSTBit);
         ECBRAMWriteByte(RSTReg , TempByte);
}
*********************************************************************************
```

```
*********************************************************************************
VOID ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        IOWriteByte(EcBRAMData, Value);


        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x30);                  //Write start
}

Byte ECBRAMReadByte(byte
      OPReg){ IOWriteByte(EcBRAMIndex, 0x10);
      IOWriteByte(EcBRAMData, BRAMLDNReg);
      IOWriteByte(EcBRAMIndex, 0x11);
      IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x10);                  //Read start


        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        Return              IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```

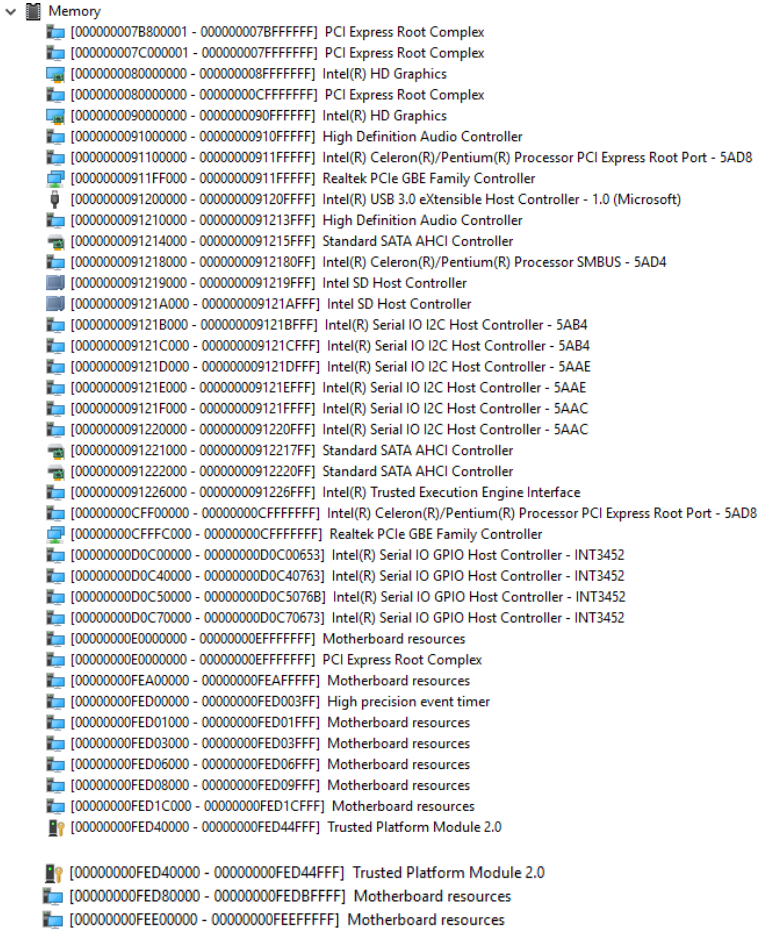
Appendix B

I/O Information

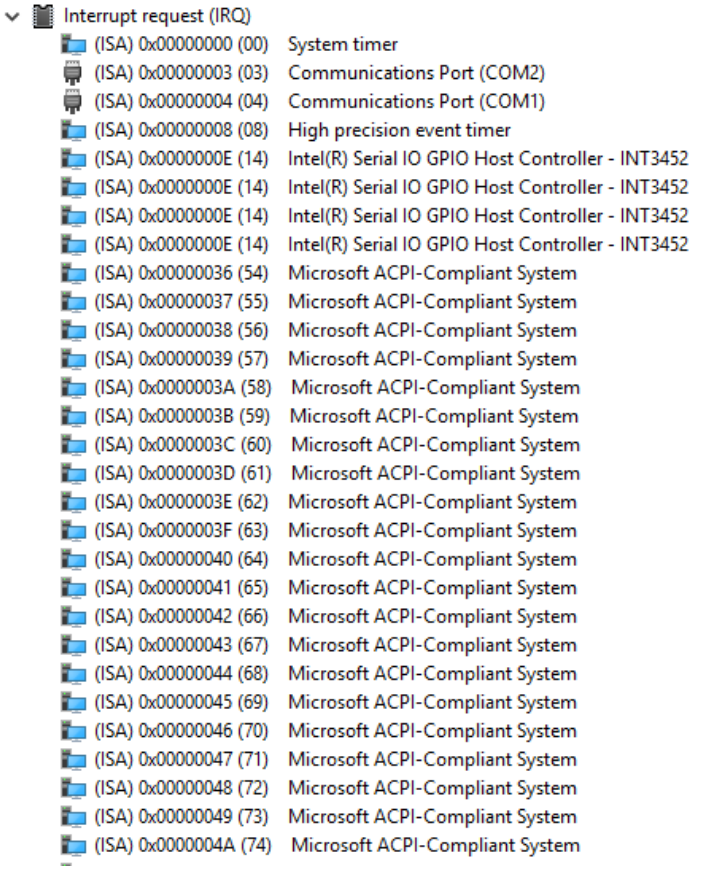
B.1 I/O Address Map



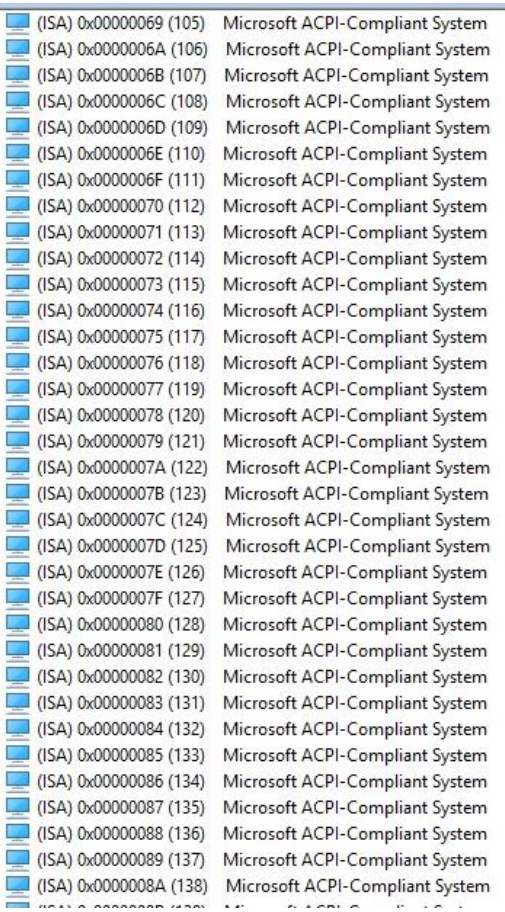
B.2 Memory Address Map



B.3 IRQ Mapping Chart



(ISA) 0x0000004A (74) Microsoft ACPI-Compliant System
(ISA) 0x0000004B (75) Microsoft ACPI-Compliant System
(ISA) 0x0000004C (76) Microsoft ACPI-Compliant System
(ISA) 0x0000004D (77) Microsoft ACPI-Compliant System
(ISA) 0x0000004E (78) Microsoft ACPI-Compliant System
(ISA) 0x0000004F (79) Microsoft ACPI-Compliant System
(ISA) 0x00000050 (80) Microsoft ACPI-Compliant System
(ISA) 0x00000051 (81) Microsoft ACPI-Compliant System
(ISA) 0x00000052 (82) Microsoft ACPI-Compliant System
(ISA) 0x00000053 (83) Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84) Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85) Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86) Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87) Microsoft ACPI-Compliant System
(ISA) 0x00000058 (88) Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89) Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90) Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91) Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103) Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System


(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System

(ISA) 0x000001E3 (483) Microsoft ACPI-Compliant System
(ISA) 0x000001E4 (484) Microsoft ACPI-Compliant System
(ISA) 0x000001E5 (485) Microsoft ACPI-Compliant System
(ISA) 0x000001E6 (486) Microsoft ACPI-Compliant System
(ISA) 0x000001E7 (487) Microsoft ACPI-Compliant System
(ISA) 0x000001E8 (488) Microsoft ACPI-Compliant System
(ISA) 0x000001E9 (489) Microsoft ACPI-Compliant System
(ISA) 0x000001EA (490) Microsoft ACPI-Compliant System
(ISA) 0x000001EB (491) Microsoft ACPI-Compliant System
(ISA) 0x000001EC (492) Microsoft ACPI-Compliant System
(ISA) 0x000001ED (493) Microsoft ACPI-Compliant System
(ISA) 0x000001EE (494) Microsoft ACPI-Compliant System
(ISA) 0x000001EF (495) Microsoft ACPI-Compliant System
(ISA) 0x000001F0 (496) Microsoft ACPI-Compliant System
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000016 (22) Realtek PCIe GBE Family Controller
(PCI) 0x00000019 (25) High Definition Audio Controller
(PCI) 0x0000001B (27) Intel(R) Serial IO I2C Host Controller - 5AAC
(PCI) 0x0000001C (28) Intel(R) Serial IO I2C Host Controller - 5AAE
(PCI) 0x0000001F (31) Intel(R) Serial IO I2C Host Controller - 5AB4
(PCI) 0x00000027 (39) Intel SD Host Controller
(PCI) 0xFFFFFFFA (-6) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFFB (-5) Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFFC (-4) Intel(R) HD Graphics
(PCI) 0xFFFFFFFD (-3) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFE (-2) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8

Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN51,CN61	COM	JCTC	11002H00-9P	COM Port Cable	1701090122
CN12	Audio	Molex	51021-1000	Audio Cable	1703100084
CN52	Speaker	Molex	51021-0200	N/A	N/A
CN60	DIO	PINREX	633-92-03GB00	N/A	N/A
CN50	Front Panel	PINREX	633-92-04GB00	N/A	N/A
CN39	SATA PWR	JST	PHR-4	SATA power cable	1702150121
CN18	LPC Port	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN9	Battery	Molex	51021-0200	Battery Cable	175011301C

Appendix D

Programming Digital IO

D.1 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
IO DirectionFunction and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
IO Vaule/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note11)	GPF0
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note12)	GPF1
GPO0 Pin Status	0x00(Note6)	2(Note9)	(Note13)	GPE0
GPO1 Pin Status	0x00(Note6)	3(Note10)	(Note14)	GPE1

D.2 Digital I/O Sample Program

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte EcBRAMIndex    //This parameter is represented from Note1
#define byte EcBRAMData    //This parameter is represented from Note2
#define byte BRAMLDNReg //This parameter is represented from Note3
#define byte BRAMFnData0Reg //This parameter is represented from Note4
#define byte BRAMFnData1Reg //This parameter is represented from Note5
#define void EcBRAMWriteByte(byte Offset, byte Value);
#define    byte    EcBRAMReadByte(byte Offset);
#define void IOWriteByte(byte Offset, byte Value);
#define byte IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DIO0ToDIO7Reg // This parameter is represented from Note6
#define byte DIO0Bit // This parameter is represented from Note7
#define byte DIO1Bit // This parameter is represented from Note8
#define byte DIO2Bit // This parameter is represented from Note9
#define byte DIO3Bit // This parameter is represented from Note10
#define byte DIO0Val // This parameter is represented from Note11
#define byte DIO1Val // This parameter is represented from Note12
#define byte DIO2Val // This parameter is represented from Note13
#define byte DIO3Val // This parameter is represented from Note14
*******************************************************************************
```

```
*********************************************************************************************
VOID Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //                  Example, Read Digital I/O Pin 1 status
         // Output :
         //                 InputStatus :
         //                          0: Digital I/O Pin level is low
         //                          1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO1Bit);


        // Procedure : AaeonSetOutputLevel
        // Input :
        //                  Example, Set Digital I/O Pin 1
        level AaeonSetOutputLevel(DIO0ToDIO7Reg,
        DIO1Bit, DIO1Val);
}
*********************************************************************************************
```

```
**********************************************************************************
Boolean AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg,
        OptionReg); If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){ Byte
        TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum); ECBRAMWriteByte(OptionReg, BitNum,
        Value);
}

**********************************************************************************
```

```
*********************************************************************************
VOID ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);                    //Write start
}

Byte ECBRAMReadByte(byte FnDataReg, byte
        OPReg){ IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, FnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);                    //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return              IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```