PICO-APL1-SEMI

PICO-SEMI System

User's Manual 1st Ed

Last Updated: March 4, 2024

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-APL1-SEMI	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚(PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	O	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	PICO-SEMI
CPU	Intel® Celeron® Processor N3350 (2C/2T, 1.10 GHz, up to 2.40 GHz, TDP 6W)
Chipset	Integrated with Intel® SoC
Memory Type	DDR3L 1600MHz (Max 8GB)/1866MHz (Max 4GB), SODIMM x 1, Non-ECC*
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Security	—
RTC Battery	Lithium Battery 3V/240mAh
Dimension	4.8" x 3.15" x 1.73" (122mm x 80mm x 44mm)
Gross Weight	0.59 lb. (0.27Kg)
OS Support	Windows 10 (64 bit) Linux Ubuntu 20.04.4/ Kernel 5.11.0-13-generic

Note: 1866MHz frequency is limited to verified DDR modules from AAEON's Approved Vendor List.

Power	
Power Requirement	+12V
Power Supply Type	ATX
Connector	Lockable DC Jack Connector
Power Consumption	Intel® Celeron® Processor N3350, DDR3L 8GB, 0.91A@+12V (Typical)

Display

Controller	Intel® HD Graphics 500/505
LVDS/eDP	—
Display Interface	HDMI 1.4b x 1 (up to 3840 x 2160)
Multiple Display	—

Audio

Codec	Realtek ALC897/892 (Optional)
Audio Interface	Line-out (Optional)
Speaker	—

External I/O

Ethernet	Intel® Ethernet Controller I210 GbE, RJ-45 x 1
USB	USB 3.2 Gen 1 x 2
Serial Port	—
Video	HDMI 1.4b x 1 (up to 3840 x 2160)

Internal I/O

USB	—
Serial Port	COM 1: RS-232 x 1 (Optional) COM 2: RS-232/422/485 x 1 (Ring/+5V/+12V) (Optional)
Video	—
SATA	—
Audio	Line-out (Optional)
DIO/GPIO	—
SMBus/I2C	—
Touch	—
FAN	—

External I/O

SIM	—
Front Panel	HDD LED, PWR LED, Power Button, Buzzer, Reset
Others	—

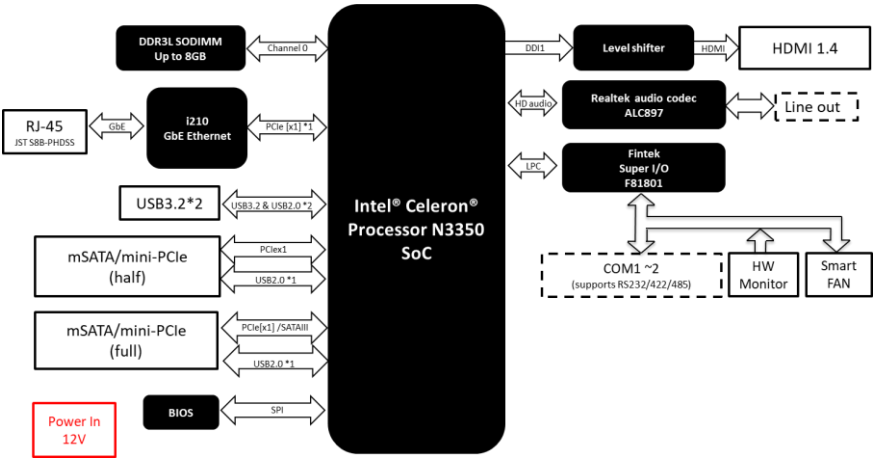
Expansion

Mini PCI-E/mSATA	Full-size mSATA/mPCIe x 1 (Default: mSATA, select with HW BOM) Half-size mPCIe x 1
M.2	—
Others	—

Environment

Operating Temperature	32°F ~ 122°F (0°C ~ 50°C) with 0.5 m/s airflow
Storage Temperature	-40°F ~ 185°F (-40°C ~ 85°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	170,000
EMC	CE/FCC Class A

1.2 Function Block

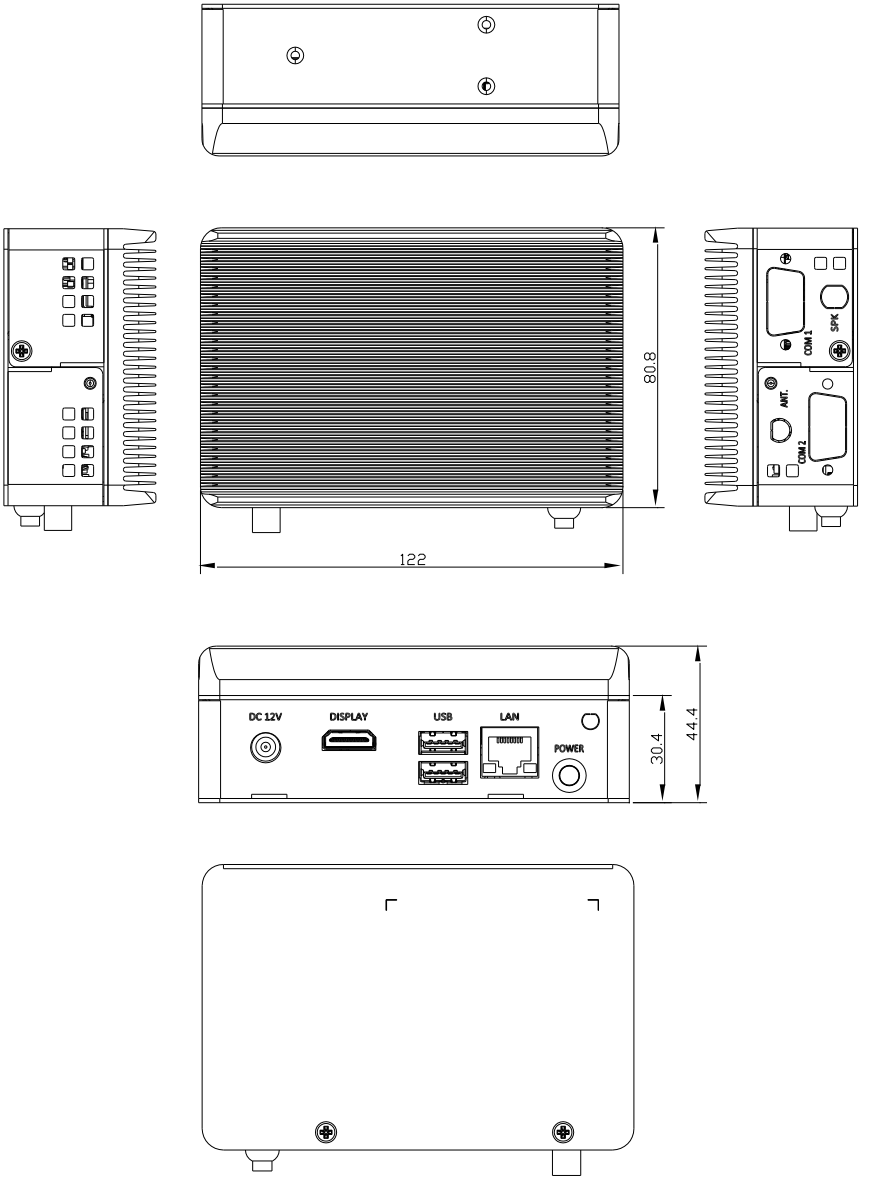


Chapter 2

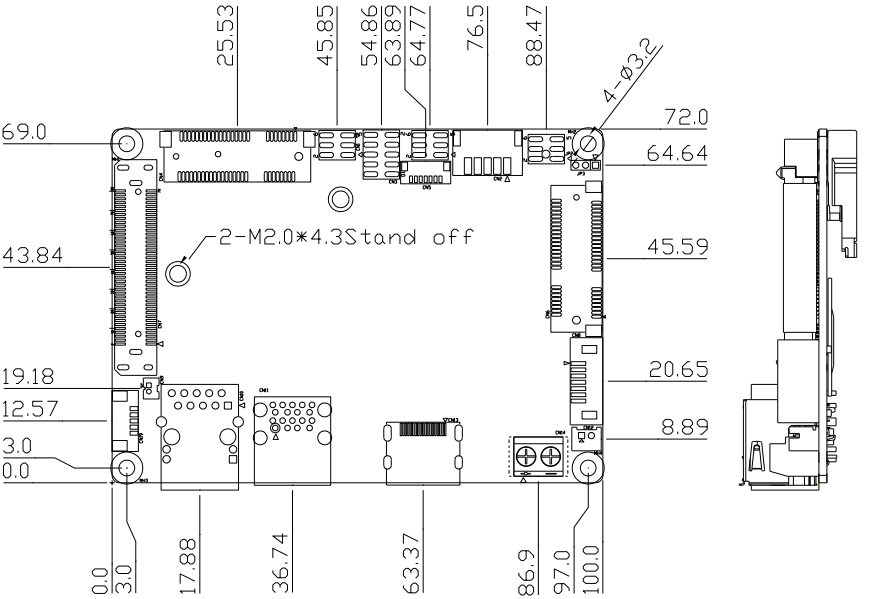
Hardware Information

2.1 Dimensions

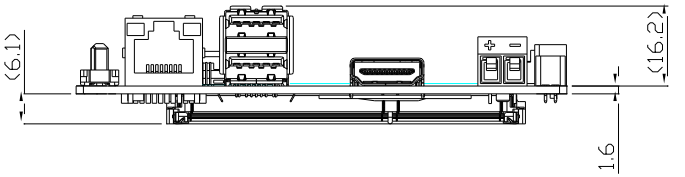
System Dimensions

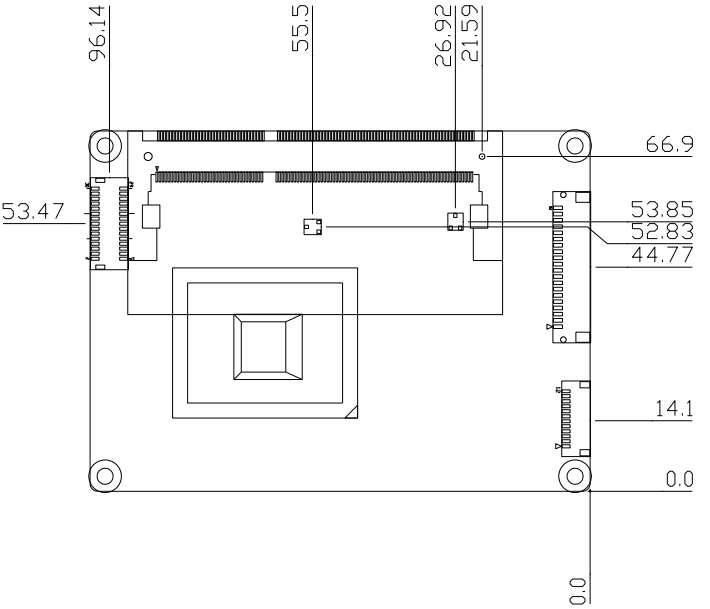


Board Dimensions



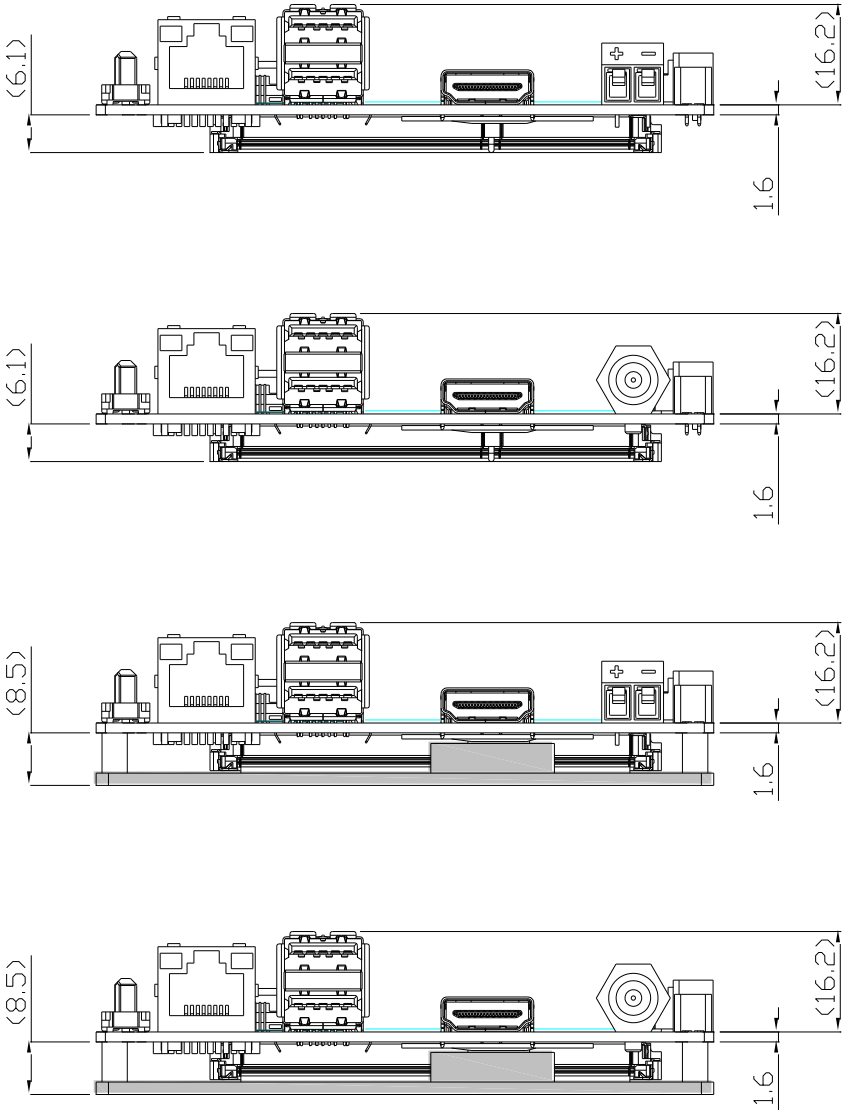
Component Side



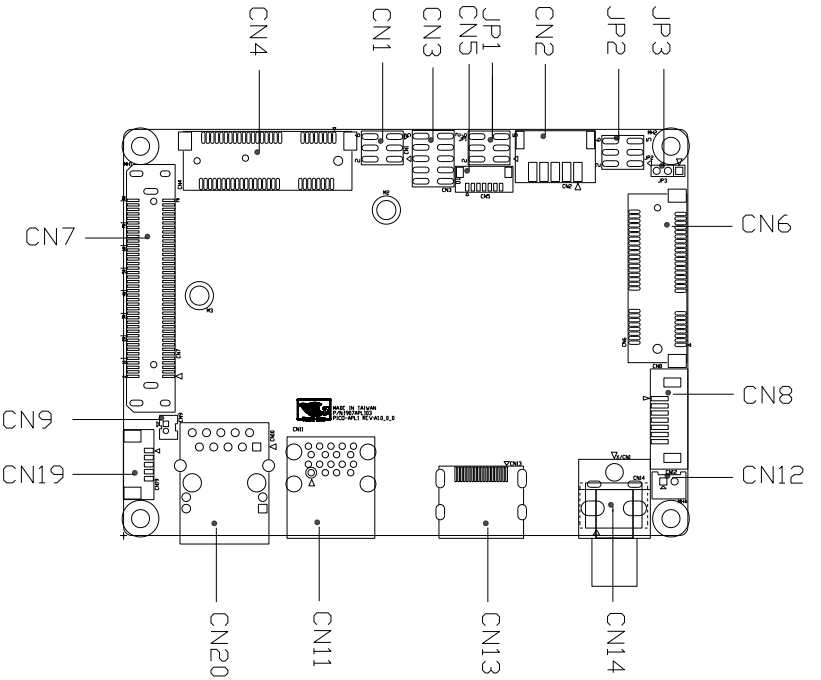


Solder Side

Rear I/O Configuration

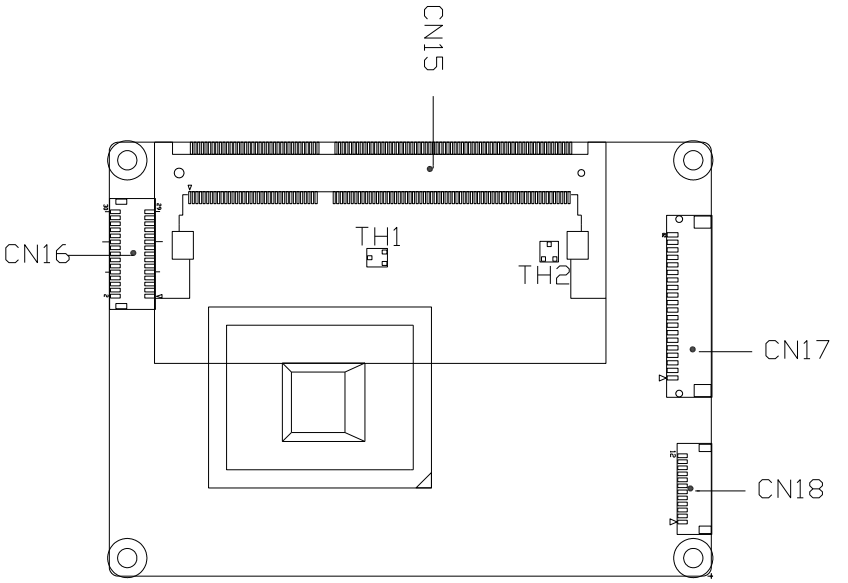


2.2 Jumpers and Connectors



Component Side

Solder Side



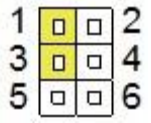
Solder Side

2.3 List of Jumpers

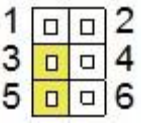
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1 (Pins 1, 3, 5)	Clear CMOS Jumper
JP1 (Pins 2, 4, 6)	Auto Power Button Enable/Disable Selection

2.3.1 Clear CMOS Jumper (JP1 Pins 1, 3, 5)

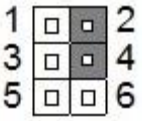


Normal (**Default**)

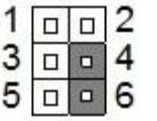


Clear CMOS

2.3.2 Auto Power Button Mode Selection (JP1 Pins 2, 4, 6)



Enable (**Default**)



Disable

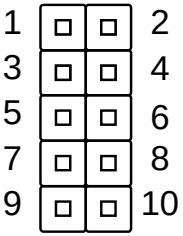
Note: To prevent damage to the system or unwanted operation, do not use any other configuration for JP1 than what is shown in Ch2.3.1 and Ch2.3.2.

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application.

Label	Function
CN3	Front Panel
CN4	Mini Card Slot (Half-size)
CN5	SPI Programming Header
CN6	Mini Card Slot (Full-size)/mSATA (By BOM)
CN8	SATA Port
CN9	Battery
CN11	USB 3.2 Gen 1 Port 1/Port 2
CN12	+5V Output for SATA HDD
CN13	HDMI Port
CN14	External +12V Input
CN15	DDR3L SODIMM Slot
CN17	COM Port 1/Port 2 and Line-Out Connector
CN18	LPC Port
CN19	USB 2.0 Port 1
CN20	RJ-45 LAN Port

2.4.1 Front Panel (CN3)



Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	BUZZER-	6	BUZZER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

2.4.2 Mini Card Slot (Half-size) (CN4)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	

Pin	Pin Name	Signal Type	Signal Level
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

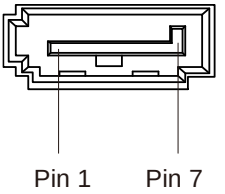
2.4.3 Mini Card/mSATA Slot (Full-size) (CN6)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB/+3.3V	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	

Pin	Pin Name	Signal Type	Signal Level
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-/mSATARX+	DIFF	
24	+3.3VSB/+3.3V	PWR	+3.3V
25	PCIE_RX+/mSATARX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-/mSATATX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+/mSATATX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB/+3.3V	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
40	GND	GND	
41	+3.3VSB/+3.3V	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB/+3.3V	PWR	+3.3V

2.4.4 SATA (CN8)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX1+	DIFF	
3	SATA_TX1-	DIFF	
4	GND	GND	
5	SATA_RX1-	DIFF	
6	SATA_RX1+	DIFF	
7	GND	GND	

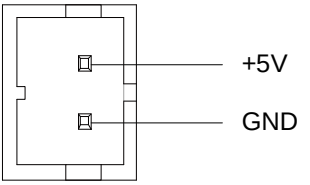
2.4.5 Battery (CN9)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.6 USB 3.2 Gen 1 Port 1/2 (CN11)

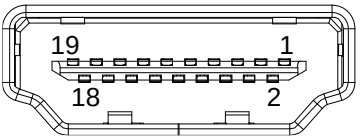
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX−	DIFF	
18	USB1_SSTX+	DIFF	

2.4.7 +5V Output for SATA HDD (CN12)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

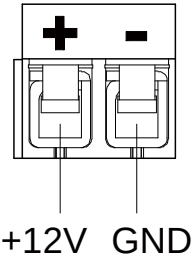
2.4.8 HDMI Port (CN13)



Pin	Pin Name	Signal Type	Signal Level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.4.9 External +12V Input (CN14)

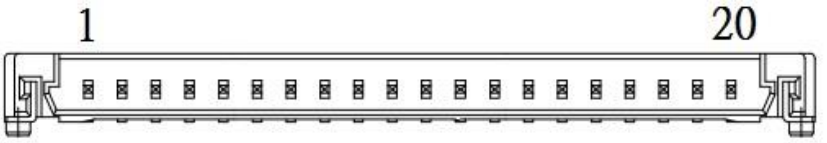


Pin	Pin Name	Signal Type	Signal Level
1	+121V	PWR	+12V
2	GND	GND	

2.4.10 DDR3L SODIMM Slot (CN15)

Standard specification.

2.4.11 COM Port 1/2 and Line-Out Connector (CN17)



Pin	Pin Name	Signal Type	Signal Level
1	DCDB	IN	
2	DSRB	IN	
3	RXB	IN	
4	RTSB	OUT	±9V
5	TXB	OUT	±9V
6	CTSB	IN	
7	DTRB	OUT	±9V
8	RIB/+5V/+12V	IN/ PWR	+5V/+12V
9	DCDA	IN	
10	DSRA	IN	
11	RXA	IN	
12	RTSA	OUT	±9V
13	TXA	OUT	±9V
14	CTSA	IN	
15	DTRA	OUT	±9V
16	RIA	IN	
17	GND	GND	
18	AGND	GND	
19	LOUT_R	I/O	
20	LOUT_L	I/O	

COM Port 2 (RS-485/422)

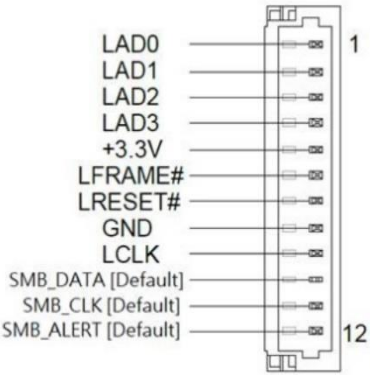
RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
17	GND	GND	

RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
17	GND	GND	

Note 1: COM 2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

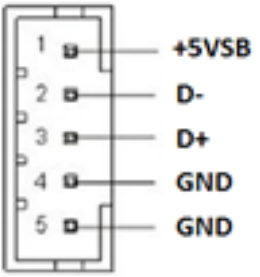
Note 2: COM 2 RI/+5V/+12V function can be set by BOM (R248-RI/ R256-+12V/ R250-+5V).

2.4.12 LPC Port (CN18)



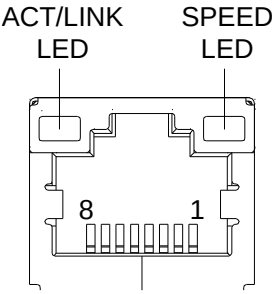
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA [Default]/I2C_DATA	I/O	+3.3V
11	SMB_CLK [Default]/I2C_CLK	OUT	+3.3V
12	SMB_ALERT [Default]/INT_SERIRQ	I/O	+3.3V

2.4.13 USB 2.0 Port 1 (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USBD5-	DIFF	
3	USBD5+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.14 RJ-45 LAN Port (CN20)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.5 Specifications for I/O Ports

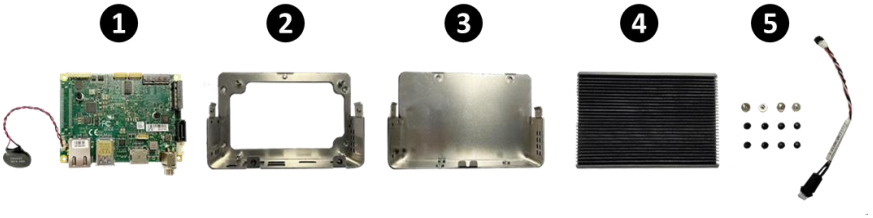
I/O	Reference	Signal Name	Rate Output
Mini-Card Slot	CN4	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
Mini-Card Slot	CN6	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
USB 3.2 Gen 1 Port 1 & 2	CN11	+5VSB	+5VSB/1A (per channel)
+5V Output for SATA HDD	CN12	+5V	+5V/1A
COM Port 2	CN17	+5V/+12V	+5V/1A or +12V/1A
LPC Port	CN18	+3.3V	+3.3V/0.5A
USB 2.0 Port 1	CN19	+5VSB	+5VSB/0.5A

2.6 Installation Guide

This section will guide you through the basic installation process for your new PICO-APL1-SEMI. For this process you will need a Phillips head screwdriver.

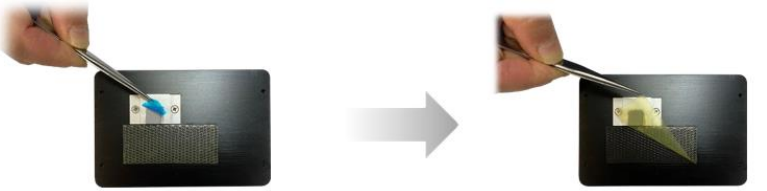
PICO-APL1-SEMI component list:

Item No.	Description	Remark/PN
1	PICO-APL1 Board	MB
2	Top Chassis	M1APL30010
3	Bottom Chassis	M1APL30020
4	Heatsink	TH0APL1010
5	Accessory Kits	
	Power Button Cable x 1	1709040104
	Screw.M3. Black x 8pcs	S1D3004031
	Screw.M3 Nickel x 4pcs	S1D5106010

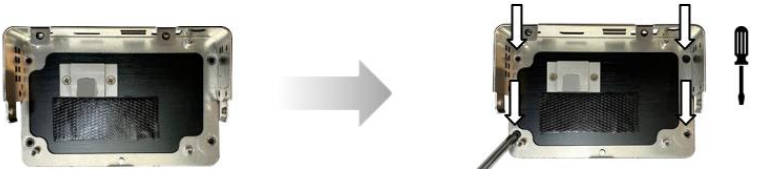


2.6.1 Installation Steps

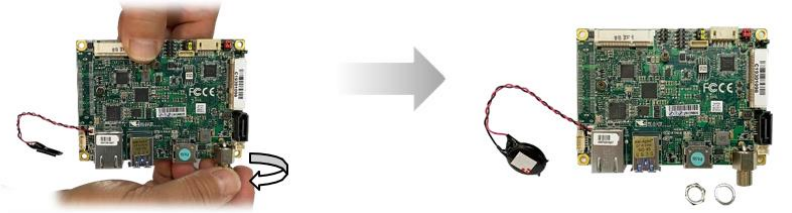
Step 1: On the heatsink, remove the two plastic coverings as shown.



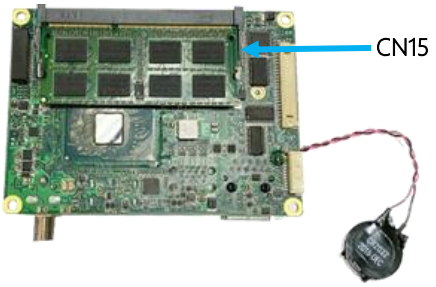
Step 2: Place the top chassis onto the heatsink. Note the orientation of the chassis with the heatsink. Secure with four black screws.



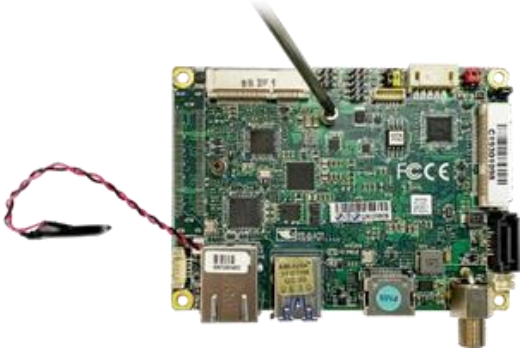
Step 3: On the PICO-APL1 board, remove the nut and washer from the power input port.



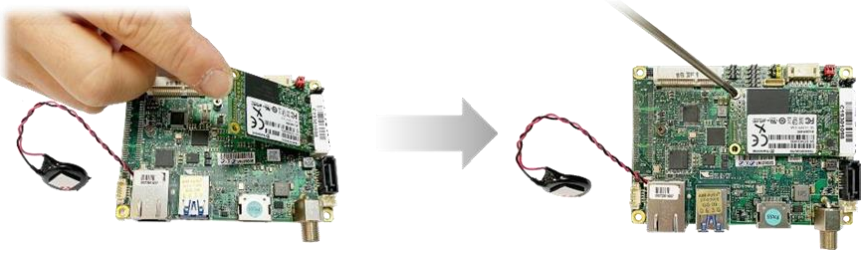
Step 4: On the solder side of the PICO-APL1 board, install the memory RAM module. Insert at an angle (~30°) and then gently press down until it is secured.



Step 5: To install M.2 storage module, remove the securing screw from the board's component side.

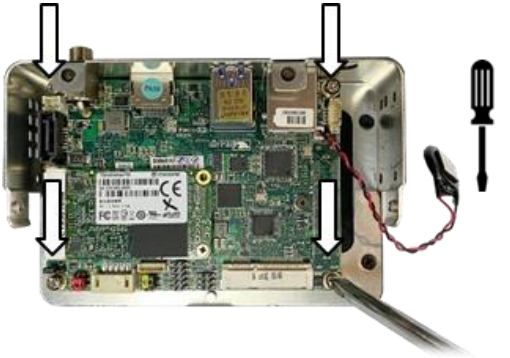


Step 6: Insert the M.2 module at an angle (~30°). Press down gently and secure with the screw.

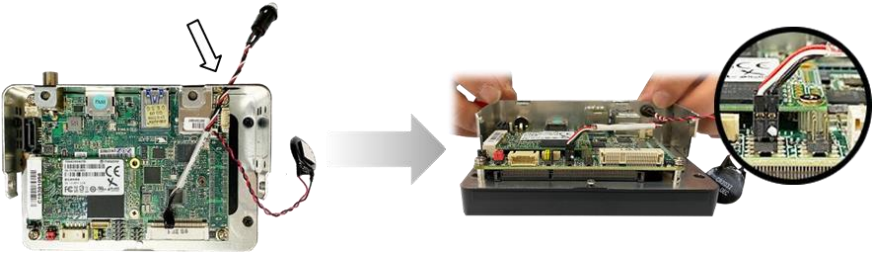


Step 7: Insert the PICO-APL1 board into the chassis assembly with the solder side toward the heatsink. DO NOT place the CMOS battery between the board and heatsink.

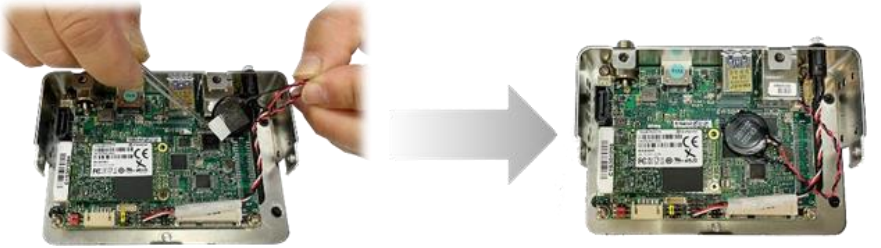
Step 8: Check that the I/O ports are properly aligned. Secure board with four nickel screws.



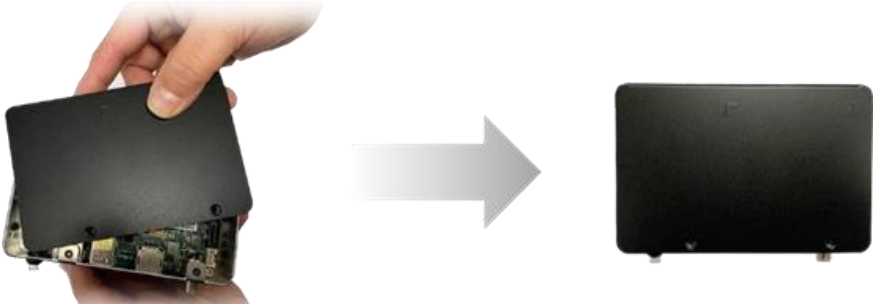
Step 9: Thread the power button cable through the hole for the power button. Plug the cable into the front panel connector (CN3). **Note**: The white dot indicates PIN 1 connector, make sure the connector is properly aligned. Next, gently push the power button in until it is secure (you will hear a 'snap'). Be careful not to tangle the power button cable with the CMOS battery cable.



Step 10: Peel the backing off of the tape on the CMOS battery. Gently press the battery onto the PICO-APL1 board to secure it.

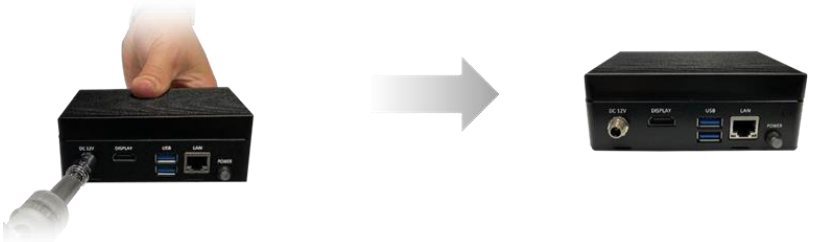


Step 11: Attach the bottom chassis by first lining up the right side, then swivel the chassis into place. **Note**: the bottom chassis does not slide directly on, it must swivel into place as shown in the figure.



Step 12: Ensure the bottom chassis is properly lined up and attached. Use black screws to secure, two screws on the bottom and one screw on the left and right sides of the chassis.

Step 13: Replace the washer and nut for the power input port.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or display an error message. The system can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the system will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable/disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Security

Set setup administrator password.

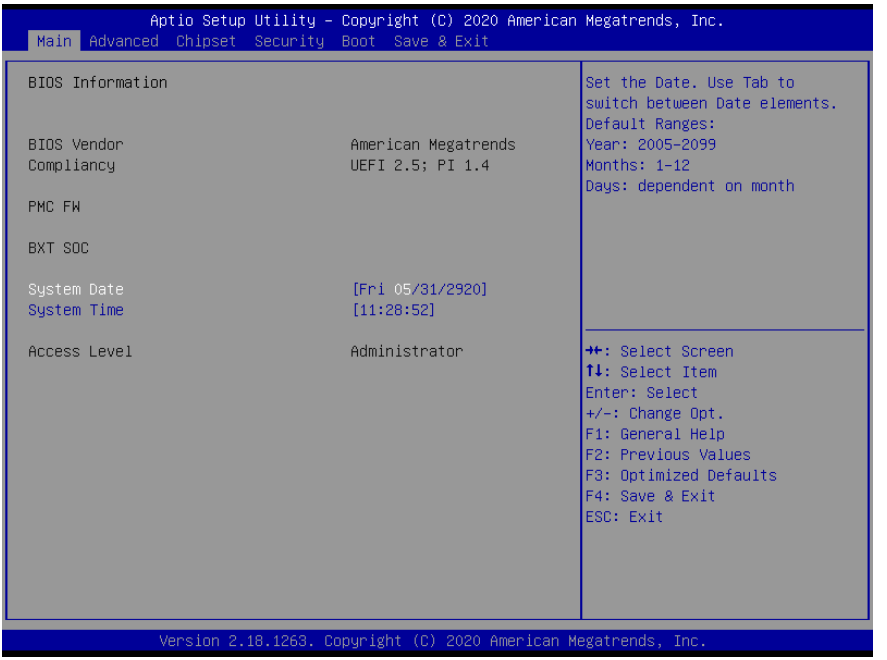
Boot

Enables/disable quiet boot option.

Save & Exit

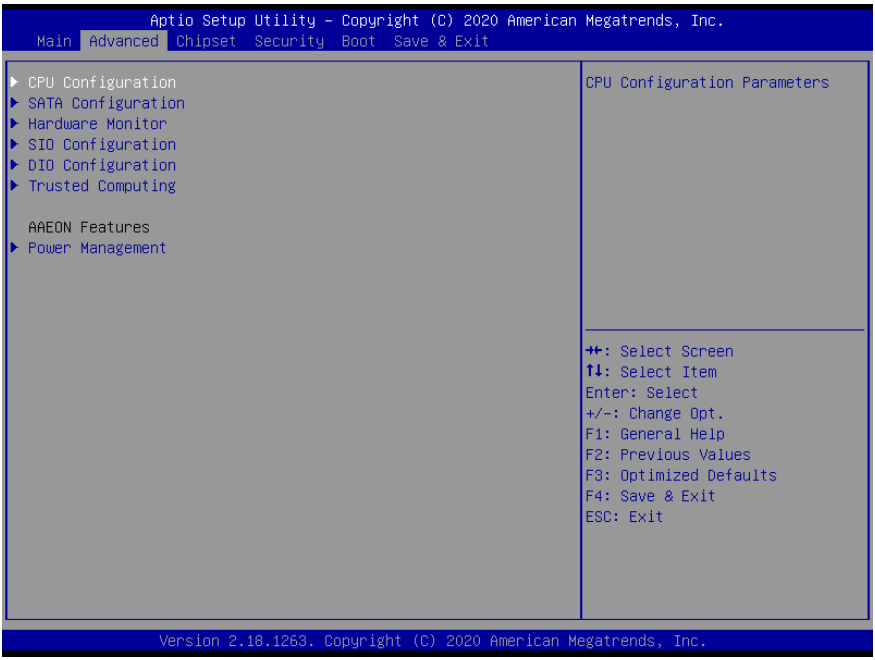
Save changes and exit setup.

3.3 Setup Submenu: Main



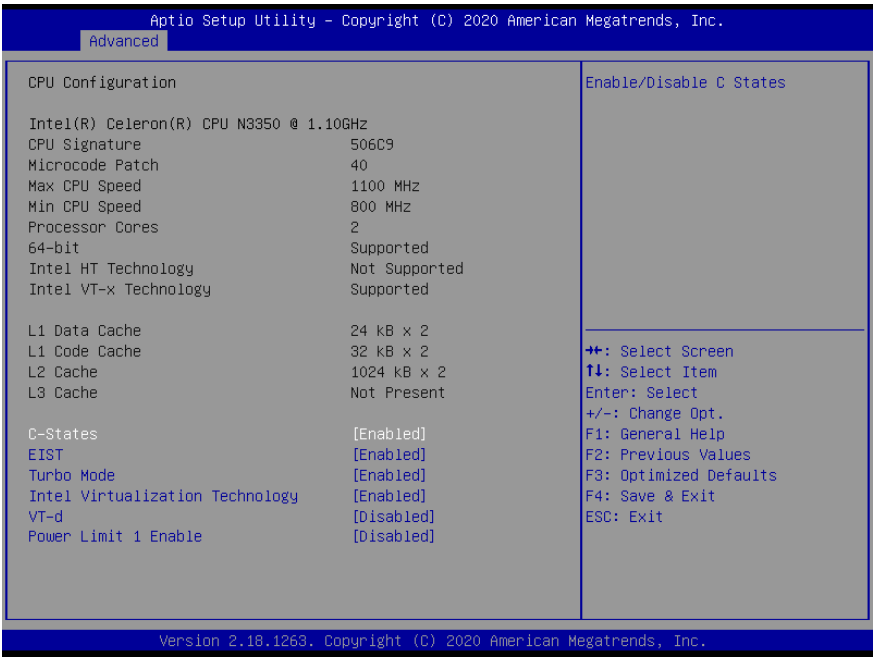
Options Summary		
System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

3.4 Setup Submenu: Advanced



Options Summary	
CPU Configuration	Menu for CPU Configuration Parameters.
SATA Configuration	Menu for SATA Device Configuration.
Hardware Monitor	Display system hardware status (CPU temperature, etc.).
SIO Configuration	SIO Chip configuration. Enable or Disable SIO Logical Devices, Resources and Features settings, etc.
DIO Configuration	Set Input/ Output of Digital Port Configuration.
Trusted Computing	Set Security Device Support Parameters.
Power Management	System ACPI/ Power Mode/ Wake Event Configuration.

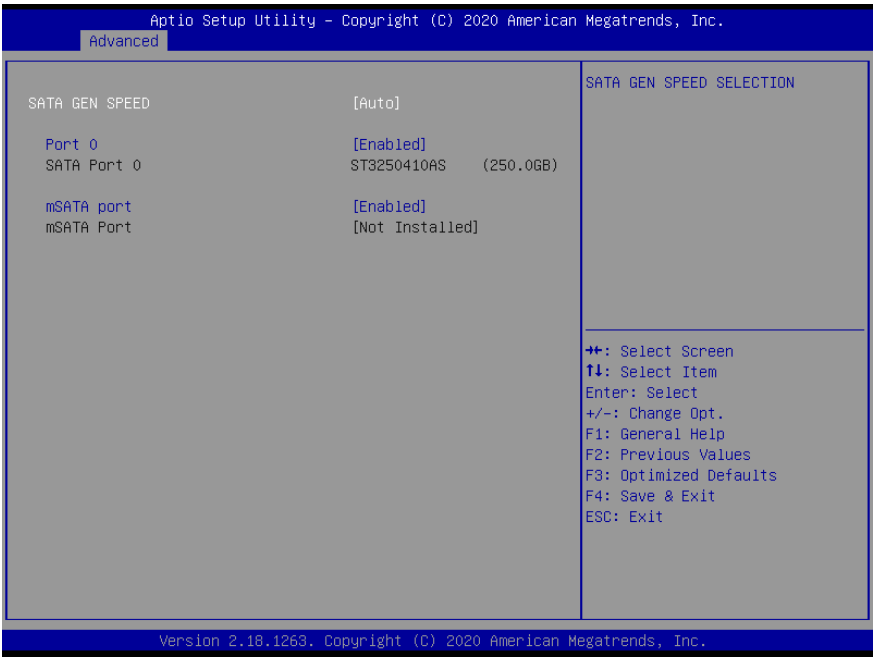
3.4.1 CPU Configuration



Options Summary		
C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo mode.		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		

Options Summary		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU VT-d.		
Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1.		

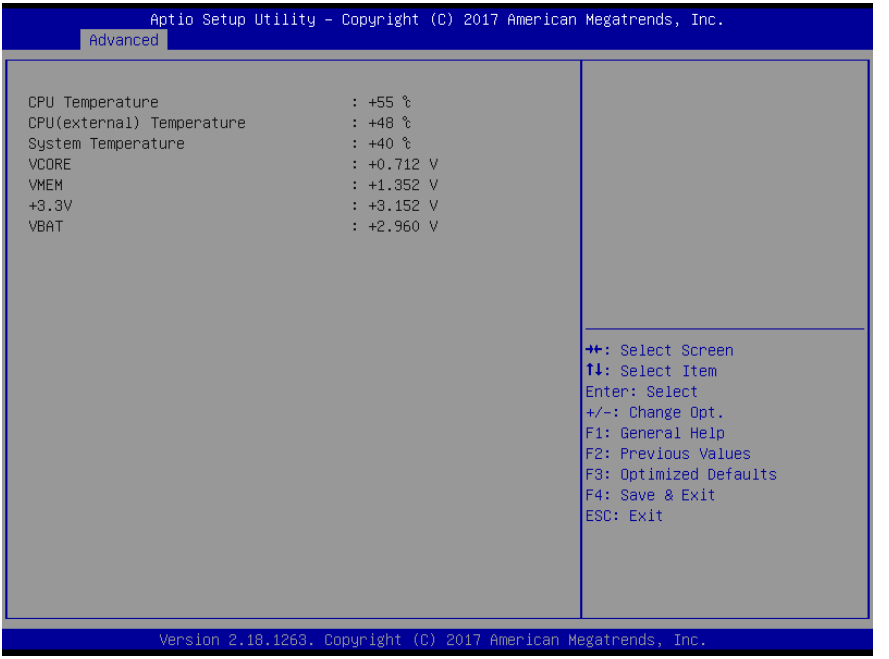
3.4.2 SATA Configuration



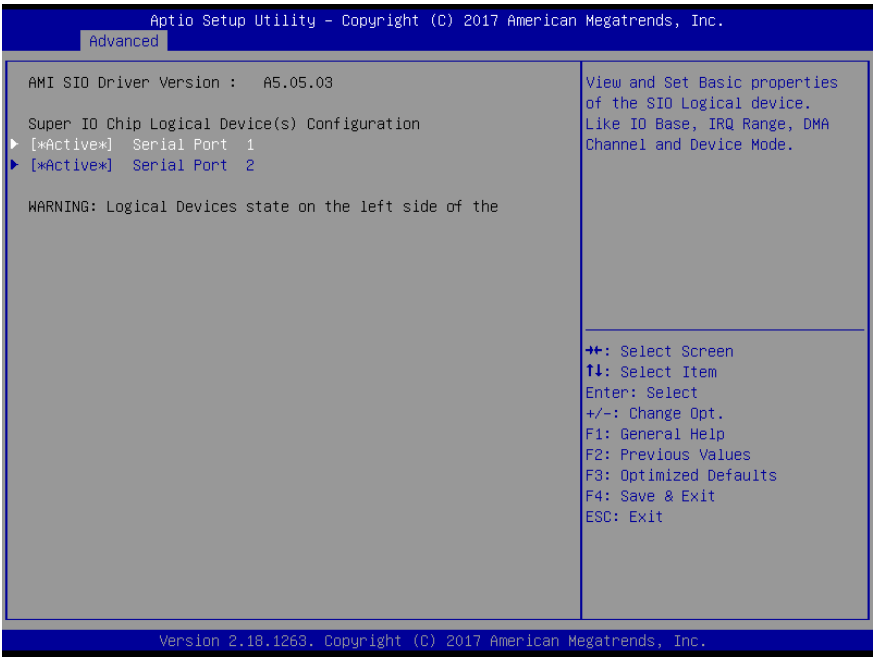
Options Summary		
SATA GEN SPEED	AUTO	Optimal Default, Failsafe Default
	GEN1	
	GEN2	
	GEN3	
SATA GEN SPEED selection.		

Options Summary		
Port 0/ mSATA port	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA port		

3.4.3 Hardware Monitor

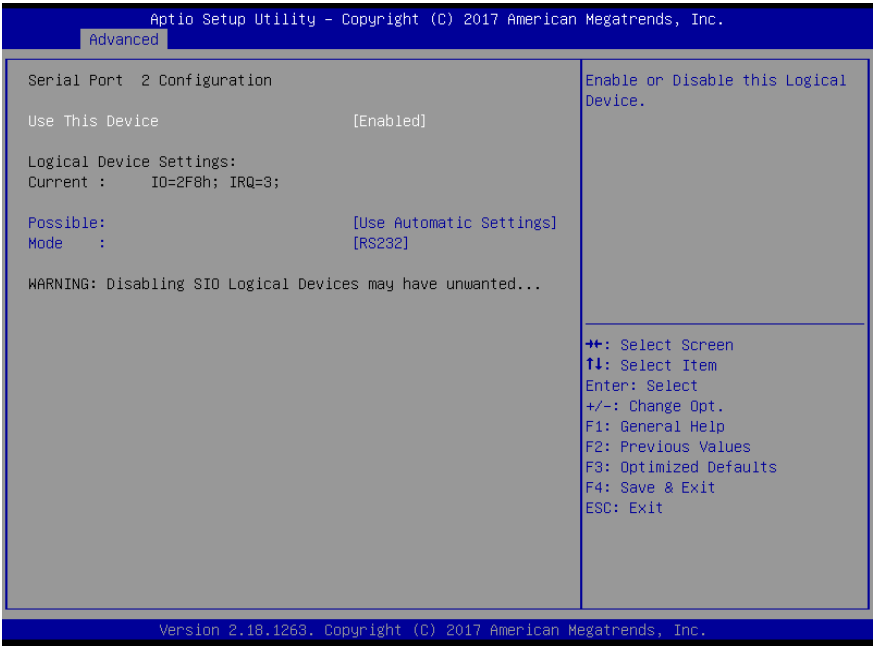


3.4.4 SIO Configuration



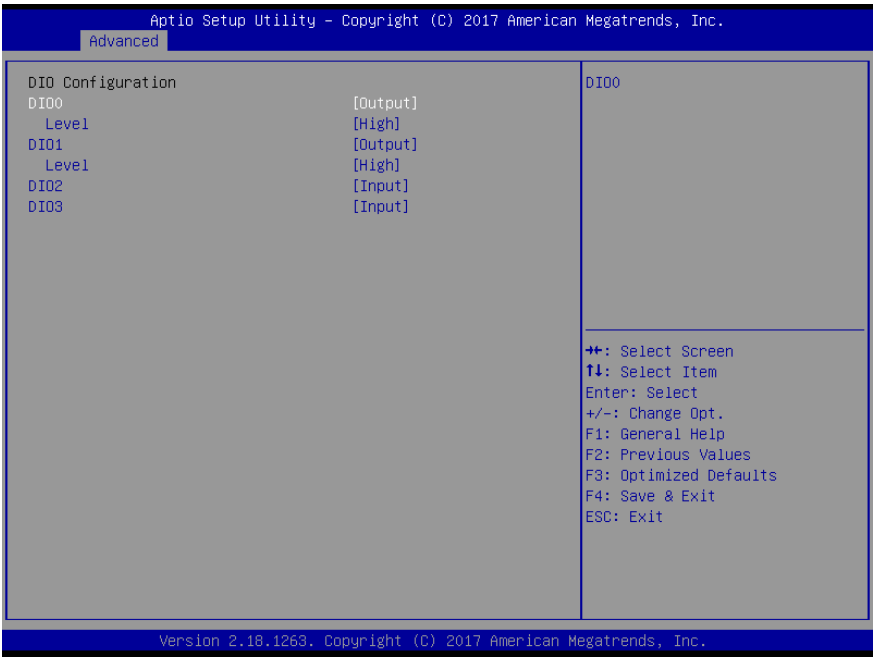
Options Summary	
Serial Port 1/2 Configuration	
View and Set Basic properties of the SIO Logical device. Like IO Base , IRQ Range , DMA Channel and Device Mode.	

3.4.4.1 Serial Port Configuration



Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.5 DIO Configuration



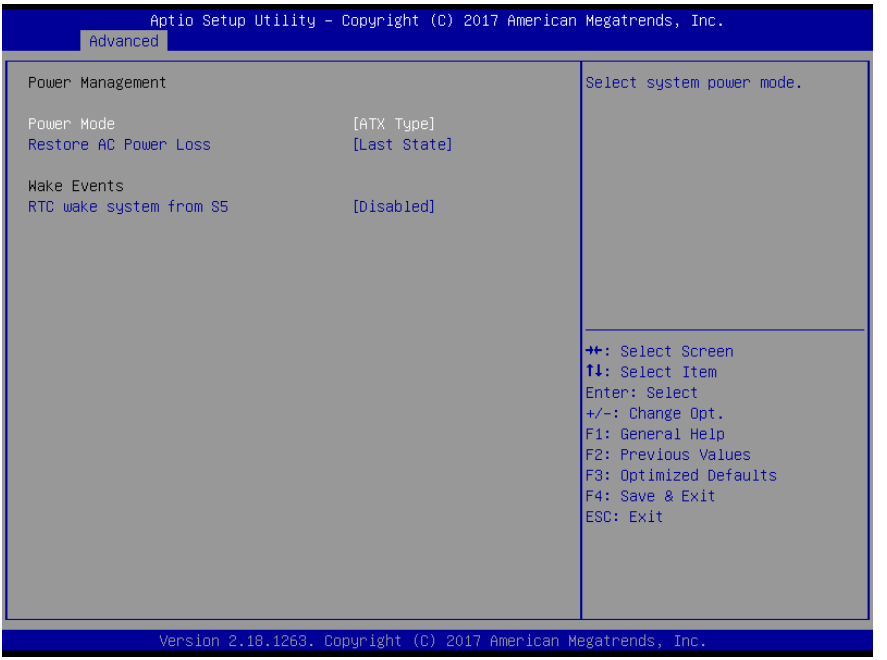
Options Summary		
DIO *	Output	
	Input	
Set DIO as Input or Output.		
Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output.		

3.4.6 Trusted Computing

Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank.		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank.		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. **NOTE**: Your Computer will reboot during restart in order to change State of Security Device.		

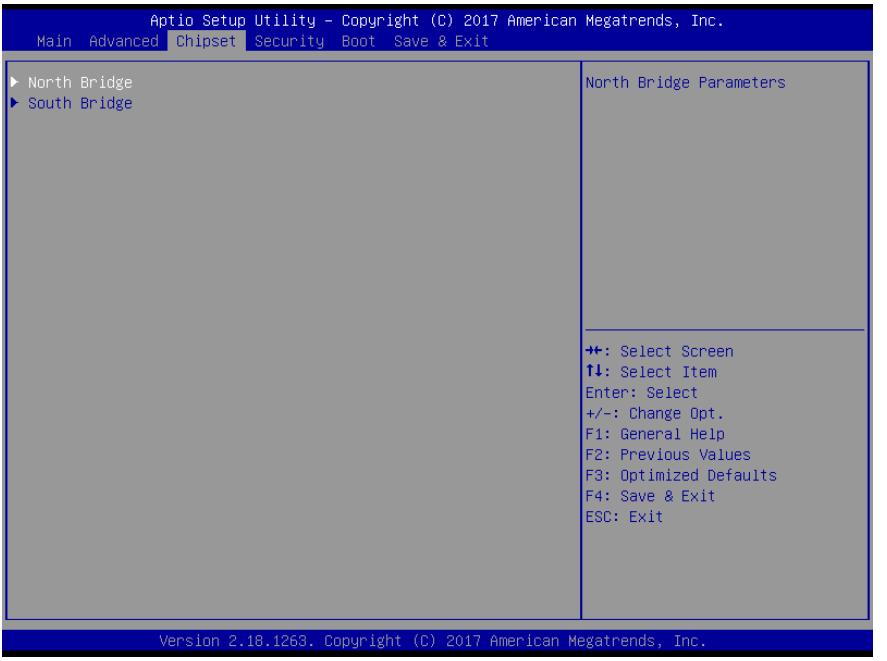
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy.		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy.		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy.		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support. TCG_1_2: The compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.7 Power Management

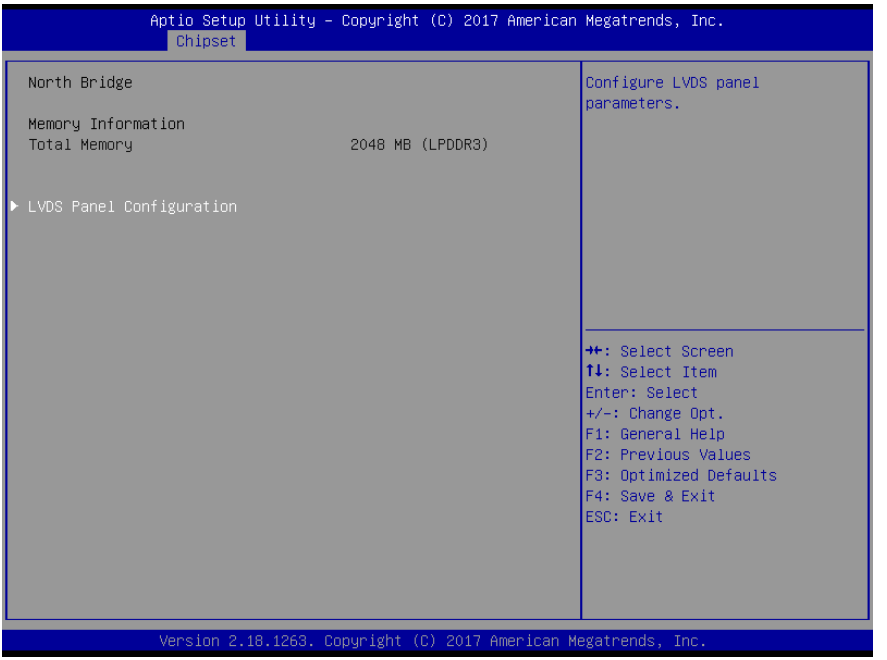


Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Determine if the system turns on or off after AC resume from G3 to S5 state.		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
RTC wake.		

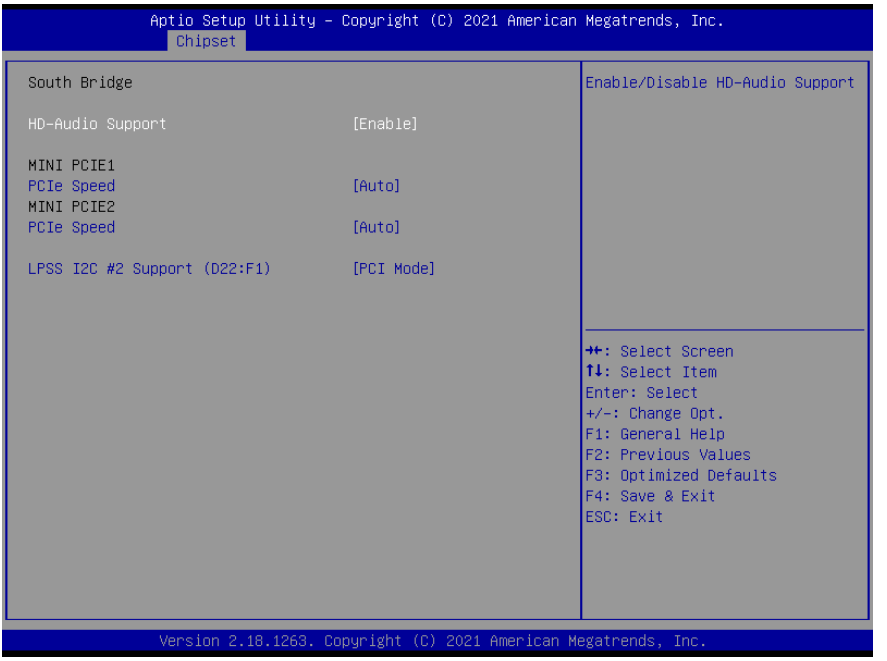
3.5 Setup Submenu: Chipset



3.5.1 North Bridge

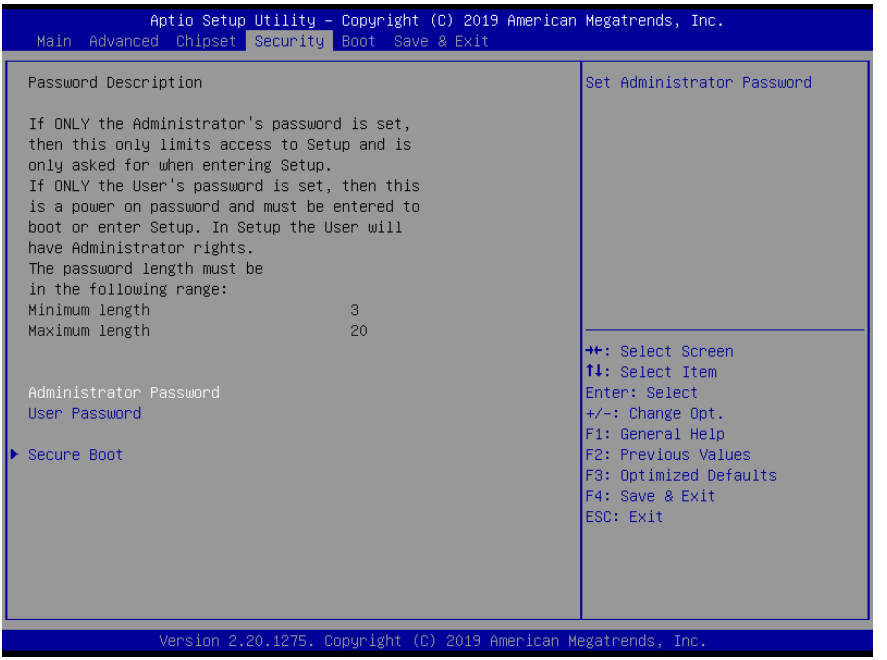


3.5.2 South Bridge



Options Summary		
HD-Audio Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/ Disabled HD audio.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe Speed.		
LPSS I2C #2 Support (D22:F1)	Disable	
	PCI Mode	Optimal Default, Failsafe Default
	ACPI Mode	
Enable/ Disable LPSS I2C #2 Support.		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

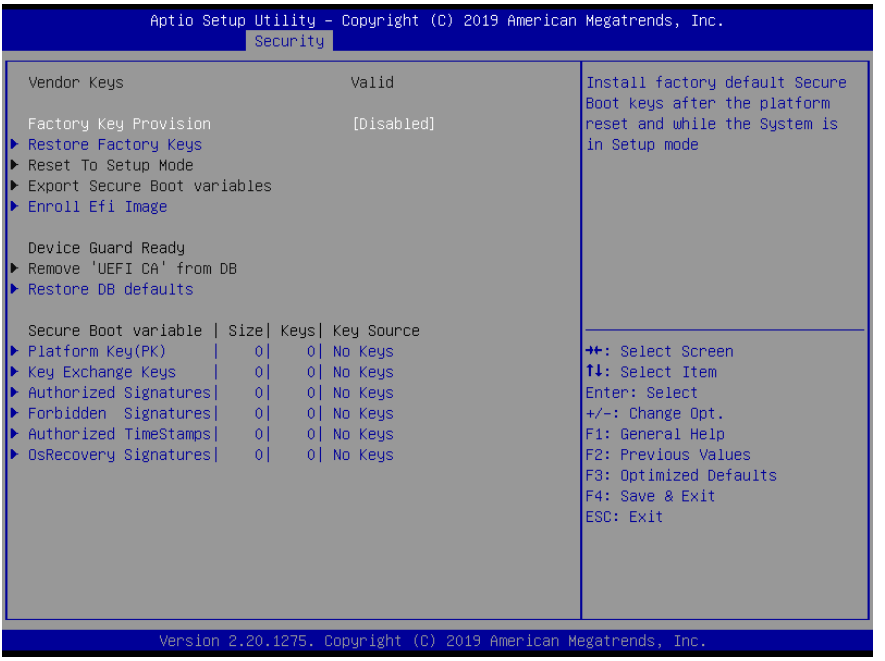
Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Reset to Setup Mode		
Delete all Secure Boot key databases from NVRAM.		

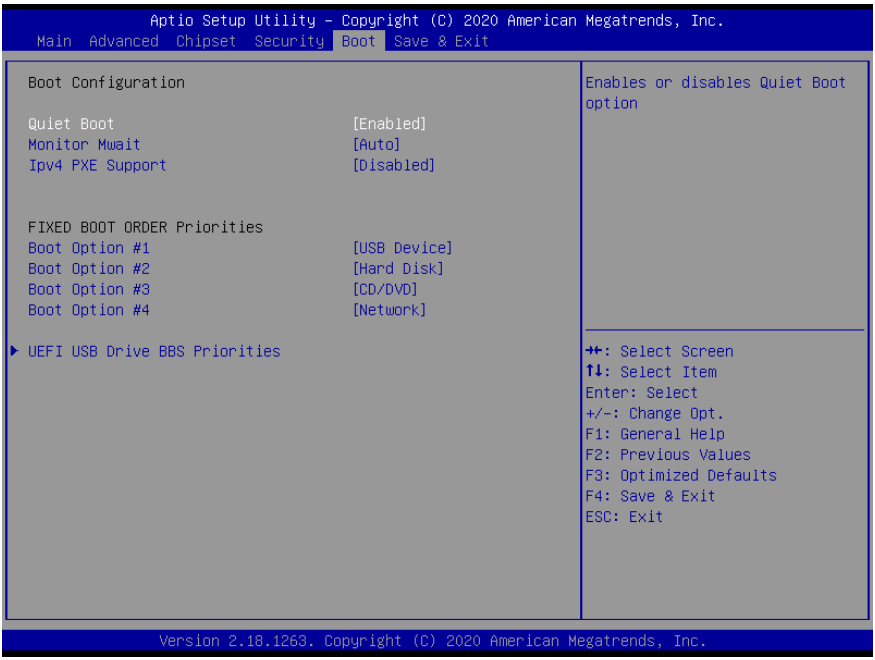
3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM.		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).		

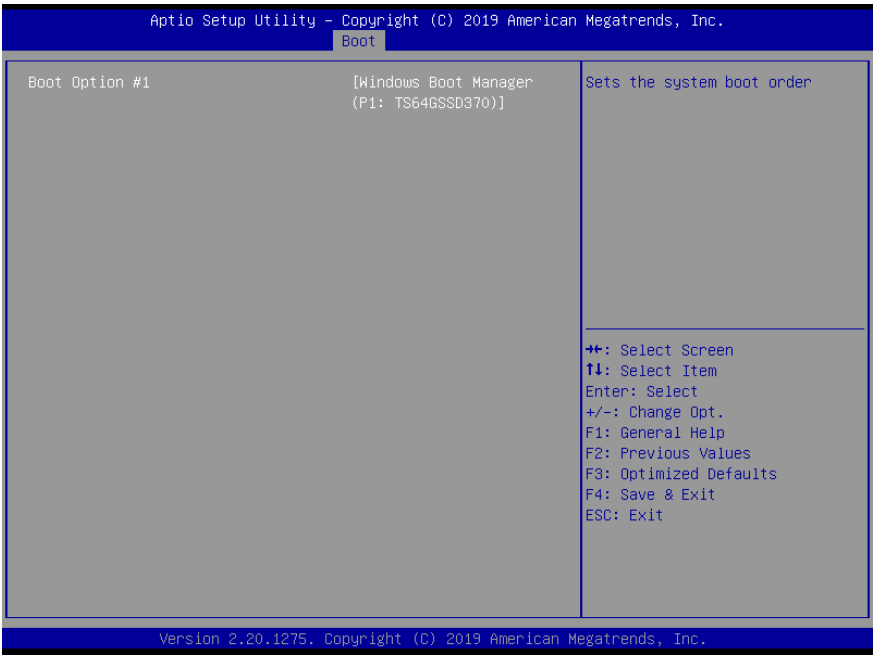
Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db).		
Restore DB defaults		
Restore DB variable to factory defaults.		
Platform Key(PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2. Authenticated UEFI Variable 3. EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed.		

3.7 Setup Submenu: Boot

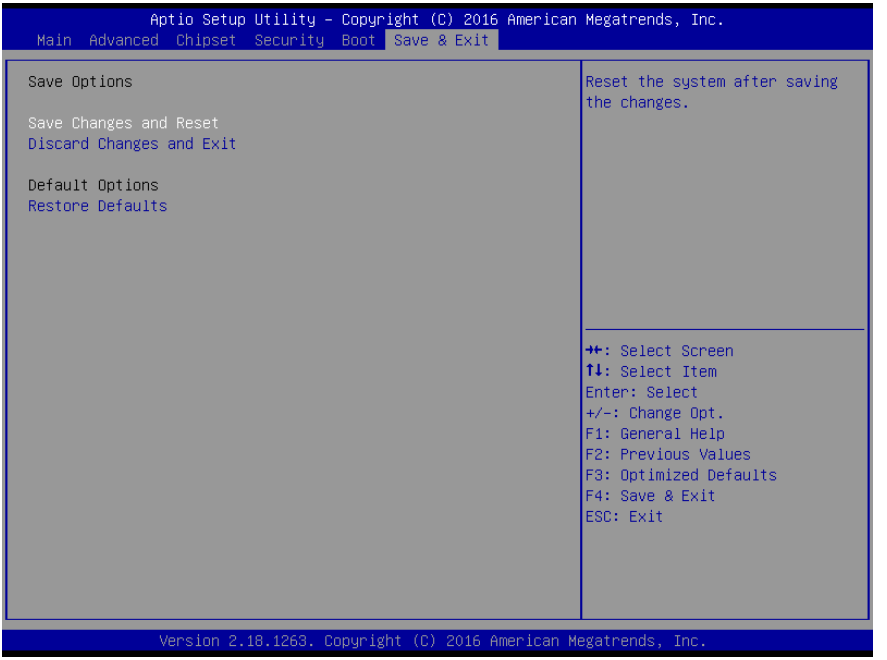


Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
EnableDisable showing boot logo.		
Monitor Mwait	Disable	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.7.1 BBS Priorities



3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the PICO-APL1-SEMI can be downloaded from the product page of the PICO-APL1 board level product on AAEON website by following this link:

https://www.aaeon.com/en/p/pico-itx-boards-pico-apl1#downloads

Download the driver(s) you need and follow the steps below to install them.

Install Chipset Driver

1. Open the **Chipset Driver** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Install Graphic Driver

1. Open the **Graphics Driver** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Install LAN Driver

1. Open the **LAN Driver** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Driver will be installed automatically

Install Audio Driver

1. Open the **Audio Driver** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Install TXE Driver

1. Open the **ME & TXE Driver** folder and open the **SetupTXE.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Install COM Port Driver

1. Open the **COM port Driver** folder and open the **FintekSerial.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Install Linux Peripheral Drivers

1. Open the **Linux Driver-Peripheral** folder
2. Follow the instructions provided in the **PICO-APL1 Linux Driver User Guide.pdf** document to manually install driver(s)

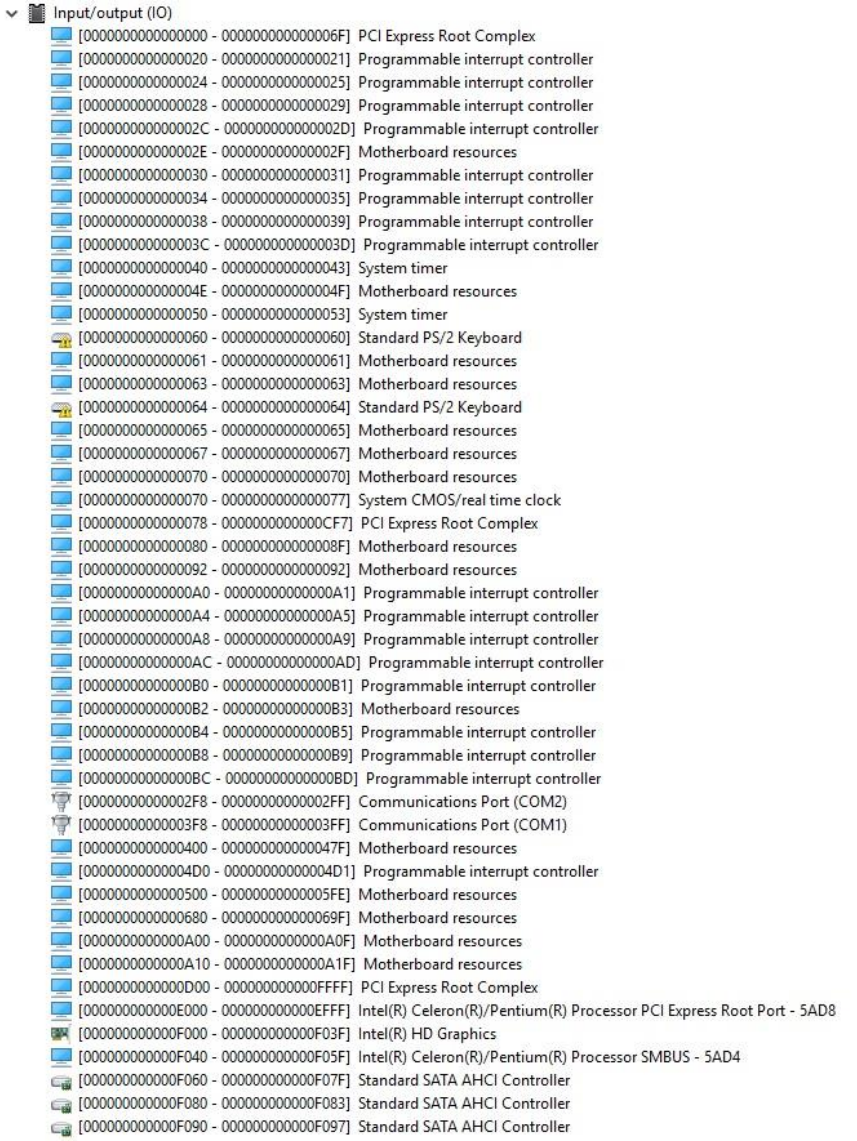
Install Serial IO Driver

1. Open the **Peripheral Driver** folder and open the **SetupSerialIO.exe** file
2. Follow the instructions
3. Driver will be installed automatically

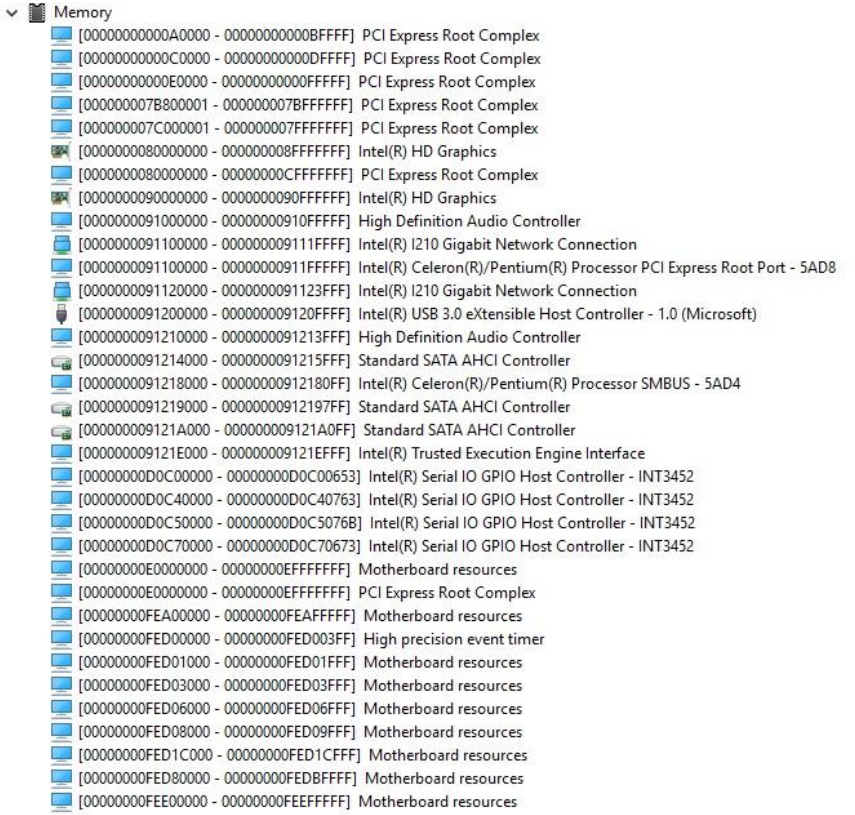
Appendix A

I/O Information

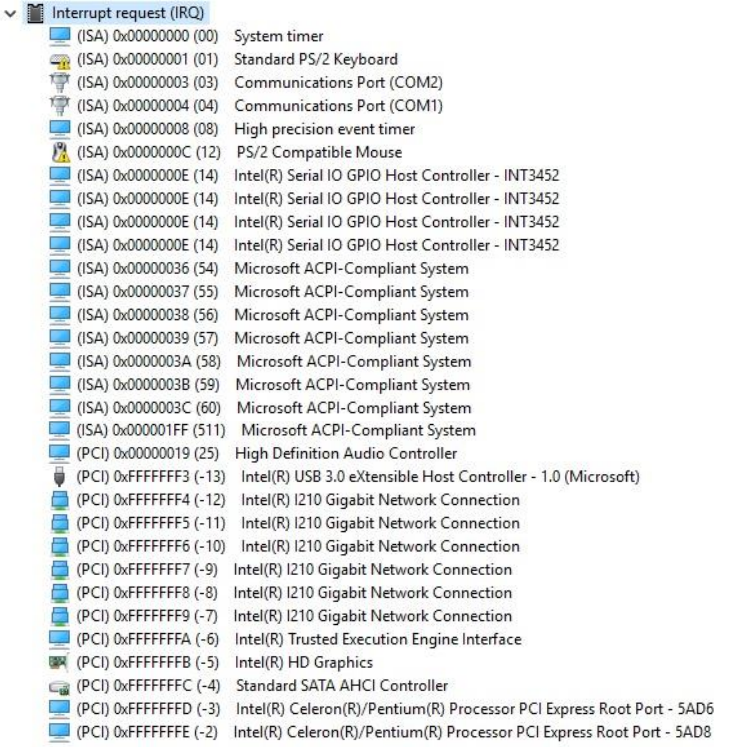
A.1 I/O Address Map



A.2 Memory Address Map



A.3 IRQ Mapping Chart



Appendix B

Mating Connectors

B.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN3	Front Panel Connector	Molex	51110-1050	Front Panel Cable	1701100156
CN8	SATA Port	Molex	887505318	SATA Cable	1709070500
CN9	Battery	Molex	51021-0200	Battery Cable	175011301C
CN12	+5V Output for SATA HDD	JST	PHR-2	SATA power cable	1702150155
CN14	External +12V Input	Molex	19211-0003	Power cable	170204010R
CN17	COM Port 1/2 & line out connector	HRS	DF14-20S-1.25C	COM Port 1/2 & line out cable	1703200052
CN18	LPC Port	JST	SHR-12V-S-B	AAEON LPC Cable	N/A
CN19	USB Connector	Molex	51021-0500	USB Cable	1700050207
CN20	LAN Connector	Molex	44915-0001	N/A	N/A