PICO-APL1

PICO-APL1 Single-Board Computer

User's Manual 1st Ed

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● PICO-APL1	1
● Product DVD with drivers	1
● Heat Spreader (optional)	1
● COM + Line-out Cable (optional)	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WHERE THE STORAGE TEMPERATURE IS BELOW -20° C (-4°F) OR ABOVE 60°C (140°F) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	PICO-APL1
Processor	Intel® Pentium Processor N4200 Intel® Celeron Processor N3350
System Memory	204-pin DDR3L 1600/1333MHz SODIMM x 1, max up to 8 GB
Chipset	Intel® Pentium N4200/Celeron N3350 integrated
BIOS	AMI / SPI
Wake On LAN	Yes
Watchdog Timer	255 levels
Power Requirement	DC 12 V
Power Supply Type	AT/ATX (default). lockable connector optional
System Cooling	Head spreader & Heatsink (optional)
Board Size	100 x 72 mm (3.94 x 2.84")
Gross Weight	200 g (0.44 .lb)
Operating Temperature	0 ~ 60°C (32 ~ 140°F)
Storage Temperature	-40 ~ 80°C (-40 ~176°F)
Operation Humidity	0 ~ 90% relative humidity, non-condensing

Display

● Chipset	Intel® Pentium N4200/Celeron N3350 integrated graphic
● Resolution	LVDS (18/24bit 2CH) 1920 x 1200 HDMI up to 3840 x 2160 DDI (BIO)
● LCD Interface	LVDS (18/24bit) up to 1920 x1200@ 60Hz [select by BIOS or jumper] HDMI up to 3840 x 2160 @ 30Hz; Or DDI (by BIO Board optional)

I/O

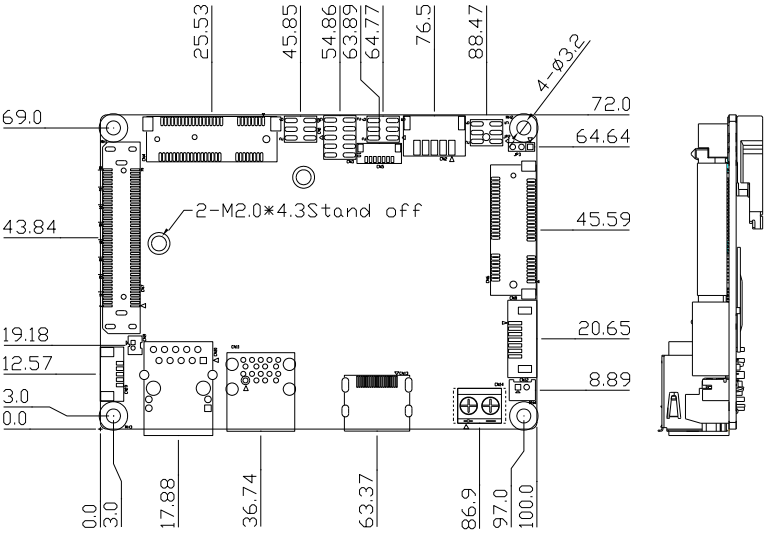
● Storage	SATA 6.0Gb/s x 1, mSATA(Default)/MiniCard x 1
● Ethernet	HD Audio Codec (RealteK ALC892)
● USB	USB 3.0 x 2, USB 2.0 x 1
● Serial Port	RS-232 x 1 RS-232/422/485 x 1 (Ring / +5V / +12V)
● Audio	Line-out x 1
● DI/O	4-bit programmable (2-in/ 2-out)
● Expansion Slot	Mini Card(Half-size) x 1, BIO x 1, (Optional) I2C x 1 or Smbus x 1

Chapter 2

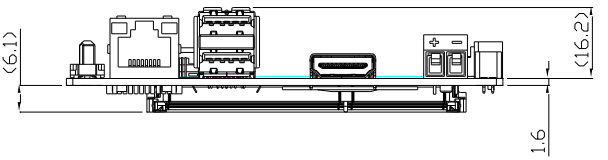
Hardware Information

2.1 Dimensions

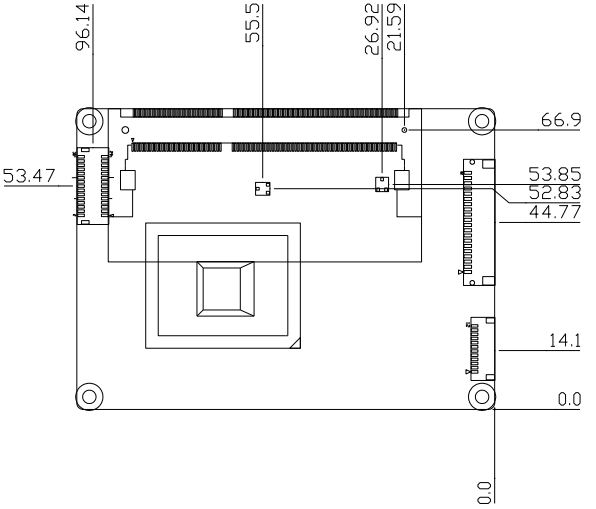
Component Side



Component Side

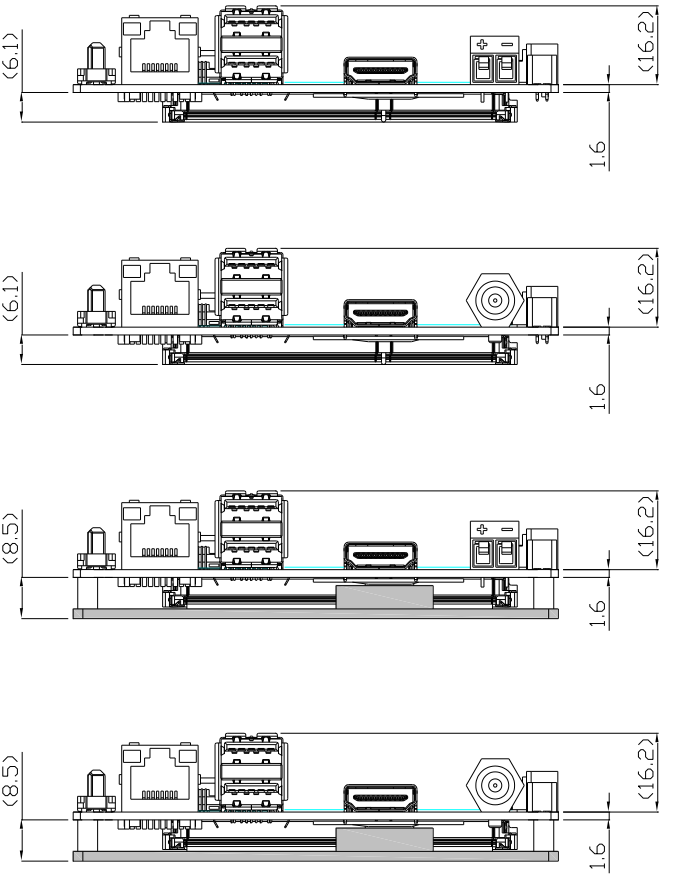


Solder Side



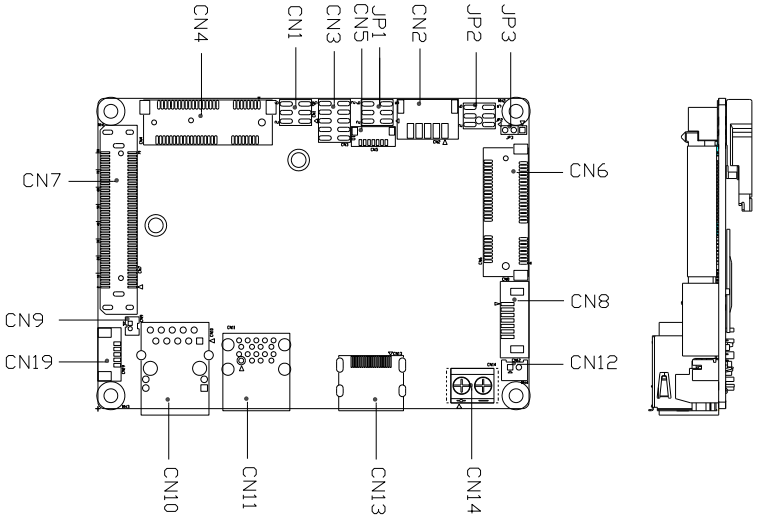
Solder Side

Rear I/O Configuration

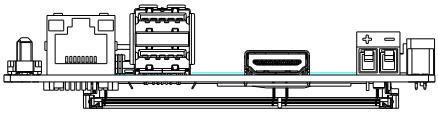


2.2 Jumpers and Connectors

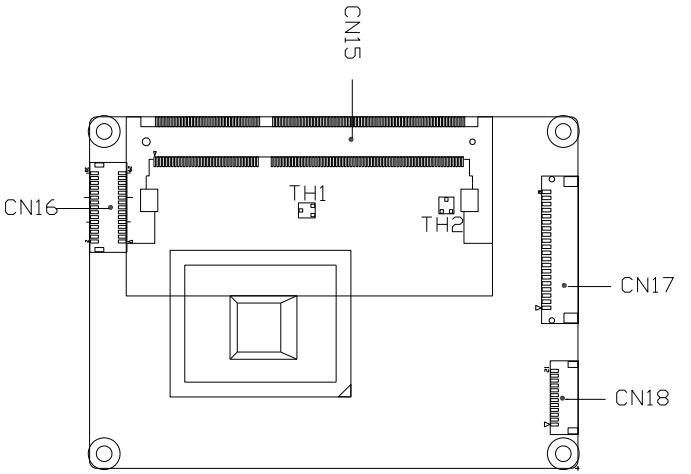
Component Side



Component Side



Solder Side



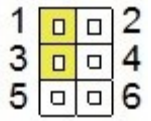
Solder Side

2.3 List of Jumpers

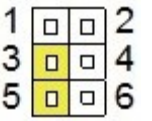
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1(1,3,5)	Clear CMOS Jumper
JP1(2,4,6)	Auto Power Button Enable/Disable Selection
JP2(1,3,5)	LVDS Port Operating Voltage Selection
JP2(2,4,6)	LVDS Port Backlight Inverter Voltage Selection
JP3	LVDS Port Backlight Lightness Control Mode Selection

2.3.1 Clear CMOS Jumper (JP1 1, 3, 5)

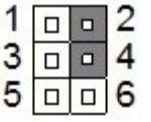


Normal (Default)

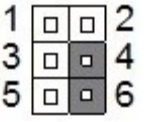


Clear CMOS

2.3.2 Auto Power Button Enable/Disable Selection (JP1 2, 4, 6)

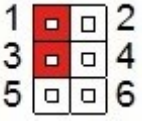


Enable (Default)

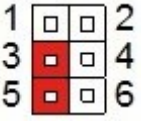


Disable

2.3.3 LVDS Port Operating Voltage Selection (JP2 1,3,5)

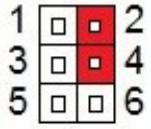


+5V

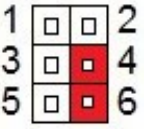


+3.3V (Default)

2.3.4 LVDS Port Backlight Inverter Voltage Selection Selection (JP2 2,4,6)

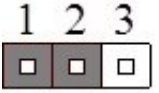


+12V

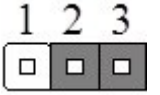


+5V (Default)

2.3.5 LVDS Port Backlight Lightness Control Mode (JP3)



VR Mode (Default)



PWM Mode

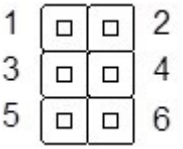
2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	Digital IO Port
CN2	LVDS Port Inverter / Backlight Connector
CN3	Front Panel
CN4	Mini-Card Slot (Half-Mini Card)
CN5	SPI Programming Header
CN6	Mini-Card Slot (Full-Mini Card)/mSATA (By BOM)
CN7	BIO connector
CN8	SATA Port
CN9	Battery
CN10	LAN (RJ-45) Port
CN11	USB 3.0 Port 1,2
CN12	+5V Output for SATA HDD
CN13	HDMI port
CN14	External +12V Input
CN15	DDR3L SO-DIMM Slot
CN16	LVDS Port

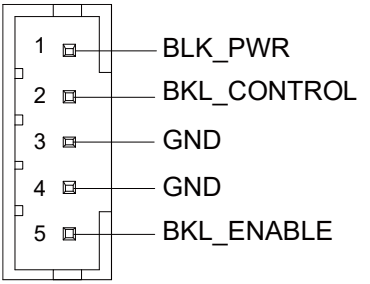
CN17	COM Port 1/2 & line out connector
CN18	LPC Port
CN19	USB 2.0 Port 1

2.4.1 Digital IO Port (CN1)



Pin	Pin Name	Signal Type	Pin Name
1	+5V	PWR	+5V
2	DIO0	I/O	+5V
3	DIO1	I/O	+5V
4	DIO2	I/O	+5V
5	DIO3	I/O	+5V
6	GND	GND	

2.4.2 LVDS Port Inverter / Backlight Connector (CN2)



Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V

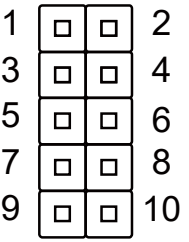
Pin	Pin Name	Signal Type	Signal level
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

※ LVDS/BKL_PWR can be set to +5V or +12V by JP2.

※ LVDS/BKL_CONTROL can be set by JP3.

※ The driving current supports up to 2A.

2.4.3 Front Panel (CN3)



Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

2.4.4 Mini-Card Slot (Half-Mini Card) (CN4)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		

20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	

41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

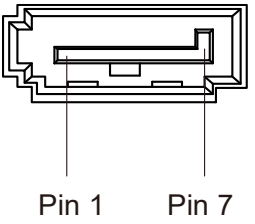
2.4.5 BIO connector (CN7)

Pin	Pin Name	Pin	Pin Name
1	+12VSB	2	GND
3	GND	4	PCIE_TXN0
5	PCIE_RXN0	6	PCIE_TXP0
7	PCIE_RXP0	8	GND
9	GND	10	NC
11	NC	12	NC

Pin	Pin Name	Pin	Pin Name
13	NC	14	GND
15	GND	16	PS_ON#
17	NC	18	NC
19	+5VSB	20	+5VSB
21	+5VSB	22	+5VSB
23	PCIE_REF_CLK0	24	RESET#
25	PCIE_REF_CLK0#	26	GND
27	GND	28	NC
29	NC	30	NC
31	NC	32	GND
33	GND	34	NC
35	NC	36	NC
37	NC	38	GND
39	GND	40	NC
41	NC	42	GND
43	NC	44	NC
45	GND	46	NC
47	USBN0	48	GND
49	USBP0	50	USBN1
51	GND	52	USBP2

Pin	Pin Name	Pin	Pin Name
53	SMB_CLK	54	GND
55	SMB_DATA	56	WAKE#
57	GND	58	USB_OC0#
59	+5V	60	USB_OC1#
61	+5V	62	+5V
63	+5V	64	+5V
65	LPC_AD0	66	LPC_FRAME#
67	LPC_AD1	68	SERIRQ
69	LPC_AD2	70	LPC_DRQ
71	LPC_AD3	72	GPIO0
73	GND	74	AGND
75	LPC_CLK	76	AUD_LINEOUT_L
77	PME#	78	AUD_LINEOUT_R
79	GND	80	GND

2.4.6 SATA Port (CN8)

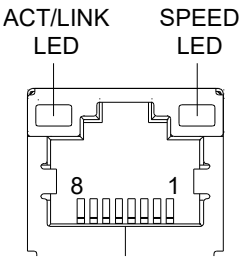


Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX1+	DIFF	
3	SATA_TX1-	DIFF	
4	GND	GND	
5	SATA_RX1-	DIFF	
6	SATA_RX1+	DIFF	
7	GND	GND	

2.4.7 Battery (CN9)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.8 LAN (RJ-45) Port (CN10)



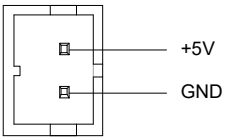
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.4.9 USB3.0 Ports 0 and 1 (CN11)

Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V

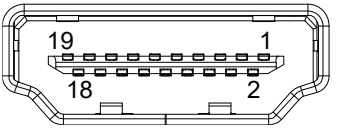
11	USB1_D-	DIFF
12	USB1_D+	DIFF
13	GND	GND
14	USB1_SSRX–	DIFF
15	USB1_SSRX+	DIFF
16	GND	GND
17	USB1_SSTX–	DIFF
18	USB1_SSTX+	DIFF

2.4.10 +5V Output for SATA HDD (CN12)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

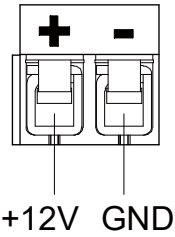
2.4.11 HDMI Port (CN13)



Pin	Pin Name	Signal Type	Signal level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V

Pin	Pin Name	Signal Type	Signal level
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.4.12External +12V Input (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	+121V	PWR	+12V
2	GND	GND	

2.4.13DDR3L SO-DIMM Slot (CN15)

Standard specification

2.4.14LVDS Port (CN16)

※ LVDS LCD_PWR can be set to +3.3V or +5V by JP2

※ The max. driving current is 2A.

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	

2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	

23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.4.15COM Port 1/2 & line out connector (CN17)

Pin	Pin Name	Signal Type	Signal Level
1	DCDB	IN	
2	DSRB	IN	
3	RXB	IN	
4	RTSB	OUT	±9V
5	TXB	OUT	±9V
6	CTSB	IN	
7	DTRB	OUT	±9V
8	RIB/+5V/+12V	IN/ PWR	+5V/+12V

Pin	Pin Name	Signal Type	Signal Level
9	DCDA	IN	
10	DSRA	IN	
11	RXA	IN	
12	RTSA	OUT	±9V
13	TXA	OUT	±9V
14	CTSA	IN	
15	DTRA	OUT	±9V
16	RIA	IN	
17	GND	GND	
18	AGND	GND	
19	LOUT_R	I/O	
20	LOUT_L	I/O	

2.4.16COM port2 RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		

6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
17	GNDGND	IN	

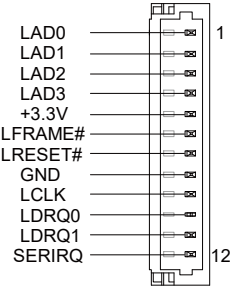
2.4.17COM port2 RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

※ COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

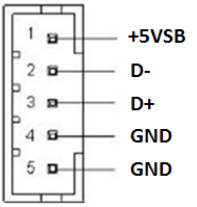
※ COM2 RI/+5V/+12V function can be set by BOM(R248-RI/R256-+12V/R250-+5V)

2.4.18LPC port2 (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.4.19USB 2.0 Port 1 (CN19)



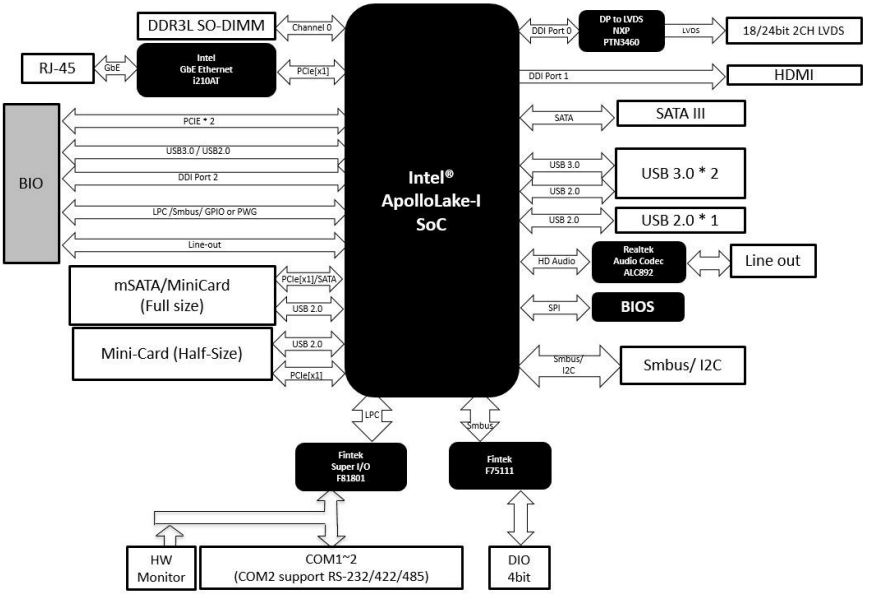
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USBD5-	DIFF	
3	USBD5+	DIFF	
4	GND	GND	
5	GND	GND	

2.4.20 Specifications for I/O Port

I/O	Reference	Signal Name	Rate Output
Digital IO Port	CN1	D0~D3	+5V/(Open drain)
LVDS Port Inverter / Backlight Connector	CN2	VDD	+5V/2A or +12V/2A
Mini-Card Slot	CN4	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
Mini-Card Slot	CN6	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
USB 3.0 Port 1 & 2	CN10	+5VSB	+5VSB/1A (per channel)
+5V Output for SATA HDD	CN12	+5V	+5V/1A
LVDS Port	CN16	VCC	+3.3V/2A or +5V/2A

COM Port 2	CN17	+5V/+12V	+5V/1A or +12V/1A
LPC Port	CN18	+3.3V	+3.3V/0.5A
USB 2.0 Port 1	CN19	+5VSB	+5VSB/0.5A

2.4.21 Function Block



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PICO-APL1 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

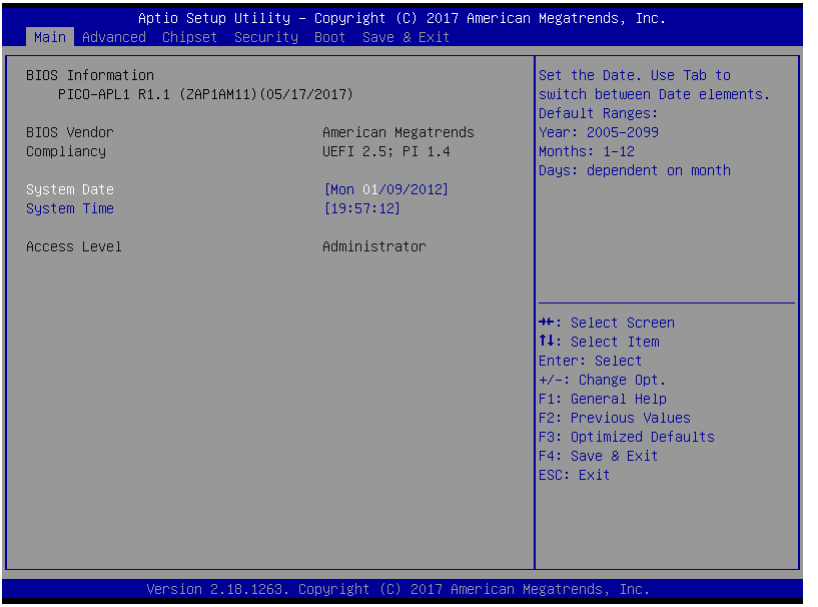
Set setup administrator password.

Save & Exit

Exit system setup after saving the changes.

3.3 Setup Submenu: Main

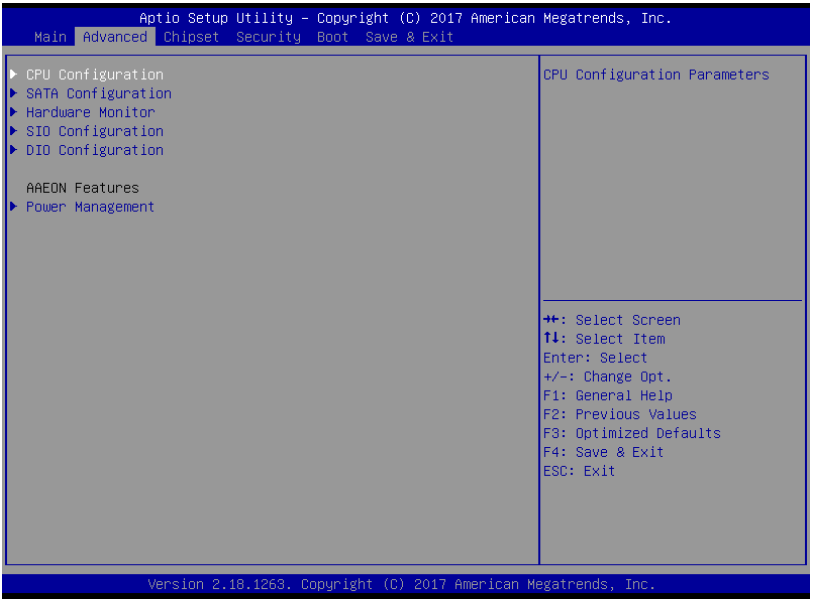
Press "Delete" to enter Setup



Options summary: (***default setting***)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

3.4 Setup Submenu: Advanced

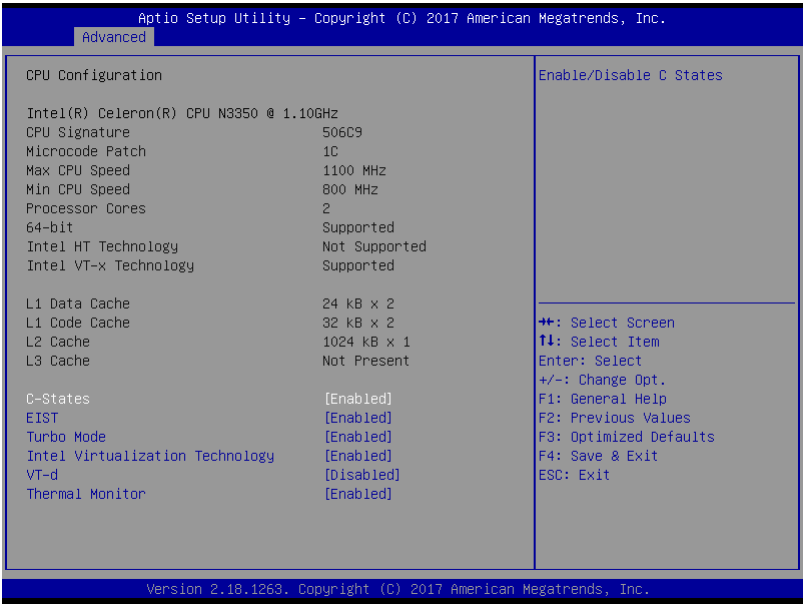


Options summary: (***default setting***)

CPU Configuration		
CPU Configuration Parameters		
SATA Configuration		
SATA Device Configuration		
USB Configuration		
USB Configuration Parameters		
SIO Configuration		
SIO Chip configuration .Enable or Disable SIO Logical Devices, Resources and Features settings, etc.		
Hardware Monitor		

Power Management		
System ACPI/Power Mode/Wake Event Configuration		
Digital IO Port Configuration		
Set Input/Output of digital Port Configuration		

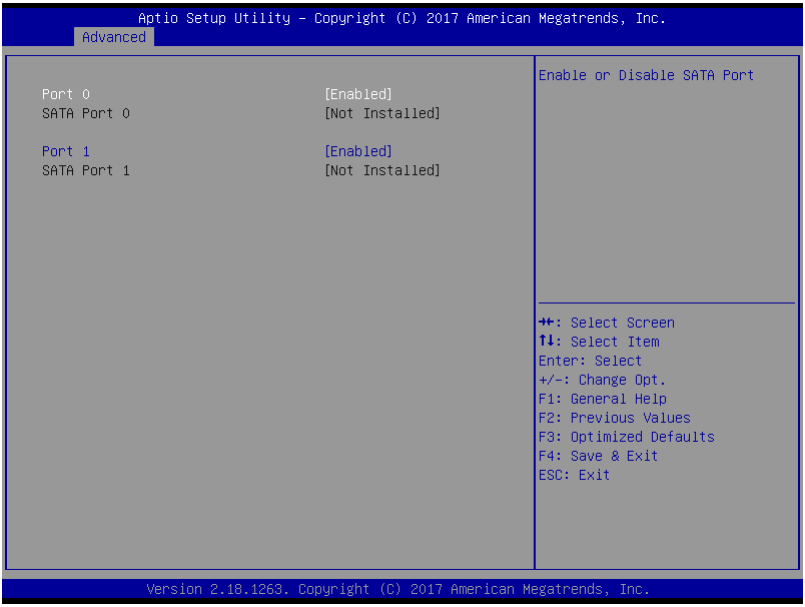
3.4.1 CPU configuration



Options summary:

C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU VT-d		
Thermal Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Thermal Monitor		

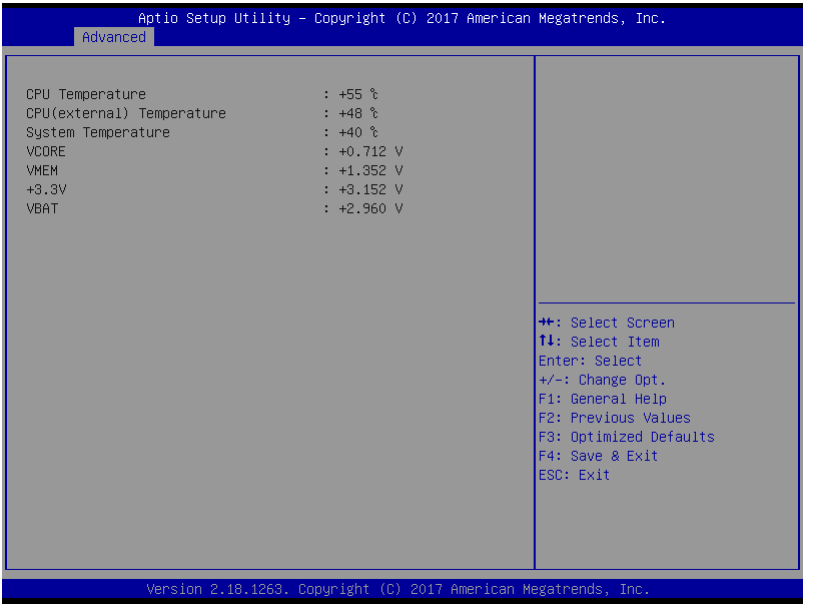
3.4.2 SATA Configuration



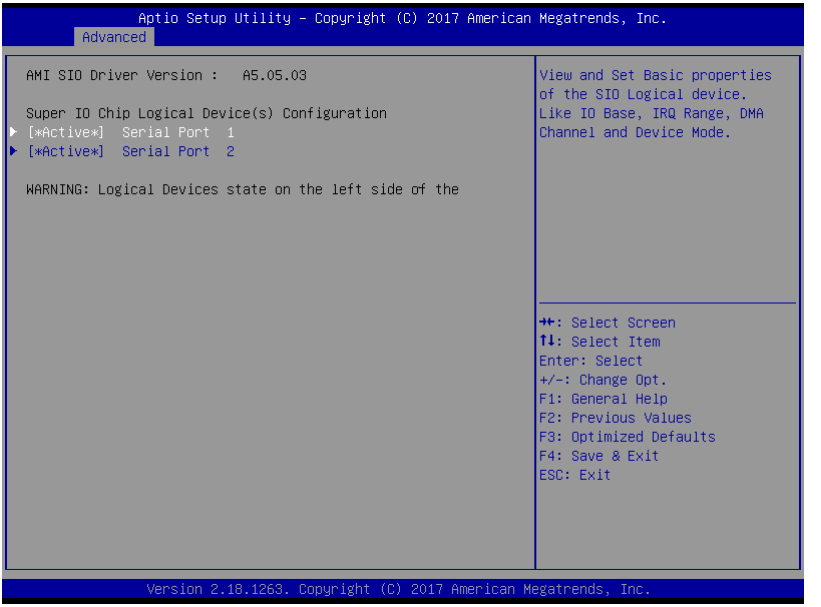
Options summary:

Port 0/1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA port		

3.4.3 Hardware Monitor



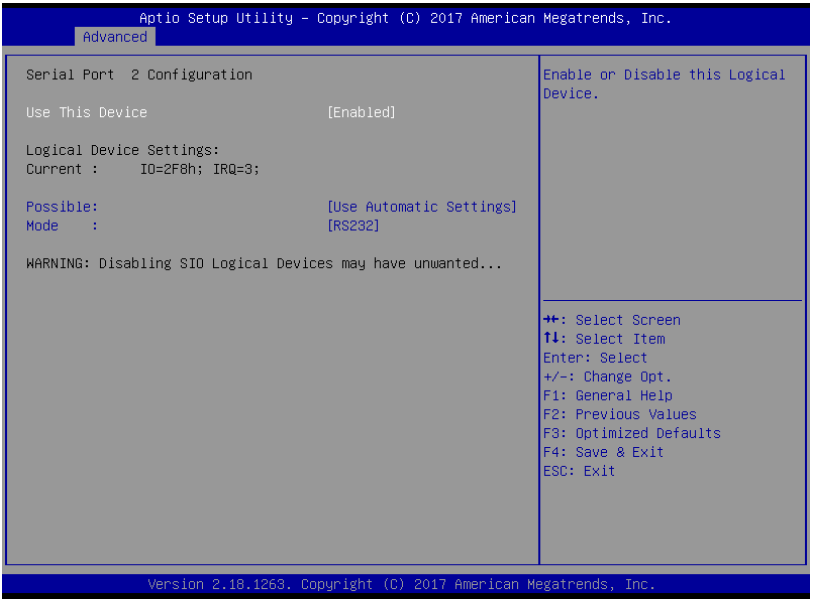
3.4.4 SIO Configuration



Options summary: (***default setting***)

Serial Port 1/2 Configuration		
View and Set Basic properties of the SIO Logical device. Like IO Base , IRQ Range , DMA Channel and Device Mode.		

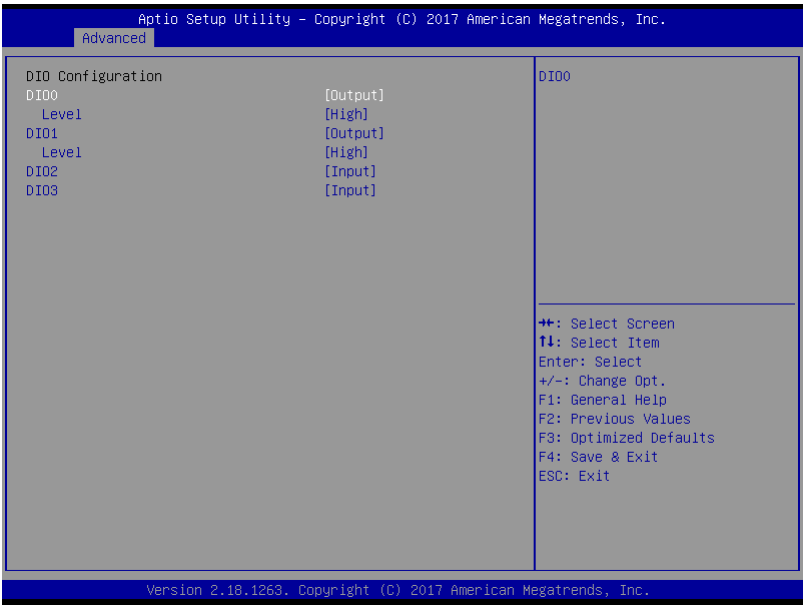
3.4.4.1 Serial Port Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

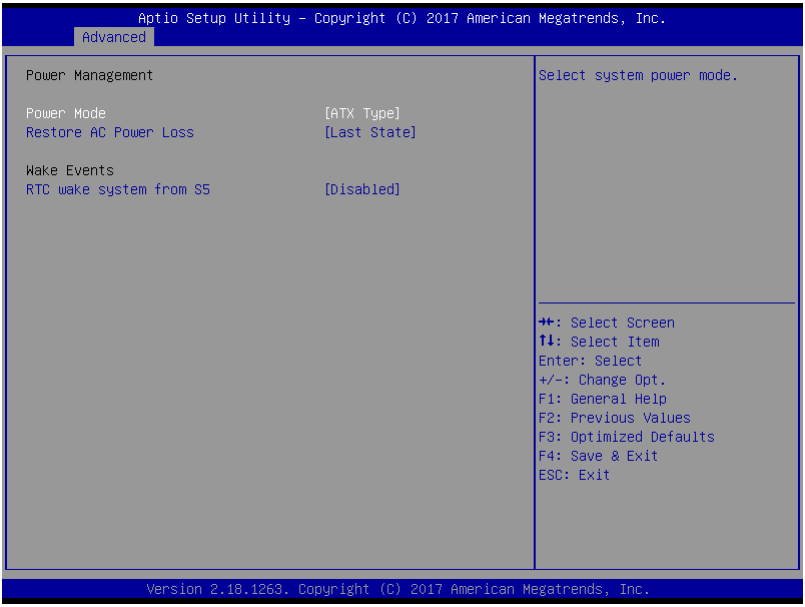
3.4.5 Dio Configuration



Options summary:

DIO *	Output	
	Input	
Set DIO as Input or Output		
Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

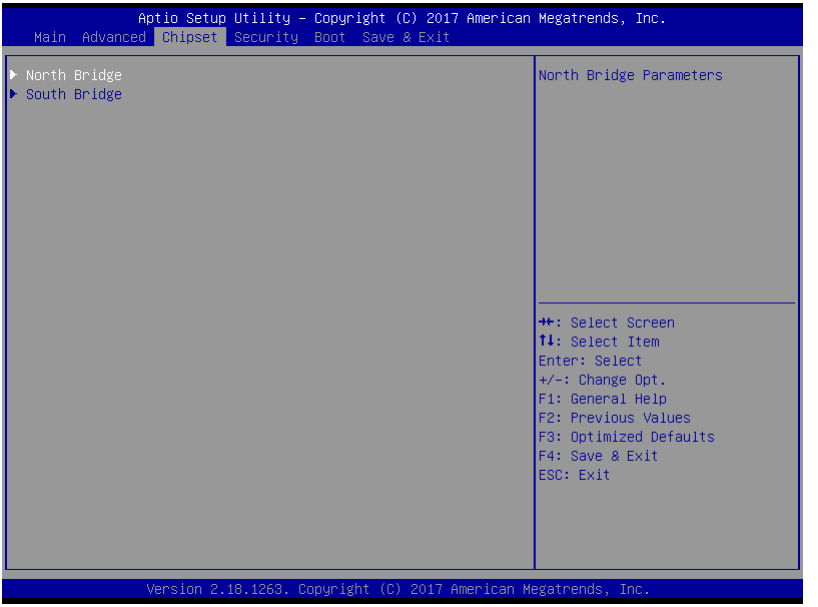
3.4.6 Power Management



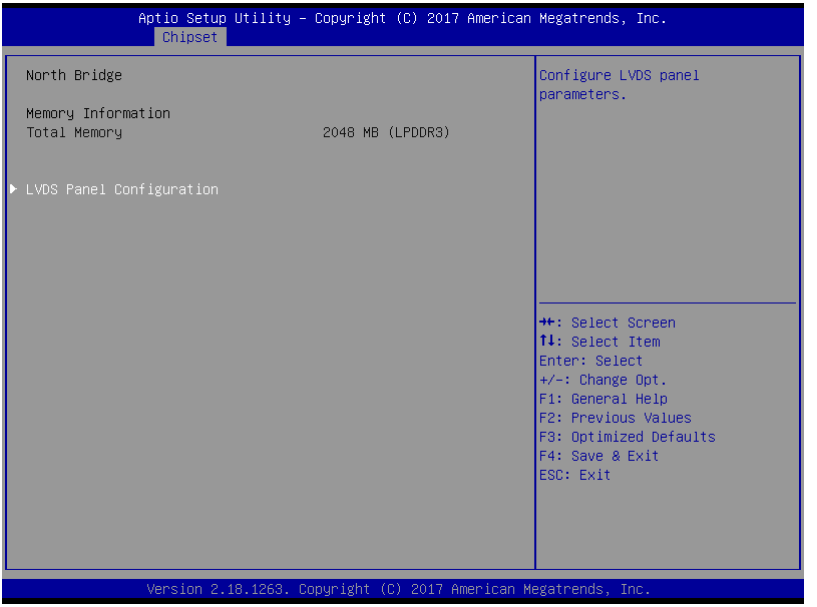
Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
RTC wake		

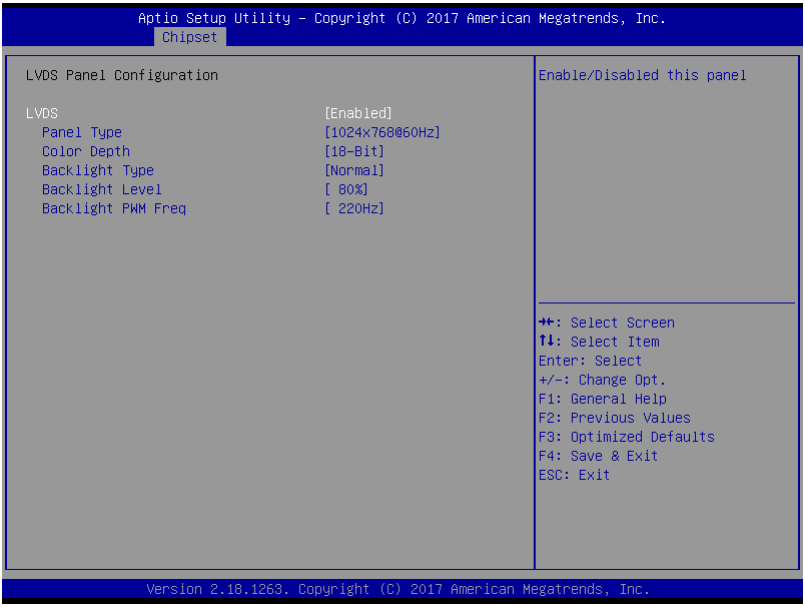
3.4.7 Setup submenu: Chipset



3.4.8 North Bridge



3.5 LVDS Panel Configuration



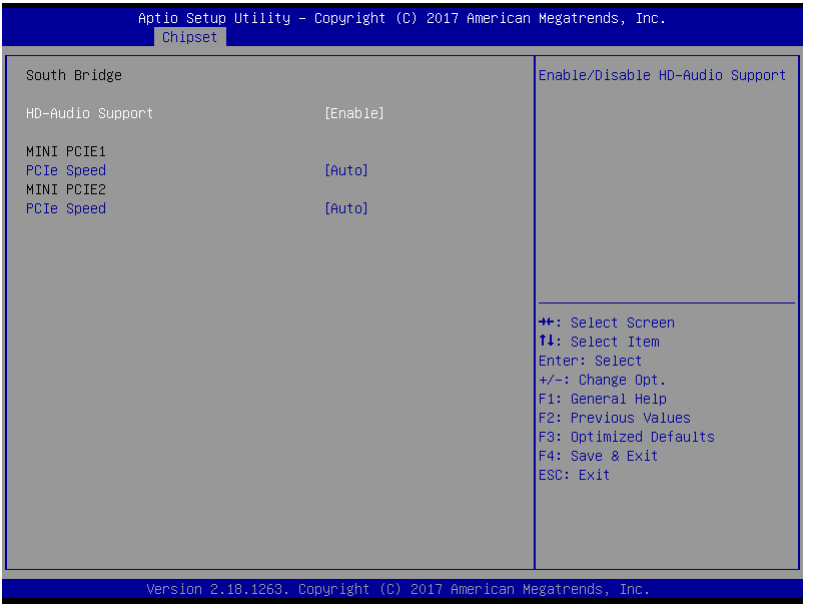
Options summary:

LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled this panel.		
LVDS Panel Type	640X480@60HZ	
	800X480@60HZ	
	800X600@60HZ	
	1024X600@60HZ	
	1024X768@60HZ	Optimal Default, Failsafe Default
	1280X768@60HZ	
	1280X800@60HZ	
	1280X1024@60HZ	

	1366X768@60HZ	
	1440X900@60HZ	
	1600X1200@60HZ	
	1920X1080@60HZ	
	1920X1200@60HZ	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	Optimal Default, Failsafe Default
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1.1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

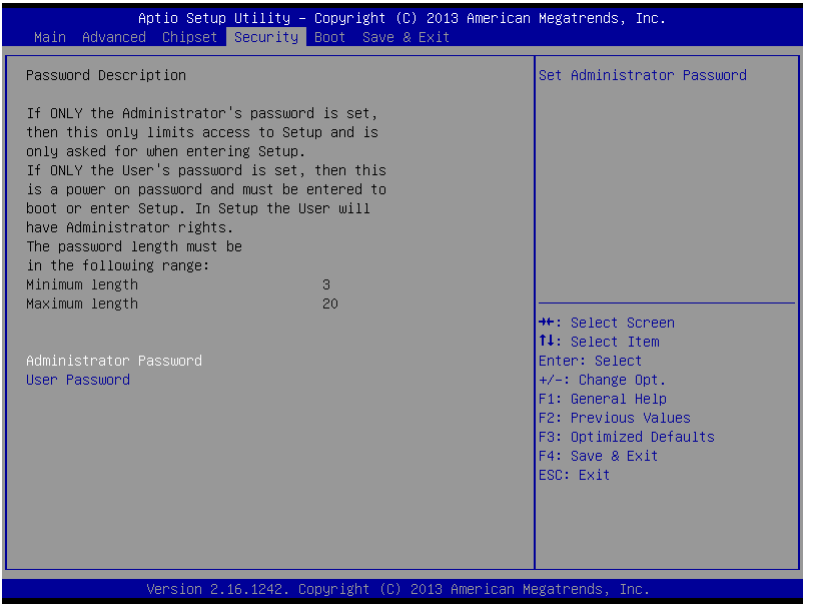
3.5.1 South Bridge



Options summary:

HD-Audio Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled HD audio		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe Speed		

3.5.1.1 Setup submenu: Security



Change User/Supervisor Password

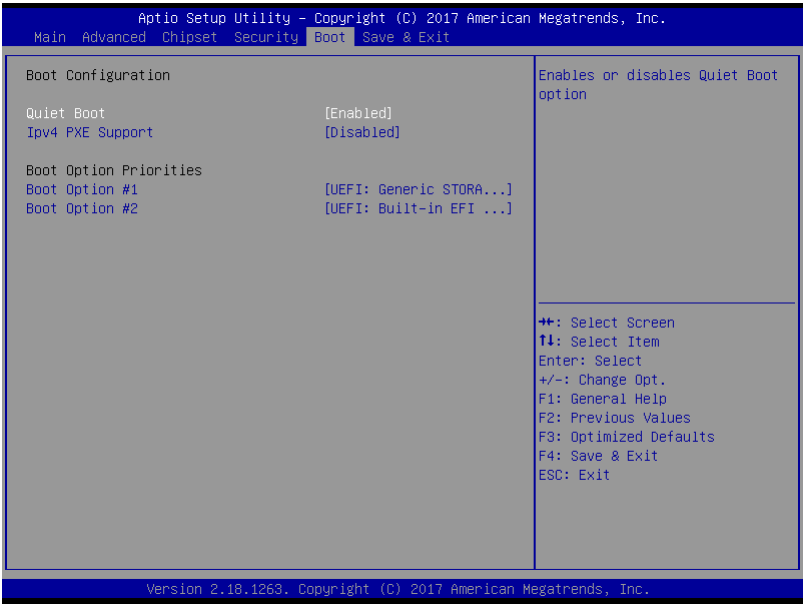
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

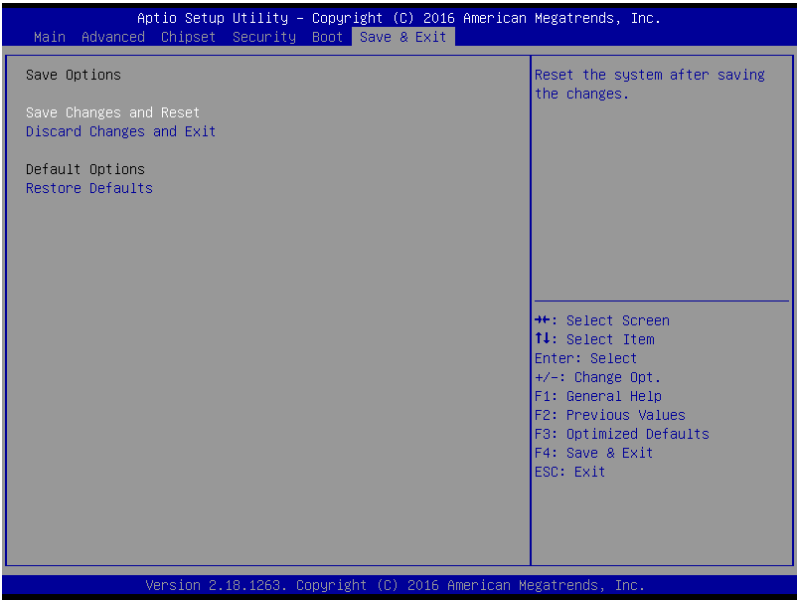
3.5.2 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
EnableDisable showing boot logo.		
Monitor Mwait	Disable	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.6 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The PICO-APL1 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **STEP1 - CHIPSET** folder and open the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **STEP2 - VGA** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 3 – Install LAN Driver

1. Open the **STEP3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Driver will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - AUDIO** folder and open the **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 5 – Install TXE Driver

1. Open the **STEP5 - TXE** folder and open the **SetupTXE.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 6 – Install FintekSerial_Patch_T4R8 Driver

1. Open the **STEP6-FintekSerial_Patch_T4R8** folder and open the **Setup.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Step 7 – Install GPIO Driver

1. Open the **STEP7 - GPIO** folder and open the **SetupSerialIO.exe** file
2. Follow the instructions
3. Driver will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0x2E	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s *Pulse width is must longer then 16ms.*
Signal Polarity	0x05	2	0	0: low active 1: high active *Must set this bit to 0*
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse *Must set this bit to 1*
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg         0x00   // Device configuration register
     #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
     #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
     #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
     #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
     #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
     #define   PolarityVal    0x00     // Low active for WDTRST#
     #define   UnitBit        0x03     // Unit for timer (Bit3)
     #define   ModeBit        0x04     // WDTRST# mode (Bit4)
     #define   ModeVal        0x01     // 0:level 1: pulse
     #define   EnableBit      0x05     // WDT timer enable (Bit5)
     #define   EnableVal      0x01     // 1: enable
     #define   StatusBit      0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*****************************************************************************

*****************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        EnterSIOconfig();
        SetWDT();
        AaeonWDTConfig(Counter, Unit);
        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
        ExitSIOconfig();
}
*****************************************************************************
```

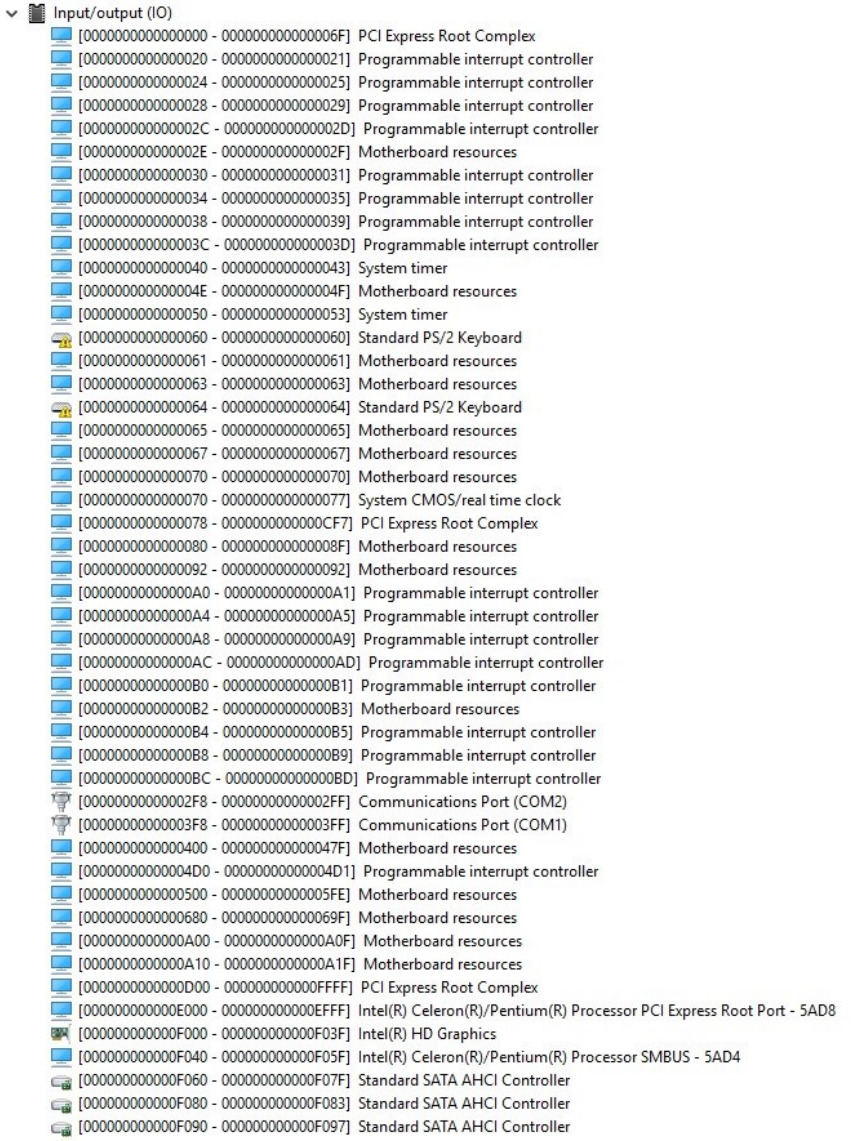
```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    EnterSIOconfig ( ){
          IOWriteByte (IoConfAddr,0x87);
          IOWriteByte (IoConfAddr,0x87);
}

VOID    ExitSIOconfig ( ){
          IOWriteByte (IoConfAddr,0xAA);
}

VOID    SetWDT ( )
          IOWriteByte (IoConfAddr,0x2B);
          IOWriteByte(IoConfAddr+1, (IOReadByte(IoConfAddr+1)&0xFC));
}

// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
          WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
          // Disable WDT counting
          WDTEnableDisable(0);
          // Clear Watchdog Timeout Status
          WDTClearTimeoutStatus();
          // WDT relative parameter setting
          WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
          If (Value == 1)
               WDTSetBit(TimerReg, EnableBit, 1);
          else
               WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
          // Watchdog Timer counter setting
          WDTWriteByte(CounterReg, Counter);
         // WDT counting unit setting
```

```
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
         // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
VOID    WDTWriteByte(byte Register, byte Value){
        IOWriteByte(WDTAddr+Register, Value);
}

byte    WDTReadByte(byte Register){
        return IOReadByte(WDTAddr+Register);
}

VOID    WDTSetBit(byte Register, byte Bit, byte Val){
        byte TmpValue;

        TmpValue = WDTReadByte(Register);
        TmpValue &= ~(1 << Bit);
        TmpValue |= Val << Bit;
        WDTWriteByte(Register, TmpValue);
}

*****************************************************************************
```

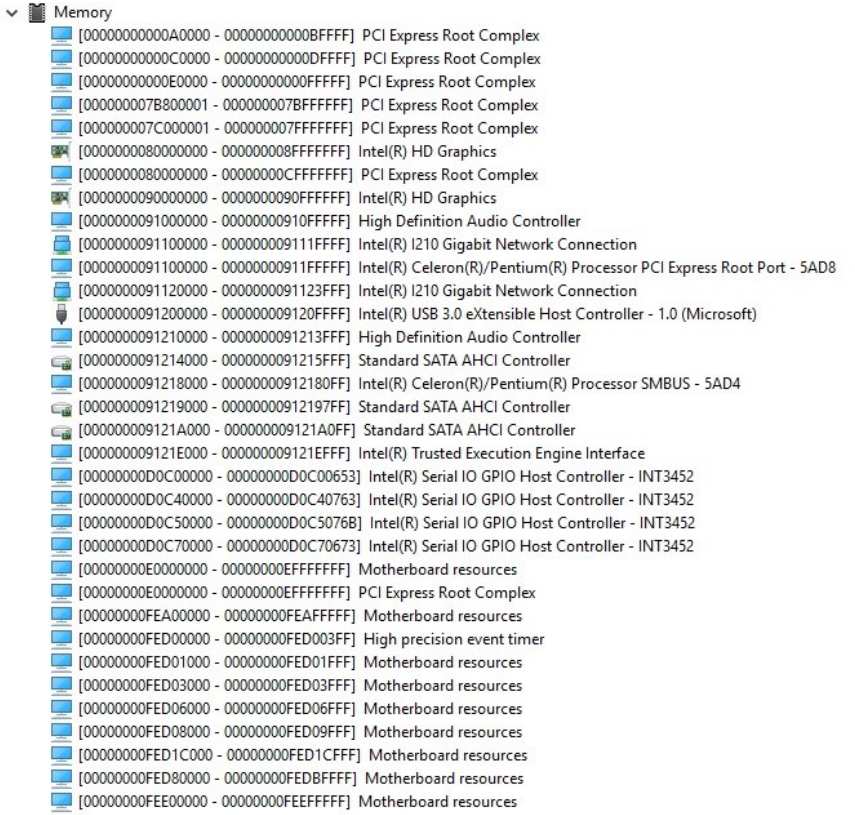
Appendix B

I/O Information

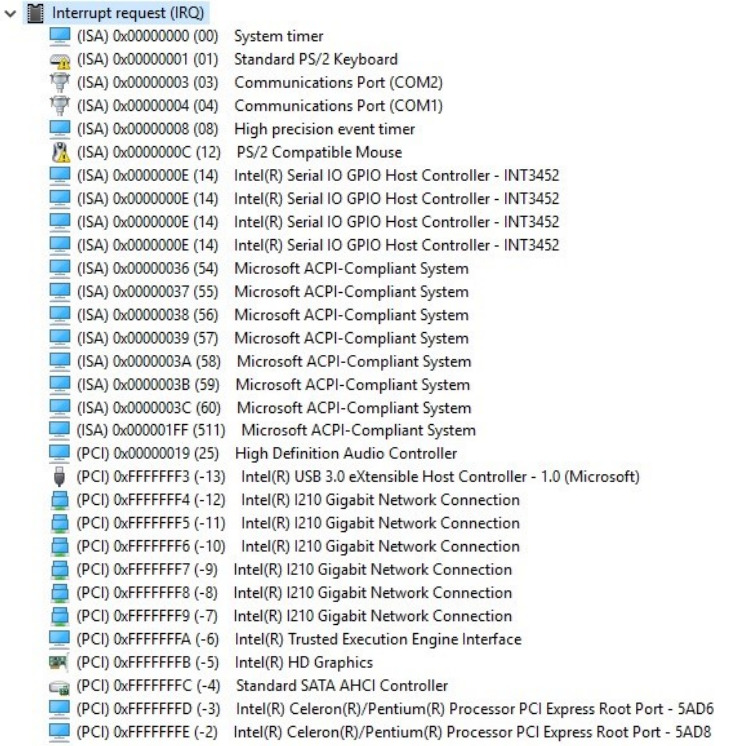
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Function	Description	Mating Connector Vendor	Vendor P/N	Pin No.	AAEON P/N	Mating Cable P/N
HDMI	1 x HDMI	FOXCONN	QJ51191-LFB4-7F	19	1654401932	N/A
COM Port	2 x COMs, 1x Line-out Cable.WL1253H-20P 1.25mm Housing.Dual DB9(M).Line-Out Jack.15cm	PINREX	712-94-20TWR8	20	1655820100	1703200153
LAN	1 x RJ45 Connector, 90D. (F), DIP	UDE	RT7-17FAAM1A	10	1652514 20B	N/A
USB	1 x Dual USB Connector, 90D. (F), DIP	LOTES	ABA-USB-254-K01	13	1654801832	N/A
LVDS LCD	Board to Wrie Conn.15P*2.90D(M).SMD.1.0mm	ACES	50246-03001-001	30	1653515210	N/A

LCD Inverter	1 x Wafer Box, 5P, 90D. (M) DIP. ,2.0mm	PINREX	721-94-05TWR9	5	1655305130	N/A
SATA	1 x SATA Connector, 180D. (M), SMT	TechBest	007-01-00757	7	1654907009	N/A
SATA PWR	1 x Wafer Box, 2P, 180D. (M) DIP. ,2.0mm	PINREX	721-81-02TW00	2	1655302025	1702150155
Power Conn.	TERMINAL.2P*1.90D(M).DIP	Dinkle	DT-126VP-S2016002P	2	1652602105	
Digital I/O	1 x WAFER BOX.6P. 180D.(M).2.0mm	PINREX	222-97-03GBE1	6	1653003200L	N/A
Front Panel	1 x WAFER BOX.10P. 180D.(M).2.0mm	PINREX	222-97-05GBE1	10	1653005200Y	N/A
Audio	2 x COMs, 1x Line-out Cable.WL1253H-20P 1.25mm	PINREX	712-94-20TWR8	20	1655820100	1703200153

	Housing.Dual DB9(M).Line-Out Jack.15cm					
USB	1 x Wafer Box, 5P, 180D.(M) SMD. ,1.25mm	CATCH	1201-700-05SM	5	1655905037	1700050207
BIO	Board-Board Connector.80P.180D(F)..Hirose.FX18-80P-0.8SV	Hirose	FX18-80P-0.8SV	80	1654008020	N/A

Appendix D

DIO

D.1 DIO

The F75111 provides one serial access interface, I2C Bus, to read/write internal registers.

The address of Serial Bus is 0x6E (0110_1110)

The related register for configuring DIO is list as follows:

Configuration and Control Register – Index 01h

Power-on default [7:0] =0000_1000b

Bit	Name	R/W	PWR	Description
7	INIT	R/W	VSB3V	Software reset for all registers including Test Mode registers. Users use only.
6	Reserved	R/W	VSB3V	
5	EN_WDT10	R/W	VSB3V	Enable Reset Out. If set to 1, enable WDTOUT10# output. Default is disable.
4	Reserved	R/W	VSB3V	
3	Reserved	R/W	VSB3V	
2	Reserved	R/W	VSB3V	
1	SMART_POWR_MANAGEMENT	R/W	VSB3V	Set this bit to 1 will enable auto power down mode, when all function are idle then 20ms the chip will auto power down, it will wakeup when GPIO state change or read write register
0	SOFT_POWR_DOWN	R/W	VSB3V	Set this bit to 1 will power down all of the analog block and stop internal clock, write 0 to clear this bit or when GPIO state change will auto clear this bit to 0.

GPIO2x Output Control Register – Index 20h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_OCTRL	R/W	VSB3V	GPIO 27 output control. Set to 1 for output function. Set to 0 for input function(default).
6	GP26_OCTRL	R/W	VSB3V	GPIO 26 output control. Set to 1 for output function. Set to 0 for input function(default).
5	GP25_OCTRL	R/W	VSB3V	GPIO 25 output control. Set to 1 for output function. Set to 0 for input function(default).
4	GP24_OCTRL	R/W	VSB3V	GPIO 24 output control. Set to 1 for output function. Set to 0 for input function(default).

GPIO2x Output Data Register – Index 21h

Power-on default [7:0] =0000_0000b

Bit	Name	R/W	PWR	Description
7	GP27_ODATA	R/W	VSB3V	GPIO 27 output data.
6	GP26_ODATA	R/W	VSB3V	GPIO 26 output data.
5	GP25_ODATA	R/W	VSB3V	GPIO 25 output data.
4	GP24_ODATA	R/W	VSB3V	GPIO 24 output data.

GPIO2x Input Status Register – Index 22h

Power-on default [7:0] =xxxx_xxxxb

Bit	Name	R/W	PWR	Description
7	GP27_PSTS	RO	VSB3V	Read the GPIO27 data on the pin.
6	GP26_PSTS	RO	VSB3V	Read the GPIO26 data on the pin.
5	GP25_PSTS	RO	VSB3V	Read the GPIO25 data on the pin.
4	GP24_PSTS	RO	VSB3V	Read the GPIO24 data on the pin.

The following is a sample code for 8 input

```
.MODEL SMALL
.CODE
begin:
mov cl,01h
mov al,80h
call CT_I2CWriteByte
call Delay5ms

        mov al,00h
mov cl,20h
call CT_I2CWriteByte

mov cl,22h
call CT_I2CReadByte

;Input : CL - register index
```

```
; CH - device ID
;Output : AL - Value read
Ct_I2CReadByte Proc Near
mov ch,06eh
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
inc ch ; Set the slave address and
mov al, ch ; prepare for a READ command
out dx, al
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to read
out dx, al
mov dx, F040h + 06h

xor al, al ; Clear old data
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
out dx, al

mov dx, F040h + 00h ; Host Control Reegister
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready
mov dx, F040h + 06h
```

```
in al, dx

ret
Ct_I2CReadByte Endp
;Input : CL - register index
; CH - device ID
; AL - Value to write
;Output: none

Ct_I2CWriteByte Proc Near
mov ch,06eh

xchg ah, al
mov dx, F040h + 00h ; Host Control Register
xor al, al ; Clear previous commands
out dx, al
call Delay5ms
mov dx, F040h + 04h ; Transmit Slave Address Register
mov al, ch ; Set the slave address and
out dx, al ; prepare for a WRITE command
mov dx, F040h + 05h ; Host Command Register
mov al, cl ; offset to write
out dx, al
mov dx, F040h + 06h
mov al, ah
out dx, al
mov dx, F040h + 01h ; Host Status Register
mov al, 07h ; Clear all status bits
```

```
out dx, al
mov dx, F040h + 00h ; Host Control Register
mov al, 12h ; Start a byte access
out dx, al
call CT_Chk_SMBus_Ready ;R14
ret
Ct_I2CWriteByte Endp
; Wait until the busy bit clears, indicating that the SMBUS
; activity has concluded.
CT_Chk_SMBus_Ready Proc Near
mov dx, F040h + 01h ; Host Status Register
Check_I2C_ByteRead_ForBusy:
in al, dx
test al, 08h
jnz Check_I2C_ByteRead_ForBusy
Check_I2C_ByteRead_ForStatus:
in al, dx
test al, 07h ; HSTS[2:0]=All clearable status bits
jz Check_I2C_ByteRead_ForStatus
ret
CT_Chk_SMBus_Ready Endp
END begin
```