

**PFM-HDS**

AMD® G-series T16R Processor

DDR3 1066 SODIMM

18-bit Single Channel LVDS LCD

4 USB2.0, 4 COM, 1 SATA, 1 CFast™

1 Gigabit Ethernet, PC/104+

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## Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- Jumper Cap
- Product DVD
- PFM-HDS with Heatsink

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

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Chapter

1

**General  
Information**



## 1.1 Introduction

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AAEON Technology, a leading company in embedded boards manufacturing with a full range of PC/104 Modules, launches a brand new PC/104 CPU Module-PFM-HDS. Its compact size and rich functionality ensures the most cost effective and compatible module to coincide with your existing system planning devices.

PFM-HDS adopts an AMD<sup>®</sup> G-series T16R Processor. Although PFM-HDS is a small board, it offers the full functions for customers demand. The chipset of PFM-HDS deploys AMD<sup>®</sup> G-series T16R and AMD<sup>®</sup> A55E that make this board achieve high performance. It features one 10/100/1000Base-TX Ethernet port, four USB 2.0 ports, four COM ports. In addition, the PFM-HDS equips PC/104+ socket and one CFast<sup>™</sup> for flexible expansions.

This model supports CRT/LCD simultaneous/ dual view displays and deploys one 18-bit single channel LVDS. It also supports AAEON Hi-Safe SDK/Utility and is perfect for the applications of Industrial Control Box, Industrial Automation, Transportation, Test & Measurement, Security, Defense & Government, and etc.

## 1.2 Features

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- Onboard AMD® G-Series T16R Processor
- AMD A55E
- SODIMM DDR3 1066 up to 4GB
- 10/100/1000Base-TX Ethernet x 1
- CRT, 18-bit LVDS
- 2CH HD Audio
- SATA 3.0Gb/s x 1, CFast™ x 1
- USB2.0 x 4, COM x 4, 8-bit Digital I/O
- PC/104+ Expansion
- +5V Only Operation
- AAeon Hi-Safe SDK/Utility Supported

## 1.3 Specifications

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### System

- Form Factor PC/104
- Processor AMD® G-series T16R processor
- System Memory DDR3 1066 MHz SODIMM x 1, Max. 4 GB
- Chipset AMD® A55E
- I/O Chipset Fintech F81866DG
- Ethernet Realtek RTL8111E for 10/100/1000Base-TX x 1
- BIOS AMI Plug & Play SPI BIOS – 4MB Flash
- Wake on LAN Yes
- Watchdog Timer Generates a time-out system reset
- H/W Status Monitoring Supports power supply voltages and temperature monitoring
- Expansion Interface PC/104+
- Power Requirement +5V or AT/ ATX
- Battery Lithium battery
- Board Size 3.77" x 4.05" (96mm x 103mm)
- Gross Weight 0.35 lb (0.16 Kg)

- Operating Temperature 32°F ~ 140°F (0°C ~ 60°C)
- Storage Temperature -40°F ~ 176°F (-40°C ~ 80°C)
- Operating Humidity 0%~90% relative humidity, non-condensing

***Display: Supports CRT/LCD simultaneous/ dual view displays***

- Chipset AMD® T16R processor integrated
- Resolutions Up to 1920x1200 for CRT; Up to 1366x768 for LVDS
- LCD Interface 18-bit Single Channel LVDS

***I/O***

- Storage SATA 3.0 Gb/s x 1, CFast™ x 1
- Serial Port RS-232 x 3, RS-232/422/485 (auto flow) x 1
- Universal Serial Bus USB 2.0 x 4
- Digital I/O 8-bit Digital I/O (Programmable 4-in/ 4-out)
- Audio Line-in, Line-out, Mic-in

Chapter

2

**Quick  
Installation  
Guide**

## 2.1 Safety Precautions

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**Warning!**

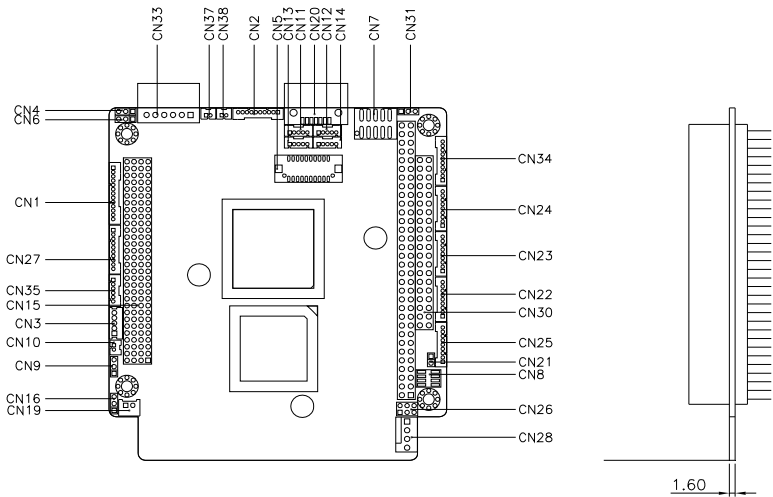
*Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.*

**Caution!**

*Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis*

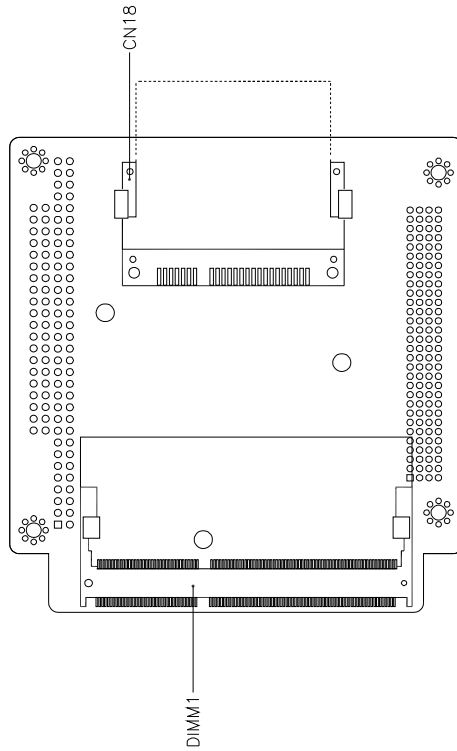
## 2.2 Location of Connectors and Jumpers

### Component Side



Component Side

Solder Side

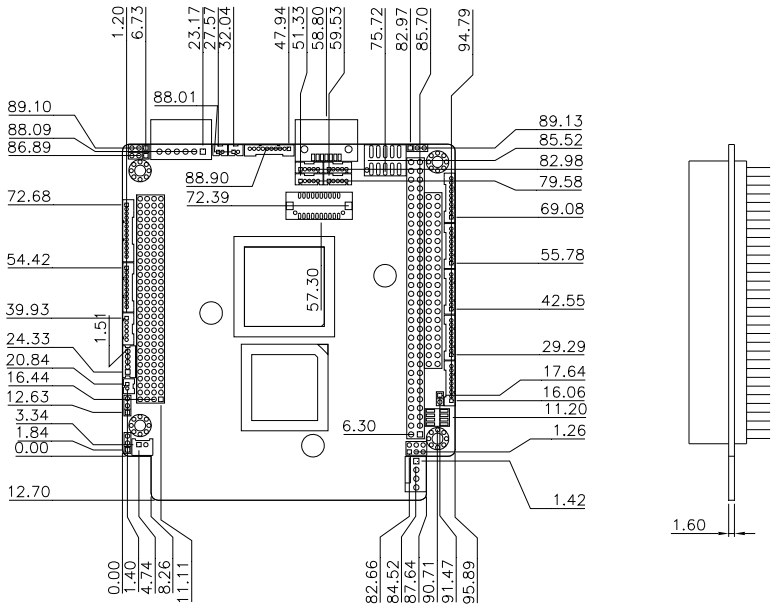


Solder Side

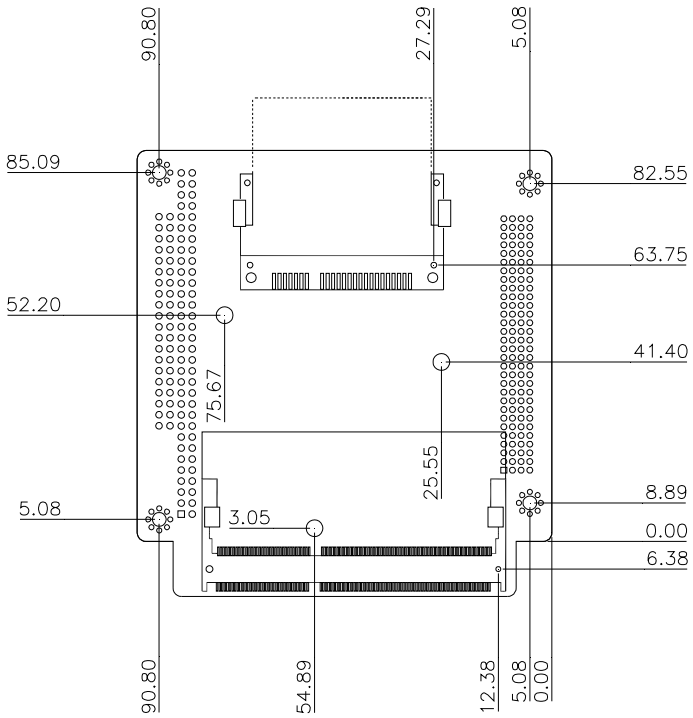


### 2.3 Mechanical Drawing

#### Component Side



Solder Side



Solder Side

## 2.4 List of Jumpers

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The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Label	Function
CN4	Backlight Control Voltage Selection
CN6	LVDS Voltage Selection
CN9	Clear CMOS
CN16	PCI104 VIO Voltage Selection
CN21	AT/ATX Selection
CN26	COM2 +5V/Ring/+12V Selection
CN31	PC104 -5V/-12V Voltage Selection(Reserved)

## 2.5 List of Connectors

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The board has a number of connectors that allow you to configure your system to suit your application. The table below shows the function of each board's connectors:

Label	Function
CN1	CRT Connector
CN2	Audio Connector
CN3	LVDS Backlight Connector
CN5	Internal LVDS Connector
CN7	LAN Connector
CN8	BIOS Connector
CN10	Battery Connector
CN11	USB2.0 Connector
CN12	USB2.0 Connector
CN13	USB2.0 Connector
CN14	USB2.0 Connector
CN15	PCI104 Connector
CN18	CFast Connector
CN19	SATA Power Connector
CN20	SATA Connector
CN22	COM1 RS232 Connector
CN23	COM3 RS232 Connector
CN24	COM4 RS232 Connector
CN25	COM2 RS232/422/485 Connector
CN27	Digital I/O Connector

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CN28	Smart Fan Connector
CN29/ CN30	PC104/ISA Connector
CN33	Power Input Connector
CN34	Front Panel Connector
CN35	PS2 Keyboard/Mouse Connector
CN37	SPK Out Right Channel
CN38	SPK Out left Channel
DIMM1	DDR3 SO-DIMM Connector

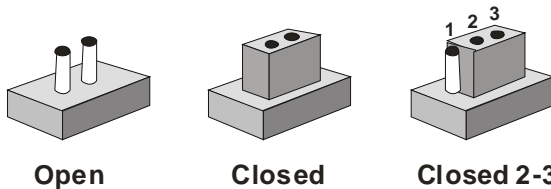
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## 2.6 Setting Jumpers

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You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.

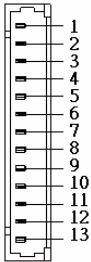


A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

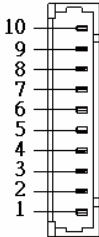
## 2.7 CRT Connector (CN1)



Pin	Pin Name	Signal Type	Signal Level
1	VSYNC	OUT	
2	HSYNC	OUT	
3	GND	GND	
4	SCL	I/O	+5V
5	SDA	I/O	+5V
6	GND	GND	
7	BLUE	OUT	
8	GND	GND	
9	GREEN	OUT	
10	GND	GND	
11	RED	OUT	
12	GND	GND	
13	VCC	PWR	+5V

## 2.8 Audio Connector (CN2)

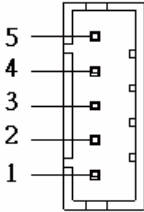
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Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_L	IN	
3	GND	GND	
4	LINE_L	IN	
5	LINE_R	IN	
6	GND	GND	
7	LOUT_L	OUT	
8	GND	GND	
9	LOUT_R	OUT	
10	VCC	PWR	+5V



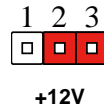
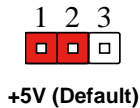
## 2.9 Backlight Brightness Control Connector (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	LVDS Voltage select	OUT	
2	LVDS Backlight control	OUT	
3	GND	GND	
4	GND	GND	
5	LVDS Backlight Enable	OUT	

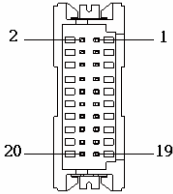
Note: LVDS Voltage can be set to +5V or +12V by CN4.

## 2.10 LVDS Backlight Control Voltage Selection (CN4)



CN4	Function
1-2	+5V (Default)
2-3	+12V

## 2.11 Internal LVDS Connector (CN5)



Pin	Pin Name	Signal Type	Signal Level
1	LVDS_BKLEN	OUT	
2	LVDS_BKLCTL	OUT	
3	LVDS Voltage	PWR	+3.3V/+5V
4	LVDS Voltage	+3.3V/ 5V	
5	LVDS_CLKN	OUT	
6	LVDS_TX2	OUT	
7	LVDS_CLKP	OUT	
8	LVDS_TX#2	OUT	
9	LVDS Voltage	PWR	+3.3V/+5V
10	GND	GND	
11	LVDS_TX0	OUT	
12	LVDS_TX3	OUT	
13	LVDS_TX#0	OUT	
14	LVDS_TX#3	OUT	
15	GND	GND	
16	GND	GND	

<b>PC/104 Module</b>	<b>PFM-HDS</b>
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17	LVDS_TX1	OUT	
18	LVDS_DDCDAT	I/O	+3.3V
19	LVDS_TX#1	OUT	
20	LVDS_DDCCLK	I/O	+3.3V

### 2.12 LVDS Voltage Selection (CN6)



+5V



+3.3V(Default)

CN6	Function
1-2	+5V
2-3	+3.3V (Default)

### 2.13 Clear CMOS (CN9)



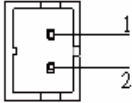
Normal (Default)



Clear CMOS

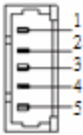
CN9	Function
1-2	Normal (Default)
2-3	Clear CMOS

## 2.14 Battery Connector (CN10)



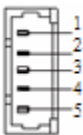
Pin	Pin Name	Signal Type	Signal Level
1	RTCBAT	PWR	3.3V
2	GND	GND	

## 2.15 USB2.0 Connector (CN11)



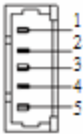
Pin	Pin Name	Signal Type	Signal Level
1	USB_VCC0	PWR	+5V
2	USBP0-	OUT	
3	USBP0+	OUT	
4	GND	GND	
5	GND	GND	

## 2.16 USB2.0 Connector (CN12)



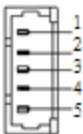
Pin	Pin Name	Signal Type	Signal Level
1	USB_VCC0	PWR	+5V
2	USBP1-	OUT	
3	USBP1+	OUT	
4	GND	GND	
5	GND	GND	

### 2.17 USB2.0 Connector (CN13)



Pin	Pin Name	Signal Type	Signal Level
1	USB_VCC1	PWR	+5V
2	USBP2-	OUT	
3	USBP2+	OUT	
4	GND	GND	
5	GND	GND	

### 2.18 USB2.0 Connector (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	USB_VCC1	PWR	+5V

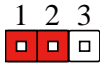
PC/104 Module		PFM-HDS
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2	USBP3-	OUT
3	USBP3+	OUT
4	GND	GND
5	GND	GND

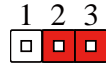
### 2.19 PCI-104 Connector (CN15)

Standard PCI-104 Slot

### 2.20 PCI104 VIO Voltage Selection (CN16)



+5V



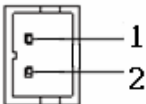
+3.3V (Default)

CN16	Function
1-2	+5V
2-3	+3.3V (Default)

### 2.21 CFast Connector (CN18)

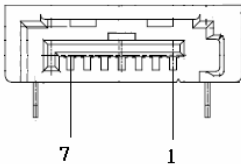
Standard CFast Connector

### 2.22 SATA Power Connector (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	GND

### 2.23 SATA Connector (CN20)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TXP0	DIFF	
3	SATA_TXN0	DIFF	
4	GND	GND	
5	SATA_RXN0	DIFF	
6	SATA_RXP0	DIFF	
7	GND	GND	

### 2.24 AT/ATX Selection (CN21)



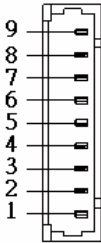
ATX



AT

CN21	Function
1-2 (Open)	ATX
1-2	AT

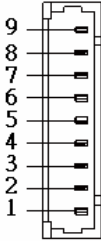
## 2.25 COM1 RS232 Connector (CN22)



Pin	Pin Name	Signal Type	Signal Level
1	DCD1	IN	
2	DSR1	IN	
3	RXD1	IN	
4	RTS1	OUT	±9V
5	TXD1	OUT	±9V
6	CTS1	IN	
7	DTR1	OUT	±9V
8	RI1	IN	
9	GND	GND	

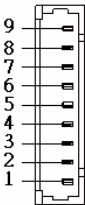


## 2.26 COM3 RS232 Connector (CN23)



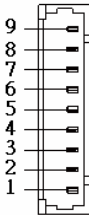
Pin	Pin Name	Signal Type	Signal Level
1	DCD3	IN	
2	DSR3	IN	
3	RXD3	IN	
4	RTS3	OUT	±9V
5	TXD3	OUT	±9V
6	CTS3	IN	
7	DTR3	OUT	±9V
8	RI3	IN	
9	GND	GND	

## 2.27 COM4 RS232 Connector (CN24)



Pin	Pin Name	Signal Type	Signal Level
1	DCD4	IN	
2	DSR4	IN	
3	RXD4	IN	
4	RTS4	OUT	±9V
5	TXD4	OUT	±9V
6	CTS4	IN	
7	DTR4	OUT	±9V
8	RI4	IN	
9	GND	GND	

## 2.28 COM2 RS232/422/485 Connector (CN25)



### RS-232

Pin	Pin Name	Signal Type	Signal Level
1	DCD2	IN	
2	DSR2	IN	
3	RXD2	IN	
4	RTS2	OUT	±9V

**PC/104 Module****PFM-HDS**

5	TXD2	OUT	±9V
6	CTS2	IN	
7	DTR2	OUT	±9V
8	RI2	IN	
9	GND	GND	

**RS-422**

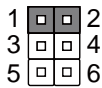
Pin	Pin Name	Signal Type	Signal Level
1	TX-	OUT	±5V
2	N.C		
3	RX+	IN	
4	N.C		
5	TX+	OUT	±5V
6	N.C		
7	RX-	IN	
8	+5V/+12V	PWR	+5V/+12V
9	GND	GND	

**RS-485**

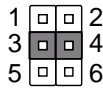
Pin	Pin Name	Signal Type	Signal Level
1	B (Data-)	I/O	±5V
2	N.C		
3	N.C		
4	N.C		
5	A (Data+)	I/O	±5V

6	N.C		
7	N.C		
8	+5V/+12V	PWR	+5V/+12V
9	GND	GND	

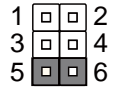
### 2.29 COM2 +5V/Ring/+12V Selection (CN26)



+12V



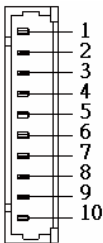
RI2#



+5V

CN26	Function
1-2	+12V
3-4	RI2#
5-6	+5V

### 2.30 Digital I/O Connector (CN27)



Pin	Pin Name	Signal Type	Signal Level
1	GPIO	IN	

2	GPI1	IN	
3	GPI2	IN	
4	GPI3	IN	
5	GPO0	OUT	
6	GPO1	OUT	
7	GPO2	OUT	
8	GPO3	OUT	
9	+3.3V	PWR	+3.3V
10	GND	GND	

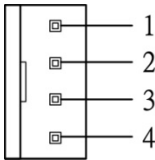
Digital I/O base address: 0xA00

Pin	Pin Name	I/O Port Access Address
1	GPI0	Bit 0 of 0xA00
2	GPI1	Bit 1 of 0xA00
3	GPI2	Bit 2 of 0xA00
4	GPI3	Bit 3 of 0xA00
5	GPO0	Bit 4 of 0xA00
6	GPO1	Bit 5 of 0xA00
7	GPO2	Bit 6 of 0xA00
8	GPO3	Bit 7 of 0xA00

GPIO Port	Location (Pin #)	Access Address based on SIO LDN6	
		Input	Output
GPIO1	1	Reg 0x8A, bit 0	Reg 0x89, bit 0
GPIO2	2	Reg 0x8A, bit 1	Reg 0x89, bit 1
GPIO3	3	Reg 0x8A, bit 2	Reg 0x89, bit 2
GPIO4	4	Reg 0x8A, bit 3	Reg 0x89, bit 3

GPIO5	5	Reg 0x8A, bit 4	Reg 0x89, bit 4
GPIO6	6	Reg 0x8A, bit 5	Reg 0x89, bit 5
GPIO7	7	Reg 0x8A, bit 6	Reg 0x89, bit 6
GPIO8	8	Reg 0x8A, bit 7	Reg 0x89, bit 7

### 2.31 FAN Connector (CN28) (Reserved)

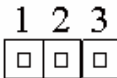


Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SENSE	IN	
3	FAN_CTL	OUT	
4	FAN_TAC	IN	

### 2.32 PC104/ISA Connector (CN29 and CN30)

Standard PC104/ISA Slot

### 2.33 PC104 -5V/-12V Voltage Selection (CN31) (Reserved)



CN31	Function
1	-12V
2	-5V

---

3                      GND

---

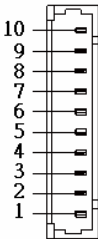
### 2.34 +5VSB and +12VSB Power Input Connector (CN33)

---

Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	+5VSB	PWR	+5V
3	GND	GND	
4	GND	GND	
5	GND	GND	
6	+12VSB	PWR	+12V

### 2.35 Front Pane Connector (CN34)

---

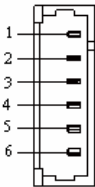


Pin	Pin Name	Signal Type	Signal Level
1	POWER BUTTON	IN	
2	POWRR BUTTON#	IN	
3			
4			
5	HDD LED	OUT	

---

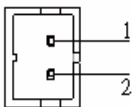
6	HDD LED#	OUT
7	POWER LED	OUT
8	POWER LED#	OUT
9	RESET	IN
10	RESET#	IN

### 2.36 PS2 Keyboard and Mouse Connector (CN35)



Pin	Pin Name	Signal Type	Signal Level
1	KBDATA	OUT	
2	KBCLK	OUT	
3	GND	GND	
4	+5V	PWR	+5V
5	MSDATA	OUT	
6	MSCLK	OUT	

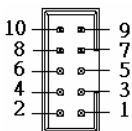
### 2.37 Stereo-Right Channel (CN37)





Pin	Pin Name	Signal Type	Signal Level
1	SPK_L+	OUT	
2	SPK_L-	OUT	

### 2.38 LAN Connector (LAN1)



Pin	Pin Name	Signal Type	Signal Level
1	LAN1_TX1+	DIFF	
2	LAN1_TX1-	DIFF	
3	LAN1_RX1+	DIFF	
4	LAN1_RX1-	DIFF	
5	GND	GND	
6	GND	GND	
7	LAN1_TX2+	DIFF	
8	LAN1_TX2-	DIFF	
9	LAN1_RX2+	DIFF	
10	LAN1_RX2-	DIFF	

### 2.39 DDR3 SODIMM Connector (DIMM1)

Standard DDR3 SODIMM Specification

## Below Table for China RoHS Requirements

产品中有毒有害物质或元素名称及含量

## AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
<p><b>O:</b> 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p><b>X:</b> 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 此产品所标示之环保使用期限, 系指在一般正常使用状况下。</p>						

Chapter

3

**AMI  
BIOS Setup**

### 3.1 System Test and Initialization

---

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

#### System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The PFM-HDS CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

## 3.2 AMI BIOS Setup

---

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

### Entering Setup

Power on the computer and press <Del> or <F2> immediately. This will allow you to enter Setup.

### Main

Set the date, use tab to switch between date elements.

### Advanced

Enable/disable boot option for legacy network devices.

### Chipset

Host bridge parameters.

### Boot

Enables/disables quiet boot option.

### Security

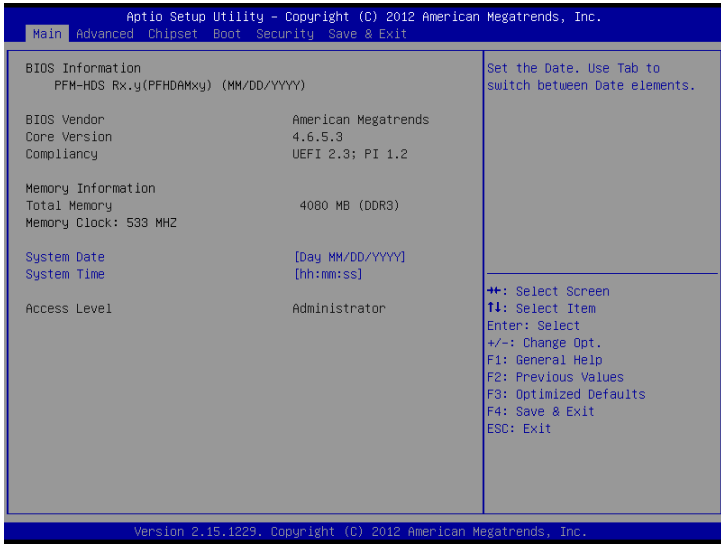
Set setup administrator password.

### Save&Exit

Exit system setup after saving the changes.

## Setup Menu

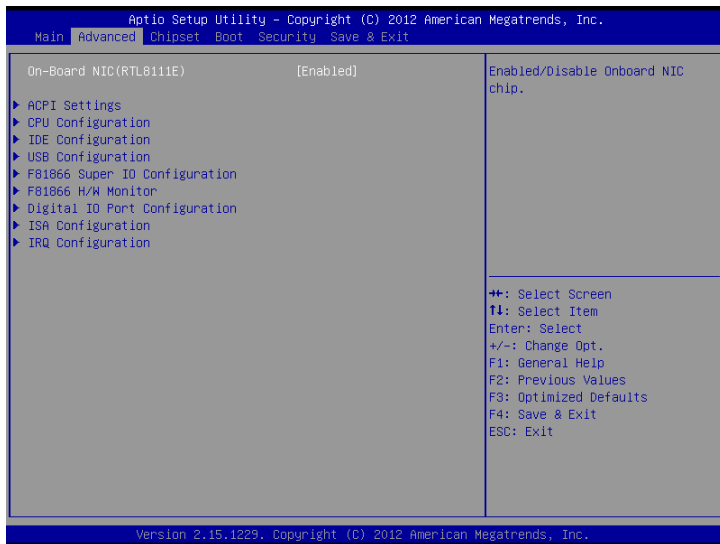
### Setup submenu: Main



#### Options summary: (**default setting**)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	hh : mm : ss	
Change the clock of the system.		

### Setup submenu: Advanced



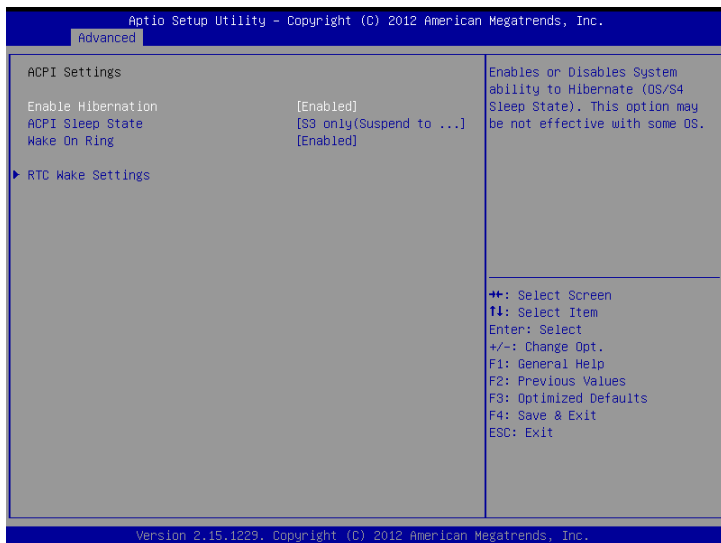
#### Options summary: (*default setting*)

On-Board NIC(RTL8111E)	<b>Enabled</b>	
	Disabled	
Enabled/Disabled Onboard NIC chip.		
ACPI Settings		
System ACPI Parameters		
CPU Configuration		
CPU Configuration Parameters		
IDE Configuration		
IDE Device Options Settings		
USB Configuration		

USB Configuration Parameters		
F81866 Super IO Configuration		
System Super IO Chip Parameters.		
F81866 H/W Monitor		
Monitor hardware status		
Digital IO Port Configuration		
Set Input/Output of Digital IO Port Configuration		
ISA Configuration		
Configure IO or Memory address which will be decoded to ISA BUS		
IRQ Configuration		
Configure IRQs for ISA or PCI devices.		



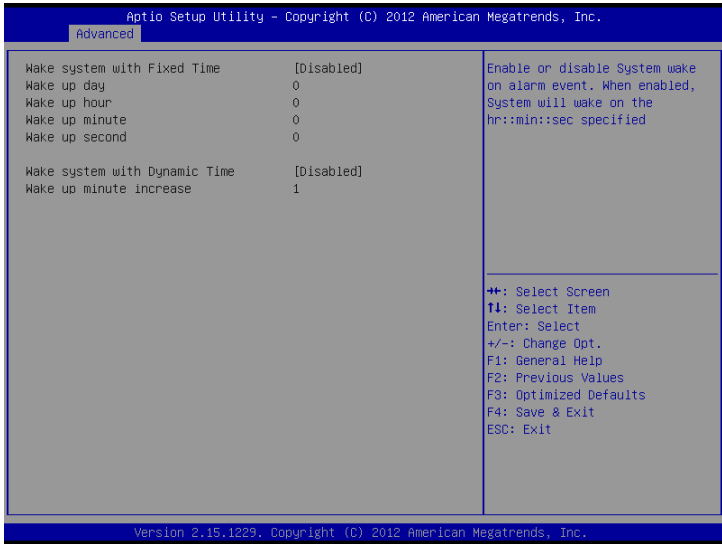
## ACPI Settings

Options summary: (**default setting**)

Enable Hibernation	<b>Enabled</b>	
	Disabled	
Enabled or disabled hibernate (OS/S4 Sleep State).		
ACPI Sleep State	Suspend Disabled	
	<b>S3 only(Suspend to RAM)</b>	
Select the ACPI state used for System Suspend		
Wake on Ring	<b>Enabled</b>	
	Disabled	
Enabled or disabled wake on ring function.		
RTC Wake Settings		

Enable system to wake from S5 using RTC alarm.

### RTC Wake Settings

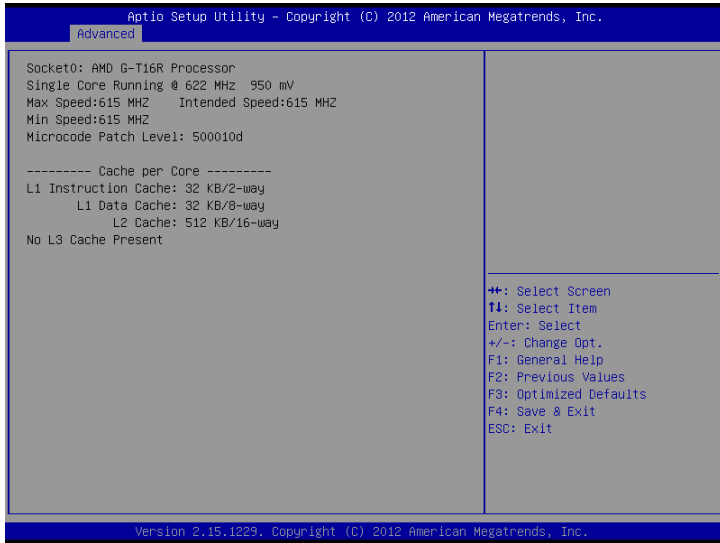


Options summary: **(default setting)**

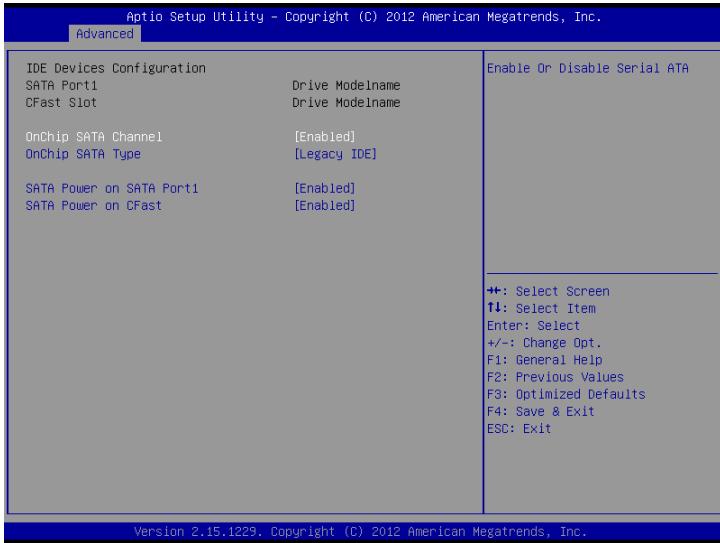
Wake system with Fixed Time	<b>Disabled</b>	
	Enabled	
Enable or disable System wake on alarm event. Wake up time is setting by following settings.		
Wake up day	0-31	
Select 0 for daily system wake up, 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0-23	

Wake up minute	0-59	
Wake up second	0-59	
Wake system with	<b>Disabled</b>	
Dynamic Time	Enabled	
Enable or disable System wake on alarm event. Wake up time is current time + Increase minutes.		
Wake up minute increase	1-5	

## CPU Configuration



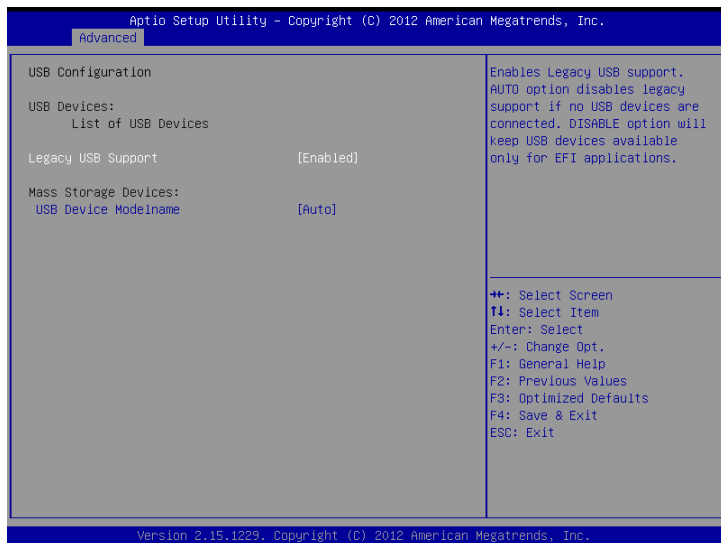
## IDE Configuration



Options summary: (**default setting**)

OnChip SATA Channel	Disabled	
	<b>Enabled</b>	
Enable or Disable Serial ATA		
OnChip SATA Type	<b>Legacy IDE</b>	
	AHCI	
Configure SATA controller operating as IDE/AHCI mode.		
SATA Power on SATA Port1/CFast	<b>Enabled</b>	
	Power Down	
Enable Or Disable SATA Power on SATA Port1/CFast slot.		

## USB Configuration



### Options summary: (*default setting*)

Legacy USB Support	<b>Enabled</b>	
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application		
Device Name (Emulation Type)	<b>Auto</b>	
	Floppy	
	Forced FDD	

	Hard Disk	
	CD-ROM	
<p>If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)</p>		

### F81866 Super IO Configuration

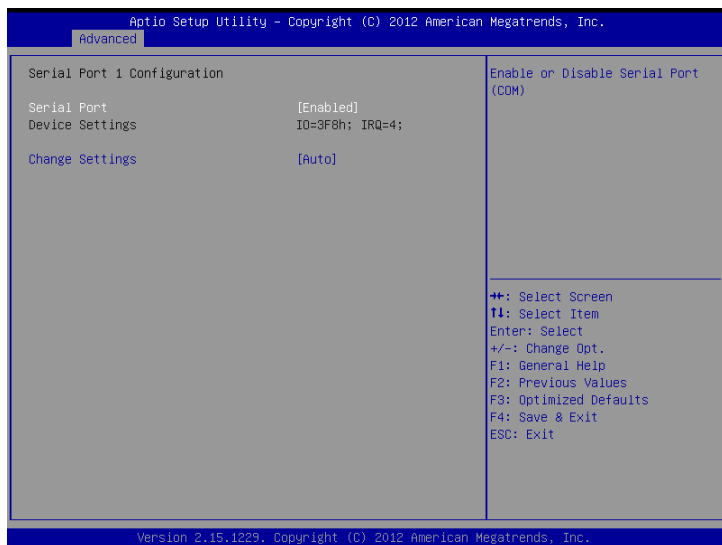


Options summary: (**default setting**)

Serial Port 1/2/3/4 Configuration		
Set Parameters of Serial Port 1/2/3/4		
Power Failure	<b>Always OFF</b>	

	Always ON	
	Keep last state	
Select AC power state when power is re-applied after a power failure.		
Parallel Port Configuration	<b>Disabled</b>	
	Enabled	
ERP Function Enable/Disable		

## Serial Port 1 Configuration



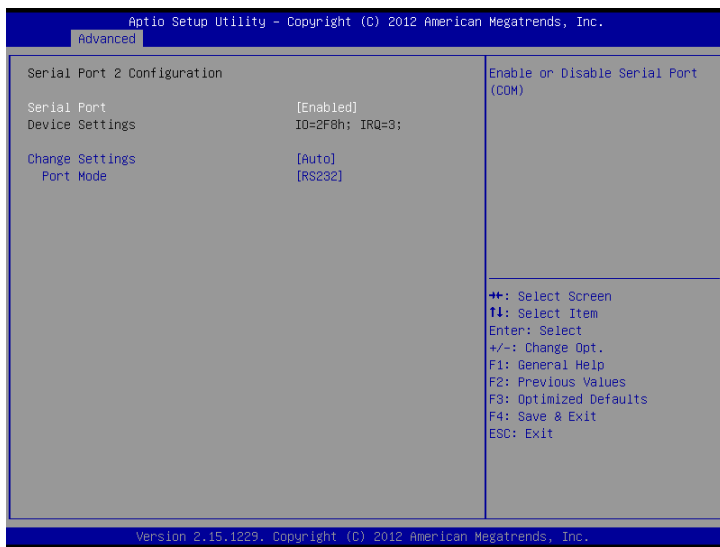
Options summary: **(default setting)**

Serial Port	Disabled	
	<b>Enabled</b>	
En/Disable specified serial port.		



Change Settings	<b>Auto</b>
	IO=3F8h; IRQ=4;
	IO=3F8h; IRQ=3,4,5,7,10,11,12;
	IO=2F8h; IRQ=3,4,5,7,10,11,12;
	IO=3E8h; IRQ=3,4,5,7,10,11,12;
	IO=2E8h; IRQ=3,4,5,7,10,11,12;
Select a resource setting for Super IO device.	

### Serial Port 2 Configuration



Options summary: **(default setting)**

Serial Port	Disabled
	<b>Enabled</b>

En/Disable specified serial port.

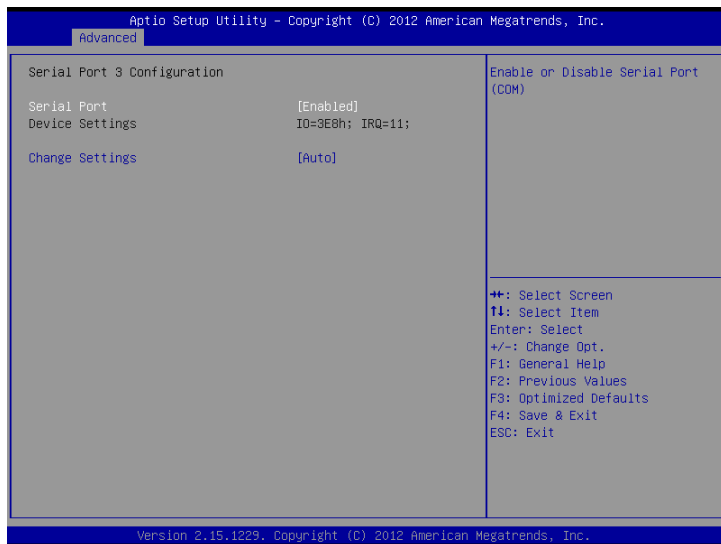
Change Settings	<b>Auto</b>	
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4,5,7,10,11,12;	
	IO=2F8h; IRQ=3,4,5,7,10,11,12;	
	IO=3E8h; IRQ=3,4,5,7,10,11,12;	
	IO=2E8h; IRQ=3,4,5,7,10,11,12;	

Select a resource setting for Super IO device.

Port Mode	<b>RS232</b>	
	RS422	
	RS485	

RS232/422,485 port mode switch

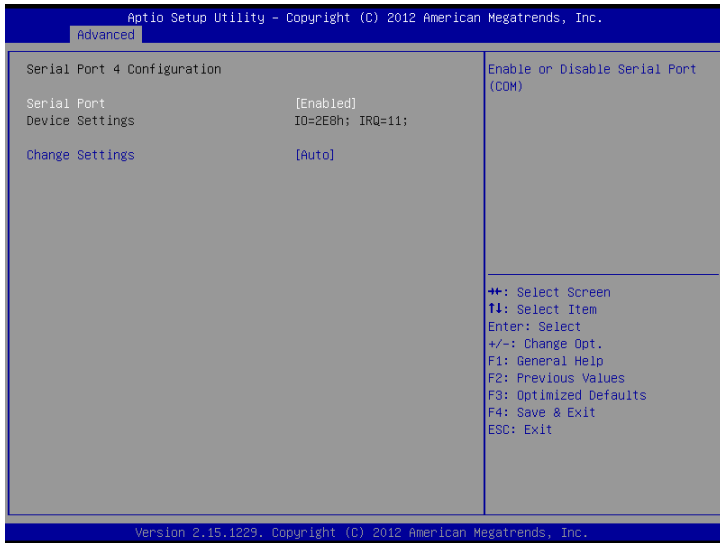
### Serial Port 3 Configuration



Options summary: *(default setting)*

Serial Port	Disabled	
	<b>Enabled</b>	
En/Disable specified serial port.		
Change Settings	<b>Auto</b>	
	IO=3E8h; IRQ=11;	
	IO=3E8h; IRQ=3,4,5,7,10,11,12;	
	IO=2E8h; IRQ=3,4,5,7,10,11,12;	
	IO=228h; IRQ=3,4,5,7,10,11,12;	
	IO=220h; IRQ=3,4,5,7,10,11,12;	
Select a resource setting for Super IO device.		

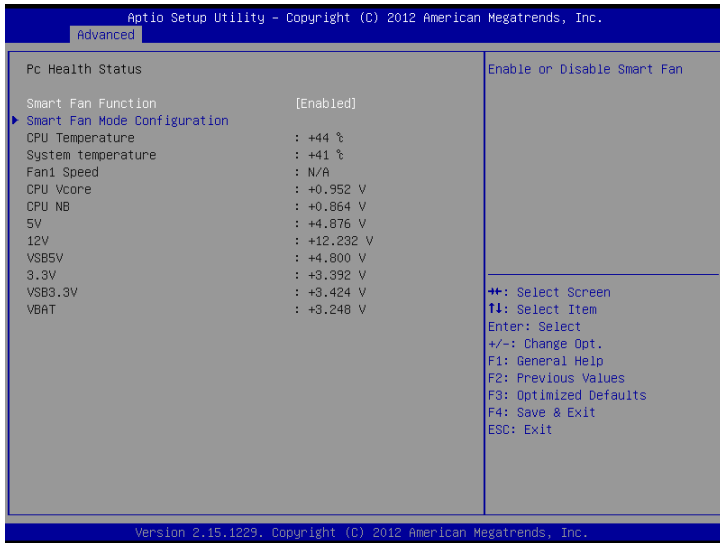
### Serial Port 4 Configuration



Options summary: **(default setting)**

Serial Port	Disabled	
	<b>Enabled</b>	
En/Disable specified serial port.		
Change Settings	<b>Auto</b>	
	IO=2E8h; IRQ=11;	
	IO=3E8h; IRQ=3,4,5,7,10,11,12;	
	IO=2E8h; IRQ=3,4,5,7,10,11,12;	
	IO=228h; IRQ=3,4,5,7,10,11,12;	
	IO=220h; IRQ=3,4,5,7,10,11,12;	
Select a resource setting for Super IO device.		

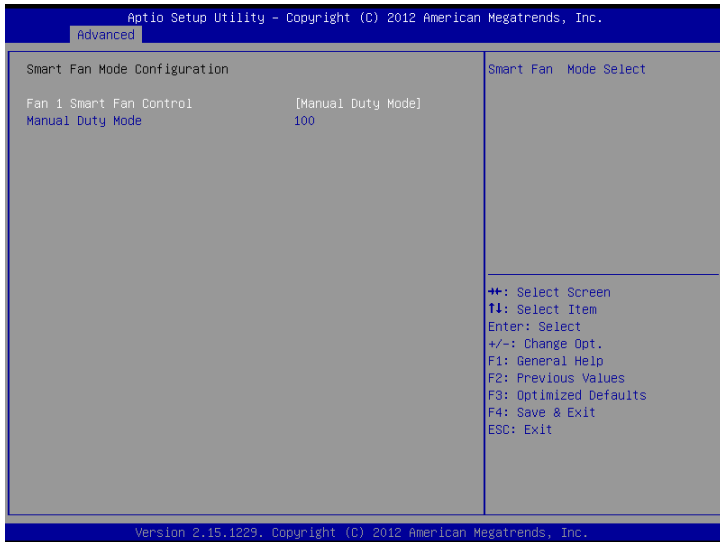
**F81866 H/W Monitor**

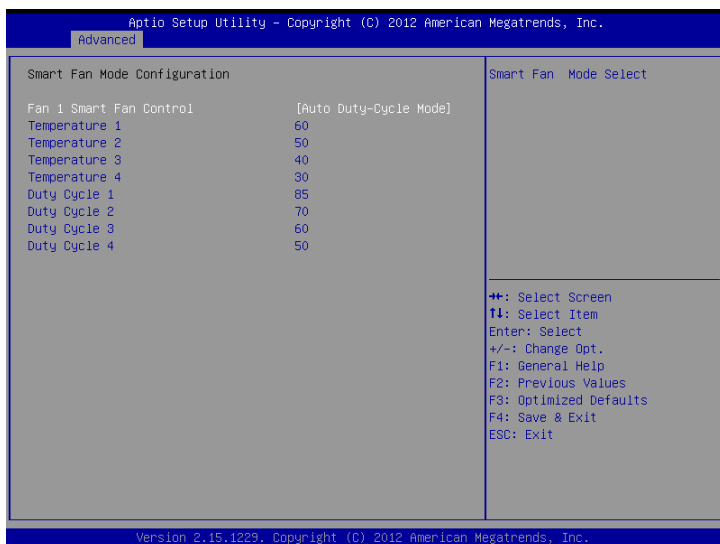


Options summary: (*default setting*)

Smart Fan Function	<b>Enabled</b>	
	Disabled	
Enable or Disable Smart Fan		
Smart Fan Mode Configuration		
Smart Fan Mode Select		

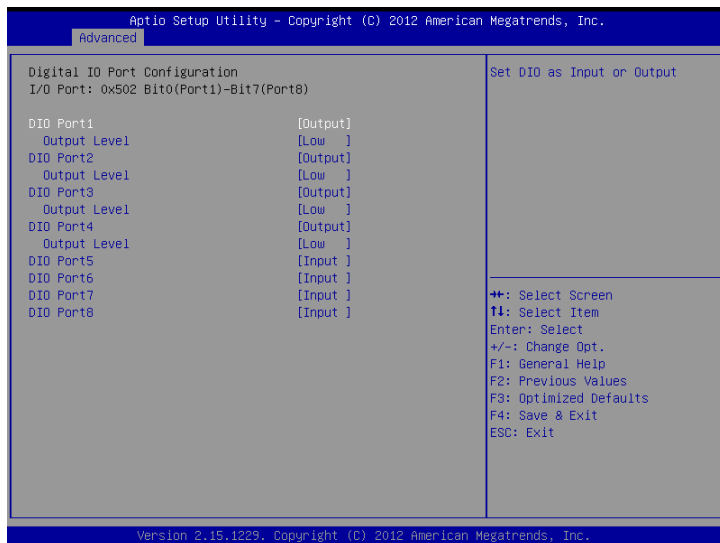
## Smart Fan Mode Configuration



Options summary: (**default setting**)

FAN 1 Smart Fan Control	<b>Manual Duty Mode</b>	
	Auto Duty-Cycle Mode	
En/Disable specified serial port.		
Manual Duty Mode	1-100	
Manual mode fan control, user can write expected duty cycle(PWM fan type) 1-100		
Temperature 1/2/3/4	1-100	
Duty Cycle 1/2/3/4	1-100	
Auto fan speed control. Fan speed will follow different temperature by different duty cycle		

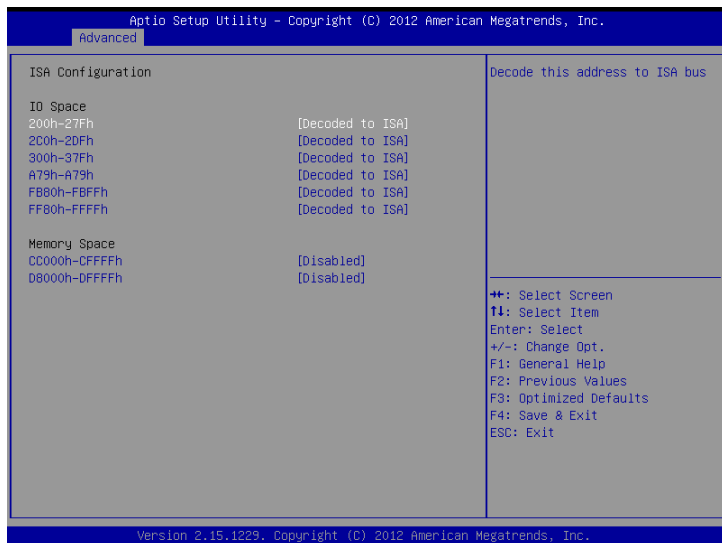
## Digital IO Port Configuration



### Options summary: (*default setting*)

DIO Port1/ DIO Port2/ DIO	Input	
Port3/ DIO Port4	<b>Output</b>	
Set DIO Port x as Input or Output		
DIO Port5/ DIO Port6/ DIO	<b>Input</b>	
Port7/ DIO Port8	Output	
Set DIO Port x as Input or Output		
Output Level	Hi	
	<b>Low</b>	
Set DIO output level when used as output pin		

## ISA Configuration

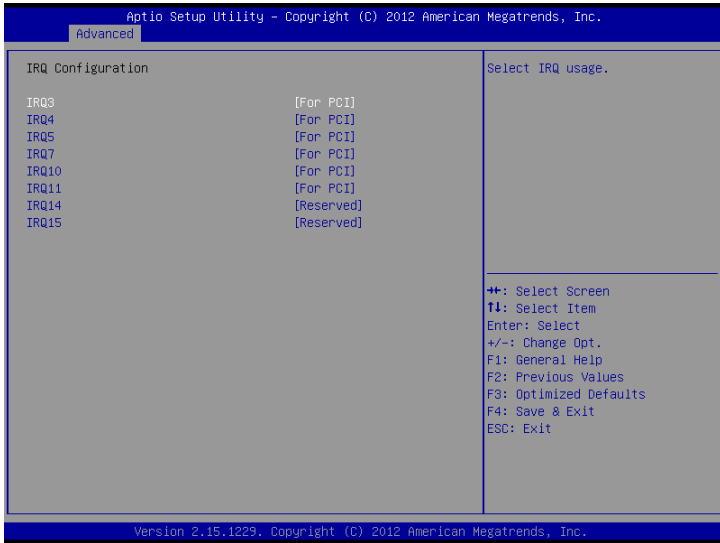


### Options summary: (*default setting*)

200h-27Fh/2C0h-20Fh/ 300h-37Fh/A79h-A79h/	Disabled	
FB80h-FBFFh/ FF80h-FFFFh	<b><i>Decoded to ISA</i></b>	
Decode specified IO address to ISA BUS		
CC000h-CFFFFh/ D8000h-DFFFFh	Disabled	
	<b><i>Decoded to ISA</i></b>	
Decode specified memory address to ISA BUS		



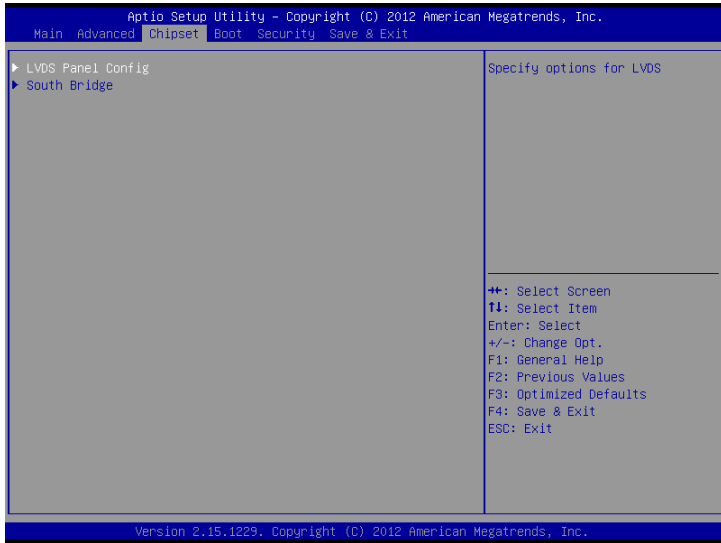
## IRQ Configuration



### Options summary: (*default setting*)

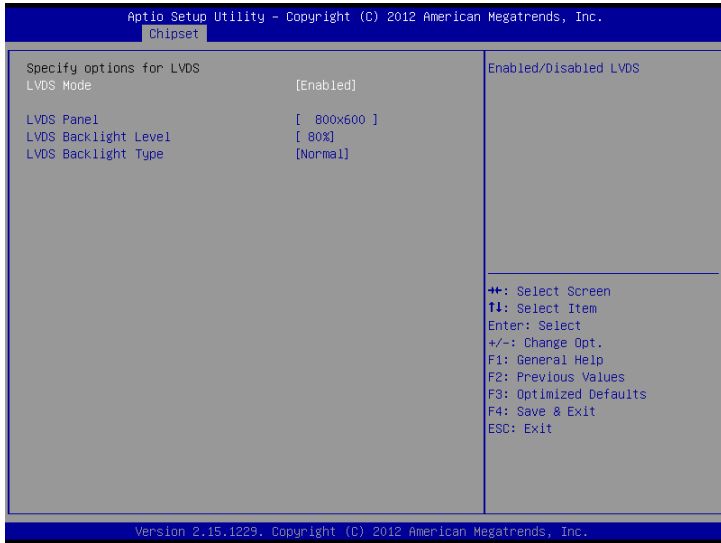
IRQ3/IRQ4/IRQ5/	Reserved	
IRQ7/IRQ10/IRQ11	<b>For PCI</b>	
Select specified IRQ can be used by PCI device or reserved for ISA devices.		
IRQ14/IRQ15	<b>Reserved</b>	
	For PCI	
Select specified IRQ can be used by PCI device or reserved for ISA devices.		

## Setup submenu: Chipset

Options summary: (**default setting**)

LVDS Panel Config		
Specify options for LVDS panel		
South Bridge		
South Bridge Parameters		

## LVDS Panel Config

Options summary: (*default setting*)

LVDS Mode	<b>Enabled</b>	
	Disabled	
Enabled/Disabled LVDS		
LVDS Panel	640x480	
	800x480	
	<b>800x600</b>	
	1024x600	
	1024x768	
	1280x768	
	1366x768	

Select the resolution for LVDS Panel

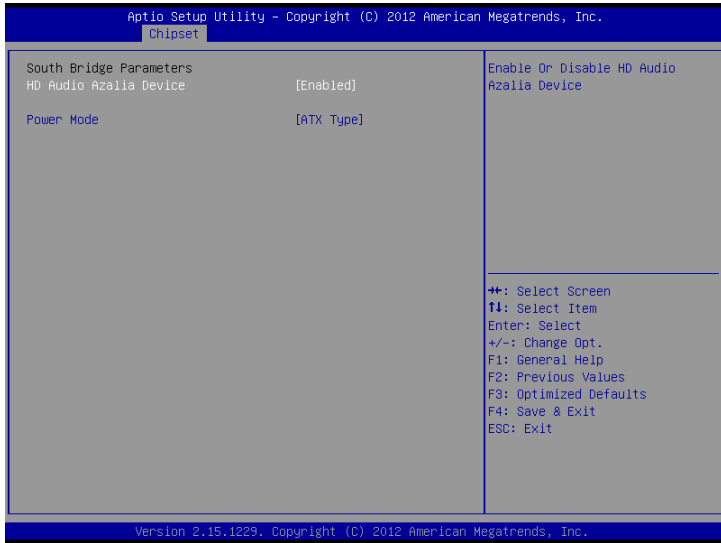
LVDS Backlight Level	100%	
	90%	
	<b>80%</b>	
	70%	
	60%	
	50%	
	40%	
	30%	
	20%	
	10%	
	0%	

Select the backlight level for LVDS Panel

LVDS Backlight Type	<b>Normal</b>	
	Inverted	

Select the signal type for backlight control.

## South Bridge



### Options summary: (*default setting*)

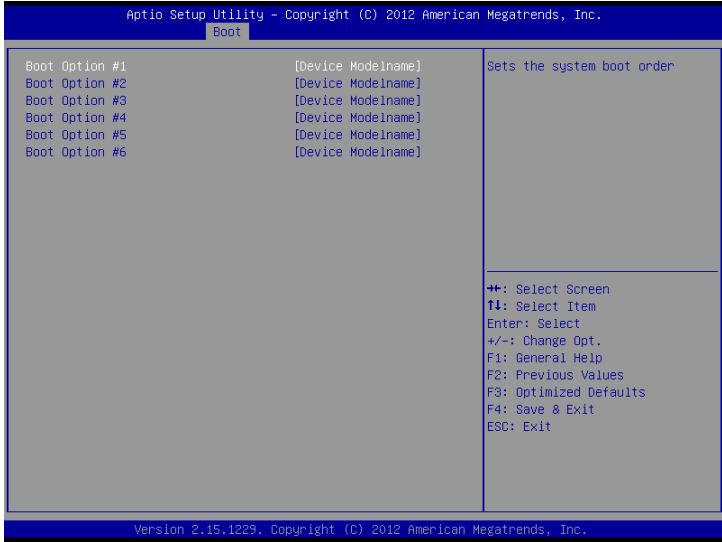
HD Audio Azalia Device	<b>Enabled</b>	
	Disabled	
Enable or Disable HD Audio Controller		
Power Mode	<b>ATX Type</b>	
	AT Type	
Select the power type used on the system		

## Setup submenu: Boot

Options summary: (*default setting*)

Quiet Boot	Disabled	
	<b>Enabled</b>	
En/Disable showing boot logo.		
Launch RTL8111E PXE OpROM	<b>Disabled</b>	
	Enabled	
En/Disable PXE boot for RTL8111E LAN		
Boot Option #X/ XXXX Drive BBS Priorities		
The order of boot priorities.		

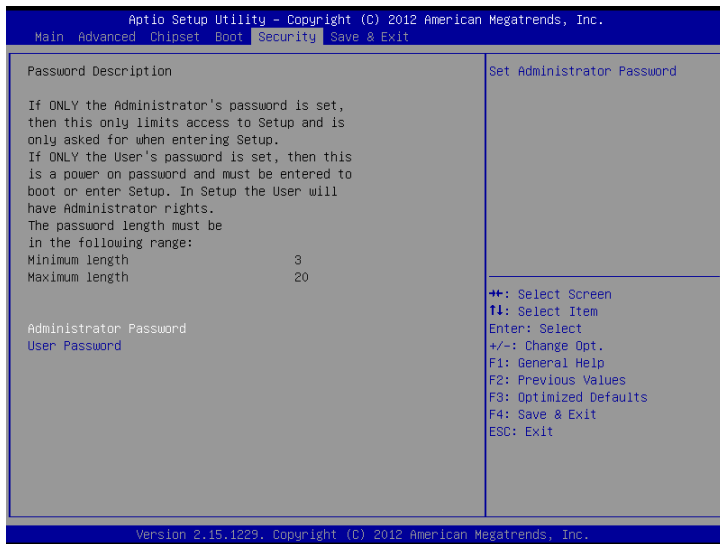
## BBS Priorities



Options summary: (**default setting**)

Boot Option #x	Disabled	
	Device name	
Sets the system boot order		

### Setup submenu: Security



Options summary: (**default setting**)

Administrator Password/	<b>Not set</b>	
User Password		

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

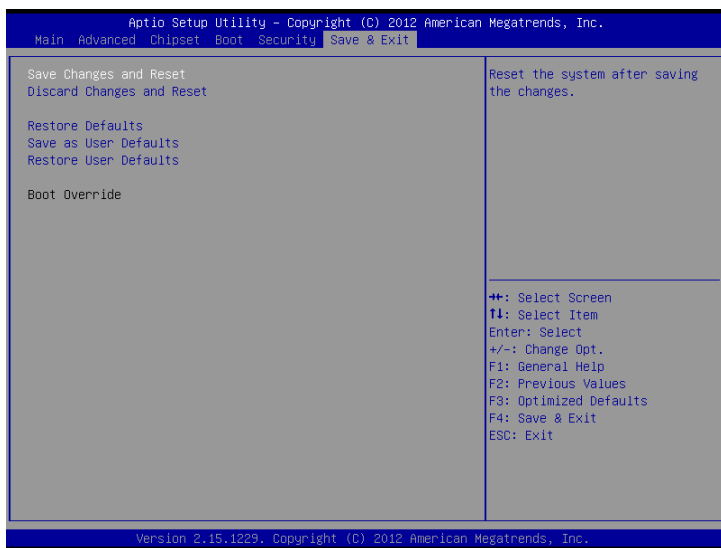
*Install the Password:*

Press Enter on this item, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.



*Removing the Password:*

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

**Setup submenu: Exit**Options summary: (**default setting**)

Save Changes and Reset		
Reset the system after saving the changes		
Discard Changes and Reset		
Reset system setup without saving any changes		
Restore Defaults		
Restore/Load Default values for all the setup options.		

Save as User Defaults		
Save the changes done so far as User Defaults		
Restore User Defaults		
Restore the User Defaults to all the setup options		
Boot Override		
Boot to specified device.		

Chapter

4

**Driver  
Installation**

The PFM-HDS comes with a DVD-ROM that contains all drivers and utilities that meet your needs.

***Follow the sequence below to install the drivers:***

Step 1 – Install Chipset Driver

Step 2 – Install Audio Driver

Step 3 – Install LAN Driver

Step 4 – Install PCI to ISA Bridge Driver

Step 5 – Install Serial Port Driver (Optional)

Step 6 – Install AHCI (Optional)

Please read instructions below for further detailed installations.

## 4.1 Installation:

---

Insert the PFM-HDS CD-ROM into the DVD-ROM Drive. And install the drivers from Step 1 to Step 6 in order.

### Step 1 – Install Chipset Driver

1. Click on the **STEP1-CHIPSET** folder and select the OS folder your system is
2. Double click on the **Setup.exe** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

### Step 2 – Install Audio Driver

1. Click on the **STEP2- AUDIO** folder and select the OS folder your system is
2. Double click on the **Setup.exe** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

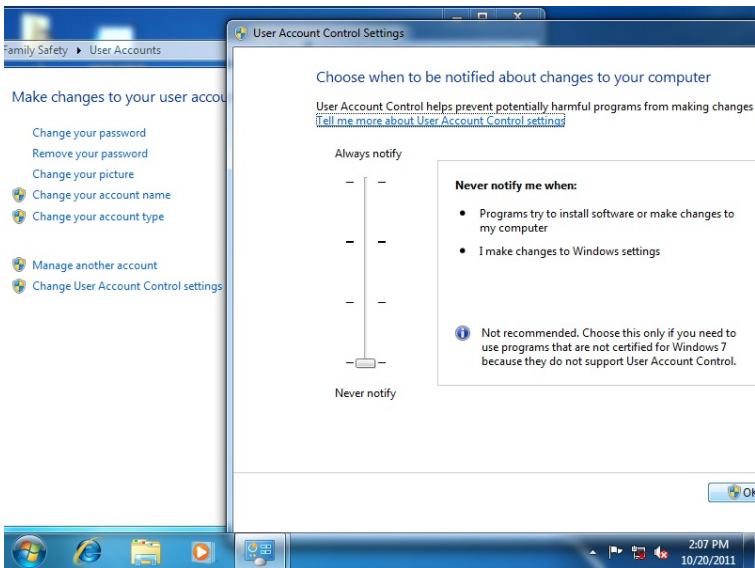
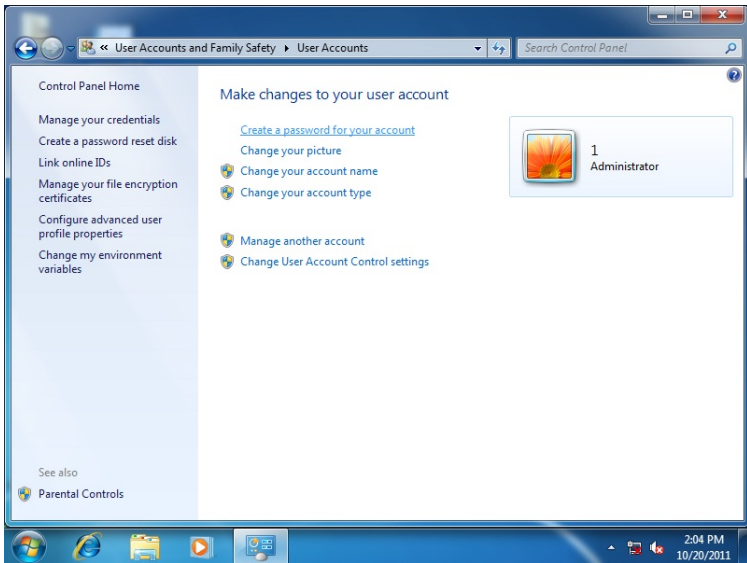
### Step 3 – Install LAN Driver

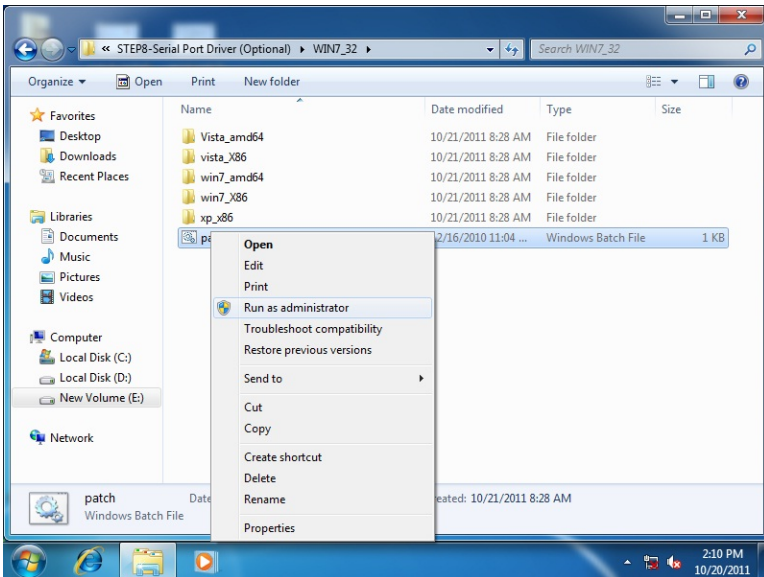
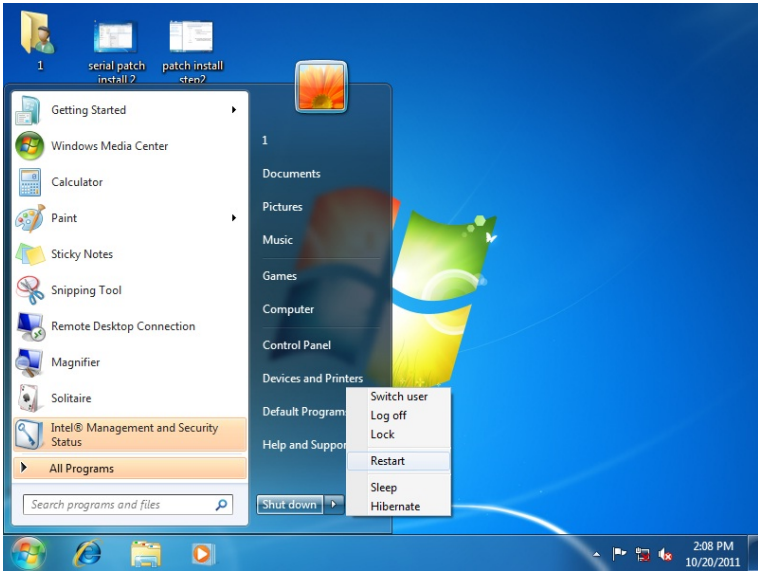
1. Click on the **STEP3- LAN** folder and select the OS folder your system is
  2. Double click on the **setup.exe** file located in each OS folder
  3. Follow the instructions that the window shows
  4. The system will help you install the driver automatically
-

#### Step 4 – Install PCI to ISA Bridge Driver

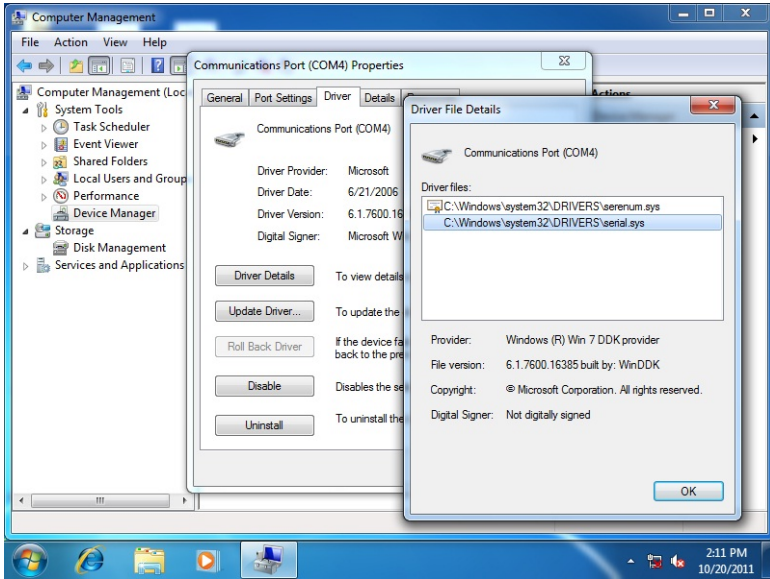
1. Click on **Start** button.
2. Click on **Settings** button
3. Click on **Control Panel** button
4. Click on **System** button
5. Select **Hardware** and click on **Device Manager...**
6. Double click on **Other PCI Bridge Device**
7. Click on **Update Driver...**
8. Click on **Next**
9. Select **Search for a suitable driver...**, then click on **Next**
10. Select **Specify a location**, then click on **Next**
11. Click on **Browse**
12. Select “**Ite**” file from DVD-ROM (**Driver/ STEP4 - PCI to ISA Bridge**) then click on **open**
13. Click on **OK**
14. Click on **Next**
15. Click on **Yes**
16. Click on **Finish**

## Step 5 – Install Serial Port Driver (Optional)









## Step 6 – Install AHCI Driver (Optional)

Please refer to Appendix D AHCI Setting

Appendix

**A**

# Programming the Watchdog Timer

## A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0x510	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s <b>Pulse width is must longer then 16ms.</b>
Signal Polarity	0x05	2	0	0: low active 1: high active <b>Must set this bit to 0</b>
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse <b>Must set this bit to 1</b>
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

## A.2 WatchDog Sample Program

---

```

*****
****
// WDT I/O operation relative definition (Please reference to Table 1)
#define WDTAddr      0x510 // WDT I/O base address
Void WDTWriteByte(byte Register, byte Value);
byte WDTReadByte(byte Register);
Void WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define DevReg       0x00 // Device configuration register
    #define WDRstBit 0x80 // Watchdog WDRST# (Bit7)
    #define WDRstVal 0x80 // Enabled WDRST#
#define TimerReg     0x05 // Timer register
    #define PSWidthBit 0x00 // WDRST# Pulse width (Bit0:1)
    #define PSWidthVal 0x01 // 25ms for WDRST# pulse
    #define PolarityBit 0x02 // WDRST# Signal polarity (Bit2)
    #define PolarityVal 0x00 // Low active for WDRST#
    #define UnitBit     0x03 // Unit for timer (Bit3)
    #define ModeBit     0x04 // WDRST# mode (Bit4)
    #define ModeVal     0x01 // 0:level 1: pulse
    #define EnableBit   0x05 // WDT timer enable (Bit5)
    #define EnableVal   0x01 // 1: enable
    #define StatusBit   0x06 // WDT timer status (Bit6)
#define CounterReg   0x06 // Timer counter register
*****
****

*****
****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig(Counter, Unit);
}

```

```

// Procedure : AaeonWDTEnable
// This procedure will enable the WDT counting.
AaeonWDTEnable();
}
*****

*****

// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable (){
    WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (byte Counter, BOOLEAN Unit){
    // Disable WDT counting
    WDTEnableDisable(0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting(Timer, Unit);
}

VOID WDTEnableDisable(byte Value){
    If (Value == 1)
        WDTSetBit(TimerReg, EnableBit, 1);
    else
        WDTSetBit(TimerReg, EnableBit, 0);
}

VOID WDTParameterSetting(byte Counter, BOOLEAN Unit){
    // Watchdog Timer counter setting
    WDTWriteByte(CounterReg, Counter);
    // WDT counting unit setting
    WDTSetBit(TimerReg, UnitBit, Unit);
    // WDT output mode set to pulse

```

```

    WDTSetBit(TimerReg, ModeBit, ModeVal);
    // WDT output mode set to active low
    WDTSetBit(TimerReg, PolarityBit, PolarityVal);
    // WDT output pulse width is 25ms
    WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
    // Watchdog WDRST# Enable
    WDTSetBit(DevReg, WDRstBit, WDRstVal);
}

VOID WDTClearTimeoutStatus(){
    WDTSetBit(TimerReg, StatusBit, 1);
}

*****

*****

VOID WDTWriteByte(byte Register, byte Value){
    IOWriteByte(WDTAddr+Register, Value);
}

byte WDTReadByte(byte Register){
    return IOReadByte(WDTAddr+Register);
}

VOID WDTSetBit(byte Register, byte Bit, byte Val){
    byte TmpValue;

    TmpValue = WDTReadByte(Register);
    TmpValue &= ~(1 << Bit);
    TmpValue |= Val << Bit;
    WDTWriteByte(Register, TmpValue);
}

*****

*****
















































```

Appendix

























**B**

# I/O Information

## B.1 I/O Address Map

Input/output (IO)	
	[00000000 - 0000000F] Direct memory access controller
	[00000000 - 0000000F] Motherboard resources
	[00000000 - 000003AF] PCI bus
	[00000010 - 0000001F] Motherboard resources
	[00000020 - 00000021] Programmable interrupt controller
	[00000022 - 0000003F] Motherboard resources
	[00000040 - 00000043] System timer
	[00000044 - 0000005F] Motherboard resources
	[00000060 - 00000060] Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
	[00000061 - 00000061] System speaker
	[00000062 - 00000063] Motherboard resources
	[00000064 - 00000064] Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
	[00000065 - 0000006F] Motherboard resources
	[00000070 - 00000071] System CMOS/real time clock
	[00000072 - 0000007F] Motherboard resources
	[00000080 - 00000080] Motherboard resources
	[00000081 - 00000083] Direct memory access controller
	[00000084 - 00000086] Motherboard resources
	[00000087 - 00000087] Direct memory access controller
	[00000088 - 00000088] Motherboard resources
	[00000089 - 0000008B] Direct memory access controller
	[0000008C - 0000008E] Motherboard resources
	[0000008F - 0000008F] Direct memory access controller
	[00000090 - 0000009F] Motherboard resources
	[000000A0 - 000000A1] Programmable interrupt controller
	[000000A2 - 000000BF] Motherboard resources
	[000000C0 - 000000DF] Direct memory access controller
	[000000E0 - 000000EF] Motherboard resources
	[000000F0 - 000000FF] Numeric data processor
	[00000170 - 00000177] Secondary IDE Channel
	[000001F0 - 000001F7] Primary IDE Channel
	[00000274 - 00000277] ISAPNP Read Data Port
	[00000279 - 00000279] ISAPNP Read Data Port
	[000002E8 - 000002EF] Communications Port (COM4)
	[000002F8 - 000002FF] Communications Port (COM2)
	[00000376 - 00000376] Secondary IDE Channel
	[000003B0 - 000003BB] AMD Radeon HD 6250 Graphics
	[000003B0 - 000003DF] PCI bus
	[000003C0 - 000003DF] AMD Radeon HD 6250 Graphics
	[000003E0 - 00000CF7] PCI bus
	[000003E8 - 000003EF] Communications Port (COM3)
	[000003F6 - 000003F6] Primary IDE Channel
	[000003F8 - 000003FF] Communications Port (COM1)
	[0000040B - 0000040B] Motherboard resources
	[000004D0 - 000004D1] Motherboard resources
	[000004D6 - 000004D6] Motherboard resources
	[00000500 - 0000050F] Motherboard resources



	[00000510 - 0000051F]	Motherboard resources
	[00000520 - 0000052F]	Motherboard resources
	[00000800 - 0000089F]	Motherboard resources
	[00000900 - 0000090F]	Motherboard resources
	[00000910 - 0000091F]	Motherboard resources
	[00000A79 - 00000A79]	ISAPNP Read Data Port
	[00000B20 - 00000B3F]	Motherboard resources
	[00000C00 - 00000C01]	Motherboard resources
	[00000C14 - 00000C14]	Motherboard resources
	[00000C50 - 00000C51]	Motherboard resources
	[00000C52 - 00000C52]	Motherboard resources
	[00000C6C - 00000C6C]	Motherboard resources
	[00000C6F - 00000C6F]	Motherboard resources
	[00000CD0 - 00000CD1]	Motherboard resources
	[00000CD2 - 00000CD3]	Motherboard resources
	[00000CD4 - 00000CD5]	Motherboard resources
	[00000CD6 - 00000CD7]	Motherboard resources
	[00000CD8 - 00000CDF]	Motherboard resources
	[00000D00 - 0000FFFF]	PCI bus
	[0000E000 - 0000E0FF]	Realtek PCIe GBE Family Controller
	[0000E000 - 0000EFFF]	PCI standard PCI-to-PCI bridge
	[0000F000 - 0000F0FF]	AMD Radeon HD 6250 Graphics
	[0000F100 - 0000F10F]	Standard Dual Channel PCI IDE Controller
	[0000FE00 - 0000FEFE]	Motherboard resources























## B.2 1<sup>st</sup> MB Memory Address Map

---

Memory	
[000A0000 - 000BFFFF]	AMD Radeon HD 6250 Graphics
[000A0000 - 000BFFFF]	PCI bus
[000C0000 - 000DFFFF]	PCI bus
[A8000000 - BFFFFFFF]	Motherboard resources
[C0000000 - CFFFFFFF]	AMD Radeon HD 6250 Graphics
[C0000000 - FFFFFFFF]	PCI bus
[D0000000 - D0003FFF]	Realtek PCIe GBE Family Controller
[D0000000 - D00FFFFF]	PCI standard PCI-to-PCI bridge
[D0004000 - D0004FFF]	Realtek PCIe GBE Family Controller
[E0000000 - EFFFFFFF]	System board
[FEB00000 - FEB3FFFF]	AMD Radeon HD 6250 Graphics
[FEB40000 - FEB43FFF]	Microsoft UAA Bus Driver for High Definition Audio
[FEB44000 - FEB47FFF]	Microsoft UAA Bus Driver for High Definition Audio
[FEB48000 - FEB480FF]	Standard Enhanced PCI to USB Host Controller
[FEB49000 - FEB49FFF]	Standard OpenHCD USB Host Controller
[FEB4A000 - FEB4A0FF]	Standard Enhanced PCI to USB Host Controller
[FEB4B000 - FEB4BFFF]	Standard OpenHCD USB Host Controller
[FEB4C000 - FEB4C0FF]	Standard Enhanced PCI to USB Host Controller
[FEB4D000 - FEB4DFFF]	Standard OpenHCD USB Host Controller
[FEC00000 - FEC00FFF]	Motherboard resources
[FEC10000 - FEC10FFF]	Motherboard resources
[FED00000 - FED003FF]	High precision event timer
[FED00000 - FED00FFF]	Motherboard resources


## B.3 IRQ Mapping Chart

---

Interrupt request (IRQ)	
	(ISA) 0 System timer
	(ISA) 1 Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
	(ISA) 3 Communications Port (COM2)
	(ISA) 4 Communications Port (COM1)
	(ISA) 8 System CMOS/real time clock
	(ISA) 9 Microsoft ACPI-Compliant System
	(ISA) 11 Communications Port (COM3)
	(ISA) 11 Communications Port (COM4)
	(ISA) 12 Microsoft PS/2 Mouse
	(ISA) 13 Numeric data processor
	(ISA) 14 Primary IDE Channel
	(PCI) 16 Microsoft UAA Bus Driver for High Definition Audio
	(PCI) 16 PCI standard PCI-to-PCI bridge
	(PCI) 16 Realtek PCIe GBE Family Controller
	(PCI) 17 Standard Enhanced PCI to USB Host Controller
	(PCI) 17 Standard Enhanced PCI to USB Host Controller
	(PCI) 17 Standard Enhanced PCI to USB Host Controller
	(PCI) 18 AMD Radeon HD 6250 Graphics
	(PCI) 18 Standard OpenHCD USB Host Controller
	(PCI) 18 Standard OpenHCD USB Host Controller
	(PCI) 18 Standard OpenHCD USB Host Controller
	(PCI) 19 Microsoft UAA Bus Driver for High Definition Audio

## B.4 DMA Channel Assignments

---

Direct memory access (DMA)	
	4 Direct memory access controller

Appendix

C

# Mating Connector

## C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model number		
CN1	CRT Connector	CATCH	H752-13	VGA Cable	1709150151
CN2	Audio Line In/Out and MIC Connector	CATCH	H752-10	Audio Cable	1709100254
CN3	LVDS Backlight Connector	CATCH	H738-05	LVDS Backlight Cable	1705050153
CN5	Internal LVDS Connector(18bit)	HIROSE	DF13-20S-1.25C	Internal LVDS Cable	1704200200
CN7	LAN Connector	CATCH	H820-2-10	LAN Cable	1700100201
CN11	USB2.0 Connector	CATCH	H752-05	USB2.0 Cable	1700050207
CN12	USB2.0 Connector	CATCH	H752-05	USB2.0 Cable	1700050207
CN13	USB2.0 Connector	CATCH	H752-05	USB2.0 Cable	1700050207
CN14	USB2.0 Connector	CATCH	H752-05	USB2.0 Cable	1700050207
CN19	SATA Power Connector	CATCH	H732-02	SATA Power Cable	1702150155
CN20	SATA Connector	HI-TOP	SA07FGP	SATA Cable	1709070500
CN22	COM1 RS232 Connector	CATCH	H752-09	COM Cable	1701090150

CN23	COM3 RS232 Connector	CATCH	H752-09	COM Cable	1701090150
CN24	COM4 RS232 Connector	CATCH	H752-09	COM Cable	1701090150
CN25	COM2 RS232/422/ 485 Connector	CATCH	H752-09	COM Cable	1701090150
CN27	Digital I/O Connector	CATCH	H752-10	Digital I/O Cable	1701010150
CN33	Power Input Connector	HOBASE	A2501H02-06	Power Input Cable	1702060105
CN34	Front Panel Connector	CATCH	H752-10	Front Panel Cable	1701010150
CN35	PS/2 Keyboard & Mouse	CATCH	H752-06	PS/2 Keyboard & Mouse Cable	1700060155
CN37	Stereo-R Channel	HOBASE	A1251H02-2	Stereo-R Channel Cable	N/A
CN38	Stereo-L Channel	HOBASE	A1251H02-2	Stereo-L Channel Cable	N/A

Appendix

**D**

**AHCI Setting**

## D.1 Setting AHCI

---

OS installation to SETUP AHCI Mode

Step 1: Copy files from “Driver DVD -> Step6 – AHCI(Optional)\WinXP\_32” to diskette.



Step 2: Connect the USB Floppy drive to the board and insert the diskette from previous step.

Step 3: Configure SATA Controller to AHCI mode in **BIOS SETUP**

Step 4: Boot to DVD/CD-ROM device to install OS

Step 5: Press “**F6**” to install AHCI driver





Step 6: Press “S” to install AHCI driver



Step 7: Choose “**AMD AHCI Compatible RAID Controller-x86 platform**” for Windows XP 32-bit system; “**AMD AHCI Compatible RAID Controller-x64 platform**” for Windows XP 64-bit system.

Step 8: Windows Setup will display the controller name you selected in previous step and continue to install OS when “**ENTER**” pressed.

Appendix

**E**

**Digital I/O Ports**

## E.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification						
Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO1	I/O	0.8	2.0	0	3.3	
DIO2	I/O	0.8	2.0	0	3.3	
DIO3	I/O	0.8	2.0	0	3.3	
DIO4	I/O	0.8	2.0	0	3.3	
DIO5	I/O	0.8	2.0	0	3.3	
DIO6	I/O	0.8	2.0	0	3.3	
DIO7	I/O	0.8	2.0	0	3.3	
DIO8	I/O	0.8	2.0	0	3.3	

**Note:** All DIO pins are 5V tolerance in input mode.

## E.2 DIO Programming

---

PFM-HDS utilizes FINTEK F81866D chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DIO program is also attached based on which you can develop customized program to fit your application. There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

### E.3 Digital I/O Register

	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

	LDN	Register	BitNum	Note
GPIO1 Direction	0x06	0x88	0	0:input, 1: output
GPIO2 Direction	0x06	0x88	1	
GPIO3 Direction	0x06	0x88	2	
GPIO4 Direction	0x06	0x88	3	
GPIO5 Direction	0x06	0x88	4	
GPIO6 Direction	0x06	0x88	5	
GPIO7 Direction	0x06	0x88	6	
GPIO8 Direction	0x06	0x88	7	
GPIO1 Output Level	0x06	0x89	0	0:low, 1: high
GPIO2 Output Level	0x06	0x89	1	
GPIO3 Output Level	0x06	0x89	2	
GPIO4 Output Level	0x06	0x89	3	
GPIO5 Output Level	0x06	0x89	4	
GPIO6 Output Level	0x06	0x89	5	
GPIO7 Output Level	0x06	0x89	6	
GPIO8 Output Level	0x06	0x89	7	
GPIO1 Status	0x06	0x8A	0	0:low, 1: high
GPIO2 Status	0x06	0x8A	1	
GPIO3 Status	0x06	0x8A	2	
GPIO4 Status	0x06	0x8A	3	
GPIO5 Status	0x06	0x8A	4	
GPIO6 Status	0x06	0x8A	5	
GPIO7 Status	0x06	0x8A	6	
GPIO8 Status	0x06	0x8A	7	

## E.4 Digital I/O Sample Program

---

```

*****
// SuperIO relative definition (Please reference to Table 2)
#define SI0Index 0x2E
#define SI0Data 0x2F
#define DI0LDN 0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// D10 relative definition (Please reference to Table 3)
#define DirReg 0x88 // 0:input, 1: output
    #define InputPin 0x00
    #define OutputPin 0x01
#define OutputReg 0x89 // 0:low, 1: high
#define StatusReg 0x8A // 0:low, 1: high
    #define PinLow 0x00
    #define PinHigh 0x01
#define Pin1Bit 0x00
#define Pin2Bit 0x01
#define Pin3Bit 0x02
#define Pin4Bit 0x03
#define Pin5Bit 0x04
#define Pin6Bit 0x05
#define Pin7Bit 0x06
#define Pin8Bit 0x07
*****

*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    // Example, Read Digital I/O Pin 3 status
    // Output :
    // InputStatus :

```

```

//          0: Digital I/O Pin level is low
//          1: Digital I/O Pin level is High
PinStatus = AaeonReadPinStatus(Pin3Bit);

// Procedure : AaeonSetOutputLevel
// Input :
// Example, Set Digital I/O Pin 2 to high level
AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****

*****
Boolean AaeonReadPinStatus(byte PinBit){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(DIOLDN, StatusReg, PinBit);
    Return PinStatus ;
}
VOID AaeonSetOutputLevel(byte PinBit, byte Value){
    ConfigDioMode(PinBit, OutputPin);
    SIOBitSet(DIOLDN, OutputReg, PinBit, Value);
}
*****
*****

*****VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07

```

```

        IOWriteByte(SIOData, LDN);
    }

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}

*****
*****

```



```

*****
Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID ConfigDioMode(byte PinBit, byte Mode){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(DIOLDN);
    IOWriteByte(SIOIndex, DirReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (Mode << PinBit);
    IOWriteByte(SIOData, DirReg);
    SIOExitMBPnPMode();
}
*****

```