NanoCOM-WHU Rev B

COM Express Module

User's Manual 1st Ed

Last Updated: June 23, 2021

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● NanoCOM-WHU Rev B	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	X	O	O	O	O	O
Wires & Connectors for External Connections	X	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

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Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	COM Express Mini, 84mm x 55mm
CPU	8th Generation Intel® Core™ ULT Series Processors
CPU Frequency	—
Chipset	Onboard 8th Generation Intel® Core™ SoC
Memory Type	Onboard DDR4-2400/2133, non ECC support.
Max. Memory Capacity	Up to 8GB
BIOS	AMI BIOS, Legacy free BIOS
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	Standard: +12V
Power Supply Type	AT Mode
Power Consumption (Typical)	TBD
Dimension (L x W)	3.31" x 2.17" (84 mm x 55 mm)
Operating Temperature	32°F~ 140°F (0°C ~ 60°C)
Storage Temperature	-4°F ~ 158°F (-20°C ~ 70°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	TBD
Certification	CE/FCC Class A

Display

VGA/LCD Controller	Intel® UHD Graphics 620 / 610
Video Output	eDP, DDI x 1
LVDS Interface	—

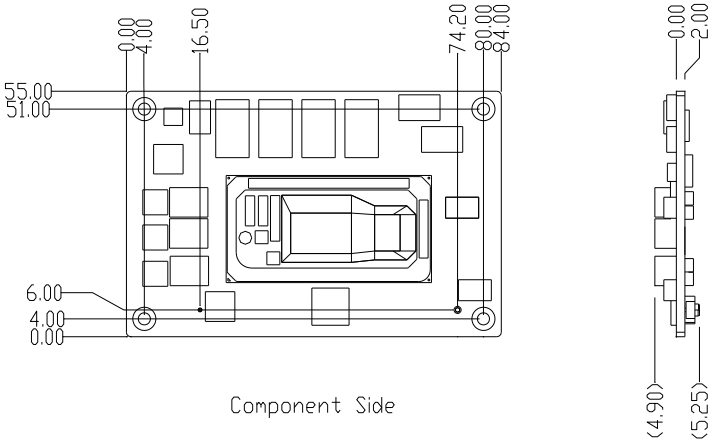
I/O

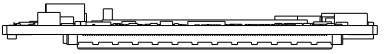
Ethernet	Intel® i219 Gbps Ethernet x 1
Audio	HD Audio x 1
USB port	USB3.2 Gen 2 x 2
	USB2.0 x 8
Serial Port	2-wire UART x 2 (TX/RX)
HDD Interface	SATA3 x 2
Onboard Storage	eMMC
Expansion Slot	PCIe [x1] x4
	I2C
	LPC
	SMBus
GPIO	8-bit
TPM	fTPM

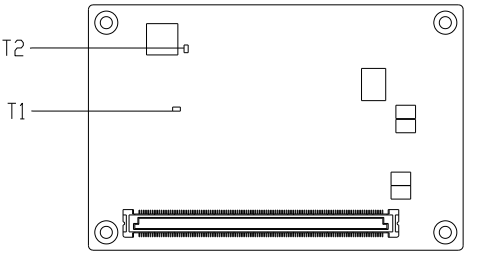
Chapter 2

Hardware Information

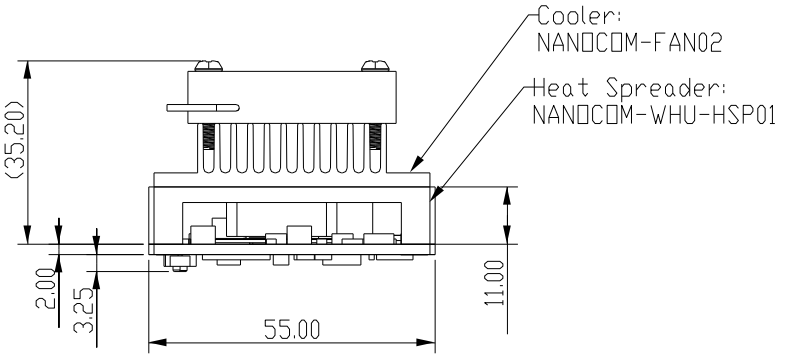
2.1 Dimensions





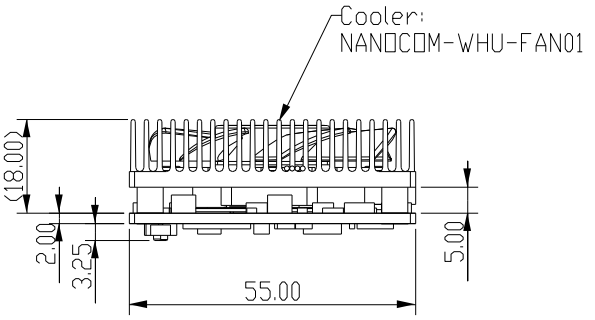


With Standard Thermal Solution



Unit:mm

With one-piece Thermal Solution



Unit:mm

2.2 Row A/B Connector Pin Definitions

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	N.C	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB3_RXN0	B22	USB3_TXN0
A23	USB3_RXP0	B23	USB3_TXP0
A24	SUS_S4#	B24	PWR_OK

Row A		Row B	
A25	USB3_RX1_N	B25	USB3_TX1_N
A26	USB3_RX1_P	B26	USB3_TX1_P
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	N.C
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	N.C
A48	N.C	B48	N.C
A49	N.C	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#

Row A		Row B	
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C	B52	N.C
A53	N.C	B53	N.C
A54	GPI0	B54	GPO1
A55	N.C	B55	N.C
A56	N.C	B56	N.C
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+(EDP_TX2_P)	B71	DDI0_PAIR0+
A72	LVDS_A0-(EDP_TX2_N)	B72	DDI0_PAIR0-
A73	LVDS_A1+(EDP_TX1_P)	B73	DDI0_PAIR1+
A74	LVDS_A1-(EDP_TX1_N)	B74	DDI0_PAIR1-
A75	LVDS_A2+(EDP_TX0_P)	B75	DDI0_PAIR2+
A76	LVDS_A2-(EDP_TX0_N)	B76	DDI0_PAIR2-

Row A		Row B	
A77	LVDS_VDD_EN(EDP_VDDEN_3_3)	B77	N.C
A78	LVDS_A3+	B78	N.C
A79	LVDS_A3-	B79	LVDS_BKLD_EN(EDP_BKLTEN_3_3)
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+(EDP_TX3_P)	B81	DDI0_PAIR3+
A82	LVDS_A_CK-(EDP_TX3_N)	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK(EDP_AUXP)	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT(EDP_AUXN)	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	EC_KBRST#(option)	B86	VCC_5V_SBY
A87	EDP_HPD_A87	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	N.C
A92	SPI_MISO	B92	N.C
A93	GPO0	B93	N.C
A94	SPI_CLK	B94	N.C
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	GND	B96	N.C
A97	Pull down 47k ohm to GND	B97	SPI_CS#
A98	RS1_TX	B98	DDI0_CTRL_CLK
A99	RS1_RX	B99	DDI0_CTRL_DATA
A100	GND (FIXED)	B100	GND (FIXED)
A101	RS2_TX	B101	FAN_PWMOUT
A102	RS2_RX	B102	FAN_TACHIN

Row A		Row B	
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Manage advanced hardware settings and options

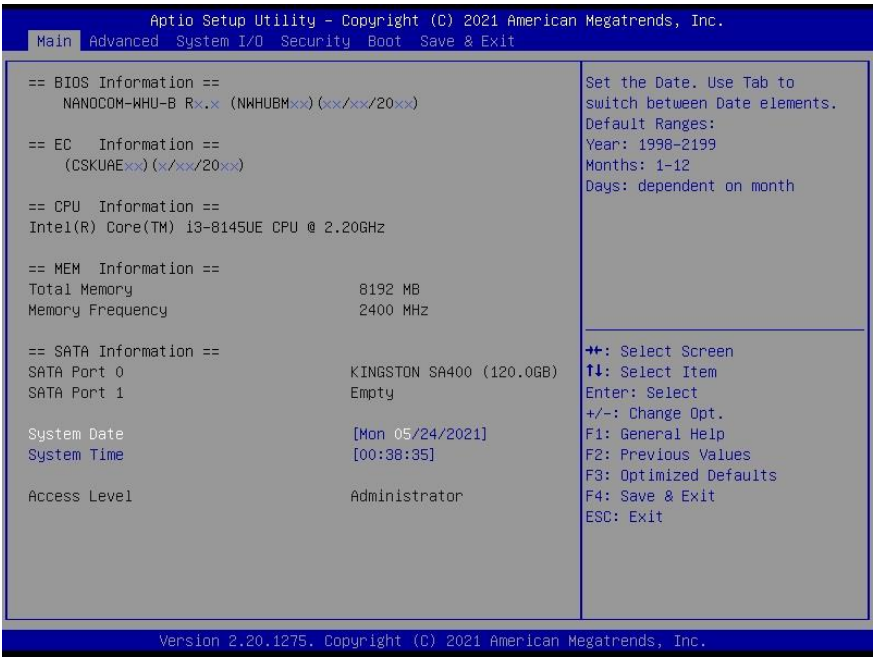
System I/O – Configure I/O settings including PCI Express and storage options

Security – Security options including setup administrator password, Secure Boot and Key Management

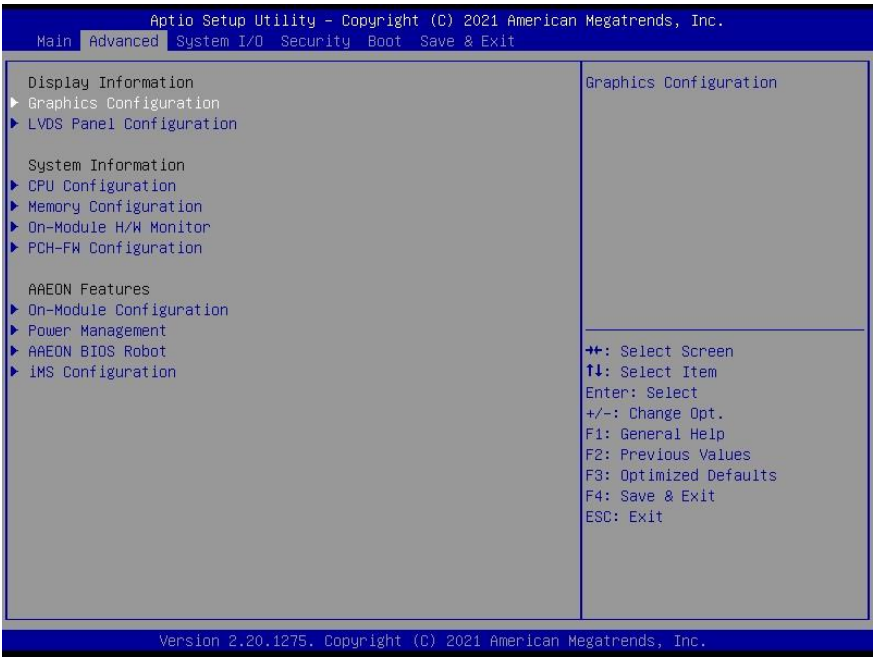
Boot – Manage boot options including BBS Priority and Quiet Boot.

Save & Exit –Save your changes and exit the program

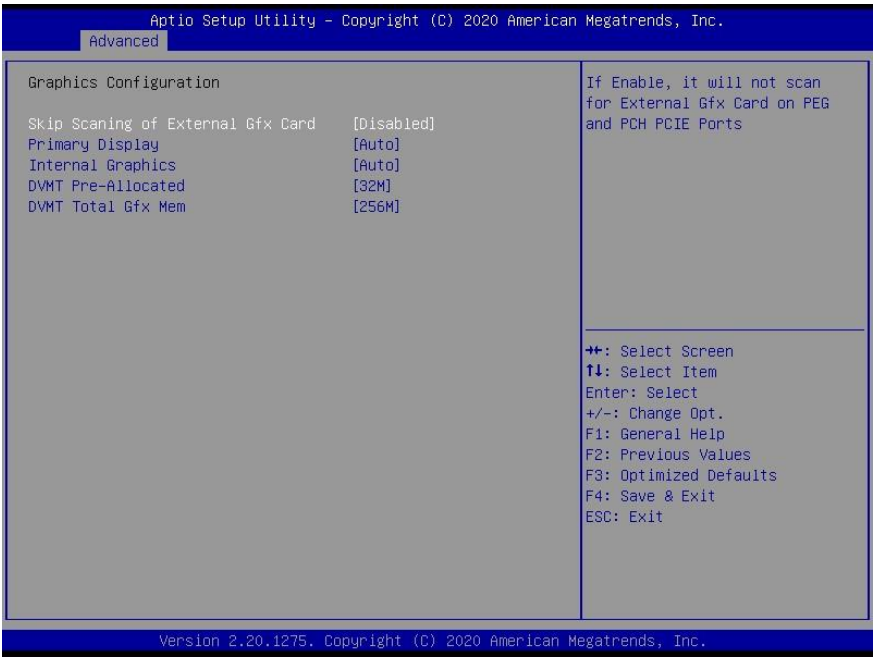
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



3.4.1 Graphics Configuration

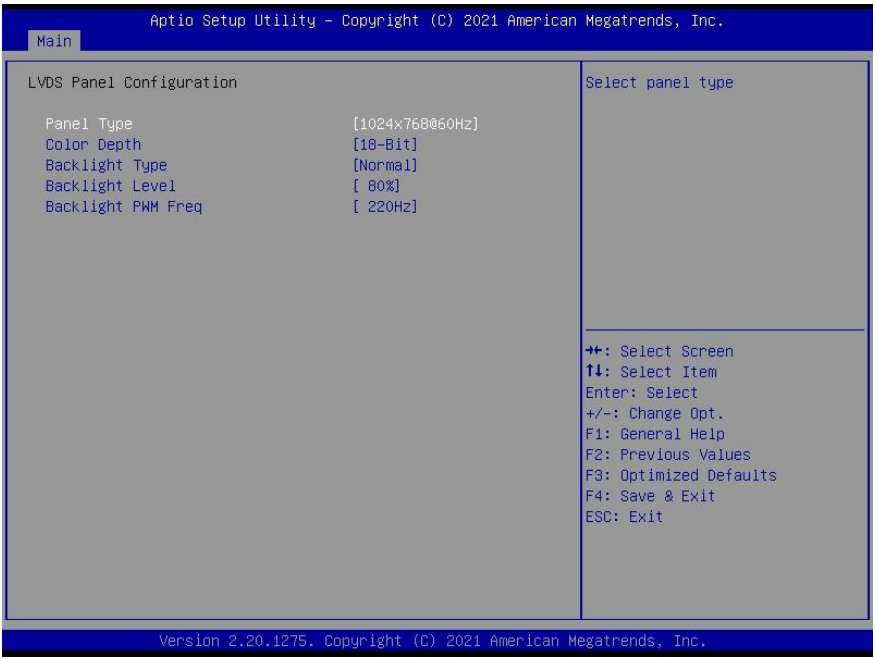


Options Summary		
Skip Scanning of External Gfx Card	Enable	
	Disable	Optimal Default, Failsafe Default
If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports.		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFS	
	PCI	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Internal Graphics	Auto	Optimal Default, Failsafe Default
	Disabled	
	Enabled	
Keep IGFS enabled based on the setup options.		

Table Continues on Next Page…

Options Summary		
DVMT Pre-Allocated	0M	
	32M	Optimal Default, Failsafe Default
	64M	
	4M	
	8M	
	12M	
	16M	
	20M	
	24M	
	28M	
	32M/F7	
	36M	
	40M	
	44M	
	48M	
	52M	
	56M	
	60M	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128M	
	256M	Optimal Default, Failsafe Default
	MAX	

3.4.2 LVDS Panel Configuration



Options Summary		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x800@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	
Select panel type		

Options Summary		
Color Depth	18-Bit	Optimal Default, Failsafe Default
	24-Bit	
	36-Bit	
	48-Bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM Frequency of backlight control signal		

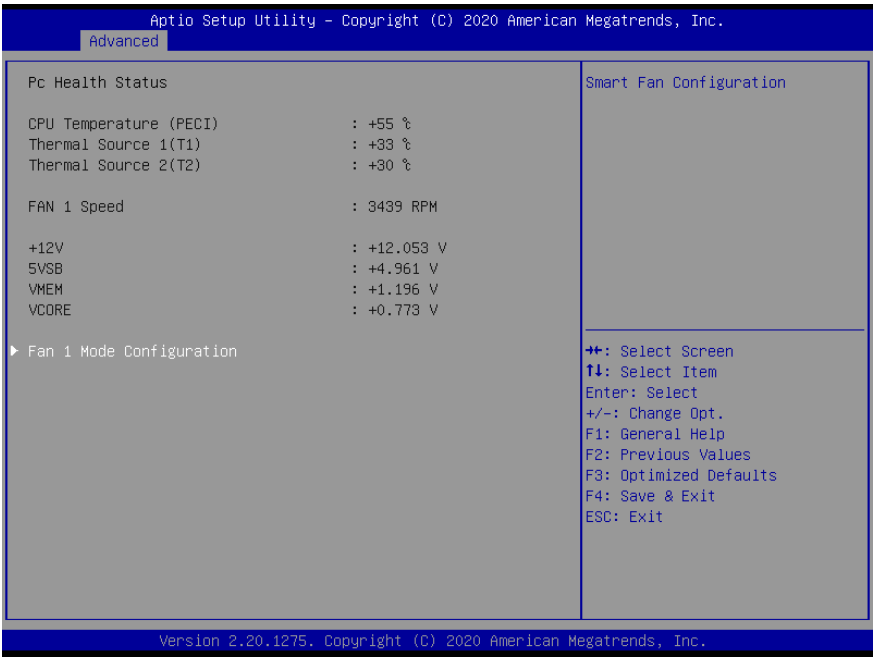
3.4.3 CPU Configuration

Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disabled Hyper-Threading Technology.		
Intel Trusted Execution Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology. Changes require a full power cycle to take effect.		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		

Options Summary		
Intel® SpeedStep™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).		

3.4.4 Memory Configuration

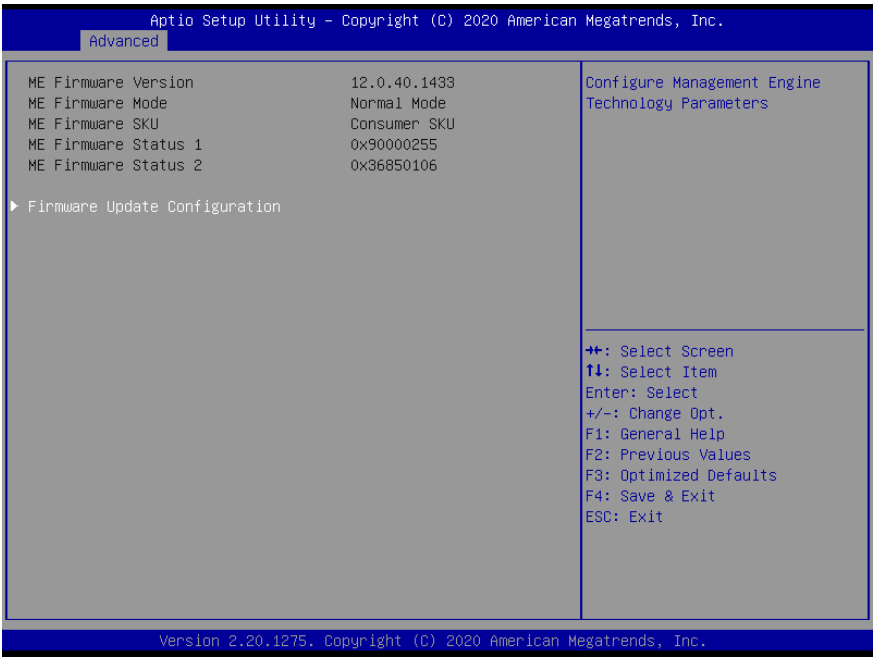
3.4.5 On-Module H/W Monitor



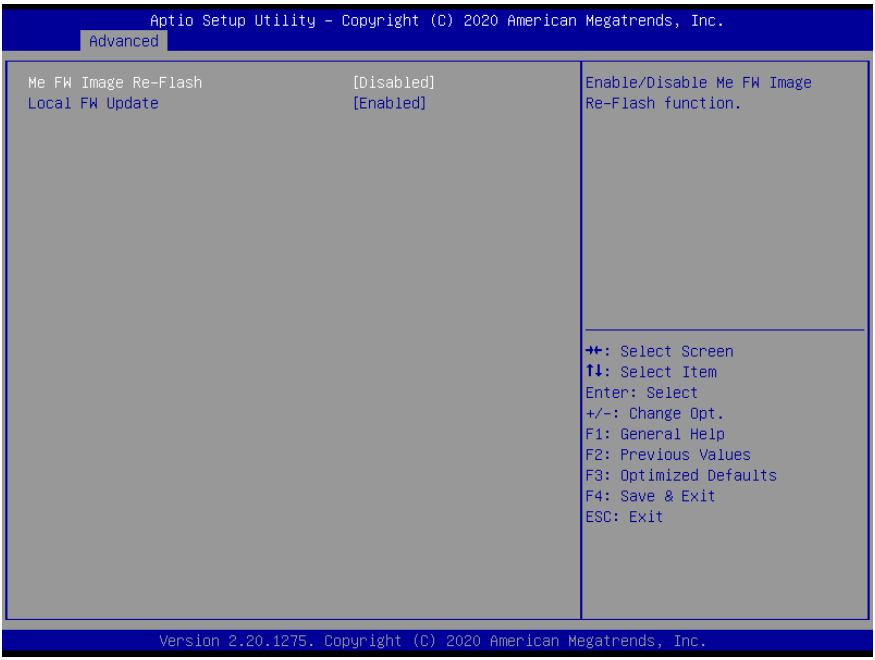
3.4.5.1 Fan 1 Mode Configuration

Options Summary		
FAN 1	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
Choose the mode for FAN 1.		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal.		

3.4.6 PCH-FW Configuration

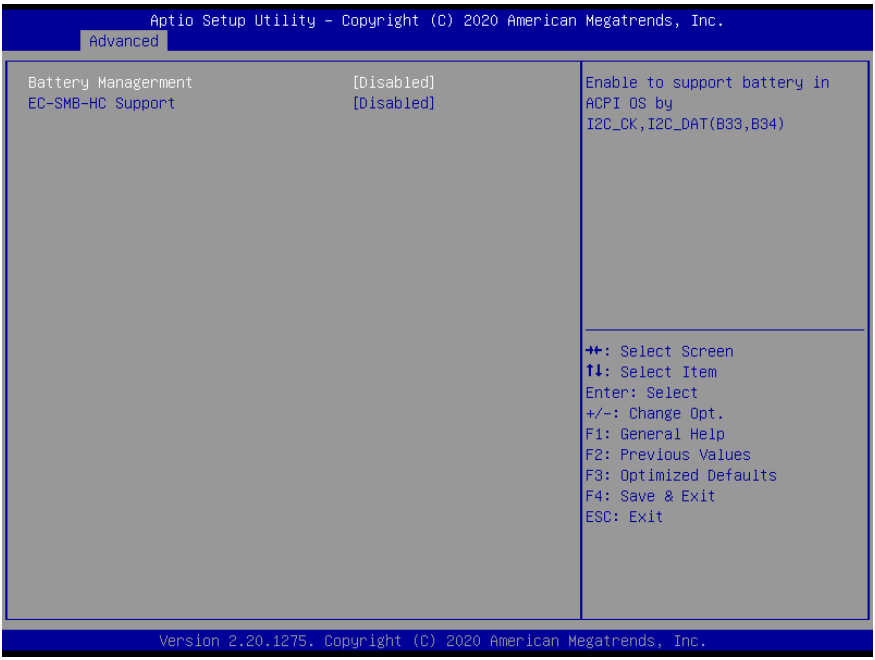


3.4.6.1 Firmware Update Configuration



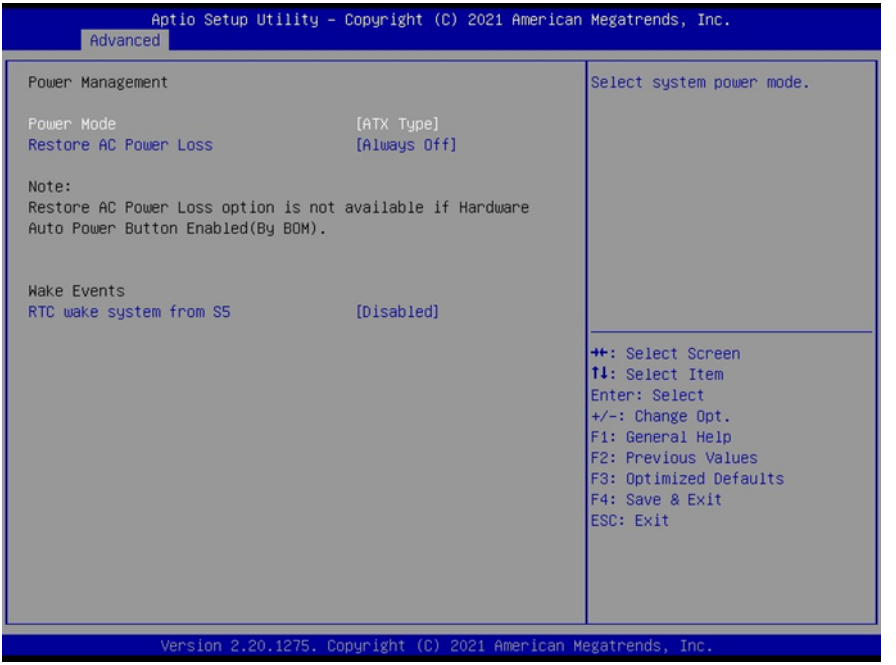
Options Summary		
Me FW Image Re-Flash	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable/Disable Me FW Image Re-Flash function.		
Local FW Update	Enabled	Optimal Default, Failsafe Default
	Disabled	
Options for Local FW Update function.		

3.4.7 On-Module Configuration



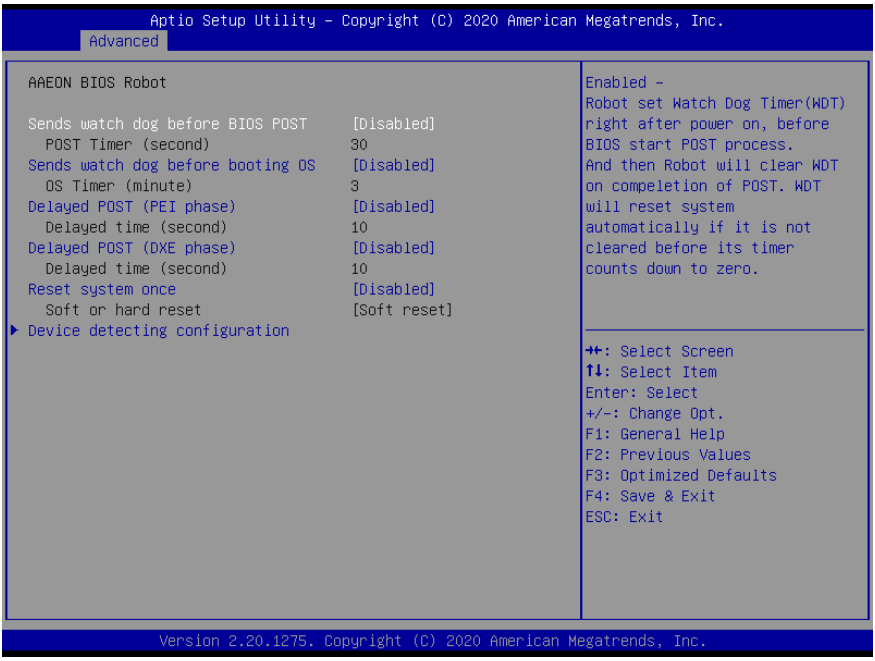
Options Summary		
Battery Management	Disabled	Optimal Default, Failsafe Default
	One Battery	
Enable to support battery in ACPI OS by I2C_CK, I2C_DAT(B33,B34)		
EC-SMB-HC Support	Enabled	
	Disabled	Optimal Default, Failsafe Default
SMBus Host Controller Interface via Embedded Controller.		

3.4.8 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
IO Restore AC Power Loss. **Note:** Restore AC Power Loss option is not available if Hardware Auto Power Button is Enabled (by BIOS option menu)		
RTC wake system from S5.	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time: System will wake on the hr:min:sec specified. Dynamic Time: System will wake on the current time + Increase minute(s)		

3.4.9 AAEON BIOS Robot

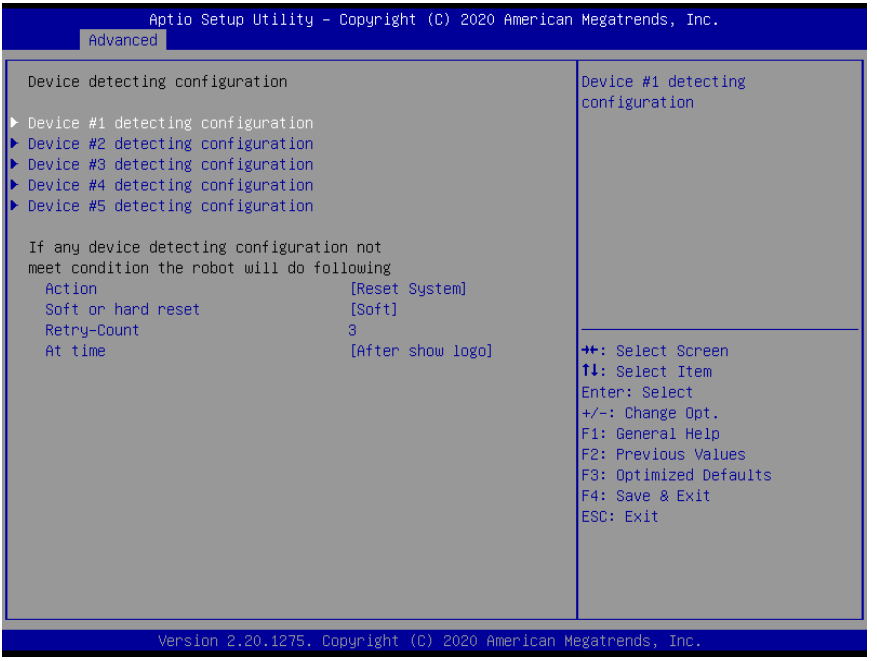


Options Summary		
Sends watch dog before BIOS POST.	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) right after power on, before BIOS start POST process. And then Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfer control to OS. WARNING: Before enabling this function, a program in OS must be in responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		

Table Continues on Next Page

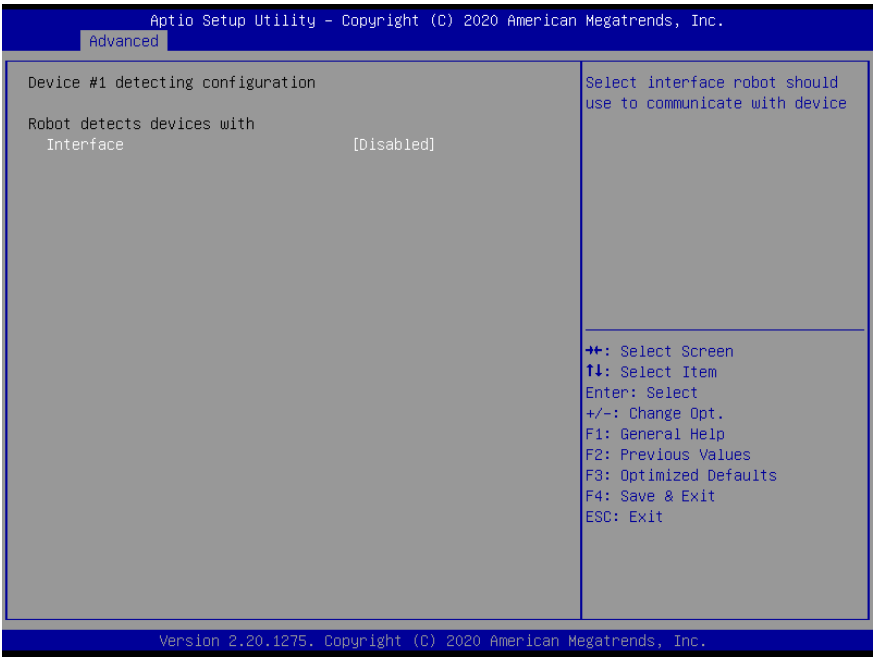
Options Summary		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled – Robot holds BIOS from starting POST, right after power. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled – Robot holds BIOS from starting POST, right after power. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.		
Reset System once	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled – Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		

3.4.9.1 Device Detecting Configuration



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let the system continues its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo: Robot will do action after logo is displayed. System devices are almost ready. Before show logo: Robot will do action earlier before logo, but some devices may not be ready.		

3.4.9.1.1 Device #1~5 Detecting Configuration



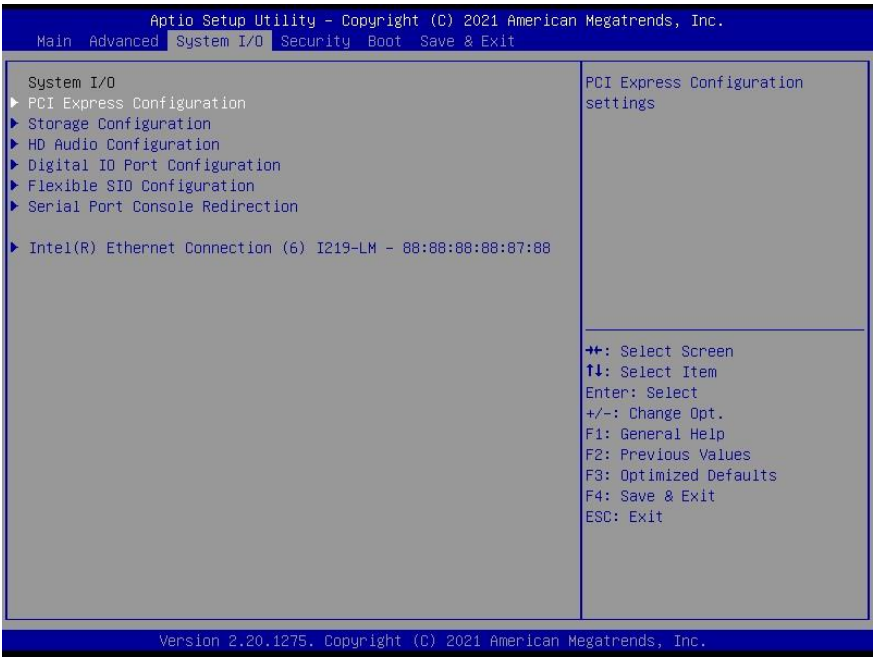
Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

Note: This menu is the same for all Devices #1 thru #5.

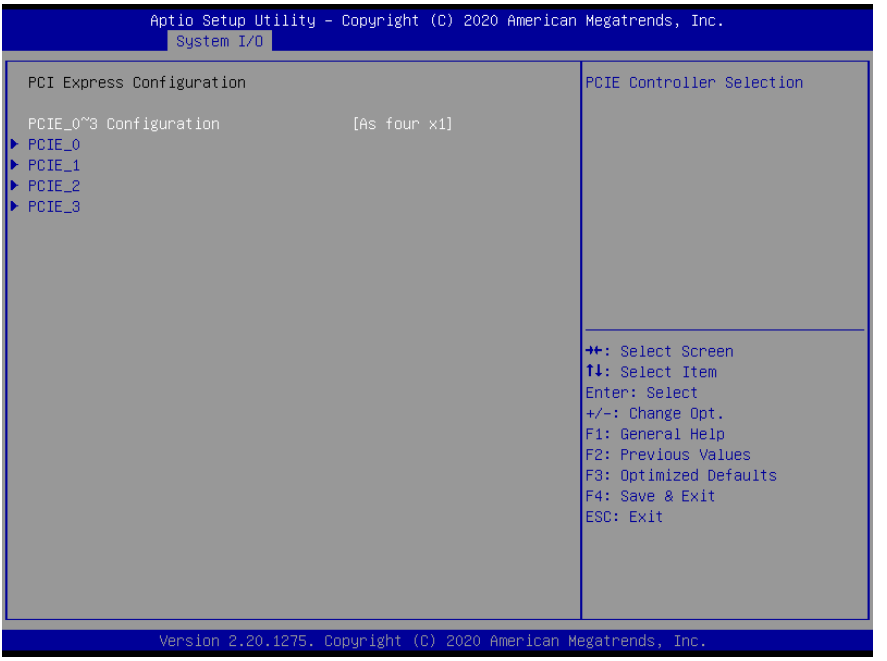
3.4.10 iMS Configuration

Options Summary		
iMS Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Intelligent Memory Surveillance		

3.5 Setup Submenu: System I/O

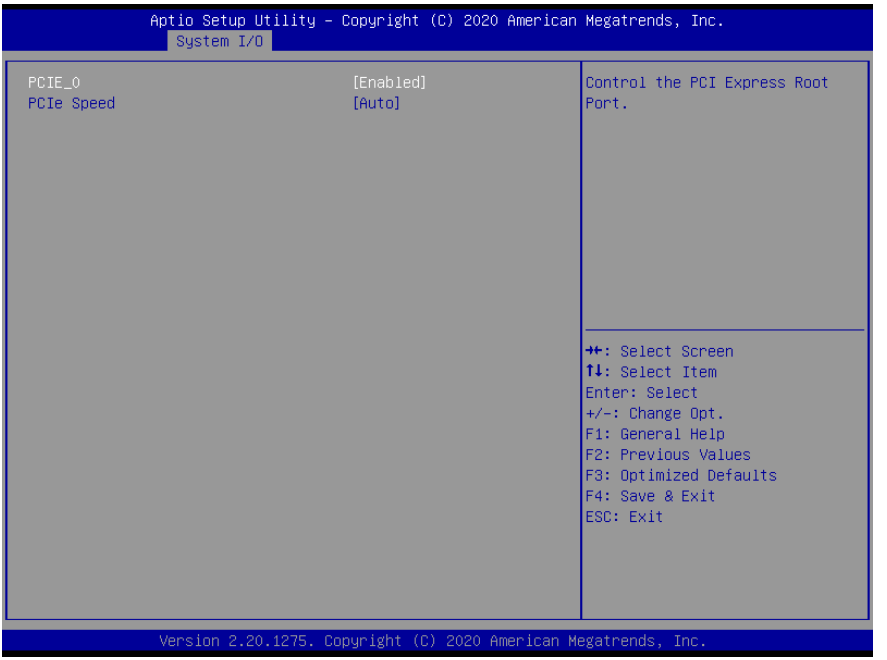


3.5.1 PCI Express Configuration



Options Summary		
PCIE_0~3 Configuration	As four x1	Optimal Default, Failsafe Default
	As one x2 and two x1	
	As two x2	
	As one x4	
PCIE Controller Selection.		

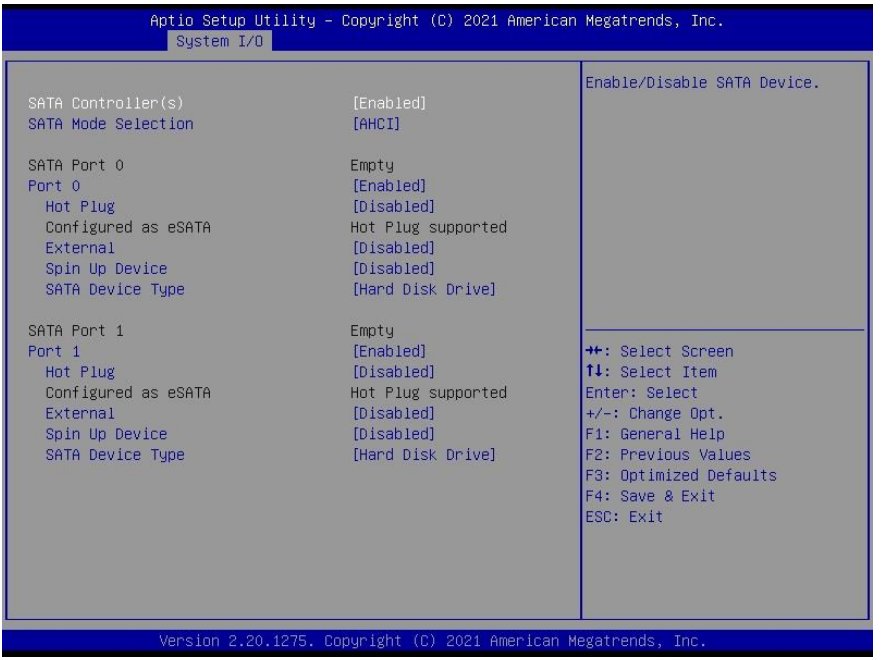
3.5.1.1 PCIE_# Configuration



Options Summary		
PCIE_N	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed.		

Note: This menu is the same for PCIE_0, PCIE_1, PCIE_2, and PCIE_3.

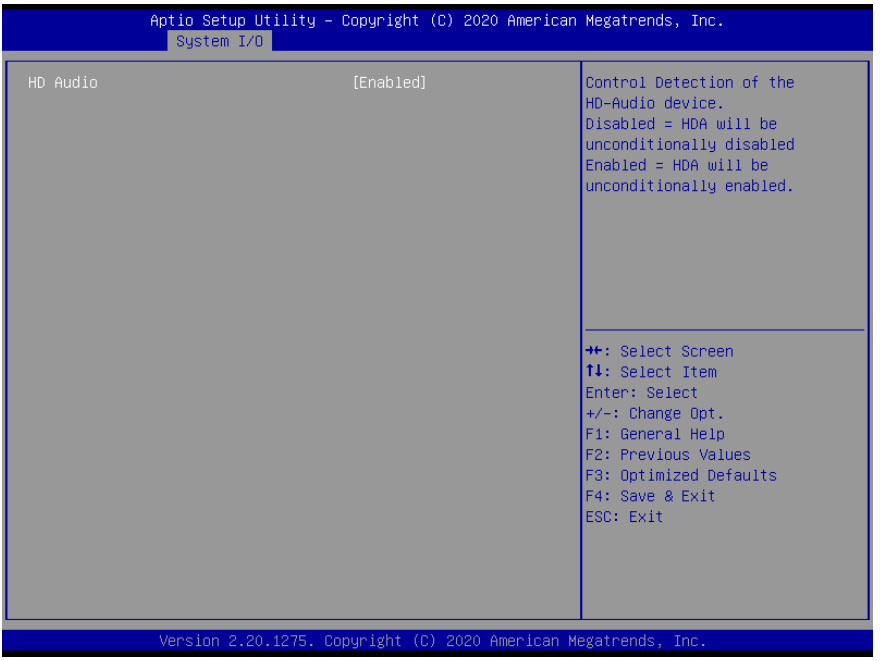
3.5.2 Storage Configuration



Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable SATA Device.		
SATA Mode Selection	AHCI	Optimal Default, Failsafe Default
	Intel RST Premium with Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
SATA Port 0/1 Configuration		
Port 0/1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port 0/1		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

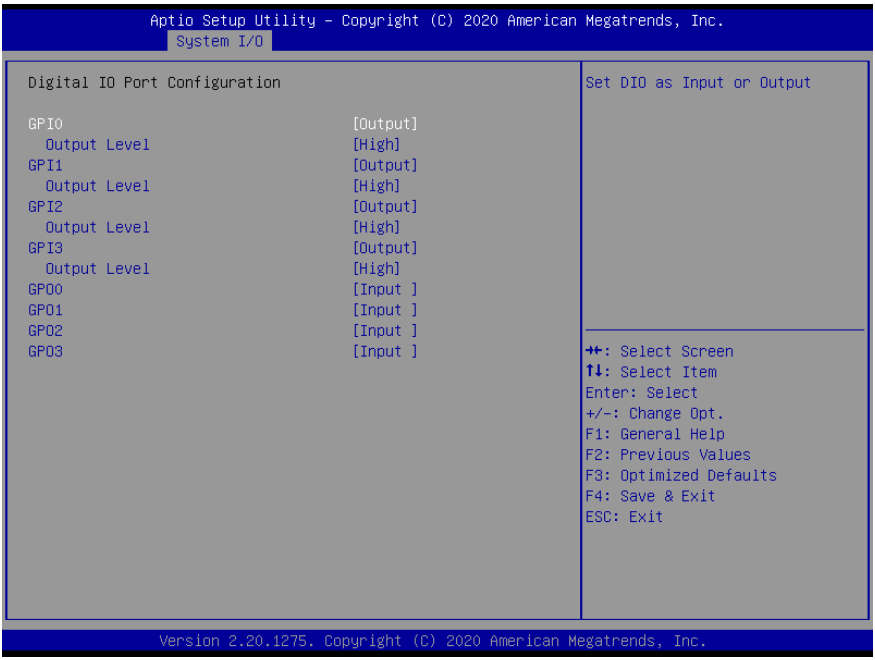
Options Summary		
External	Disabled	Optimal Default, Failsafe Default
	Enabled	
Marks this port as external.		
Spin Up Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.		
SATA Device Type	Hard Disk Drive	Optimal Default, Failsafe Default
	Solid State Drive	
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.		

3.5.3 HD Audio Configuration



Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled: HD-Audio will be unconditionally disabled. Enabled: HD-Audio will be unconditionally disabled.		

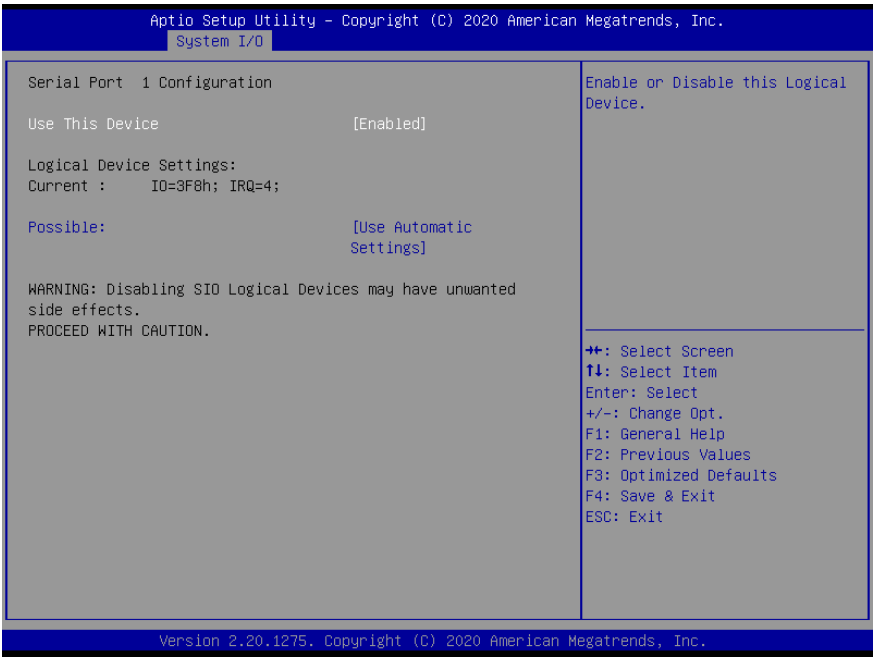
3.5.4 Digital IO Port Configuration



Options Summary		
IO Type	Output	Optimal Default, Failsafe Default
	Input	
Set IO as Input or Output		
IO Data	Low	
	High	Optimal Default, Failsafe Default
Set is output level when DIO pin is output		

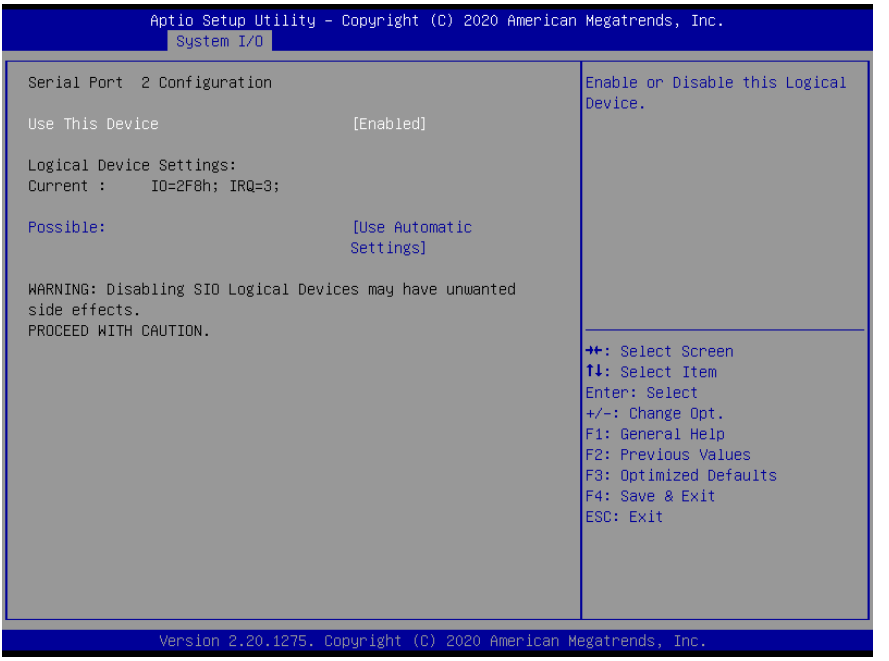
3.5.5 Legacy Logical Devices Configuration

3.5.5.1 [*Active*] Serial Port 1



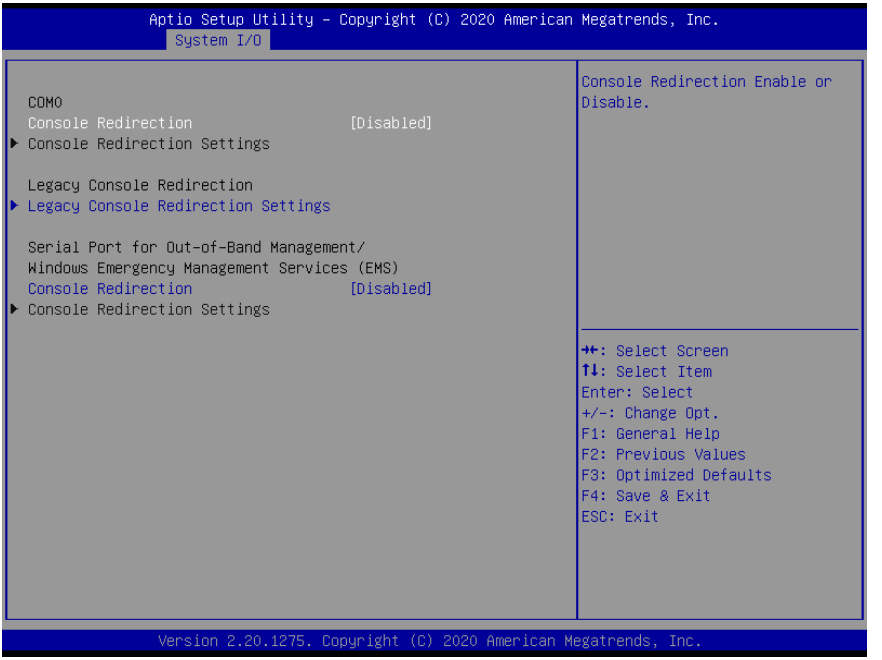
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4; DMA;	
	IO=2C8h; IRQ=11; DMA	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.5.2 [*Active*] Serial Port 2



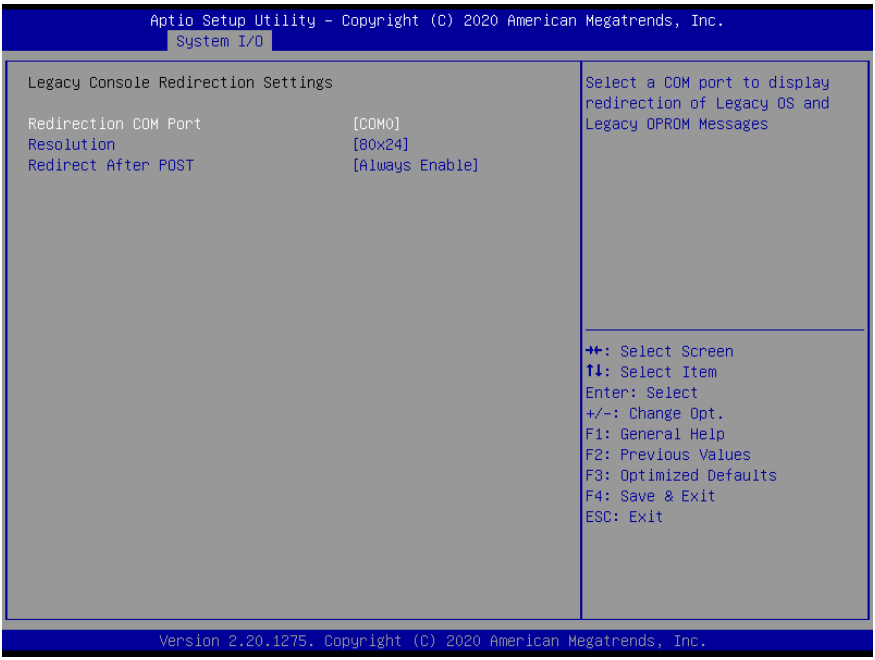
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3; DMA;	
	IO=2D8h; IRQ=10; DMA	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.6 Serial Port Console Redirection



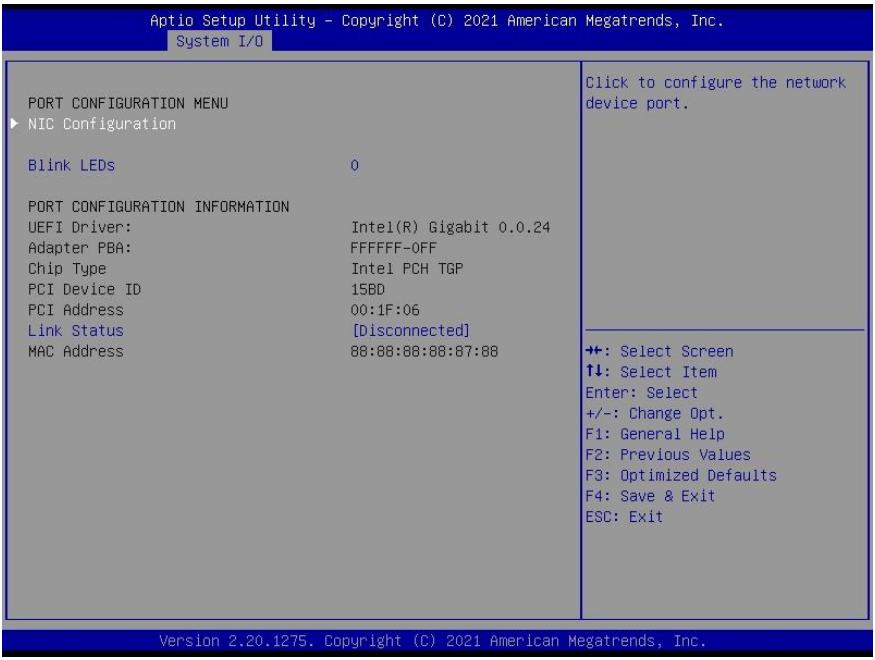
Options Summary		
Console Redirection (COM0)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.5.6.1 Legacy Console Redirection Settings



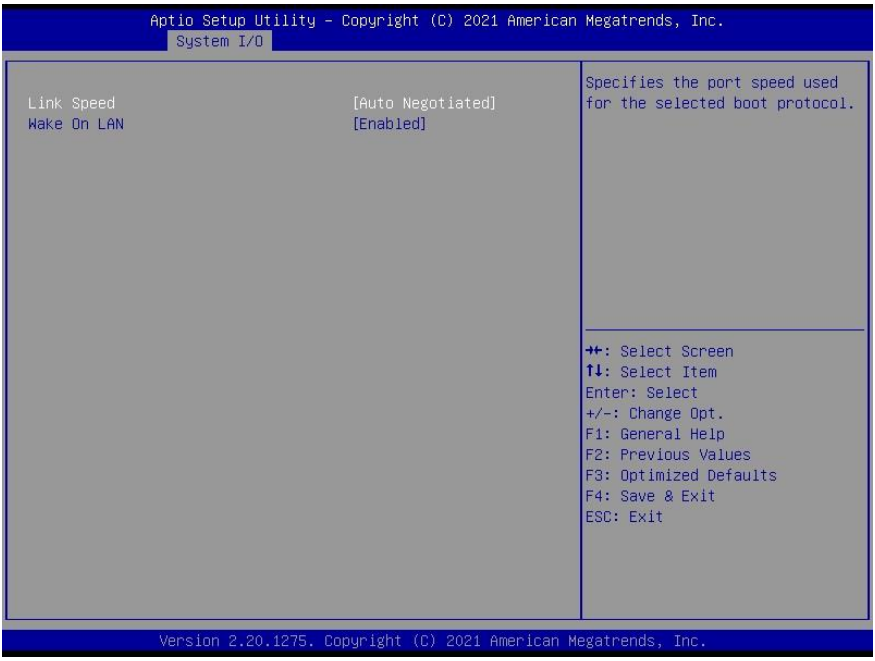
Options Summary		
Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection.		
Redirect After POST	Always Enable	Optimal Default, Failsafe Default
	Bootloader	
When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.		

3.5.7 Intel(R) Ethernet Connection (6) I219-LM



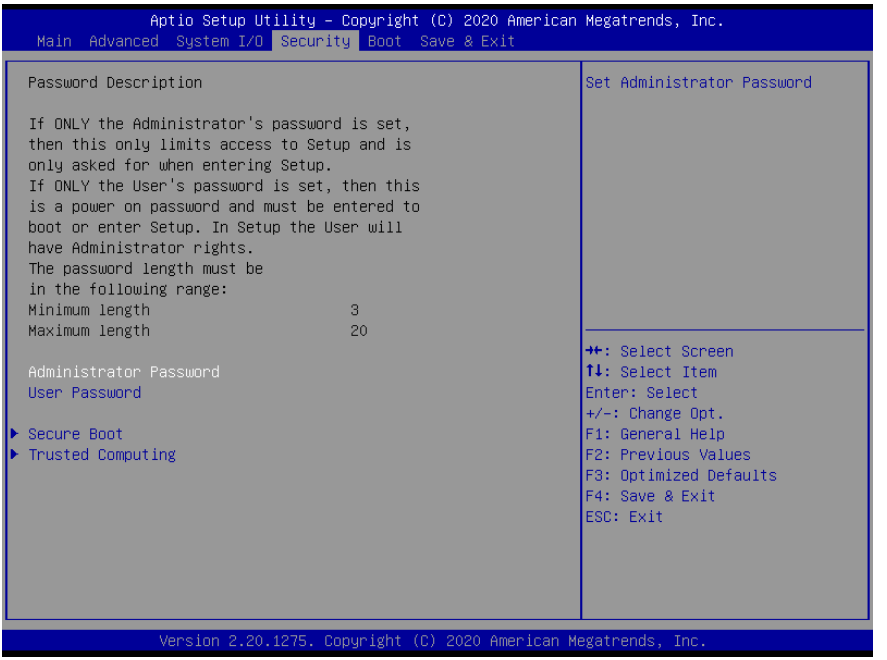
Options Summary		
Blink LEDs	0	Optimal Default, Failsafe Default
Identify the physical network port by blinking the associated LED.		

3.5.7.1 NIC Configuration



Options Summary		
Link Speed	Auto Negotiated	Optimal Default, Failsafe Default
	10 Mbps Half	
	10 Mbps Full	
	100 Mbps Half	
	100 Mbps Full	
Specifies the port speed used for the selected boot protocol.		
Wake On LAN	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables the server to be powered on using an in-band magic packet.		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

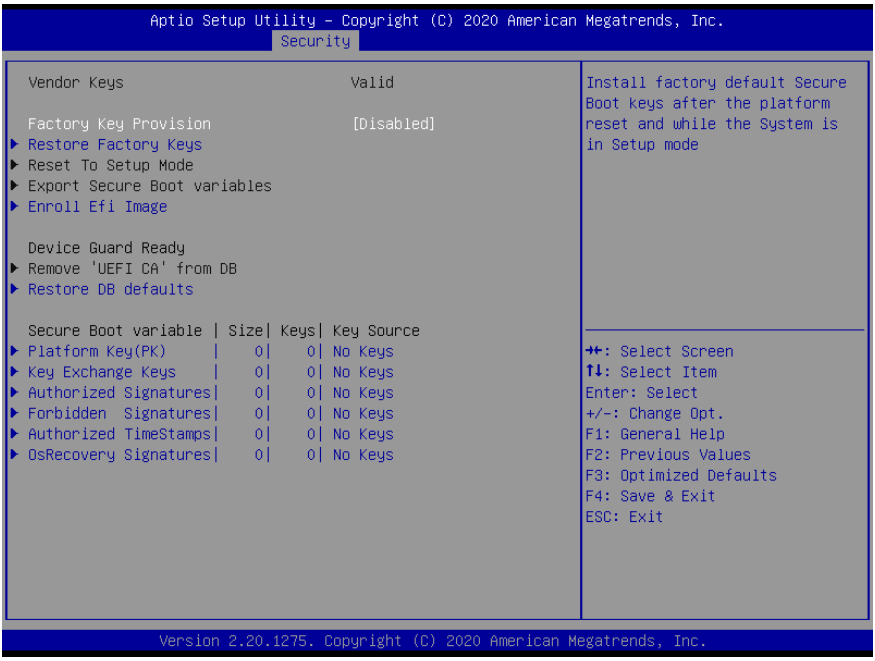
Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot

Options Summary		
Secure Boot	Disable	Optimal Default, Failsafe Default
	Enable	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System mode is in User mode. Changing the mode requires platform reset.		
Secure Boot Mode	Standard	Optimal Default, Failsafe Default
	Custom	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.		
Restore Factory Keys	No	Press 'Yes' to restore factory keys
	Yes	
Force System to User Mode. Install factory default Secure Boot key databases		
Key Management		
Enables expert users to modify Secure Boot Policy variables without full authentication		

3.6.2 Key Management



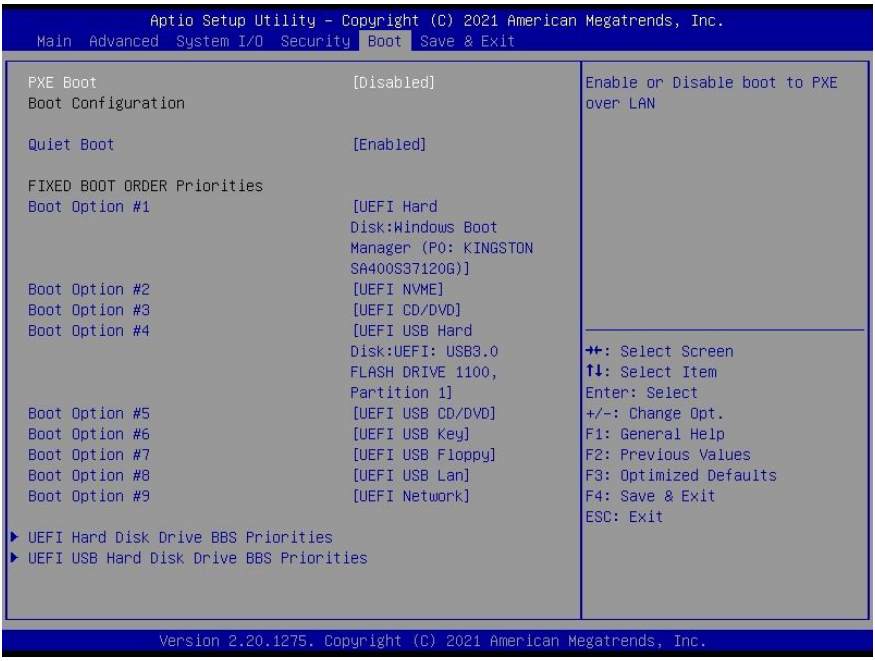
Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.		
Restore Factory Keys	No	Press 'Yes' to install factory default keys
	Yes	
Force System to User Mode. Install Factory default Secure Boot key databases.		
Enroll EFI image	-	-
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database(db).		
Restore DB defaults	No	Press 'Yes' to install factory default keys
	Yes	
Restore DB Variable to factory defaults.		

Secure Boot Variable | Size | Keys# | Key Source		
Platform Key (PK) | 0 | 0 | No Key	Update	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed
Key Exchange keys | 0 | 0 | No Key	Update Append	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed
Authorized Signatures| 0 | 0 | No Key	Update Append	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed

Table Continues on Next Page

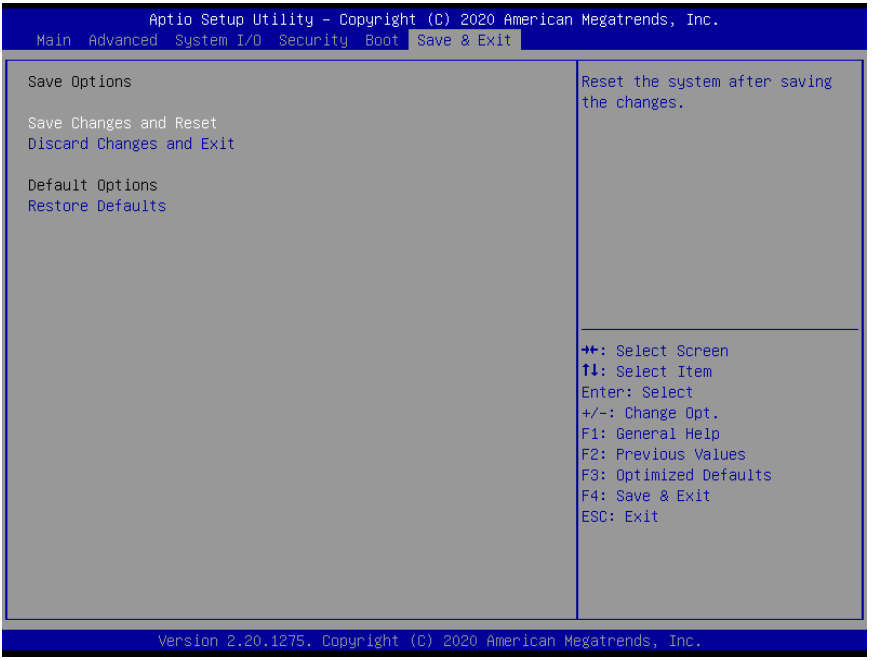
Secure Boot Variable | Size | Keys# | Key Source		
Forbidden Signatures | 0 | 0 | No Key	Update Append	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed
Authorized TimeStamps| 0 | 0 | No Key	Update Append	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed
OsRecovery Signatures| 0 | 0 | No Key	Update Append	Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed

3.7 Setup Submenu: Boot



Options Summary		
PXE Boot	Disabled	Optimal Default, Failsafe Default
	UEFI	
Controls the execution of UEFI and Legacy Network OpROM		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables Quiet Boot option.		

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Driver Download and Installation

Drivers for the NanoCOM-WHU Rev B can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/com-express-modules-nanocom-WHU Rev B

Download the driver(s) you need and extract the zip. Then, follow the steps below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Intel(R) Chipset Device Software 10.1.18019.8144** folder.
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Intel Graphic 27.20.100.7922 x64** folder
2. Run the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. A Read Me file is included in the folder in case you have any questions during installation

Step 3 – Install Network Drivers

1. Open the **Intel(R) Network Connections Software 24.1** folder
2. Run the **PROWinx64.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Audio Driver** folder
2. Run the **0009-64bit_Win7_Win8_Win81_Win10_R282.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Intel Management Engine Firmware

1. Open the **Intel(R) Management Engine Firmware 1910.12.0.1239** folder
2. Run the **MEISetup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install Intel Serial IO Drivers

1. Open the **Intel Serial IO 30.100.1841.2** folder
2. Run the **SetupSerialIO.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. A Read Me file is included in the folder in case you have any questions during installation, as well as instructions to verify installation

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2: Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnDataReg   //This parameter is represented from Note4
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerReg   //This parameter is represented from Note5
#define byte   TimerVal   // This parameter is represented from Note10
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note11
#define byte   RSTReg   //This parameter is represented from Note8
#define byte   RSTBit   //This parameter is represented from Note9
#define byte   RSTVal   //This parameter is represented from Note12
*******************************************************************************
```

```
*******************************************************************************
VOID  Main(){
      // Procedure : AaeonWDTConfig
      // (byte)Timer : Time of WDT timer.(0x00~0xFF)
      // (boolean)Unit : Select time unit(0: second, 1: minute).
      AaeonWDTConfig();

      // Procedure : AaeonWDTEnable
       // This procudure will enable the WDT counting.
      AaeonWDTEnable();
}
*******************************************************************************
```

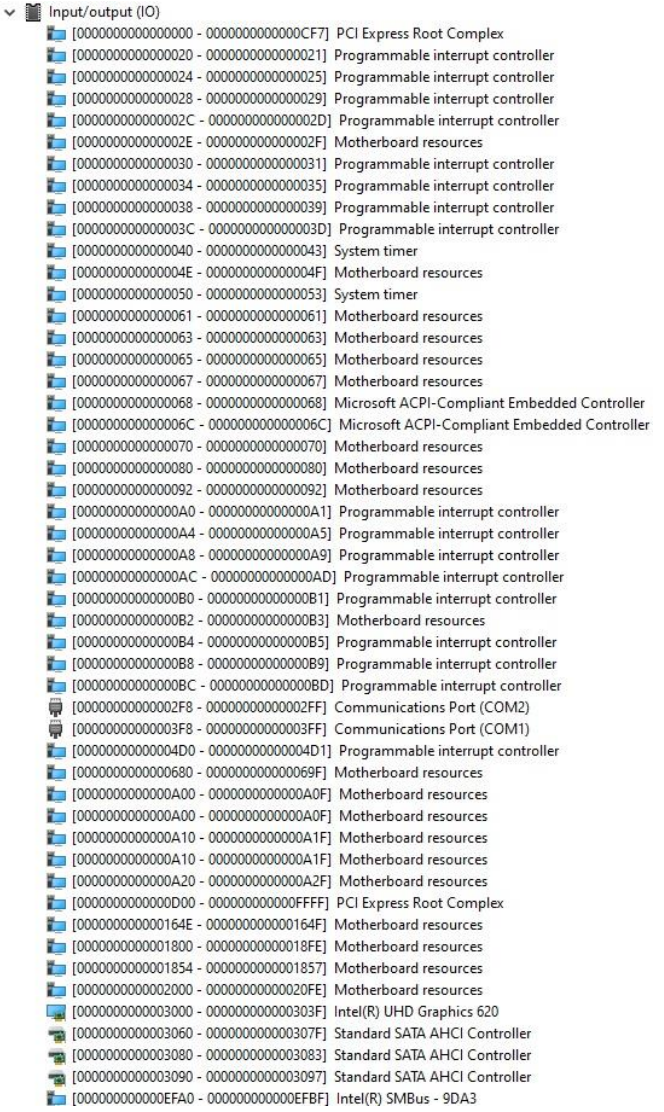
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(0);
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte Value){
       ECBRAMWriteByte(TimerReg , Value);
}

VOID   WDTParameterSetting(){
       Byte TempByte;

        // Watchdog Timer counter setting
        ECBRAMWriteByte(TimerReg , TimerVal);
       // WDT counting unit setting
        TempByte = ECBRAMReadByte(UnitReg);
        TempByte |= (UnitVal << UnitBit);
        ECBRAMWriteByte(UnitReg , TempByte);
        // WDT RST pulse width setting
        TempByte = ECBRAMReadByte(RSTReg);
        TempByte |= (RSTVal << RSTBit);
        ECBRAMWriteByte(RSTReg , TempByte);
}
*******************************************************************************
```

```
*********************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```

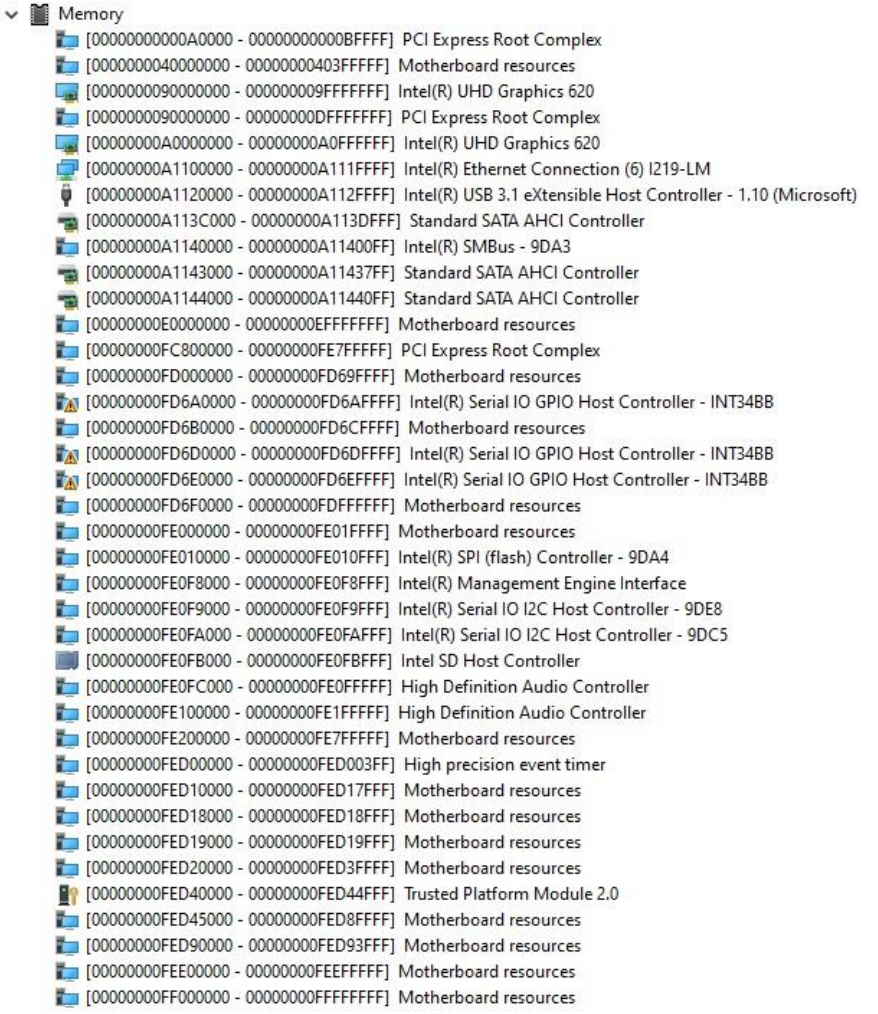
Appendix B

I/O Information

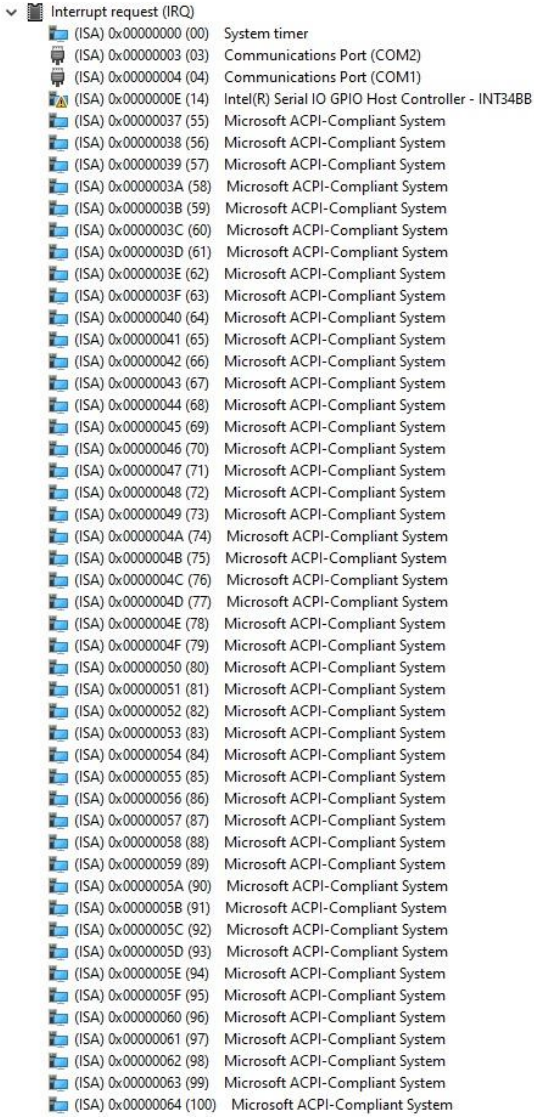
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



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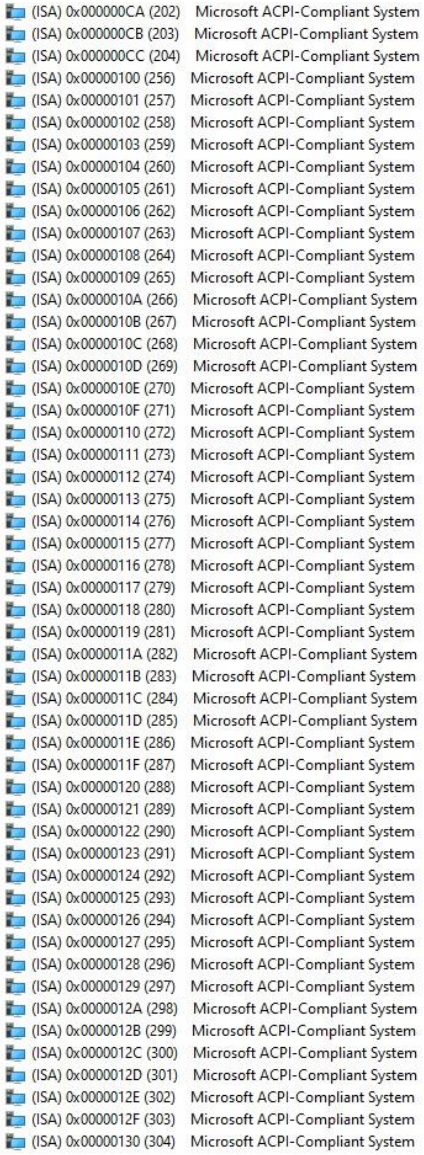
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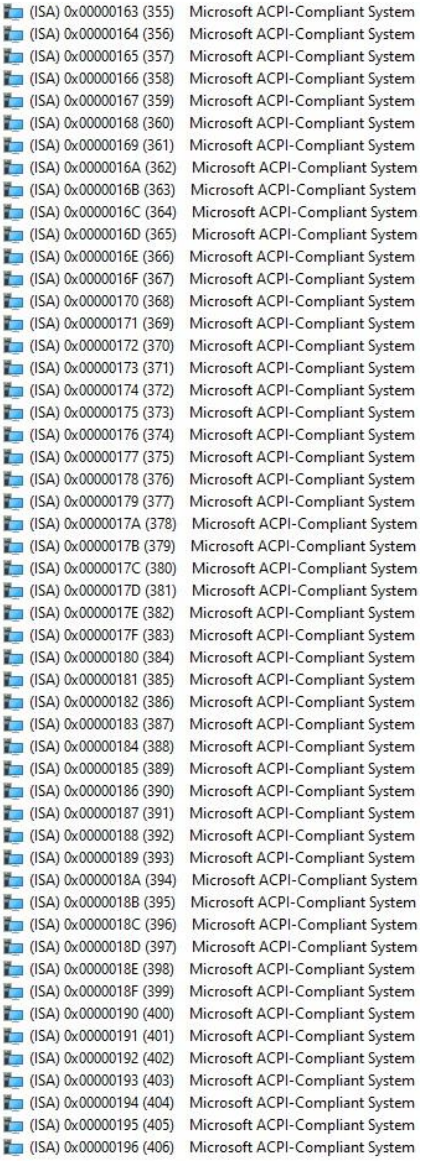
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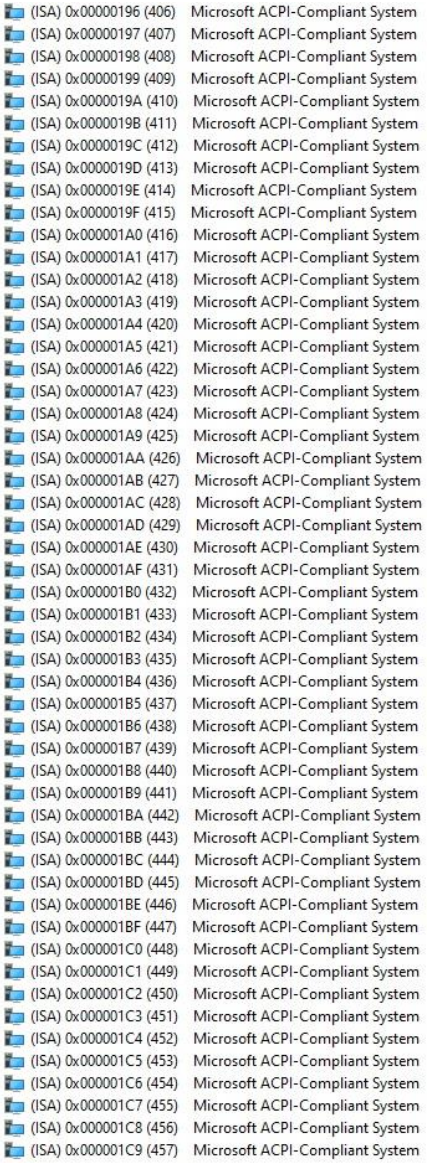
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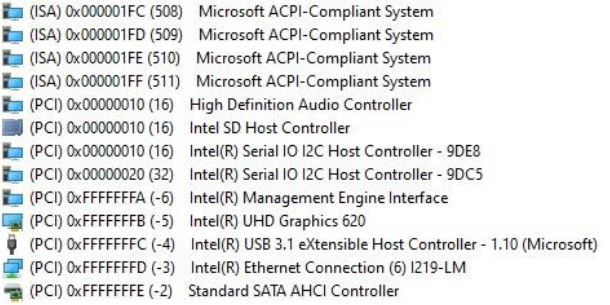
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(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0x00000010 (16) Intel SD Host Controller
(PCI) 0x00000010 (16) Intel(R) Serial IO I2C Host Controller - 9DE8
(PCI) 0x00000020 (32) Intel(R) Serial IO I2C Host Controller - 9DC5
(PCI) 0xFFFFFFFA (-6) Intel(R) Management Engine Interface
(PCI) 0xFFFFFFFB (-5) Intel(R) UHD Graphics 620
(PCI) 0xFFFFFFFC (-4) Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
(PCI) 0xFFFFFFFD (-3) Intel(R) Ethernet Connection (6) I219-LM
(PCI) 0xFFFFFFFE (-2) Standard SATA AHCI Controller

Appendix C

Programming Digital I/O

C.1 DIO Programming

NanoCOM-WHU Rev B utilizes an AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can use to develop a customized program to fit your application.

C.2 Digital I/O Register

Table 1: Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
IO Direction Function and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
IO Value/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2: Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

C.3 Digital I/O Sample Program

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnData0Reg   //This parameter is represented from Note4
#define byte   BRAMFnData1Reg   //This parameter is represented from Note5
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DIO0ToDIO7Reg   // This parameter is represented from Note6
#define byte   DIO0Bit   // This parameter is represented from Note7
#define byte   DIO1Bit   // This parameter is represented from Note8
#define byte   DIO2Bit   // This parameter is represented from Note9
#define byte   DIO3Bit   // This parameter is represented from Note10
#define byte   DIO4Bit   // This parameter is represented from Note11
#define byte   DIO5Bit   // This parameter is represented from Note12
#define byte   DIO6Bit   // This parameter is represented from Note13
#define byte   DIO7Bit   // This parameter is represented from Note14
#define byte   DIO0Val   // This parameter is represented from Note15
#define byte   DIO1Val   // This parameter is represented from Note16
#define byte   DIO2Val   // This parameter is represented from Note17
#define byte   DIO3Val   // This parameter is represented from Note18
#define byte   DIO4Val   // This parameter is represented from Note19
#define byte   DIO5Val   // This parameter is represented from Note20
#define byte   DIO6Val   // This parameter is represented from Note21
#define byte   DIO7Val   // This parameter is represented from Note22
*******************************************************************************
```

```
*********************************************************************************
VOID  Main(){
      Boolean PinStatus ;

      // Procedure : AaeonReadPinStatus
      // Input :
      //       Example, Read Digital I/O Pin 3 status
       // Output :
       //       InputStatus :
       //                0: Digital I/O Pin level is low
       //                1: Digital I/O Pin level is High
      PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

      // Procedure : AaeonSetOutputLevel
      // Input :
      //       Example, Set Digital I/O Pin 6 level
      AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*********************************************************************************
```

```
*****************************************************************************
Boolean   AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID   AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
         ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*****************************************************************************
```

```
*****************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, FnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*****************************************************************************
```