NanoCOM-KBU-A20

COM Express Module

User's Manual 2nd Ed

Last Updated: August 8, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● NanoCOM-KBU-A20	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	X	O	O	O	O	O
Wires & Connectors for External Connections	X	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	COM Express Mini Size, Type 10
CPU	Onboard 7th Generation Intel® Core™ U-series SoC Processor
CPU Frequency	Up to i7-7600U 2C / 2.8 GHz
Chipset	Onboard 7th Generation Intel® Core™ U-series SoC
Memory Type	Onboard Non-ECC DDR4-2133
Max. Memory Capacity	Onboard 8GB DDR4
BIOS	AMI BIOS, Legacy Free
Wake on LAN	YES
Watchdog Timer	255 Levels
Power Requirement	Nominal : +12V
Power Supply Type	AT/ATX
Power Consuption (Typical)	i7-7600U, Onboard 8GB DDR4, full loading 1.83A@12V during 100% loading burn in test
Dimension (L x W)	3.31" x 2.17" (84mm x 55mm)
Operating Temperature	32 °F ~ 140 °F (0 °C ~ 60 °C) -40 °F ~ 185 °F (-40 °C ~ 80 °C), Optional for NANOCOM-SKU series
Storage Temperature	-40°F ~ 185°F (-40°C ~ 85°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	80,000
Certification	CE / FCC Class A

Display

VCD/LCD Controller	Onboard 7th Gen Intel® Core U-Series Processor, GT2-620/610
Video Output	LVDS/eDP, DDI x 1
LVDS Interface	—

I/O

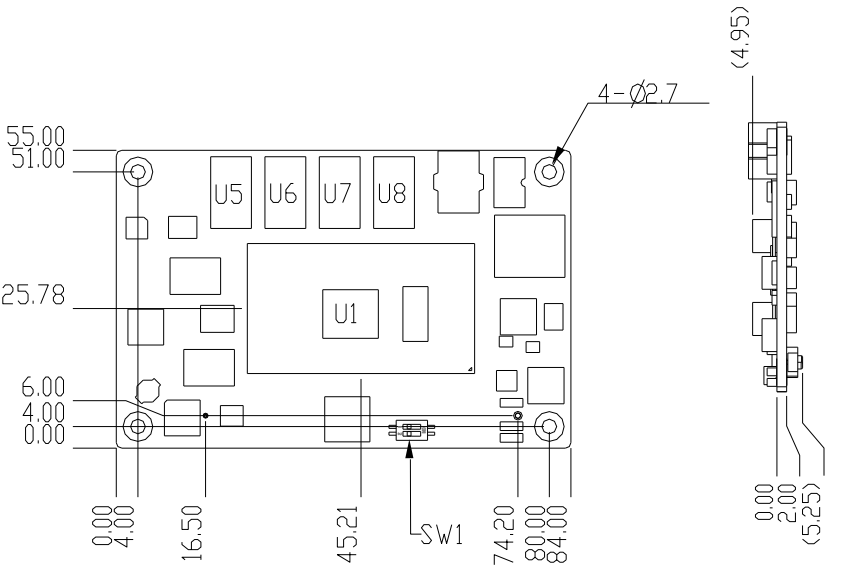
Ethernet	Intel® I219-LM Gigabit Ethernet
Audio	HD Audio
USB Port	USB 2.0 x 8
	USB 3.0 x 2
Serial Port	2-Wire UART (Tx/Rx) x 2
HDD Interface	SATAIII x 2
Onboard Storage	eMMC Optional
Expansion Slot	PCIe [x1] x 4 (up to 4 devices)
	LPC
	SMBus
	I2C
GPIO	GPIO 8-bit
TPM	fTPM Support
Note	—

Chapter 2

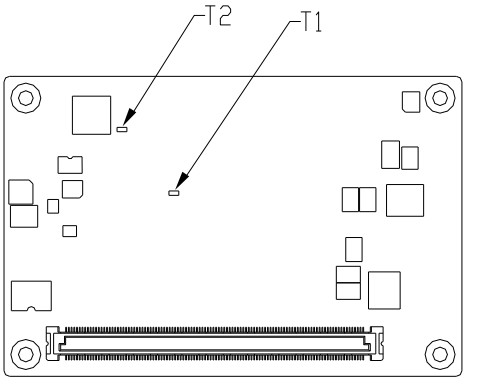
Hardware Information

2.1 Dimensions, Jumpers and Connectors

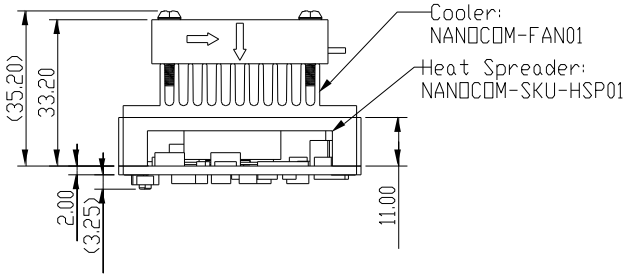
Component Side



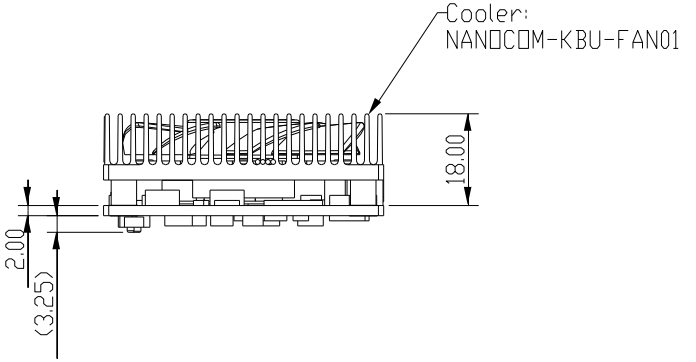
Solder Side



With Fan and Heat Spreader



With Fan Only (no Heat Spreader)



2.2 List of Switches and Connectors

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
SW1	AT/ ATX switch
CN1	ROW A/B connector

2.2.1 AT/ATX Switch (SW1)

Pin	Function
1 (On)	AT Mode
1 (Off)	ATX Mode (Default)
2 (On)	RTC reset
2 (Off)	RTC Normal (Default)

2.2.2 ROW A/B Connector (CN1)

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	N.C	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-

Row A		Row B	
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB3_RXN0	B22	USB3_TXN0
A23	USB3_RXP0	B23	USB3_TXP0
A24	SUS_S5#	B24	PWR_OK
A25	USB3_RXN1	B25	USB3_TXN1
A26	USB3_RXP1	B26	USB3_TXP1
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	N.C
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	N.C
A37	USB6+	B37	N.C
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#

Row A		Row B	
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C	B52	N.C
A53	N.C	B53	N.C
A54	GPI0	B54	GPO1
A55	N.C	B55	N.C
A56	N.C	B56	N.C
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	DDI0_PAIR0+

Row A		Row B	
A72	LVDS_A0-	B72	DDI0_PAIR0-
A73	LVDS_A1+	B73	DDI0_PAIR1+
A74	LVDS_A1-	B74	DDI0_PAIR1-
A75	LVDS_A2+	B75	DDI0_PAIR2+
A76	LVDS_A2-	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN	B77	N.C
A78	LVDS_A3+	B78	N.C
A79	LVDS_A3-	B79	LVDS_BKLD_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	DDI0_PAIR3+
A82	LVDS_A_CK-	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	N.C	B86	VCC_5V_SBY
A87	N.C	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	N.C
A92	SPI_MISO	B92	N.C
A93	GPO0	B93	N.C
A94	SPI_CLK	B94	N.C
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	GND	B96	N.C
A97	TYPE10#	B97	SPI_CS#
A98	RS1_TX	B98	DDI0_CTRL_CLK

Row A		Row B	
A99	RS1_RX	B99	DDI0_CTRL_DATA
A100	GND (FIXED)	B100	GND (FIXED)
A101	RS2_TX	B101	FAN_PWMOUT
A102	RS2_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The NanoCOM-KBU-A20 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

3.2.1 Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Security

Set setup administrator password.

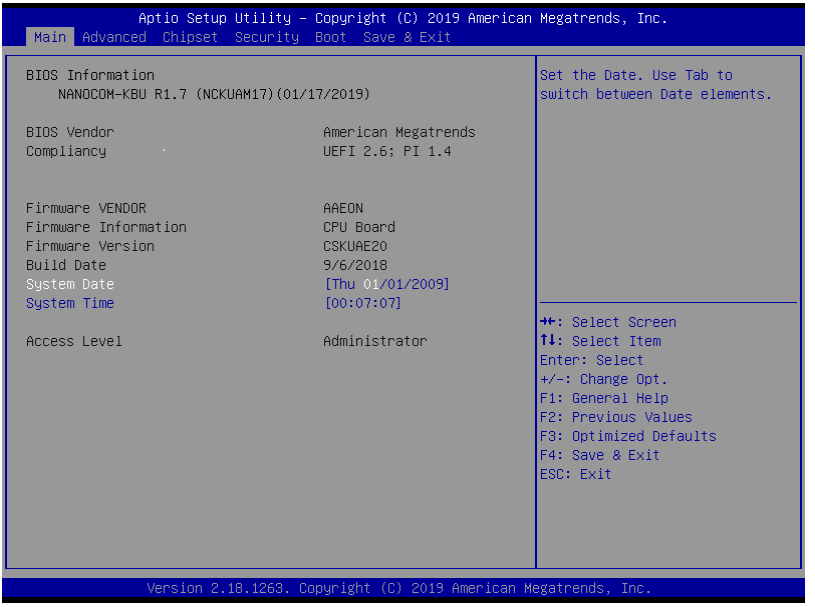
Boot

Enables/disable quiet boot option.

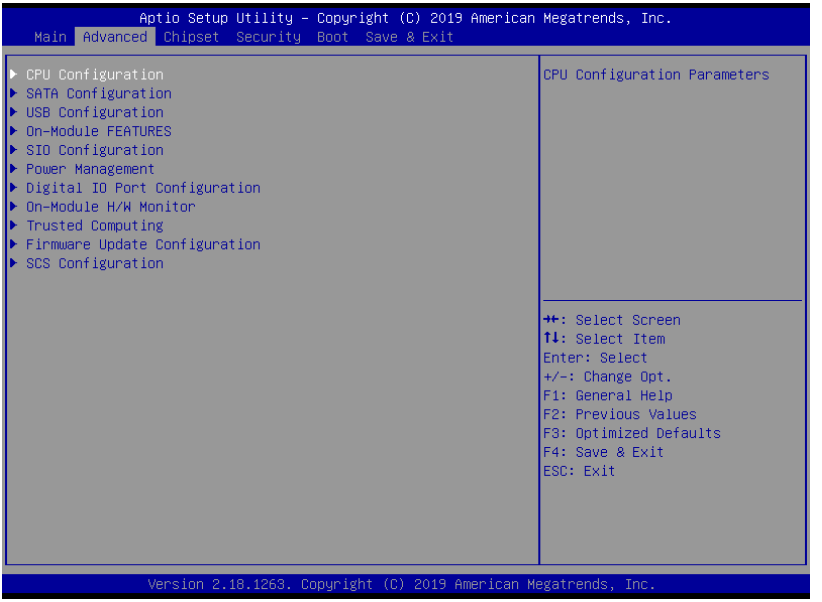
Save & Exit

Exit system setup after saving the changes.

3.3 Main


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
BIOS Information
NANOCOM-KBU R1.7 (NCKUAM17)(01/17/2019)
BIOS Vendor
American Megatrends
Compliancy
UEFI 2.6; PI 1.4
Firmware VENDOR
AAEON
Firmware Information
CPU Board
Firmware Version
CSKUAE20
Build Date
9/6/2018
System Date
[Thu 01/01/2009]
System Time
[00:07:07]
Access Level
Administrator
Set the Date. Use Tab to switch between Date elements.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.

3.4 Advanced


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
CPU Configuration
SATA Configuration
USB Configuration
On-Module FEATURES
SIO Configuration
Power Management
Digital IO Port Configuration
On-Module H/W Monitor
Trusted Computing
Firmware Update Configuration
SCS Configuration
CPU Configuration Parameters
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
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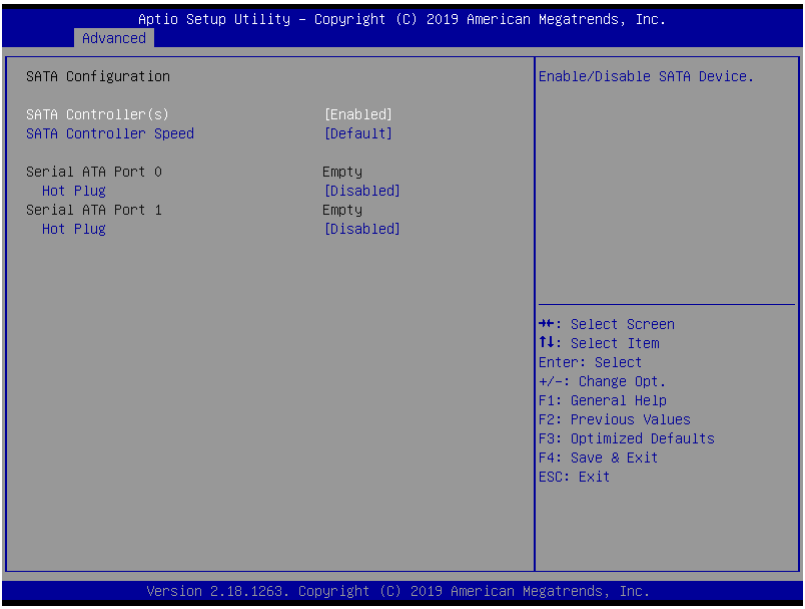
3.4.1 CPU Configuration

Options Summary		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel® SpeedStep™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		

3.4.2 SATA Configuration



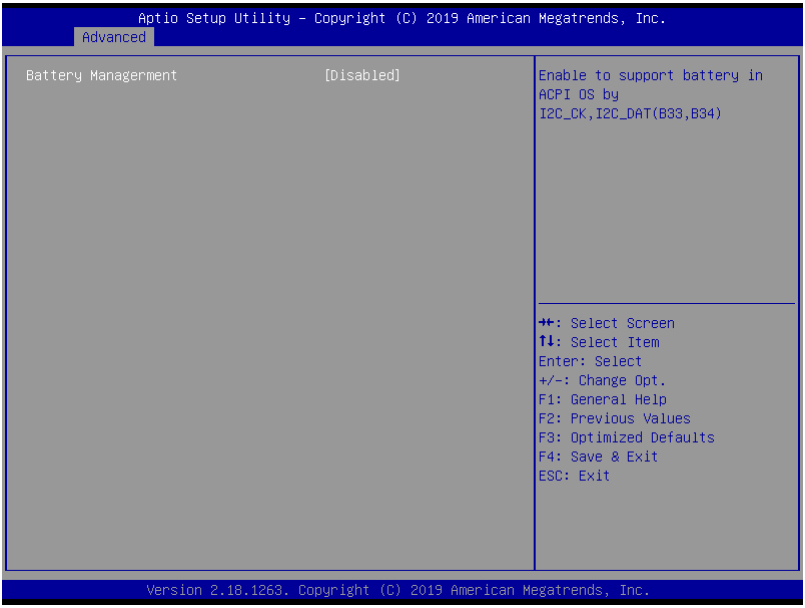
Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable SATA Device.		
SATA Controller Speed	Disabled	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Indicates the maximum speed the SATA controller can support.		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		

Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		
Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.3 USB Configuration

Options Summary		
Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables Legacy USB Support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB device available only for EFI applications.		

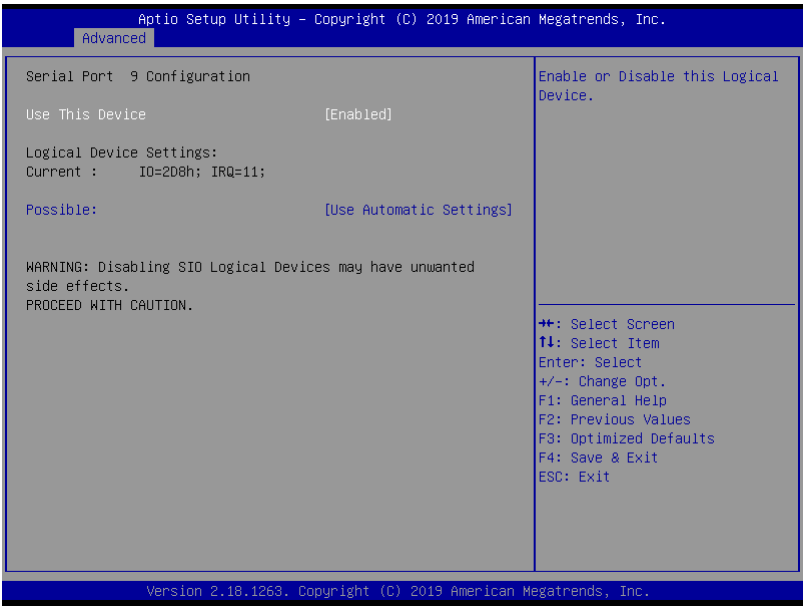
3.4.4 On-Module FEATURES



Options Summary		
Battery Managerment	Disabled	Optimal Default, Failsafe Default
	One Battery	
Enable to support battery in ACPI OS by I2C_CK,I2C_DAT(B33,B34)		

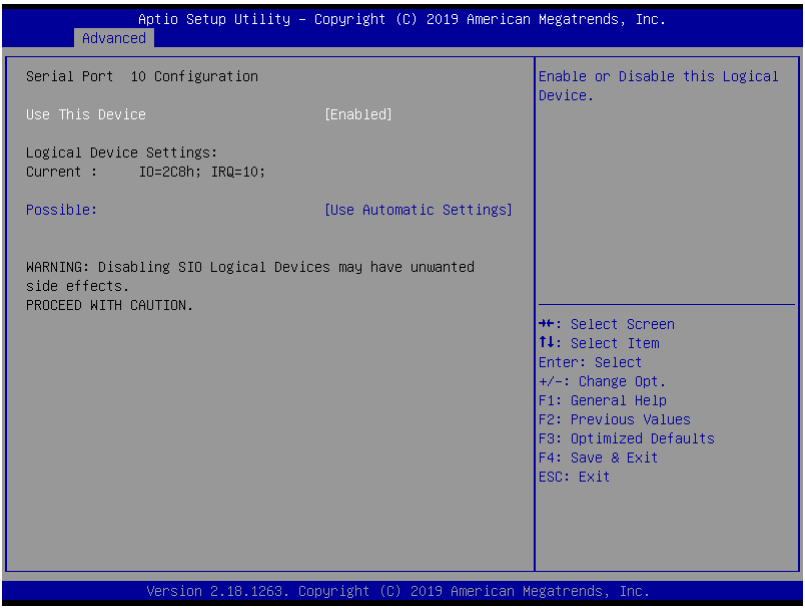
3.4.5 SIO Configuration

3.4.5.1 SIO Configuration: Serial Port 9 Configuration



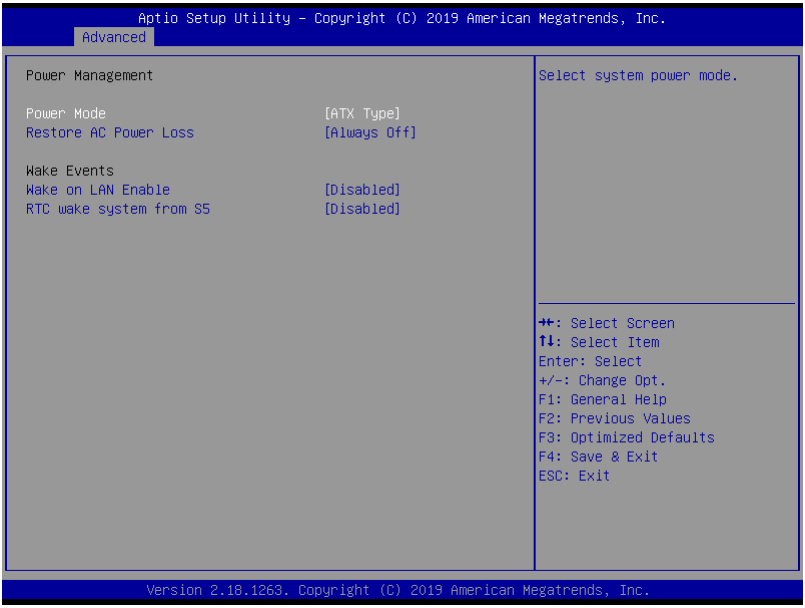
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2D8; IRQ=11; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.5.2 SIO Configuration: Serial Port 10 Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2C8; IRQ=10; DMA;	
	IO=2D8; IRQ=10; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.6 Power Management

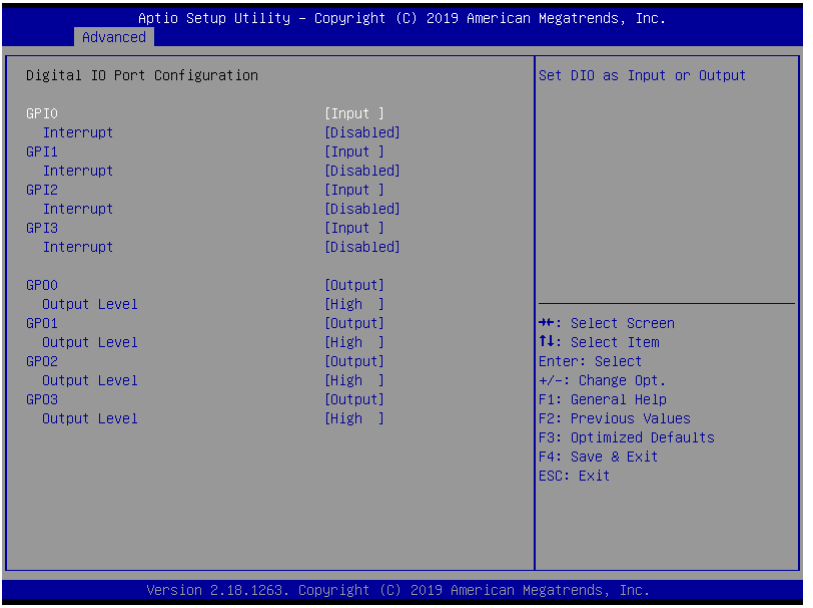


Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
Wake on LAN Enable	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enabled/ Disabled integrated LAN to wake the system.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	

Fixed Time: System will wake on the hr::min::sec specified.

Dynameic time: System will wake on the current time + Increase minute(s)

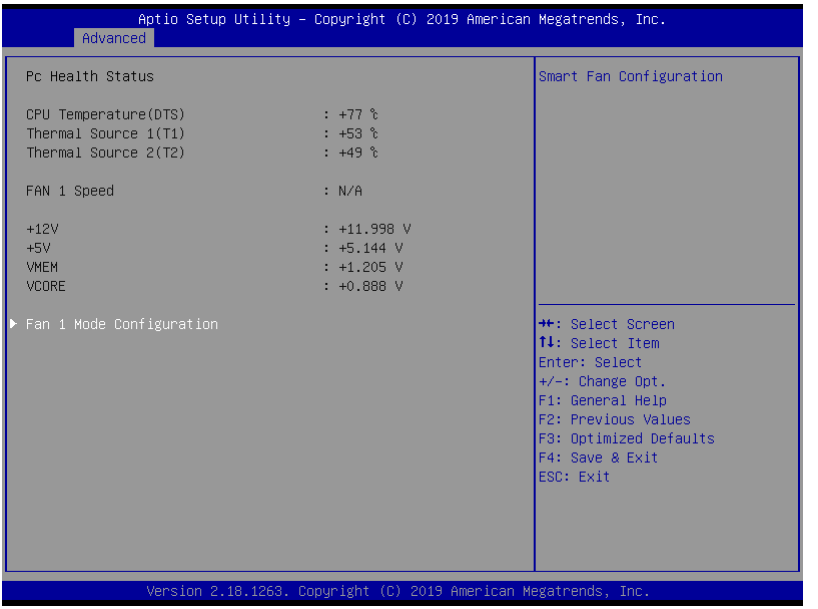
3.4.7 Digital IO Port Configuration



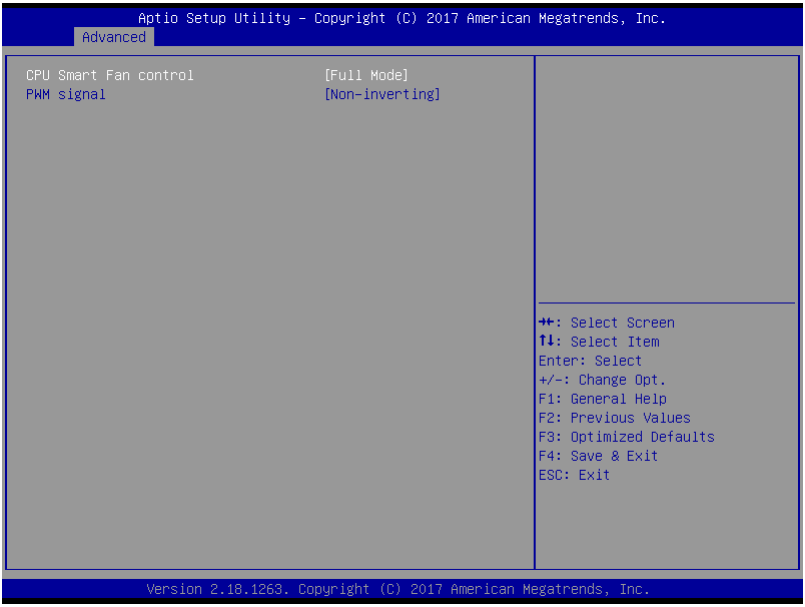
Options Summary		
GPI *	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
Interrupt	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled interrupt function with low pulse mode. This triggered pulse needs more then the 10ms.		
GPO *	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default

	Low	
Set output level when DIO pin is output		

3.4.8 On Module Hardware Monitor

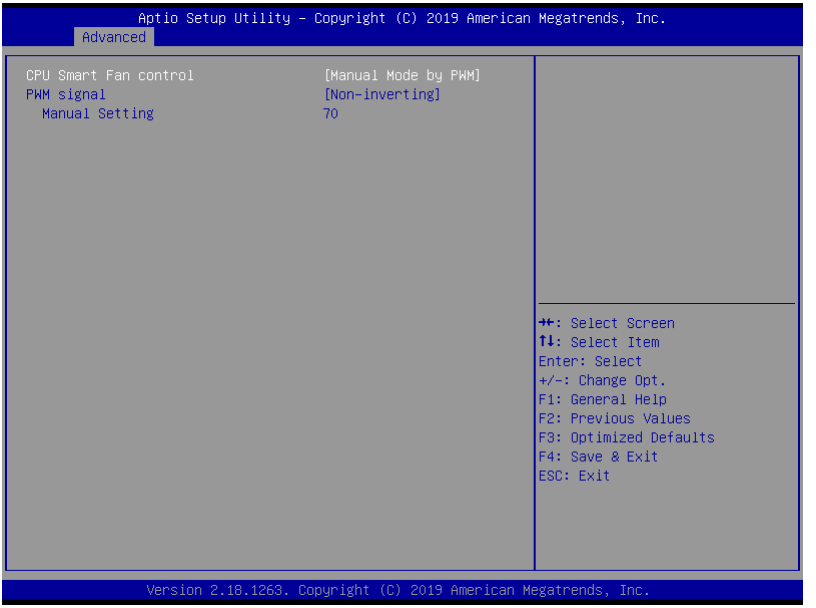


3.4.8.1 Fan 1 Mode Configuration



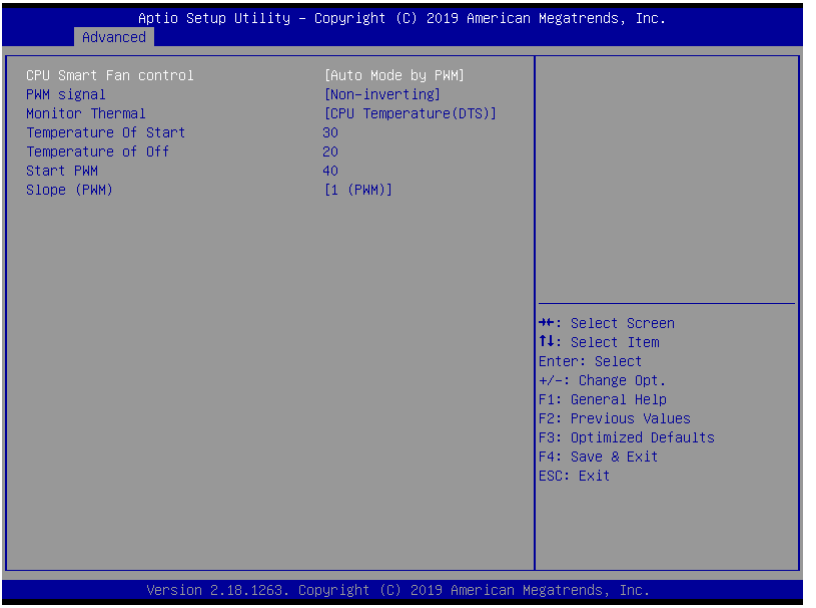
Options Summary		
CPU Smart Fan Mode	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
Smart Fan Mode Select		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-uninverting signal		

3.4.8.2 CPU Smart Fan Mode: Manual Mode by PWM



Options Summary		
Manual Setting	70	Optimal Default, Failsafe Default
Set Fan at fixed Duty-Cycle Min=. Max=100 Please input Dec number:		

3.4.8.3 CPU Smart Fan Mode : Auto Mode by PWM

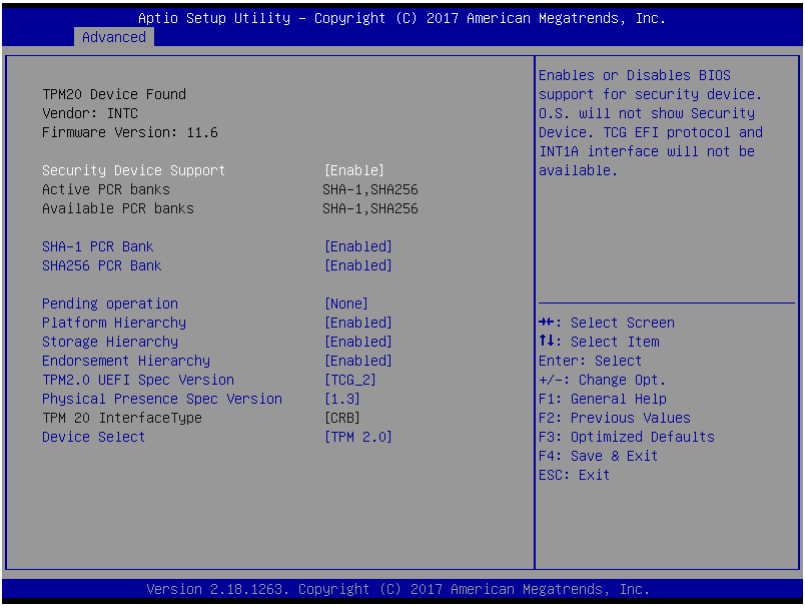


Options summary:

Options Summary		
Monitor Thermal	CPU Temperature(DTS)	Optimal Default, Failsafe Default
	Thermal Source 1(T1)	
	Thermal Source 2(T2)	
Select monitor thermal source		
Temperature of Start	30	Optimal Default, Failsafe Default
Temperature Of Start		
Temperature Of Off	20	Optimal Default, Failsafe Default
Temperature Of Off		
Start PWM	40	Optimal Default, Failsafe Default
Start PWM		

Slope (PWM)	0 (PWM)	
	1 (PWM)	Optimal Default, Failsafe Default
	2 (PWM)	
	4 (PWM)	
	8 (PWM)	
	16 (PWM)	
	32 (PWM)	
	64 (PWM)	
Slope (PWM)		

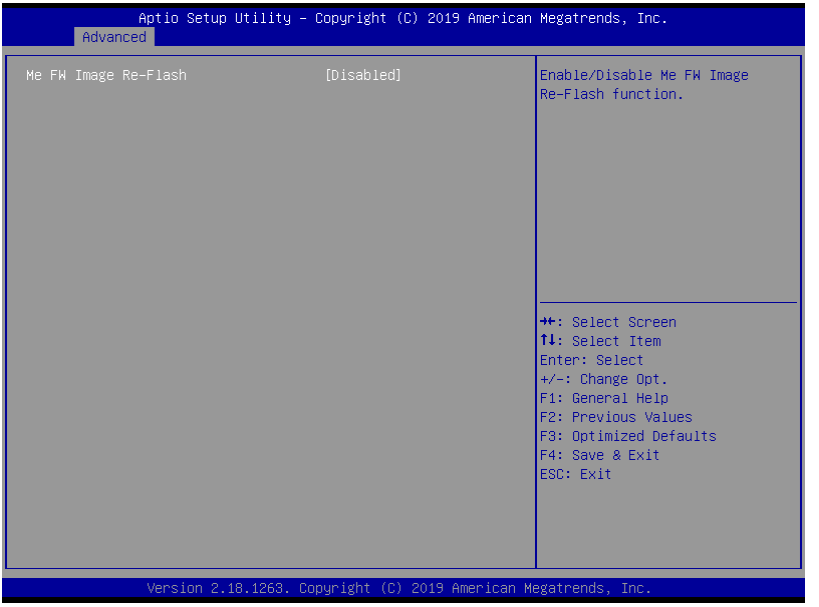
3.4.9 Trusted Computing



Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default

Enable or Disable SHA256 PCR Bank		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
	TPM 2.0	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

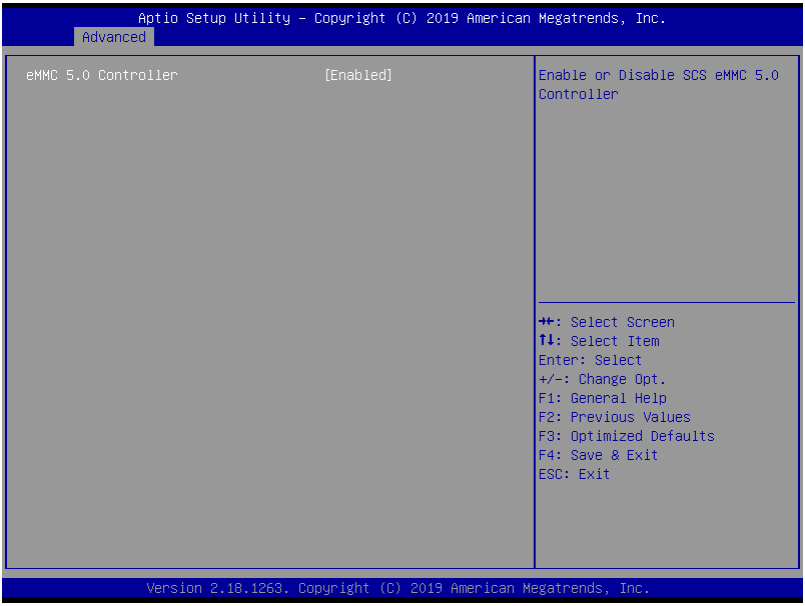
3.4.10 Firmware Update Configuration



Options summary:

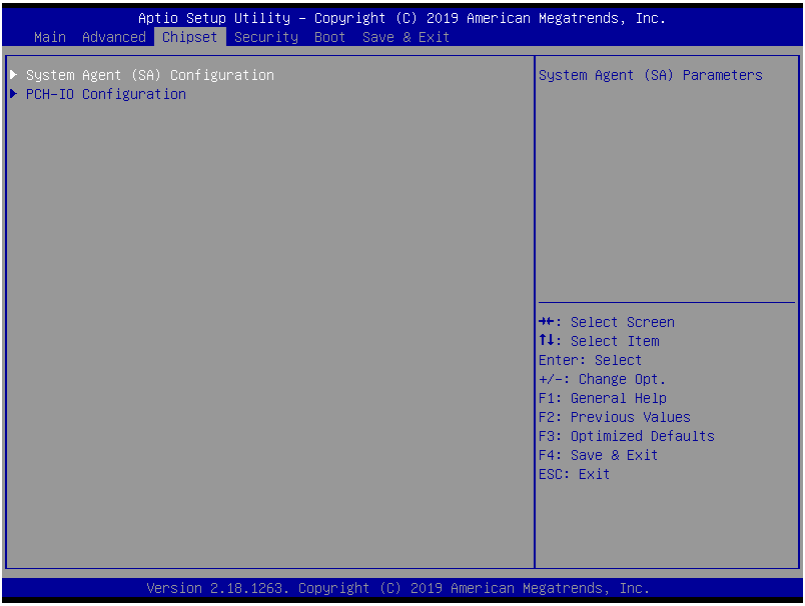
Options Summary		
Me FW Image Re-Flash	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/ Disable Me FW Image Re-Flash functinn.		

3.4.11 SCS Configuration

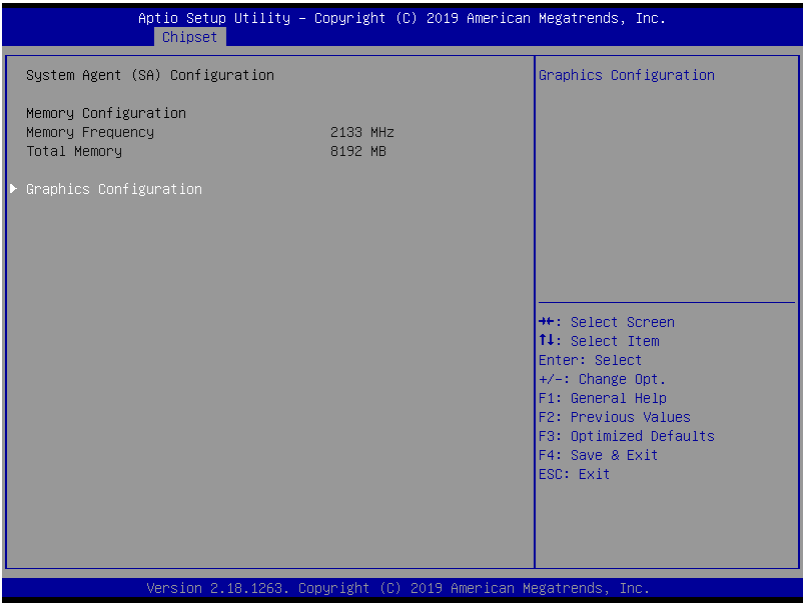


Options Summary		
Emmc 5.0 Controller	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Emmc 5.0 Controller		

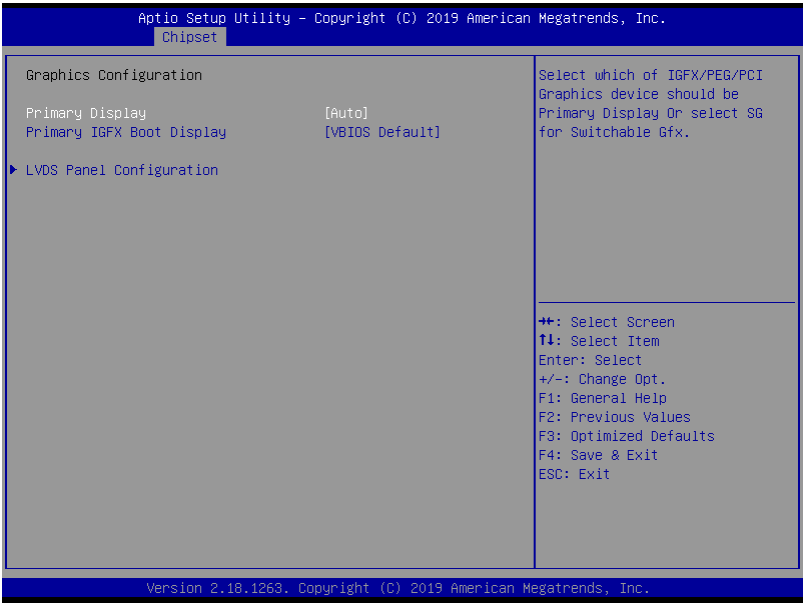
3.5 Chipset


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
System Agent (SA) Configuration
PCH-IO Configuration
System Agent (SA) Parameters
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.

3.5.1 System Agent (SA) Configuration



3.5.1.1 Graphics Configuration



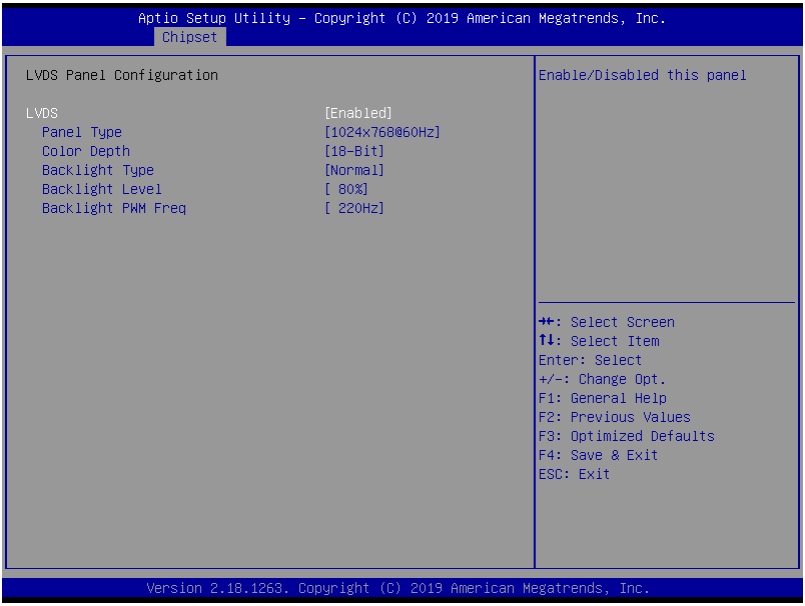
Options Summary		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	Display Port	
	LVDS	

Select the Video Device which will be activated during POST. This has no effect if external graphic present.

Secondary boot display selection will appear based on your selection.

VGA modes will be supported only on primary display

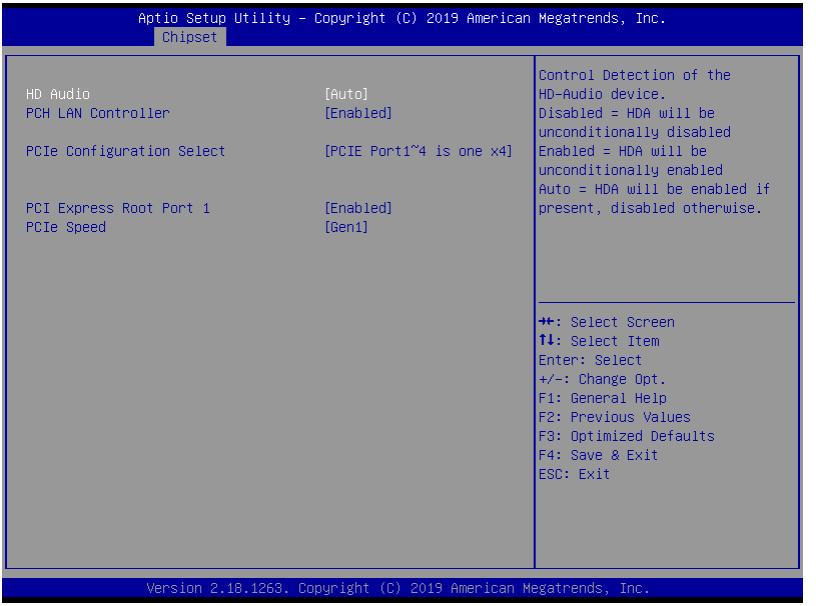
3.5.1.2 LVDS Panel Configuration



Options Summary		
LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled/ Disabled this panel		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x800@60Hz	
	1366x768@60Hz	

Select panel type		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

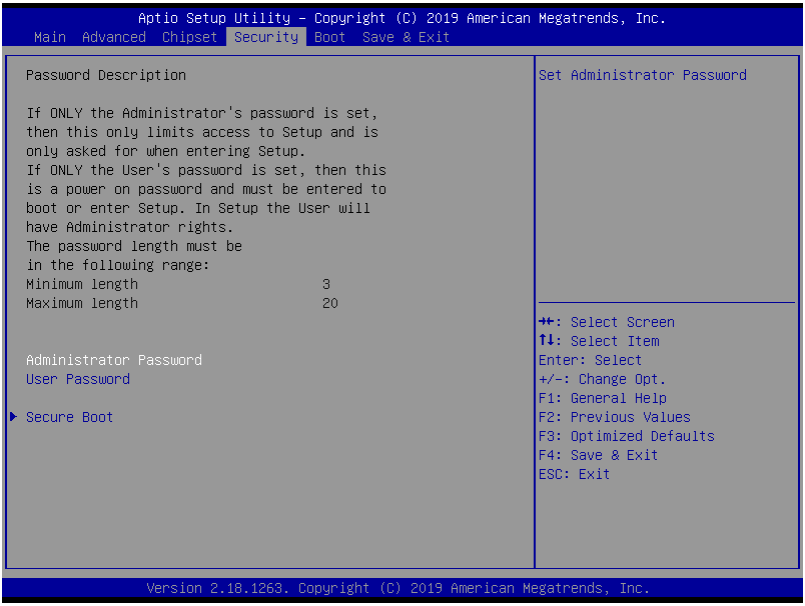
3.5.2 PCH-IO Configuration



Options Summary		
HD Audio	Disabled	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise.		
PCH LAN Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable onboard NIC.		

PCIe Configuration Select	PCIE Port1~4 are four x1	
	PCIE Port1~4 is one x4	Optimal Default, Failsafe Default
PCIE Port1~4 Selection		
PCI Express Root Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	
	Gen1	Optimal Default, Failsafe Default
	Gen2	
	Gen3	
Comfigure PCIe Speed		

3.6 Security



Change User/Supervisor Password

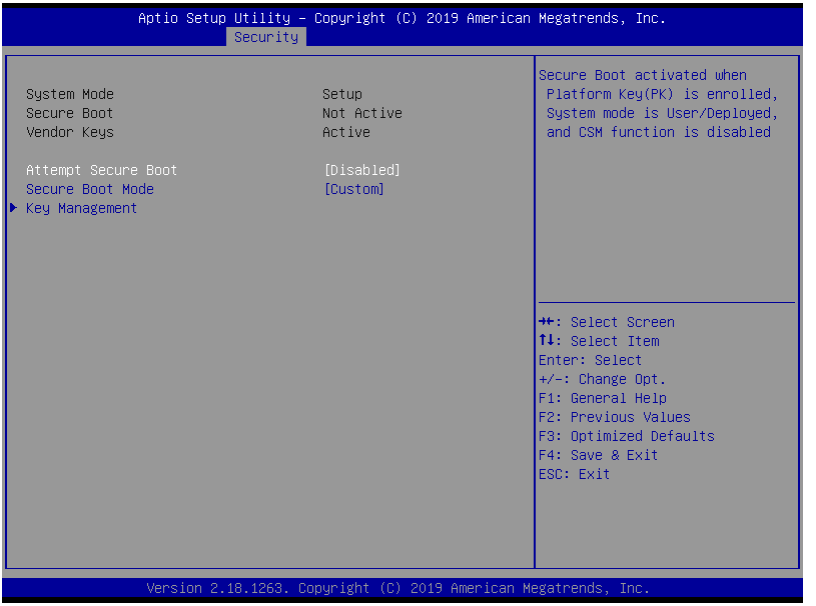
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

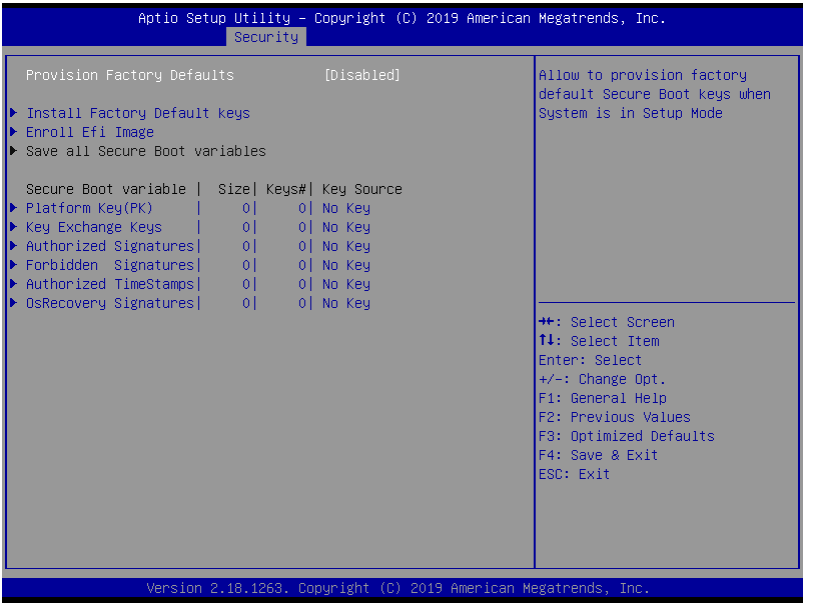
Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot



Options Summary		
Attempt Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot activated when Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM function is disable		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot Mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication		

3.6.1.1 Key Management



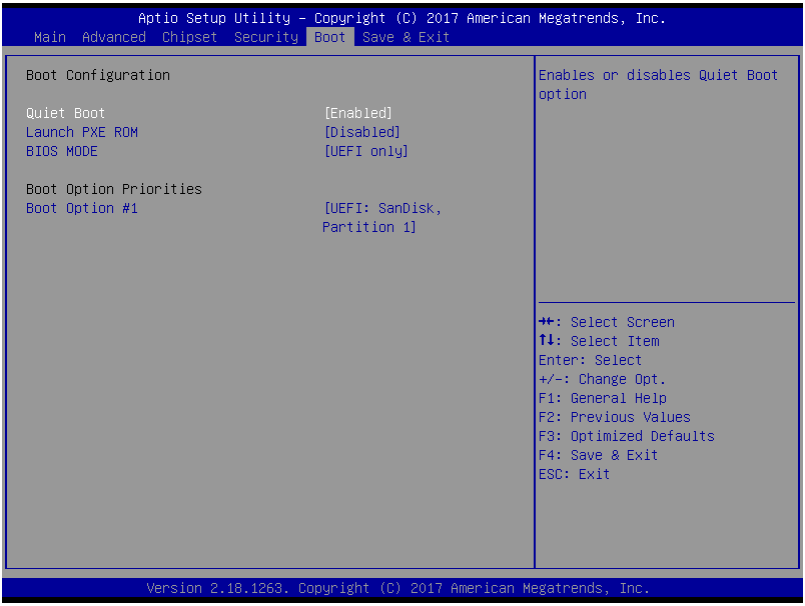
Options Summary		
Provision Factory Defaults	Disabled	Optimal Default, Failsafe Default
	Enabled	
Allow to provision factory default Secure Boot keys when System is in setup Mode		
Install Factory Default keys		
Force System to User Mode - install all Factory Default keys		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Authorized Signature Database (db)		

Platform Key(PK)	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	
Key Exchange Keys	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	

Authorized Signatures	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	
Forbidden Signatures	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	

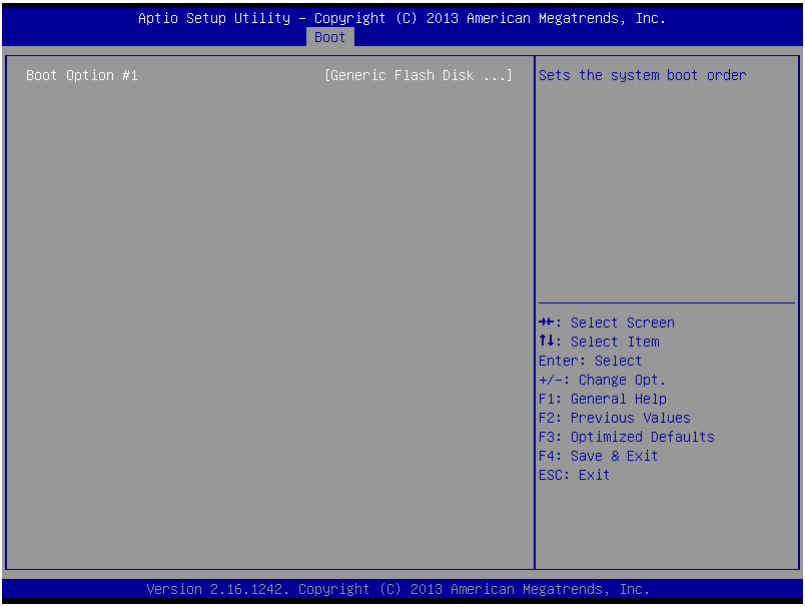
Authorized TimeStamps	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	
OsRecovery Signatures	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Default,External,Mixed,Test	

3.7 Boot

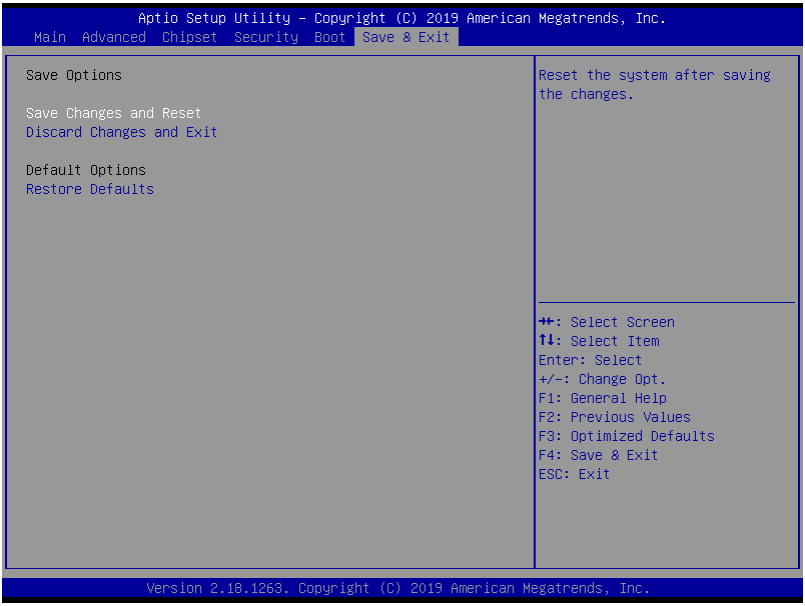


Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disable showing boot logo.		
Launch PXE OpROM	Do not launch	Optimal Default, Failsafe Default
	UEFI	
	UEGI and Legacy	
Controls the execution of UEFI and Legacy PXE OpROm		
BIOS MODE	UEFI only	Optimal Default, Failsafe Default
	UEFI and Legacy	
Select using BIOS mode		

3.7.1 Boot: BBS Priorities



3.8 Save & Exit


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced Chipset Security Boot Save & Exit
Save Options
Save Changes and Reset
Discard Changes and Exit
Default Options
Restore Defaults
Reset the system after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.

Chapter 4

Drivers Installation

4.1 Driver Download and Installation

Drivers for the NanoCOM-KBU-A20 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/com-express-modules-nanocom-kbu-a20

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step1 – Chipset** followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step2 - Graphic** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Open the **Step3 - LAN** folder followed by **Autorun.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Step4 - Audio** folder followed by **0002-R276.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install ME Drivers

1. Open the **Step5 - ME** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Serial IO Drivers (Windows 10)

1. Open the **Step6 – Serial IO** folder followed by the **Win10_x64** folder
2. Run **Setup.exe**
3. Follow the instructions
4. Drivers will be installed automatically

Step 7 – Install Interrupt DIO Drivers (Windows 10)

1. Open the **Step7 – InteruptDIO** folder followed by the **Win10_x64** folder
2. Follow instructions in **ACPI Driver Test SOP.docx** to install and test drivers.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte    EcBRAMIndex    //This parameter is represented from Note1
#define byte    EcBRAMData     //This parameter is represented from Note2
#define byte    BRAMLDNReg     //This parameter is represented from Note3
#define byte    BRAMFnDataReg    //This parameter is represented from Note4
#define   void    EcBRAMWriteByte(byte Offset, byte Value);
#define   byte    EcBRAMReadByte(byte Offset);
#define   void    IOWriteByte(byte Offset, byte Value);
#define   byte    IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte    TimerReg    //This parameter is represented from Note5
#define byte    TimerVal    // This parameter is represented from Note10
#define byte    UnitReg    //This parameter is represented from Note6
#define byte    UnitBit    //This parameter is represented from Note7
#define byte    UnitVal    //This parameter is represented from Note11
#define byte    RSTReg    //This parameter is represented from Note8
#define byte    RSTBit    //This parameter is represented from Note9
#define byte    RSTVal    //This parameter is represented from Note12
*******************************************************************************
```

```
*******************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*******************************************************************************
```

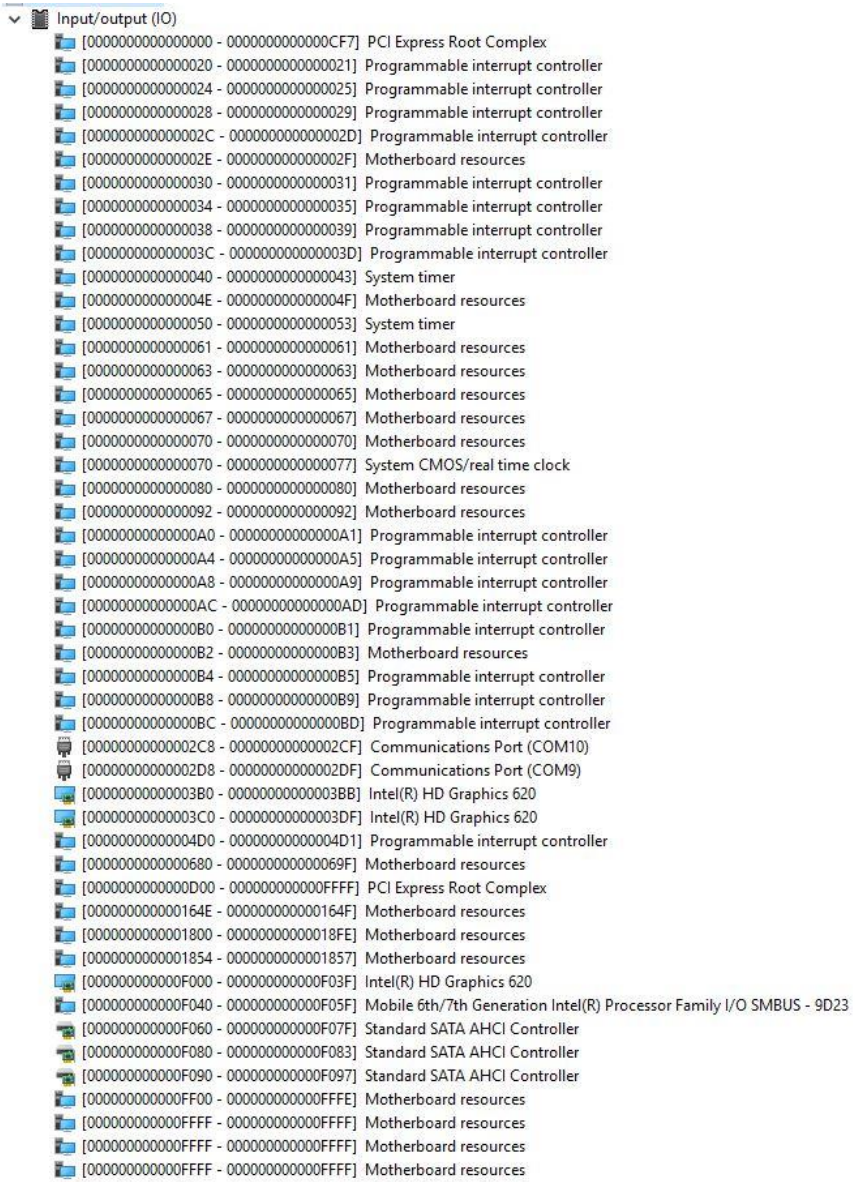
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
         WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(0);
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte Value){
        ECBRAMWriteByte(TimerReg , Value);
}

VOID    WDTParameterSetting(){
        Byte TempByte;

         // Watchdog Timer counter setting
         ECBRAMWriteByte(TimerReg , TimerVal);
        // WDT counting unit setting
         TempByte = ECBRAMReadByte(UnitReg);
         TempByte |= (UnitVal << UnitBit);
         ECBRAMWriteByte(UnitReg , TempByte);
         // WDT RST pulse width setting
         TempByte = ECBRAMReadByte(RSTReg);
         TempByte |= (RSTVal << RSTBit);
         ECBRAMWriteByte(RSTReg , TempByte);
}
*******************************************************************************
```

```
*****************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*****************************************************************************
```

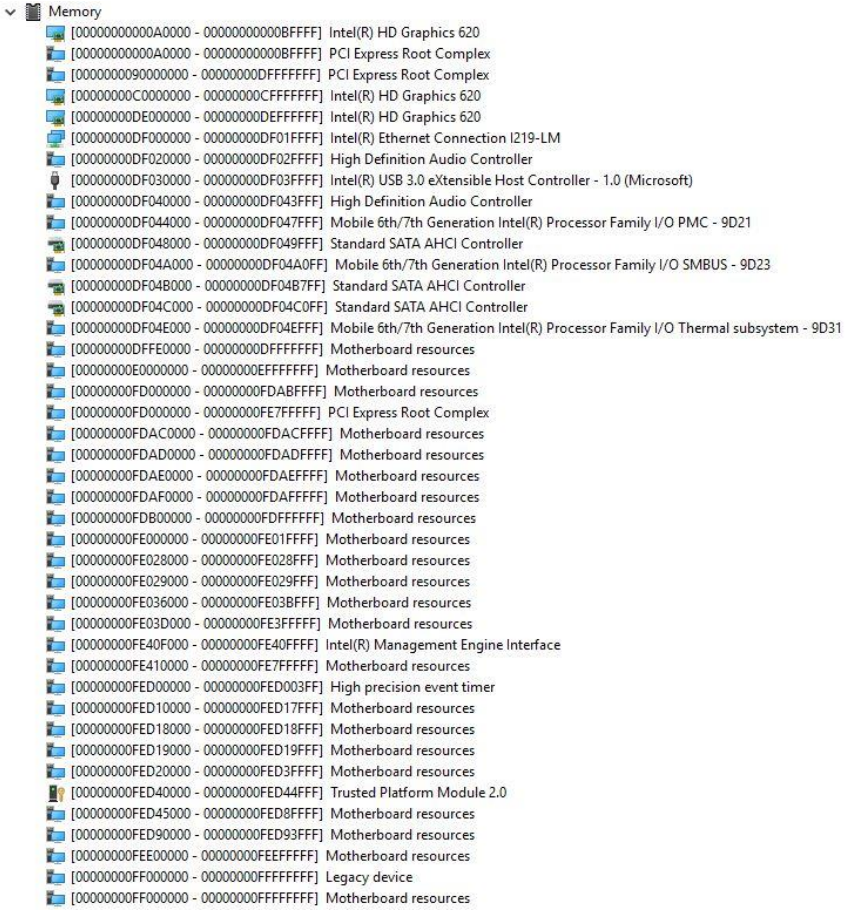
Appendix B

I/O Information

B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart

Appendix C

Programming Digital I/O

C.1 Digital I/O Programming

NanoCOM-KBU-A20 utilizes AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can develop customized program to fit your application.

C.2 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
IO Direction Function and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
IO Vaule/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

C.3 Digital I/O Sample Program

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte    EcBRAMIndex    //This parameter is represented from Note1
#define byte    EcBRAMData     //This parameter is represented from Note2
#define byte    BRAMLDNReg     //This parameter is represented from Note3
#define byte    BRAMFnData0Reg     //This parameter is represented from Note4
#define byte    BRAMFnData1Reg     //This parameter is represented from Note5
#define    void    EcBRAMWriteByte(byte Offset, byte Value);
#define    byte    EcBRAMReadByte(byte Offset);
#define    void    IOWriteByte(byte Offset, byte Value);
#define    byte    IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte    DIO0ToDIO7Reg    // This parameter is represented from Note6
#define byte    DIO0Bit    // This parameter is represented from Note7
#define byte    DIO1Bit    // This parameter is represented from Note8
#define byte    DIO2Bit    // This parameter is represented from Note9
#define byte    DIO3Bit    // This parameter is represented from Note10
#define byte    DIO4Bit    // This parameter is represented from Note11
#define byte    DIO5Bit    // This parameter is represented from Note12
#define byte    DIO6Bit    // This parameter is represented from Note13
#define byte    DIO7Bit    // This parameter is represented from Note14
#define byte    DIO0Val    // This parameter is represented from Note15
#define byte    DIO1Val    // This parameter is represented from Note16
#define byte    DIO2Val    // This parameter is represented from Note17
#define byte    DIO3Val    // This parameter is represented from Note18
#define byte    DIO4Val    // This parameter is represented from Note19
#define byte    DIO5Val    // This parameter is represented from Note20
#define byte    DIO6Val    // This parameter is represented from Note21
#define byte    DIO7Val    // This parameter is represented from Note22
*******************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //        Example, Read Digital I/O Pin 3 status
         // Output :
         //       InputStatus :
         //                0: Digital I/O Pin level is low
         //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //        Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*********************************************************************************
```

```
*******************************************************************************
Boolean    AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID    AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
         ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*******************************************************************************
```

```
*****************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, FnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*****************************************************************************
```

Appendix D

Note for Users

D.1 Notes for Users – HSIO configurations

NANOCOM-KBU-A20's HSIO has specific settings as follow.

PICMG PCIe No.	Config 1 (Default)	Config 2* (Custom BIOS only)
PCIe#0	PCIe[x1]	PCIe[x4]
PCIe#1	PCIe[x1]	
PCIe#2	PCIe[x1]	
PCIe#3	PCIe[x1]	
GbE	GbE	GbE
SATA#0	SATA#0	SATA#0
SATA#1	SATA#1	SATA#1

*Config 2 can be requested through your AAEON contact.

D.2 Notes for Users – Display Mode

	BIOS or DOS	Under OS
UEFI Mode	Single Display only, default is DP via DDI0.	2 display ok
Legacy	Single Display only, default is DP via DDI0.	2 display ok

*NANOCOM-KBU-A20 supports either LVDS + DDI0 (DP/HDMI) or option for eDP + DDI0 (DP/HDMI)

**Please reach your AAEON contact for eDP support

D.3 Notes for Users – CPU Support Matrix

This product supports both Intel® Core™ 6xxxU series and 7xxxU series. In order to separate the two platforms, they have been given the following naming and CPU support:

I. NanoCOM-SKU-A20-xx-xxxxx

This product supports:

i7-6600U, i5-6300U, i3-6100U, and Celeron 3955U

II. NanoCOM-KBU-A20-xx-xxxxx

This product supports:

i7-7600U, i5-7300U, i3-7100U, and Celeron 3965U