NanoCOM-BT/BT4

COM Express Module

User's Manual 4th Ed

Last Updated: July 25, 2018

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● NanoCOM-BT	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	X	O	O	O	O	O
Wires & Connectors for External Connections	X	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	Nano Module, Pin-out Type 10, COM.0 Rev. 2.1
Processor	Intel® Atom™ N2000/E3800 processor
System Memory	Onboard DDR3L 2 GB/ 4 GB
Chipset	Intel® Atom™ SOC
I/O Chipset	Intel® Atom™ SOC
Ethernet	Intel® I211/i210,10/100/1000Base-TX
BIOS	AMI BIOS, Legacy free BIOS
EEPROM	Fremont FT24C02A-5SR-T
Wake On LAN	Yes
BBS (BIOS Boot Spec)	Yes
Watchdog Timer	ITE IT8528
H/W Status Monitoring	Supports CPU temperature monitoring
Expansion Interface	PCI-Express [x1] x 3 LPC bus x 1 SMBus x 1
Power Requirement	Standard: +7 ~ 20 V AT/ATX Optional: +5 V, AT/ATX
Board Size	84 x 55 mm (3.31 x 2.17")
Gross Weight	0.2 kg (0.44 lb)

- **Operating Temperature** 0 ~ 60˚C (32 ~ 140˚F)

  -40 ~ 85˚C (-40 ~ 185˚F) - E3845/E3825
- **Storage Temperature** -40 ~ 80˚C (-40 ~ 176˚F)
- **Operation Humidity** 0% ~ 90% relative humidity, non-condensing

Display

- **Chipset** Intel® Atom™ SOC
- **Memory** Shared system memory up to 512MB
- **Resolution** LCD: Up to 1920x1200 @ single 24bit LVD

  DDI: Up 2560 x 1600 (Display Port)
- **LCD Interface** 18/24-bit single channel LVDS (Shared with eDP)
- **Display Combination** CRT + LVDS (Simultaneous/ dual display)

I/O

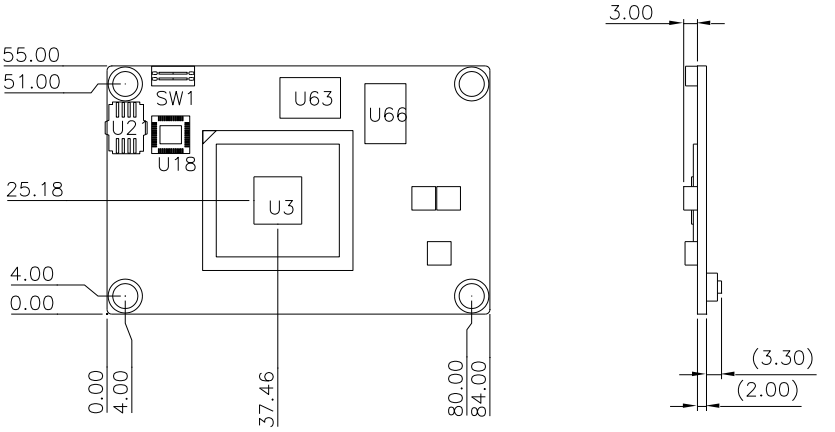
- **Storage** SATA x 2, eMMC up to 16 GB (optional)
- **USB** USB 2.0/3.0 x 1, USB 2.0 x 6
- **Serial Port** TX/RX x 2
- **Audio** High definition audio
- **GPI/O** Up to 4 in and 4 out share with SDIO
- **Keyboard & Mouse** From LPC interface on carrier board

Chapter 2

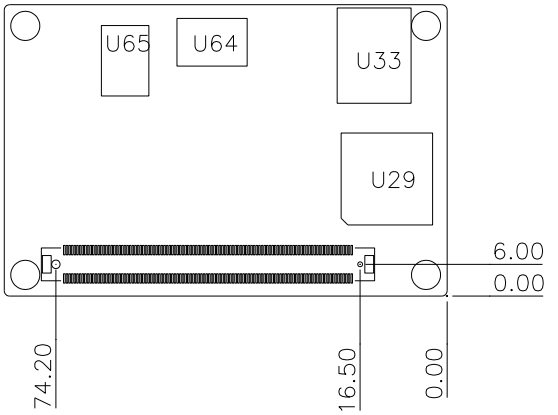
Hardware Information

2.1 Dimensions, Jumpers and Connectors

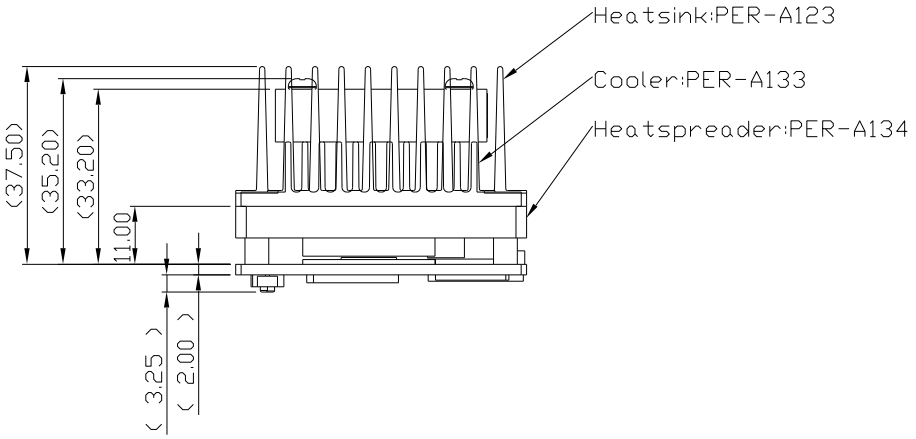
Component Side



Solder Side



With heat spreader



2.2 List of Switches and Connectors

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
SW1	AT/ ATX switch
CN1	ROW A/B connector

2.2.1 AT/ATX Switch (SW1)

Pin	Function
1 (On)	AT Mode
2 (On)	RTC reset
1 (Off)	ATX Mode
2 (Off)	RTC Normal

2.2.2 ROW A/B Connector (CN1)

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	N.C	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-

A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB3_RXN0	B22	USB3_TXN0
A23	USB3_RXP0	B23	USB3_TXP0
A24	SUS_S5#	B24	PWR_OK
A25	N.C	B25	N.C
A26	N.C	B26	N.C
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	N.C
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	N.C
A37	USB6+	B37	N.C
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-

A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C	B52	N.C
A53	N.C	B53	N.C
A54	GPI0	B54	GPO1
A55	N.C	B55	N.C
A56	N.C	B56	N.C
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	DDI0_PAIR0+
A72	LVDS_A0-	B72	DDI0_PAIR0-
A73	LVDS_A1+	B73	DDI0_PAIR1+

A74	LVDS_A1-	B74	DDI0_PAIR1-
A75	LVDS_A2+	B75	DDI0_PAIR2+
A76	LVDS_A2-	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN	B77	N.C
A78	LVDS_A3+	B78	N.C
A79	LVDS_A3-	B79	LVDS_BKLD_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	DDI0_PAIR3+
A82	LVDS_A_CK-	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	N.C	B86	VCC_5V_SBY
A87	N.C	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	N.C
A92	SPI_MISO	B92	N.C
A93	GPO0	B93	N.C
A94	SPI_CLK	B94	N.C
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	GND	B96	N.C
A97	TYPE10#	B97	SPI_CS#
A98	RS1_TX	B98	DDI0_CTRL_CLK
A99	RS1_RX	B99	DDI0_CTRL_DATA
A100	GND (FIXED)	B100	GND (FIXED)
A101	RS2_TX	B101	FAN_PWMOUT

A102	RS2_RX	**B102**	FAN_TACHIN
A103	LID#	**B103**	SLEEP#
A104	VCC_12V	**B104**	VCC_12V
A105	VCC_12V	**B105**	VCC_12V
A106	VCC_12V	**B106**	VCC_12V
A107	VCC_12V	**B107**	VCC_12V
A108	VCC_12V	**B108**	VCC_12V
A109	VCC_12V	**B109**	VCC_12V
A110	GND (FIXED)	**B110**	GND (FIXED)

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

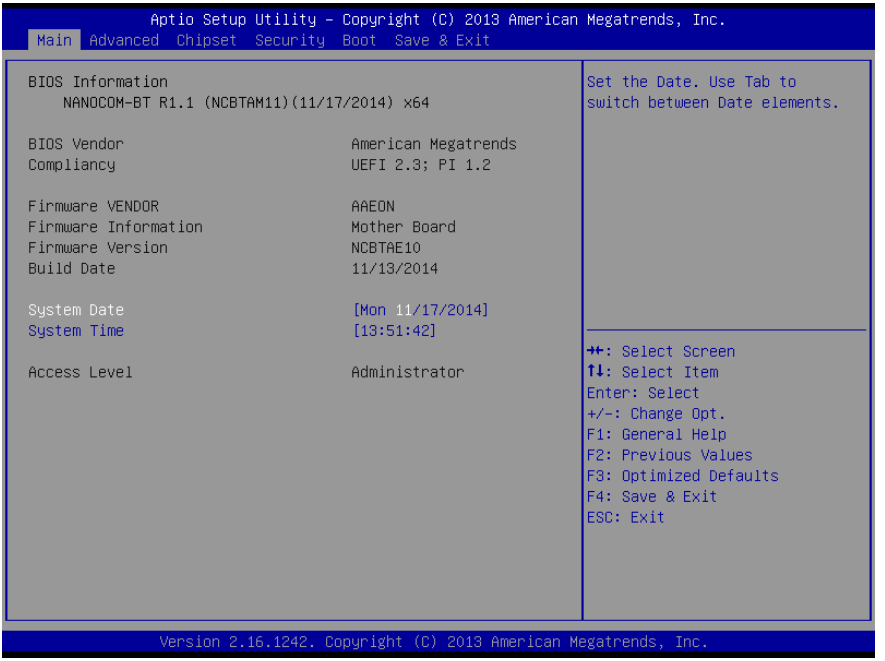
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

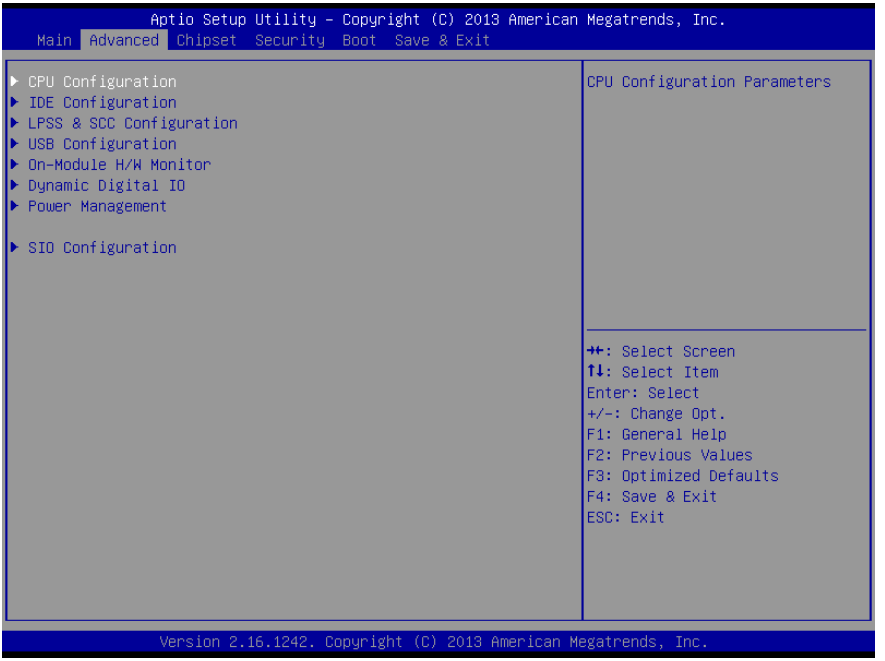
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

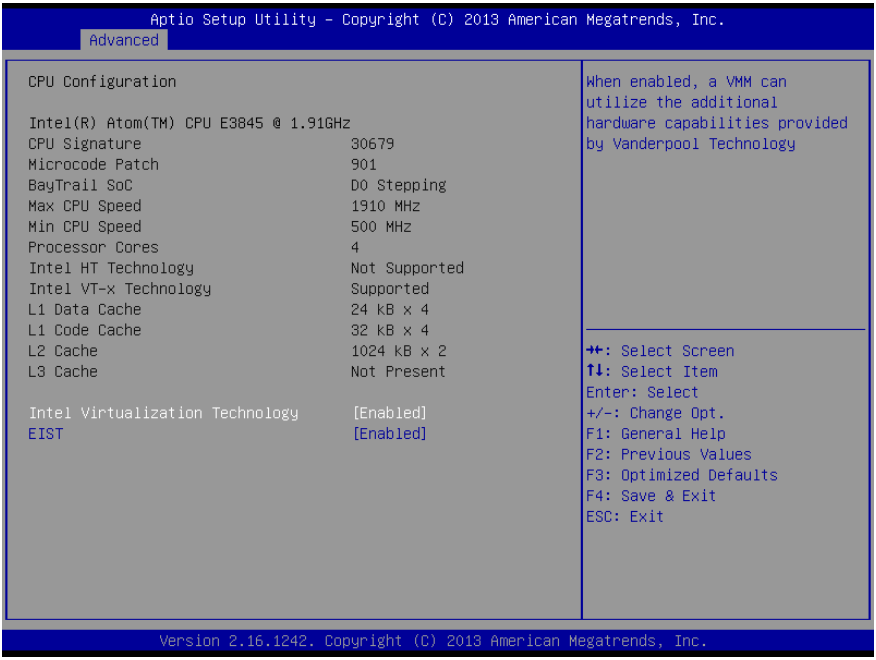
3.3 Setup submenu: Main



3.4 Setup submenu: Advanced



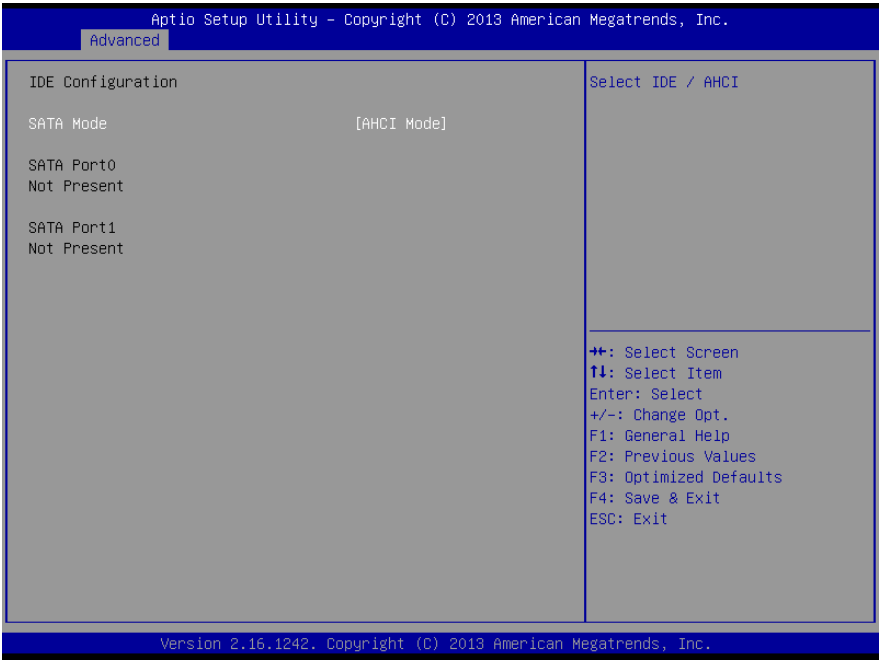
3.4.1 Advanced: CPU Configuration



Options summary:

Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default

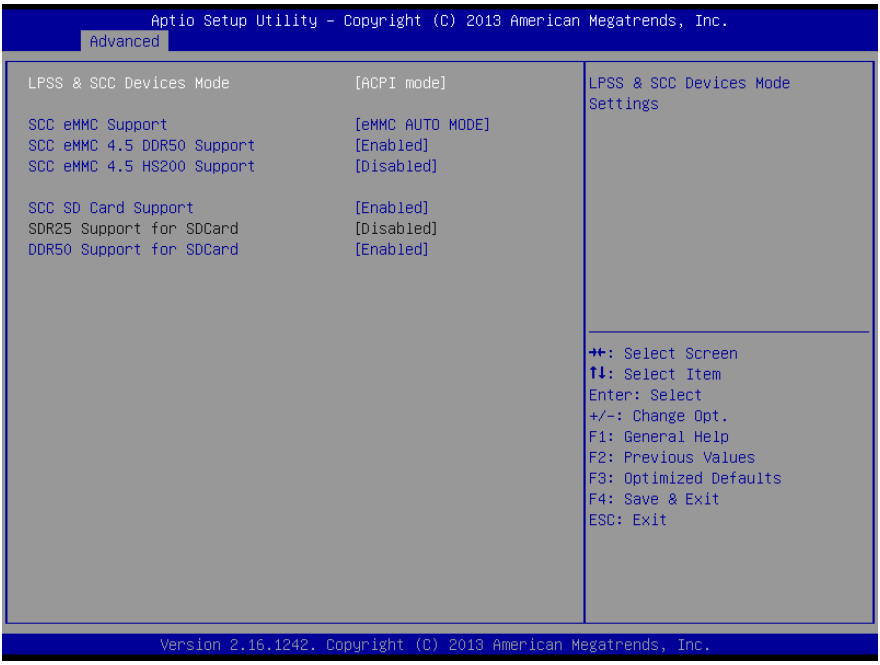
3.4.2 Advanced: IDE Configuration



Options summary:

SATA Mode	IDE Mode	
	AHCI Mode	Optimal Default, Failsafe Default

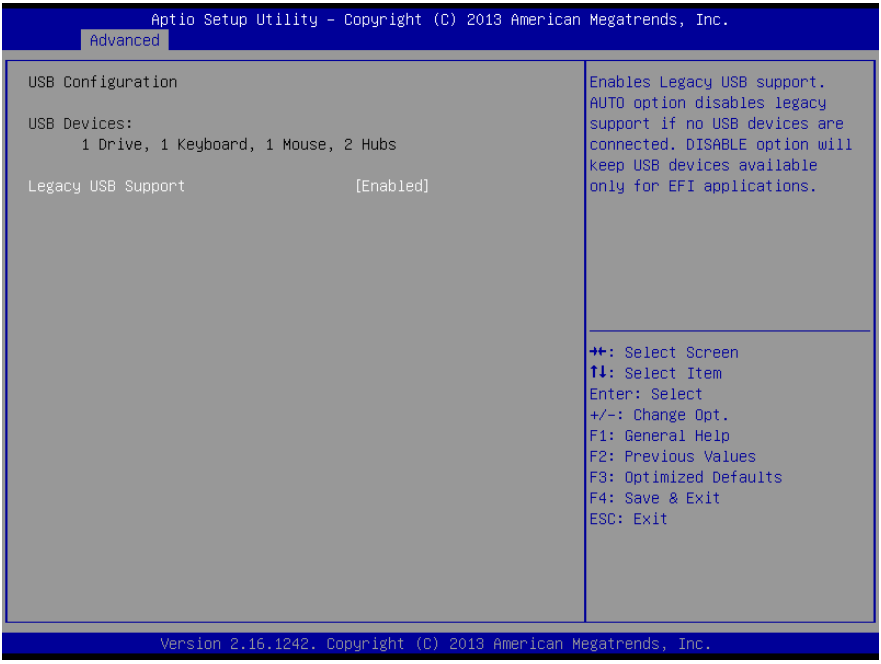
3.4.3 Advanced: LPSS & SCC Configuration



LPSS & SCC Devices Mode	ACPI mode	Optimal Default, Failsafe Default
	PCI mode	
LPSS & SCC Devices Mode Settings (Please set PCI mode for Linux O/S)		
SCC eMMC Support	Enable eMMC 4.5 Support	Optimal Default, Failsafe Default
	Enable eMMC 4.41 Support	
	eMMC AUTO MODE	
	Disabled	
SCC eMMC Support Enable\Disable		
SCC eMMC 4.5 DDR50 Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
SCC eMMC 4.5 DDR50 Support Enable\Disable		
SCC eMMC 4.5 HS200	Enabled	

Support	Disabled	Optimal Default, Failsafe Default
SCC eMMC 4.5 HS200 Support Enable\Disable		
SCC SD Card Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
SCC SD Card Support Enable\Disable		
SDR25 Support for SDCard	Enabled	
	Disabled	Optimal Default, Failsafe Default
Disable/Enable SDR25 Capability in SD Card controller		
SDR50 Support for SDCard	Enabled	Optimal Default, Failsafe Default
	Disabled	
Disable/Enable SDR50 Capability in SD Card controller		

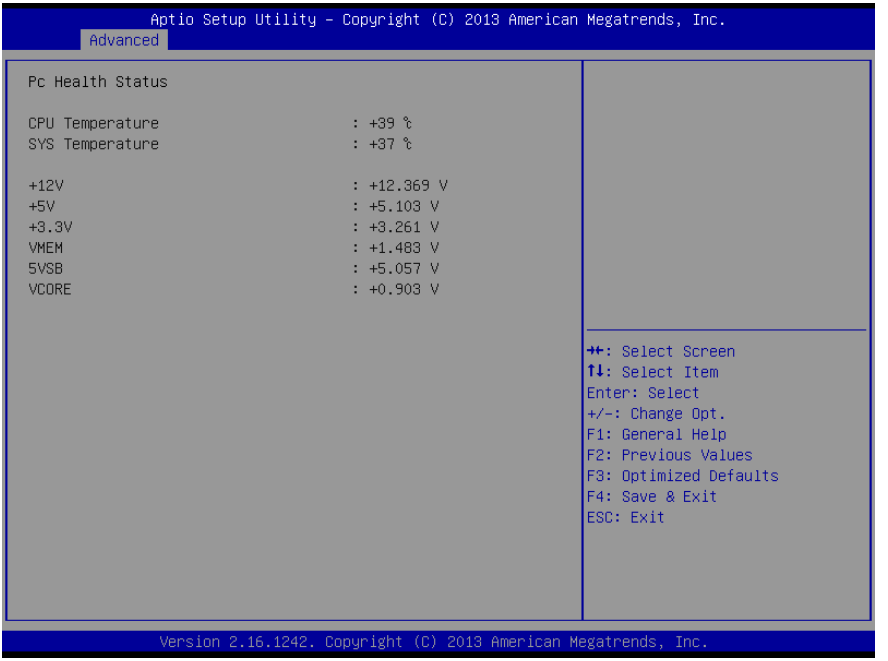
3.4.4 Advanced: USB Configuration



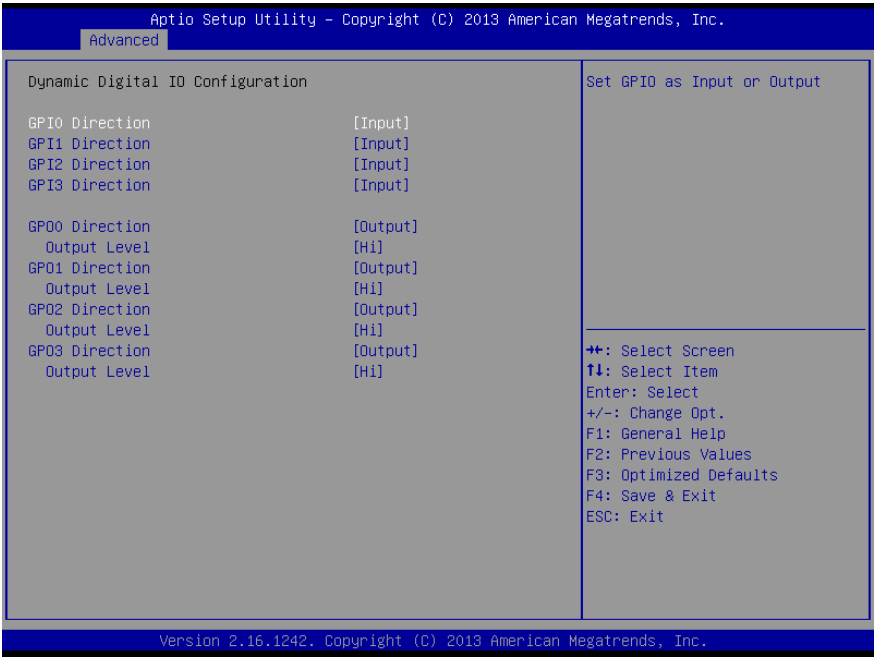
Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
	CDROM	
If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)		
USB Port 0/1 function routing	FCH USB port 8/9	Optimal Default, Failsafe Default
	FCH USB port 0/1	

3.4.5 Advanced: Hardware Monitor



3.4.6 Advanced: Dynamic Digital IO Configuration



Options summary:

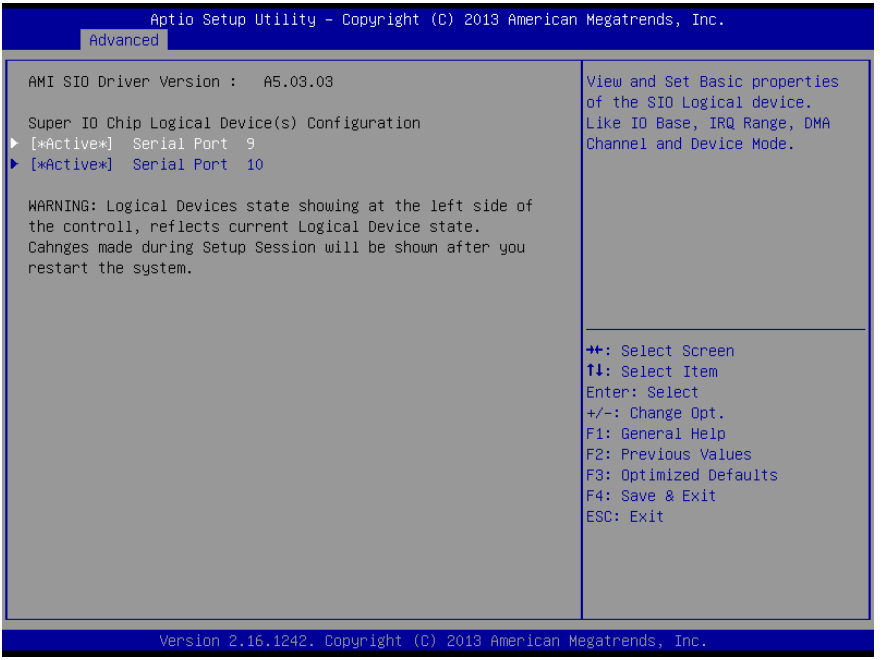
GPI[3:0] Direction	Input	Optimal Default, Failsafe Default
	Output	
Set GPI[3:0] as Input or Output		
GPI[3:0] Output Level	Hi	Optimal Default, Failsafe Default
	Low	
Set GPI[3:0] Output as Hi or Low		
GPO[3:0] Direction	Input	
	Output	Optimal Default, Failsafe Default
Set GPO[3:0] as Input or Output		
GPO[3:0] Output Level	Hi	Optimal Default, Failsafe Default
	Low	
Set GPO[3:0] Output as Hi or Low		

3.4.7 Advanced: Power Management

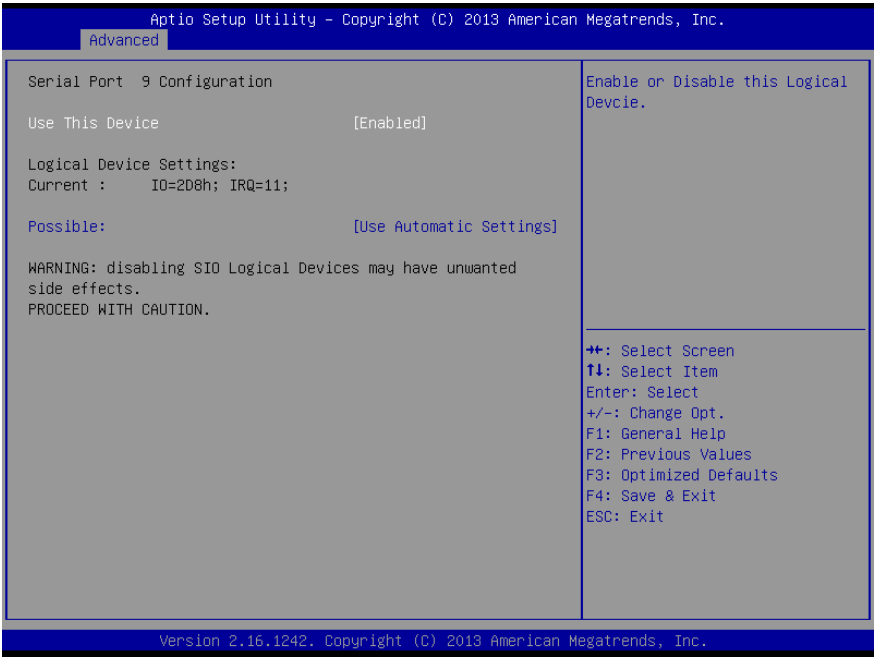
Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore on Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

3.4.8 Advanced: SIO Configuration



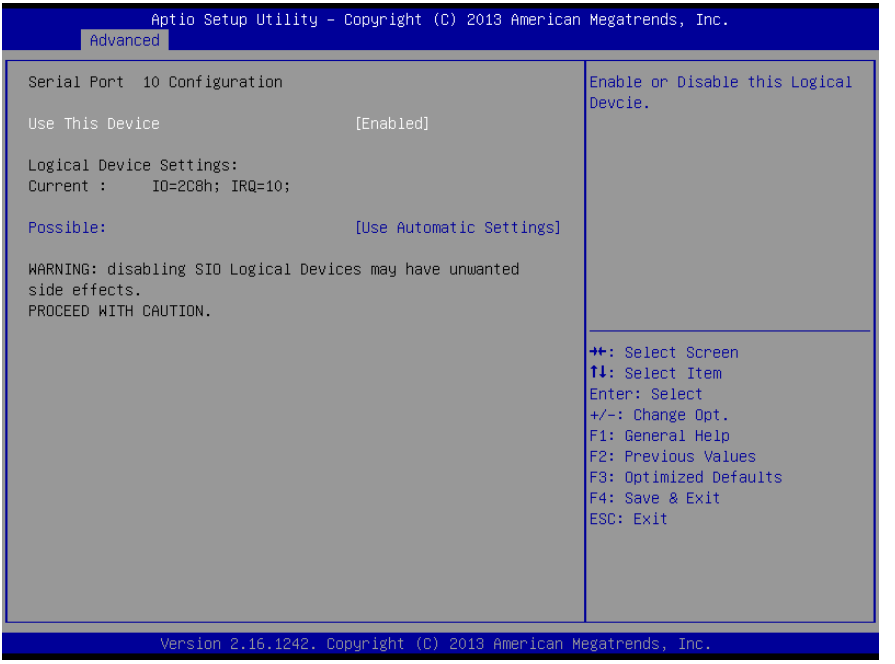
3.4.8.1 SIO Configuration: Serial Port 9 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2D8; IRQ=11;	
	IO=2C8; IRQ=11;	
Select an optimal setting for IO device		

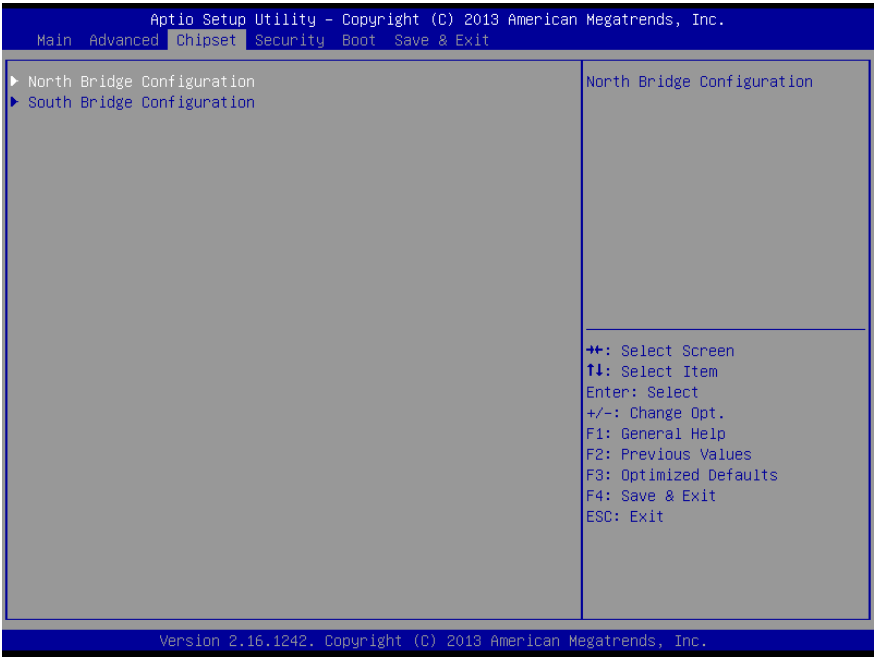
3.4.8.2 SIO Configuration: Serial Port 10 Configuration



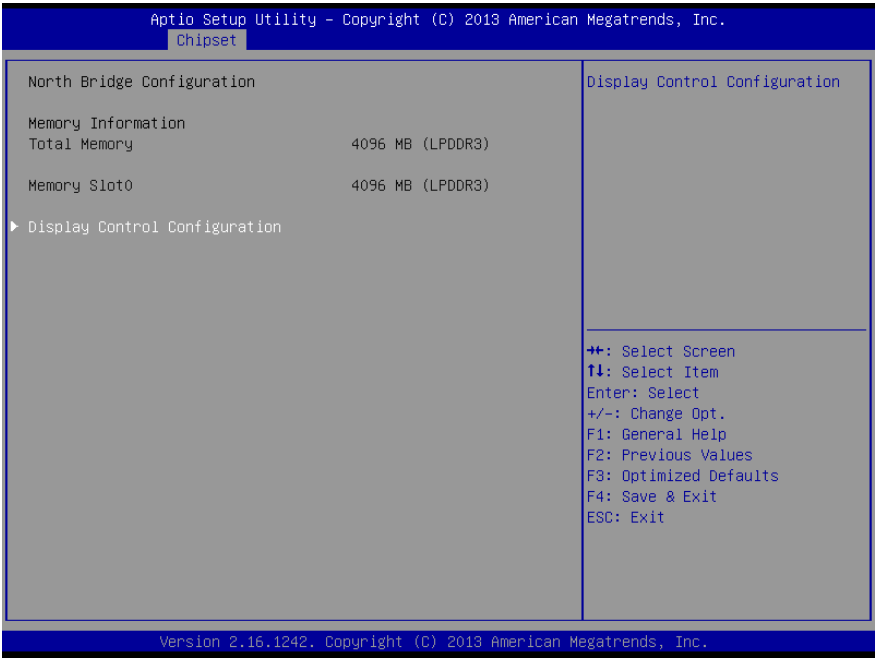
Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2D8; IRQ=11;	
	IO=2C8; IRQ=11;	
Select an optimal setting for IO device		

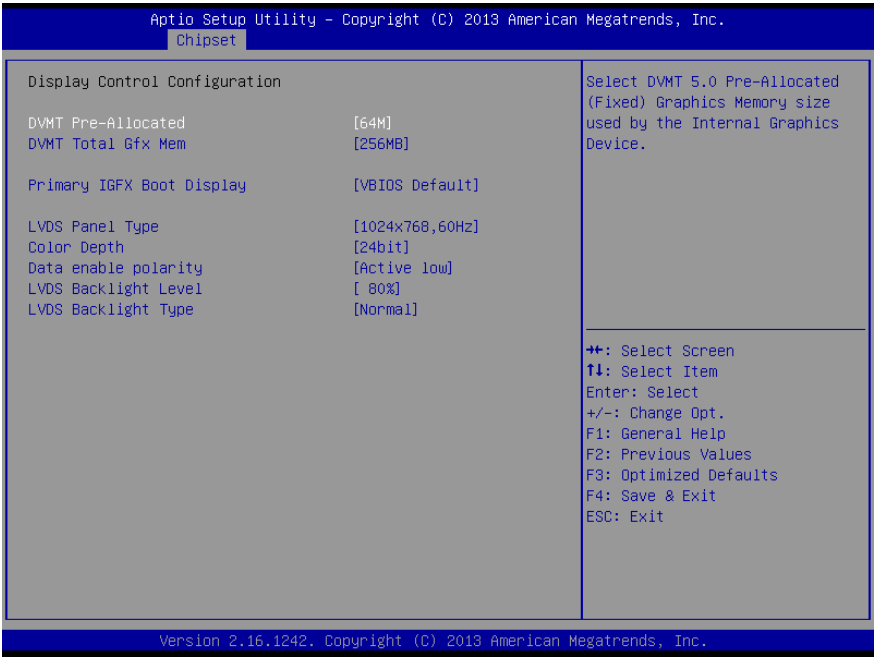
3.5 Setup submenu: Chipset



3.5.1 Chipset: North Bridge



3.5.1.1 North Bridge: Display Control Configuration

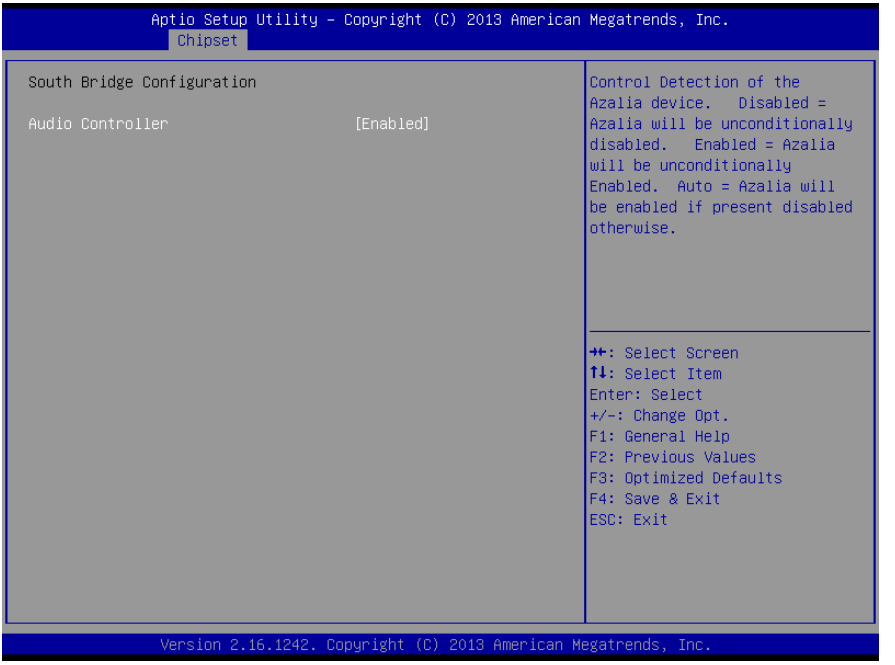


Options summary:

DVMT Pre-Allocated	64M	Optimal Default, Failsafe Default
	96M	
	128M	
	160M …	
	512M	
DVMT Total Gfx Mem	128MB	Optimal Default, Failsafe Default
	256MB	
	Max	
Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	CRT	
	LVDS	
	DP/HDMI	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display		

Secondary IGFX Boot Display	Disabled	Optimal Default, Failsafe Default
	CRT	
	LVDS	
	DP/HDMI	
Select Secondary Display Device		
LVDS Panel Type	640x480,18bit,60Hz	Optimal Default, Failsafe Default
	800x480,18bit,60Hz	
	800x600,18bit,60Hz	
	1024x600,18bit,60Hz	
	1024x768,18bit,60Hz	
	1024x768,24bit,60Hz	
	1280x768,24bit,60Hz	
	1280x1024,48bit,60Hz	
	1366x768,24bit,60Hz	
	1440x900,48bit,60Hz	
	1600x1200,48bit,60Hz	
	1920x1080,48bit,60Hz	
	1920x1200,48bit,60Hz	
Color Depth	24bit	Optimal Default, Failsafe Default
	18bit	
Data enable polarity	Active Low	Optimal Default, Failsafe Default
	Active High	

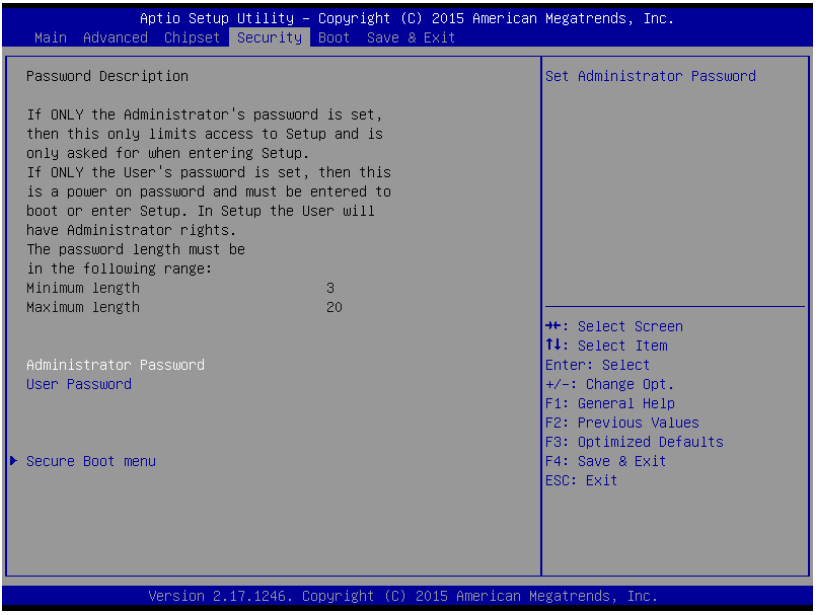
3.5.2 Chipset: South Bridge



Options summary:

Audio Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	

3.6 Setup submenu: Security



Change User/Administrator Password

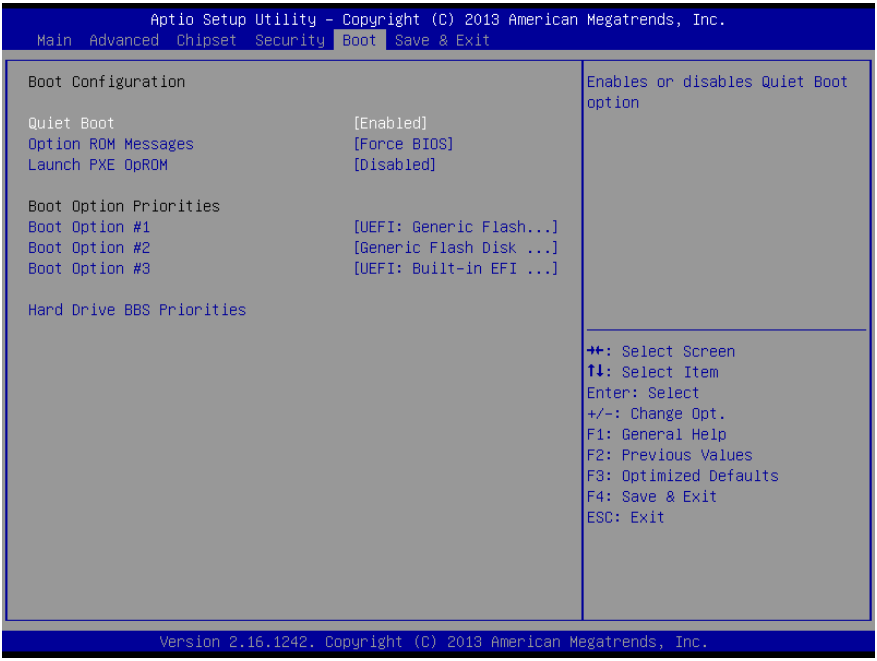
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup submenu: Boot

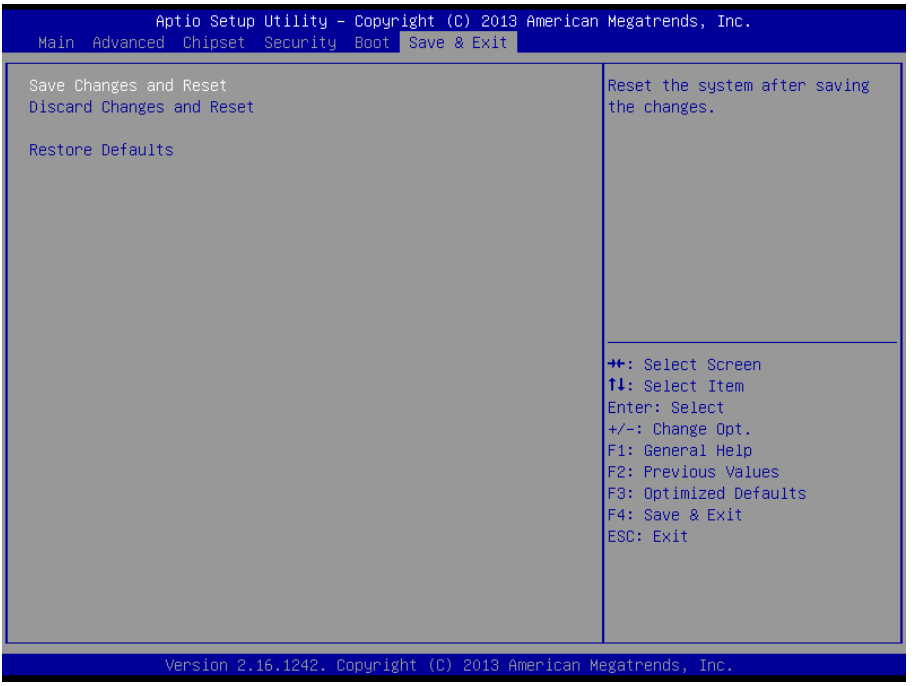


Options summary:

Quiet Boot	Disabled	
	Enabled	Default
En/Disable showing boot logo.		
Option ROM Messages	Force BIOS	Default
	Keep Current	
Set display mode for Option ROM		
Launch PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option		

3.7.1 Boot: BBS Priorities

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The NanoCOM-BT comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step1 – Chipset** followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step2 - Graphic** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install Atom E3800 I/O Driver

1. Click on the **Step3 – Atom_E3800_IO** folder and select your OS
2. Open the **.exe or .msi** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Network Drivers

1. Open the **Step4 - Network** folder and select your OS
2. Open the.**exe** file in the folder

3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **Step5 - USB3.0** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Intel Sideband Fabric Device Driver

1. Open the **Step6 – Intel Sideband Fabric Driver** folder followed **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnDataReg   //This parameter is represented from Note4
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerReg   //This parameter is represented from Note5
#define byte   TimerVal   // This parameter is represented from Note10
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note11
#define byte   RSTReg   //This parameter is represented from Note8
#define byte   RSTBit   //This parameter is represented from Note9
#define byte   RSTVal   //This parameter is represented from Note12
*******************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable ()
       WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig ()
        // Disable WDT counting
        WDTEnableDisable(0);
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte Value)
      ECBRAMWriteByte(TimerReg , Value);
}

VOID   WDTParameterSetting()
      Byte TempByte;

        // Watchdog Timer counter setting
       ECBRAMWriteByte(TimerReg , TimerVal);
      // WDT counting unit setting
       TempByte = ECBRAMReadByte(UnitReg);
       TempByte |= (UnitVal << UnitBit);
       ECBRAMWriteByte(UnitReg , TempByte);
       // WDT RST pulse width setting
       TempByte = ECBRAMReadByte(RSTReg);
       TempByte |= (RSTVal << RSTBit);
       ECBRAMWriteByte(RSTReg , TempByte);
}
*****************************************************************************
```

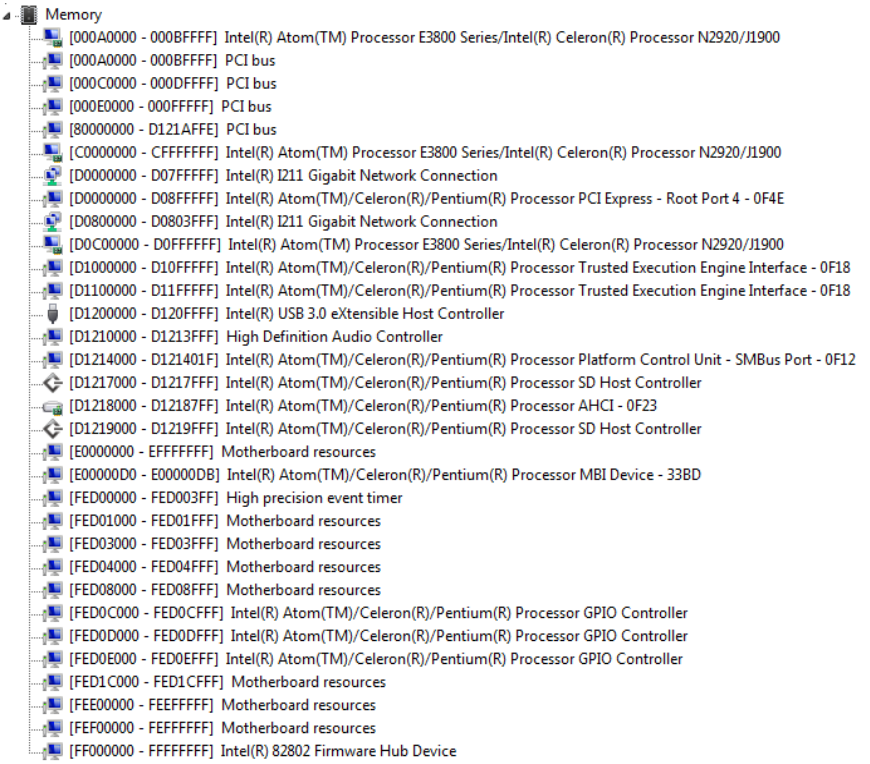
```
*******************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        IOWriteByte(EcBRAMData, Value);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x30);              //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x10);              //Read start

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        Return      IOReadByte(EcBRAMData, Value);
}
*******************************************************************************
```

Appendix B

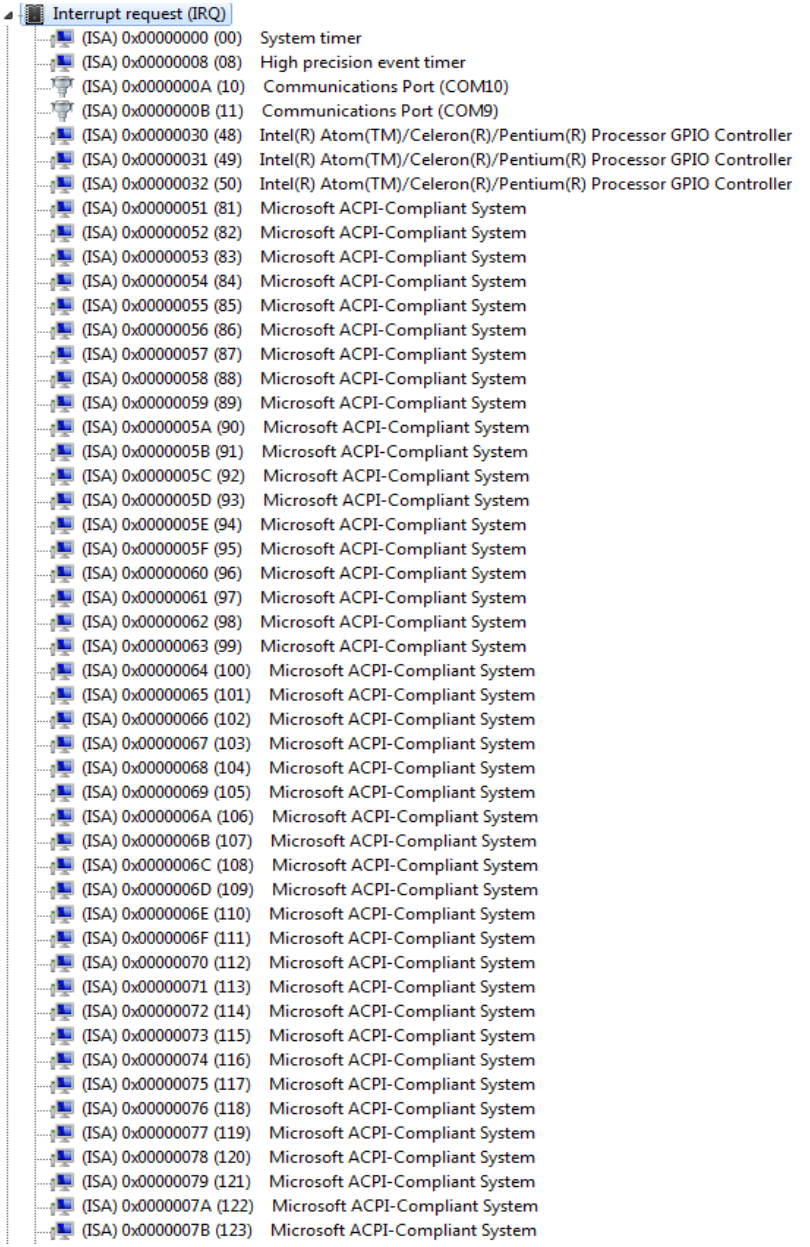
I/O Information

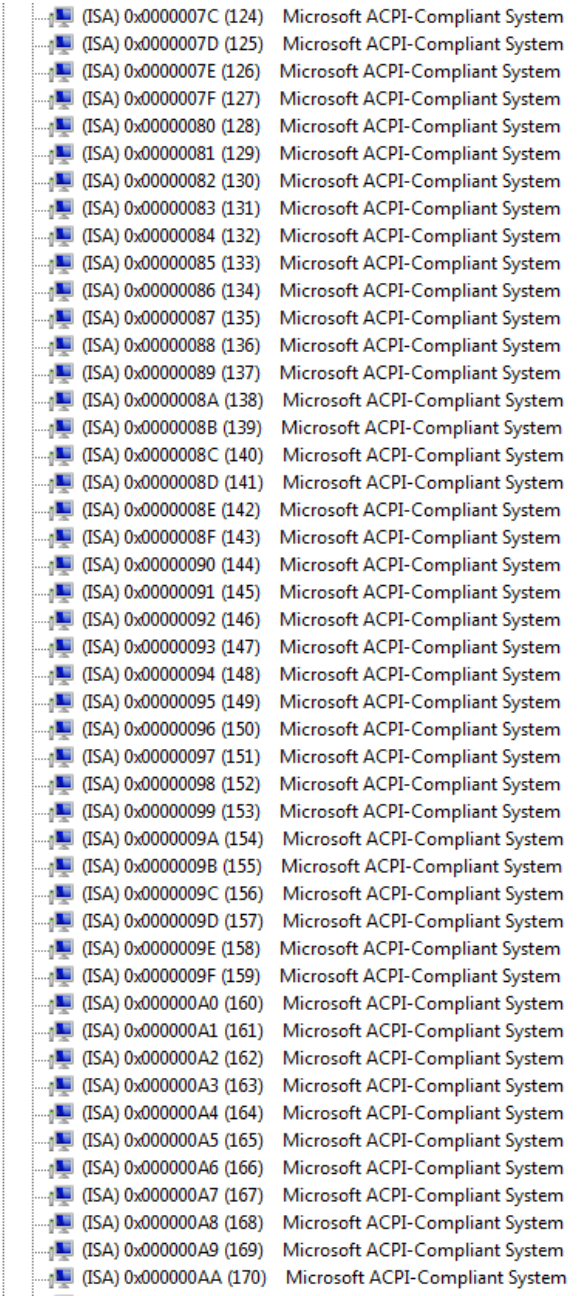
B.1 I/O Address Map

B.2 Memory Address Map



B.3 IRQ Mapping Chart




(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System

- (ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
- (ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
- (ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
- (ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
- (ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
- (ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
- (ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
- (ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
- (ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
- (ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
- (ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
- (ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
- (ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
- (ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
- (ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
- (ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
- (ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
- (PCI) 0x00000003 (03) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Platform Control Unit - SMBus Port - 0F12
- (PCI) 0x00000004 (04) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Trusted Execution Engine Interface - 0F18
- (PCI) 0x00000010 (16) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 1 - 0F48
- (PCI) 0x00000011 (17) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 2 - 0F4A
- (PCI) 0x00000012 (18) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor SD Host Controller
- (PCI) 0x00000012 (18) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 3 - 0F4C
- (PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- (PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 4 - 0F4E
- (PCI) 0x00000016 (22) High Definition Audio Controller
- (PCI) 0xFFFFFFF7 (-9) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF8 (-8) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF9 (-7) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFFA (-6) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFFB (-5) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFFC (-4) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFFD (-3) Intel(R) USB 3.0 eXtensible Host Controller
- (PCI) 0xFFFFFFFE (-2) Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900

Appendix C

Programming Digital I/O

C.1 DI/O Programming

NanoCOM-BT utilizes ITE8518 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can develop customized program to fit your application.

C.2 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
Input/Output Function and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
Output Data Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

C.3 Digital I/O Sample Program

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnData0Reg    //This parameter is represented from Note4
#define byte   BRAMFnData1Reg    //This parameter is represented from Note5
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DIO0ToDIO7Reg   // This parameter is represented from Note6
#define byte   DIO0Bit   // This parameter is represented from Note7
#define byte   DIO1Bit   // This parameter is represented from Note8
#define byte   DIO2Bit   // This parameter is represented from Note9
#define byte   DIO3Bit   // This parameter is represented from Note10
#define byte   DIO4Bit   // This parameter is represented from Note11
#define byte   DIO5Bit   // This parameter is represented from Note12
#define byte   DIO6Bit   // This parameter is represented from Note13
#define byte   DIO7Bit   // This parameter is represented from Note14
#define byte   DIO0Val   // This parameter is represented from Note15
#define byte   DIO1Val   // This parameter is represented from Note16
#define byte   DIO2Val   // This parameter is represented from Note17
#define byte   DIO3Val   // This parameter is represented from Note18
#define byte   DIO4Val   // This parameter is represented from Note19
#define byte   DIO5Val   // This parameter is represented from Note20
#define byte   DIO6Val   // This parameter is represented from Note21
#define byte   DIO7Val   // This parameter is represented from Note22
*******************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //      Example, Read Digital I/O Pin 3 status
        // Output :
        //      InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //      Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*********************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID    AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
         ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*****************************************************************************
```

```
*****************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        IOWriteByte(EcBRAMData, Value);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x30);              //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, FnDataReg);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x10);              //Read start

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        Return      IOReadByte(EcBRAMData, Value);
}
*****************************************************************************
```