NanoCOM-APL

COM Express Module

User's Manual 4th Ed

Last Updated: October 1, 2021

Copyright Notice

Acknowledgements

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● NanoCOM-APL-A11	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	X	O	O	O	O	O
Wires & Connectors for External Connections	X	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	COM Express Mini Size, Type 10
CPU	Intel® Atom™/ Celeron®/ Pentium® Processor
CPU Frequency	Up to 2.00 GHz (J1900)
Chipset	Intel® Atom™/Celeron®/Pentium® SoC
Memory Type	Onboard LPDDR4 up to 2400 MT/s
Max. Memory Capacity	Up to 8GB
BIOS	AMI BIOS, Legacy free
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	Standard: +12V
Power Supply Type	AT/ATX
Power Consumption (Typical)	0.82A at 12V, full load, E3950
Dimension (L x W)	3.31" x 2.17" (84mm x 55mm)
Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
	-40°F ~ 185°F (-40°C ~ 85°C) (Optional)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	885,779 Hours
Certification	CE/ FCC Class A

Display	
VGA/LCD Controller	Intel® HD Graphics 505/500
Video Output	Dual Display:
	Single Channel LVDS (18/24 bit) or eDP, DDI x 1

I/O

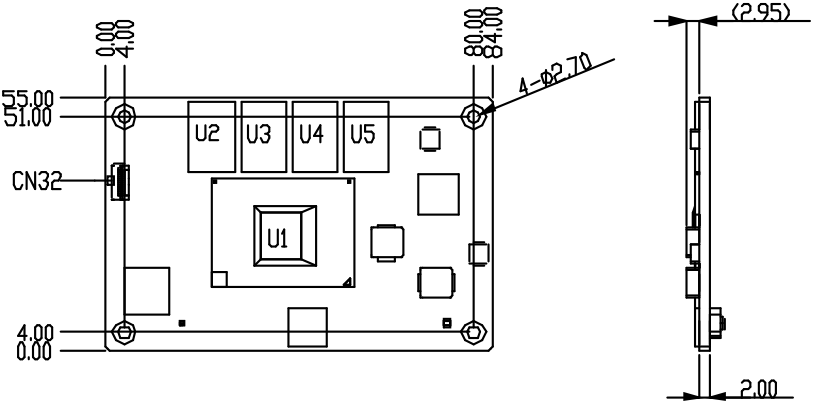
Ethernet	Intel® i211AT Gigabit Ethernet x 1
Audio	High Definition Audio Interface
USB Support	USB2.0 x 8
	USB3.2 Gen 1 x 2
Serial Port	2-wire UART (Tx/Rx) x 2
HDD Interface	SATA III x 2
Expansion	PCIe [x1] x 4 (up to 3 devices)
	LPC
	SMbus
	I2C
GPIO	GPIO 8-bit
Onboard Storage	Onboard eMMC (Up to 64GB, optional)
TPM	—

Chapter 2

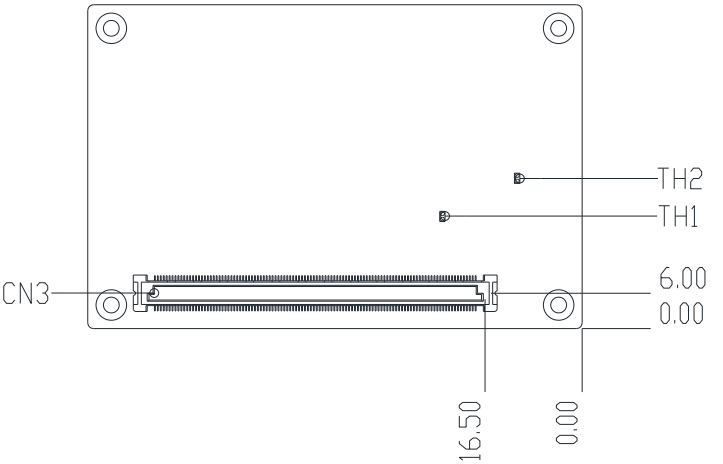
Hardware Information

2.1 Dimensions, Jumpers and Connectors

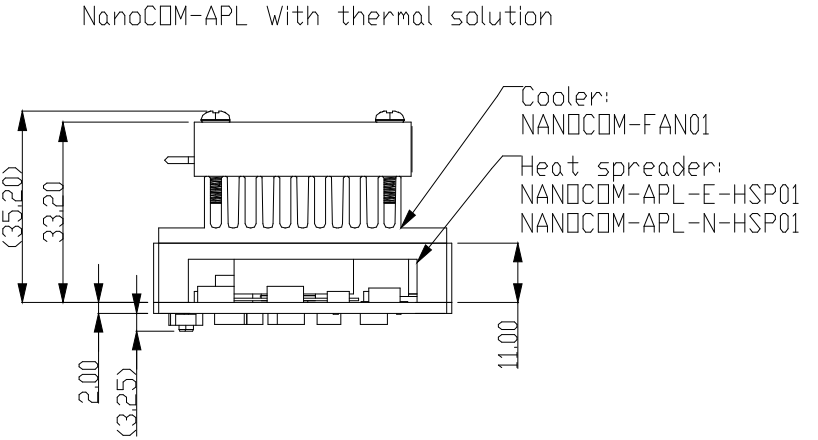
Component Side



Solder Side



With heat spreader



2.2 List of Switches and Connectors

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN3	ROW A/B

2.2.1 ROW A/B Connector (CN3)

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	N.C	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+

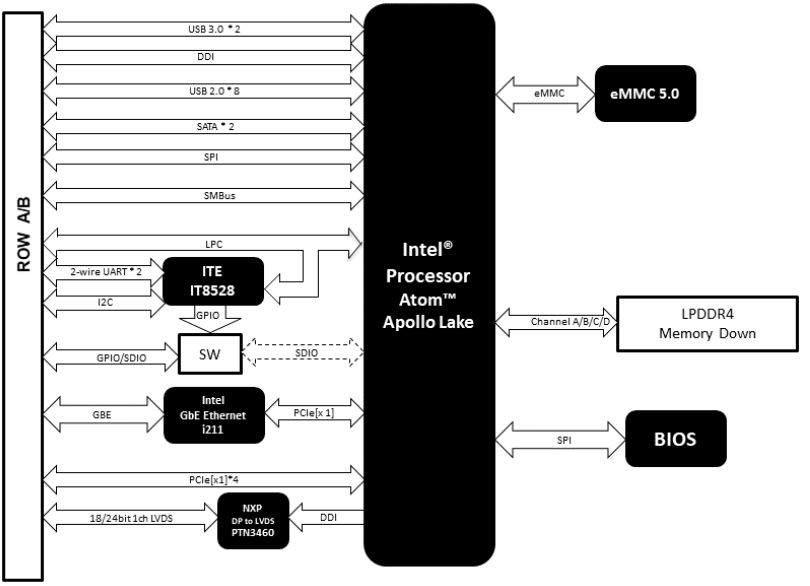
Row A		Row B	
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB3_RXN0	B22	USB3_TXN0
A23	USB3_RXP0	B23	USB3_TXP0
A24	SUS_S4#	B24	PWR_OK
A25	USB3_RX1_N	B25	USB3_TX1_N
A26	USB3_RX1_P	B26	USB3_TX1_P
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	N.C
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-

Row A		Row B	
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C	B52	N.C
A53	N.C	B53	N.C
A54	GPI0	B54	GPO1
A55	N.C	B55	N.C
A56	N.C	B56	N.C
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+

Row A		Row B	
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+(EDP_TX2_P)	B71	DDI0_PAIR0+
A72	LVDS_A0-(EDP_TX2_N)	B72	DDI0_PAIR0-
A73	LVDS_A1+(EDP_TX1_P)	B73	DDI0_PAIR1+
A74	LVDS_A1-(EDP_TX1_N)	B74	DDI0_PAIR1-
A75	LVDS_A2+(EDP_TX0_P)	B75	DDI0_PAIR2+
A76	LVDS_A2-(EDP_TX0_N)	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN(EDP_VDDEN_3_3)	B77	N.C
A78	LVDS_A3+	B78	N.C
A79	LVDS_A3-	B79	LVDS_BKLD_EN(EDP_BKLTEN_3_3)
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+(EDP_TX3_P)	B81	DDI0_PAIR3+
A82	LVDS_A_CK-(EDP_TX3_N)	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK(EDP_AUXP)	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT(EDP_AUXN)	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	EC_KBRST#(option)	B86	VCC_5V_SBY
A87	DDI0_HPD_3.3S(option)	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	N.C
A92	SPI_MISO	B92	N.C
A93	GPO0	B93	N.C
A94	SPI_CLK	B94	N.C

Row A		Row B	
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	GND	B96	N.C
A97	TYPE10#	B97	SPI_CS#
A98	RS1_TX	B98	DDI0_CTRL_CLK
A99	RS1_RX	B99	DDI0_CTRL_DATA
A100	GND (FIXED)	B100	GND (FIXED)
A101	RS2_TX	B101	FAN_PWMOUT
A102	RS2_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

2.3 Function Block



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ disable boot option for legacy network devices

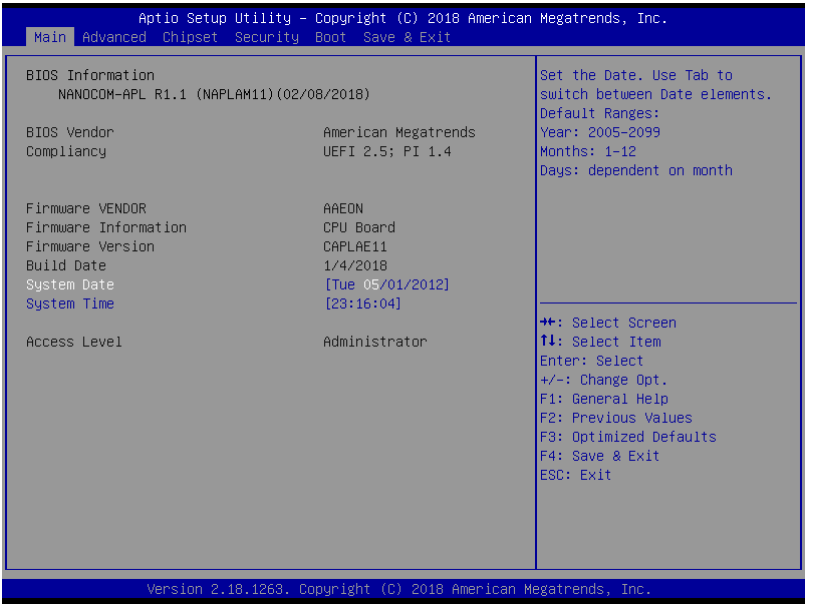
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

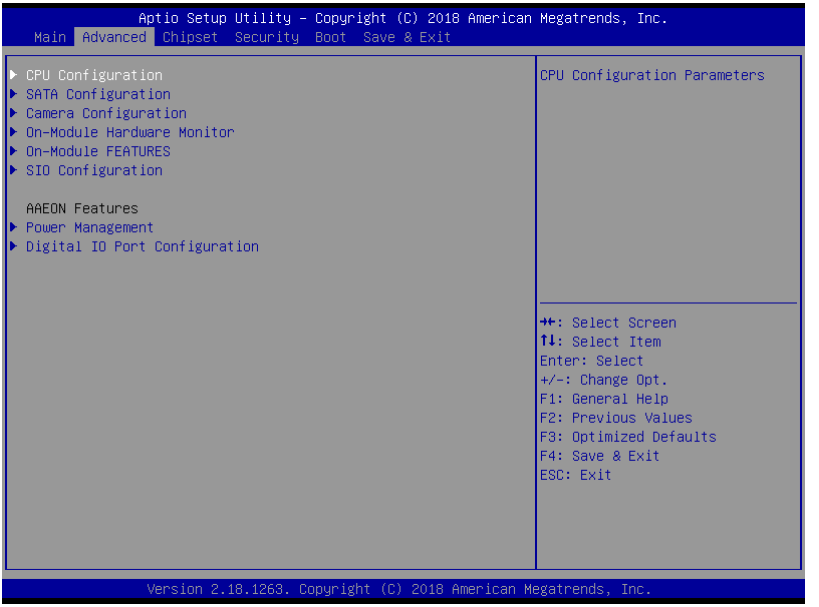
Boot – Enable/ disable Quiet Boot option

Save & Exit –Save your changes and exit the program

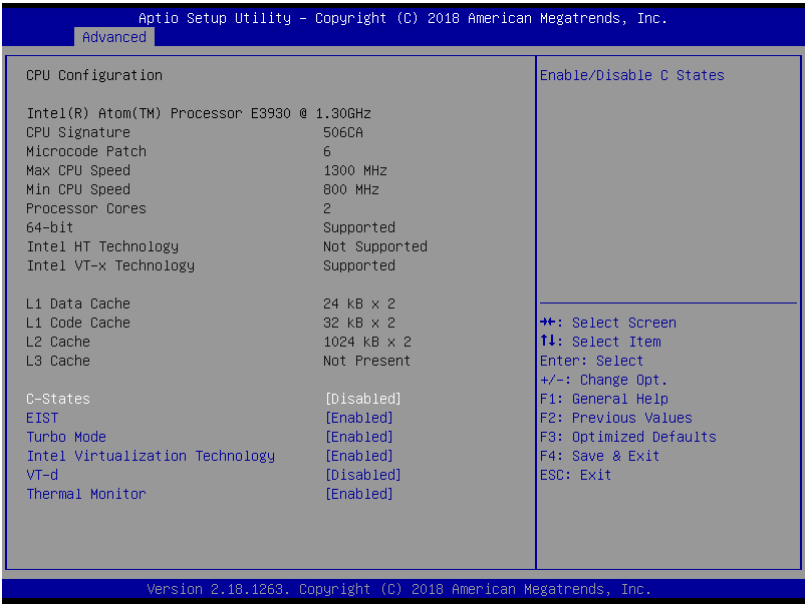
3.3 Setup submenu: Main



3.4 Setup submenu: Advanced



3.4.1 Advanced: CPU Configuration

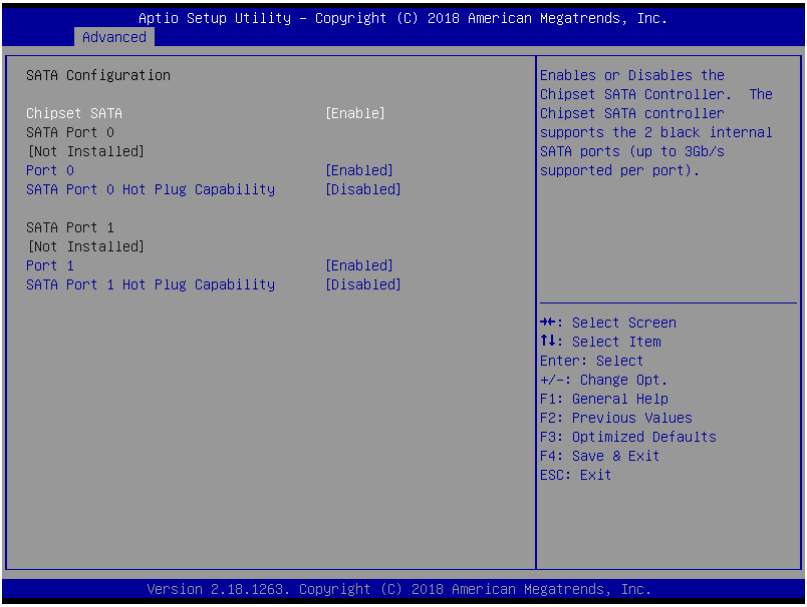


Options Summary		
C-states	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable C states.		
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Intel speedstep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode.		

Table Continues on Next Page

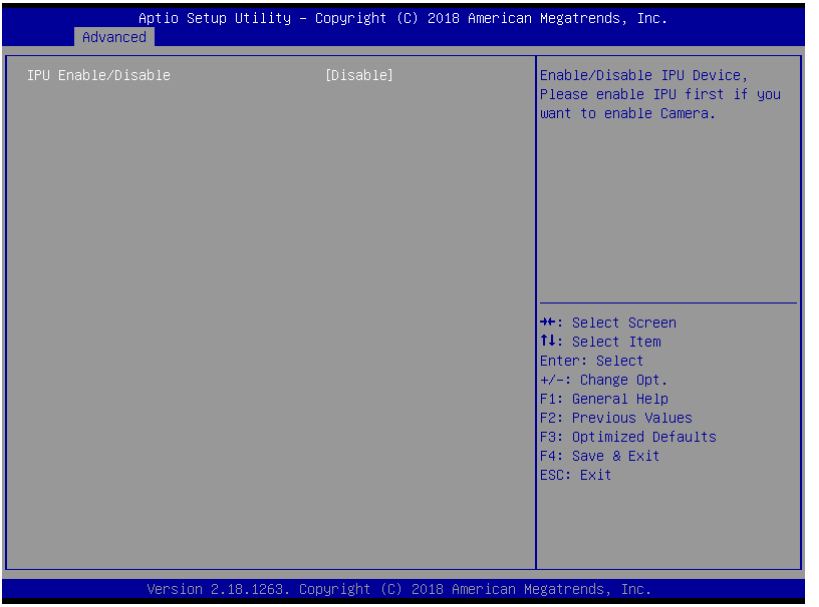
Options Summary		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable CPU VT-d.		
Thermal Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Thermal Monitor.		

3.4.2 Advanced: SATA Configuration



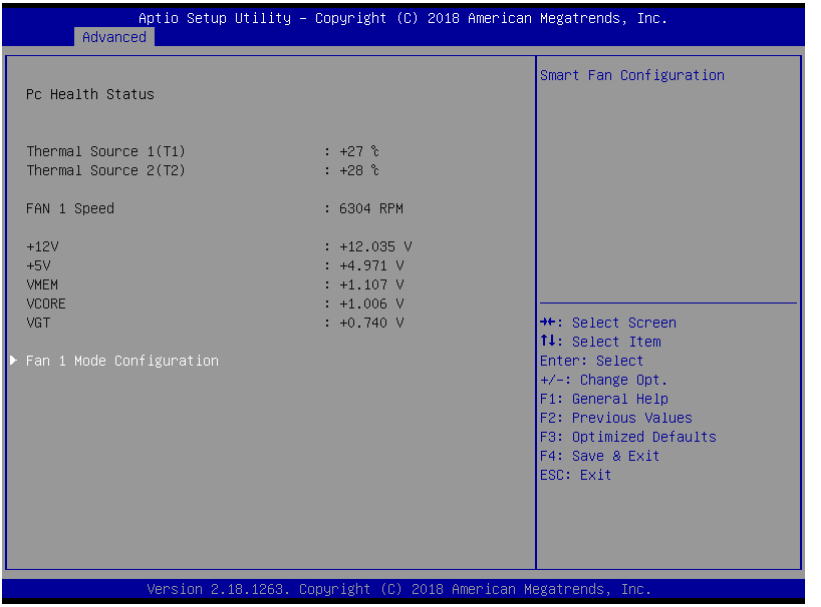
Options Summary		
Chipset SATA	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable the Chipset SATA Controller. The Chipset SATA Controller support the 2 black internal SATA ports (up to 3Gb/s supported per port).		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

3.4.3 Advanced: Camera Configuration

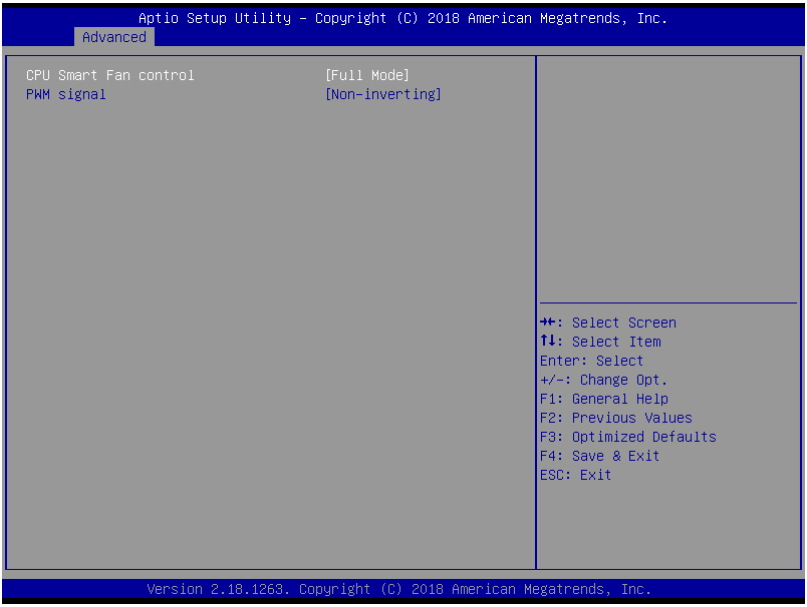


Options Summary		
IPU Enable / Disable	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/Disable IPU Device, Please enable IPU first if you want enable camera.		

3.4.4 Advanced: On-Module Hardware Monitor



3.4.4.1 Fan 1 Mode Configuration: Full Mode

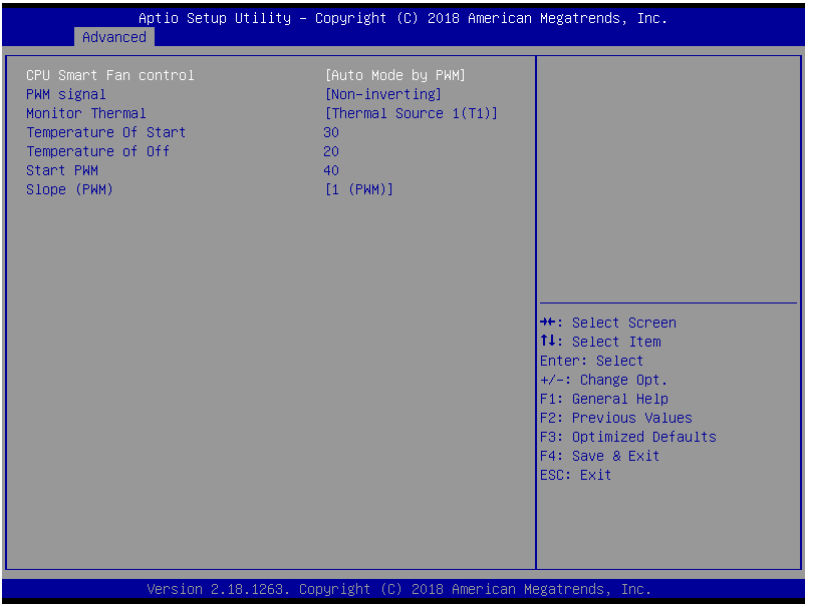


Options Summary		
CPU Smart Fan control	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		

3.4.4.2 Fan Mode Configuration: Manual Mode by PWM

Options Summary		
Manual Setting	70	Optimal Default, Failsafe Default
Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number:		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		

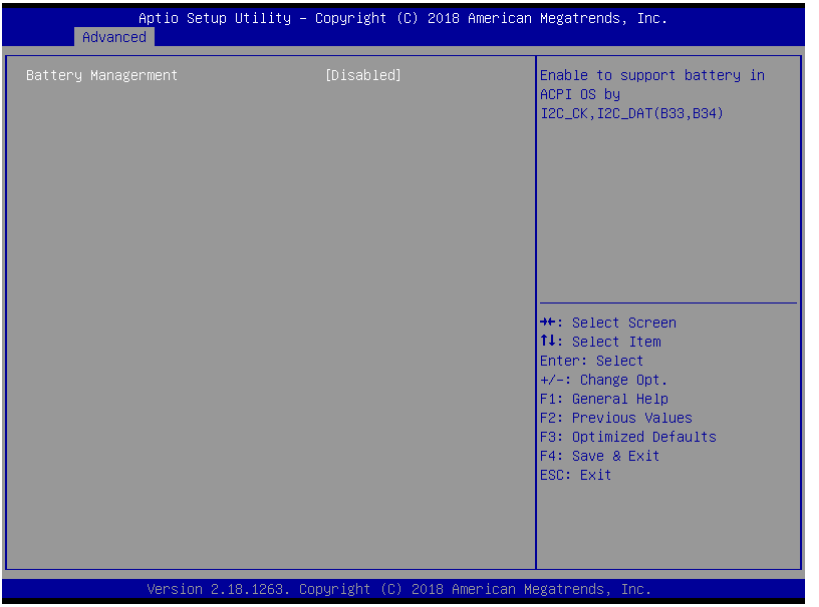
3.4.4.3 Fan Mode Configuration: Auto Mode by PWM



Options Summary		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		
Monitor Thermal	Thermal Source 1(T1)	Optimal Default, Failsafe Default
	Thermal Source 2(T2)	
Select monitor thermal source		
Temperature of	30	Optimal Default, Failsafe Default
Temperature Of Start		
Temperature Of Off	20	Optimal Default, Failsafe Default
Temperature Of Off		

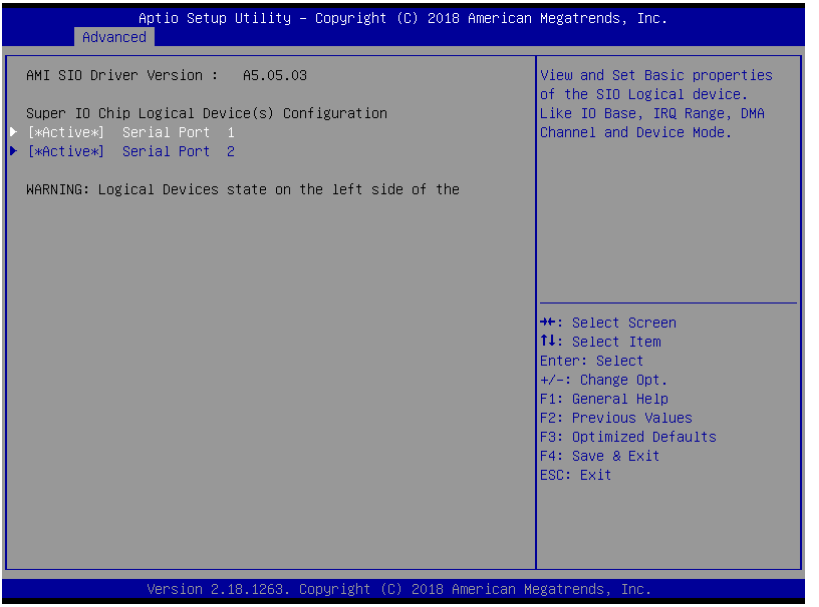
Options Summary		
Start PWM	40	Optimal Default, Failsafe Default
Start PWM		
Slope (PWM)	0 (PWM)	
	1 (PWM)	Optimal Default, Failsafe Default
	2 (PWM)	
	4 (PWM)	
	8 (PWM)	
	16 (PWM)	
	32 (PWM)	
	64 (PWM)	
Slope (PWM)		

3.4.5 Advanced: On-Module FEATURES

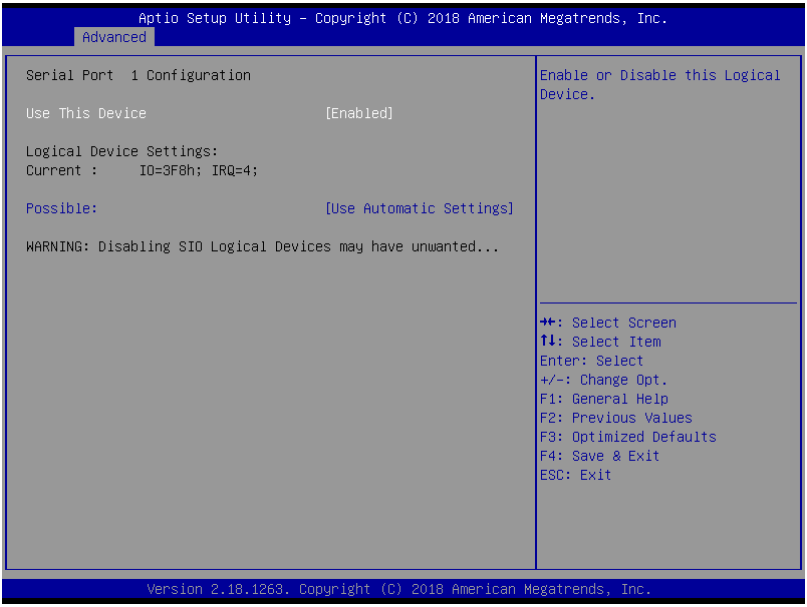


Options Summary		
Battery Management	Disable	Optimal Default, Failsafe Default
	One battery	
Enable to support battery in ACPI OS by I2C_CK, I2C_DAT(B33, B34)		

3.4.6 Advanced: SIO Configuration

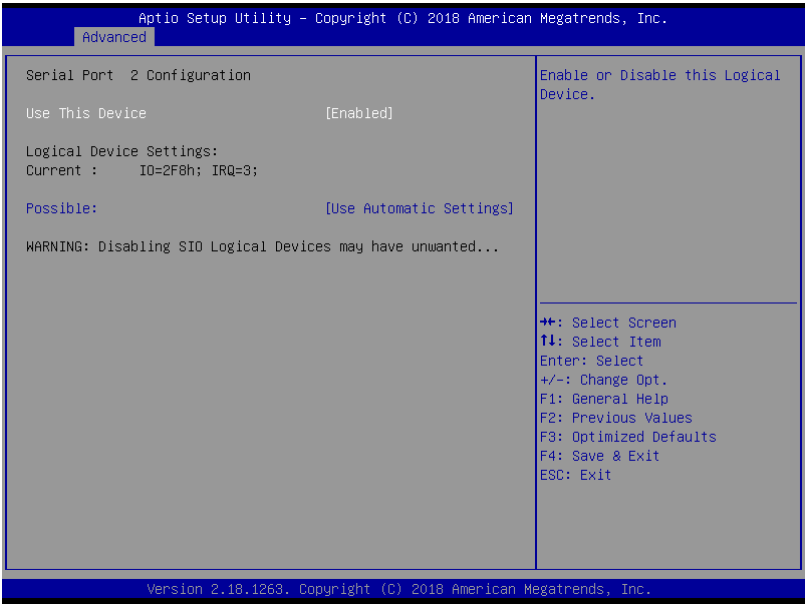


3.4.6.1 SIO Configuration: Serial Port 1 Configuration



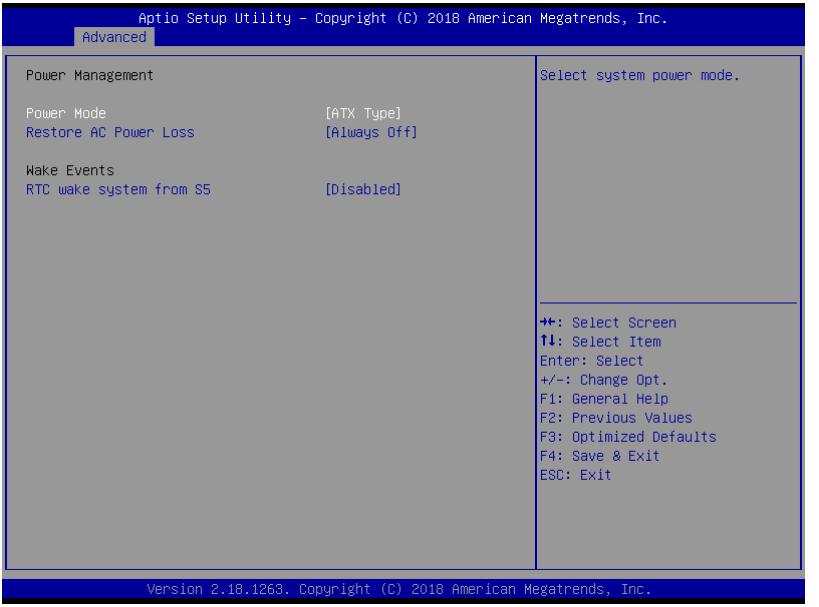
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.6.2 SIO Configuration: Serial Port 2 Configuration



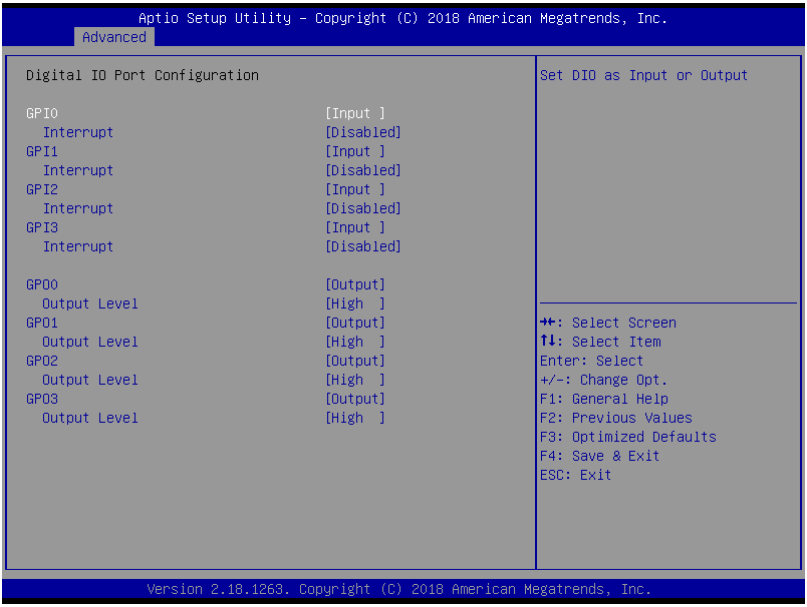
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3; DMA;	
	IO=2D8; IRQ=10; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.7 Advanced: Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time : System will wake on the hr :: min :: sec Specified Dynamic Time: System will wake on the current time + Increase minutes(s).		

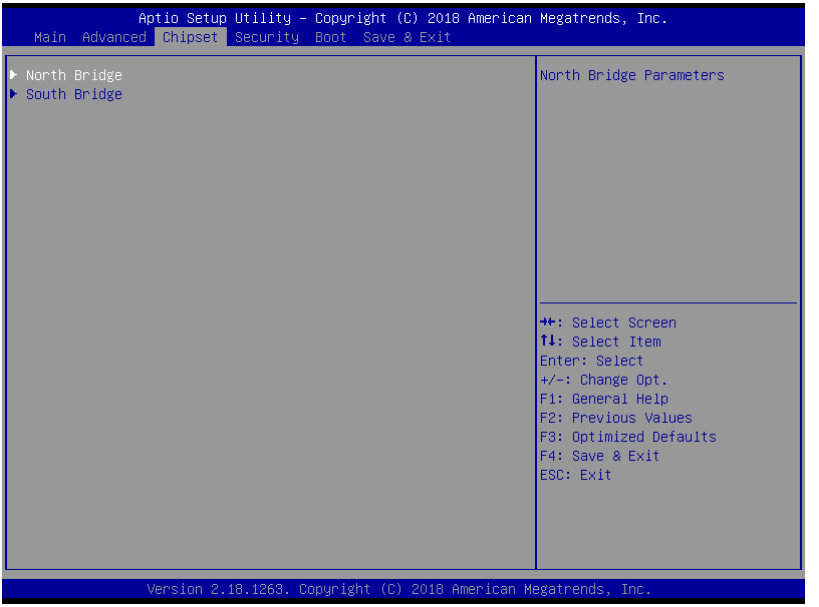
3.4.8 Advanced: Digital IO Port Configuration



Options Summary		
GPI*	Output	
	Input	
Set DIO as Input or Output		
Interrupt	Disable	Optimal Default, Failsafe Default
	Enable	
Enable interrupt function with low pulse mode. This triggered pulse needs more than the 10ms.		
GPO*	Output	
	Input	
Set DIO as Input or Output		

Options Summary		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

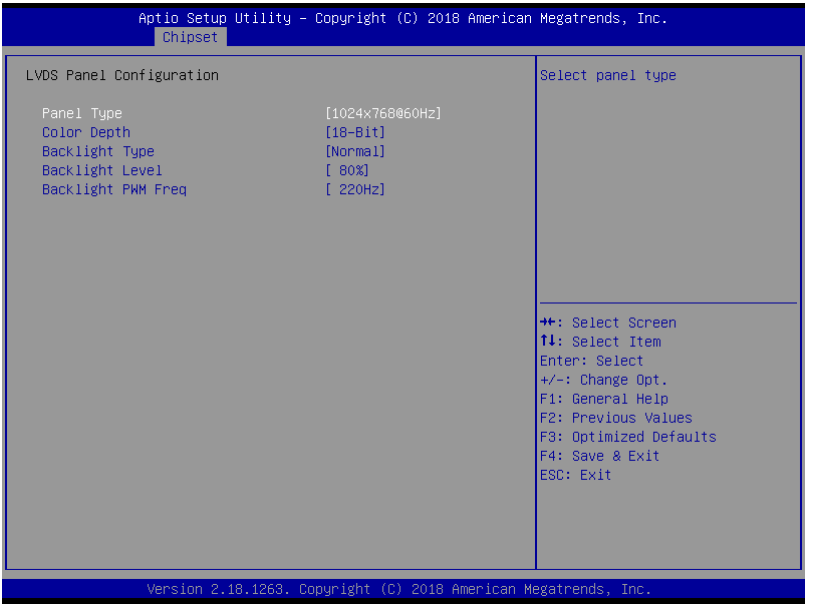
3.5 Setup submenu: Chipset



3.5.1 Chipset: North Bridge

Options Summary		
Total Memory	2048 MB (LPDDR4)	
LVDS Panel Configuration	Configure LVDS panel parameters.	

3.5.1.1 North Bridge: LVDS Panel Configuration



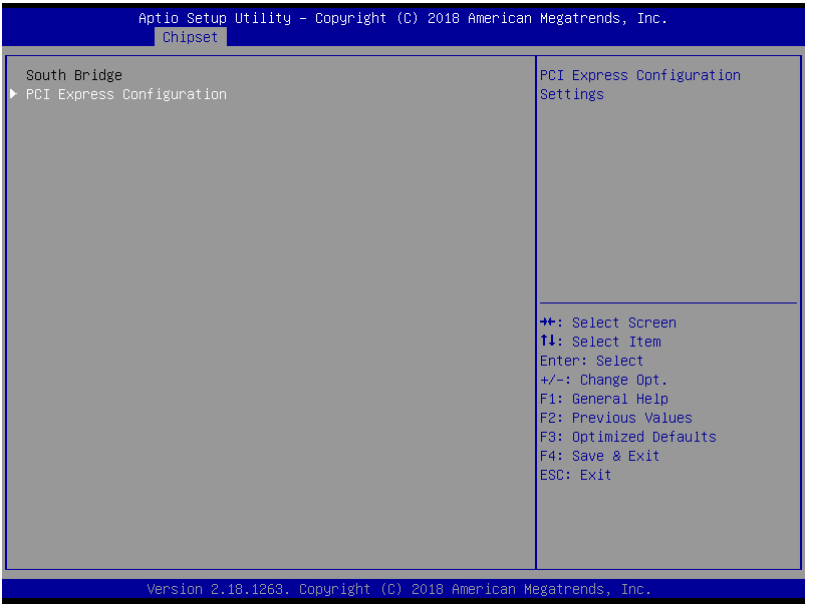
Options Summary		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x800@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	

Options Summary		
Panel Type	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@,60Hz	
Select panel type.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		

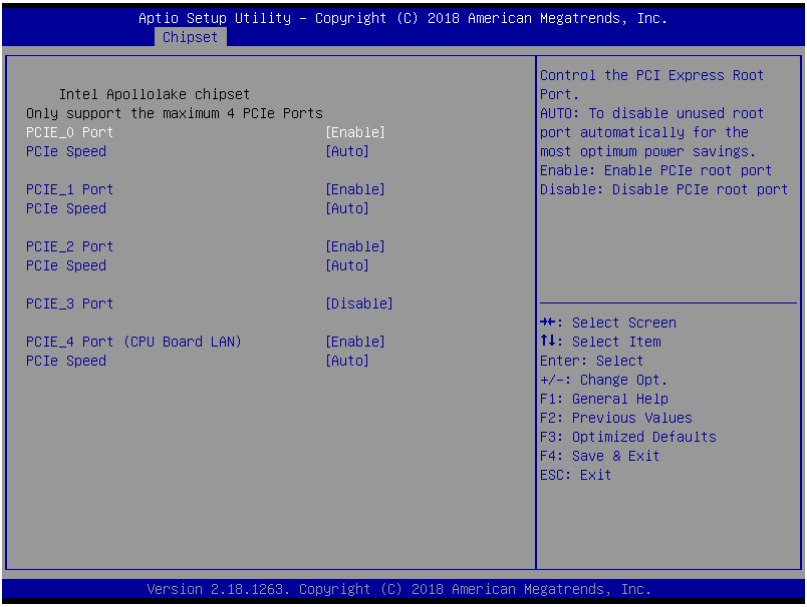
Table continues on Next Page

Options Summary		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.5.2 Chipset: South Bridge

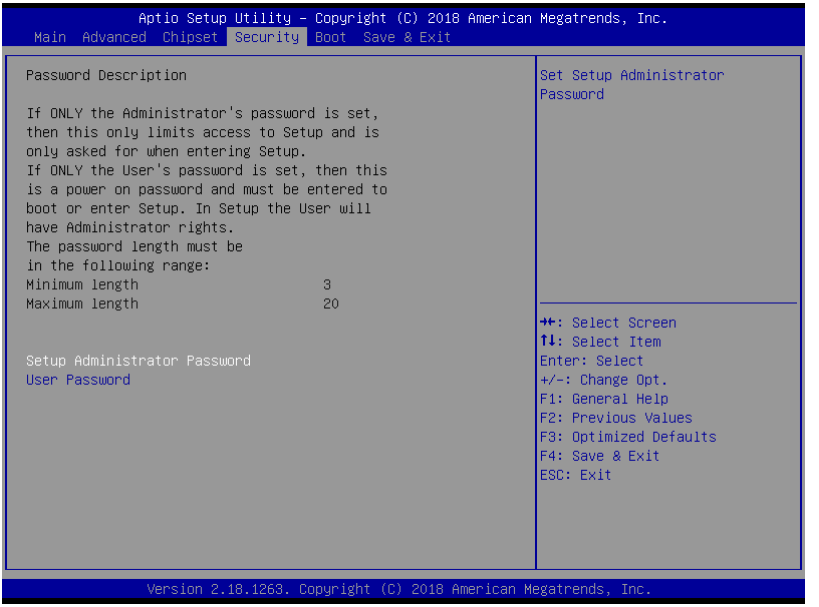


3.5.2.1 South Bridge: PCI Express Configuration



Options Summary		
PCIE_* Port	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port. AUTO : To disable unused root port automatically for the most optimum power savings. Enable : Enable PCIe root port. Disable : Disable PCIe root port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe speed.		

3.6 Setup submenu: Security



Change User/Administrator Password

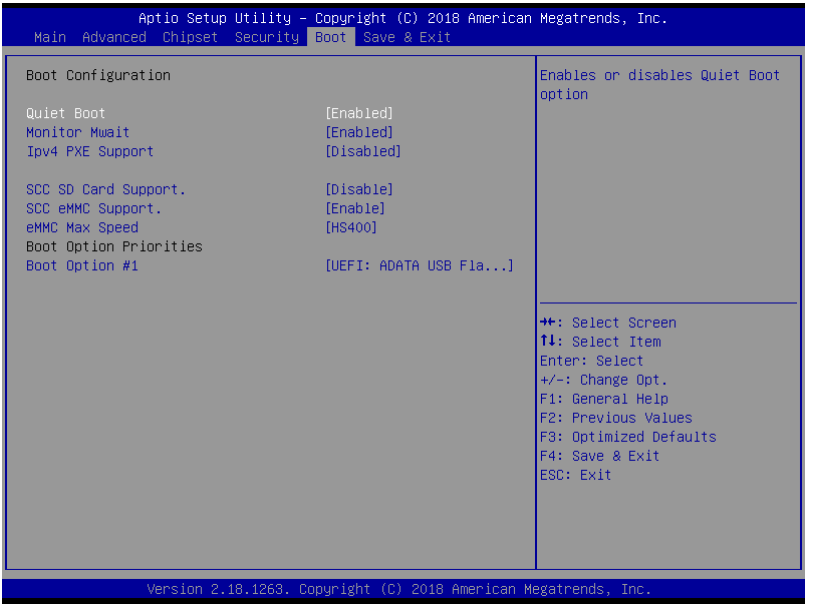
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

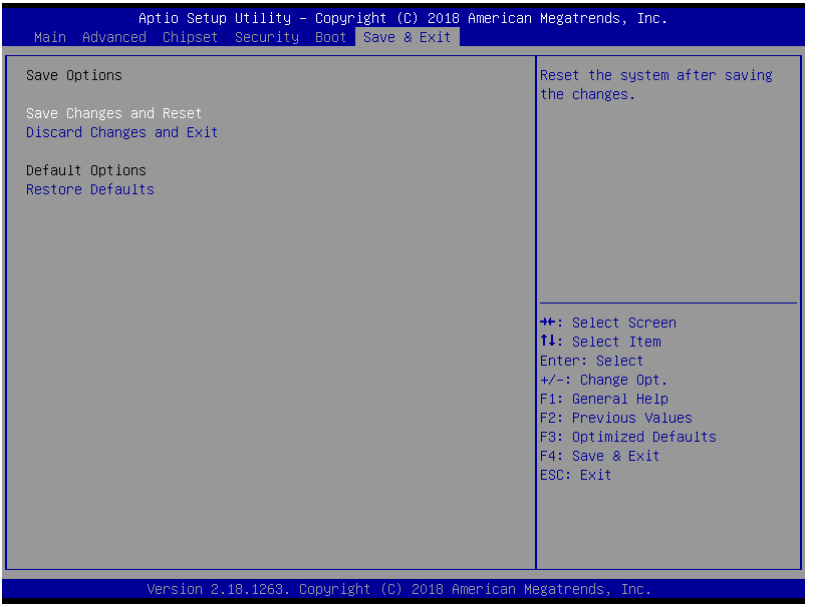
3.7 Setup submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 Boot Support. If disabled IPV4 PXE boot option will not be created.		

Options Summary		
SCC SD Card Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
SD card support requires HW change. Contact your AAEON Tech support or Contact your AAEON Support for detail.		
SCC eMMC Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable eMMC Support.		
eMMC Max Speed	HS400	Optimal Default, Failsafe Default
	HS200	
	DDR50	
Select the eMMC max Speed allowed.		
Boot Option #1	UEFI : ADATA USB Flash Drive 1100, Partition 1	Optimal Default, Failsafe Default
	Disabled	
Sets the system boot order.		

3.8 Setup submenu: Save & Exit



Save Change and Reset

Reset the system after saving the changes.

Discard Changes and Exit

Exit system setup without saving any changes.

Restore Defaults

Restore / Load Default values for all the setup options.

Chapter 4

Drivers Installation

4.1 Driver Download and Installation

Drivers for the NanoCOM-APL can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/com-express-modules-nanocom-apl

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step1 – Chipset** followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step2 - VGA** folder.
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Open the **Step3 - LAN** folder followed by **PROWinx64_20_3.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Step4 - Audio** folder followed by **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install TXE Drivers

1. Open the **Step5 - TXE** folder followed by **Setup TXE.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Serial I/O Drivers

1. Open the **Step6 – Serial IO** folder.
2. Follow the instructions in **README.txt** to setup and verify installation.

Step 7 – Install CSI Camera Drivers (Optional)

1. Open the **Step7 – CSI Camera (Optional)** folder followed by the folder for the drivers you want to install.
2. Follow the instructions in the **.inf** files to install drivers.

Step 8 – Install GPIO Interrupt Drivers

1. Open the **Step8 – GPIO_Interrupt** folder
2. Follow the instructions in the **ACPI Driver Test SOP** to setup and verify installation of drivers.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte    EcBRAMIndex    //This parameter is represented from Note1
#define byte    EcBRAMData    //This parameter is represented from Note2
#define byte    BRAMLDNReg    //This parameter is represented from Note3
#define byte    BRAMFnDataReg    //This parameter is represented from Note4
#define    void    EcBRAMWriteByte(byte Offset, byte Value);
#define    byte    EcBRAMReadByte(byte Offset);
#define    void    IOWriteByte(byte Offset, byte Value);
#define    byte    IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte    TimerReg    //This parameter is represented from Note5
#define byte    TimerVal    // This parameter is represented from Note10
#define byte    UnitReg    //This parameter is represented from Note6
#define byte    UnitBit    //This parameter is represented from Note7
#define byte    UnitVal    //This parameter is represented from Note11
#define byte    RSTReg    //This parameter is represented from Note8
#define byte    RSTBit    //This parameter is represented from Note9
#define byte    RSTVal    //This parameter is represented from Note12
*******************************************************************************
```

```
*********************************************************************************
VOID  Main(){
      // Procedure : AaeonWDTConfig
      // (byte)Timer : Time of WDT timer.(0x00~0xFF)
      // (boolean)Unit : Select time unit(0: second, 1: minute).
      AaeonWDTConfig();

      // Procedure : AaeonWDTEnable
       // This procudure will enable the WDT counting.
      AaeonWDTEnable();
}
*********************************************************************************
```

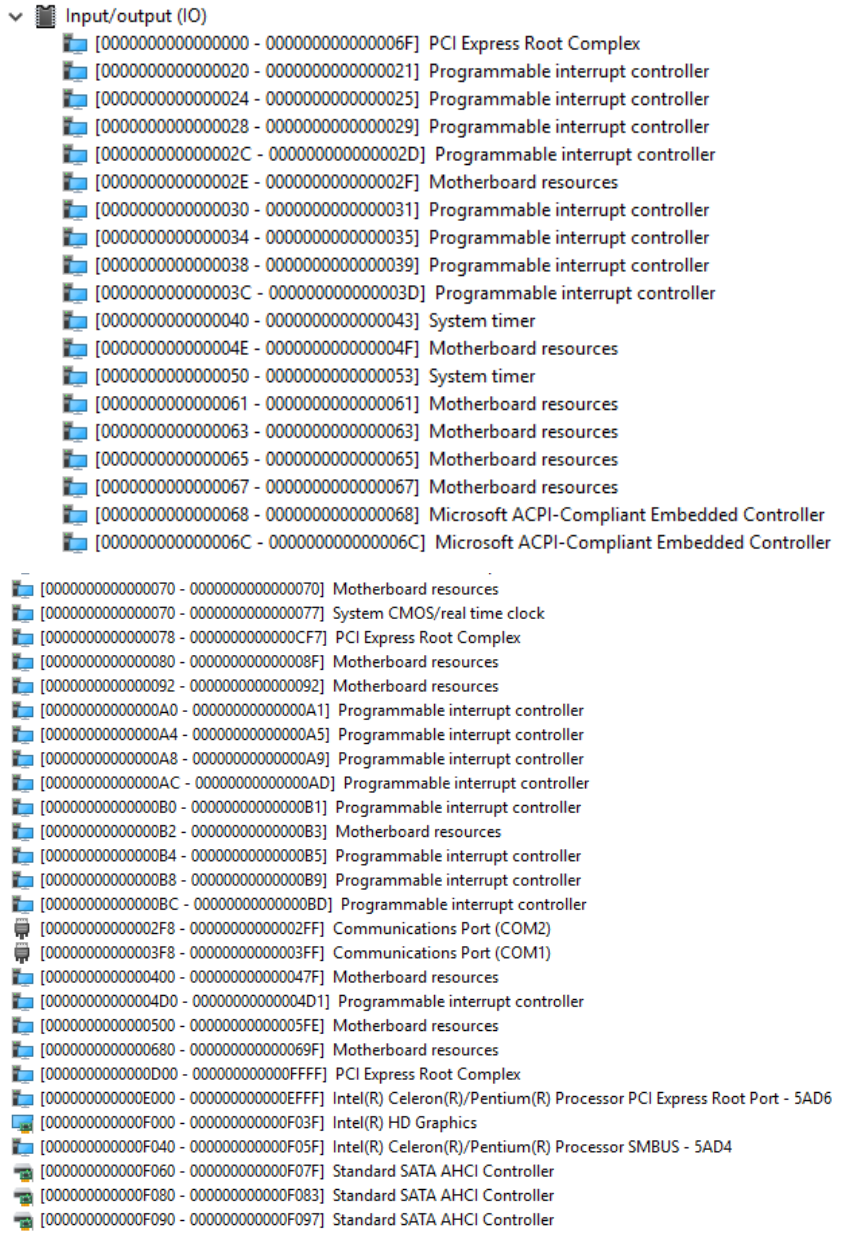
```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
         WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(0);
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID   WDTEnableDisable(byte Value){
        ECBRAMWriteByte(TimerReg , Value);
}

VOID   WDTParameterSetting(){
        Byte TempByte;

         // Watchdog Timer counter setting
         ECBRAMWriteByte(TimerReg , TimerVal);
        // WDT counting unit setting
         TempByte = ECBRAMReadByte(UnitReg);
         TempByte |= (UnitVal << UnitBit);
         ECBRAMWriteByte(UnitReg , TempByte);
         // WDT RST pulse width setting
         TempByte = ECBRAMReadByte(RSTReg);
         TempByte |= (RSTVal << RSTBit);
         ECBRAMWriteByte(RSTReg , TempByte);
}
*********************************************************************************
```

```
*********************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```

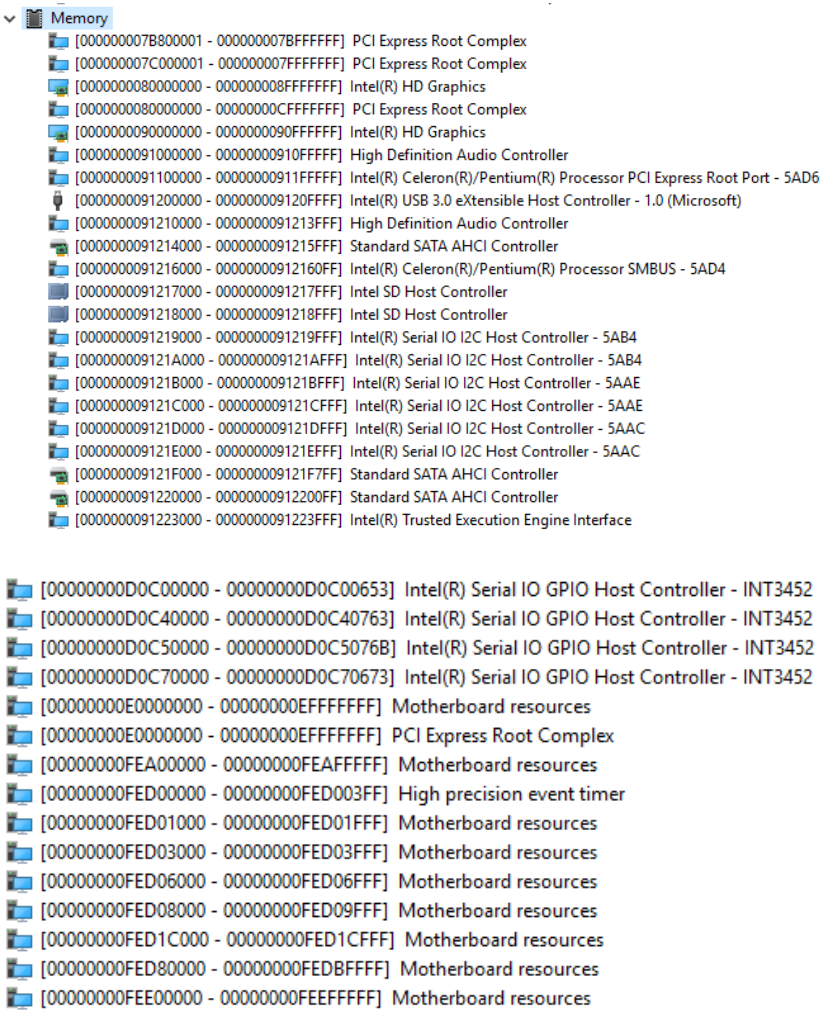
Appendix B

I/O Information

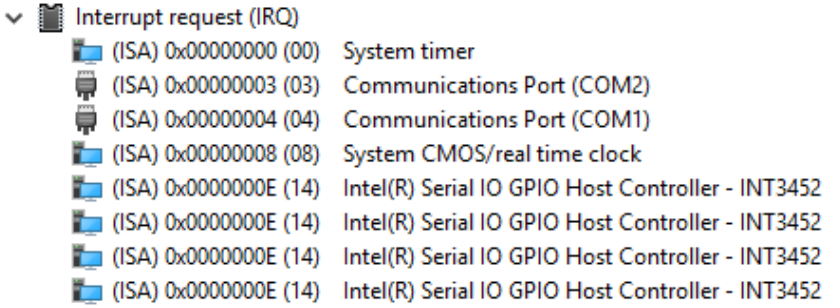
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



Appendix C

Programming Digital I/O

C.1 DI/O Programming

NanoCOM-APL utilizes AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can develop customized program to fit your application.

C.2 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
IO Direction Function and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
IO Vaule/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

C.3 Digital I/O Sample Program

```
**********************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnData0Reg   //This parameter is represented from Note4
#define byte   BRAMFnData1Reg   //This parameter is represented from Note5
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DIO0ToDIO7Reg   // This parameter is represented from Note6
#define byte   DIO0Bit   // This parameter is represented from Note7
#define byte   DIO1Bit   // This parameter is represented from Note8
#define byte   DIO2Bit   // This parameter is represented from Note9
#define byte   DIO3Bit   // This parameter is represented from Note10
#define byte   DIO4Bit   // This parameter is represented from Note11
#define byte   DIO5Bit   // This parameter is represented from Note12
#define byte   DIO6Bit   // This parameter is represented from Note13
#define byte   DIO7Bit   // This parameter is represented from Note14
#define byte   DIO0Val   // This parameter is represented from Note15
#define byte   DIO1Val   // This parameter is represented from Note16
#define byte   DIO2Val   // This parameter is represented from Note17
#define byte   DIO3Val   // This parameter is represented from Note18
#define byte   DIO4Val   // This parameter is represented from Note19
#define byte   DIO5Val   // This parameter is represented from Note20
#define byte   DIO6Val   // This parameter is represented from Note21
#define byte   DIO7Val   // This parameter is represented from Note22
**********************************************************************************
```

```
*****************************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //       Example, Read Digital I/O Pin 3 status
         // Output :
         //      InputStatus :
         //              0: Digital I/O Pin level is low
         //              1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //       Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*****************************************************************************************
```

```
*********************************************************************************
Boolean   AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID   AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
         ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*********************************************************************************
```

```
*********************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);              //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, FnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);              //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return          IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```