# ICS-6270

Industrial DIN Rail Network Appliance

User's Manual 6th Ed

## Copyright Notice

## Acknowledgement

## Packing List

Before setting up your product, please make sure the following items have been shipped:

| Item | Quantity |
|---|---|
| ICS-6270 | 1 |
| DIN Rail Kit | 1 |
| SATA Cable | 1 |
| SATA Power Cable | 1 |
| 2 Pin Phoenix Contact Connector (Male) | 1 |

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

## Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

## FCC Statement


This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

*Caution:*

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

*Attention:*

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.*
*Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

# 产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

| 部件名称 | 有毒有害物质或元素 | | | | | |
|---|---|---|---|---|---|---|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| 印刷电路板及其电子组件 | × | ○ | ○ | ○ | ○ | ○ |
| 外部信号连接器及线材 | × | ○ | ○ | ○ | ○ | ○ |
| 外壳 | ○ | ○ | ○ | ○ | ○ | ○ |
| 中央处理器与内存 | × | ○ | ○ | ○ | ○ | ○ |
| 硬盘 | × | ○ | ○ | ○ | ○ | ○ |
| 液晶模块 | × | ○ | ○ | ○ | ○ | ○ |
| 光驱 | × | ○ | ○ | ○ | ○ | ○ |
| 触控模块 | × | ○ | ○ | ○ | ○ | ○ |
| 电源 | × | ○ | ○ | ○ | ○ | ○ |
| 电池 | × | ○ | ○ | ○ | ○ | ○ |

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

## China RoHS Requirement (EN)

### Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

| Component Name | Hazardous or Toxic Materials or Elements | | | | | |
|---|---|---|---|---|---|---|
| | Lead (Pb) | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (Cr(VI)) | Polybrominated biphenyls (PBBs) | Polybrominated diphenyl ethers (PBDEs) |
| PCB and Components | X | O | O | O | O | O |
| Wires & Connectors for Ext.Connections | X | O | O | O | O | O |
| Chassis | O | O | O | O | O | O |
| CPU & RAM | X | O | O | O | O | O |
| HDD Drive | X | O | O | O | O | O |
| LCD Module | X | O | O | O | O | O |
| Optical Drive | X | O | O | O | O | O |
| Touch Control Module | X | O | O | O | O | O |
| PSU | X | O | O | O | O | O |
| Battery | X | O | O | O | O | O |

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

# Table of Contents

# Chapter 1

Product Specifications

## 1.1 Specifications

| System | |
|---|---|
| Form Factor | DIN Rail/Desktop |
| Processor | Intel® Celeron® Processor N3350 SoC |
| System Memory | DDR3L 1866MHz Single-Channel SODIMM x 1 (Max. 8GB, up to 1600MHz) |
| Chipset | — |
| Ethernet | Intel® i211 GbE x 6 |
| Bypass | Supports up to 2 pairs |
| BIOS | AMI SPI Flash BIOS |
| SATA | SATA III x 1 |
| CFast/mSATA | CFast™ Socket x 1 (colay mSATA) |
| Expansion Interface | Mini Card x 1 with SIM |
| USB | USB 3.0 x 2 |
| Serial Port | COM Port x 2 for RS-232/422/485 |
| Watchdog Timer | 1~255 steps by software programmable |
| RTC | Internal RTC |
| System Fan | Fanless |
| Color | Dark Grey |
| Power Supply | 2-Pin Terminal Block |
| Dimension | 4.96" x 2.93" x 5.74" (126mm x 74.5mm x 146mm) |
| Power Requirement | +9 ~ 36V via 2-Pin Terminal Block |
| MTBF (Hours) | 101,292 |

**Note**: To avoid random non-booting issue caused by the incompatibility of Intel® Pentium® Processor N Series with certain unstable 1866MHz memories, memory with frequency greater than 1600MHz will automatically fix to 1600MHz, while memory that runs at a speed lower than 1600MHz will maintain its original speed.

| Display | |
|---|---|
| **Chipset** | Intel® HD Graphics 500 |
| **Interface** | VGA x 1 |

| I/O | |
|---|---|
| **Front I/O Panel** | RJ-45 GbE x 6,<br>COM Port x 2 for RS-232/422/485<br>VGA x 1<br>USB 3.0 x 2<br>Software Programmable Button x 1<br>Power LED x 1<br>HDD LED x 1<br>Status LED x 1<br>Bypass LED x 2 |
| **Rear I/O Panel** | DIN Rail/Wallmount Lock |
| **Top Panel** | +9~36VDC 2-Pin Terminal Block x 1 |

## Environmental Parameters and Dimensions

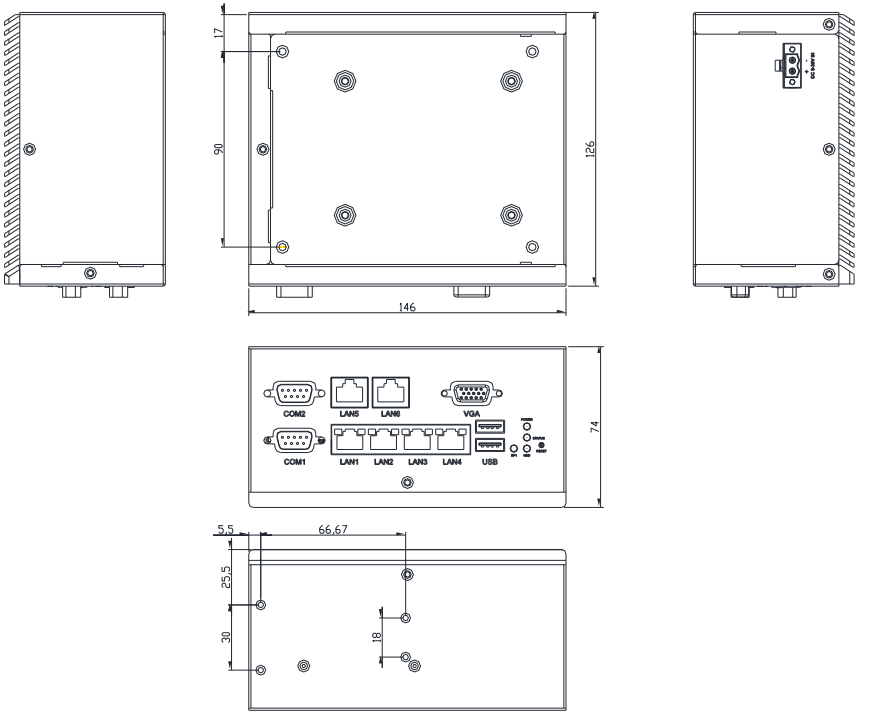
| | |
|---|---|
| **Operating Temperature** | -40°F ~ 156°F (-40°C ~ 75°C) |
| **Storage Temperature** | -40°F ~ 185°F (-40°C ~ 85°C) |
| **Operating Humidity** | 10% ~ 80% relative humidity, non-condensing |
| **Storage Humidity** | 10% ~ 80% @40°C; non-condensing |
| **Vibration** | 0.5 Grms/ 5 ~ 500Hz/ operation (SSD) |
| | 1.5 Grms/ 5 ~ 500Hz / non-operation |
| **Shock** | 10 G peak acceleration (11 m sec. duration), operation |
| | 20 G peak acceleration (11 m sec. duration), non-operation |

# Chapter 2

Hardware Information

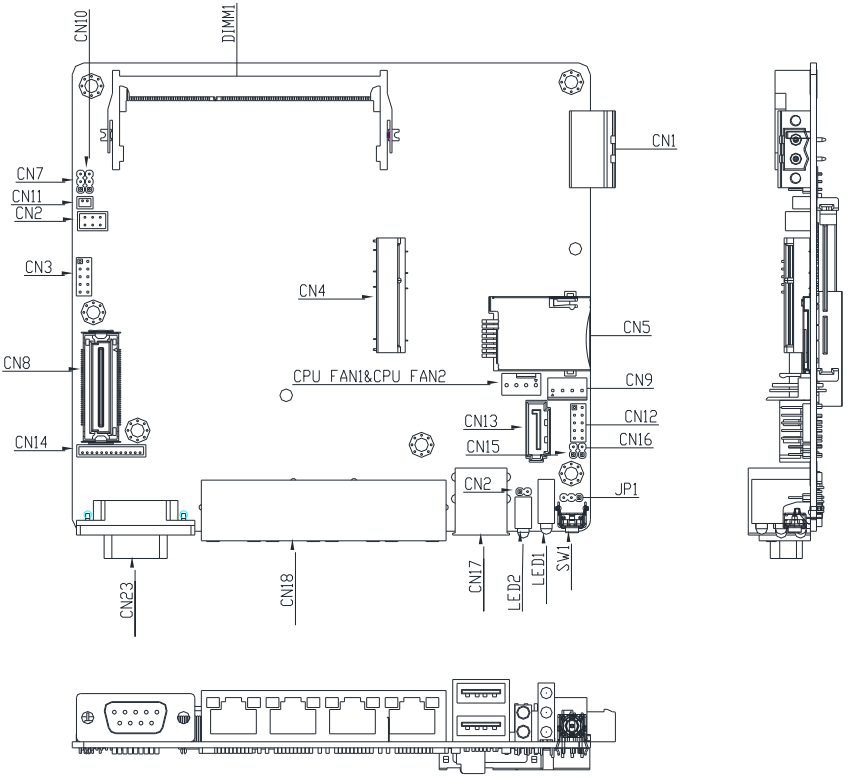
## 2.1 Dimensions

### System

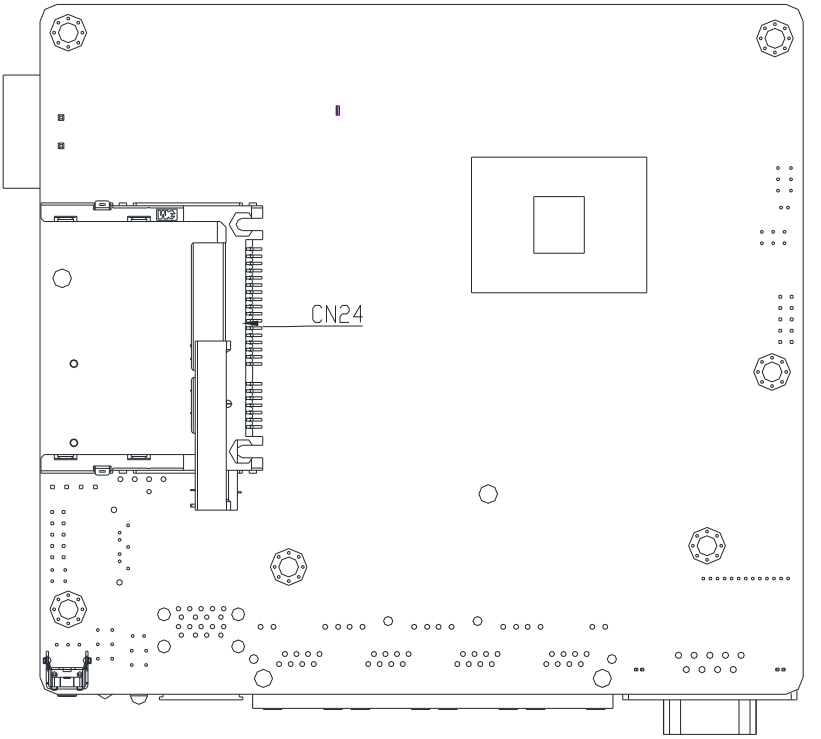


## Board

### Component Side

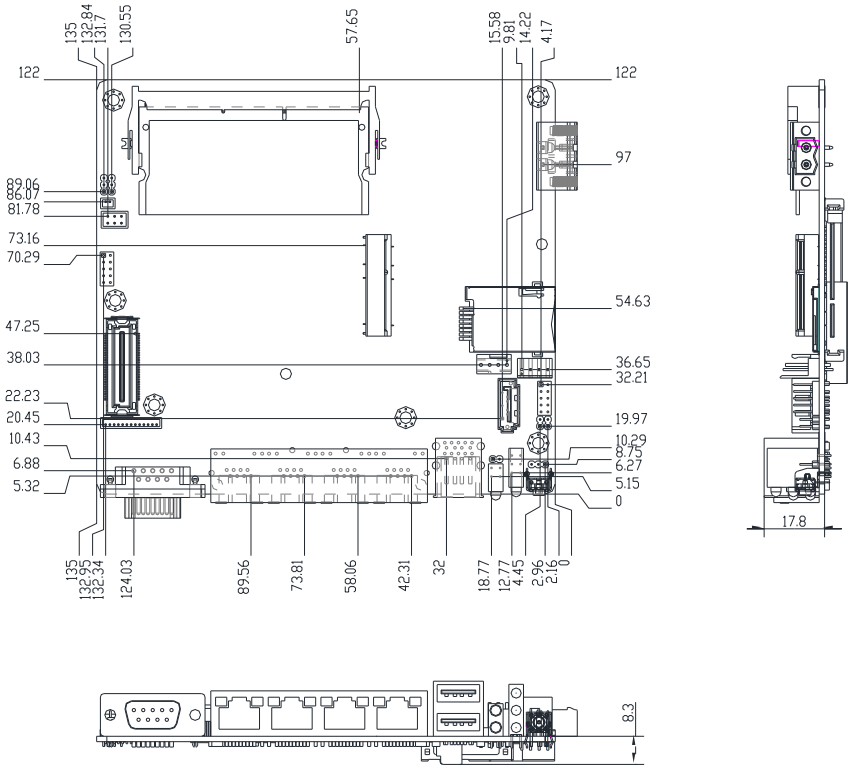


Solder Side

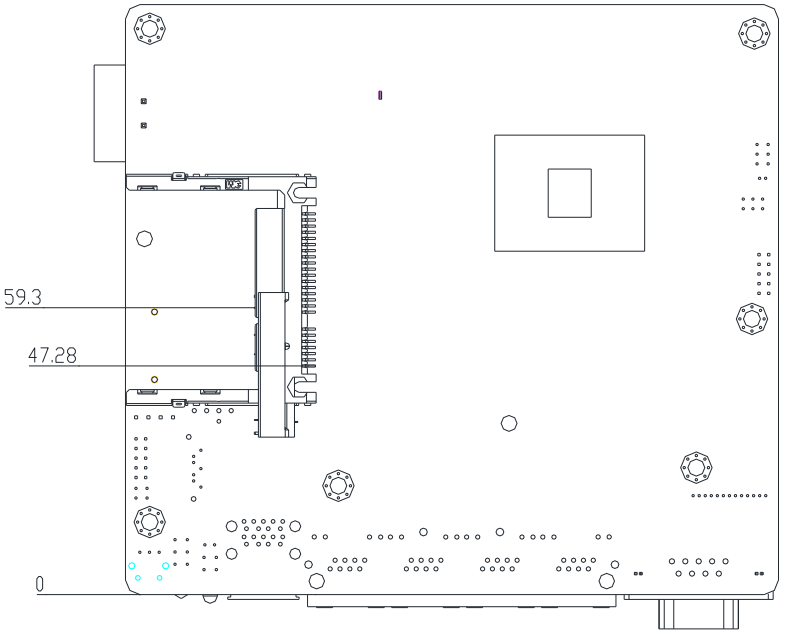


## 2.2 Jumpers and Connectors

### Component Side



Solder Side

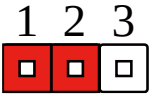


## 2.3 List of Jumpers

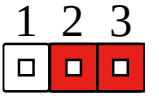
Please refer to the table below for all of the board's jumpers that you can configure for your application.

| Label | Function |
|---|---|
| JP1 | Auto PWRBTN Selection |
| CN7 | CMOS Setting Selection |

### 2.3.1 CMOS Setting Selection (CN1)

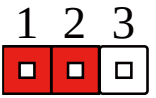



Normal (**Default**)

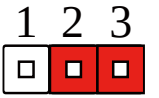



Clear CMOS

### 2.3.2 Auto PWRBTN Selection (JP1)




Don't use Auto PWRBTN




Use Auto PWRBTN

## 2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

| Label | Function |
|---|---|
| DIMM1 | DDR3L SODIMM Socket |
| CPU_FAN1 | 4P Smart Fan |
| CN2 | KB/MS |
| CN23 | COM Port for RS232/RS422/RS485 |
| CN13 | SATA Interface |
| CN9 | SATA Power |
| CN4 | Mini PCIe |
| CN24 | CFast Card |
| CN5 | SIM Card |
| CN15 | Reset |
| CN16 | Power Button |
| CN17 | Dual USB 3.0 Port |
| CN3 | Digital I/O |
| CN18 | LAN 1-4 |
| CN1 | DC-In |

### 2.4.1 Digital I/O (CN3)

This connector offers 4-pair of digital I/O functions and address is 801H. The pin definitions are illustrated below:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Digital- IN/OUT1 | 2 | Digital- IN/OUT2 |
| 3 | Digital- IN/OUT3 | 4 | Digital- IN/OUT4 |
| 5 | Digital- IN/OUT5 | 6 | Digital- IN/OUT6 |
| 7 | Digital- IN/OUT7 | 8 | Digital- IN/OUT8 |
| 9 | +5V | 10 | GND |

### 2.4.2 DC-In (CN1)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | POWER |

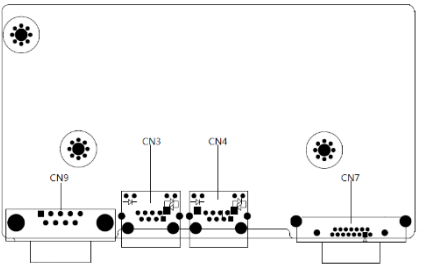
### 2.4.3 COM Port (CN23)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD/ RS422_TX-/ RS485_D- | 2 | RXD/RS422_TX+/ RS485_D+ |
| 3 | TXD/ RS422_RX+ | 4 | DTR/ RS422_RX- |
| 5 | GND | 6 | DSR |
| 7 | RTS | 8 | CTS |
| 9 | RI | | |

## 2.5 List of Connectors for T461 Type A

Please refer to the table below for all of the board's connectors that you can configure for your application.

| Label | Function |
|---|---|
| CN3 | GbE LAN |
| CN4 | GbE LAN |
| CN7 | VGA |
| CN9 | COM 2 for RS232/RS422/RS485 |

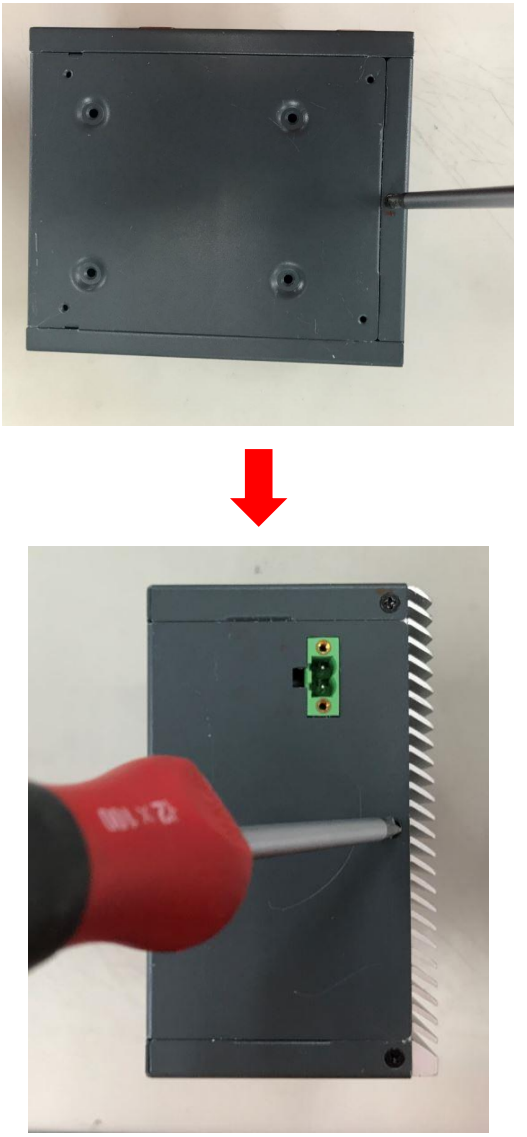



### 2.5.1 COM Port (CN9)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD/ RS422_TX-/ RS485_D- | 2 | RXD/RS422_TX+/ RS485_D+ |
| 3 | TXD/ RS422_RX+ | 4 | DTR/ RS422_RX- |
| 5 | GND | 6 | DSR |
| 7 | RTS | 8 | CTS |
| 9 | RI | | |

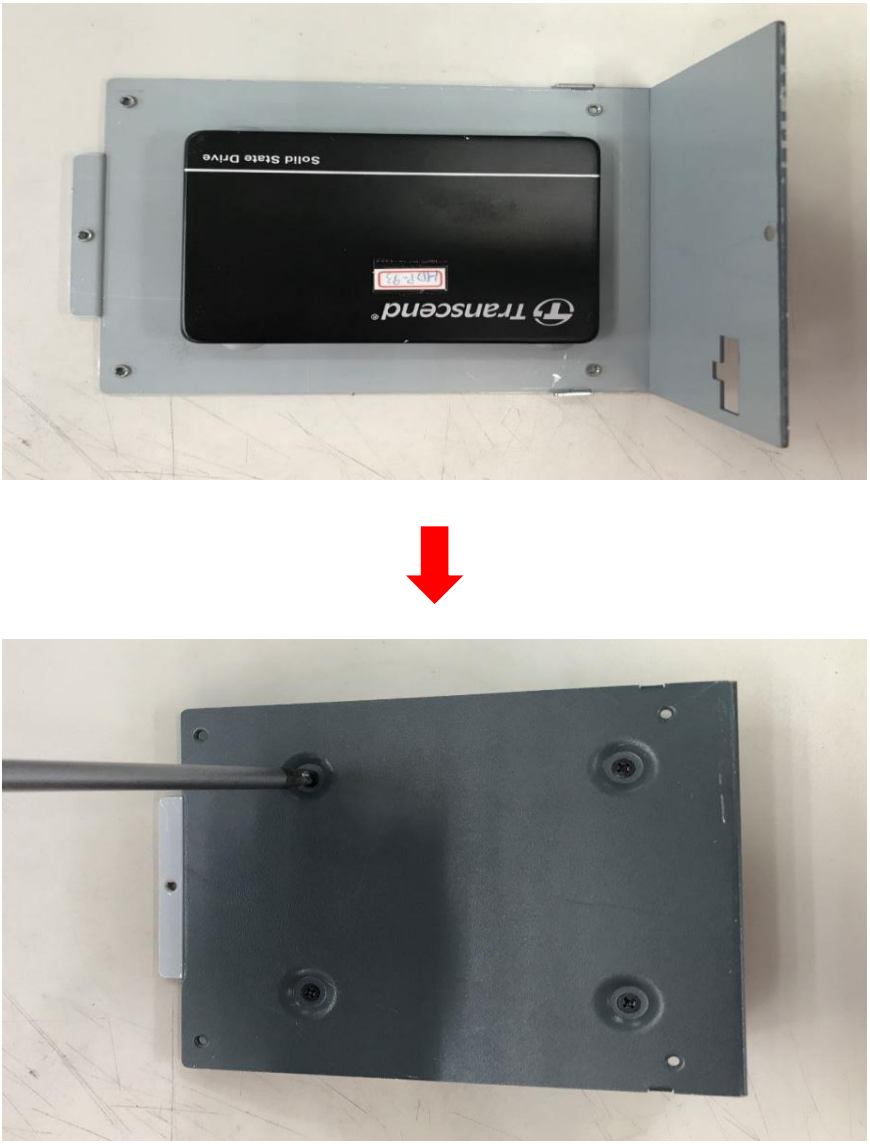
## 2.6 Hard Disk Drive Installation

1. Loosen the screw and remove the top case from the lower side.

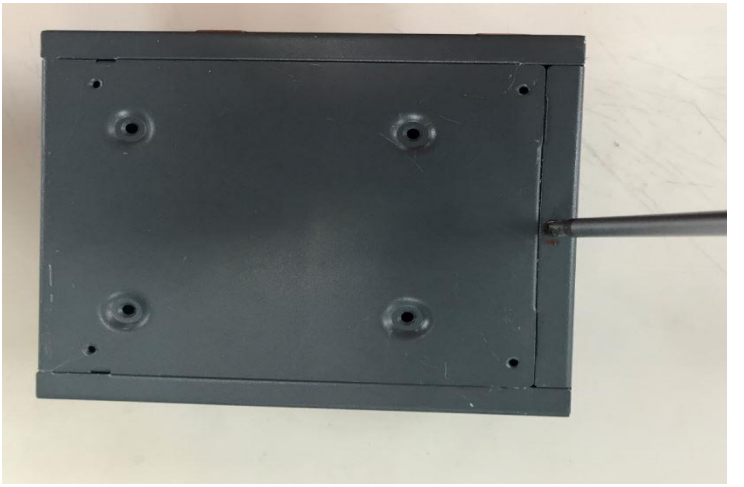


2. Place the SATA Cable and the Power cable onto the motherboard.

3. Put the SSD together and fasten tightly with screws.

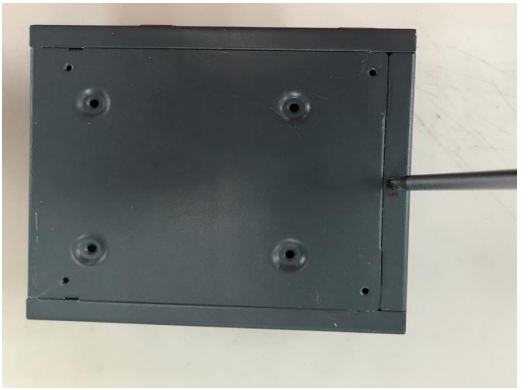


4. Put the lid back on and fasten the screws securely.



## 2.7 DIMM Sink Installation

1. Unscrew and remove the cover.

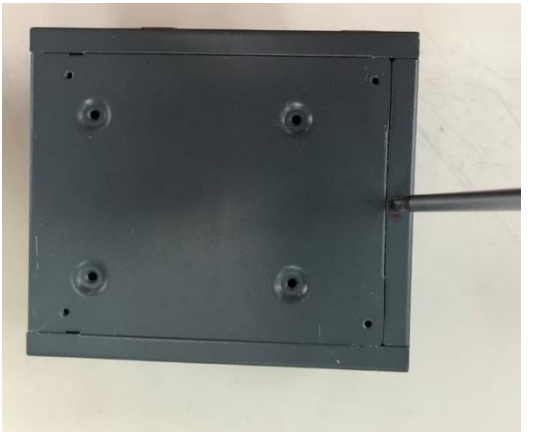


2. Place the DIMM onto the motherboard.

3. Glue the sink onto the pad.

4. Put the sink together and fasten them securely with screws.

5. . Put the lid back on and fasten the screws securely.



# Chapter 3

AMI BIOS Setup

## 3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The ICS-6270 CMOS memory has an integral lithium battery backup for data retention. You have to replace the battery when it finally runs down.

## 3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <Esc> immediately. This will allow you to enter Setup.

### Main

Basic information and set Date & Time.

### Advanced

Major feature configuration (e.g.: CPU, Super IO, Hardware Monitor, Digital I/O, etc.).

### Chipset

Configuration for Chipset features.

### Security

Set BIOS Administrator/User password.

### Boot

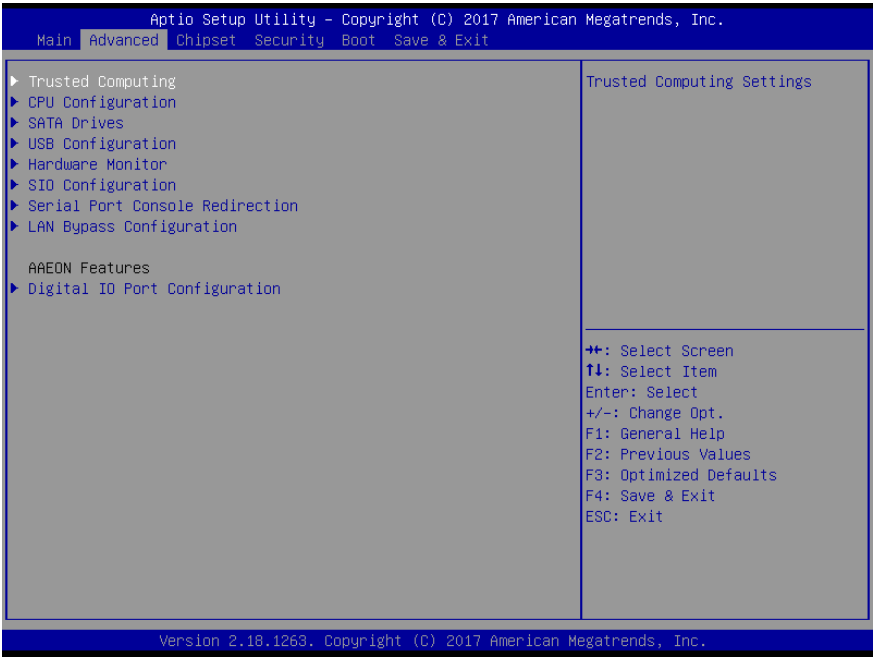
Adjust Boot configuration/priorities.

### Save& Exit

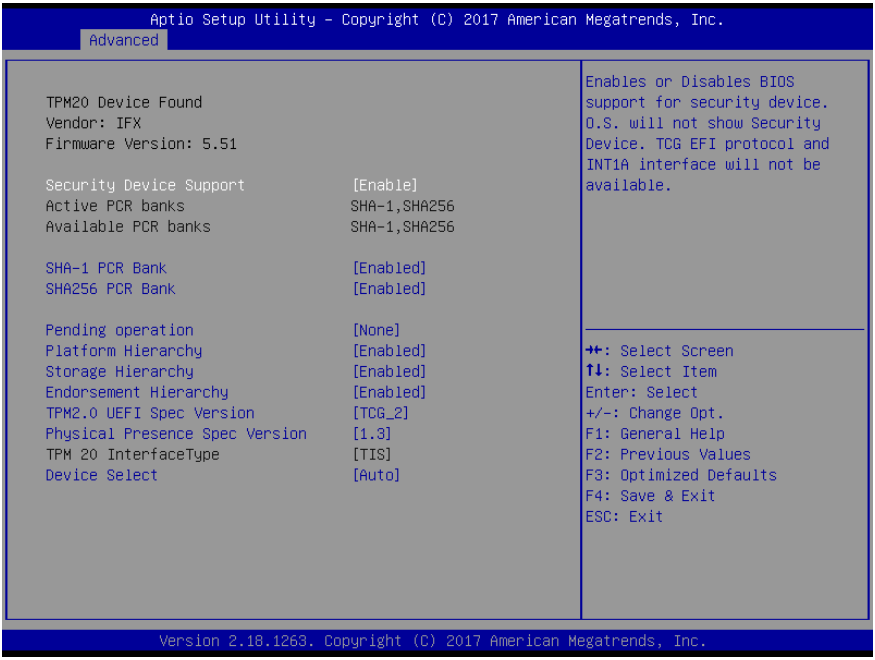
Save changes/restore defaults and exit system setup.

## 3.3 Setup Submenu: Main

## 3.4 Setup Submenu: Advanced



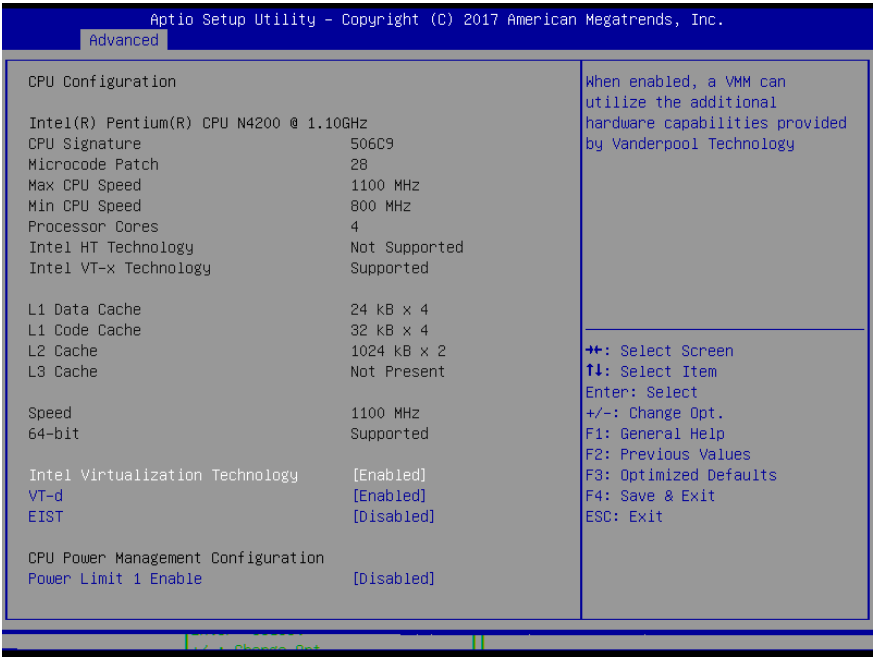
## 3.4.1 Trusted Computing




| Options Summary | |
|---|---|
| **Security Device Support** | Disabled |
| | **Enabled** |
| Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. | |
| **SHA-1 PCR Bank** | Disabled |
| | **Enabled** |
| Enable or Disable SHA-1 PCR Bank. | |
| **SHA256 PCR Bank** | Disabled |
| | **Enabled** |
| Enable or Disable SHA256 PCR Bank. | |
| **Pending operation** | **None** |
| | TPM Clear |
| Schedule an Operation for the Security Device.<br>**NOTE**: Your Computer will reboot during restart in order to change State of Security Device. | |

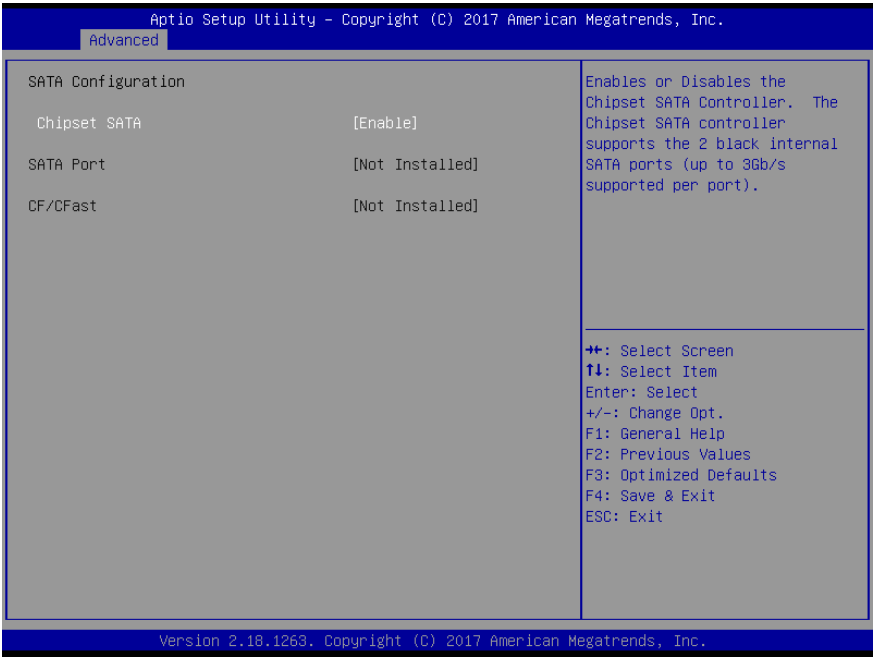
| Options Summary | |
|---|---|
| Platform Hierarchy | Disabled |
| | **Enabled** |
| Enable or Disable Platform Hierarchy. | |
| Storage Hierarchy | Disabled |
| | **Enabled** |
| Enable or Disable Storage Hierarchy. | |
| Endorsement Hierarchy | Disabled |
| | **Enabled** |
| Enable or Disable Endorsement Hierarchy. | |
| TPM2.0 UEFI Spec Version | TCG_1_2 |
| | **TCG_2** |
| Select the TCG2 Spec Version Support.<br>TCG_1_2: The Compatible mode for Win8/Win10.<br>TCG_2: Support new TCG2 protocol and event format for Win10 or later. | |
| Physical Presence Spec Version | 1.2 |
| | **1.3** |
| Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3. | |
| Device Select | TPM 1.2 |
| | TPM 2.0 |
| | **Auto** |
| TPM 1.2 will restrict support to TPM 1.2 devices.<br>TPM 2.0 will restrict support to TPM 2.0 devices.<br>Auto will support both with the default set to TPM 2.0 devices if not found.<br>TPM 1.2 devices will be enumerated. | |

## 3.4.2 CPU Configuration



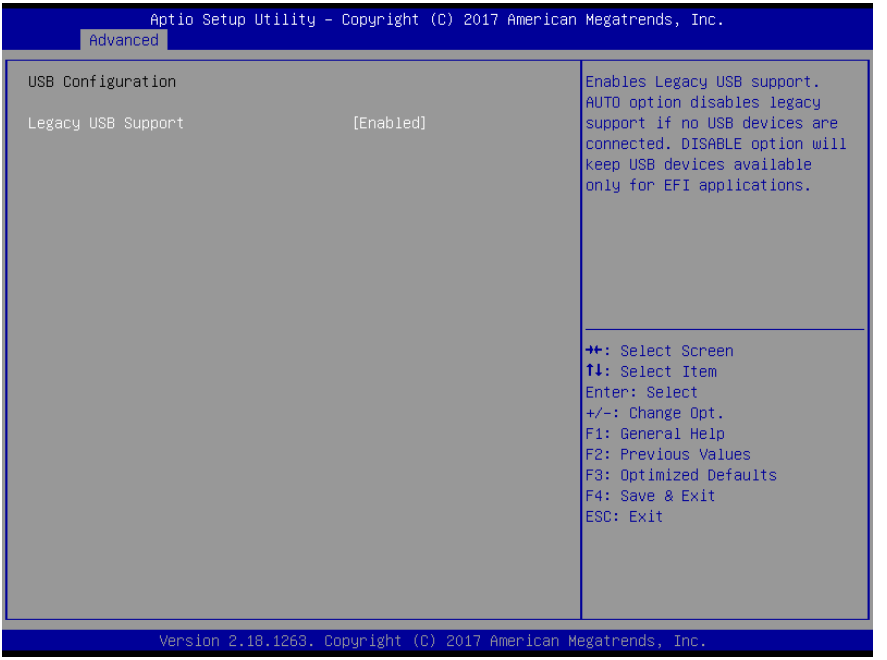

| Options Summary | |
|---|---|
| **Intel Virtualization Technology** | Disabled |
| | **Enabled** |
| When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. | |
| **VT-d** | Disabled |
| | **Enabled** |
| Enable/Disable CPU VT-d. | |
| **EIST** | **Disabled** |
| | Enabled |
| Enable/Disable Intel SpeedStep. | |
| **Power Limit 1 Enable** | **Disabled** |
| | Enabled |
| Enable/Disable Power Limit 1. | |

### 3.4.3 SATA Drives



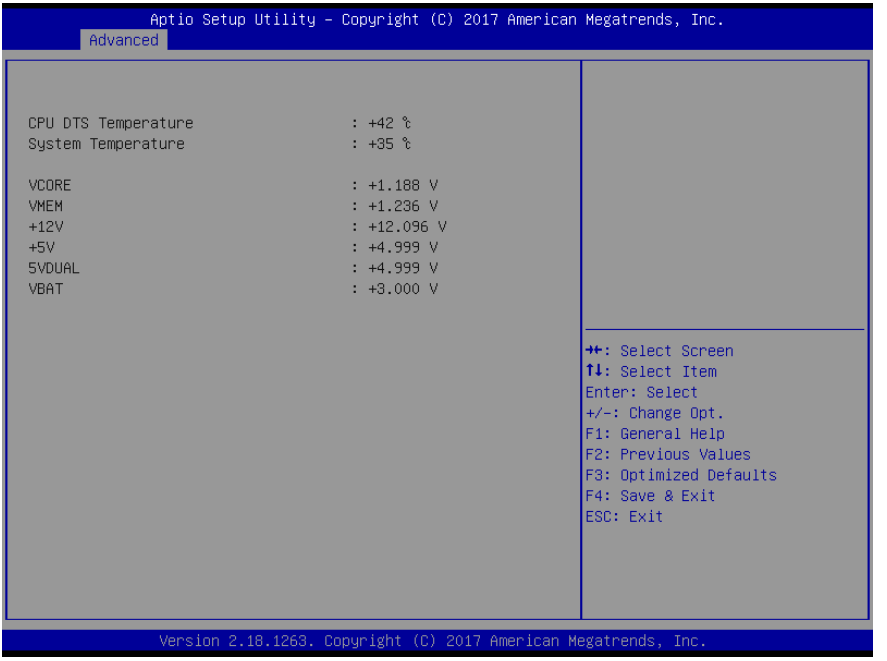

| Options Summary | |
|---|---|
| Chipset SATA | Disabled |
| | **Enabled** |
| Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port). | |

## 3.4.4 USB Configuration

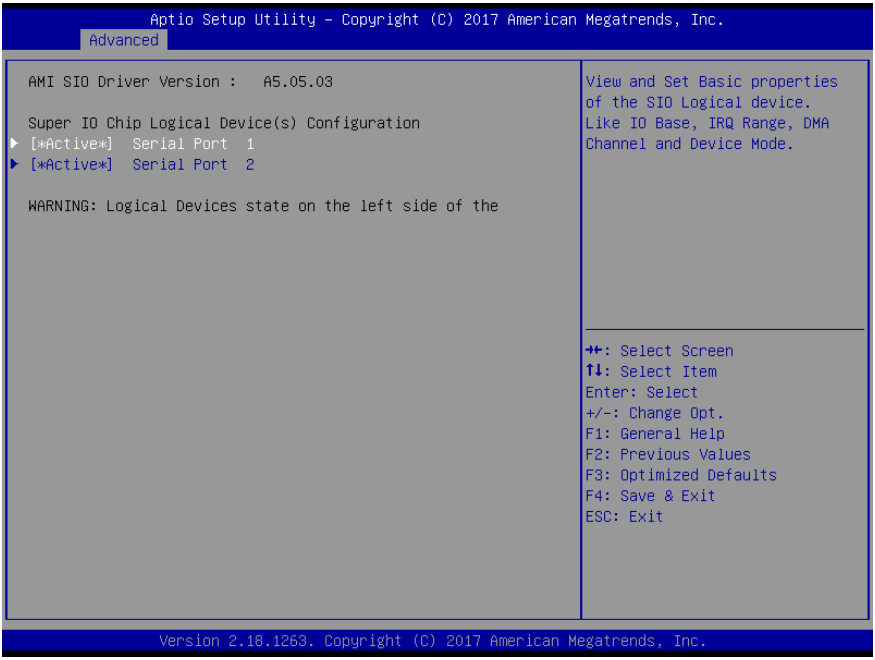



| Options Summary | |
|---|---|
| Legacy USB Support | Disabled |
| | **Enabled** |
| Enables Legacy USB support.<br>AUTO option disables legacy support if no USB devices are connected.<br>DISABLE option will keep USB devices available only for EFI applications. | |

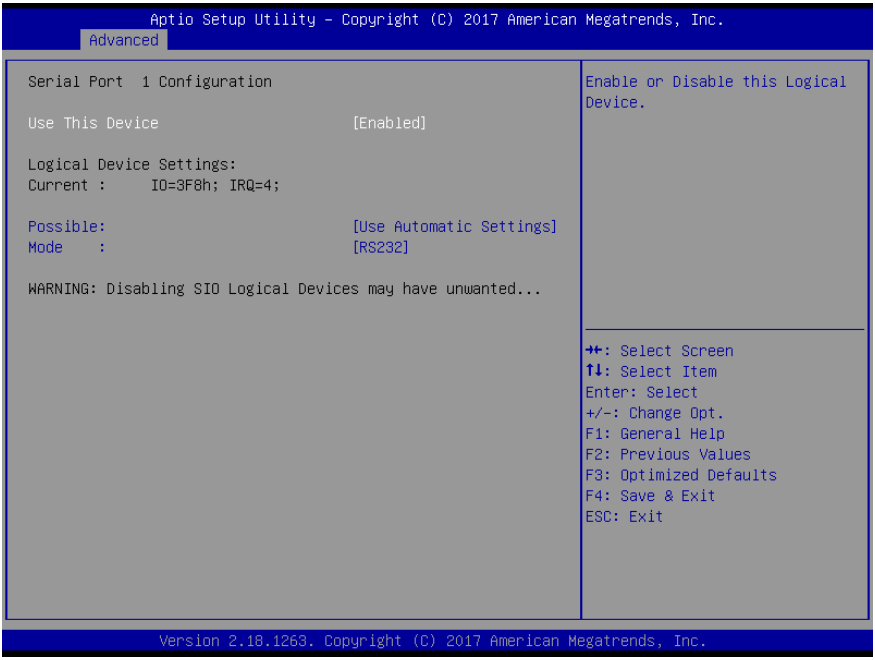
## 3.4.5 Hardware Monitor



## 3.4.6 SIO Configuration

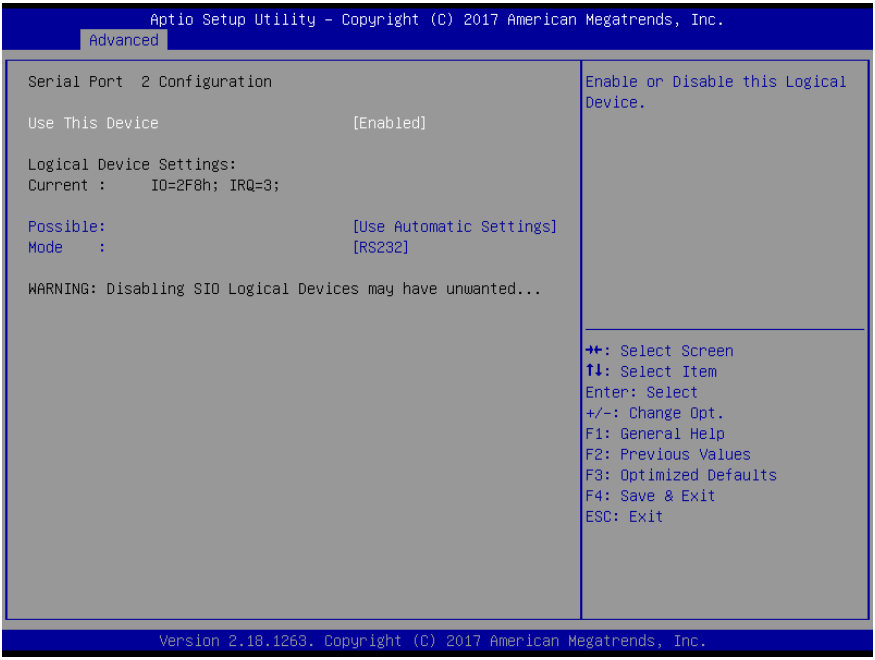


### 3.4.6.1 Serial Port 1 Configuration



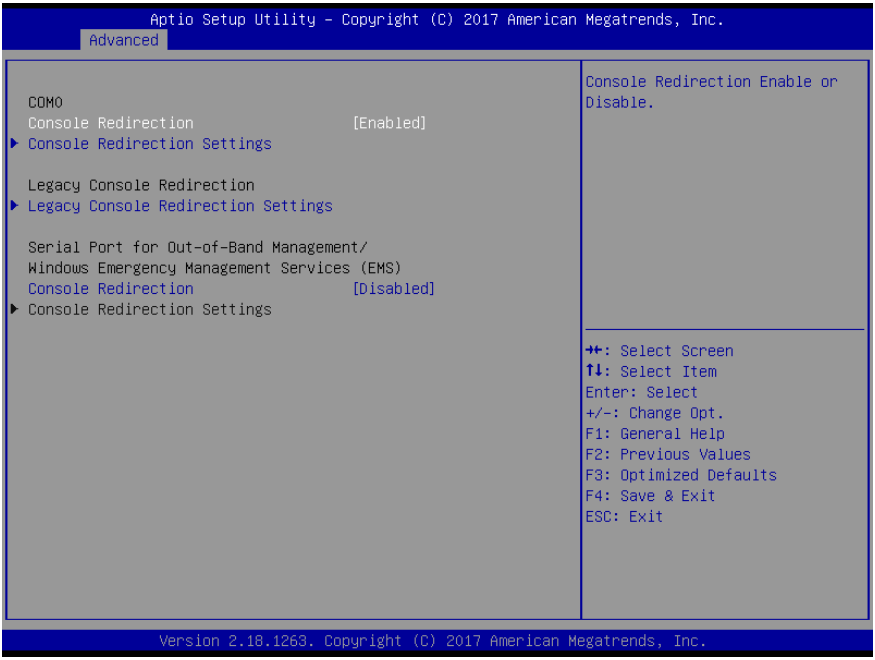

| Options Summary | |
|---|---|
| Use This Device | Disabled |
| | **Enabled** |
| Enable or Disable this Logical Device. | |
| Possible: | **Use Automatic Settings** |
| | IO=2F8h; IRQ=3; |
| | IO=3F8h; IRQ=4; |
| Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts. | |
| Mode: | **RS232** |
| | RS422 |
| | RS485 |
| UART RS232, 422, 485 selection. | |

### 3.4.6.2 Serial Port 2 Configuration



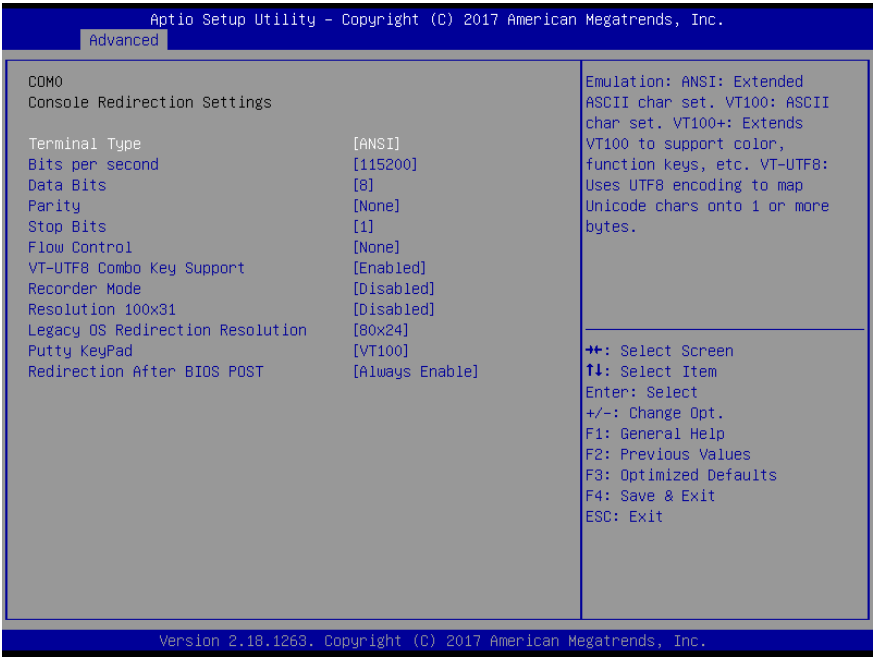

| Options Summary | |
|---|---|
| Use This Device | Disabled |
| | **Enabled** |
| Enable or Disable this Logical Device. | |
| Possible: | **Use Automatic Settings** |
| | IO=2F8h; IRQ=3; |
| | IO=3F8h; IRQ=4; |
| Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts. | |
| Mode: | **RS232** |
| | RS422 |
| | RS485 |
| UART RS232, 422, 485 selection | |

## 3.4.7 Serial Port Console Redirection




| Options Summary | |
|---|---|
| Console Redirection | Disabled |
| | Enabled |
| Console Redirection Enabled or Disabled. | |

### 3.4.7.1 Console Redirection Settings

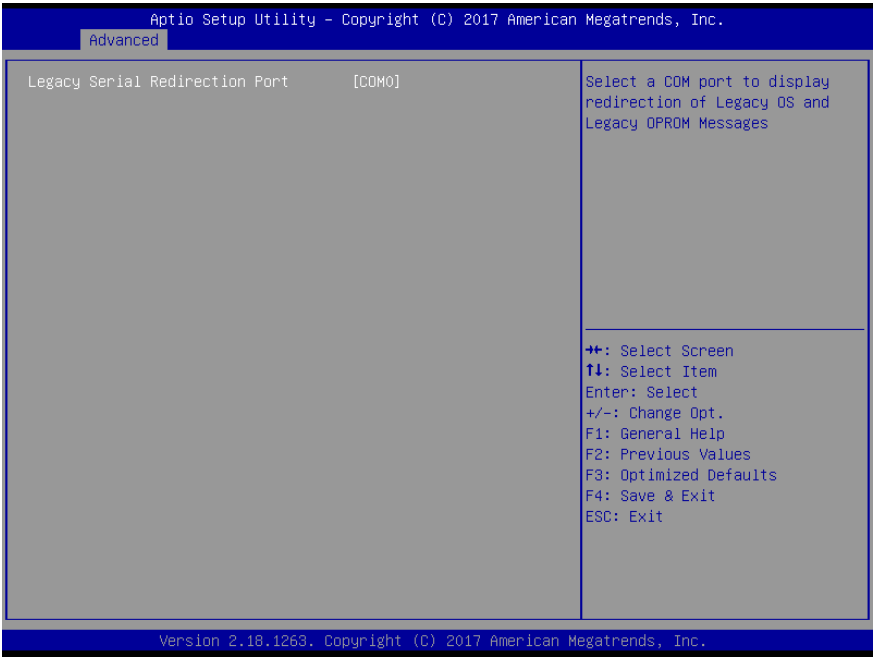



| Options Summary | |
|---|---|
| **Terminal Type** | VT100 |
| | VT100+ |
| | VT-UTF8 |
| | **ANSI** |
| Emulation: ANSI: Extended ASCII char set.<br>VT100: ASCII char set.<br>VT100+: Extends VT100 to support color, function keys, etc.<br>VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. | |
| **Bits per second** | 9600 |
| | 19200 |
| | 38400 |
| | 57600 |
| | **115200** |
| Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds. | |

| Options Summary | |
|---|---|
| Data Bits | 7 |
| | **8** |
| Data Bits. | |
| Parity | **None** |
| | Even |
| | Odd |
| | Mark |
| | Space |
| A parity bit can be sent with the data bits to detect some transmission errors.<br>Even: parity bit is 0 if the num of 1's in the data bits is even.<br>Odd: parity bit is 0 if num of 1's in the data bits is odd.<br>Mark: parity bit is always 1.<br>Space: Parity bit is always 0.<br>Mark and Space Parity do not allow for error detection. | |
| Stop Bits | **1** |
| | 2 |
| Stop bits indicate the end of a serial data packet.<br>(A start bit indicates the beginning).<br>The standard setting is 1 stop bit.<br>Communication with slow devices may require more than 1 stop bit. | |
| Flow Control | **None** |
| | Hardware RTS/CTS |
| Flow control can prevent data loss from buffer overflow.<br>When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow.<br>Once the buffers are empty, a 'start' signal can be sent to re-start the flow.<br>Hardware flow control uses two wires to send start/stop signals. | |
| VT-UTF8 Combo Key Support | Disabled |
| | **Enabled** |
| Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals. | |
| Recorder Mode | **Disabled** |
| | Enabled |
| On this mode enabled only text will be send. This is to capture Terminal data. | |
| Resolution 100x31 | **Disabled** |
| | Enabled |
| Enables or disables extended terminal resolution. | |
| Legacy OS Redirection Resolution | **80x24** |
| | 80x25 |
| On Legacy OS, the Number of Rows and Columns supported redirection. | |

| Options Summary | |
|---|---|
| Putty KeyPad | VT100 |
| | LINUX |
| | XTERMR6 |
| | SCO |
| | ESCN |
| | VT400 |
| Select FunctionKey and KeyPad on Putty. | |
| Redirection After BIOS POST | Always Enable |
| | BootLoader |
| The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS. | |

### 3.4.7.2 Legacy Console Redirection Settings



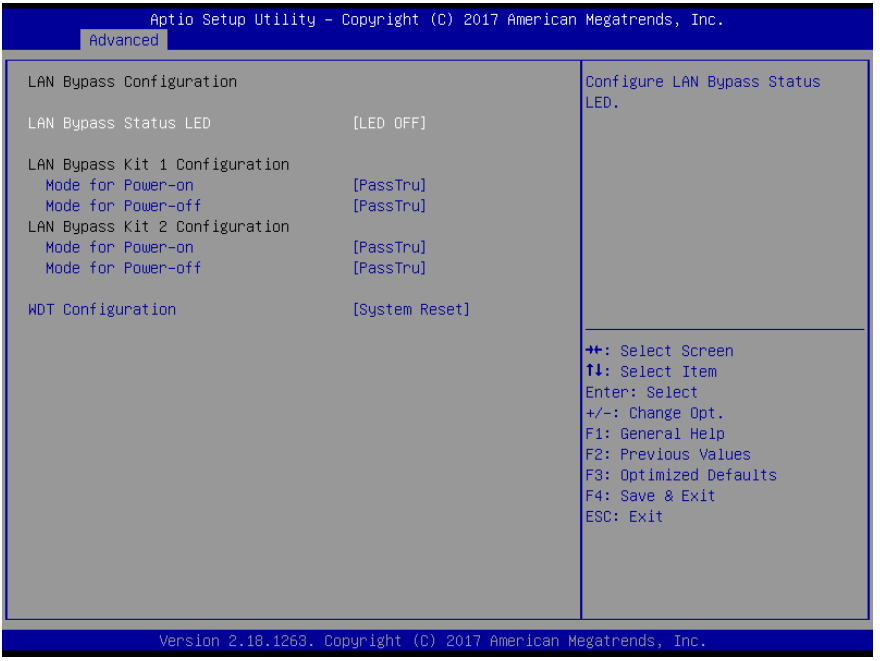

| Options Summary | |
|---|---|
| Legacy Serial Redirection Port | COM0 |
| Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages. | |

### 3.4.7.3 Serial Port for OOB Mgmt/Windows EMS


| Options Summary | |
|---|---|
| **Terminal Type** | VT100 |
| | VT100+ |
| | **VT-UTF8** |
| | ANSI |
| VT-UTF8 is the preferred terminal type for out-of-band management.<br>The next best choice is VT100+ and then VT100.<br>See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation. | |
| **Bits per second** | 9600 |
| | 19200 |
| | 57600 |
| | **115200** |
| Selects serial port transmission speed.<br>The speed must be matched on the other side. Long or noisy lines may require lower speeds. | |

| Options Summary | |
|---|---|
| Flow Control | None |
| | Hardware RTS/CTS |
| | Software Xon/Xoff |
| Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals. | |
| Data Bits | 7 |
| | 8 |
| Data Bits. | |
| Parity | None |
| | Even |
| | Odd |
| | Mark |
| | Space |
| A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even.<br>Odd: parity bit is 0 if num of 1's in the data bits is odd.<br>Mark: parity bit is always 1.<br>Space: Parity bit is always 0.<br>Mark and Space Parity do not allow for error detection. | |
| Stop Bits | 1 |
| | 2 |
| Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. | |

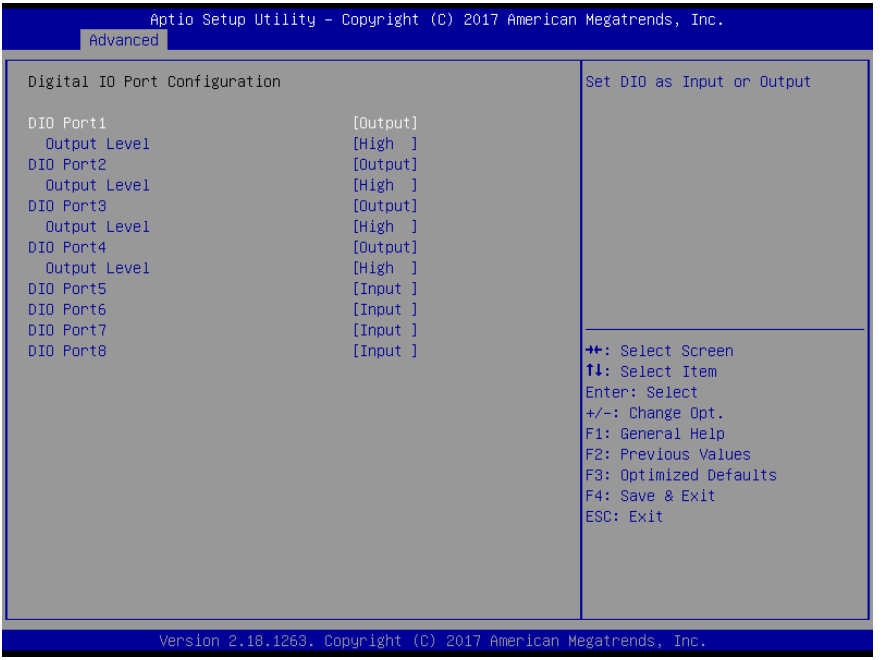
## 3.4.8 LAN Bypass Configuration




| Options Summary | |
|---|---|
| STATUS LED CTRL | **LED OFF** |
| | RED LED ON |
| | RED LED BLINK |
| | RED LED FAST BLINK |
| | GREEN LED ON |
| | GREEN LED BLINK |
| | GREEN LED FAST BLINK |
| Configure LAN Bypass Status LED. | |
| LAN kit Power ON | Bypass |
| | **PassTru** |
| Setting LAN kit function behavior when power on. (Bypass/Pass Through). | |
| LAN kit Power Off | Bypass |
| | **PassTru** |

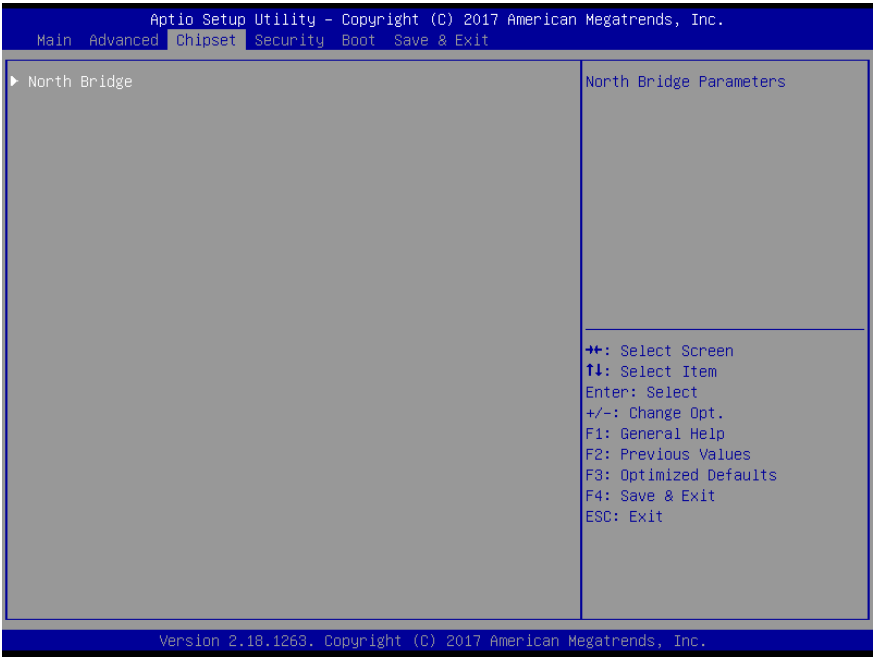
| Options Summary | |
|---|---|
| Setting LAN kit function behavior when power off.<br>(Bypass/Pass Through). | |
| WDT configuration | Force Bypass |
| | SystemReset |
| Configure WDT behavior,<br>System Reset<br>Force Bypass | |

## 3.4.9 Digital IO Port Configuration

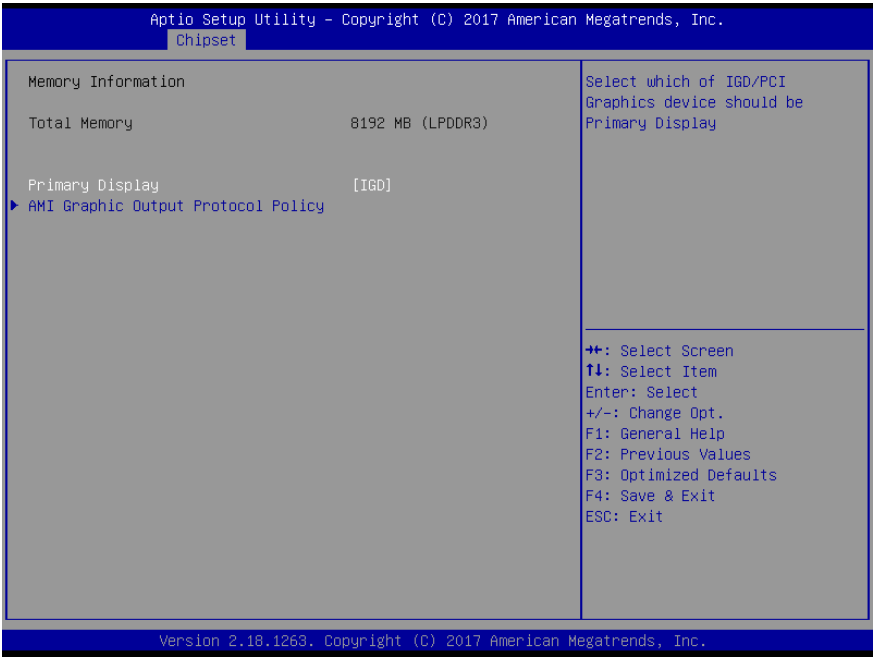



| Options Summary | |
|---|---|
| DIO_P#1~4 | Input |
| | **Output** |
| Set DIO as Input or Output. | |
| DIO_P#5~8 | **Input** |
| | Output |
| Set DIO as Input or Output. | |
| DIO_P#1~4 Direction | Low |
| | **High** |
| Set output level when DIO pin is output. | |

## 3.5 Setup Submenu: Chipset

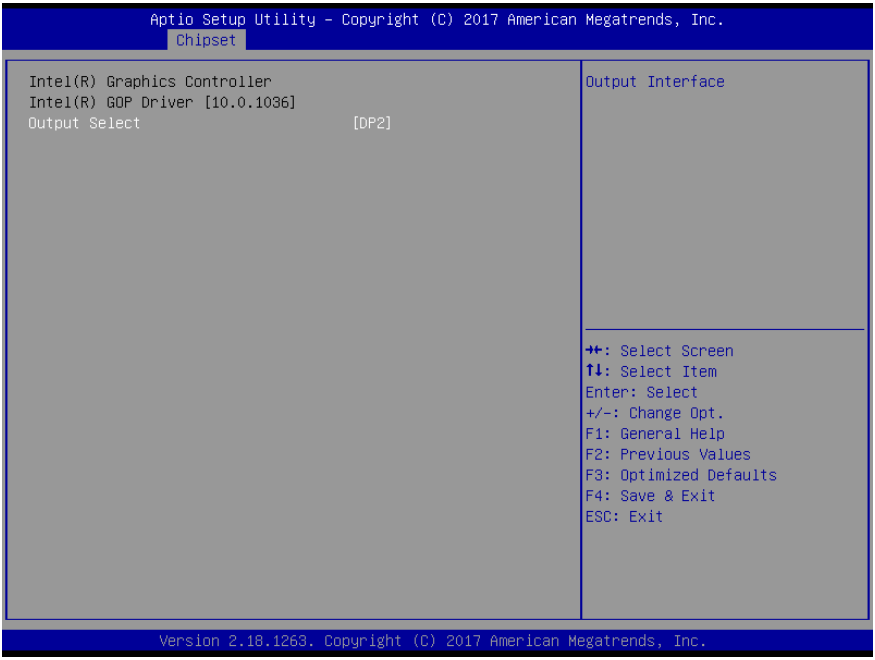


### 3.5.1 North Bridge



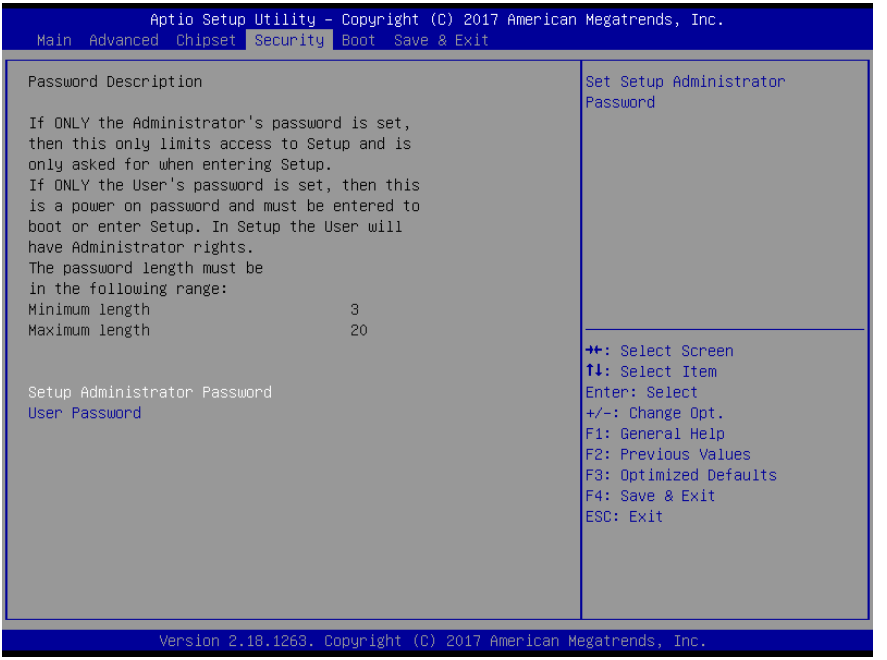

| Options Summary | |
|---|---|
| Primary Display | IGD |
| | PCIe |
| Select which of IGD/PCI Graphics device should be Primary Display. | |

### 3.5.1.1 AMI Graphic Output Protocol Policy




| Options Summary | |
|---|---|
| Output Select | DP2 |
| Output Interface. | |

## 3.6 Setup Submenu: Security




### Change User/Supervisor Password

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

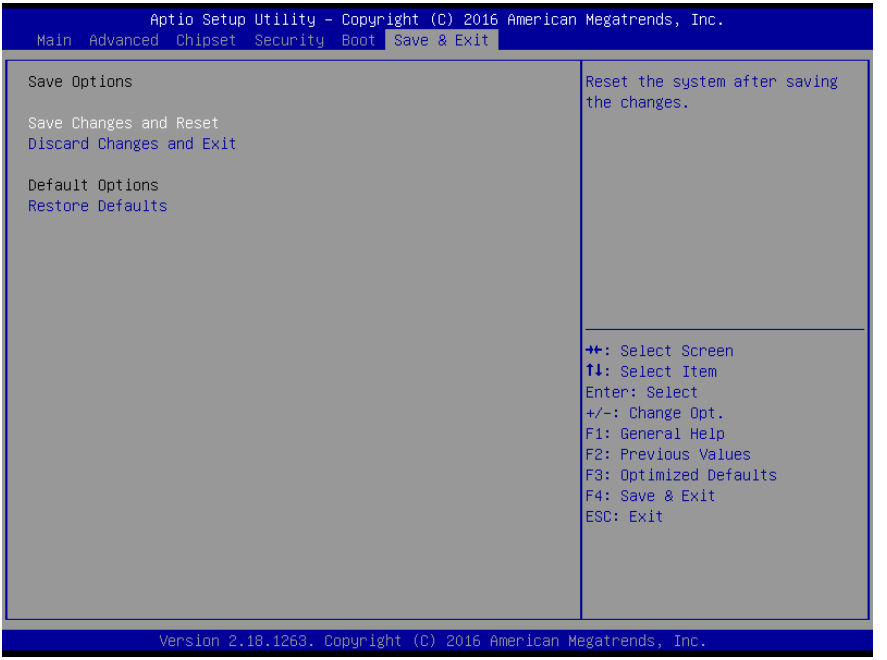
### Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

## 3.7 Setup Submenu: Boot


| Options Summary | |
|---|---|
| Quite Boot | Disabled |
| | **Enabled** |
| Enables or disables Quiet Boot option. | |
| Network Stack | **Disabled** |
| | Enabled |
| Enable/Disable UEFI Network Stack. | |

## 3.8 Setup Submenu: Exit



# Chapter 4

Driver Installation

## 4.1 Driver Installation

Please download the driver from AAEON website. It contains all the drivers and utilities you need to setup your product. Follow the steps below to install the drivers.

https://www.aaeon.com/en/p/network-appliance-ics-6270

### Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

### Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphics** folder followed by **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

### Step 3 – Install TXE Driver

1. Open the **Step 3 - TXE** folder, followed by the **SetupTXE.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

### Step 4 – Install LAN Driver

1. Open the **Step 4 – LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 5 – Install Serial IO Driver

1. Open the **Step 5 – Serial IO** folder and select your OS
2. Open the .**exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

# Appendix A

Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

| Table 1: Super I/O Relative Register Table | | |
|---|---|---|
| | Default Value | Note |
| Index | 0x2E(Note1) | SIO MB PnP Mode Index Register<br>0x2E or 0x4E |
| Data | 0x2F(Note2) | SIO MB PnP Mode Data Register<br>0x2F or 0x4F |

| Table 2: Watchdog Relative Register Table | | | | | |
|---|---|---|---|---|---|
| | LDN | Register | BitNum | Value | Note |
| Timer Counter | 0x07(Note3) | 0x73(Note4) | | (Note24) | Time of watchdog timer (0~255) This register is byte access |
| Counting Unit | 0x07(Note5) | 0x72(Note6) | 7(Note7) | 1(Note8) | Select time unit.<br>1: second<br>0: minute |
| Watchdog Enable (KRST) | 0x07(Note9) | 0x72(Note10) | 6(Note11) | 1(Note12) | 0: Disable<br>1: Enable |
| Timeout Status | 0x07(Note13) | 0x71(Note14) | 0(Note15) | 1 | 1: Clear timeout status |

```
//*************************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
//*************************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig ( ){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*********************************************************************************
```

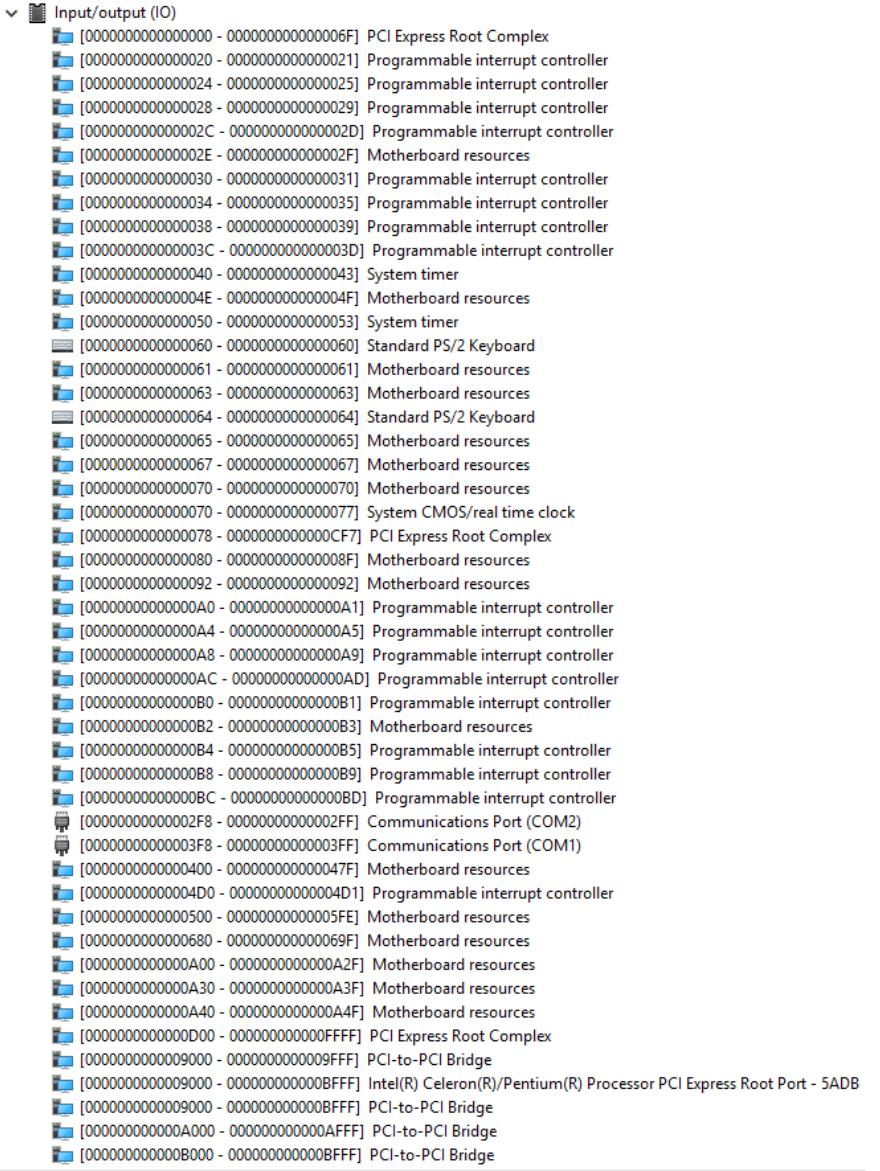
```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       Switch(SIOIndex){
              Case 0x2E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0x55);
                        Break;
              Case 0x4E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0xAA);
                     Break;
       }
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0x02);
       IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}
*****************************************************************************
```

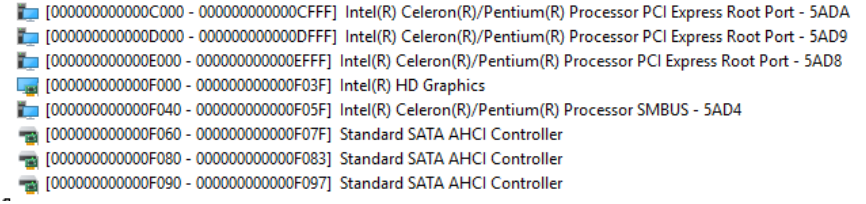
```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

# Appendix B

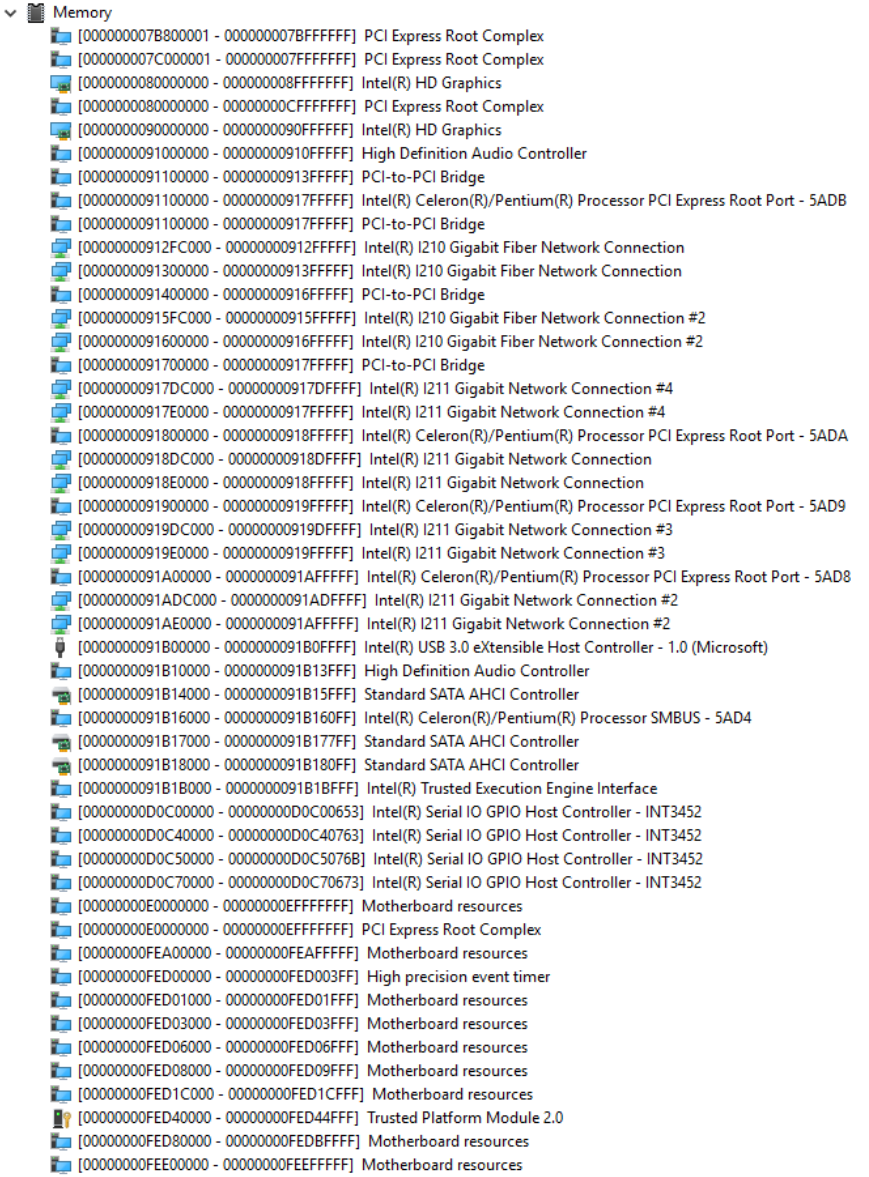
I/O Information

## B.1 I/O Address Map

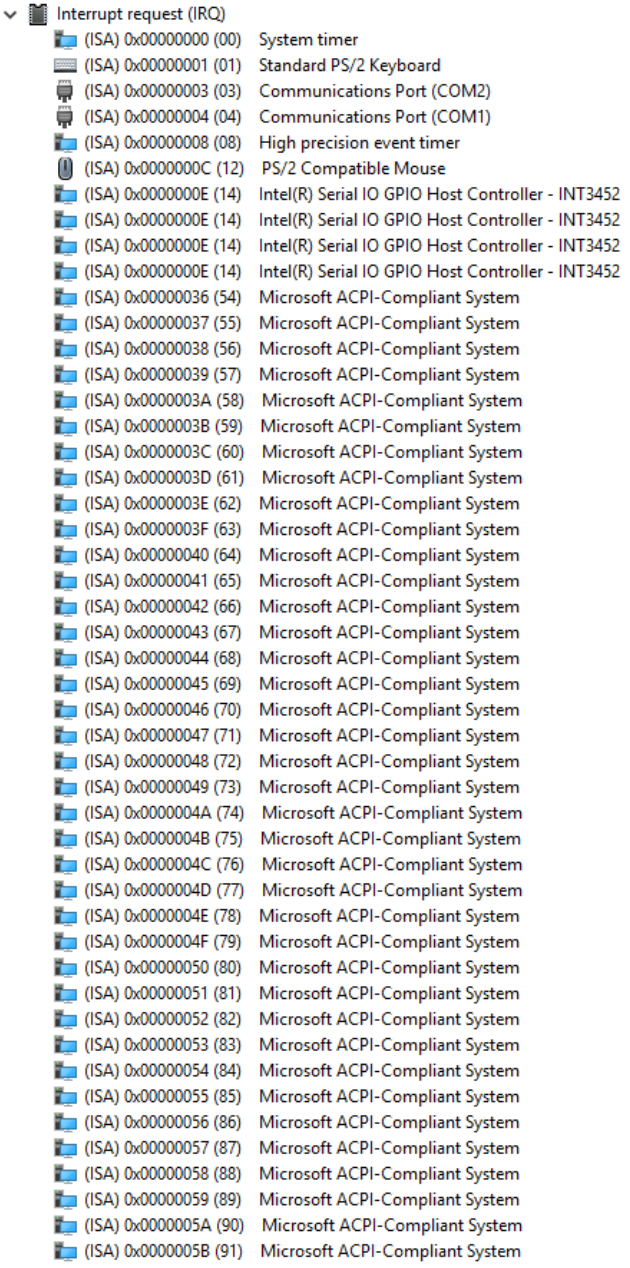


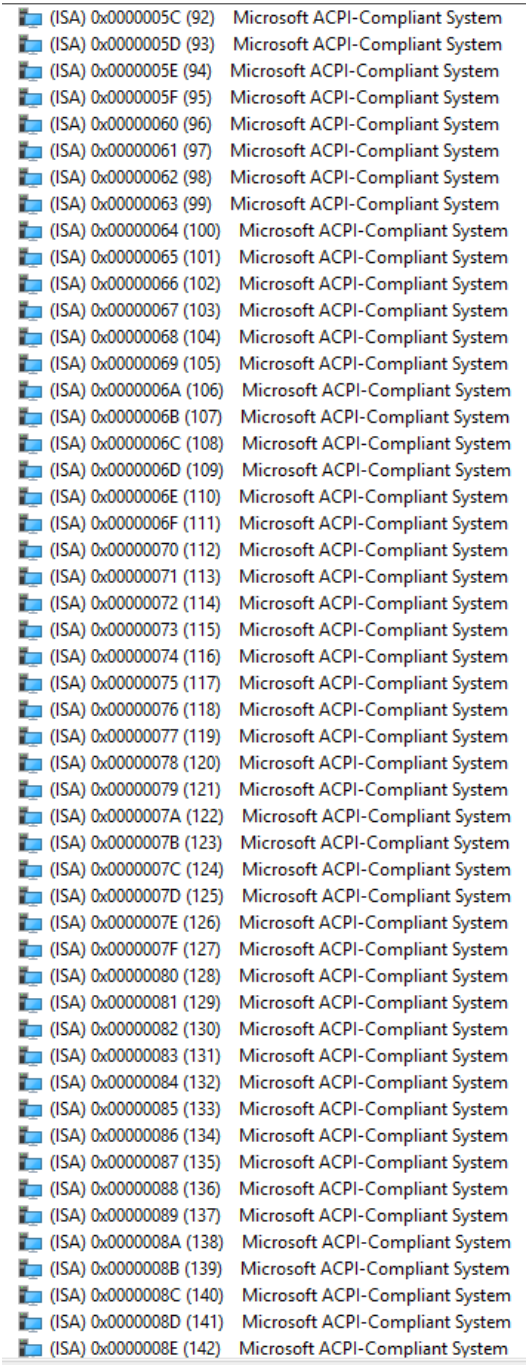

[000000000000C000 - 000000000000CFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
[000000000000D000 - 000000000000DFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[000000000000E000 - 000000000000EFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller

## B.2 Memory Address Map



## B.3 IRQ Mapping Chart




(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103) Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
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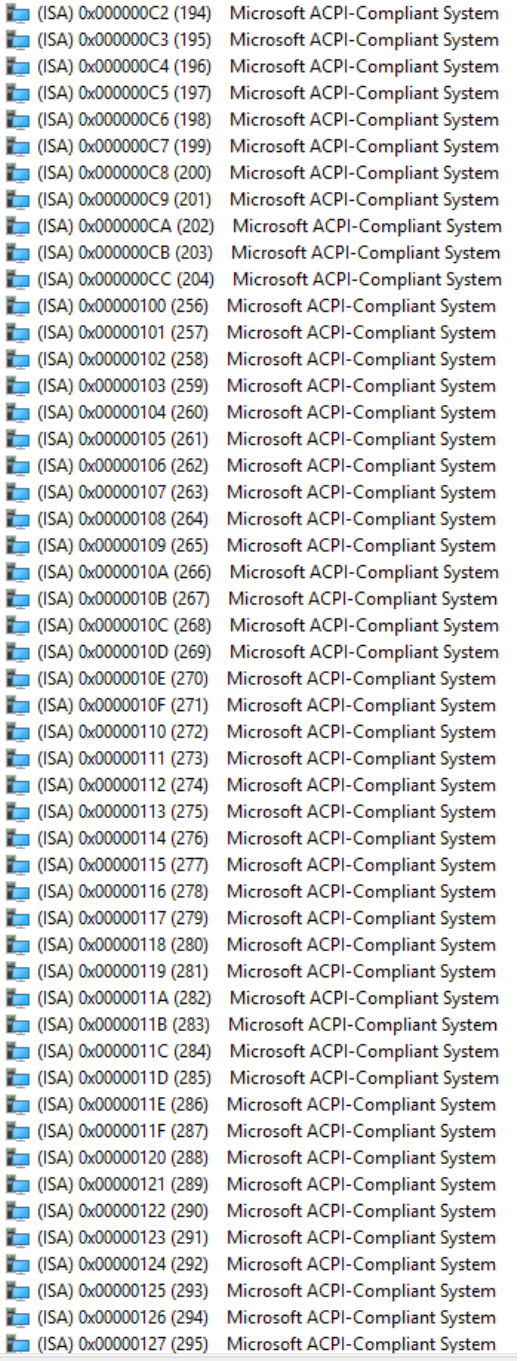
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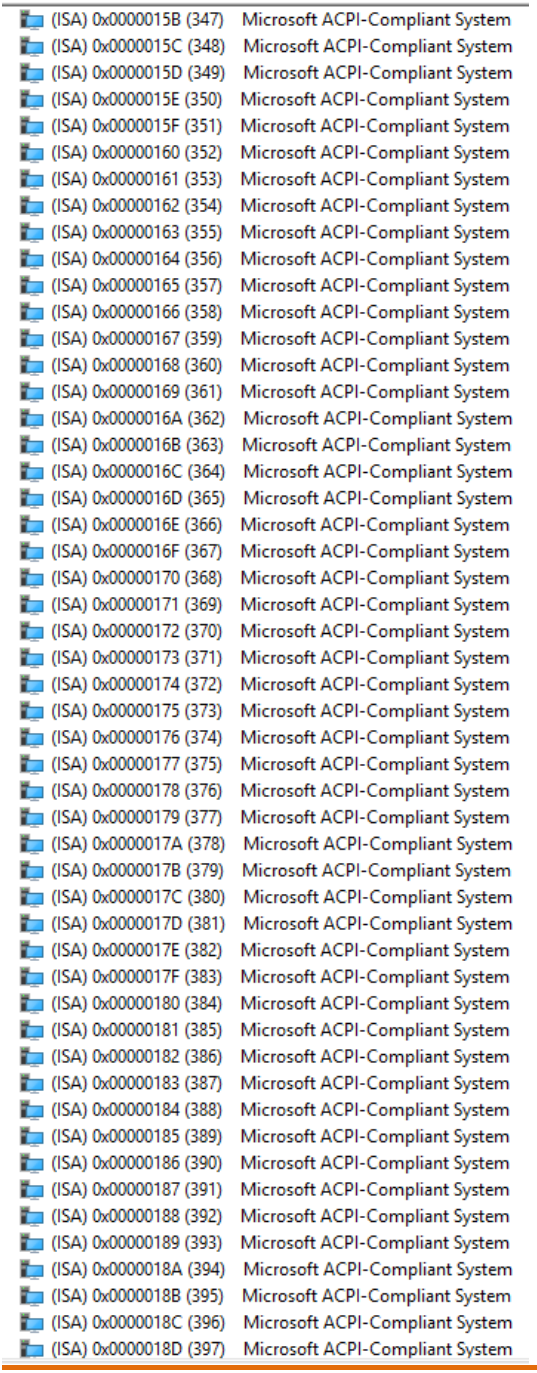
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(PCI) 0xFFFFFFE0 (-32) Intel(R) I210 Gigabit Fiber Network Connection #2
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(PCI) 0xFFFFFFF9 (-7) Intel(R) I210 Gigabit Fiber Network Connection
(PCI) 0xFFFFFFFA (-6) Intel(R) I210 Gigabit Fiber Network Connection
(PCI) 0xFFFFFFFB (-5) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFFC (-4) Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFFD (-3) Intel(R) HD Graphics
(PCI) 0xFFFFFFFE (-2) Standard SATA AHCI Controller

# Appendix C

Standard LAN Bypass Platform Setting

## C.1 Introduction to LED

ICS-6270 provides a LED indicator which can change the LED status by AAEON SDK. User is able to program the LED status to express different status.

### C.1.1 Status LED Configuration

The LED status indicator of ICS-6270 is programmable with AAEON SDK for your application.

Table 1: Table of Status LED

| STA_LED2 | STA_LED2 | STA_LED2 | STA_LED2 |
|---|---|---|---|
| 0 | 0 | 0 | LED Off |
| 0 | 0 | 1 | Red |
| 0 | 1 | 0 | Red Blinking (Slowly) |
| 0 | 1 | 1 | Red Blinking (Quickly) |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Green Blinking (Slowly) |
| 1 | 1 | 0 | Green Blinking (Quickly) |
| 1 | 1 | 1 | Green |

Table 2: Status LED Relative Register Mapping Table

| CPLD Slave Address 0x90 (Note1) | | | | |
|---|---|---|---|---|
| | Attribute | Offset (SMBUS) | BitNum | Value |
| STA_LED2 | R/W | 0x00 (Note2) | 2 | (Table 1) |
| STA_LED1 | R/W | 0x00 (Note2) | 1 | (Table 1) |
| STA_LED0 | R/W | 0x00 (Note2) | 0 | (Table 1) |

## C.1.2 Sample Code

```
*****************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*****************************************************************************************
*****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
```

```
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*********************************************************************************************
*****
```

## C.2 Introduction to LAN Bypass

ICS-6270 provides LAN Bypass kit and allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

### C.2.1 LAN Bypass

Table 1: LAN Kit ID Select

| LAN_ID2 | LAN_ID1 | LAN_ID0 | LAN kit selected |
|---|---|---|---|
| 0 | 0 | 0 | LAN Kit 1 Selected |
| 0 | 0 | 1 | LAN Kit 2 Selected |

Table 2: LAN Bypass Register Table

| Function | Description |
|---|---|
| LAN_ID3<br>LAN_ID2<br>LAN_ID1<br>LAN_ID0 | Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN. |
| PWR_ON | Use for configuring LAN Bypass function behavior to LAN kit, when system power on.<br>1: Bypass<br>0: Pass Through |
| PWR_OFF | Use for configuring LAN Bypass function behavior to LAN kit, when system power off.<br>1: Bypass<br>0: Pass Through |
| WDT_EN | Use for configuring WDT function behavior to LAN kit, when WDT triggered.<br>0: Normal WDT reset (Default)<br>1: Force Bypass |
| ACT_EN | Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state. |

Table 3: LAN Bypass Register Mapping Table

| CPLD Slave Address 0x90 (Note1) | | | | |
|---|---|---|---|---|
| | Attribute | Offset (SMBUS) | BitNum | Value |
| LAN_ID3 | R/W | 0x01(Note2) | 3 | (Table 1) |
| LAN_ID2 | R/W | 0x01(Note2) | 2 | (Table 1) |
| LAN_ID1 | R/W | 0x01(Note2) | 1 | (Table 1) |
| LAN_ID0 | R/W | 0x01(Note2) | 0 | (Table 1) |
| PWR_ON | R/W | 0x01(Note2) | 6 | (Table 2) |
| PWR_OFF | R/W | 0x01(Note2) | 5 | (Table 2) |
| WDT_EN | R/W | 0x01(Note2) | 4 | (Table 2) |
| ACT_EN | R/W | 0x01(Note2) | 7 | (Table 2) |

## C.2.2 Sample Code

```
*****************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*****************************************************************************************
*****
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xBF;
else                                    // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
```

```
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
        bData = bData & 0xEF;
else                                    // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*****************************************************************************
```

## C.3 Introduction to Software Reset Button Configuration

ICS-6270 provides a general propose input button which status get by AAEON SDK.

### C.3.1 Soft Reset Button Configuration

Table 1: Soft Reset Button Register Mapping Table

| | Attribute | Register(I/O) | BitNum | Value | Attribute |
|---|---|---|---|---|---|
| BTN_STS | R | 0xA05(Note1) | 4(Note2) | (Note3) | BTN_STS |

Table 2: LAN Bypass Relative Register Table

| Function | Description |
|---|---|
| BTN_STS | Reading this register returns the pin level status which is normal high active low.<br>0: Pin Level States Low.<br>1: Pin Level States High. |

## C.3.2 Sample Code

```
*********************************************************************************
#define Word        BTN_STS        //This parameter is represented from Note1
#define ByteBTN_STS_R              //This parameter is represented from Note2
*********************************************************************************
Byte    GET_Value (Word IoAddr, Byte BitNum,Byte Value){
        BYTE  TmpValue;

        TmpValue = inportb (IoAddr);
         return    (TmpValue & (1 << BitNum))
}
*********************************************************************************
VOID    Main(){
        Byte RstBtn;

        RstBtn = GET_Value (BTN_STS, BTN_STS_R);  // Active Low
}
*********************************************************************************
```