# HPC-ARHm

COM HPC Size Mini

User's Manual 1st Ed

*Last Updated: September 15, 2025*

## Copyright Notice

## Acknowledgements

## Packing List

Before setting up your product, please make sure the following items have been shipped:

| Item | Quantity |
| --- | --- |
| ● HPC-ARHm | 1 |

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

## Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

## FCC Statement


This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

*Caution:*

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

*Attention:*

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.*
*Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.*
*Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

## China RoHS Requirements (CN)

**产品中有毒有害物质或元素名称及含量**

AAEON **主板/子板/背板** QO4-381 Rev.A2

| 部件名称 | 有毒有害物质或元素 | | | | | |
|---|---|---|---|---|---|---|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| 印刷电路板及其电子组件 | × | ○ | ○ | ○ | ○ | ○ |
| 外部信号连接器及线材 | × | ○ | ○ | ○ | ○ | ○ |

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period)) : 10年

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

## China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON Main Board/Daughter Board/Backplane QO4-381 Rev.A2

| Part Name | Hazardous Substances | | | | | |
|---|---|---|---|---|---|---|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| PCB Assemblies | × | ○ | ○ | ○ | ○ | ○ |
| Connector and Cable | × | ○ | ○ | ○ | ○ | ○ |

The table is prepared in accordance with the provisions of SJ/T 11364.

○：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years

Notes: This product defined period of use is under normal condition.

# Table of Contents

# Chapter 1

Product Specifications

## 1.1 Specifications

| System | |
|---|---|
| Form Factor | COM-HPC R1.2 Mini |
| CPU | Intel® Core™ Ultra Processors:<br>Intel® Core™ Ultra 7 Processor 255H<br>(16C/16T, 2.0GHz, 28W)<br>Intel® Core™ Ultra 5 Processor 225H<br>(14C/14T, 1.7GHz, 28W)<br>Intel® Core™ Ultra 7 Processor 155H<br>(16C/22T, 1.4 GHz, 28W)<br>Intel® Core™ Ultra 5 Processor 125H<br>(14C/18T, 1.2 GHz, 28W) |
| Chipset | SoC |
| Memory | Onboard LPDDR5x, up to 64GB |
| Onboard Storage | Onboard NVMe, up to 256GB |
| BIOS | AMI UEFI |
| Wake on LAN | Yes |
| Watchdog Timer | 255 Levels |
| Dimension | 3.74" x 2.76" (95mm x 70mm) |
| Security | dTPM / fTPM |

| Power | |
|---|---|
| Power Requirement | +12V for ATX / AT |
| Power Type | AT/ATX |
| Power Consumption (Typical) | Intel® Core™ Ultra 7 265H, 4.13 @+12V |

## Display

| | |
|---|---|
| **Graphics Controller** | Series 1 CPU SKU: Intel® Arc™ Graphics |
| | Series 2 CPU SKU: Intel® Arc™ 140T/130T GPU |
| **Video Output** | DDI1: DP/HDMI, up to 3840 x 2160 |
| | DDI2: DP/HDMI, up to 3840 x 2160 |
| | eDP: up to 3840 x 2160 |

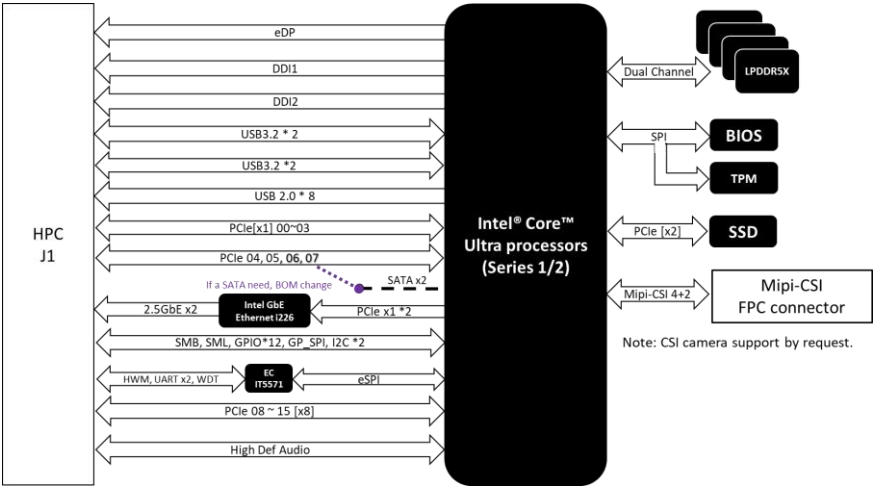
## I/O

| | |
|---|---|
| **Ethernet** | Intel® Ethernet Controller I226, 2.5GbE x 2 |
| **Audio** | High Definition Audio Interface |
| **USB Port** | USB 3.2 (10Gbps) x 4 |
| | USB 2.0 x 8 |
| **Serial Port** | 4-Wire UART x 2 (Tx/Rx/RTS/CTS) |
| **HDD Interface** | Optional: SATA 6Gb/s x 2, via PCIe lane 6 and lane 7 |
| | *BIOS and BOM change required to enable SATA |
| **Expansion** | PCIe 4.0 [x8] x 1 |
| | PCIe 3.0 [x1] x 4 |
| | PCIe 3.0 [x4] x 1 (lanes 6 and 7 co-lay with SATA) |
| **GPIO** | 12-bit |
| **SMBus/I2C** | I2C x 2 |
| | SMBus x 1 |

## Environmental

| | |
|---|---|
| Operating Temperature | 32°F ~ 140°F (0°C ~ 60°C) |
| Storage Temperature | -40°F ~ 185°F (-40°C ~ 85°C) |
| Operating Humidity | 0% ~ 90% relative humidity, non-condensing |
| EMC | CE/FCC Class A |
| OS Support | Windows 11 |
| | Ubuntu 24.04/Kernel 6.11 |
| Weight | 0.17 lb (0.08 kg) |

## 1.2 Block Diagram

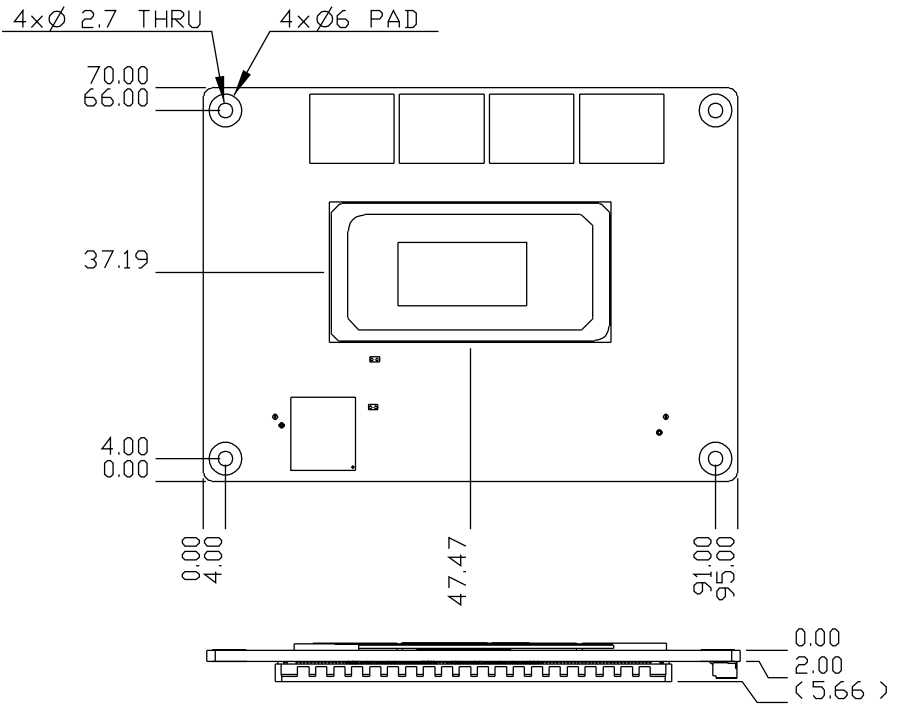


# Chapter 2

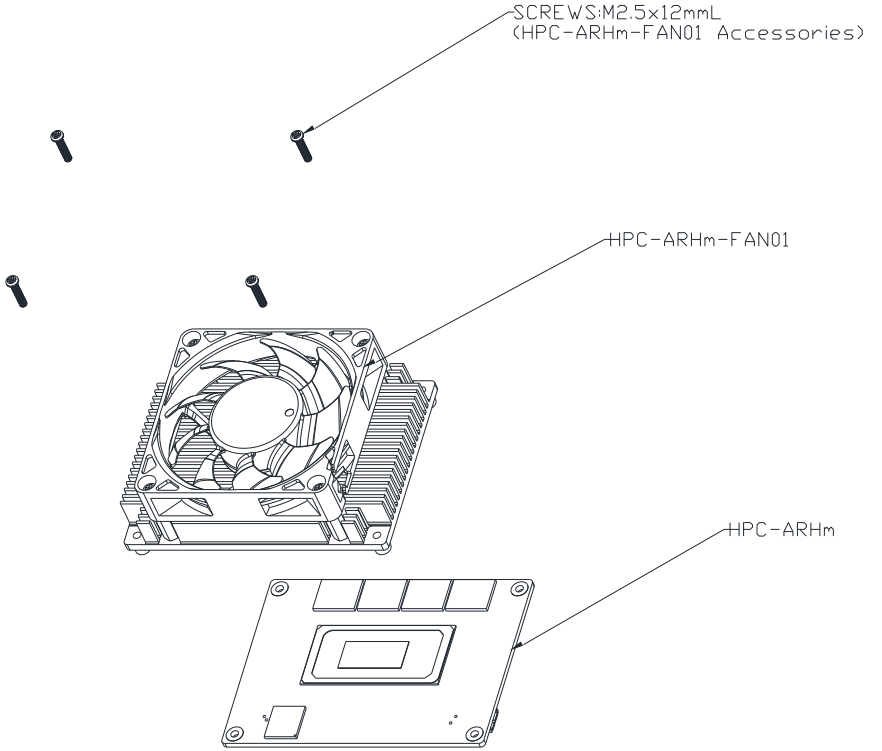
Hardware Information

## 2.1 Dimensions

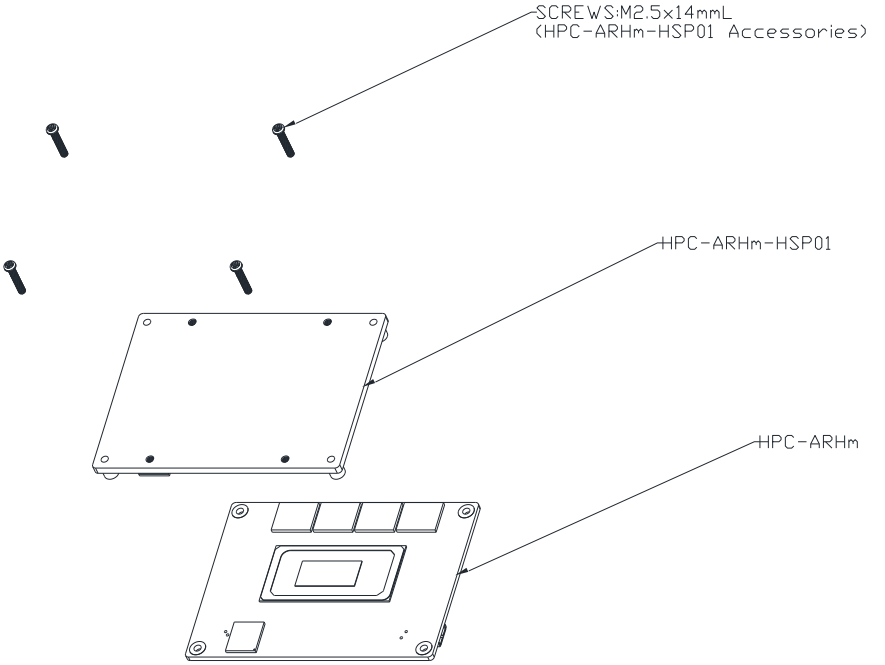
Top Side



With Active Cooler (P/N HPC-ARHm -FAN01)

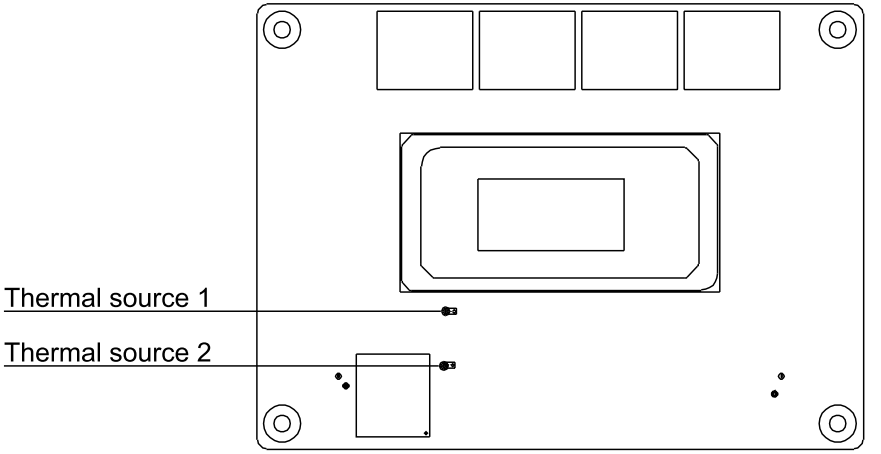


With Heat Spreader (P/N HPC-ARHm -HSP01)

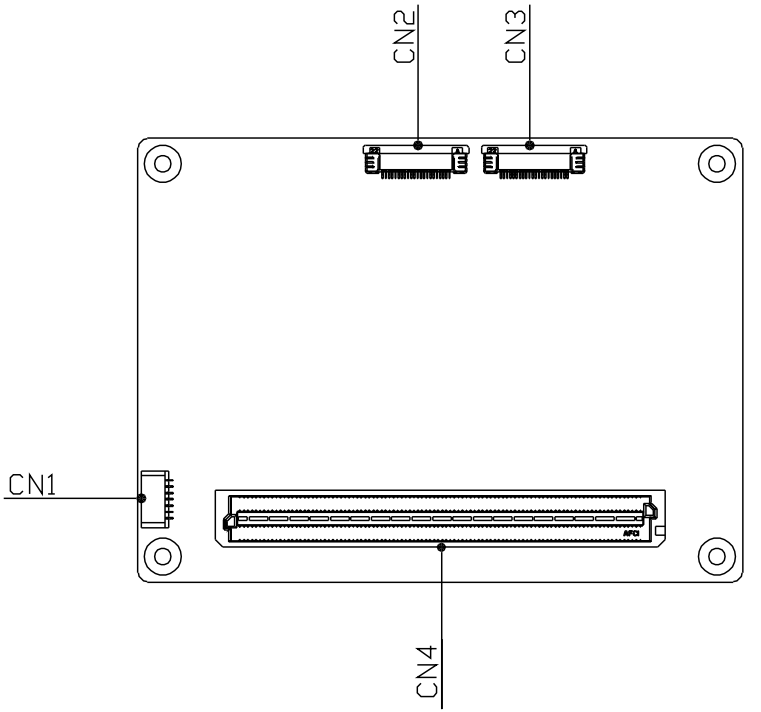


## 2.2 Jumpers and Connectors

Top Side




Bottom Side

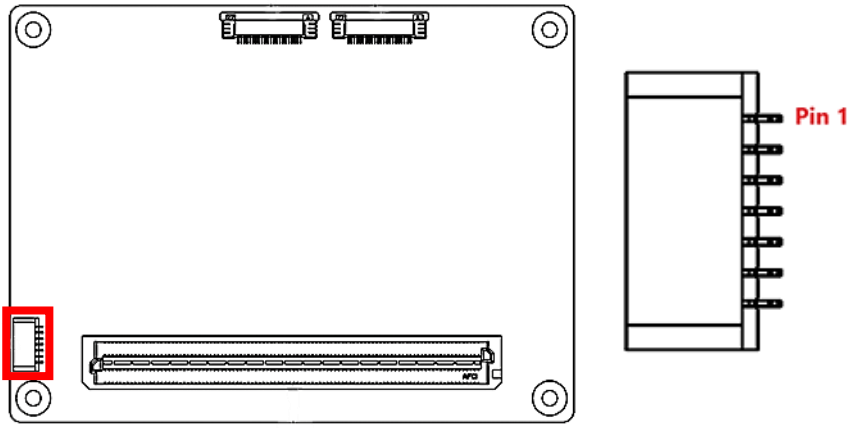


## 2.3 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

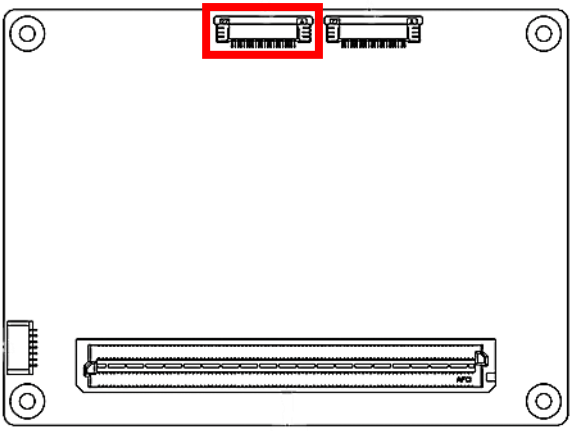
| Label | Function |
|---|---|
| CN1 | SPI ROM FLASH |
| CN2 | MIPI CSI CH 1 |
| CN3 | MIPI CSI CH 2 |
| CN4 | Row A/B/C/D |

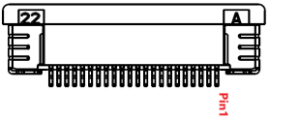
### 2.3.1 SPI ROM FLASH (CN1)




| Pin | Signal |
|---|---|
| 1 | SPI_SO |
| 2 | GND |
| 3 | SPI_CLK |
| 4 | CSI_DP_0 |
| 5 | CSI_DN_0 |
| 6 | GND |
| 7 | NC |

### 2.3.2 MIPI CSI CH1 (CN2)

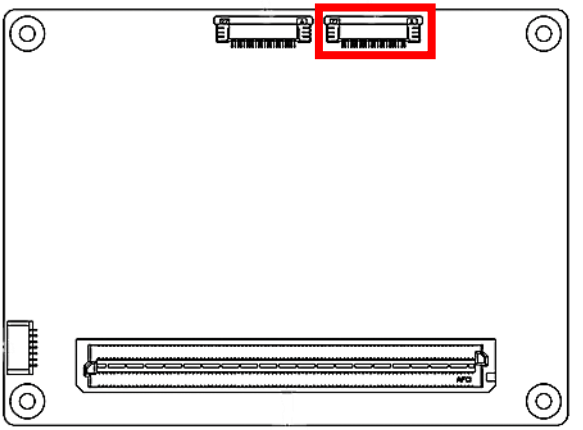


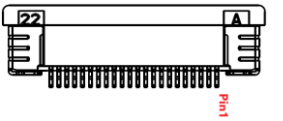



| Pin | Signal |
|---|---|
| 1 | VCC_3.3V |
| 2 | VCC_3.3V |
| 3 | GND |
| 4 | CSI_DP_0 |
| 5 | CSI_DN_0 |
| 6 | GND |
| 7 | CSI_DP_1 |
| 8 | CSI_DN_1 |
| 9 | GND |
| 10 | CSI_DP_2 |
| 11 | CSI_DN_2 |
| 12 | CAM_RST# |
| 13 | CSI_DP_3 |
| 14 | CSI_DN_3 |
| 15 | GND |
| 16 | CSI_CLK_P |
| 17 | CSI_CLK_N |
| 18 | GND |
| 19 | I2C_CLK |
| 20 | I2C_DAT |

| Pin | Signal |
|---|---|
| 21 | CRD_PWREN |
| 22 | IMGCLKOUT |

### 2.3.3 MIPI CSI CH2 (CN3)

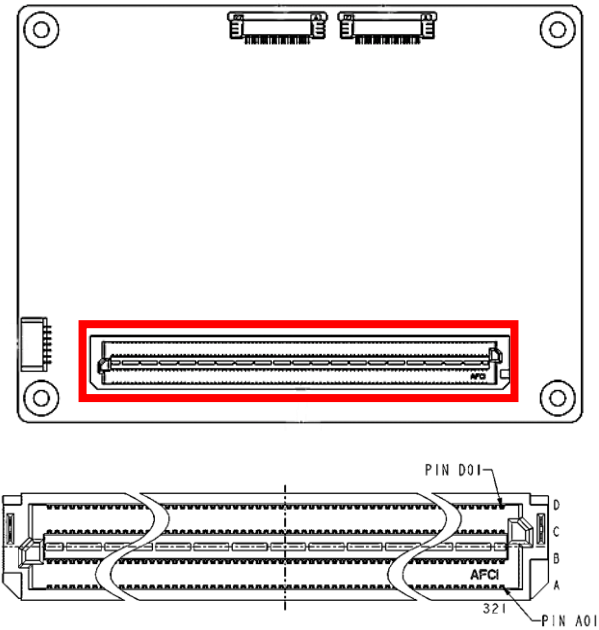





| Pin | Signal |
|---|---|
| 1 | VCC_3.3V |
| 2 | VCC_3.3V |
| 3 | GND |
| 4 | CSI_DP_0 |
| 5 | CSI_DN_0 |
| 6 | GND |
| 7 | CSI_DP_1 |
| 8 | CSI_DN_1 |
| 9 | GND |
| 10 | CSI_DP_2 |
| 11 | CSI_DN_2 |
| 12 | CAM_RST# |
| 13 | CSI_DP_3 |
| 14 | CSI_DN_3 |
| 15 | GND |
| 16 | CSI_CLK_P |

| Pin | Signal |
|---|---|
| 17 | CSI_CLK_N |
| 18 | GND |
| 19 | I2C_CLK |
| 20 | I2C_DAT |
| 21 | CRD_PWREN |
| 22 | IMGCLKOUT |

### 2.3.4 Row A/B/C/D Connector (CN4)




| Row A | | Row B | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| A1 | VCC | B1 | VCC |
| A2 | VCC | B2 | PWRBTN# |
| A3 | VCC | B3 | VCC |
| A4 | VCC | B4 | THERMTRIP# |
| A5 | VCC | B5 | N.C |
| A6 | RAPID_SHUTDOWN | B6 | TAMPER# |
| A7 | N.C | B7 | PROCHOT# |

| Row A | | Row B | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| A8 | N.C | B8 | SUS_S3# |
| A9 | N.C | B9 | N.C |
| A10 | GND | B10 | WD_STROBE# |
| A11 | N.C | B11 | WD_OUT |
| A12 | N.C | B12 | GND |
| A13 | GND | B13 | USB5- |
| A14 | USB7- | B14 | USB5+ |
| A15 | USB7+ | B15 | GND |
| A16 | GND | B16 | USB4- |
| A17 | USB6- | B17 | USB4+ |
| A18 | USB6+ | B18 | GND |
| A19 | GND | B19 | HDA_SYNC |
| A20 | SS23_SDA_AUX- | B20 | HDA_SDO |
| A21 | SS23_SDA_AUX+ | B21 | HDA_RST# |
| A22 | GND | B22 | HDA_SDI |
| A23 | SS2_TX- | B23 | HDA_BCLK |
| A24 | SS2_TX+ | B24 | RSVD |
| A25 | GND | B25 | USB67_OC# |
| A26 | SS2_RX- | B26 | USB45_OC# |
| A27 | SS2_RX+ | B27 | USB23_OC# |
| A28 | GND | B28 | USB01_OC# |
| A29 | SS3_TX- | B29 | SML1_CLK |
| A30 | SS3_TX+ | B30 | SML1_DAT |
| A31 | GND | B31 | PMCALERT# |
| A32 | SS3_RX- | B32 | SML0_CLK |
| A33 | SS3_RX+ | B33 | SML0_DAT |
| A34 | GND | B34 | USB_PD_ALERT# |
| A35 | eDP_AUX- | B35 | USB_PD_I2C_CLK |
| A36 | eDP_AUX+ | B36 | USB_PD_I2C_DAT |
| A37 | GND | B37 | USB_RT_ENA |
| A38 | eDP_TX0- | B38 | N.C |
| A39 | eDP_TX0+ | B39 | N.C |
| A40 | GND | B40 | DDI0_DDC_AUX_SEL |
| A41 | eDP_TX1- | B41 | DDI0_HPD |
| A42 | eDP_TX1+ | B42 | GND |
| A43 | GND | B43 | USB1_AUX- |
| A44 | eDP_TX2- | B44 | USB1_AUX+ |
| A45 | eDP_TX2+ | B45 | LID# |

| Row A | | Row B | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| A46 | GND | B46 | SLEEP# |
| A47 | eDP_TX3- | B47 | VCC_BOOT_SPI |
| A48 | eDP_TX3+ | B48 | BOOT_SPI_CS# |
| A49 | GND | B49 | BSEL0 |
| A50 | N.C | B50 | BSEL1 |
| A51 | N.C | B51 | BSEL2 |
| A52 | N.C | B52 | N.C |
| A53 | N.C | B53 | N.C |
| A54 | N.C | B54 | N.C |
| A55 | GND | B55 | N.C |
| A56 | PCIe_CLKREQ0_LO# | B56 | N.C |
| A57 | PCIe_CLKREQ0_HI# | B57 | N.C |
| A58 | N.C | B58 | NBASET1_LINK_MID# |
| A59 | NBASET1_LINK_MAX# | B59 | NBASET1LINK_ACT# |
| A60 | NBASET1_CTREF | B60 | GND |
| A61 | GND | B61 | PCIe08_RX- |
| A62 | PCIe08_TX- | B62 | PCIe08_RX+ |
| A63 | PCIe08_TX+ | B63 | GND |
| A64 | GND | B64 | PCIe09_RX- |
| A65 | PCIe09_TX- | B65 | PCIe09_RX+ |
| A66 | PCIe09_TX+ | B66 | GND |
| A67 | GND | B67 | PCIe10_RX- |
| A68 | PCIe10_TX- | B68 | PCIe10_RX+ |
| A69 | PCIe10_TX+ | B69 | GND |
| A70 | GND | B70 | PCIe11_RX- |
| A71 | PCIe11_TX- | B71 | PCIe11_RX+ |
| A72 | PCIe11_TX+ | B72 | GND |
| A73 | GND | B73 | PCIe12_RX- |
| A74 | PCIe12_TX- | B74 | PCIe12_RX+ |
| A75 | PCIe12_TX+ | B75 | GND |
| A76 | GND | B76 | PCIe13_RX- |
| A77 | PCIe13_TX- | B77 | PCIe13_RX+ |
| A78 | PCIe13_TX+ | B78 | GND |
| A79 | GND | B79 | PCIe14_RX- |
| A80 | PCIe14_TX- | B80 | PCIe14_RX+ |
| A81 | PCIe14_TX+ | B81 | GND |
| A82 | GND | B82 | PCIe15_RX- |
| A83 | PCIe15_TX- | B83 | PCIe15_RX+ |

| Row A | | Row B | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| A84 | PCIe15_TX+ | B84 | GND |
| A85 | GND | B85 | N.C |
| A86 | VCC_RTC | B86 | RSMRST_OUT# |
| A87 | SUS_CLK | B87 | UART1_TX |
| A88 | GPIO_00 | B88 | UART1_RX |
| A89 | GPIO_01 | B89 | UART1_RTS# |
| A90 | GPIO_02 | B90 | UART1_CTS# |
| A91 | GPIO_03 | B91 | N.C |
| A92 | GPIO_04 | B92 | N.C |
| A93 | GPIO_05 | B93 | GP_SPI_MOSI |
| A94 | GPIO_06 | B94 | GP_SPI_MISO |
| A95 | GPIO_07 | B95 | GP_SPI_CS0# |
| A96 | GPIO_08 | B96 | N.C |
| A97 | GPIO_09 | B97 | N.C |
| A98 | GPIO_10 | B98 | N.C |
| A99 | GPIO_11 | B99 | GP_SPI_CLK |
| A100 | PINOUT_TYPE0 | B100 | GP_SPI_ALERT# |

| Row C | | Row D | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| C1 | VCC | D1 | VCC |
| C2 | RSTBTN# | D2 | VCC |
| C3 | VCC | D3 | VCC |
| C4 | CARRIER_HOT# | D4 | VCC |
| C5 | N.C | D5 | PLTRST# |
| C6 | VIN_PWR_OK | D6 | N.C |
| C7 | CATERR# | D7 | N.C |
| C8 | SUS_S4_S5# | D8 | N.C |
| C9 | N.C | D9 | N.C |
| C10 | BATLOW# | D10 | WAKE0# |
| C11 | FAN_PWMOUT | D11 | WAKE1# |
| C12 | FAN_TACHIN | D12 | GND |
| C13 | GND | D13 | USB1- |
| C14 | USB3- | D14 | USB1+ |
| C15 | USB3+ | D15 | GND |
| C16 | GND | D16 | USB0- |
| C17 | USB2- | D17 | USB0+ |
| C18 | USB2+ | D18 | GND |

| Row C | | Row D | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| C19 | GND | D19 | SS01_SDA_AUX- |
| C20 | SNDW_DMIC_CLK1 | D20 | SS01_SDA_AUX+ |
| C21 | SNDW_DMIC_DAT1 | D21 | GND |
| C22 | GND | D22 | SS0_TX- |
| C23 | SNDW_DMIC_CLK0 | D23 | SS0_TX+ |
| C24 | SNDW_DMIC_DAT0 | D24 | GND |
| C25 | GND | D25 | SS0_RX- |
| C26 | DDI1_DDC_AUX_SEL | D26 | SS0_RX+ |
| C27 | N.C | D27 | GND |
| C28 | DDI1_HPD | D28 | SS1_TX- |
| C29 | N.C | D29 | SS1_TX+ |
| C30 | eDP_HPD | D30 | GND |
| C31 | eDP_VDD_EN | D31 | SS1_RX- |
| C32 | eDP_BKLT_EN | D32 | SS1_RX+ |
| C33 | eDP_BKLTCTL | D33 | GND |
| C34 | GND | D34 | ACPRESENT |
| C35 | N.C | D35 | NBASET1_SDP |
| C36 | N.C | D36 | GND |
| C37 | GND | D37 | SS6_TX- |
| C38 | SS6_RX- | D38 | SS6_TX+ |
| C39 | SS6_RX+ | D39 | GND |
| C40 | GND | D40 | SS7_TX- |
| C41 | SS7_RX- | D41 | SS7_TX+ |
| C42 | SS7_RX+ | D42 | GND |
| C43 | GND | D43 | SS4_TX- |
| C44 | SS4_RX- | D44 | SS4_TX+ |
| C45 | SS4_RX+ | D45 | GND |
| C46 | GND | D46 | SS5_TX- |
| C47 | SS5_RX- | D47 | SS5_TX+ |
| C48 | SS5_RX+ | D48 | GND |
| C49 | GND | D49 | NBASET1_MDI0- |
| C50 | BOOT_SPI_IO0 | D50 | NBASET1_MDI0+ |
| C51 | BOOT_SPI_IO1 | D51 | GND |
| C52 | BOOT_SPI_IO2 | D52 | NBASET1_MDI1- |
| C53 | BOOT_SPI_IO3 | D53 | NBASET1_MDI1+ |
| C54 | BOOT_SPI_CLK | D54 | GND |
| C55 | GND | D55 | NBASET1_MDI2- |
| C56 | PCIe_REFCLK0_HI- | D56 | NBASET1_MDI2+ |

| Row C | | Row D | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| C57 | PCIe_REFCLK0_HI+ | D57 | GND |
| C58 | GND | D58 | NBASET1_MDI3- |
| C59 | PCIe_REFCLK0_LO- | D59 | NBASET1_MDI3+ |
| C60 | PCIe_REFCLK0_LO+ | D60 | GND |
| C61 | GND | D61 | PCIe00_TX- |
| C62 | PCIe00_RX- | D62 | PCIe00_TX+ |
| C63 | PCIe00_RX+ | D63 | GND |
| C64 | GND | D64 | PCIe01_TX- |
| C65 | PCIe01_RX- | D65 | PCIe01_TX+ |
| C66 | PCIe01_RX+ | D66 | GND |
| C67 | GND | D67 | PCIe02_TX- |
| C68 | PCIe02_RX- | D68 | PCIe02_TX+ |
| C69 | PCIe02_RX+ | D69 | GND |
| C70 | GND | D70 | PCIe03_TX- |
| C71 | PCIe03_RX- | D71 | PCIe03_TX+ |
| C72 | PCIe03_RX+ | D72 | GND |
| C73 | GND | D73 | PCIe04_TX- |
| C74 | PCIe04_RX- | D74 | PCIe04_TX+ |
| C75 | PCIe04_RX+ | D75 | GND |
| C76 | GND | D76 | PCIe05_TX- |
| C77 | PCIe05_RX- | D77 | PCIe05_TX+ |
| C78 | PCIe05_RX+ | D78 | GND |
| C79 | GND | D79 | PCIe06_TX- |
| C80 | PCIe06_RX-/SATA1_RX- | D80 | PCIe06_TX+ |
| C81 | PCIe06_RX+/SATA1_RX+ | D81 | GND |
| C82 | GND | D82 | PCIe07_TX- |
| C83 | PCIe07_RX-/SATA0_RX- | D83 | PCIe07_TX+ |
| C84 | PCIe07_RX+/SATA0_RX+ | D84 | GND |
| C85 | GND | D85 | NBASET0_MDI0- |
| C86 | SMB_CLK | D86 | NBASET0_MDI0+ |
| C87 | SMB_DAT | D87 | GND |
| C88 | SMB_ALERT# | D88 | NBASET0_MDI1- |
| C89 | UART0_TX | D89 | NBASET0_MDI1+ |
| C90 | UART0_RX | D90 | GND |
| C91 | UART0_RTS# | D91 | NBASET0_MDI2- |
| C92 | UART0_CTS# | D92 | NBASET0_MDI2+ |
| C93 | I2C0_CLK | D93 | GND |
| C94 | I2C0_DAT | D94 | NBASET0_MDI3- |

| Row C | | Row D | |
|---|---|---|---|
| Pin | Signal | Pin | Signal |
| C95 | I2C0_ALERT# | D95 | NBASET0_MDI3+ |
| C96 | I2C1_CLK | D96 | GND |
| C97 | I2C1_DAT | D97 | NBASET0_LINK_MAX# |
| C98 | NBASET0_SDP | D98 | NBASET0_LINK_MID# |
| C99 | NBASET0_CTREF | D99 | NBASET0_LINK_ACT# |
| C100 | PINOUT_TYPE1 | D100 | PINOUT_TYPE2 |

# Chapter 3

AMI BIOS Setup

## 3.1 System Test and Initialization

The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:
You are starting your system for the first time.
You have changed the hardware attached to your system.
The CMOS memory has lost power and the configuration information has been erased.

The HPC-ARHm CMOS memory uses a backup battery for data retention. The battery must be replaced if it runs out of power.

## 3.2 AMI BIOS Setup

The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off.

To enter Setup, power on the computer and press <Del> immediately.

The function of each menu is as follows:

**Main** – Date and time can be set here. Use <Tab> to switch between date elements.

**Advanced** – Enable/disable boot option for legacy network devices.

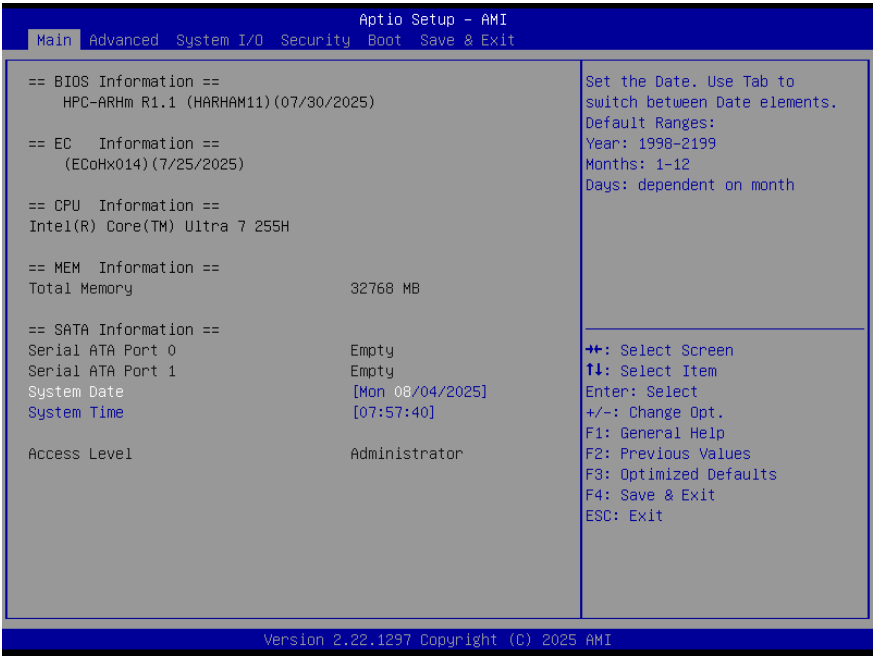
**System I/O** – Enable/ Disable System input and output port.

**Security** – Password for setup administrator can be set here.

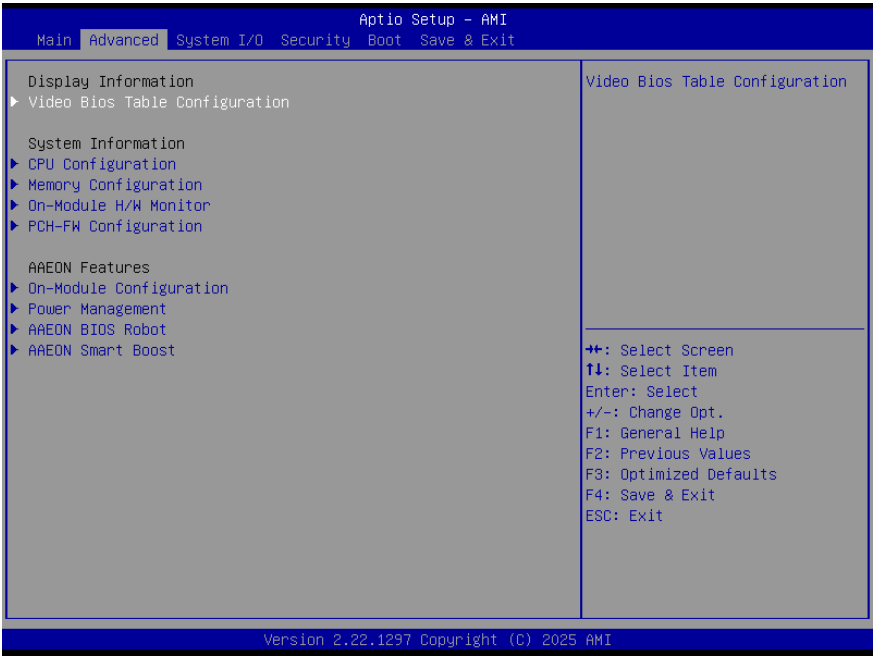
**Boot** – Enable/disable Quiet Boot option.

**Save & Exit** – Save changes and exit Setup.

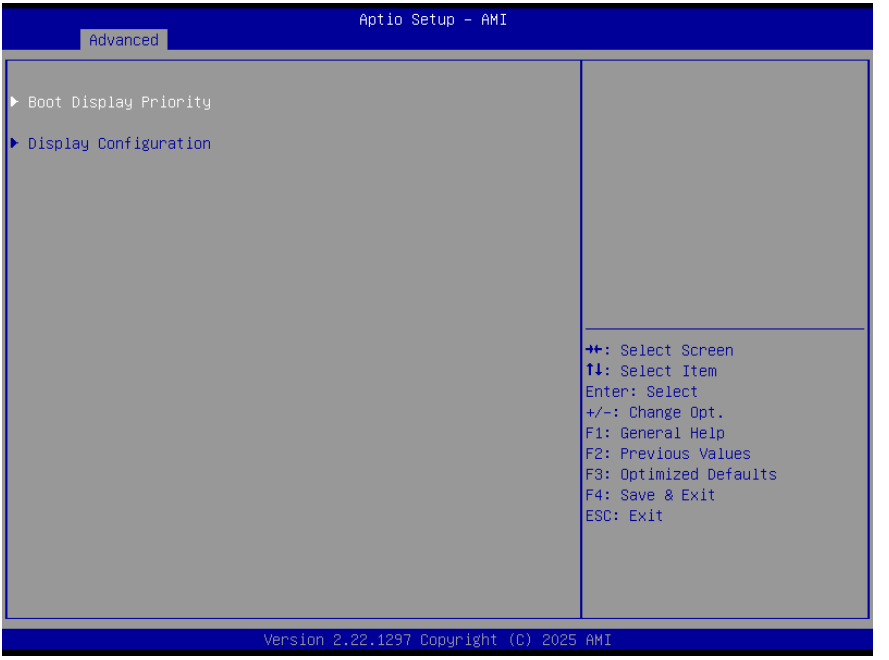
## 3.3 Setup Submenu: Main



## 3.4 Setup Submenu: Advanced



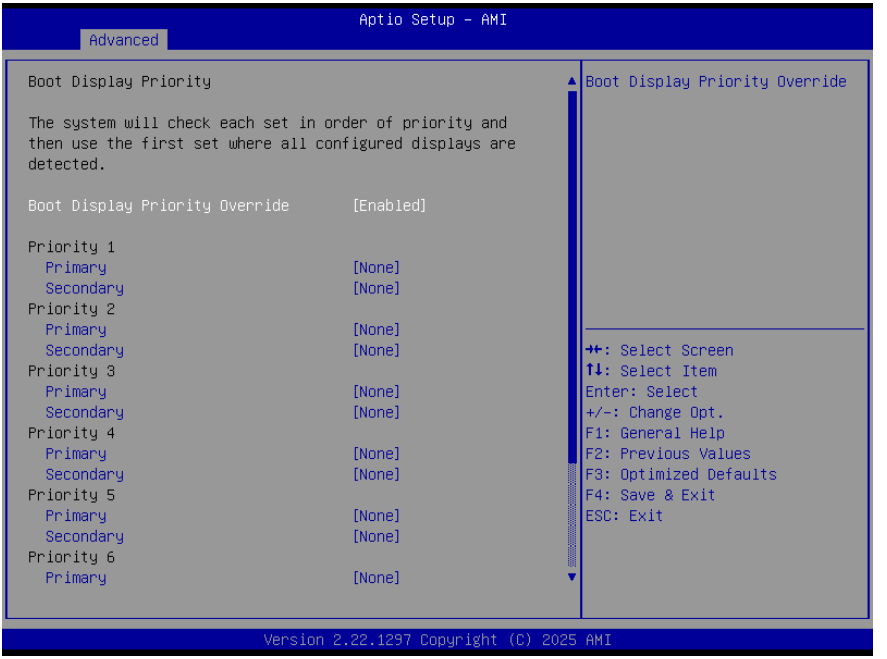
### 3.4.1 Video BIOS Table Configuration



### 3.4.1.1 Boot Display Priority

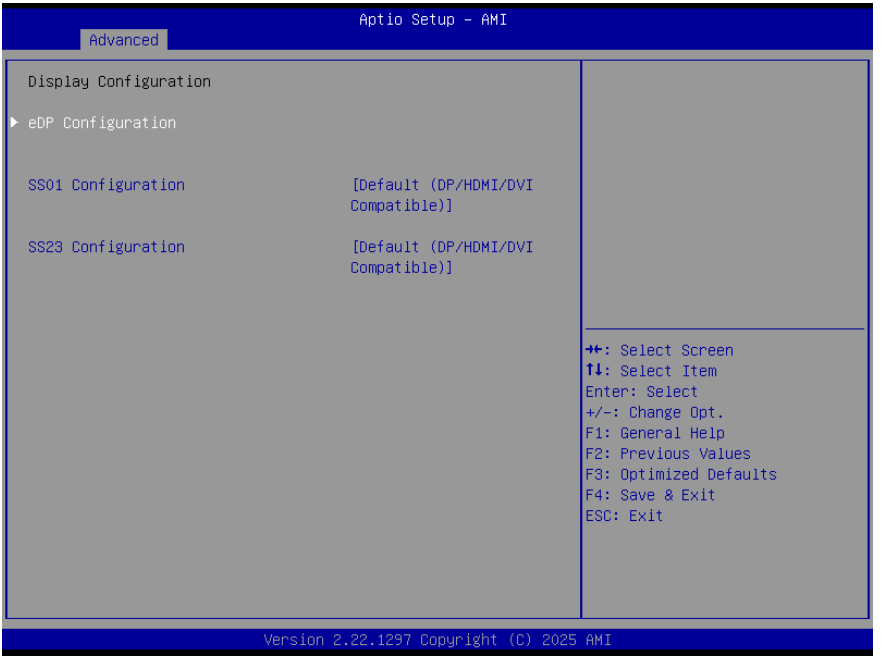

| Options Summary | | |
|---|---|---|
| Boot Display Priority Override | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Boot Display Priority Override. | | |

Set to Enabled



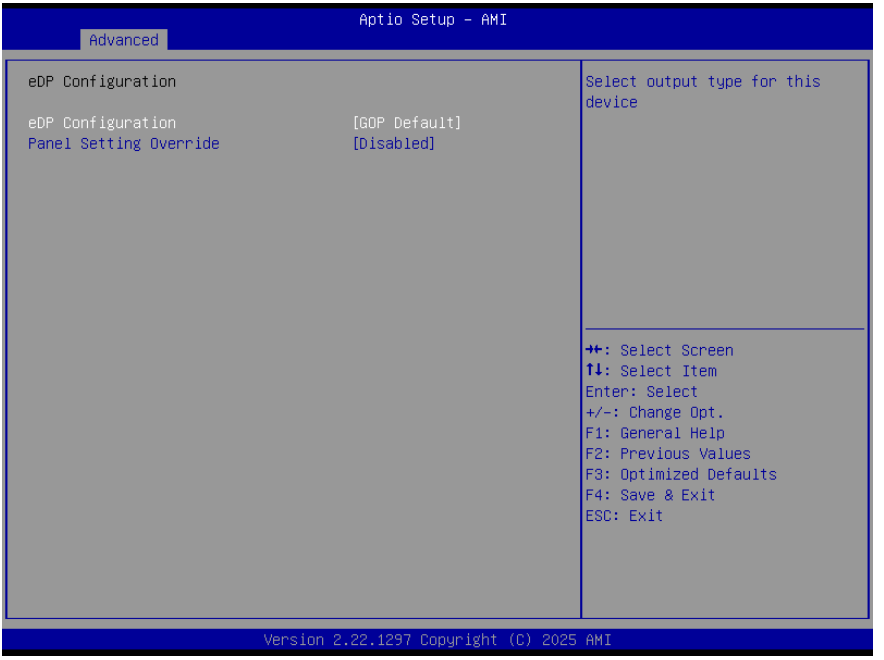

| Options Summary | | |
|---|---|---|
| **Primary** | None | Optimal Default, Failsafe Default |
| | eDP | |
| | SS01 | |
| | SS23 | |
| Primary Boot Display Priority | | |
| **Secondary** | None | Optimal Default, Failsafe Default |
| Secondary Boot Display Priority | | |

### 3.4.1.2 Display Configuration



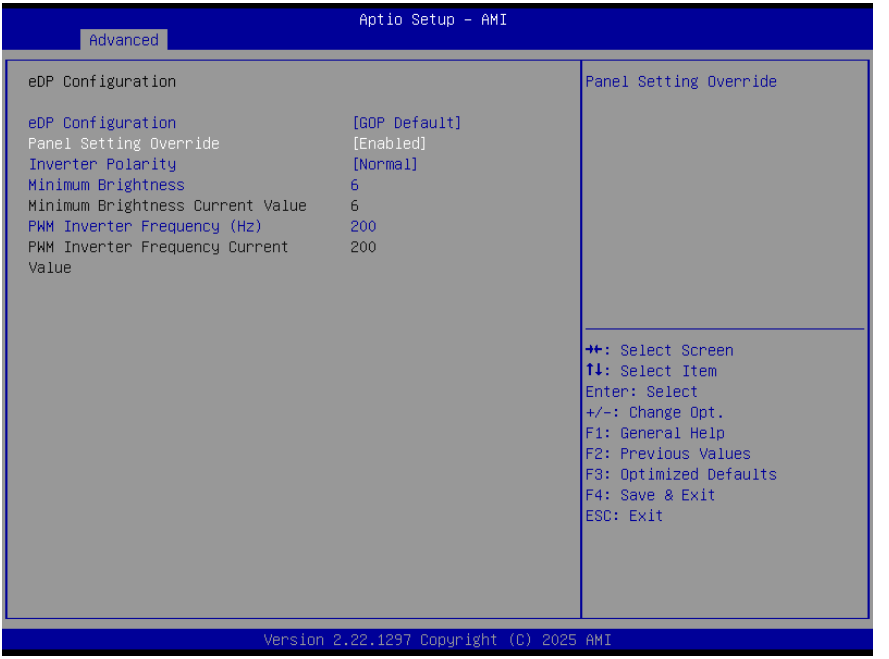

| Options Summary | | |
|---|---|---|
| SS01 Configuration | No Device | |
| | DP | |
| | DP/HDMI/DVI Compatible | |
| | HDMI/DVI | |
| | Default (DP/HDMI/DVI Compatible) | Optimal Default, Failsafe Default |
| Select output type for this device | | |
| SS23 Configuration | No Device | |
| | DP | |
| | DP/HDMI/DVI Compatible | |
| | HDMI/DVI | |
| | Default (DP/HDMI/DVI Compatible) | Optimal Default, Failsafe Default |
| Select output type for this device | | |

### 3.4.1.3 eDP Configuration



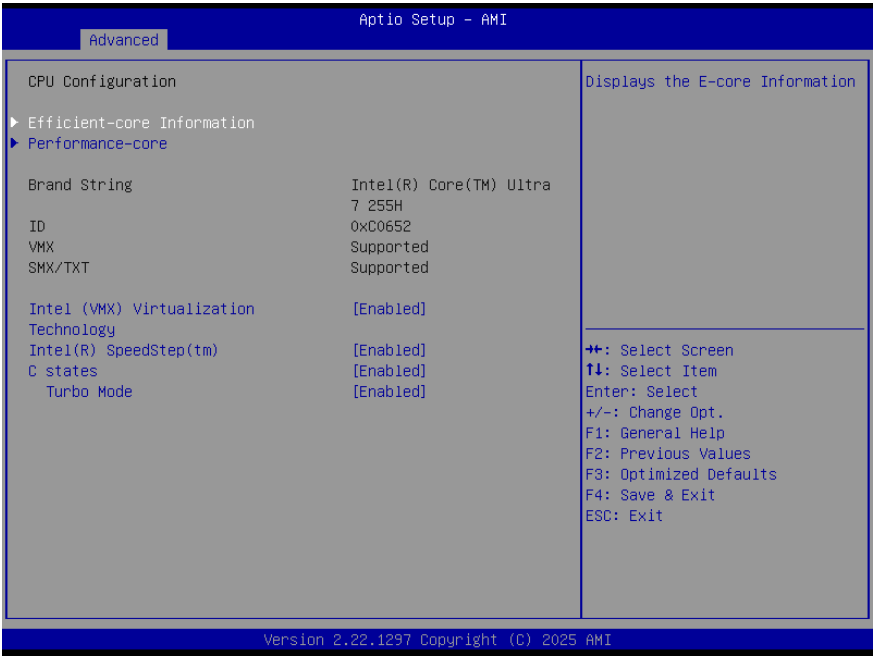

| Options Summary | | |
|---|---|---|
| **eDP Configuration** | No Device | |
| | eDP | |
| | GOP Default | Optimal Default, Failsafe Default |
| eDP Configuration | | |
| **Panel Setting Override** | Enabled | |
| | Disabled | Optimal Default, Failsafe Default |
| Panel Setting Override | | |

Set to Enabled



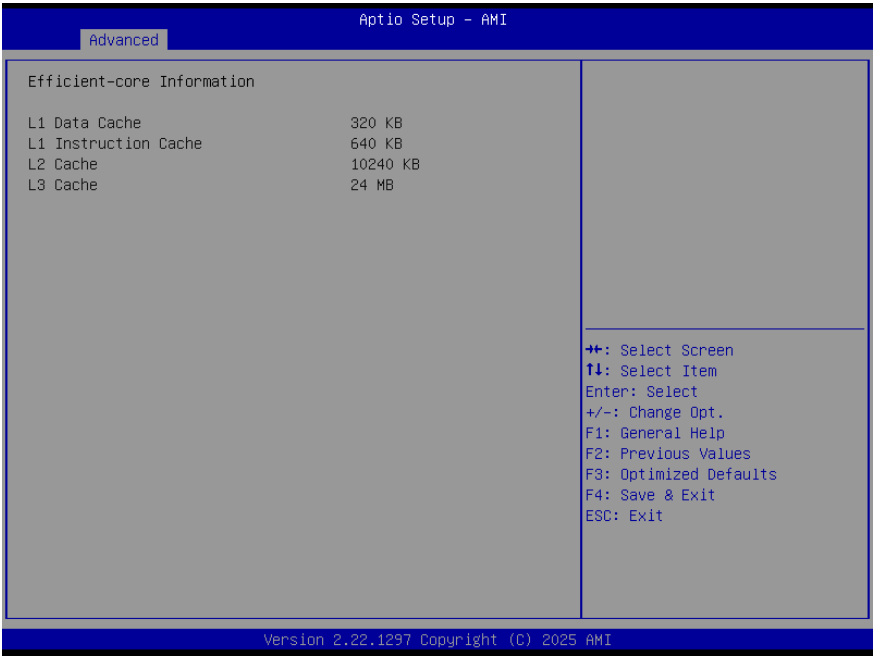

| Options Summary | | |
|---|---|---|
| **Inverter Polarity** | Normal | Optimal Default, Failsafe Default |
| | Inverted | |
| Set Polarity | | |
| **Minimum Brightness** | 6 | Optimal Default, Failsafe Default |
| Minimum Brightness Value | | |
| **PWM Inverter Frequency** | 200 | Optimal Default, Failsafe Default |
| PWM Inverter Frequency (Hz) | | |

## 3.4.2 CPU Configuration

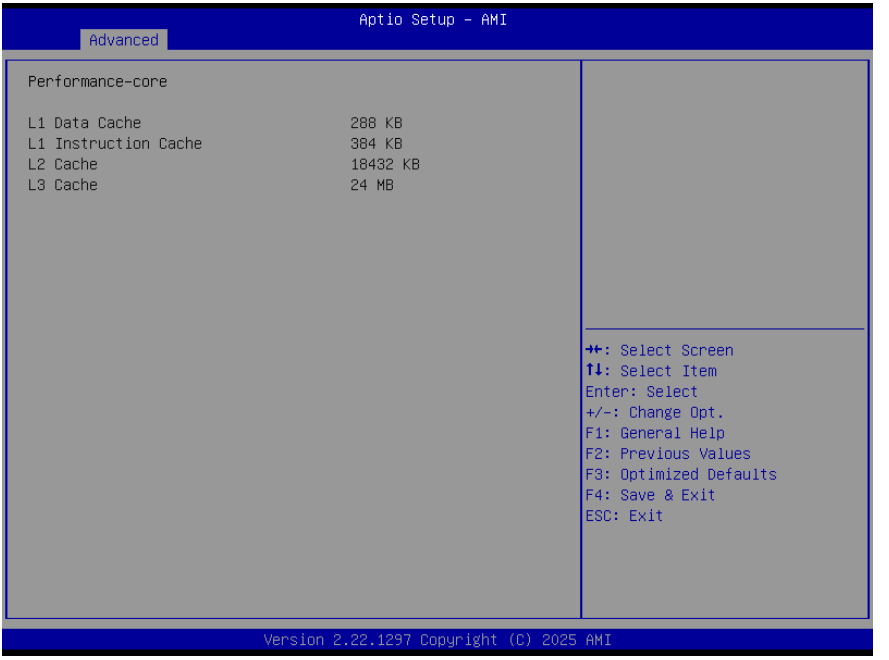



| Options Summary | | |
|---|---|---|
| Intel (VMX) Virtualization Technology | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. | | |
| Intel(R) SpeedStep(tm) | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Allows more than two frequency ranges to be supported. | | |
| C states | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized. | | |
| Turbo Mode | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable processor Turbo Mode. | | |

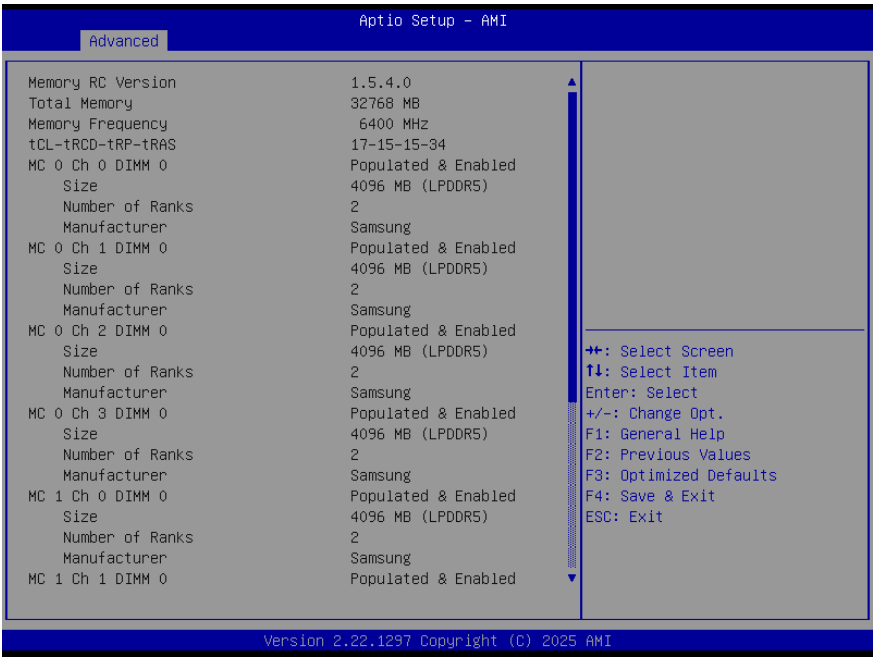
### 3.4.2.1 Efficient-Core Information



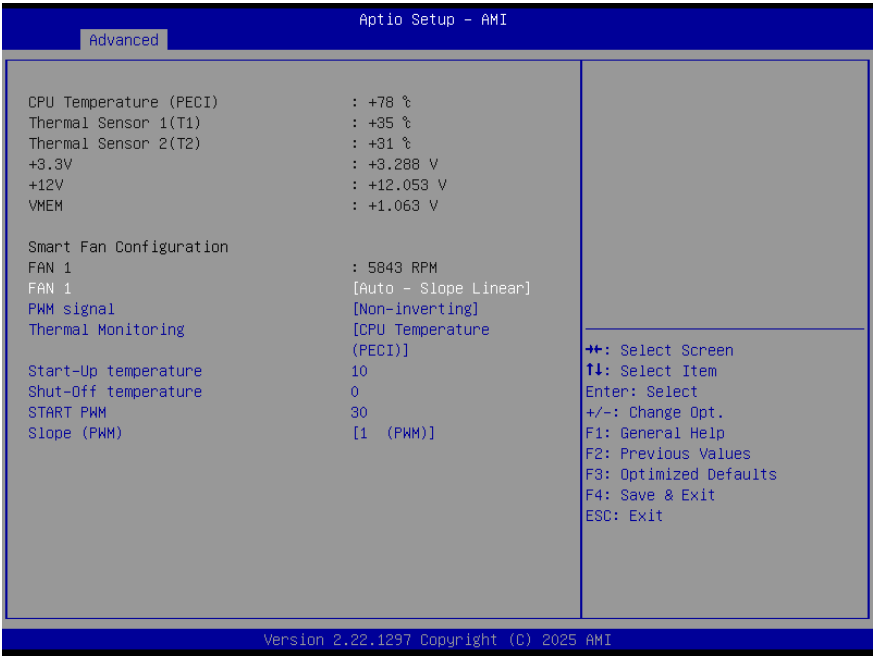
### 3.4.2.2 Performance-Core Information



### 3.4.3 Memory Configuration



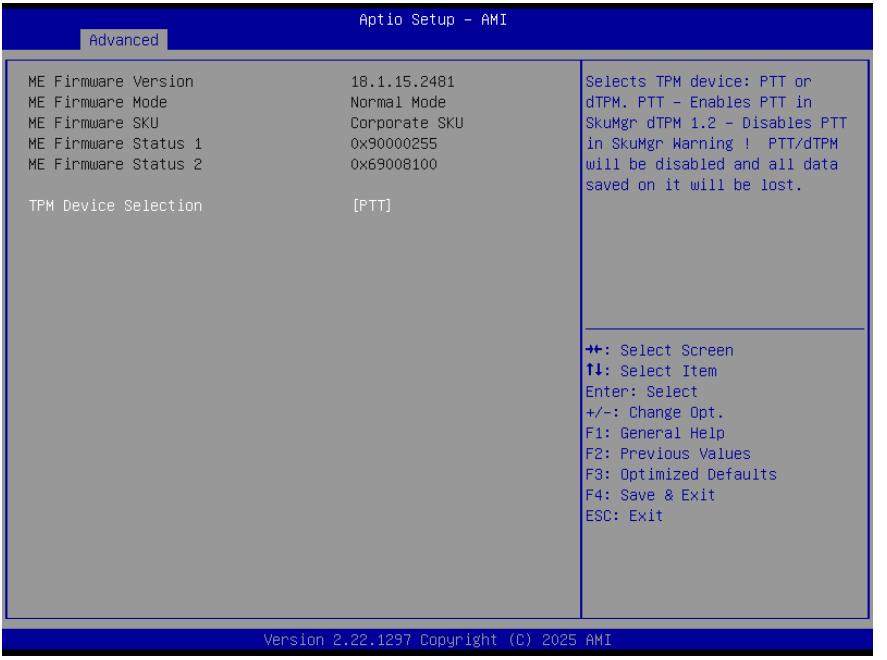
### 3.4.4 On-Module H/W Monitor




| Options Summary | | |
|---|---|---|
| FAN 1 | Full Mode | |
| | Manual Mode | |
| | Auto – Slope Linear | Optimal Default, Failsafe Default |
| Smart Fan Mode Select. | | |
| PWM signal | Non-inverting | Optimal Default, Failsafe Default |
| | Inverting | |
| Select output PWM of inverting or non-inverting signal. | | |
| Thermal Monitoring | CPU Temperature (PECI) | Optimal Default, Failsafe Default |
| | Thermal Source 1 (T1) | |
| | Thermal Source 2 (T2) | |
| Monitoring thermal sensor select. | | |
| Start-Up temperature | 10 | Optimal Default, Failsafe Default |
| Configures PWM output level triggered when the thermal sensor reading goes above the threshold.<br>Range: 0–100. | | |

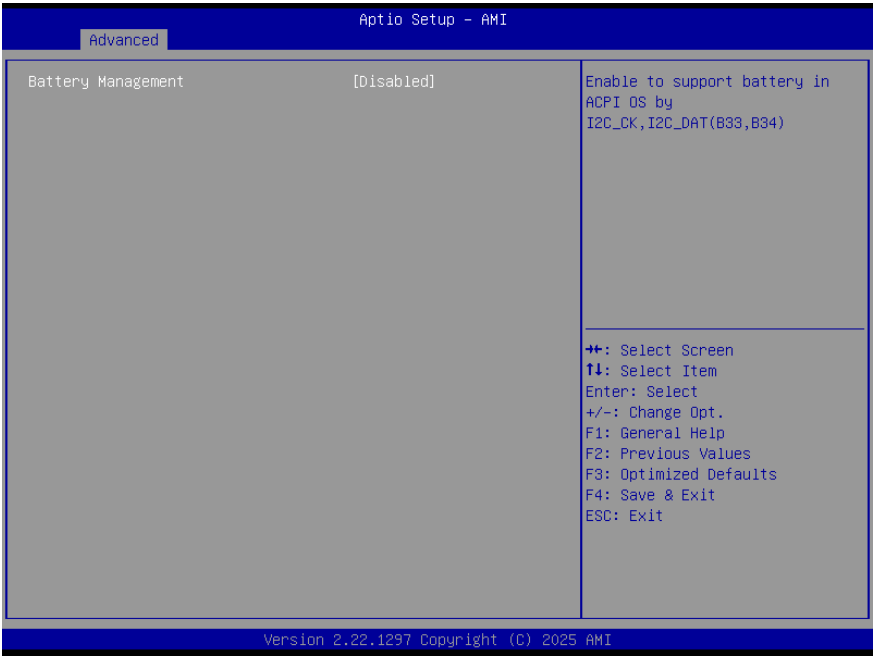
| Options Summary | | |
|---|---|---|
| Shut-Off temperature | 0 | Optimal Default, Failsafe Default |
| PWM output turns off when thermal sensor reading is less than or equal to the threshold.<br>Range: 0–100. | | |
| START PWM | 30 | Optimal Default, Failsafe Default |
| Initial PWM output value when Start-Up temperature is reached. | | |
| Slope (PWM) | 0 (PWM) | |
| | 1 (PWM) | Optimal Default, Failsafe Default |
| | 2 (PWM) | |
| | 4 (PWM) | |
| | 8 (PWM) | |
| | 16 (PWM) | |
| | 32 (PWM) | |
| | 64 (PWM) | |
| When the temperature rises above the Start-Up point, the PWM output increases with each degree. | | |

### 3.4.5 PCH-FW Configuration



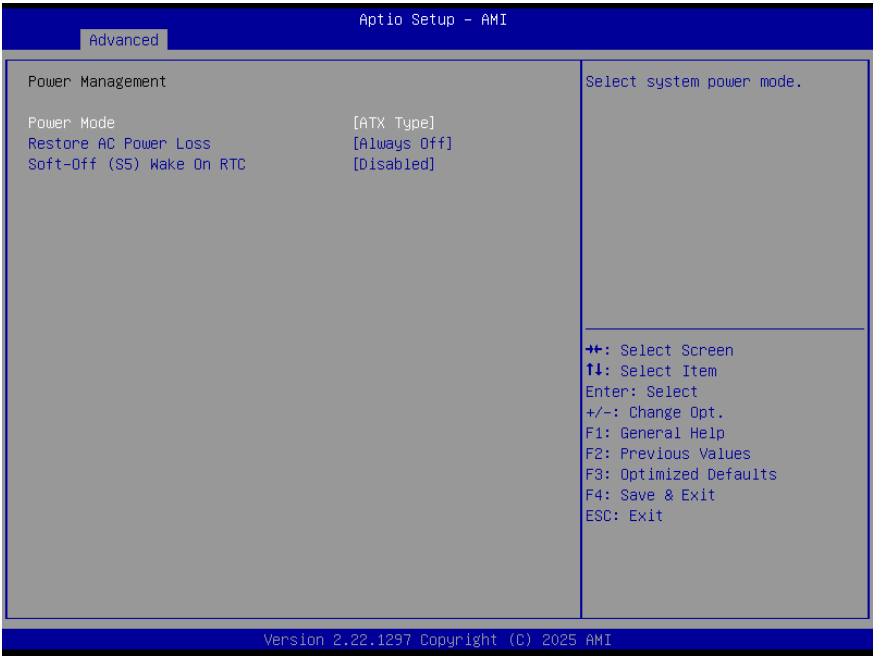

| Options Summary | | |
|---|---|---|
| TPM Device Selection | dTPM | |
| | PTT | Optimal Default, Failsafe Default |
| Selects TPM Device – Choose between PTT or dTPM.<br><br>PTT: Enables PTT in SkuMgr<br><br>dTPM 1.2: Disables PTT in SkuMgr<br><br>**Warning**: Switching between PTT and dTPM will disable the current TPM function, and all data stored in TPM will be lost. | | |

### 3.4.6 On-Module Configuration



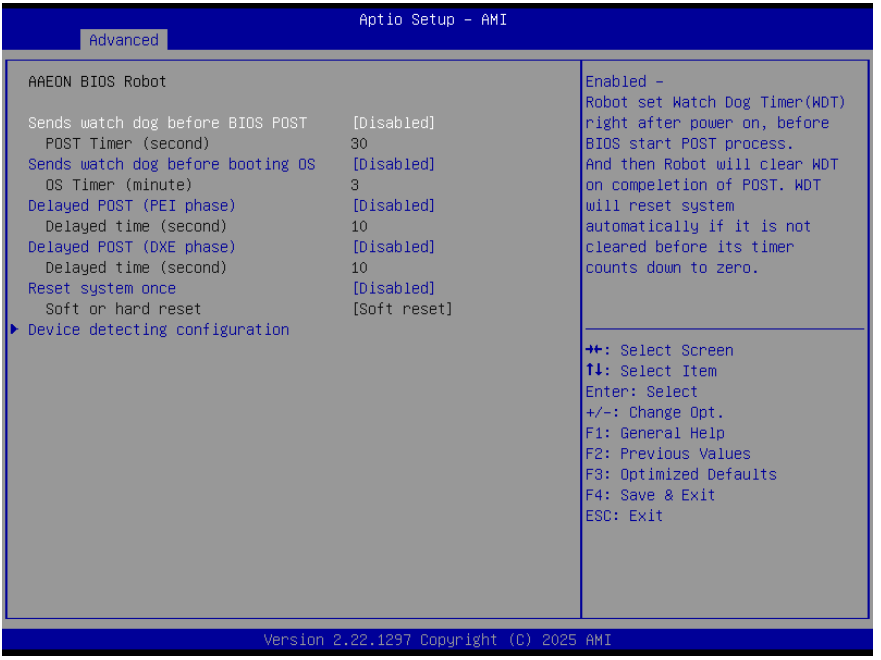

| Options Summary | | |
|---|---|---|
| Battery Management | Disabled | Optimal Default, Failsafe Default |
| | One Battery | |
| Enables battery support in ACPI OS via I2C_CK/I2C_DAT (pins B33, B34). | | |

### 3.4.7 Power Management




| Options Summary | | |
|---|---|---|
| **Power Mode** | ATX Type | Optimal Default, Failsafe Default |
| | AT Type | |
| Select system power mode. | | |
| **Restore AC Power Loss** | Last State | |
| | Always On | |
| | Always Off | Optimal Default, Failsafe Default |
| IO Restore AC power Loss. | | |
| **Soft-Off (S5) Wake On RTC** | Disable | Optimal Default, Failsafe Default |
| | By Date | |
| | By Weekday | |
| | Bypass | |
| By Date: System wakes at the exact date and time specified (hr:min:sec).<br>By Weekday: System wakes on the chosen weekday at the set time (hr:min:sec).<br>Bypass: RTC wake function not managed by BIOS. | | |

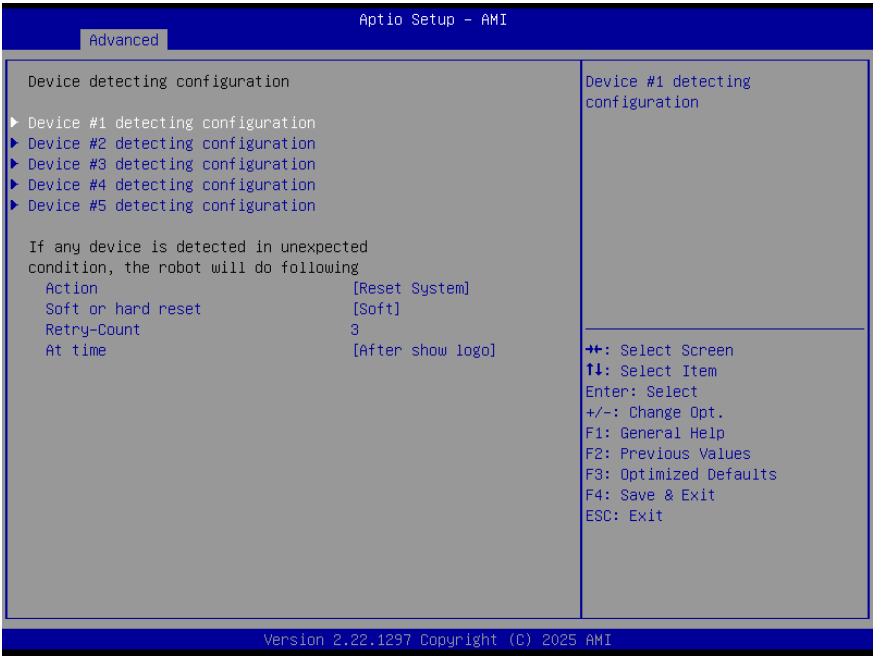
### 3.4.8 AAEON BIOS Robot




| Options Summary | | |
|---|---|---|
| **Sends watch dog before BIOS POST** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled – Robot sets the Watchdog Timer (WDT) immediately after power-on, before BIOS POST. The WDT is cleared once POST completes. If not cleared before timeout, the WDT will automatically reset the system. | | |
| **POST Timer (second)** | 30 | Optimal Default, Failsafe Default |
| WDT Timer Count – Sets the Watchdog Timer duration for POST. ⚠ Warning: Do not set equal to or shorter than normal POST time, or the system may fail to complete POST unless BIOS settings are cleared. Recommended: more than 2× normal POST time. | | |
| **Sends watch dog before booting OS** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled – Robot sets the Watchdog Timer (WDT) after POST, before BIOS transfers control to the OS.<br>**Warning**: The OS must include a program to clear the WDT. Disable this function if the OS will perform updates. | | |

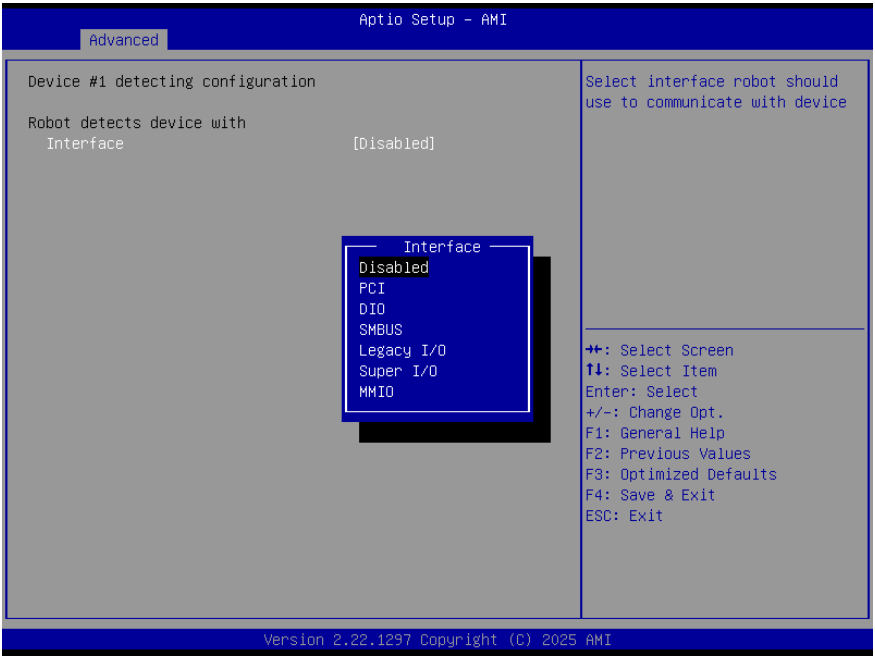
| Options Summary | | |
|---|---|---|
| **OS Timer (minute)** | 3 | Optimal Default, Failsafe Default |
| Sets the Watchdog Timer duration for OS boot/loading. | | |
| **Delayed POST (PEI phase)** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled – Robot delays BIOS POST immediately after power-on, allowing POST to start with stable power or after the system warms up.<br>**Note**: This occurs before "Send Watchdog." | | |
| **Delayed time (second)** | 10 | Optimal Default, Failsafe Default |
| Period of time for Robot to hold BIOS from POST. | | |
| **Delayed POST (DXE phase)** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled – Robot delays BIOS until POST completes, ensuring POST runs with stable power or after system warm-up.<br>**Note**: This occurs after "Send Watchdog before BIOS POST." | | |
| **Delayed time (second)** | 10 | Optimal Default, Failsafe Default |
| Period of time for Robot to hold BIOS from POST. | | |
| **Reset system once** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled – Robot performs a single system reset on each boot, sending a soft or hard reset to onboard devices to ensure a more stable state. | | |
| **Soft or hard reset** | Soft reset | Optimal Default, Failsafe Default |
| | Hard reset | |
| Select reset type robot should send on each boot. | | |

### 3.4.8.1 Device Detecting Configuration



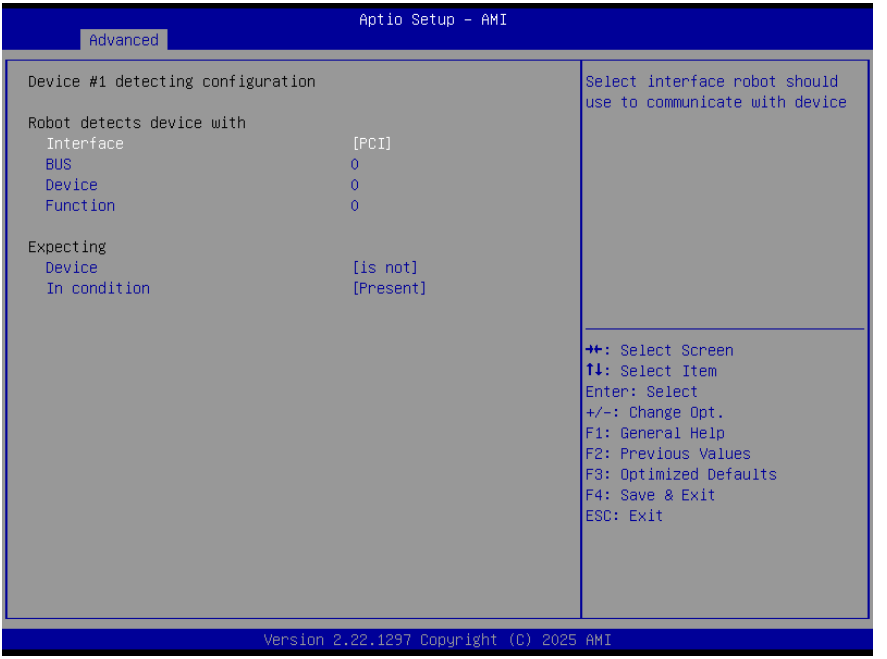

| Options Summary | | |
|---|---|---|
| Action | Reset System | Optimal Default, Failsafe Default |
| | Hold System | |
| Select action that robot should do. | | |
| Soft or hard reset | Soft | Optimal Default, Failsafe Default |
| | Hard | |
| Select reset type robot should send on each boot. | | |
| Retry-Count | 3 | Optimal Default, Failsafe Default |
| Sets the maximum number of system resets the Robot will perform before allowing POST to continue. | | |
| At time | After show logo | Optimal Default, Failsafe Default |
| | Before show logo | |
| Select Robot Action Time – Choose when the Robot performs its action:<br>After Show Logo – Executes after the logo is displayed; most system devices are ready.<br>Before Show Logo – Executes earlier, before logo display; some devices may not be ready. | | |

### 3.4.8.2 Device #1 Detecting Configuration



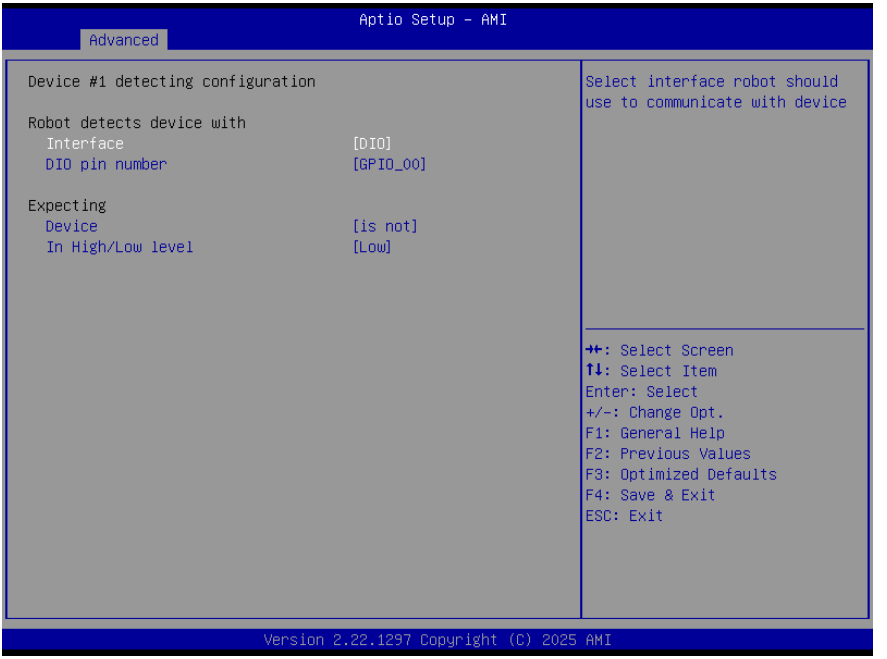

| Options Summary | | |
|---|---|---|
| Interface | Disabled | Optimal Default, Failsafe Default |
| | PCI | |
| | DIO | |
| | SMBUS | |
| | Legacy I/O | |
| | Super I/O | |
| | MMIO | |
| Select interface robot should use to communicate with device. | | |

Set to PCI




| Options Summary | | |
|---|---|---|
| When interface item set to "PCI" will show below items | | |
| BUS | 0 | Optimal Default, Failsafe Default |
| Fill BUS number to a PCI device, in hexadecimal. Range: 0 – FF. | | |
| Device | 0 | Optimal Default, Failsafe Default |
| Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 – FF. | | |
| Function | 0 | Optimal Default, Failsafe Default |
| Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 – FF. | | |
| Device | is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |
| In condition | Present | Optimal Default, Failsafe Default |
| | Specified register data | |
| Device Check Condition – Select how the Robot verifies a device:<br>Present – Device is detected.<br>According to Register – Robot reads the device register based on configuration.<br>Note: A device is considered Present if the data read is not 0xFF. | | |

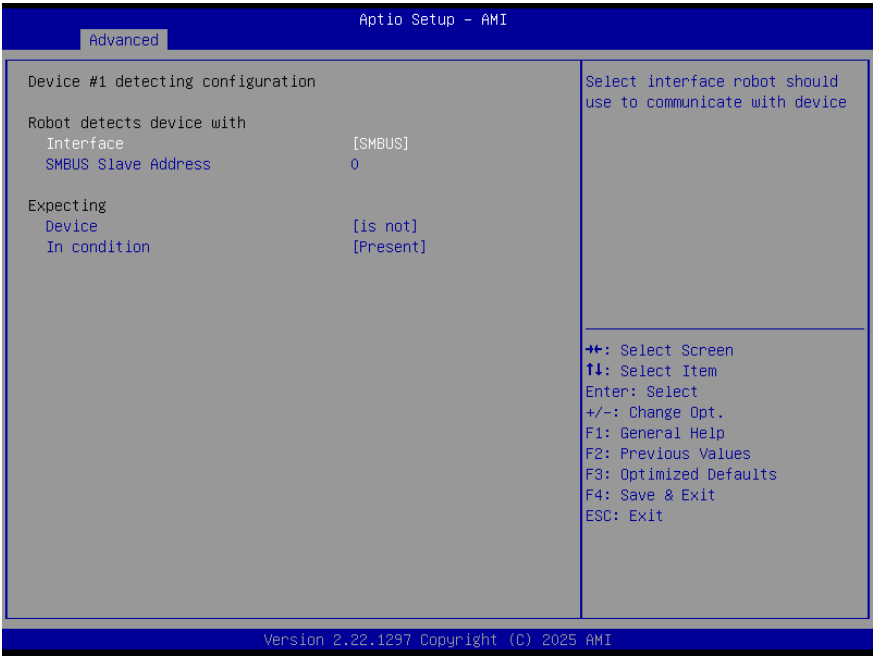
Set to DIO




| Options Summary | | |
|---|---|---|
| When interface item set to "DIO" will show below items | | |
| DIO pin number | GPIO_00 | Optimal Default, Failsafe Default |
| | GPIO_01 | |
| | GPIO_02 | |
| | GPIO_03 | |
| | GPIO_04 | |
| | GPIO_05 | |
| | GPIO_06 | |
| | GPIO_07 | |
| DIO Pin Number – Assign the DIO pin for Robot actions.<br>For COM Express products:<br>0 – 3 → GPI0 – 3<br>4 – 7 → GPO0 – 3 | | |
| Device | is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |

| Options Summary | | |
|---|---|---|
| When interface item set to "DIO" will show below items | | |
| In High/Low level | Low | Optimal Default, Failsafe Default |
| | High | |
| Select High/Low level of the DIO pin that robot should do action. | | |

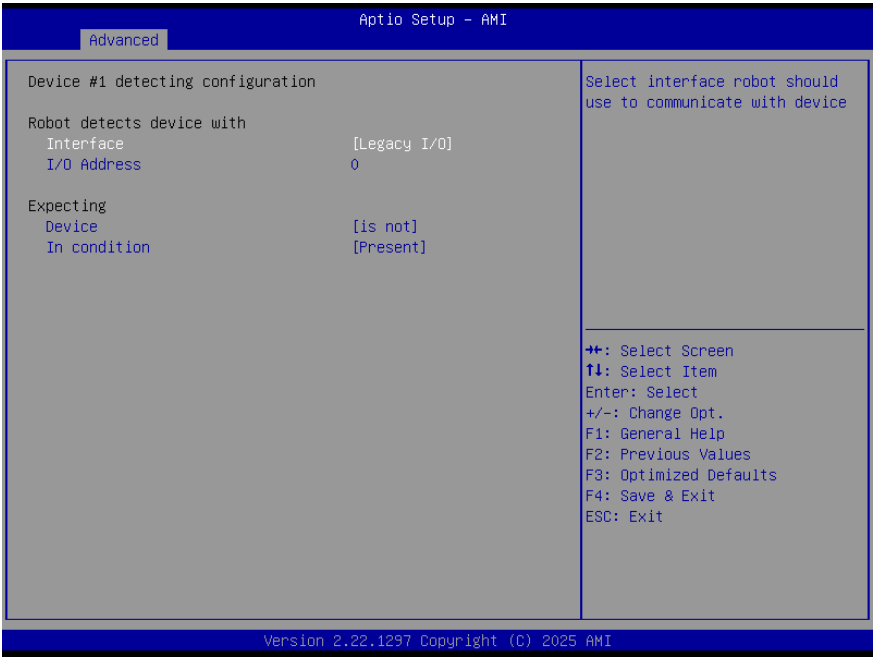
Set to SMBus




| Options Summary | | |
|---|---|---|
| When interface item set to "SMBUS" will show below items | | |
| SMBUS Slave Address | 0 | Optimal Default, Failsafe Default |
| Fill slave address to a SMBUS device, in hexadecimal. Range: 0 - FF | | |
| Device | is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |
| In condition | Present | Optimal Default, Failsafe Default |
| | Specified register data | |
| Device Check Condition – Select how the Robot verifies a device:<br>Present – Device is detected. | | |

| Options Summary |
|---|
| When interface item set to "SMBUS" will show below items |
| According to Register – Robot reads the device register based on configuration.<br>**Note**: A device is considered Present if the data read is not 0xFF. |

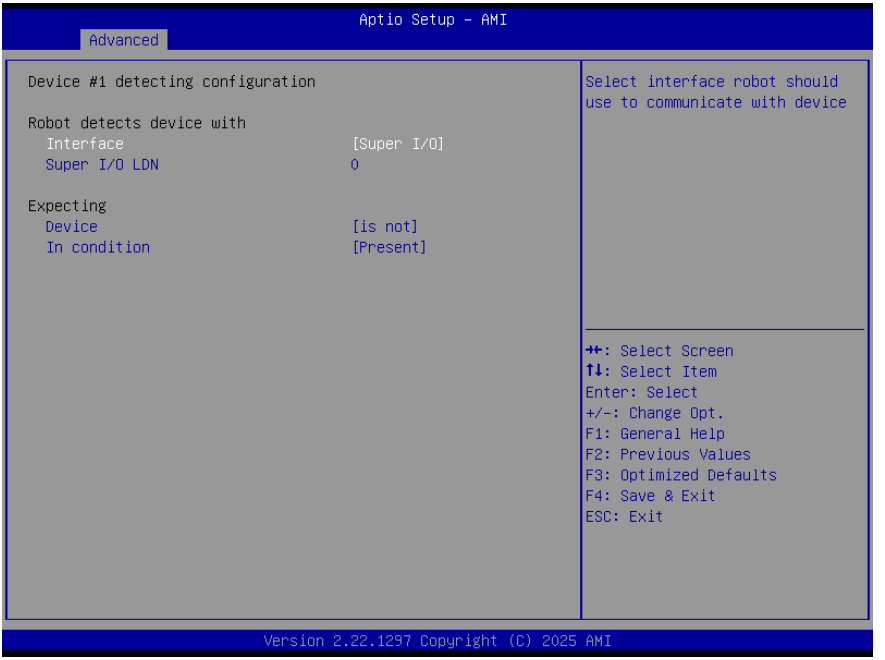
Set to Legacy I/O




| Options Summary | | |
|---|---|---|
| When interface item set to "Legacy I/O" will show below items | | |
| I/O Address | 0 | Optimal Default, Failsafe Default |
| Fill I/O address device is responding to. Range: 0~FFFF. | | |
| Device | is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |
| In condition | Present | Optimal Default, Failsafe Default |
| | Specified register data | |
| Device Check Condition – Select how the Robot verifies a device:<br>Present – Device is detected.<br>According to Register – Robot reads the device register per configuration. | | |

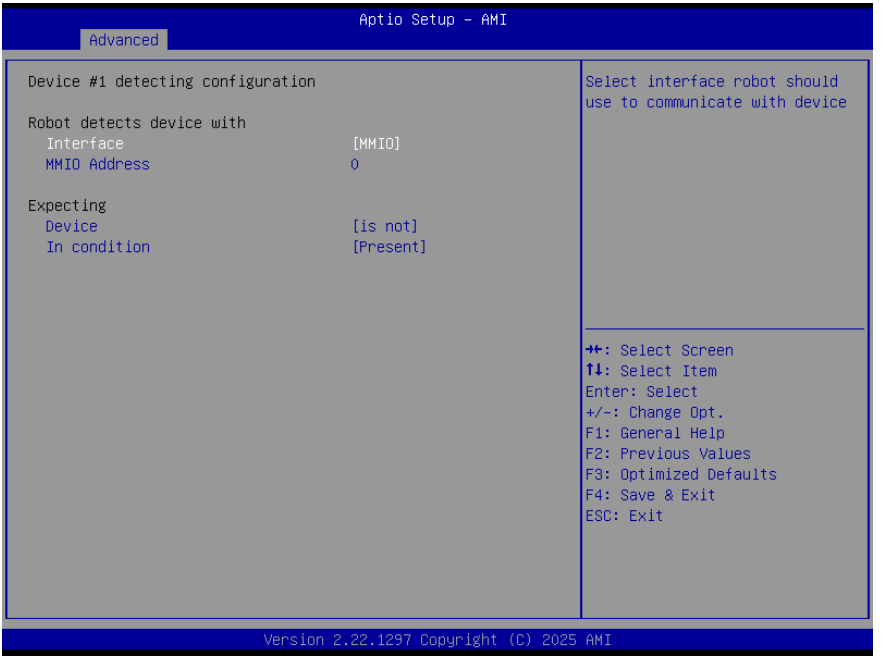
| Options Summary |
| --- |
| When interface item set to "Legacy I/O" will show below items |
| Note: A device is considered Present if the data read is not 0xFF. |

Set to Super I/O



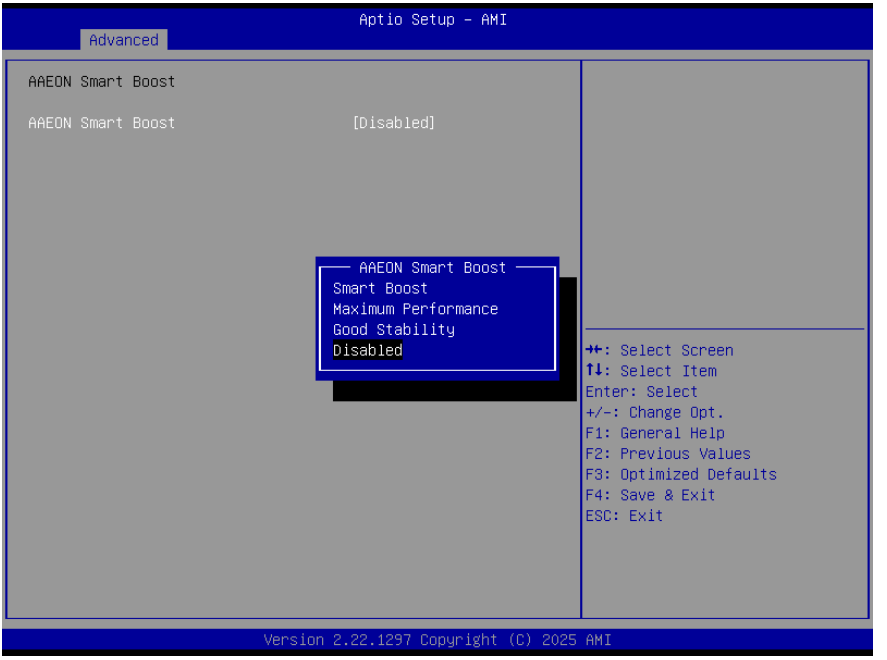

| Options Summary | | |
| --- | --- | --- |
| When interface item set to "Super I/O" will show below items | | |
| Super I/O LDN | 0 | Optimal Default, Failsafe Default |
| Fill LDN number to a Super I/O device. Range: 0~FF. | | |
| Device | Is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |
| In condition | Present | Optimal Default, Failsafe Default |
| | Specified register data | |
| Device Check Condition – Choose how the Robot verifies a device:<br>Present – Device is detected.<br>According to Register – Robot reads the device register per configuration.<br>Note: A device is considered Present if the data read is not 0xFF. | | |

Set to MMIO



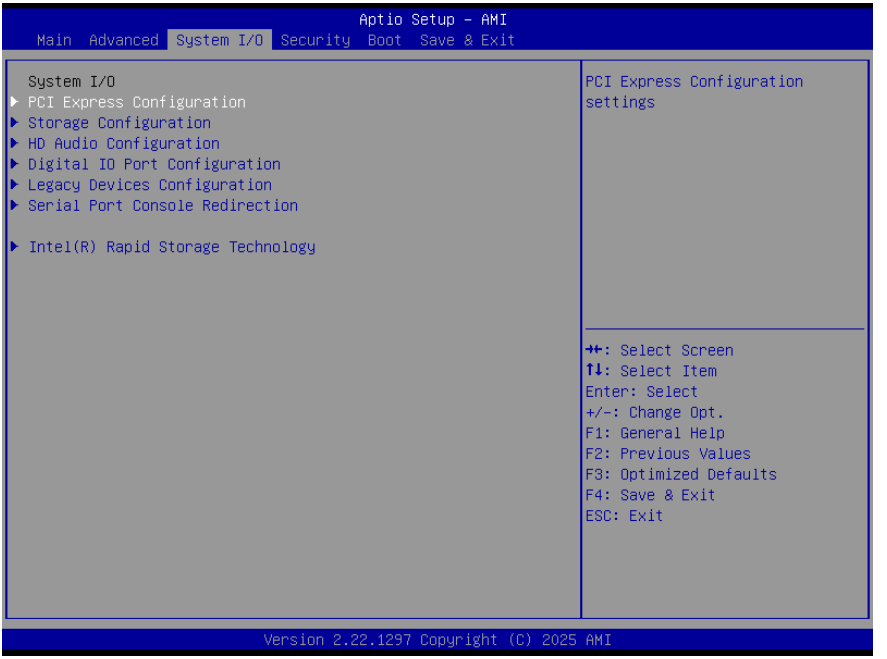

| Options Summary | | |
|---|---|---|
| When interface item set to "MMIO" will show below items | | |
| MMIO Address | 0 | Optimal Default, Failsafe Default |
| Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF. | | |
| Device | is | |
| | Is not | Optimal Default, Failsafe Default |
| Select that robot should or should not do action if condition met. | | |
| In condition | Present | Optimal Default, Failsafe Default |
| | Specified register data | |
| Device Check Condition – Select how the Robot verifies a device:<br>Present – Device is detected.<br>According to Register – Robot reads the device register per configuration.<br>Note: The device is considered Present if the data read is not 0xFF. | | |

### 3.4.9 AAEON Smart Boost

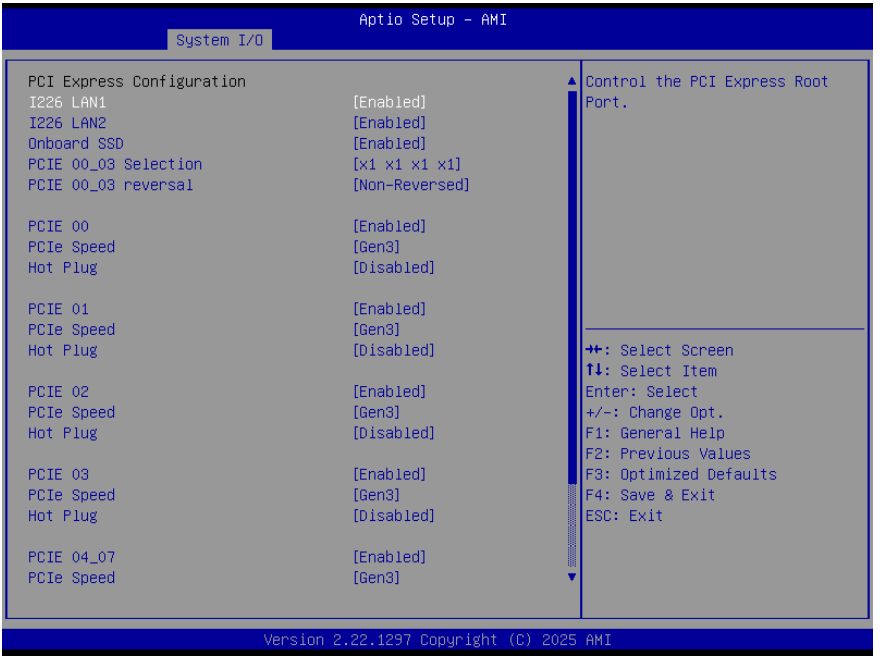



| Options Summary | | |
|---|---|---|
| AAEON Smart Boost | Smart Boost | |
| | Maximum Performance | |
| | Good Stability | |
| | Disable | Optimal Default, Failsafe Default |
| AAEON Smart Boost Mode Select. | | |

## 3.5 Setup Submenu: System I/O



### 3.5.1 PCI Express Configuration



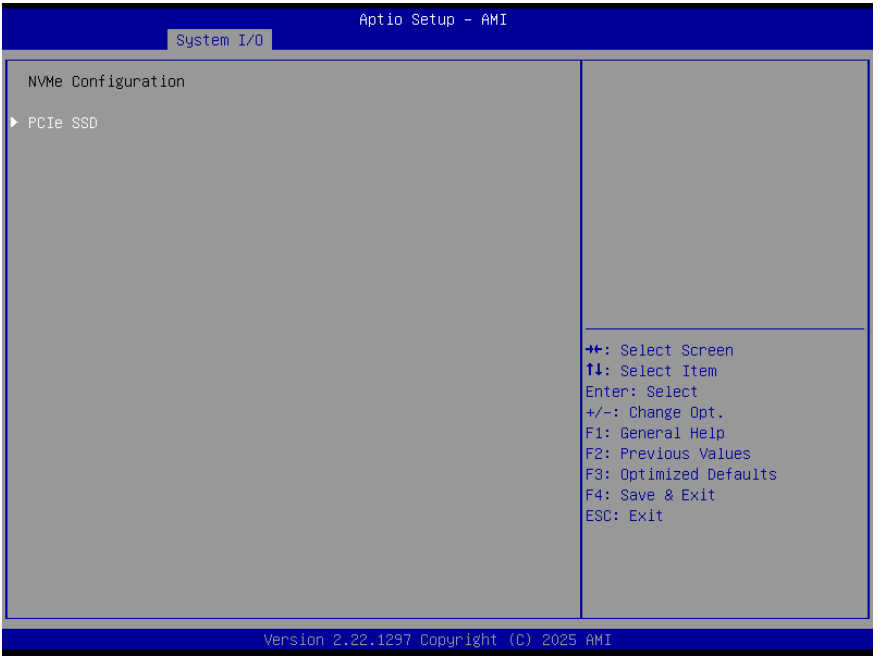

| Options Summary | | |
|---|---|---|
| I226 LAN1 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| I226 LAN1 – Enable or disable the LAN1 interface. | | |
| I226 LAN2 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| I226 LAN1 – Enable or disable the LAN2 interface. | | |
| Onboard SSD | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable the onboard SSD | | |
| PCIe 00_03 Selection | x1 x1 x1 x1 | Optimal Default, Failsafe Default |
| | X2 x1 x1 | |
| | x2 x2 | |
| | x4 | |
| PCIE Controller Setting | | |
| PCIe 00_03 reversal | Non-Reversed | Optimal Default, Failsafe Default |
| | Reversed | |

| Options Summary | | |
|---|---|---|
| PCIE LANE REVERSAL | | |
| PCIe 00 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | Optimal Default, Failsafe Default |
| | Gen4 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |
| PCIe 01 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | Optimal Default, Failsafe Default |
| | Gen4 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |
| PCIe 02 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | Optimal Default, Failsafe Default |
| | Gen4 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |
| PCIe 03 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |

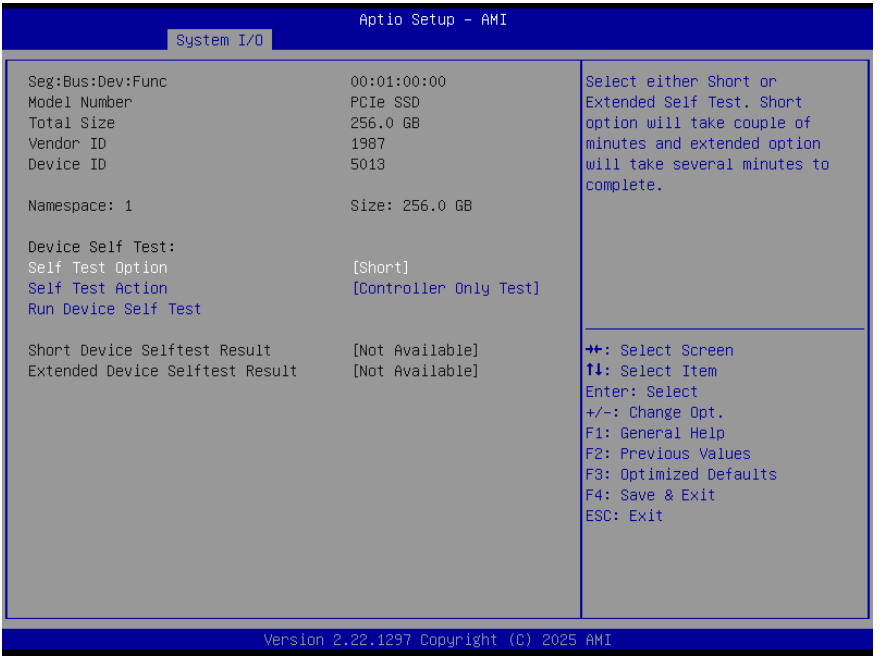
| Options Summary | | |
|---|---|---|
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | Optimal Default, Failsafe Default |
| | Gen4 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |
| PCIe 04_07 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | Optimal Default, Failsafe Default |
| | Gen4 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |
| PCIe 08_15 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control the PCI Express Root Port. | | |
| PCIe Speed | Auto | |
| | Gen1 | |
| | Gen2 | |
| | Gen3 | |
| | Gen4 | Optimal Default, Failsafe Default |
| | Gen5 | |
| Configure PCIe Speed. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| PCI Express Hot Plug Enable/Disable. | | |

### 3.5.2 Storage Configuration

### 3.5.3 NVMe Configuration

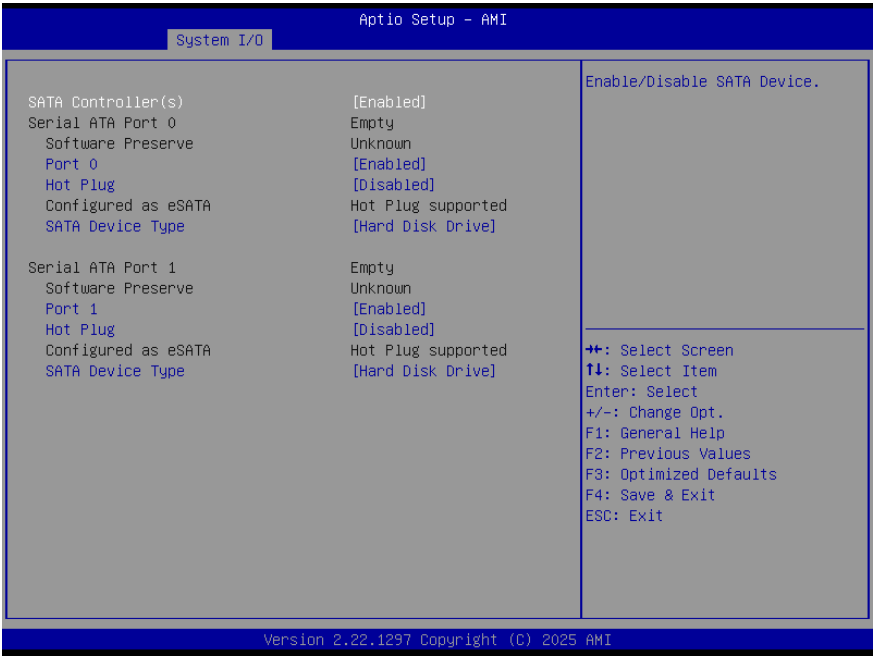


### 3.5.3.1 PCIe SSD



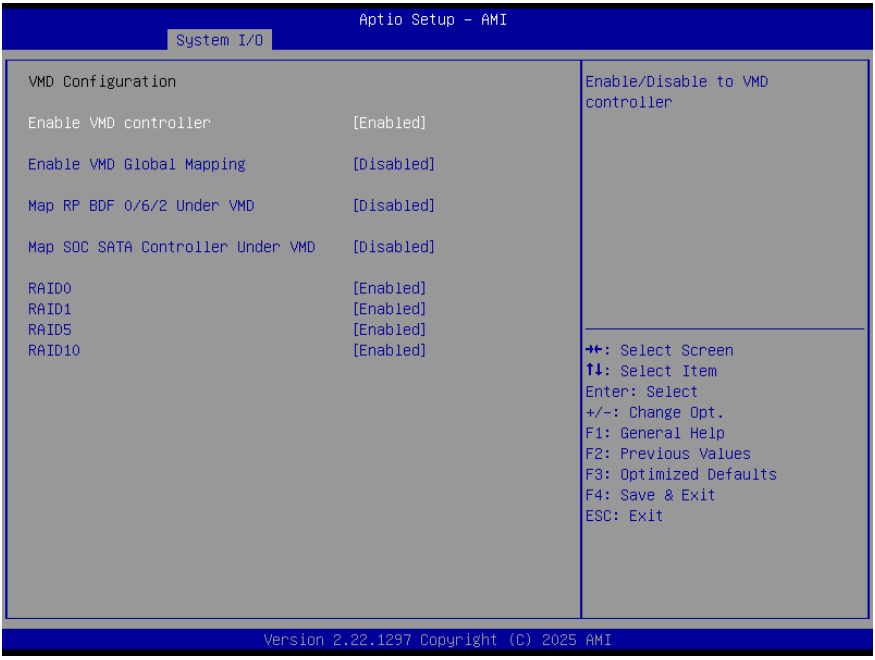

| Options Summary | | |
|---|---|---|
| **Self Test Option** | Short | Optimal Default, Failsafe Default |
| | Extended | |
| Set Option for Self Test | | |
| **Self Test Action** | Controller Only Test | Optimal Default, Failsafe Default |
| | Controller and NameSpace Test | |
| Set Action for Self Test | | |

### 3.5.3.2 SATA Configuration




| Options Summary | | |
|---|---|---|
| SATA Controller(s) | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable SATA Device. | | |
| Port 0~1 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable SATA Port. | | |
| Hot Plug | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Designates this port as Hot Pluggable. | | |
| SATA Device Type | Hard Disk Drive | Optimal Default, Failsafe Default |
| | Solid State Drive | |
| Detects whether the connected SATA port has a Solid-State Drive (SSD) or Hard Disk Drive (HDD). | | |

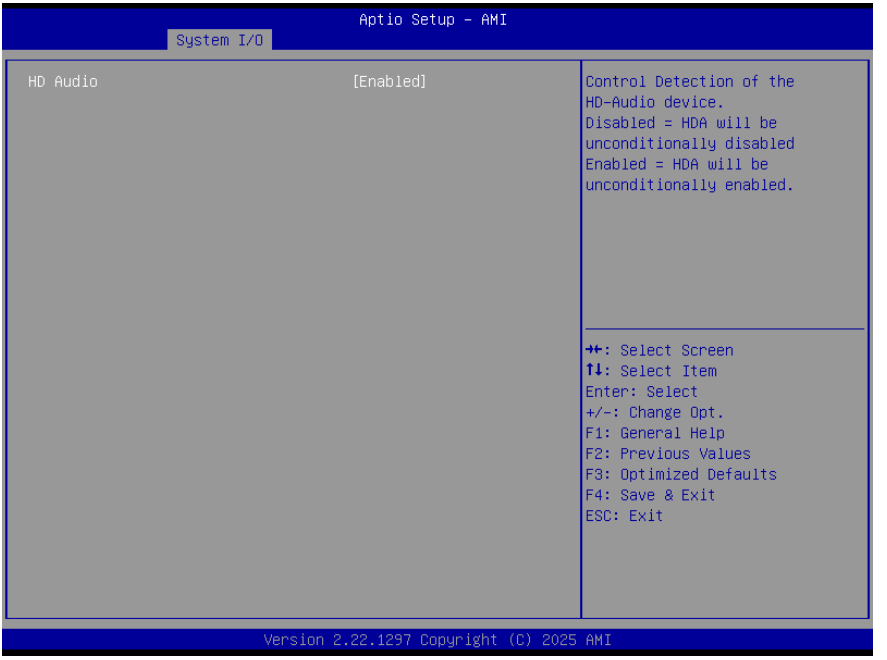
### 3.5.3.3 VMD Setup Menu




| Options Summary | | |
|---|---|---|
| **Enable VMD controller** | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable VMD controller | | |
| **Enable VMD Global Mapping** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable VMD Global Mapping | | |
| **Map RP BDF 0/6/2 Under VMD** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable Map RP BDF 0/6/2 Under VMD | | |
| **Map SOC SATA Controller Under VMD** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable Map SOC SATA Controller Under VMD | | |
| **RAID0** | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable RAID0 Support | | |

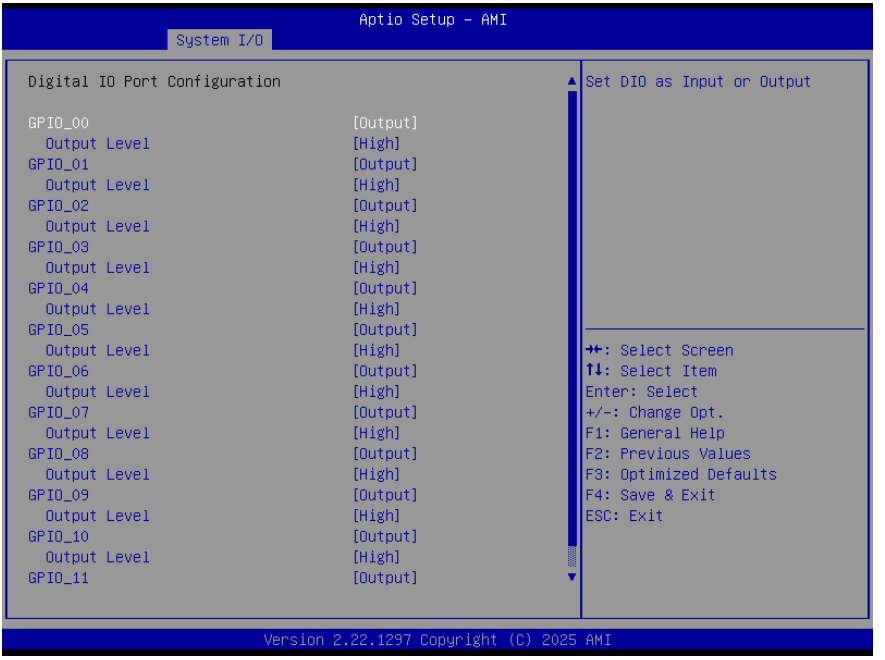
| Options Summary | | |
|---|---|---|
| RAID1 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable RAID1 Support | | |
| RAID5 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable RAID5 Support | | |
| RAID10 | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable/Disable RAID10 Support | | |

### 3.5.4 HD Audio Configuration



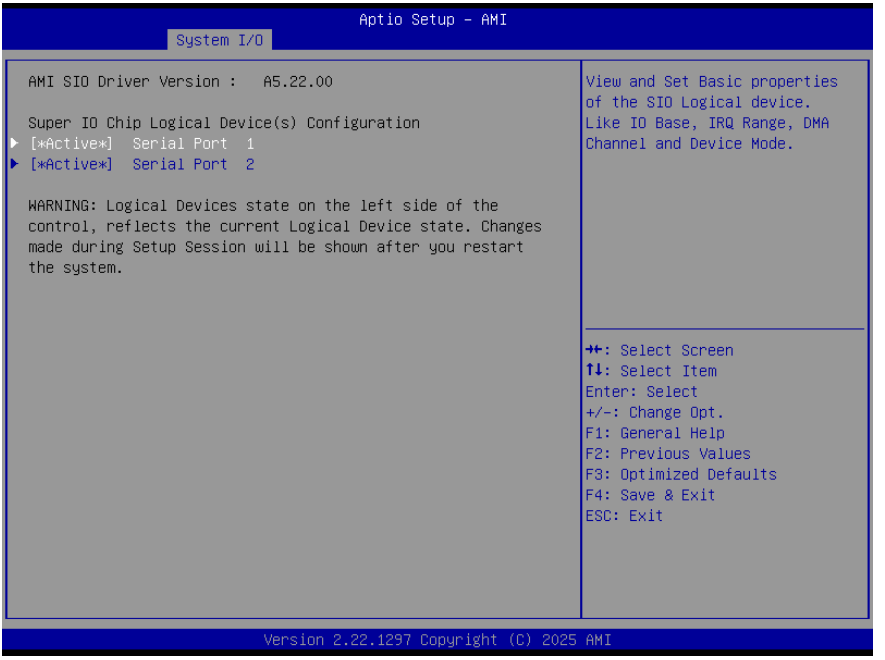

| Options Summary | | |
|---|---|---|
| HD Audio | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or disable detection of the HD-Audio device.<br>Disabled – HDA is unconditionally disabled.<br>Enabled – HDA is unconditionally enabled. | | |

### 3.5.5 Digital IO Port Configuration



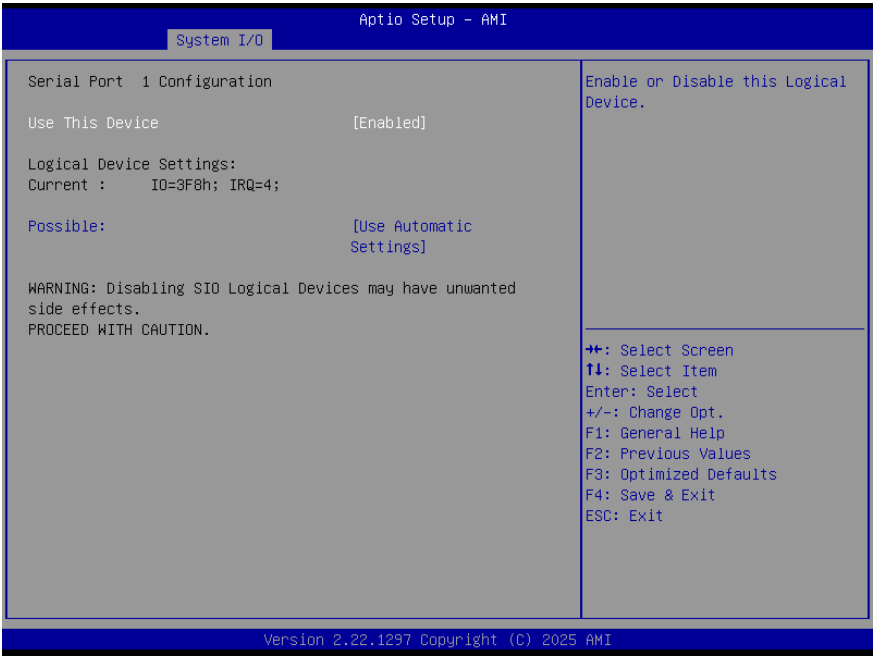

| Options Summary | | |
|---|---|---|
| GPIO_00~11 | Input | |
| | Output | Optimal Default, Failsafe Default |
| Set DIO as Input or Output. | | |
| Output Level | Low | |
| | High | Optimal Default, Failsafe Default |
| Set output level when DIO pin is output. | | |

### 3.5.6 Legacy Logical Devices Configuration



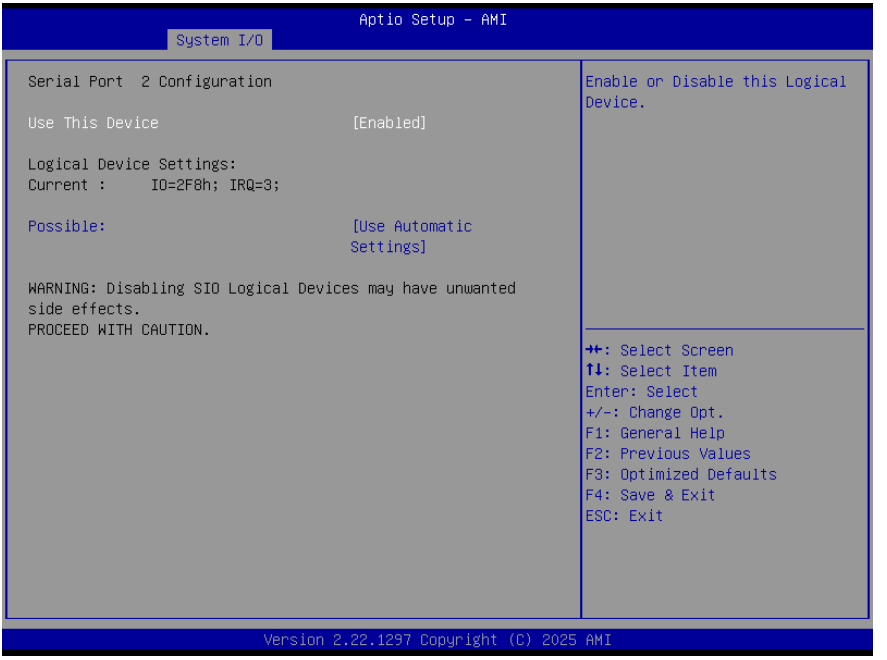

| Options Summary | | |
|---|---|---|
| HD Audio | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Control Detection of the HD-Audio device.<br>Disabled = HDA will be unconditionally disabled.<br>Enabled = HDA will be unconditionally enabled. | | |

### 3.5.6.1 Serial Port 1 Configuration



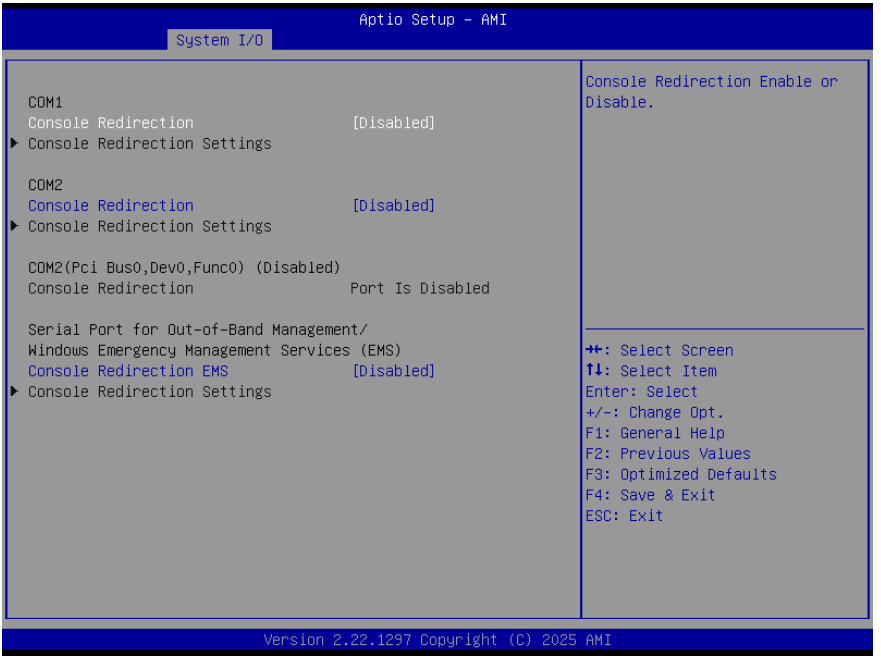

| Options Summary | | |
|---|---|---|
| Use This Device | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable this Logical Device. | | |
| Possible: | Use Automatic Settings | Optimal Default, Failsafe Default |
| | IO=3F8h; IRQ=4; DMA; | |
| | IO=2C8h; IRQ=11; DMA; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |

### 3.5.6.2 Serial Port 2 Configuration



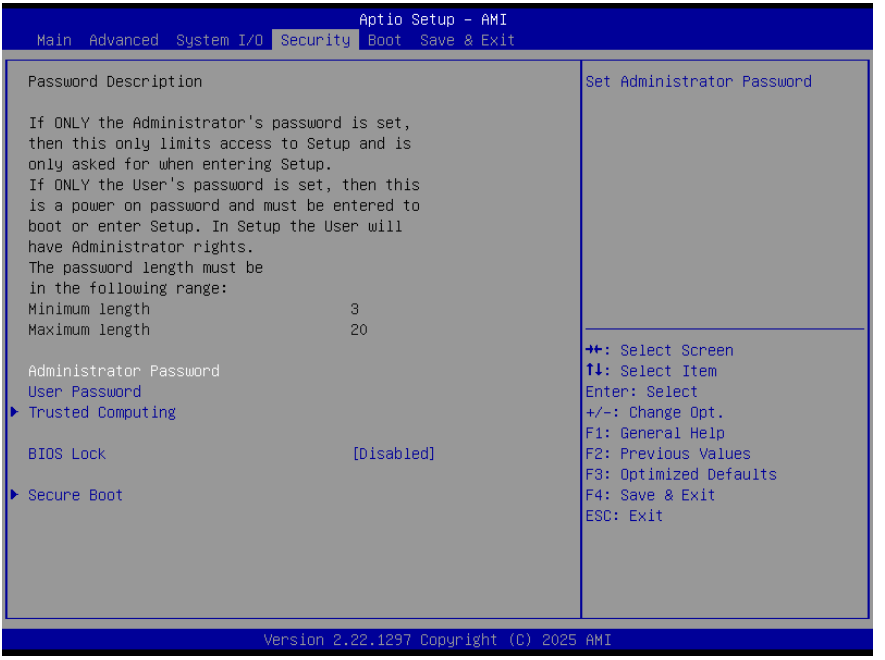

| Options Summary | | |
|---|---|---|
| Use This Device | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable this Logical Device. | | |
| Possible: | Use Automatic Settings | Optimal Default, Failsafe Default |
| | IO=2F8h; IRQ=3; DMA; | |
| | IO=2D8h; IRQ=10; DMA; | |
| Allows user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |

## 3.5.7 Serial Port Console Redirection




| Options Summary | | |
|---|---|---|
| **Console Redirection (COM1)** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Console Redirection Enable or Disable. | | |
| **Console Redirection (COM2)** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Console Redirection Enable or Disable. | | |
| **Console Redirection EMS** | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Console Redirection Enable or Disable. | | |

## 3.6 Setup Submenu: Security




### Change Administrator/User Password

You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility.

Select the password you want to set and press <Enter>. A dialog box will appear which lets you set the password. Passwords must be between 3 and 20 letters or numbers. Press <Enter> and re-enter the password into the next dialog box that appears. Press <Enter> after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

### Remove Password

Highlight this item and type in the current password. At the next dialog box press <Enter> to disable password protection.

| Options Summary | | |
|---|---|---|
| BIOS Lock | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable or disable the PCH BIOS Lock feature. Must be enabled to ensure SMM protection of the flash. | | |

### 3.6.1 Trusted Computing

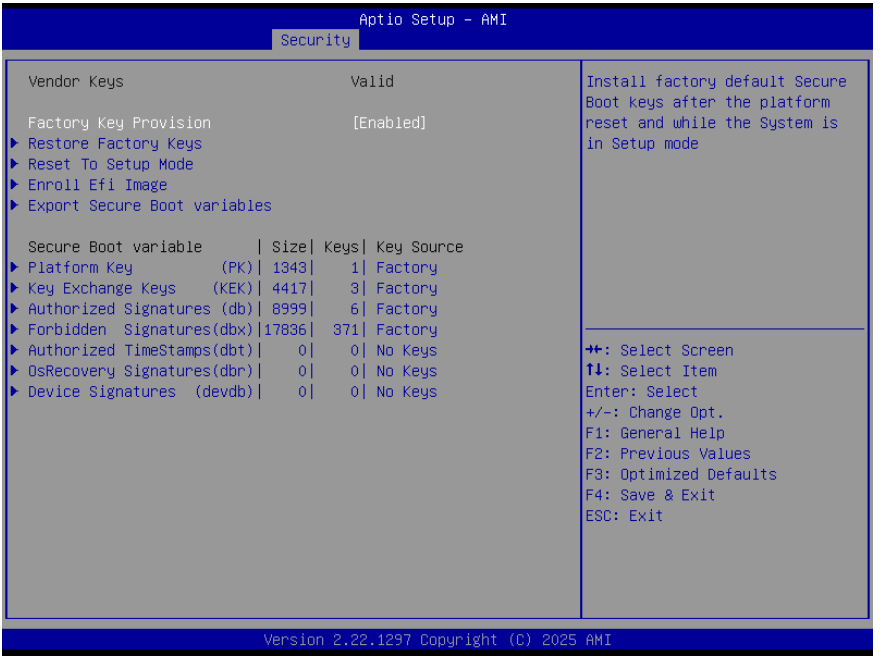

| Options Summary | | |
|---|---|---|
| Security Device Support | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or disable BIOS support for the security device.<br><br>If Disabled, the OS will not detect the Security Device, and TCG EFI protocol and INT1A interface will be unavailable. | | |
| SHA256 PCR Bank | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable SHA256 PCR Bank. | | |

| Options Summary | | |
|---|---|---|
| SHA384 PCR Bank | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable or Disable SHA384 PCR Bank. | | |
| SM3_256 PCR Bank | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable or Disable SM3_256 PCR Bank. | | |
| Pending Operation | None | Optimal Default, Failsafe Default |
| | TPM Clear | |
| Set a scheduled operation for the Security Device.<br>Note: The system will reboot to apply changes to the Security Device state. | | |
| Platform Hierarchy | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or disable Platform Hierarchy. | | |
| Storage Hierarchy | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Storage Hierarchy. | | |
| Endorsement Hierarchy | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enable or Disable Endorsement Hierarchy. | | |
| Physical Presence Spec Version | 1.2 | |
| | 1.3 | Optimal Default, Failsafe Default |
| Select the PPI specification version for OS support: 1.2 or 1.3.<br>Note: Some HCK tests may not support version 1.3. | | |
| Device Select | TPM 1.2 | |
| | TPM 2.0 | |
| | Auto | Optimal Default, Failsafe Default |

## 3.6.2 Secure Boot


| Options Summary | | |
|---|---|---|
| Secure Boot | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. | | |
| Secure Boot Mode | Standard | |
| | Custom | Optimal Default, Failsafe Default |
| Secure Boot mode options: Standard or Custom.<br>In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. | | |
| Restore Factory Keys | | |
| Force System to User Mode. Install factory default Secure Boot key databases. | | |

### 3.6.3 Key Management




| Options Summary | | |
|---|---|---|
| Factory Key Provision | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Installs the factory default Secure Boot keys after platform reset while the system is in Setup mode. | | |
| Restore Factory Keys | | |
| Forces the system into User Mode and installs the factory default Secure Boot key databases. | | |
| Reset to Setup Mode | | |
| Deletes all Secure Boot key databases from NVRAM, placing the system in Setup Mode. | | |
| Export Secure Boot variables | | |
| Saves the NVRAM contents of Secure Boot variables to a file. | | |
| Enroll Efi Image | | |
| Allows the image to run in Secure Boot mode by enrolling its SHA256 hash certificate into the Authorized Signature Database (db). | | |

| Options Summary | |
|---|---|
| Platform Key (PK) | Details |
| | Export |
| | Update |
| | Delete |
| Key Exchange Keys (KEK) | Details |
| | Export |
| | Update |
| | Append |
| | Delete |
| Authorized Signatures (db) | Details |
| | Export |
| | Update |
| | Append |
| | Delete |
| Forbidden Signatures (dbx) | Details |
| | Export |
| | Update |
| | Append |
| | Delete |
| Authorized TimeStamps (dbt) | Update |
| | Append |
| OsRecovery Signatures (dbr) | Update |
| | Append |
| Device Signatures (devdb) | Update |
| | Append |

Enroll Factory Defaults or load certificates from a file:
Public Key Certificate:

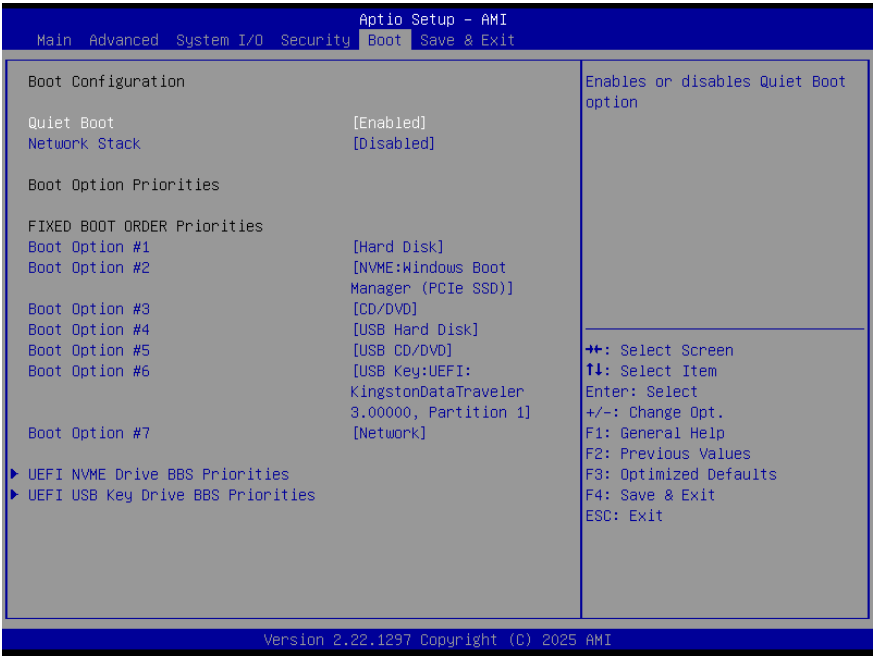
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHAXXX

Authenticated UEFI Variable

EFI PE/COFF Image (SHA256)

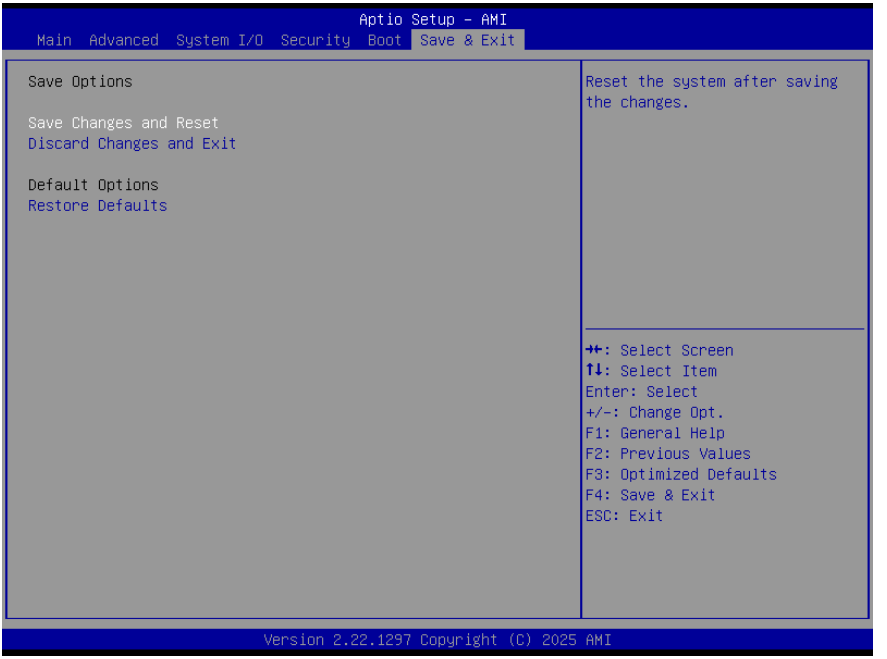
Key Source: Factory, Modified, Mixed

## 3.7 Setup Submenu: Boot




| Options Summary | | |
|---|---|---|
| Quiet Boot | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| Enables or disables Quiet Boot option | | |
| Network Stack | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable UEFI Network Stack. | | |

## 3.8 Setup Submenu: Save & Exit



# Chapter 4

Drivers Installation

## 4.1 Drivers Download and Installation

Drivers for the HPC-ARHm can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en

Download the driver(s) you need and follow the steps below to install them.

### Chipset Driver

1. Open the folder where you unzipped the **Chipset Drivers**
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Graphics Driver

1. Open the folder where you unzipped the **Graphics Drivers**
2. Run the **Installer.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

### LAN Drivers

1. Open the folder where you unzipped the **LAN Drivers**
2. Read the readme file before proceeding. Caution: Some drivers may require firmware updates first.
3. Identify the subfolder that matches your hardware: choose one of **PRO40GB, PRO1000, PRO2500, PROAVF, PROCGB, PROXGB, RDMA**.
4. Open the appropriate folder for your device, then run the executable file in that folder (e.g., setup.exe or [driver_name].exe).
5. Follow the instructions, drivers will be installed automatically.
6. If your device supports management or additional applications, optionally install software from the **APPS** folder.
7. To update firmware, open the **NVMUpdatePackage** folder and follow the instructions in its readme.

### ME Driver

1. Open the folder where you unzipped the **ME & TXE Drivers**
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

### Serial I/O Drivers

1. Open the folder where you unzipped the **Serial I/O Drivers**
2. Identify the drivers you need based on your system hardware:
    i. **iaLPSS2_GPIO2_MTL**
    ii. **iaLPSS2_I2C_MTL**
    iii. **iaLPSS2_13C_MTL**
    iv. **iaLPSS2_SPI_MTL**
    v. **iaLPSS2_UART2_MTL**
3. Open the folder for the driver you want to install.
4. Run the corresponding setup file (e.g., iaLPSS2_GPIO2_MTL.sys or setup.exe if provided), then follow the on-screen instructions; the driver will be installed automatically.
5. Repeat steps 4–6 for each additional driver required by your system.
6. After all drivers are installed, restart to complete the installation.

### Intel® NPU Drivers

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Identify the drivers you need based on your system hardware:
    i. **npu_driver_compiler.dll**
    ii. **npu_extension.dll**
    iii. **npu_level_zero_umd.dll**
    iv. **tbb12.dll**
    v. **tbbmalloc.dll**
    vi. **ze_loader.dll**
    vii. **ze_tracing_layer.dll**
    viii. **ze_validation_layer.dll**
3. Run the setup program if provided, or manually install the .sys and .dll files according to the instructions in the readme.
4. Follow the on-screen instructions; drivers and supporting libraries will be installed automatically.

### Intel® Platform Monitoring Technology Driver

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Locate the **IntcPMT.sys** file.
3. Run the setup program if provided, or manually install the .sys file according to the instructions in the readme.
4. Follow the on-screen instructions; the driver will be installed automatically.

### Intel® GNA Driver

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Locate the **gna.sys** file (system driver) and **gna.pdb** file (debug information).
3. Run the setup program if provided, or manually install the .sys file according to the instructions in the readme.
4. Follow the on-screen instructions; the driver will be installed automatically.

### Realtek Audio Driver

1. Open the folder where you unzipped the **Audio Driver**
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

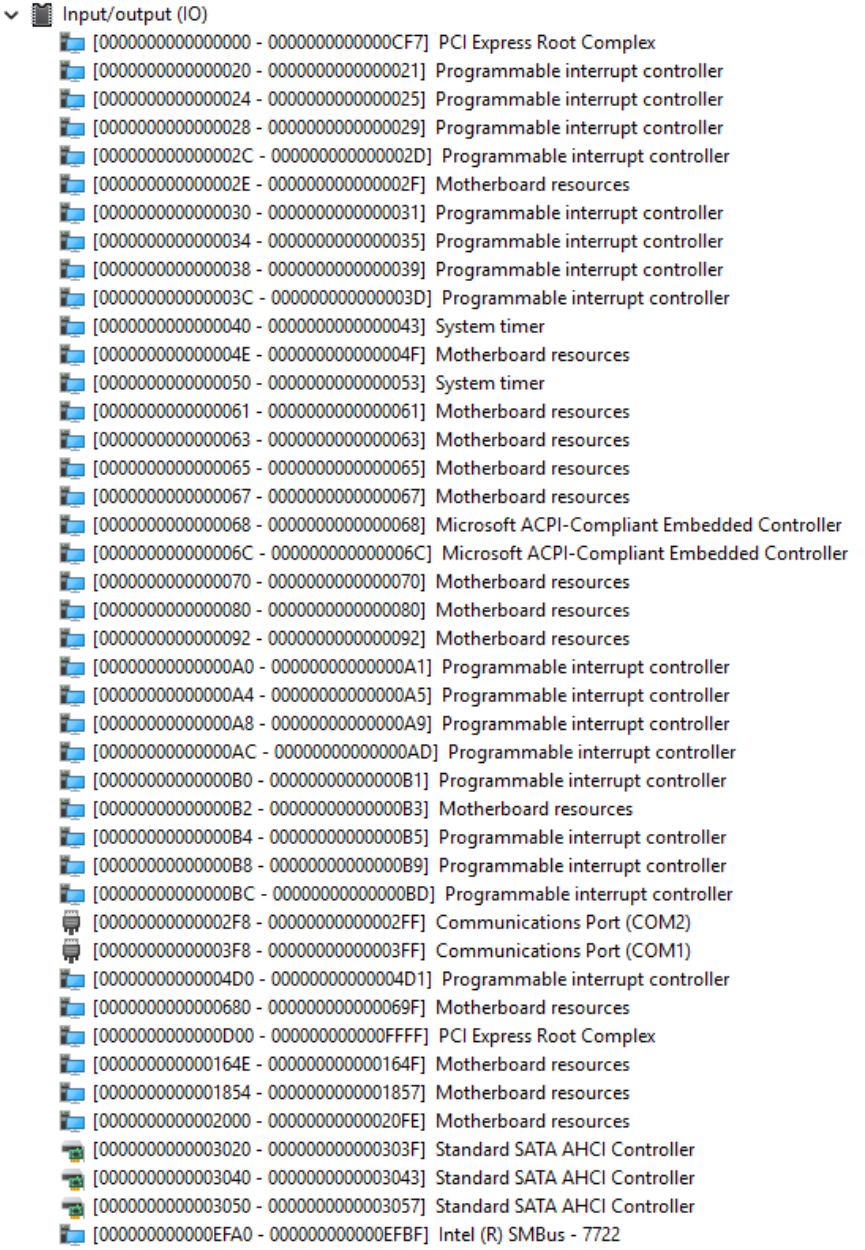
### RAID Driver

1. Open the folder where you unzipped the **RAID Driver**
2. Run the **SetupRST.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

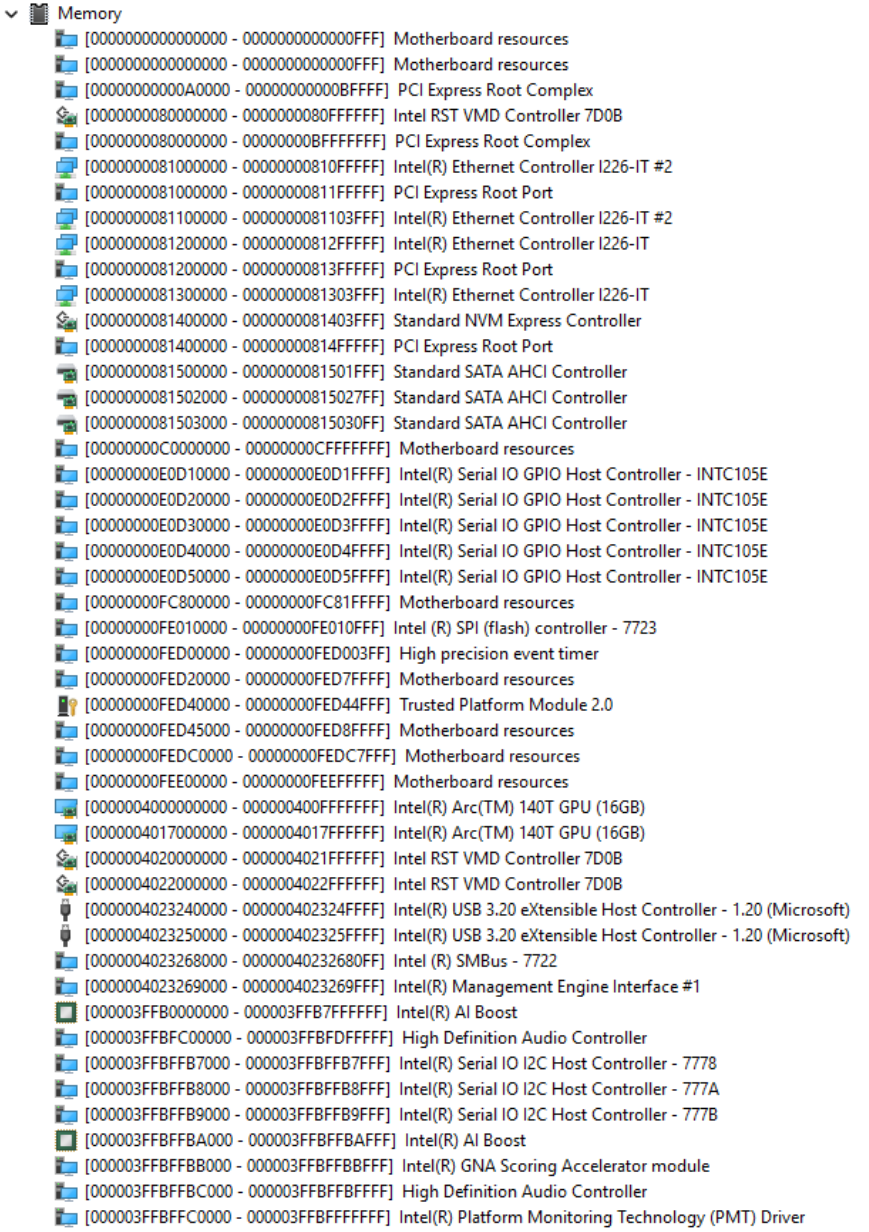
# Appendix A

I/O Information

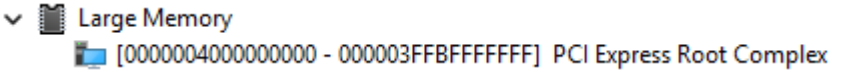
## A.1 I/O Address Map



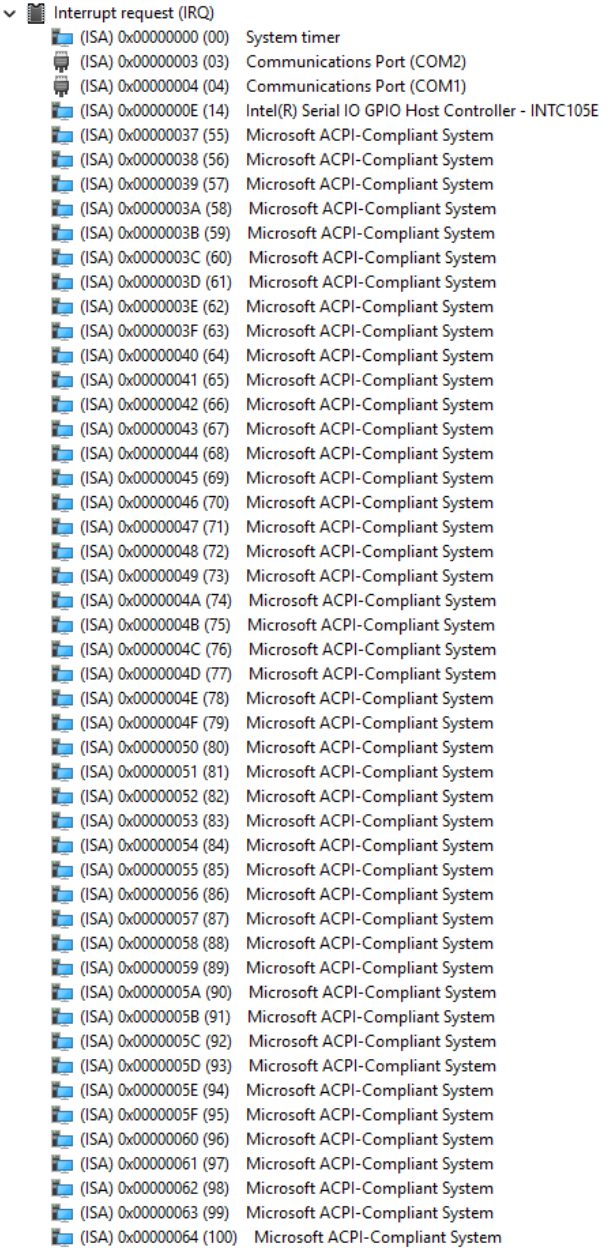
## A.2 Memory Address Map



## A.3 Large Memory Address Map



## A.4 IRQ Mapping Chart



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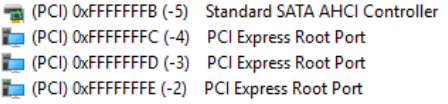
(ISA) 0x000001ED (493) Microsoft ACPI-Compliant System
(ISA) 0x000001EE (494) Microsoft ACPI-Compliant System
(ISA) 0x000001EF (495) Microsoft ACPI-Compliant System
(ISA) 0x000001F0 (496) Microsoft ACPI-Compliant System
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System

(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0x00000020 (32) Intel(R) Serial IO I2C Host Controller - 7778
(PCI) 0x00000022 (34) Intel(R) Serial IO I2C Host Controller - 777A
(PCI) 0x00000023 (35) Intel(R) Serial IO I2C Host Controller - 777B
(PCI) 0xFFFFFFCF (-49) Intel(R) GNA Scoring Accelerator module
(PCI) 0xFFFFFFD0 (-48) Intel(R) AI Boost
(PCI) 0xFFFFFFD1 (-47) Intel(R) Arc(TM) 140T GPU (16GB)
(PCI) 0xFFFFFFD2 (-46) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFD3 (-45) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFD4 (-44) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFD5 (-43) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFD6 (-42) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFD7 (-41) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFD8 (-40) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFD9 (-39) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFDA (-38) Intel(R) Ethernet Controller I226-IT #2
(PCI) 0xFFFFFFDB (-37) Intel(R) Ethernet Controller I226-IT #2
(PCI) 0xFFFFFFDC (-36) Intel(R) Ethernet Controller I226-IT #2
(PCI) 0xFFFFFFDD (-35) Intel(R) Ethernet Controller I226-IT #2
(PCI) 0xFFFFFFDE (-34) Intel(R) Ethernet Controller I226-IT #2
(PCI) 0xFFFFFFDF (-33) Standard NVM Express Controller
(PCI) 0xFFFFFFE0 (-32) Standard NVM Express Controller
(PCI) 0xFFFFFFE1 (-31) Standard NVM Express Controller
(PCI) 0xFFFFFFE2 (-30) Standard NVM Express Controller
(PCI) 0xFFFFFFE3 (-29) Standard NVM Express Controller
(PCI) 0xFFFFFFE4 (-28) Standard NVM Express Controller
(PCI) 0xFFFFFFE5 (-27) Standard NVM Express Controller
(PCI) 0xFFFFFFE6 (-26) Standard NVM Express Controller
(PCI) 0xFFFFFFE7 (-25) Standard NVM Express Controller
(PCI) 0xFFFFFFE8 (-24) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFE9 (-23) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFEA (-22) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFEB (-21) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFEC (-20) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFED (-19) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFEE (-18) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFEF (-17) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF0 (-16) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF1 (-15) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF2 (-14) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF3 (-13) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF4 (-12) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF5 (-11) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF6 (-10) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF7 (-9) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF8 (-8) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFF9 (-7) Intel RST VMD Controller 7D0B
(PCI) 0xFFFFFFFA (-6) Intel RST VMD Controller 7D0B


(PCI) 0xFFFFFFFB (-5) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFC (-4) PCI Express Root Port
(PCI) 0xFFFFFFFD (-3) PCI Express Root Port
(PCI) 0xFFFFFFFE (-2) PCI Express Root Port