GENE-TGU6

3.5" Subcompact Board

User's Manual 2nd Ed

Last Updated: April 12, 2022

Copyright Notice

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
GENE-TGU6 MB	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	3.5" Subcompact Board
CPU	Intel® 11th Generation Core™/ Celeron CPU: Core i7-1185G7E (4C/8T, 1.80GHz, up to 4.40GHz) Core i5-1145G7E (4C/8T, 1.50GHz, up to 4.10GHz) Core i3-1115G4E (2C/4T, 2.20GHz, up to 3.90GHz) Celeron® 6305E (2C/2T, 1.80GHz)
CPU TDP	15W, up to 28W: Core i7-1185G7E Core i5-1145G7E Core i3-1115G4E 15W only: Celeron® 6305E
Chipset	Integrated with Intel® SoC
Memory Type	DDR4 3200MHz, Dual Channel SODIMM x 2
ECC Support	IBECC (select SKUs)
Max Memory Capacity	64GB
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Level
Security	TPM2.0 (Optional)
RTC Battery	Lithium Battery 3V/ 240mAh

Power

Power Requirement	+9 ~ 36V (Optional: +12V)
Power Supply Type	AT/ATX
Connector	Phoenix 2-pin Connector
Power Consumption (Typical)	4.96A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2
Power Consumption (Max)	7.32A at +12V, Intel® i7-1185G7E, DDR4 3200MHz 32GB x 2

Display

Controller	Intel® Iris® Xe Graphics Intel® UHD Graphics
LVDS/ eDP	LVDS Dual Channel 18/24-bit x 1 (Optional: eDP1.4b)
Display Interface	HDMI 2.0b x 1 DP1.4a x 2 Type C DP1.4 x 1
Multiple Display Support	Up to 4 Simultaneous Displays

Audio

Codec	Realtek ALC897/892
Audio Interface	Line-in/ Line-out/ MIC
Speaker	—

External I/O

Ethernet	Intel® i219LM, 10/100/1000Base, RJ-45 x 1
	Intel® i225LM, 100/1000/2500Base, RJ-45 x 1
USB	USB3.2 Gen 2 x 4
	USB3.2 Gen 2 Type C x 1 (PD 5V/3A)
Serial Port	—
Video	HDMI 2.0b x 1
	DP1.4a x 2
	Type C DP1.4 x 1
Power Input	Phoenix 2-pin Connector
Other	—

Internal I/O

USB	USB2.0 x 2
Serial Port	COM1, COM3, COM4 (RS232/422/485)
	COM2 (RS232/422/485, supports 5V/12V/RI)
Video	LVDS/ eDP x 1 (Default: LVDS)
	eDP: up to 1080P @ 60Hz
SATA	SATA III (6.0 Gbps) x 1
	+5V SATA Power x 1
Audio	Audio Header x 1
DIO/ GPIO	8-bit
SMBus/ I2C	SMBus/ I2C x 1 (Default: SMBus)
Touch	4/5/8-wire touch controller x 1 (optional)
Fan	Smart Fan x 1
SIM	Nano-SIM x 1
Front Panel	HDD LED, PWR LED, Power Button, Buzzer, Reset
Other	—

Expansion

Mini PCIe/ mSATA	Full-Sized mSATA/mPCIe x 1 (default: mSATA, select with BIOS)
M.2	M-Key 2280 x 1 (PCIe [x4]) E-Key 2230 x 1 (PCIe, USB2.0)
BIO	—
Other	—

Mechanical

Dimensions	5.75" x 4" (146mm x 101.7mm)

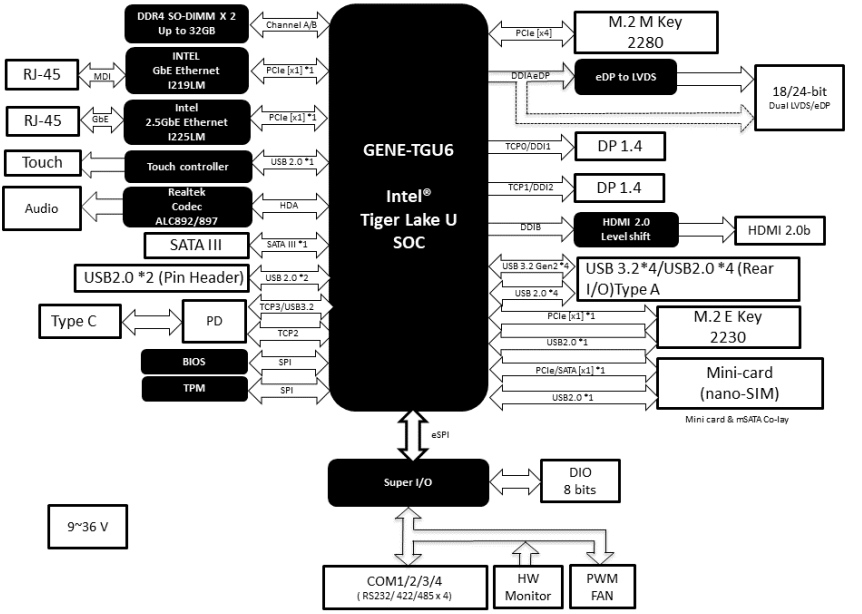
Environmental

Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	329,884

Certification

EMC	CE/ FCC Class A

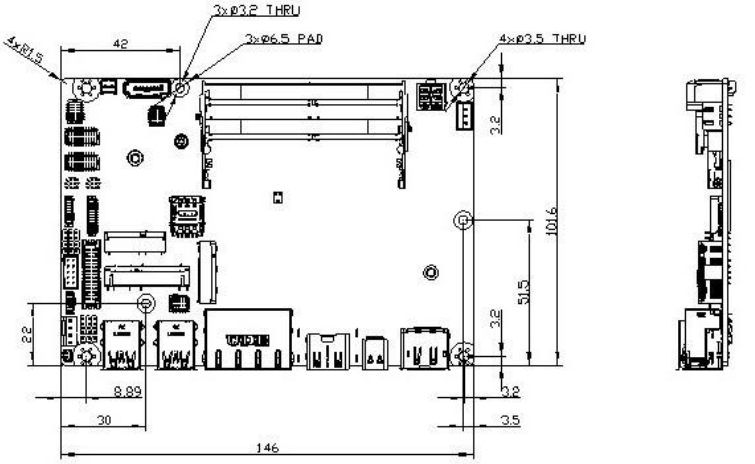
1.2 Block Diagram



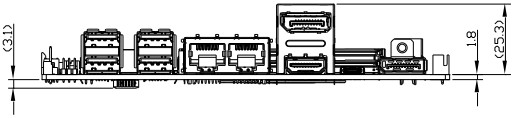
Chapter 2

Hardware Information

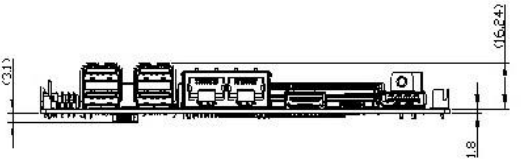
2.1 Dimensions

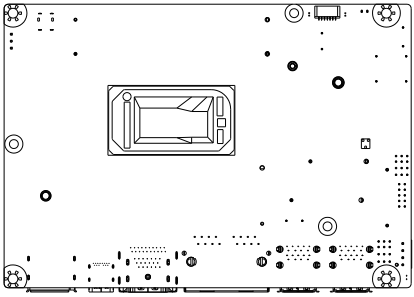


Note: Advanced version



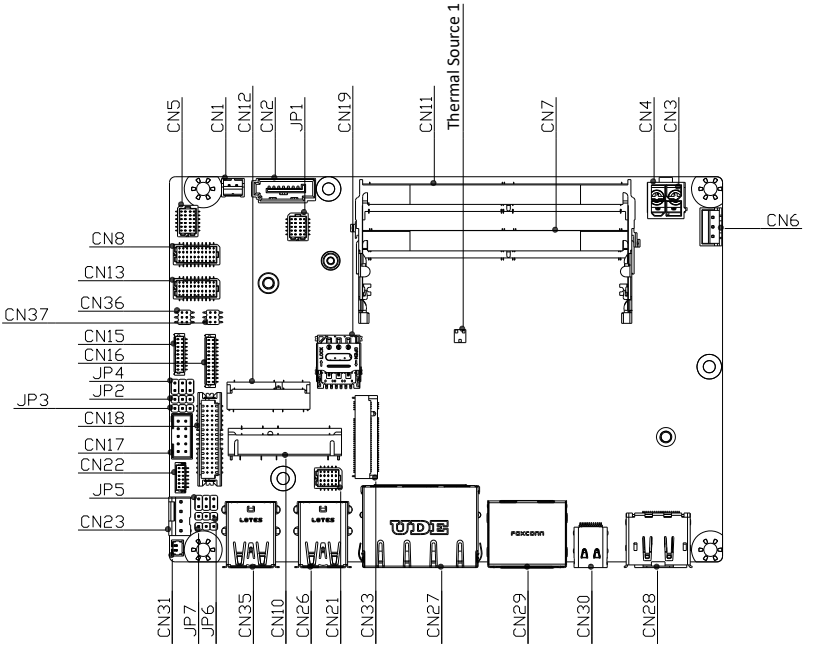
Note: Standard version



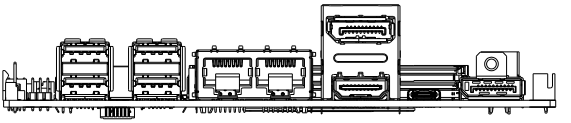


2.2 Jumpers and Connectors

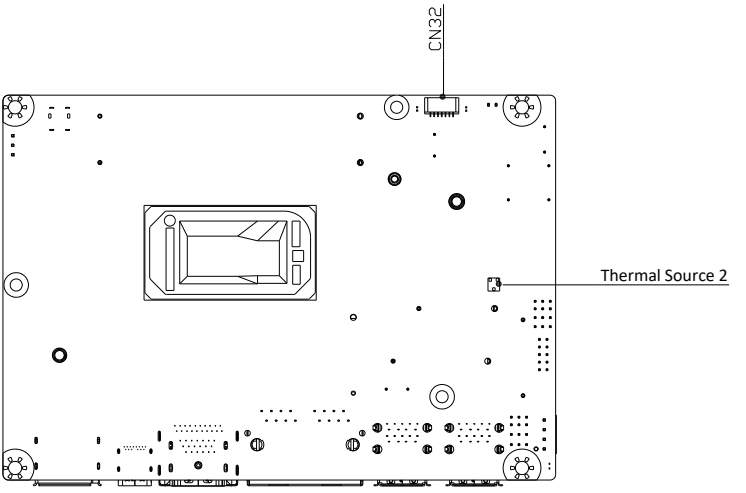
Top View



Front I/O View



Bottom View

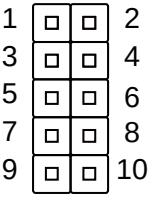


2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

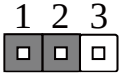
Label	Function
JP1	Front Panel Connector
JP2	Touch Screen 4/5/8-wire Mode Selection
JP3	Auto Power Button Enable/ Disable Selection
JP4	COM2 Pin 8 Function Selection
JP5	LVDS/eDP Port Backlight Inverter VCC Selection and Operating VDD Selection
JP6	LVDS/eDP Port Backlight Lightness Control Mode Selection
JP7	Clear CMOS Jumper

2.3.1 Front Panel Connector (JP1)

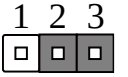


Pin	Function	Pin	Function
Pin 1	PWR_BTN-	Pin 2	PWR_BTN+
Pin 3	HDD_LED-	Pin 4	HDD_LED+
Pin 5	SPEAKER-	Pin 6	SPEAKER+
Pin 7	PWR_LED-	Pin 8	PWR_LED+
Pin 9	H/W RESET-	Pin 10	H/W RESET+

2.3.2 Touch Screen 4, 5, 8-Wire Selection (JP2)

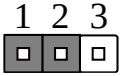


4/8-Wire Mode

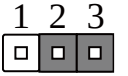


5-Wire Mode (**Default**)

2.3.3 Auto Power Button Enable/Disable Selection (JP3)

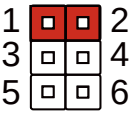


Disable/
ATX Power Mode

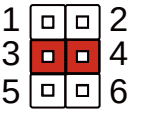


Enable/
AT Power Mode (**Default**)

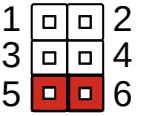
2.3.4 COM2 Pin8 Function Selection (JP4)



+12V

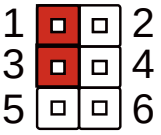
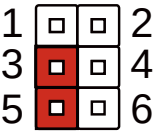
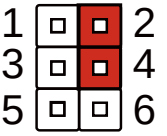
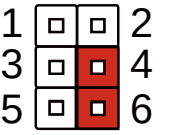


Ring (**Default**)



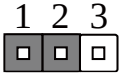
+5V

2.3.5 LVDS/eDP Backlight Inverter VCC & LVDS VDD Selection (JP5)

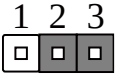
Backlight VCC Selection		LVDS VDD Selection	
			
+12V	+5V (**Default**)	+3.3V (**Default**)	+5V

Note: JP5 Default is two (2) jumpers placed on pins 3-5 and pins 2-4.

2.3.6 LVDS/eDP Port Backlight Lightness Control Mode Selection (JP6)

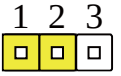


VR Mode

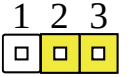


PWM Mode (**Default**)

2.3.7 Clear CMOS Jumper (JP7)



Normal (**Default**)



Clear CMOS

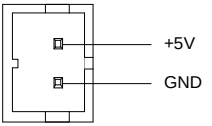
2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	+5V Output for SATA HDD
CN2	SATA Port
CN3	External Power Input
CN5	Audio I/O Port
CN6	External +5VSB Input
CN7	DDR4 SO-DIMM Slot
CN8	COM Port 3, Port 4; RS232/422/485 Dual Port Header
CN10	Mini Card Slot (Full-Size)
CN11	DDR4 SO-DIMM Slot
CN12	M.2 E Key 2230
CN13	COM Port 1, Port 2; RS232/422/485 Dual Port Header
CN15	Touch Screen Connector (Optional)
CN16	eSPI Debug Port
CN17	Digital I/O Port
CN18	LVDS/eDP Port
CN19	Nano SIM Card Socket
CN21	USB2.0 Port 5, Port 6; Dual Port Header
CN22	LVDS/eDP Port Inverter/ Backlight Connector
CN23	CPU Fan
CN26	USB3.2 Gen 2 Port 1, Port 2, Dual Port Connector
CN27	LAN (RJ-45) Dual Port Connector; i225 (left), i219 (right)
CN28	DP Connector
CN29	DP and HDMI Connector

Label	Function
CN30	Type C Connector (USB3.2 Gen 2 Only)
CN31	Battery Connector
CN32	SPI BIOS Debug Port
CN33	M.2 M Key 2280
CN35	USB3.2 Gen 2 Port 3, Port 4, Dual Port Connector
CN36	i219 LED Connector
CN37	i225 LED Connector

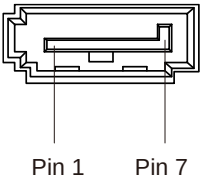
2.4.1 +5V Output for SATA HDD (CN1)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V at 1A
2	GND	GND	

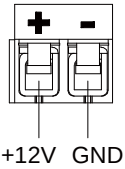
Note: Max current for Pin 1 is 1 Amp.

2.4.2 SATA Port (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

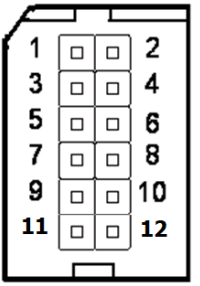
2.4.3 External Power Input (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+9~+36V (or +12V) at 8A
2	GND	GND	

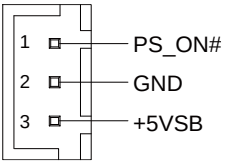
Note: There are two types of power input, 9~36V or 12V (by BOM option).

2.4.4 Audio I/O Port (CN5)



Pin	Pin Name	Signal Type
1	LOUT_R	OUT
2	MIC_R	IN
3	LOUT_L	OUT
4	MIC_L	IN
5	JD_LOUT	IN
6	JD_MIC	IN
7	AUD_GND	GND
8	AUD_GND	GND
9	JD_LIN	IN
10	LIN_R	IN
11	+VDD_AUD	PWR
12	LIN_L	IN

2.4.5 External +5VSB Input (CN6)

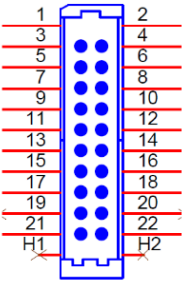


Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+5V
2	GND	GND	
3	+5VSB	PWR	+5V at 2A

2.4.6 DDR SO-DIMM Slot (CN7)

Standard Specifications

2.4.7 COM Port 3, Port 4 Dual Header (CN8)



RS-232

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	DCD	IN	
3	4	RX	IN	
5	6	TX	OUT	±5V
7	8	DTR	OUT	±5V
9	10	GND	GND	
11	12	DSR	IN	
13	14	RTS	OUT	±5V
15	16	CTS	IN	
17	18	RI	IN	
19	20	NC		

RS-485

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS485_D-	I/O	±5V
3	4	RS485_D+	I/O	±5V
5	6	NC		
7	8	NC		
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

RS-422

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS422_TX-	OUT	+5V
3	4	RS422_TX+	OUT	±5V
5	6	RS422_RX+	IN	
7	8	RS422_RX-	IN	
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

2.4.8 Mini Card Slot (Full-Size) (CN10)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
51	NC		
52	+3.3VSB	PWR	+3.3V

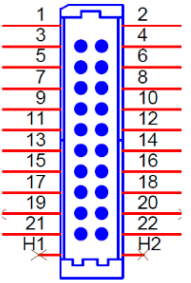
2.4.9 DDR SO-DIMM Slot (CN11)

Standard Specifications

2.4.10 M.2 E-Key 2230 (CN12)

Standard Specifications

2.4.11 COM Port 1, Port 2 Dual Header (CN13)



RS-232

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	DCD	IN	
3	4	RX	IN	
5	6	TX	OUT	±5V
7	8	DTR	OUT	±5V
9	10	GND	GND	
11	12	DSR	IN	

Pin	Pin	Pin Name	Signal Type	Signal Level
13	14	RTS	OUT	±5V
15	16	CTS	IN	
17	18	RI/+5V/+12V	IN	
19	20	NC		

Note: RI/+5V/+12V for COM2 only.

RS-485

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS485_D-	I/O	±5V
3	4	RS485_D+	I/O	±5V
5	6	NC		
7	8	NC		
9	10	GND	GND	
11	12	NC		
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

RS-422

Pin	Pin	Pin Name	Signal Type	Signal Level
1	2	RS422_TX-	OUT	+5V
3	4	RS422_TX+	OUT	±5V
5	6	RS422_RX+	IN	
7	8	RS422_RX-	IN	
9	10	GND	GND	
11	12	NC		

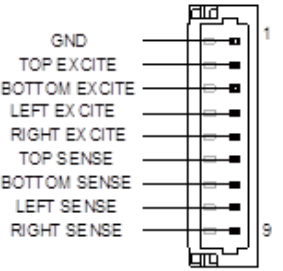
Pin	Pin	Pin Name	Signal Type	Signal Level
13	14	NC		
15	16	NC		
17	18	NC		
19	20	NC		

Note 1: COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

Note 2: Pin 8 function can be set by JP4 (See Ch 2.3.4).

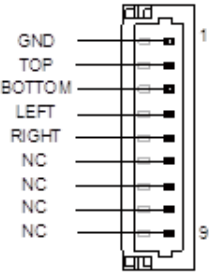
2.4.12 Touchscreen Connector (Optional) (CN15)

Note: Touch mode can be set by BIOS.



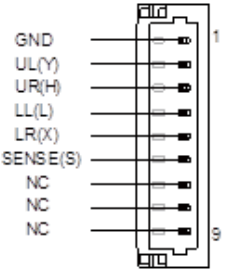
8-Wire Mode

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	
8	LEFT SENSE	IN	
9	RIGHT SENSE	IN	



4-Wire Mode

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		

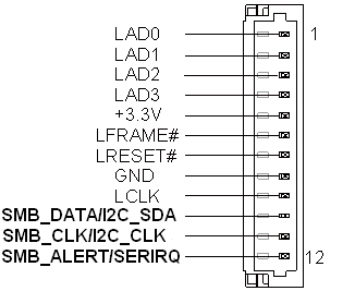


5-Wire Mode

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

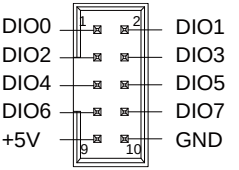
Note: Touch Mode can be set by BIOS

2.4.13 eSPI Debug Port (CN16)



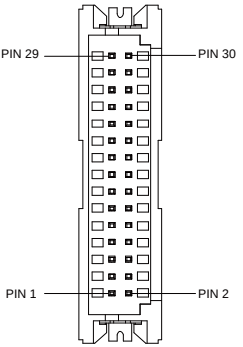
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA/I2C_SDA	I/O	
11	SMB_CLK/I2C_CLK	OUT	
12	SMB_ALERT/SERIRQ	IN	+3.3V

2.4.14 Digital I/O Connector (CN17)



Pin	Signal Description	Pin	Signal Description
1	PD0	2	PD1
3	PD2	4	PD3
5	PD4	6	PD5
7	PD6	8	PD7
9	+V5S (0.5A)	10	GND

2.4.15 LVDS/eDP Port (CN18)



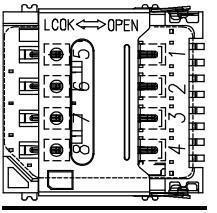
Note: LVDS LCD_PWR can be set to +3.3V or +5V by JP5. (See Ch 2.3.5)

Note: LVDS LCD_PWR supports current of 2A

Pin	LVDS	eDP	Signal Type	Signal Level
1	BKL_ENABLE	BKL_ENABLE	OUT	
2	BKL_CONTROL	BKL_CONTROL	OUT	
3	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	GND	
5	LVDS_A_CLK-	eDP_TXN3	DIFF	
6	LVDS_A_CLK+	eDP_TXP3	DIFF	
7	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	GND	
9	LVDS_DA0-	eDP_TXN2	DIFF	
10	LVDS_DA0+	eDP_TXP2	DIFF	
11	LVDS_DA1-	eDP_TXN1	DIFF	
12	LVDS_DA1+	eDP_TXP1	DIFF	
13	LVDS_DA2-	eDP_TXN0	DIFF	
14	LVDS_DA2+	eDP_TXP0	DIFF	
15	LVDS_DA3-	NC	DIFF	
16	LVDS_DA3+	eDP_HPD	DIFF	
17	DDC_DATA	eDP_AUX_N	I/O	+3.3V
18	DDC_CLK	eDP_AUX_P	I/O	+3.3V
19	LVDS_DB0-	NC	DIFF	
20	LVDS_DB0+	NC	DIFF	
21	LVDS_DB1-	NC	DIFF	
22	LVDS_DB1+	NC	DIFF	
23	LVDS_DB2-	NC	DIFF	
24	LVDS_DB2+	NC	DIFF	
25	LVDS_DB3-	NC	DIFF	
26	LVDS_DB3+	NC	DIFF	

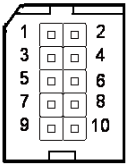
Pin	LVDS	eDP	Signal Type	Signal Level
27	LCD_PWR	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	GND	
29	LVDS_B_CLK-	NC	DIFF	
30	LVDS_B_CLK+	NC	DIFF	

2.4.16 Nano SIM Card Socket (CN19)



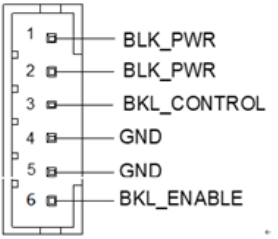
Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	NC		
5	GND	GND	
6	UIM_VPP	PWR	
7	UIM_DATA	I/O	
8	NC		

2.4.17 USB 2.0 Port 5, Port 6 Dual Header (CN21)



USB Port 5		USB Port 6	
Pin	Pin Name	Pin	Pin Name
1	+5VSB (0.5A)	2	+5VSB (0.5A)
3	USB5_D-	4	USB6_D-
5	USB5_D+	6	USB6_D+
7	GND	8	GND
9	GND	10	GND

2.4.18 LVDS/eDP Port Inverter/ Backlight Connector (CN22)



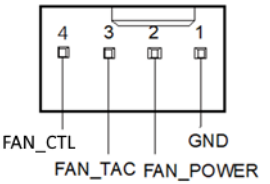
Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_PWR	PWR	+5V / +12V
3	BKL_CONTROL	OUT	
4	GND	GND	
5	GND	GND	
6	BKL_ENABLE	OUT	+3.3V

Note 1: LVDS BKL_PWR can be set to +5V or +12V by JP5. (See Ch 2.3.5)

Note 2: LVDS BKL_PWR supports current of 1.5A

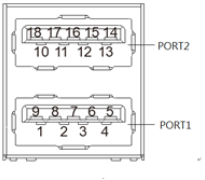
Note 3: LVDS BKL_CONTROL can be set by JP6. (See Ch 2.3.6)

2.4.19 CPU Fan (CN23)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V at 1A
3	FAN_TAC	IN	
4	FAN_CTL		

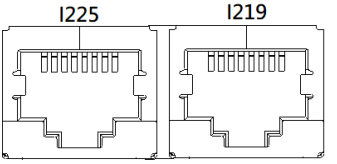
2.4.20 USB 3.2 Gen 2 Ports 1 & 2 Dual Connector (CN26)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V at 0.9A
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
7	GND	GND	
8	USB0_SSTX–	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V at 0.9A
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX–	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX–	DIFF	
18	USB1_SSTX+	DIFF	

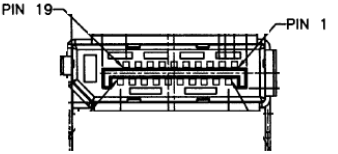
2.4.21 LAN (RJ-45) Dual Port i225 and i219 (CN27)



i225		i219	
Pin	Pin Name	Pin	Pin Name
1P1	LAN2_MDI0_P	2P1	LAN1_MDI0_P
1P2	LAN2_MDI0_N	2P2	LAN1_MDI0_N
1P3	LAN2_MDI1_P	2P3	LAN1_MDI1_P
1P4	LAN2_MDI1_N	2P4	LAN1_MDI1_N
1P7	LAN2_MDI2_P	2P7	LAN1_MDI2_P

i225		i219	
Pin	Pin Name	Pin	Pin Name
1P8	LAN2_MDI2_N	2P8	LAN1_MDI2_N
1P9	LAN2_MDI3_P	2P9	LAN1_MDI3_P
1P10	LAN2_MDI3_N	2P10	LAN1_MDI3_N

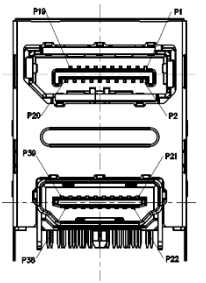
2.4.22 DP Connector (CN28)



Pin	Pin Name	Signal Type	Signal Level
1	DP1_TX0_DP	DIFF	
2	GND	GND	
3	DP1_TX0_DN	DIFF	
4	DP1_TX1_DP	DIFF	
5	GND	GND	
6	DP1_TX1_DN	DIFF	
7	DP1_TX2_DP	DIFF	
8	GND	GND	
9	DP1_TX2_DN	DIFF	
10	DP1_TX3_DP	DIFF	
11	GND	GND	
12	DP1_TX3_DN	DIFF	
13	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
14	GND	GND	
15	DP1_AUX_DP	I/O	
16	GND	GND	
17	DP1_AUX_DN	I/O	
18	DP1_HPD	I/O	
19	GND	GND	
20	+V3P3S	PWR	+3.3V

2.4.23 DP + HDMI Connector (CN29)

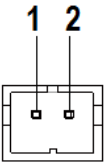


Pin	Pin Name	Signal Type	Signal Level
		DP Port	
1	DP2_TX0_DP	DIFF	
2	GND	GND	
3	DP2_TX0_DN	DIFF	
4	DP2_TX1_DP	DIFF	
5	GND	GND	
6	DP2_TX1_DN	DIFF	
7	DP2_TX2_DP	DIFF	

Pin	Pin Name	Signal Type	Signal Level
8	GND	GND	
9	DP2_TX2_DN	DIFF	
10	DP2_TX3_DP	DIFF	
11	GND	GND	
12	DP2_TX3_DN	DIFF	
13	GND	GND	
14	GND	GND	
15	DP2_AUX_DP	I/O	
16	GND	GND	
17	DP2_AUX_DN	I/O	
18	DP2_HPD	I/O	
19	GND	GND	
20	+V3P3S	PWR	+3.3V
		HDMI Port	
21	HDMI_TX2+	DIFF	
22	GND	GND	
23	HDMI_TX2-	DIFF	
24	HDMI_TX1+	DIFF	
25	GND	GND	
26	HDMI_TX1-	DIFF	
27	HDMI_TX0+	DIFF	
28	GND	GND	
29	HDMI_TX0-	DIFF	
30	HDMI_CLK+	DIFF	
31	GND	GND	
32	HDMI_CLK-	DIFF	

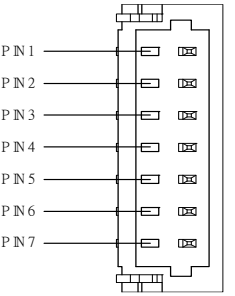
Pin	Pin Name	Signal Type	Signal Level
33	NC		
34	NC		
35	DDC_CLK	I/O	+5V
36	DDC_DATA	I/O	+5V
37	GND	GND	
38	+5V	PWR	+5V
39	HDMI_HPD		

2.4.24 Battery Connector (CN31)



Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.25 SPI BIOS Debug Port (CN32)

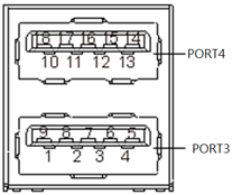


Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

2.4.26 M.2 M-Key 2280 Slot (CN33)

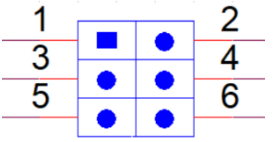
Standard specifications

2.4.27 USB3.2 Gen 2 Ports 3 & 4 Dual Connector (CN35)



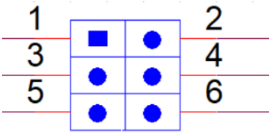
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V at 0.9A
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	USB2_SSRX–	DIFF	
6	USB2_SSRX+	DIFF	
7	GND	GND	
8	USB2_SSTX–	DIFF	
9	USB2_SSTX+	DIFF	
10	+5VSB	PWR	+5V at 0.9A
11	USB3_D-	DIFF	
12	USB3_D+	DIFF	
13	GND	GND	
14	USB3_SSRX–	DIFF	
15	USB3_SSRX+	DIFF	
16	GND	GND	
17	USB3_SSTX–	DIFF	
18	USB3_SSTX+	DIFF	

2.4.28 i219 LED Connector (CN36)



Pin	Pin Name	Signal Type	Signal Level
1	LINK_ACT#	IO	
2	+V3P3A	PWR	+3.3V
3	LAN_1000#	IO	
4	LAN_100#	IO	
5	LAN_100#	IO	
6	LAN_1000#	IO	

2.4.29 i225 LED Connector (CN37)

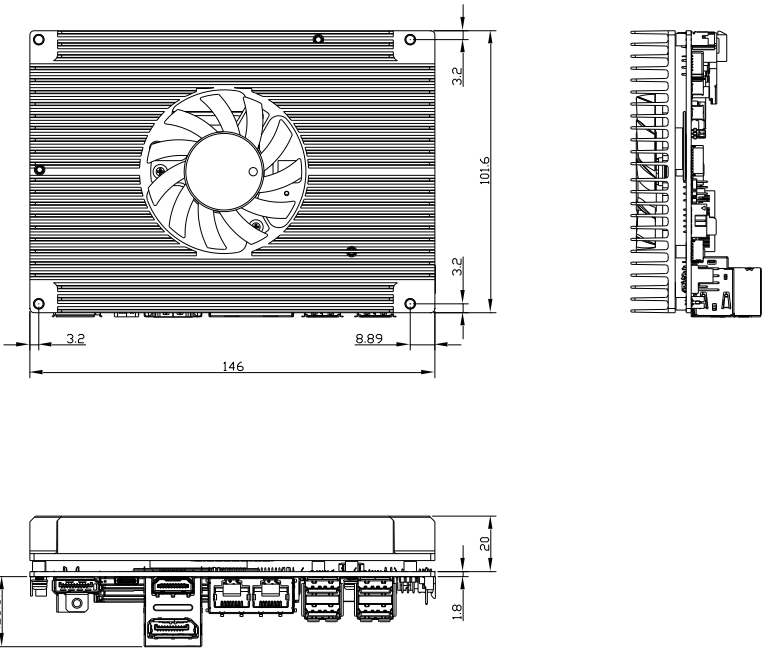


Pin	Pin Name	Signal Type	Signal Level
1	LINK_ACT#	IO	
2	+V3P3A	PWR	+3.3V
3	LAN_2500#	IO	
4	LAN_1000#	IO	
5	LAN_1000#	IO	
6	LAN_2500#	IO	

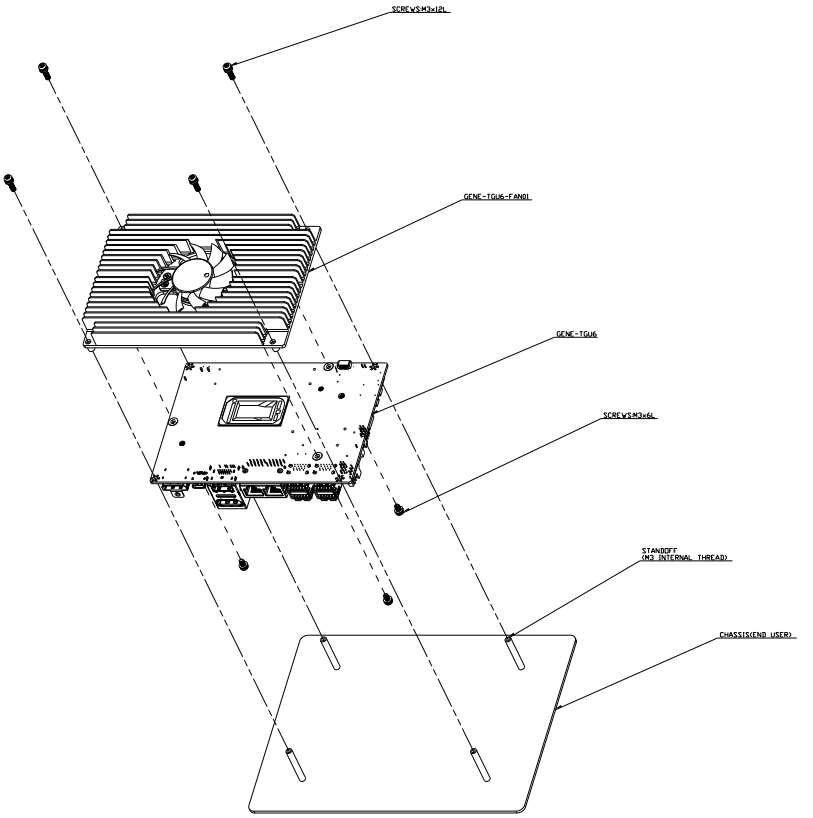
2.5 Thermal Solutions

2.5.1 GENE-TGU6-FAN01

Single piece cooler, does not require use of heat spreader

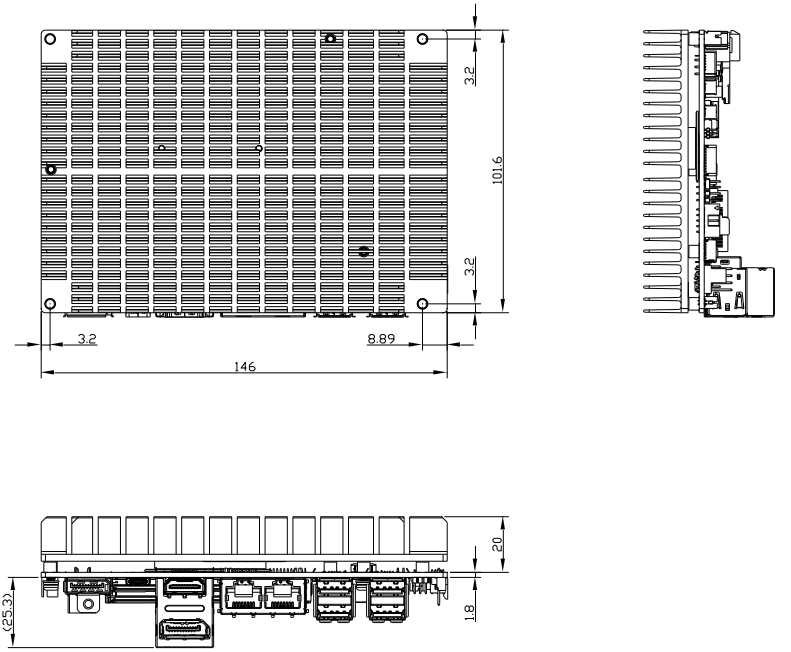


GENE-TGU6-FAN01 Assembly

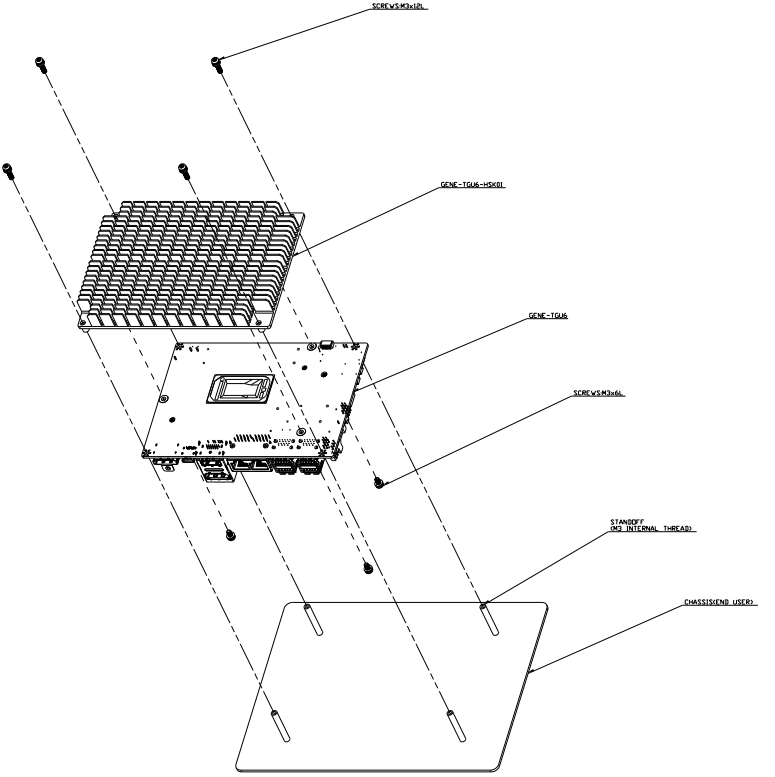


2.5.2 GENE-TGU6-HSK01

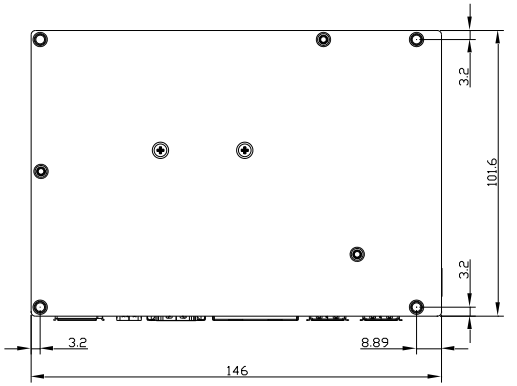
Single-piece heat sink, does not require use of heat spreader.

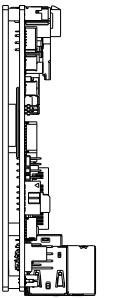


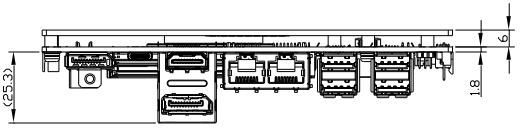
GENE-TGU6-HSK01 Assembly



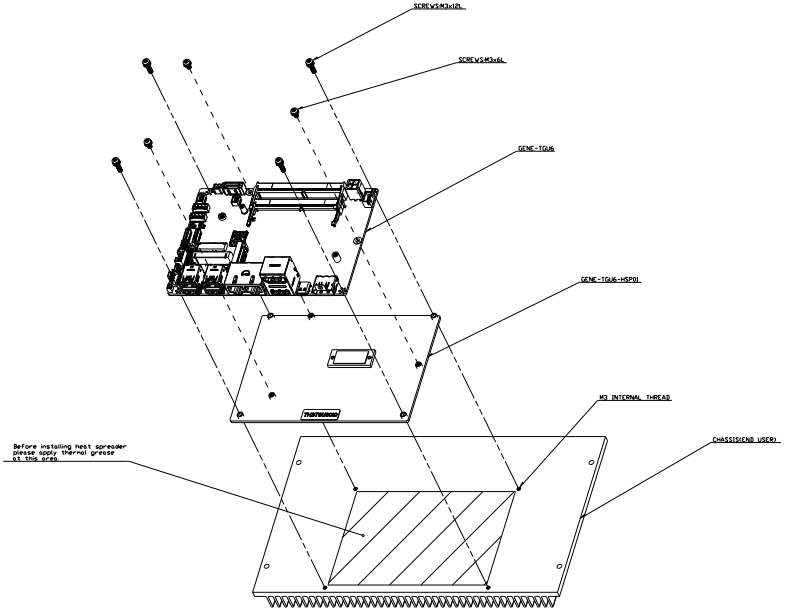
2.5.3 GENE-TGU6-HSP01







GENE-TGU6-HSP01 Assembly



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The GENE-TGU6 board uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the module will output a few short beeps or display an error message. The module can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the module will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integral lithium battery backup for data retention. You will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <ESC> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access advanced hardware settings and Hardware Monitor

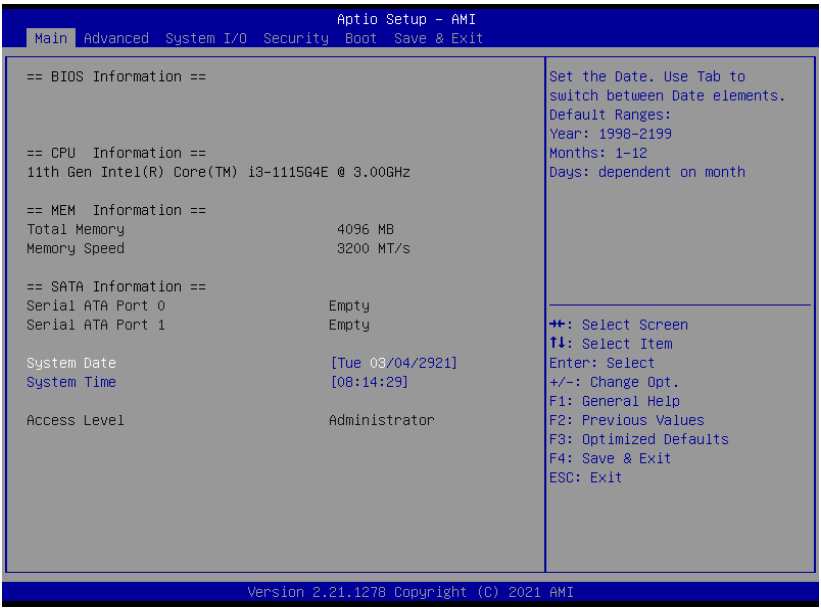
System I/O – Configure I/O settings including PCI Express and storage options

Security – Set admin and user passwords, access secure boot options

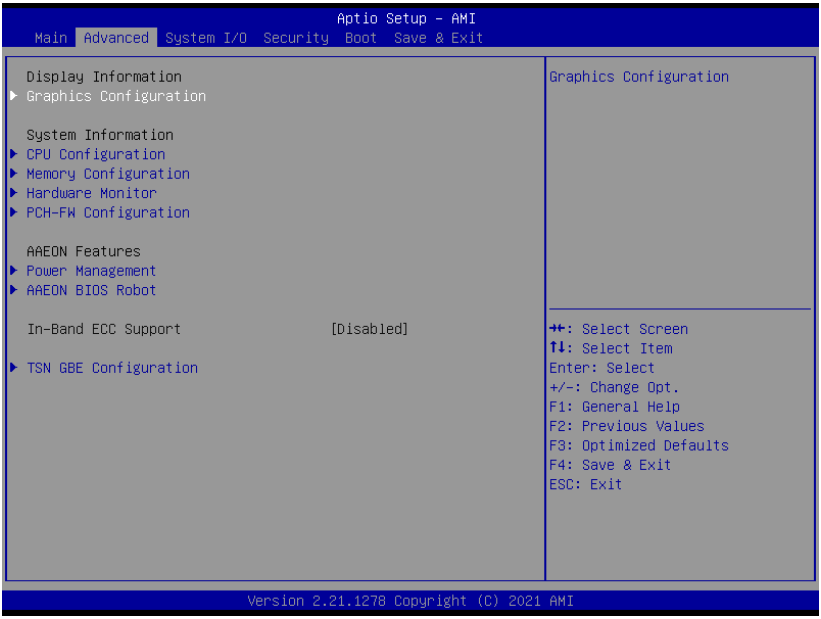
Boot – Boot options including BBS priority and Quiet Boot options

Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced

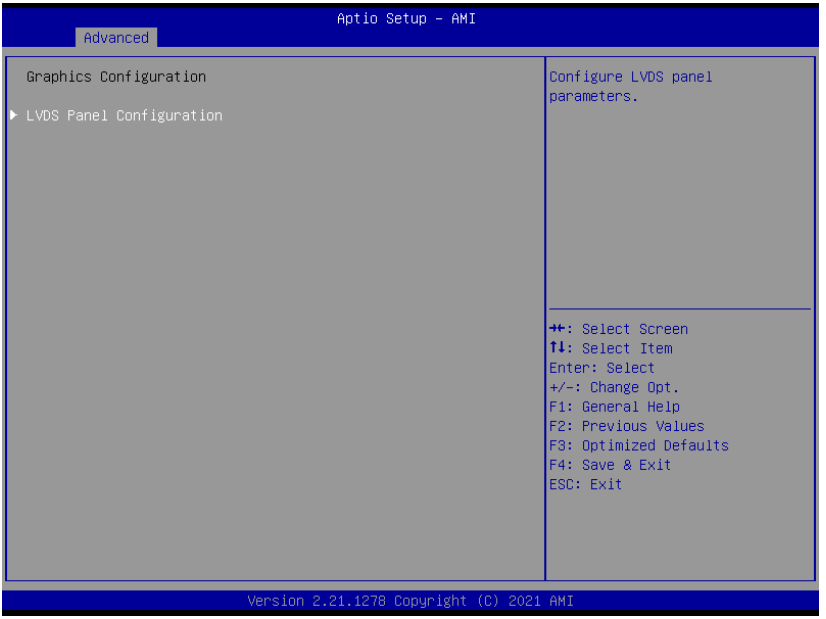


Options Summary		
In-Band ECC Support	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable/Disabled In-Band ECC Support		
In-Band ECC Error Injection	Enabled	
	Disabled	Optimal Default, Failsafe Default
By enabling this Error Injection feature, the user acknowledges the security risks. Enabling Error Injection allows attackers who have access to the Host Operating System to inject IBECC errors that can cause unintended memory corruption and enable the leak of security data in the BIOS stolen memory regions.		
In-Band ECC Operation Mode	0	
	1	
	2	Optimal Default, Failsafe Default
0: Functional Mode protects requests based on the address range, 1: Makes all requests non-protected and ignore range checks, 2: Makes all requests protected and ignore range checks		

Options Summary		
IBECC Protect Region 0-7	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled In-Band ECC for Region 0-7		

Note: In-Band ECC Support availability depends on CPU.

3.4.1 Graphics Configuration



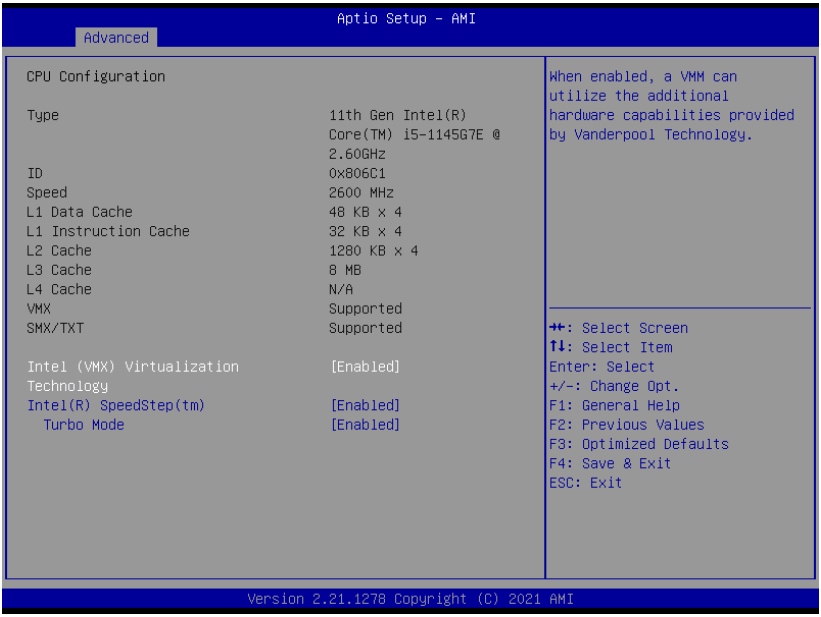
3.4.1.1 LVDS Panel Configuration

Options Summary		
LVDS/eDP	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disabled this panel.		
LVDS Panel Type	640X480@60HZ	
	800X480@60HZ	
	800X600@60HZ	
	1024X600@60HZ	
	1024X768@60HZ	Optimal Default, Failsafe Default
	1280X768@60HZ	
	1280X800@60HZ	
	1280X1024@60HZ	
	1366X768@60HZ	
	1440X900@60HZ	
	1600X1200@60HZ	
	1920X1080@60HZ	
	1920X1200@60HZ	

Options Summary		
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Mode	BIOS & Application	
	Windows Slider	Optimal Default, Failsafe Default
Select backlight control signal type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1.1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		
Swing Level	150mV	
	200mV	
	250mV	
	300mV	Optimal Default, Failsafe Default
	350mV	
	400mV	

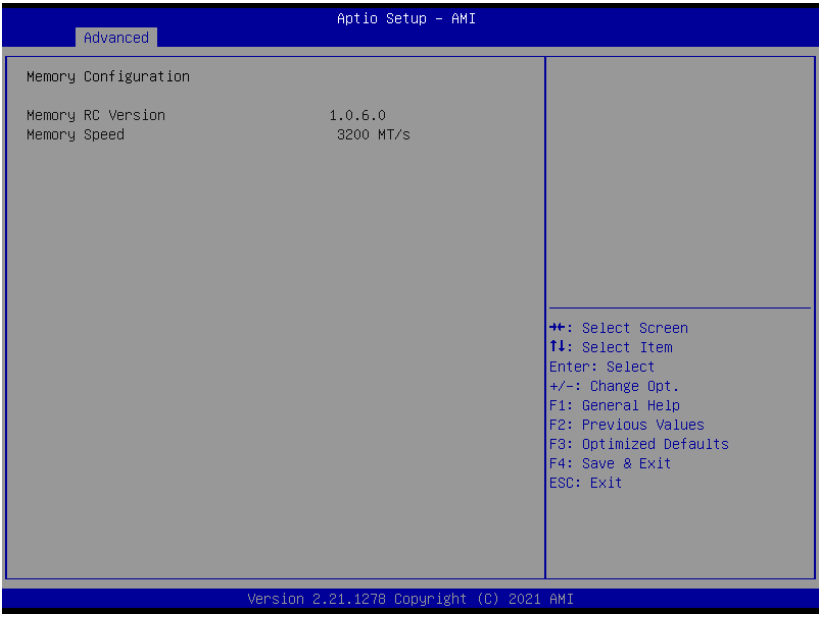
Options Summary		
Swing Level	450mV	
Select Swing Level		
Center Spreading Depth	no spreading	Optimal Default, Failsafe Default
	0.5%	
	1.0%	
	1.5%	
	2.0%	
	2.5%	
Select Center Spreading Depth		

3.4.2 CPU Configuration

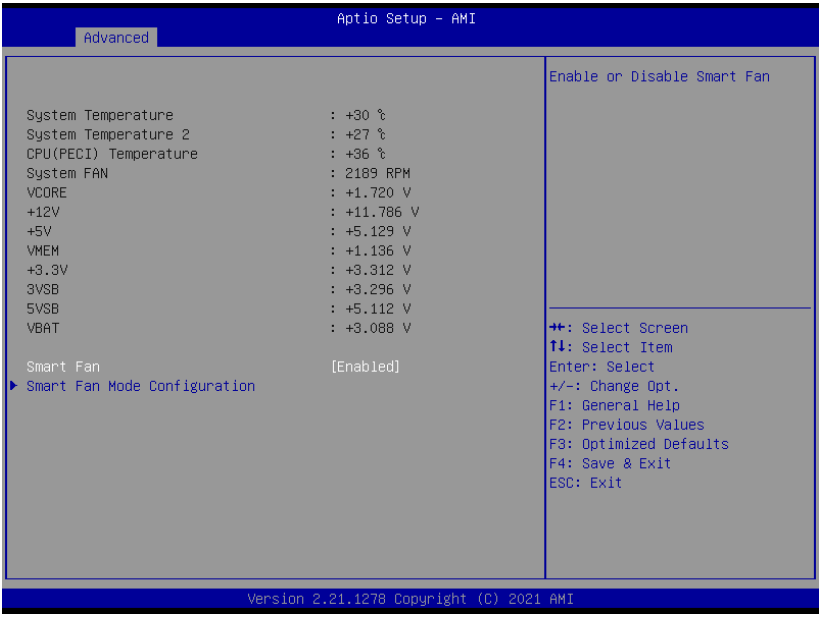


Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.		

3.4.3 Memory Configuration



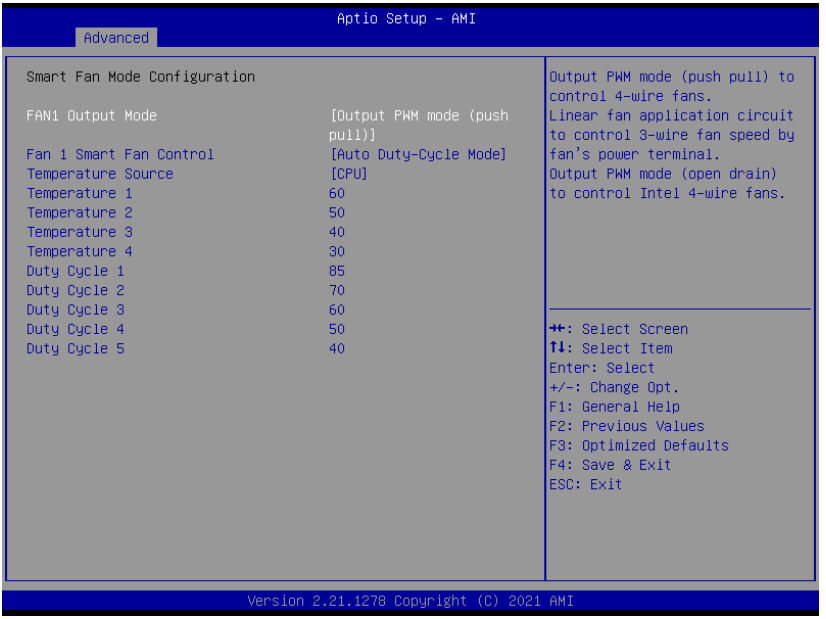
3.4.4 Hardware Monitor



Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Smart Fan		

3.4.4.1 Smart Fan Mode Configuration

Auto Duty Cycle Mode

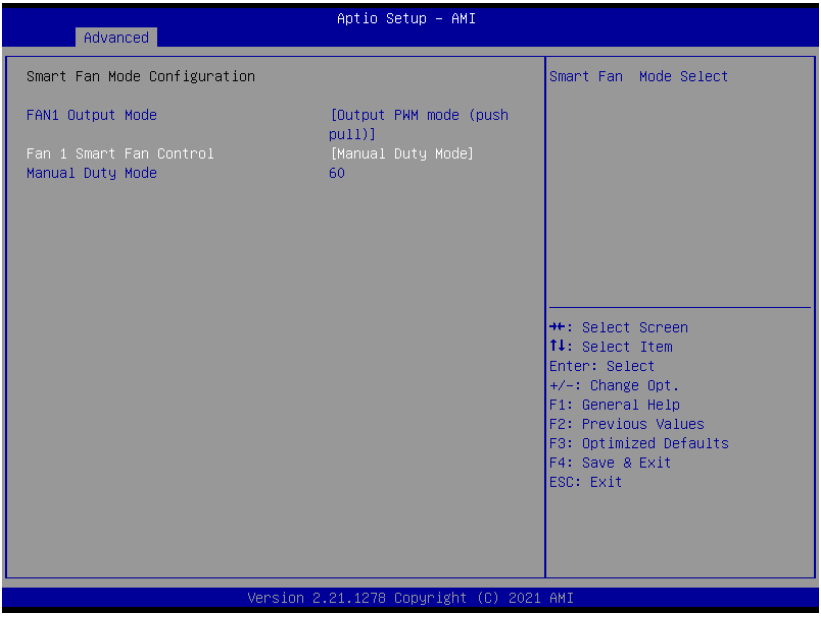


Options Summary		
FAN1 Output Mode	Output PWM mode (push pull)	
	Linear Fan Application	
	Output PWM mode (open drain)	Optimal Default, Failsafe Default
Output PWM mode (push pull) to control 4-wire fans.\nLinear fan application circuit to control 3-wire fan speed by fan's power terminal.\nOutput PWM mode (open drain) to control Intel 4-wire fans.		
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU	Optimal Default, Failsafe Default
	System Temperature 2	
	System Temperature	
Select the monitored temperature source for this fan.		

Table Continues on Next Page…

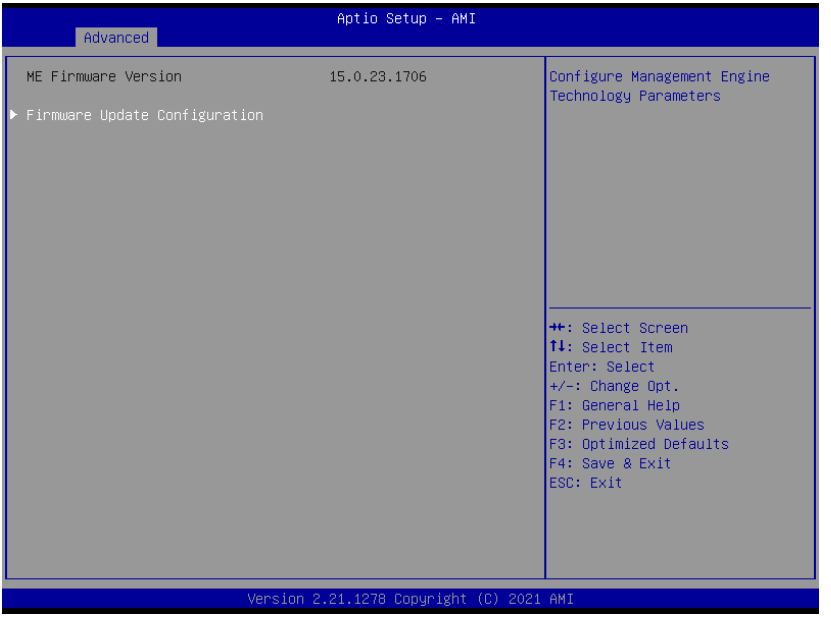
Options Summary	
Duty Cycle	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100
Temperature	

Manual Duty Mode

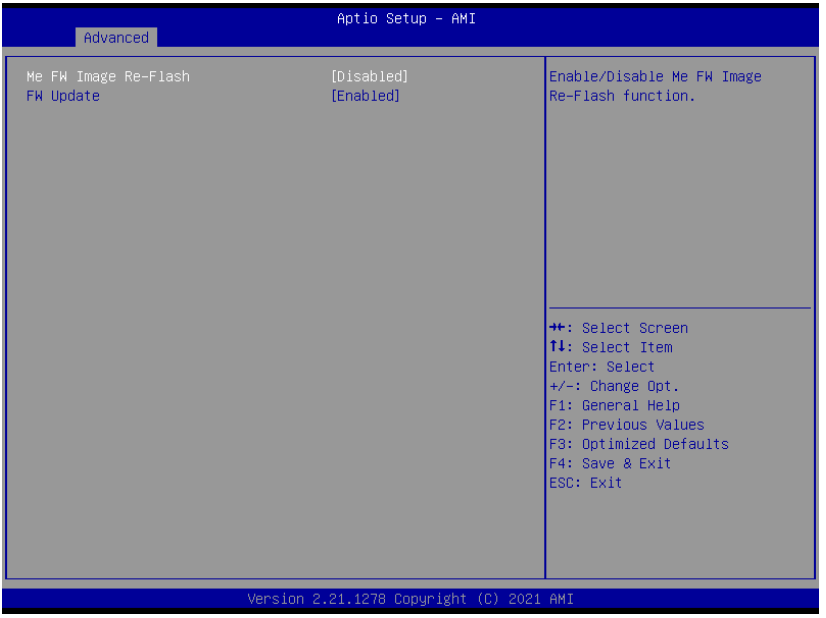


Options Summary		
Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100		

3.4.5 PCH-FW Configuration

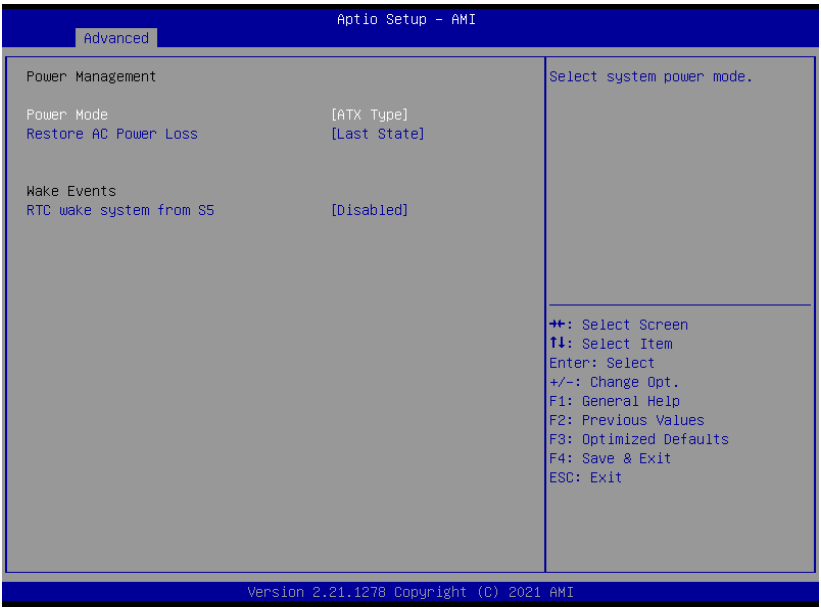


3.4.5.1 Firmware Update Configuration



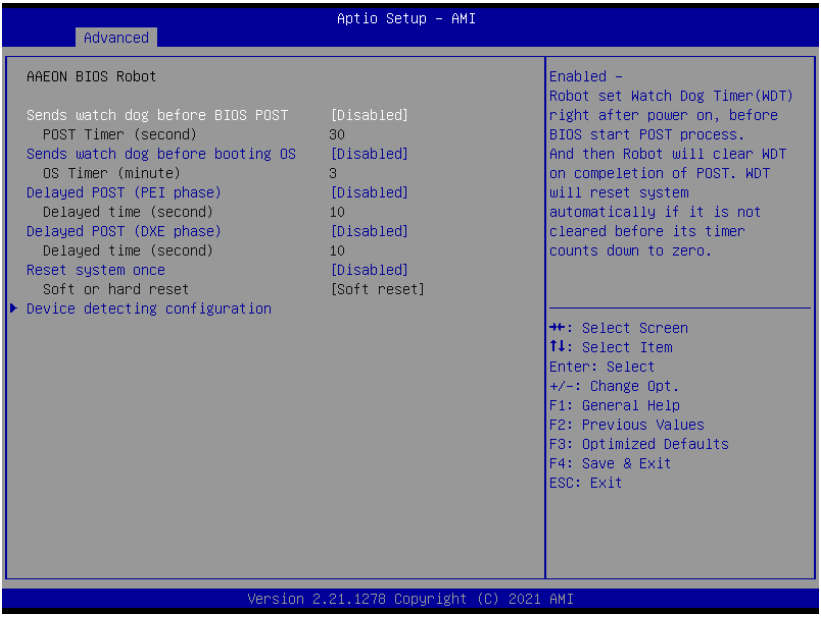
Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.6 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
IO Restore AC power Loss		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)./n Bypass: BIOS will not control RTC wake function during system shutdown		

3.4.7 AAEON BIOS Robot

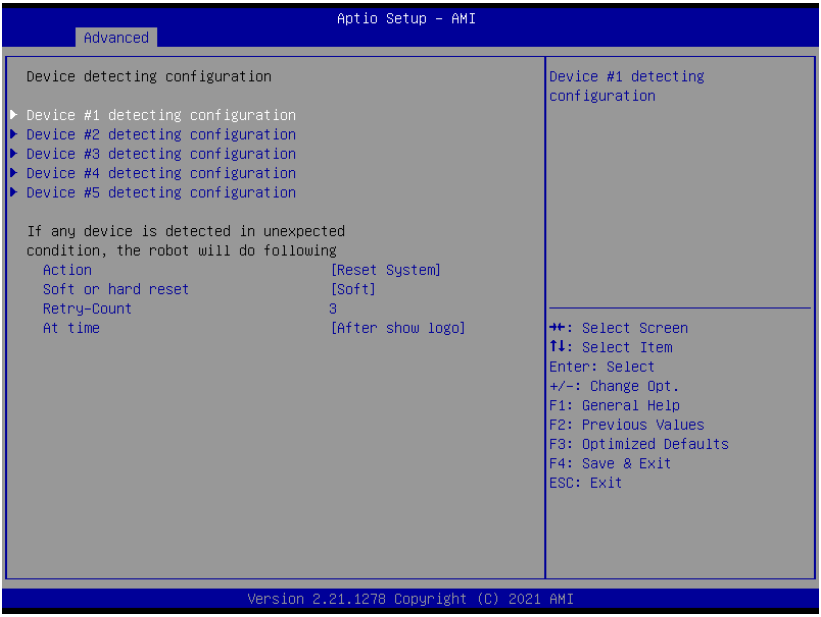


Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Time r(WDT) right after power on, before BIOS start POST process. Robot will clear WDT on completion of POST. WDT will reset system automatically if it is not cleared before its timer counts down to zero.		
POST Timer (second)	30	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for POST. WARNING: Do not set to a value equal to or shorter than normal POST time, otherwise system may never complete POST unless clearing BIOS settings. More than twice the normal POST time is suggested.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfers control to OS. WARNING: Before enabling this function, a program in OS must be responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		

Options Summary		
OS Timer (minute)	3	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for OS loading.		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this after 'Sends watch dog before BIOS POST'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset	
Select reset type robot should send on each boot.		

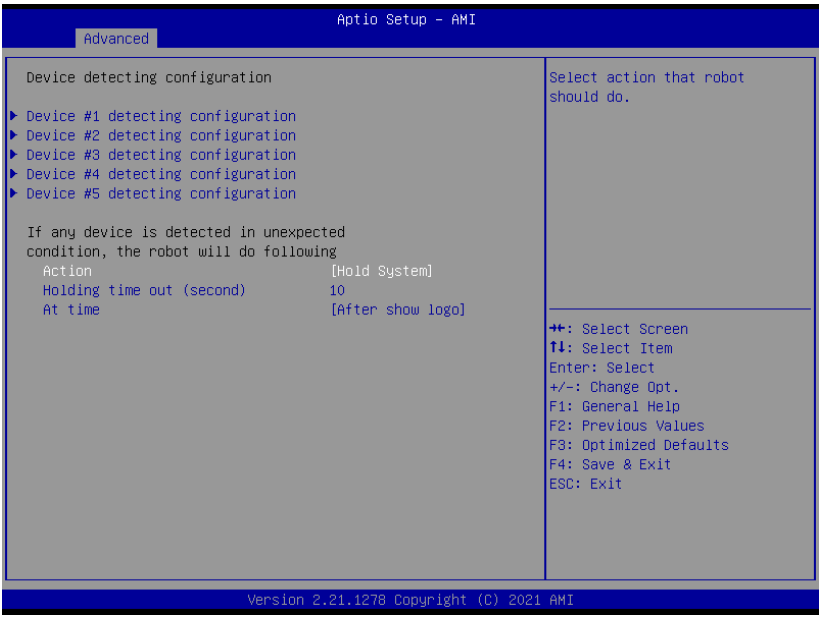
3.4.7.1 Device Detecting Configuration

Action: Rest System



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Fill retry counter here. Robot will reset system at most counter times, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo – Robot will do action after logo is displayed. System devices are almost ready. Before show logo – Robot will do action earlier before logo, but some devices may not be ready.		

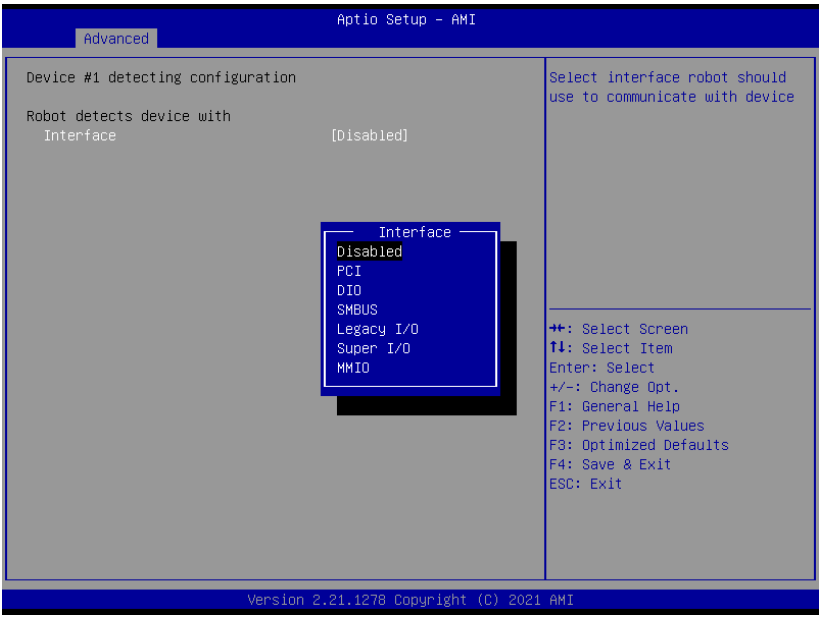
Action: Hold System



Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Holding time out (second)	10	Optimal Default, Failsafe Default
Fill hold time out here. Robot will hold system no longer then time-out value, and then let system continue its POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select robot action time: After show logo - Robot will do actoin after logo is displayed. System devices are almost ready. Before show logo - Robot will do action earlier before logo, but some devices may not be ready.		

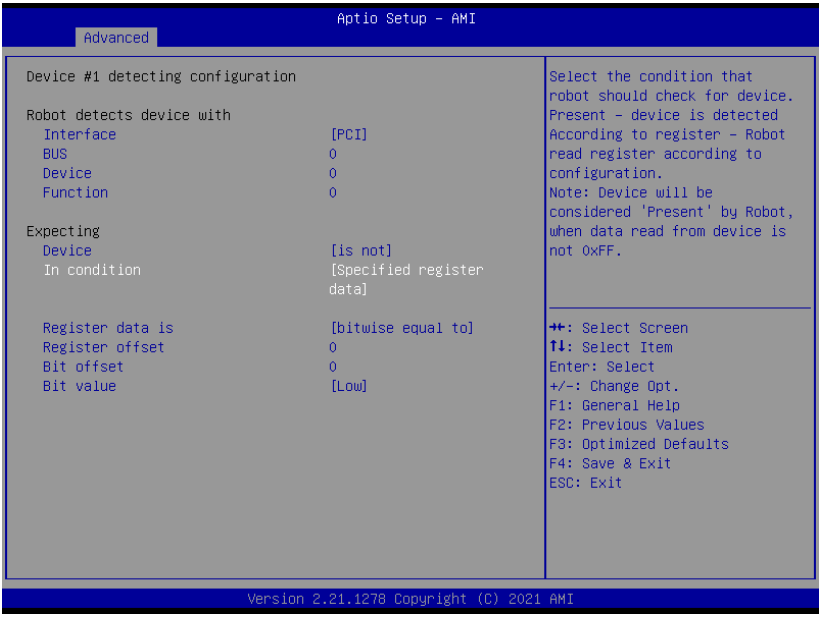
3.4.7.1.1 Device # Detecting Configuration

Interface: Disabled



Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

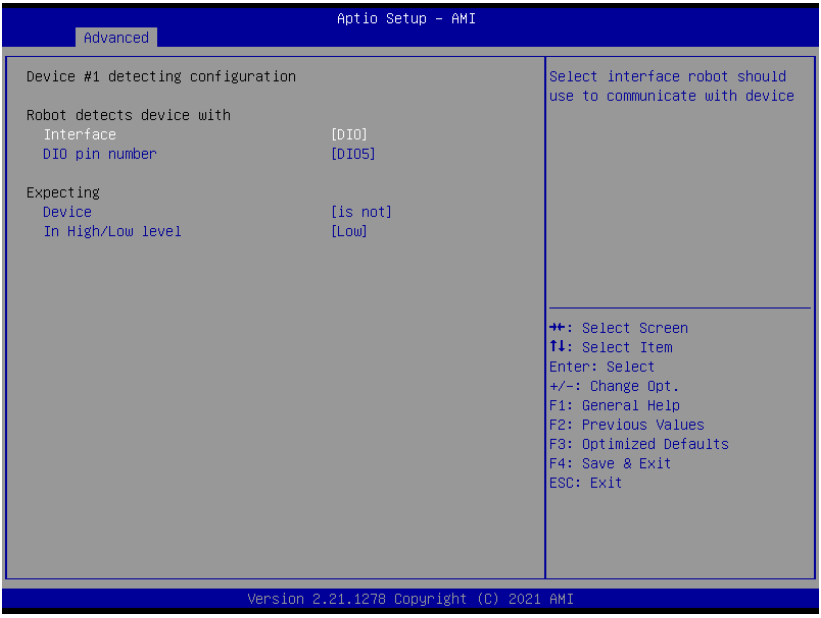
Interface: PCI



Options Summary		
BUS	0	Optimal Default, Failsafe Default
Fill BUS number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	0	Optimal Default, Failsafe Default
Fill DEVICE number to a PCI device, in hexadecimal. Range: 0 - FF		
Function	0	Optimal Default, Failsafe Default
Fill FUNCTION number to a PCI device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		

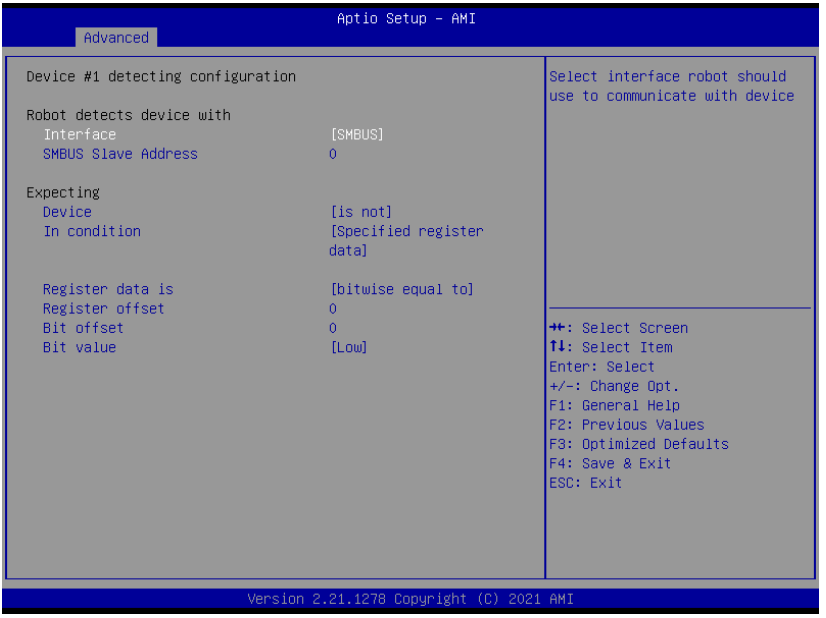
Options Summary		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

Interface: DIO



Options Summary		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
DIO pin number	DIO1	Optimal Default, Failsafe Default
	DIO*	
Fill DIO pin number. 0 - DIO0, 1 - DIO1, and so on. For COM express product: 0-3 - GPI0-3, 4-7 - GPO0-3		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In High/Low level	Low	Optimal Default, Failsafe Default
	High	
Select High/Low level of the DIO pin that robot should do action.		

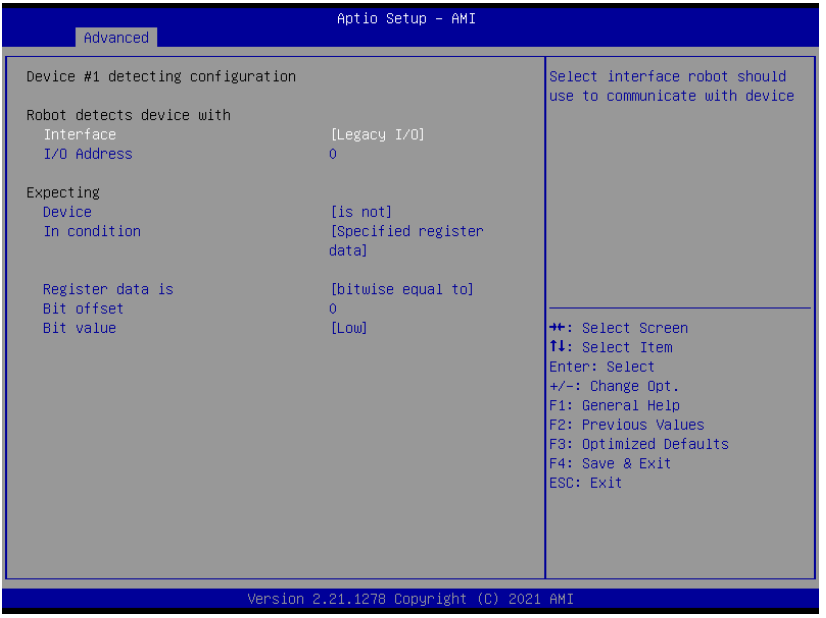
Interface: SMBUS



Options Summary		
SMBUS Slave Address	0	Optimal Default, Failsafe Default
Fill slave address to a SMBUS device, in hexadecimal. Range: 0 - FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

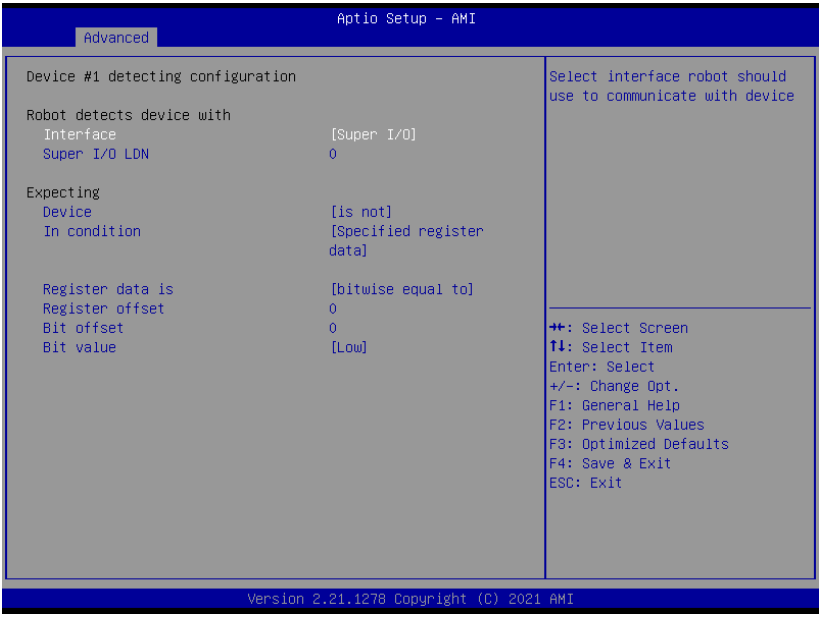
Interface: Legacy I/O



Options Summary		
I/O Address	0	Optimal Default, Failsafe Default
Fill I/O address device is responding to. Range: 0~FFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

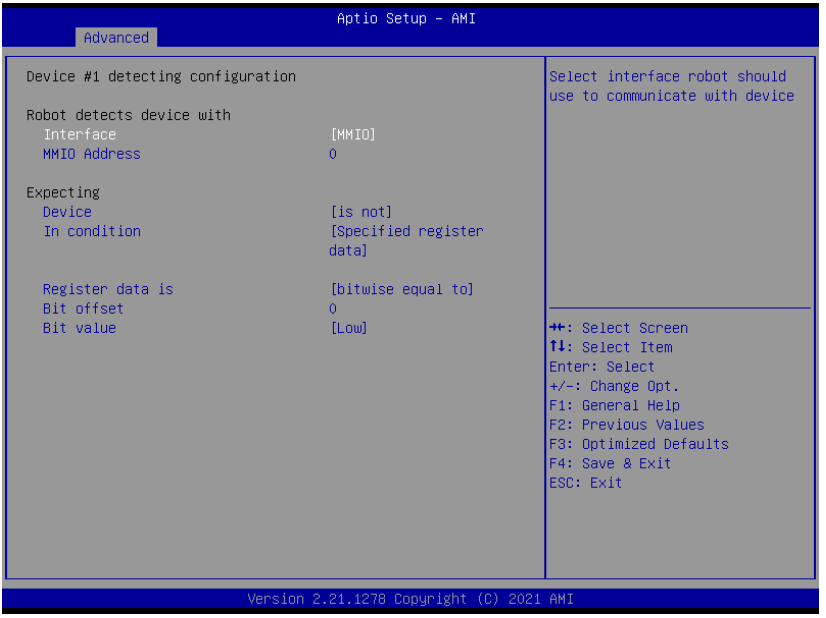
Interface: Super I/O



Options Summary		
Super I/O LDN	0	Optimal Default, Failsafe Default
Fill LDN number to a Super I/O device. Range: 0~FF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

Options Summary		
Register offset	0	Optimal Default, Failsafe Default
Fill register offset (or index) for robot to read, in hexadecimal. Range: 0 - FF		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

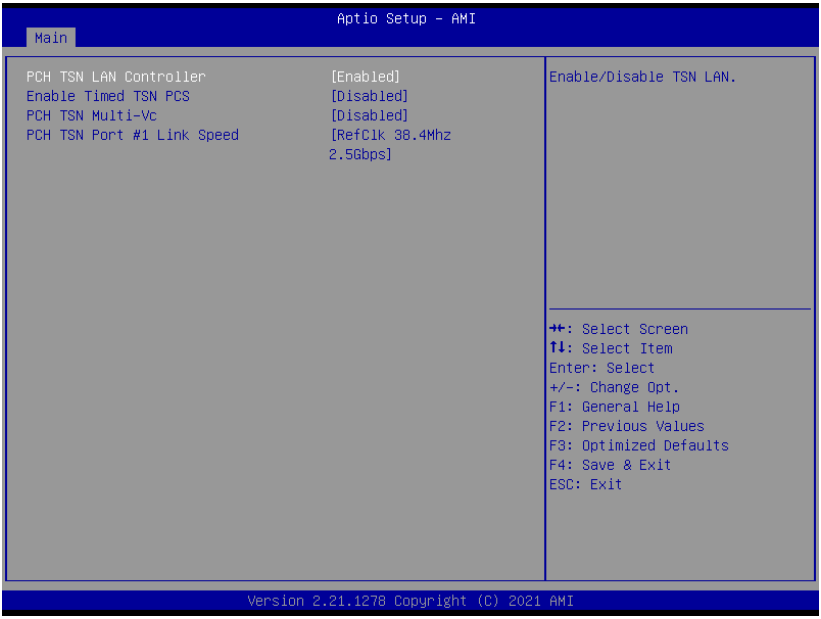
Interface: MMIO



Options Summary		
MMIO Address	0	Optimal Default, Failsafe Default
Fill Memory Mapped I/O address device is responding to. Range: 0~FFFFFFFF		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select that robot should or should not do action if condition met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select the condition that robot should check for device. Present - device is detected According to register - Robot read register according to configuration. **Note**: Device will be considered 'Present' by Robot, when data read from device is not 0xFF.		
Register data is	bitwise equal to	Optimal Default, Failsafe Default
	bytewise equal to	
	bytewise lesser than	
	bytewise larger than	
Select how robot should compare data read from register, to a value configured below.		

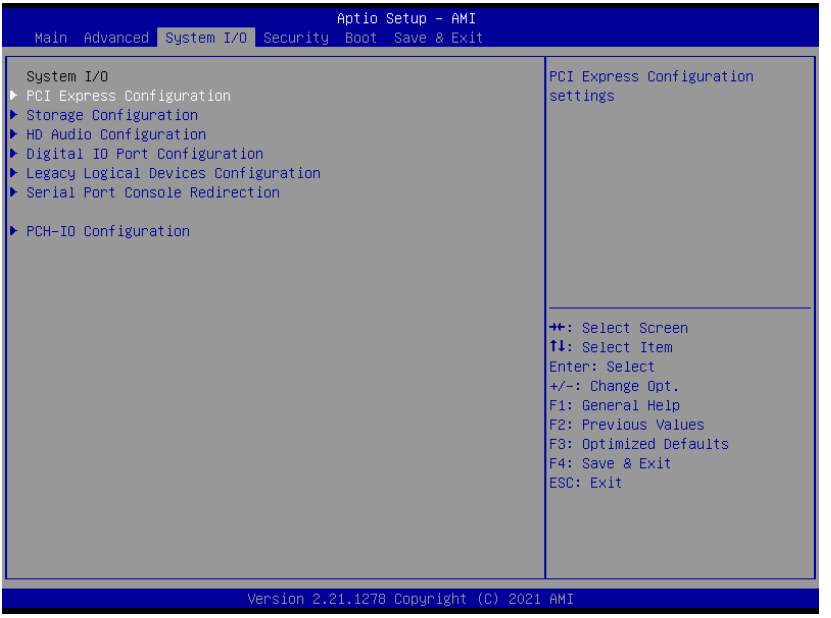
Options Summary		
Bit offset	0	Optimal Default, Failsafe Default
Fill bit offset for register, for robot to compare with bit value.		
Bit value	Low	Optimal Default, Failsafe Default
	High	
Fill bit value for robot to compare register-bit with specified offset.		
Byte value	0	Optimal Default, Failsafe Default
Fill a byte value for robot to compare register data with, in hexadecimal. Range: 0 - FF		

3.4.8 TSN GBE Configuration

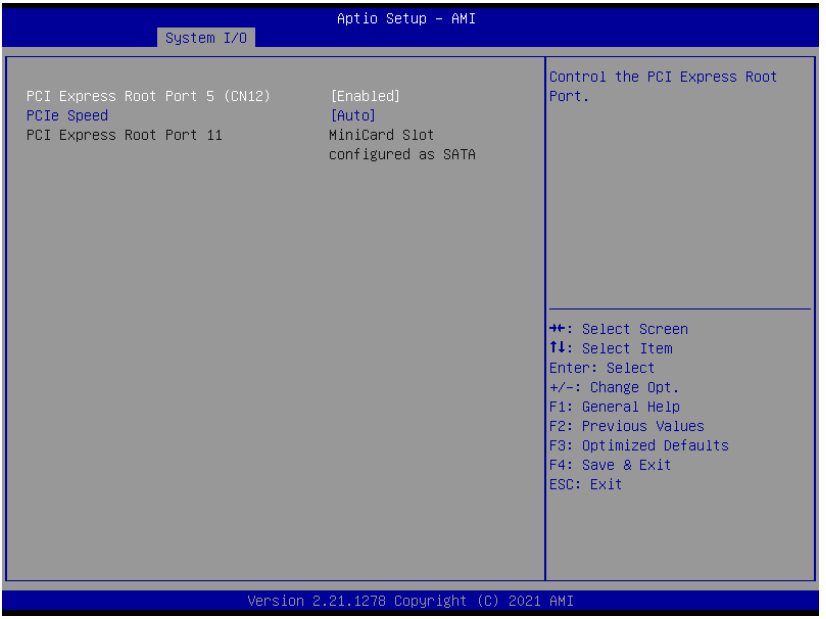


Options Summary		
PCH TSN LAN Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable TSN LAN		
Enable Timed TSN PCS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable TSN PCS. When enabled, TSN PCS device will appear in ACPI table		
PCH TSN Multi-Vc	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable PCH TSN Multi Virtual Channels		
PCH TSN Port #1 Link Speed	RefClk 24Mhz 2.5Gbps	
	RefClk 24Mhz 1Gbps	Optimal Default, Failsafe Default
	RefClk 38.4Mhz 2.5Gbps	
	RefClk 38.4Mhz 1Gbps	
PCH TSN Link Speed config		

3.5 Setup Submenu: System I/O

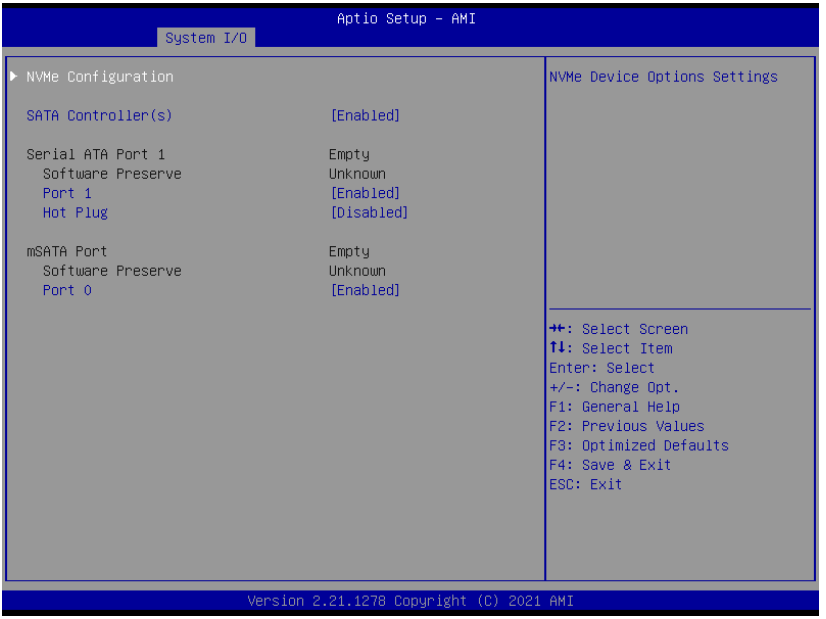


3.5.1 PCI Express Configuration



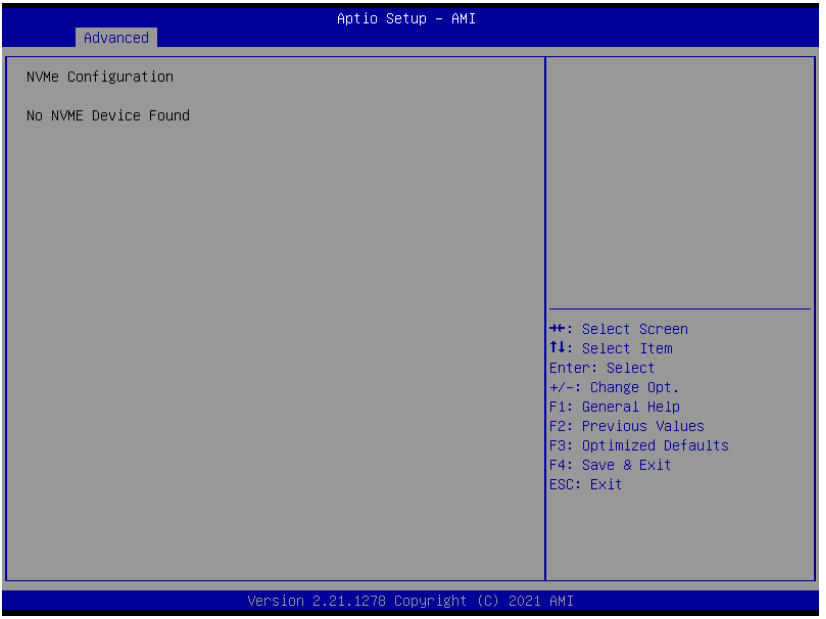
Options Summary		
PCI Express Root Port 5 (CN12) / Port11	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Control the PCI Express Speed		

3.5.2 Storage Configuration

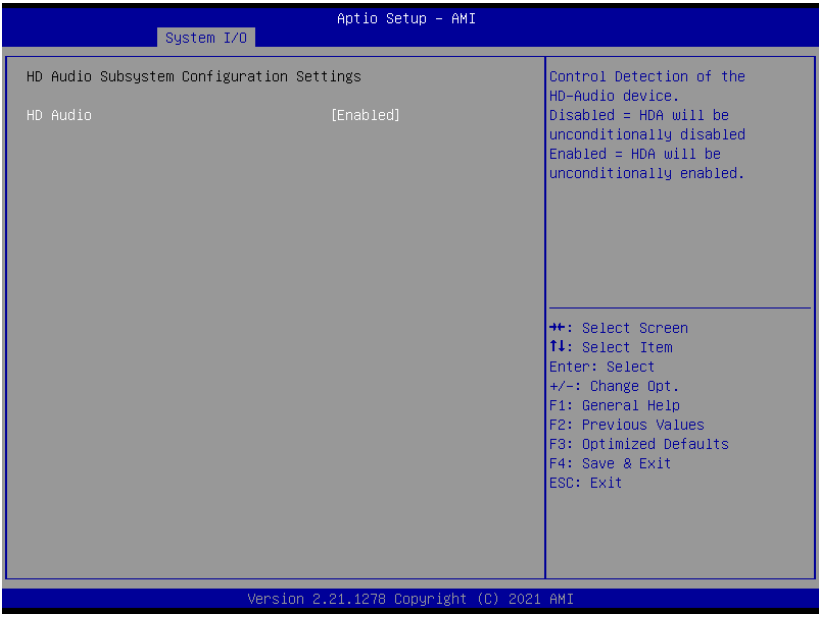


Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
Port 0 / 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.5.2.1 NVMe Configuration

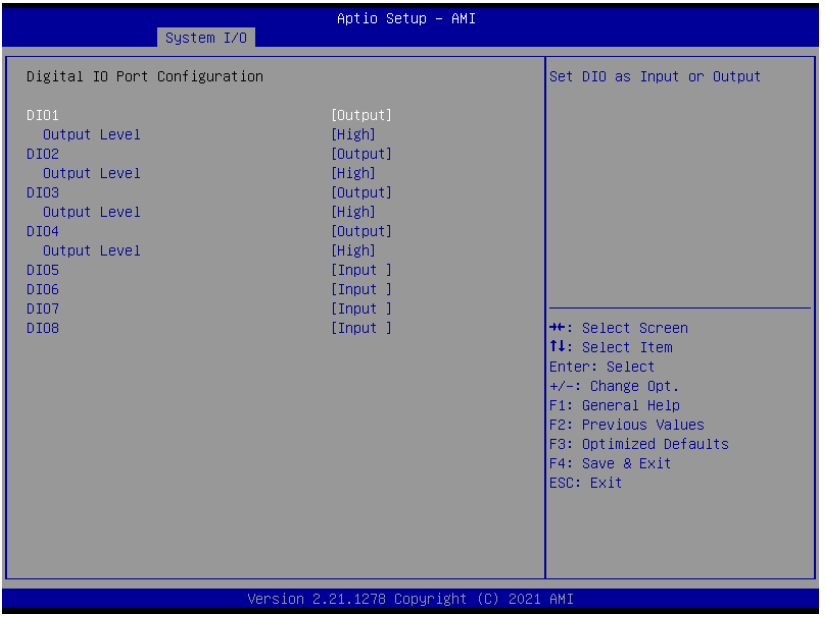


3.5.3 HD Audio Subsystem Configuration Settings



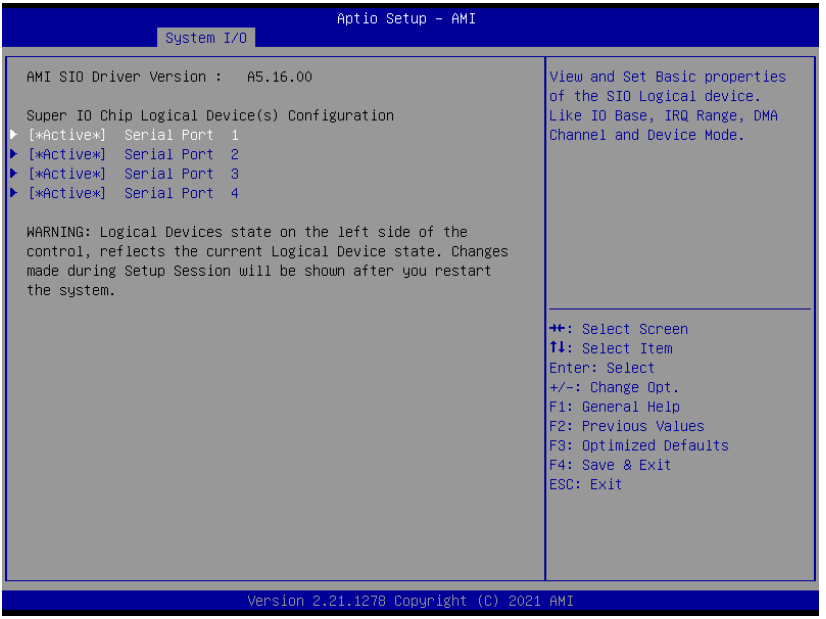
Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		

3.5.4 Digital IO Port Configuration

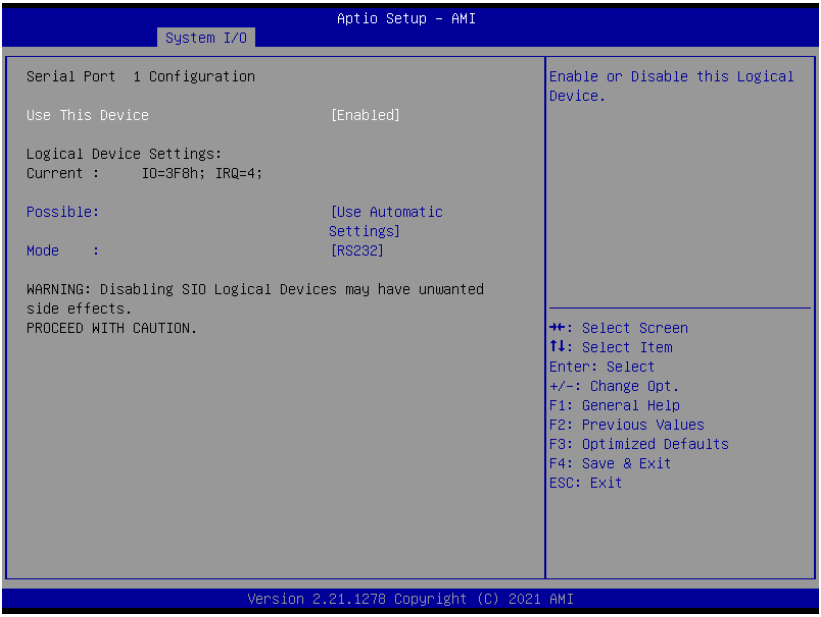


Options Summary		
DIO Port #	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.5.5 Legacy Logical Devices Configuration

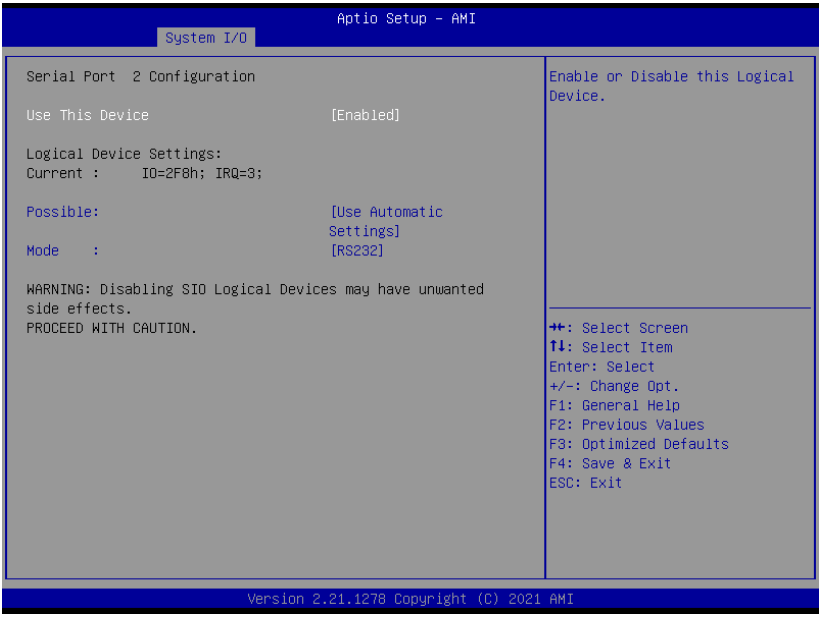


3.5.5.1 Serial Port 1 Configuration



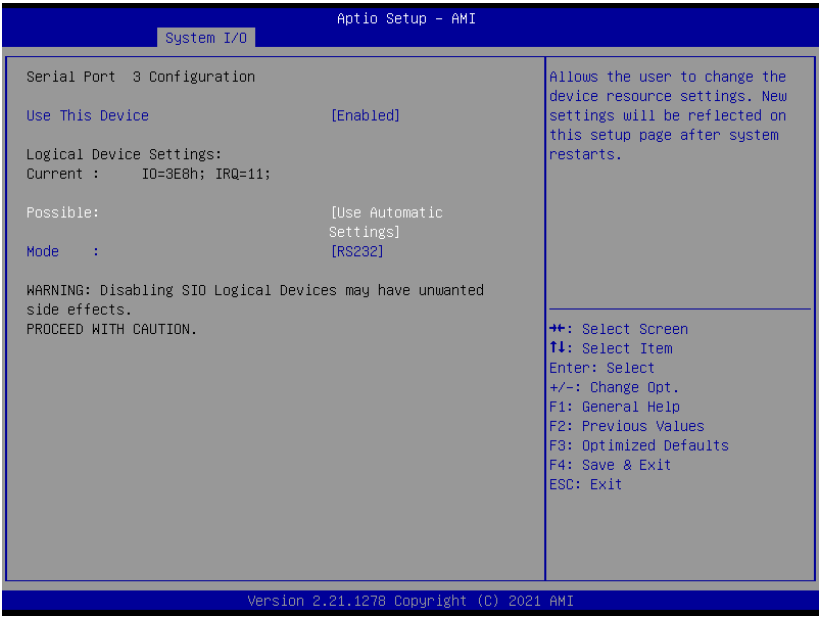
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.2 Serial Port 2 Configuration



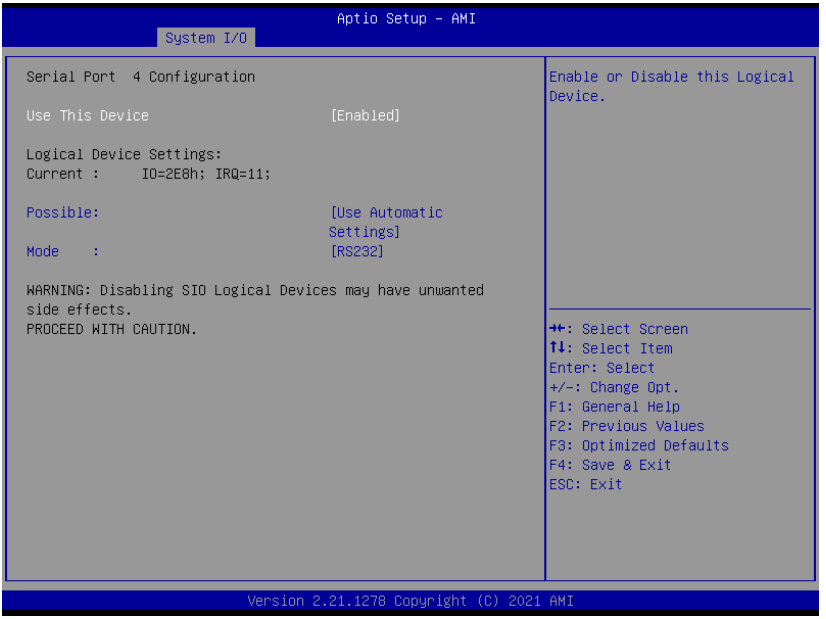
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.3 Serial Port 3 Configuration



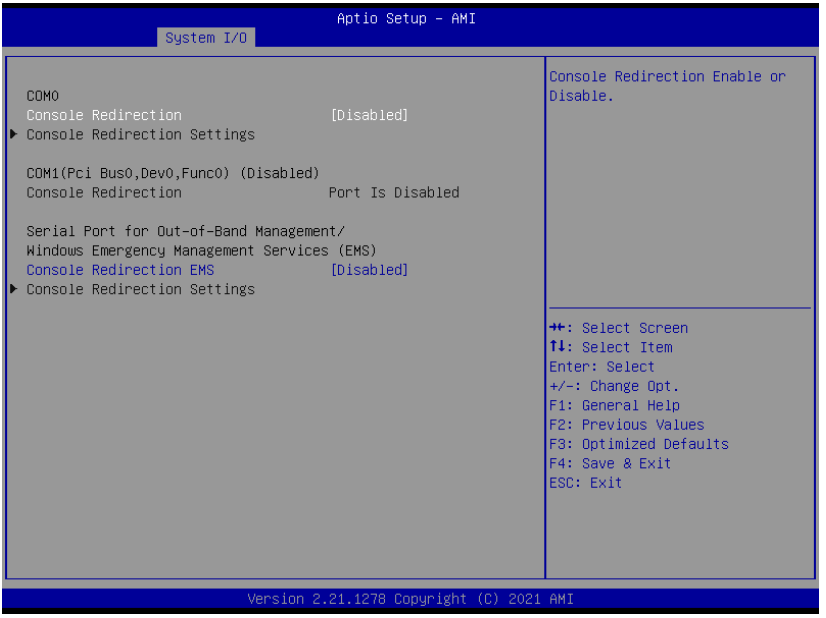
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=11	
	IO=2E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.5.4 Serial Port 4 Configuration



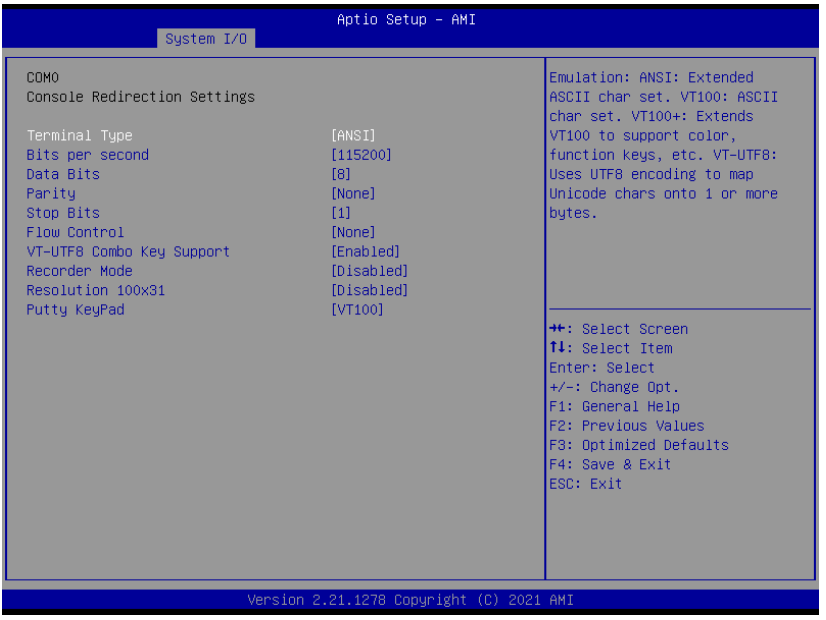
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=11	
	IO=3E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.5.6 Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

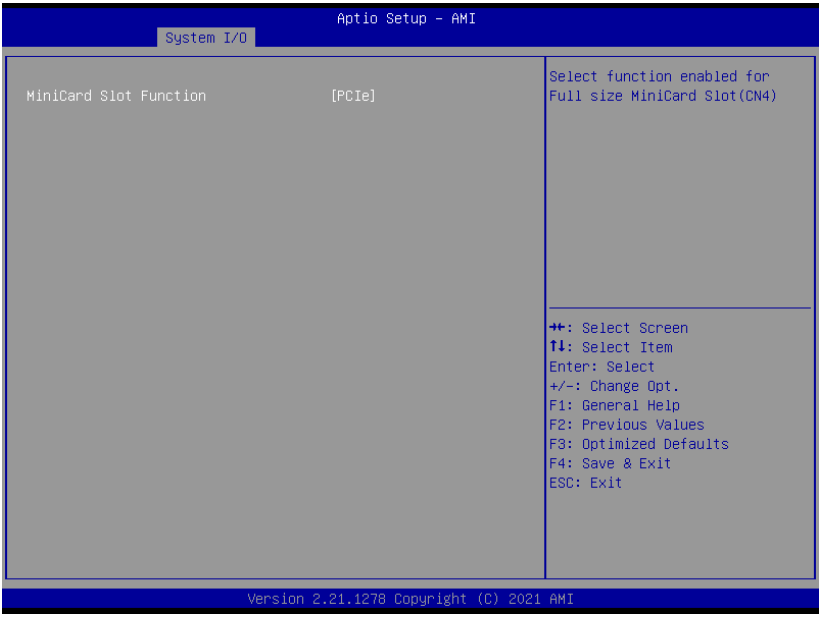
3.5.6.1 Console Redirection Settings



Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits Per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		

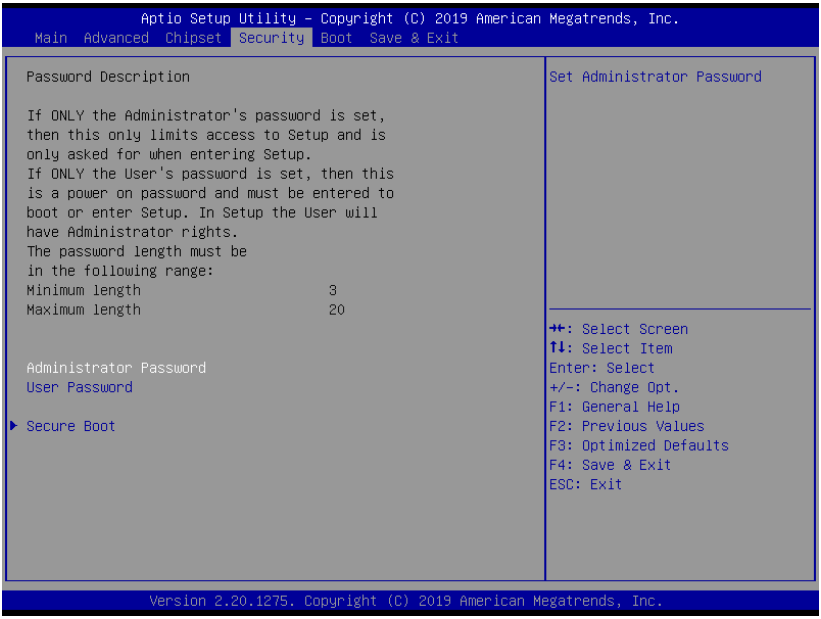
Options Summary		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.5.7 PCH-IO Configuration



Options Summary		
MiniCard Slot Function	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Full size MiniCard Slot (CN10)		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

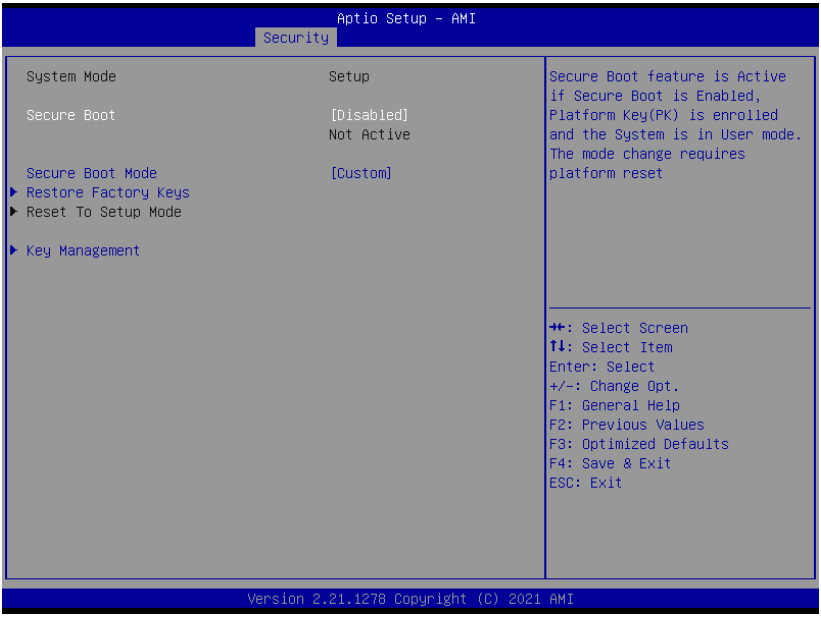
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Trusted Computing

Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

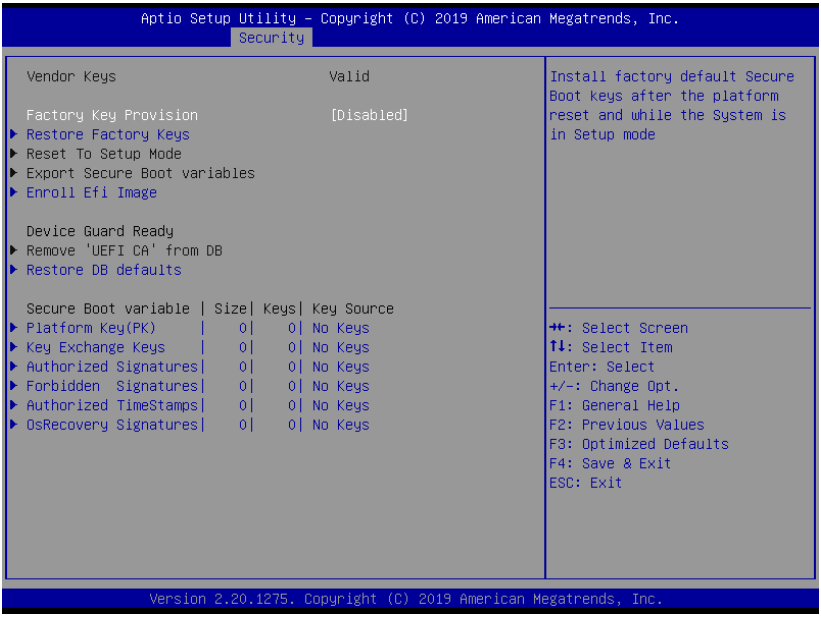
Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.6.2 Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		

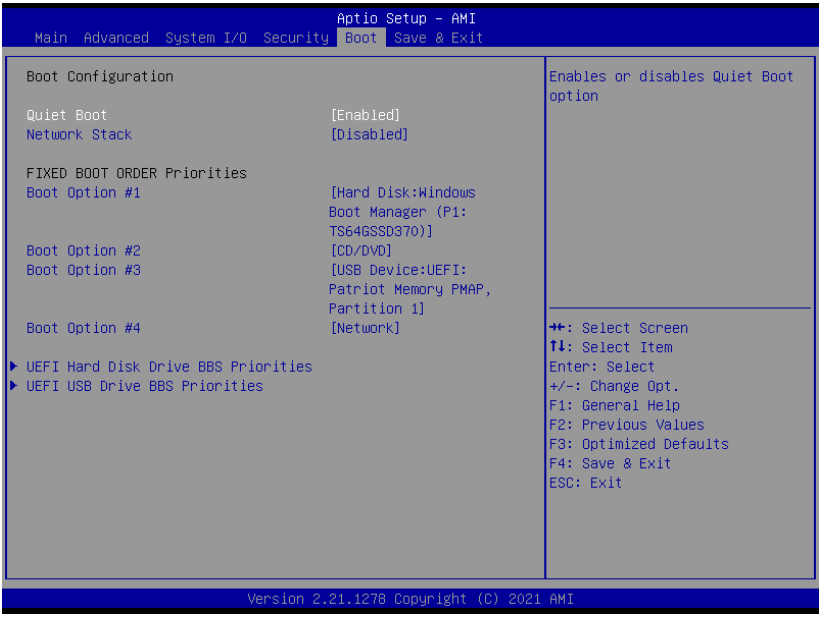
3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults		
Restore DB variable to factory defaults		
Platform Key(PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

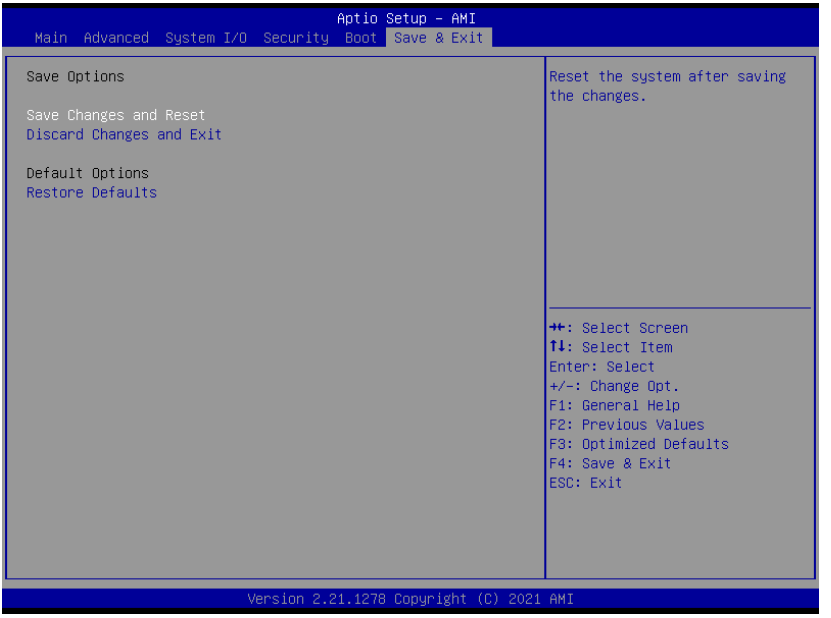
3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables showing boot logo.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

3.7.1 BBS Priorities

3.8 Setup Submenu: Save & Exit



Chapter 4

Driver Installation

4.1 Driver Download/Installation

Drivers for the GENE-TGU6 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/3-and-half-inch-sbc-gene-tgu6

Download the driver(s) you need and follow the steps below to install them.

Audio Driver (Windows 10)

1. Open the folder where you unzipped the **Audio Drivers**
2. Run the **Setup.exe** in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Chipset Driver (Windows 10)

1. Open the folder where you unzipped the **Chipset Drivers**
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Graphics Driver (Windows 10)

1. Open the folder where you unzipped the **Graphics Drivers**
2. Run the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

LAN Drivers (Windows 10)

1. Open the folder where you unzipped the **LAN Drivers**
2. Read the ReadMe.txt file before proceeding. **Caution:** Be sure to install the driver package before installing the Intel® PROSet package.
3. Open the **Wired_driver_26.3_x64** folder
4. Run the **Wired_driver_26.3_x64.exe** file in the folder
5. Follow the instructions, drivers will be installed automatically.
6. After installing the LAN driver, install Intel® PROSet package (optional)
7. Open the **Wired_PROSet_26.3_x64** folder
8. Run the **Wired_PROSet_26.3_x64.exe** file in the folder
9. Follow the instructions
10. Drivers will be installed automatically

ME & TXE Drivers (Windows 10)

1. Open the folder where you unzipped the **ME & TXE Drivers**
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Peripheral Driver (Windows 10)

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Run the **SetupSerialIO.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Touch Drivers (Windows 10)

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Peripheral Driver (Linux)

1. Open the folder where you unzipped the **Peripheral Drivers**
2. Follow the instructions contained within the user guides

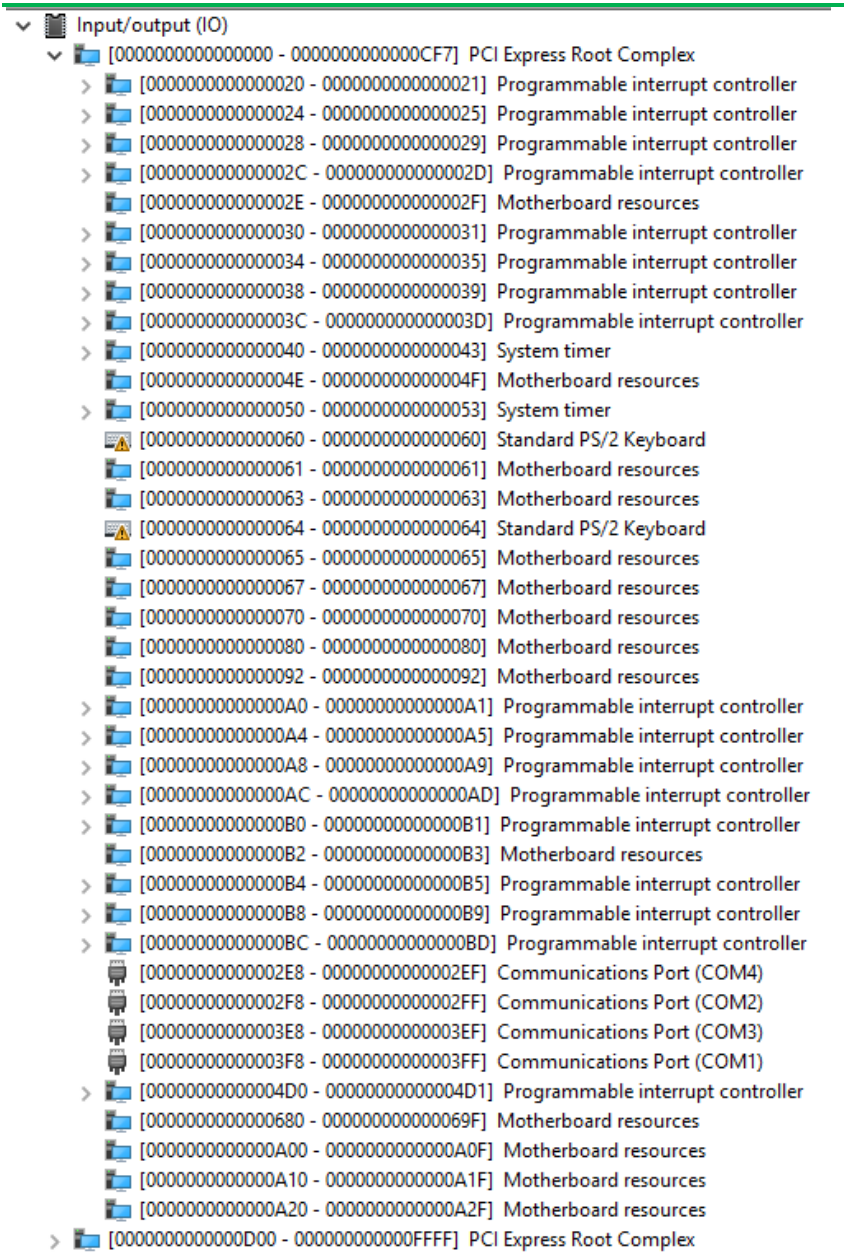
Touch Drivers (Linux)

1. Touch Drivers can be installed via terminal, or through the graphical UI if you have one installed.

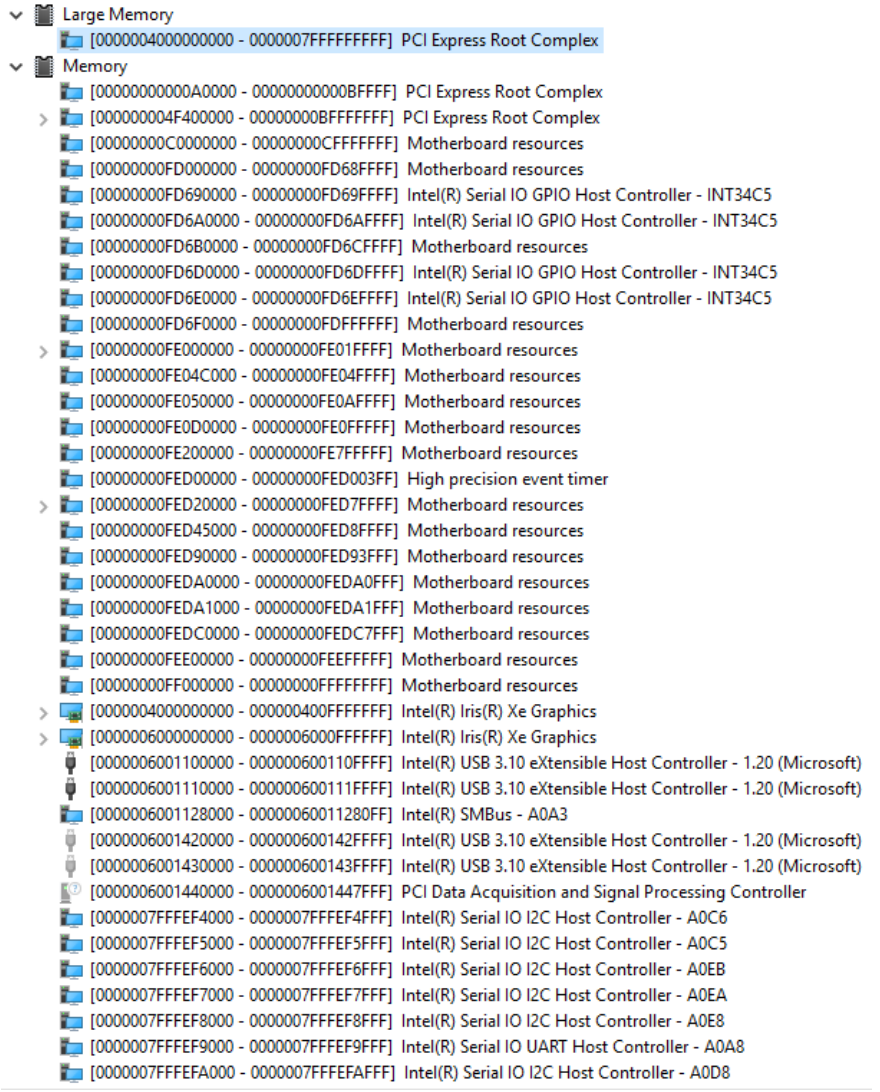
Appendix A

I/O Information

A.1 I/O Address Map

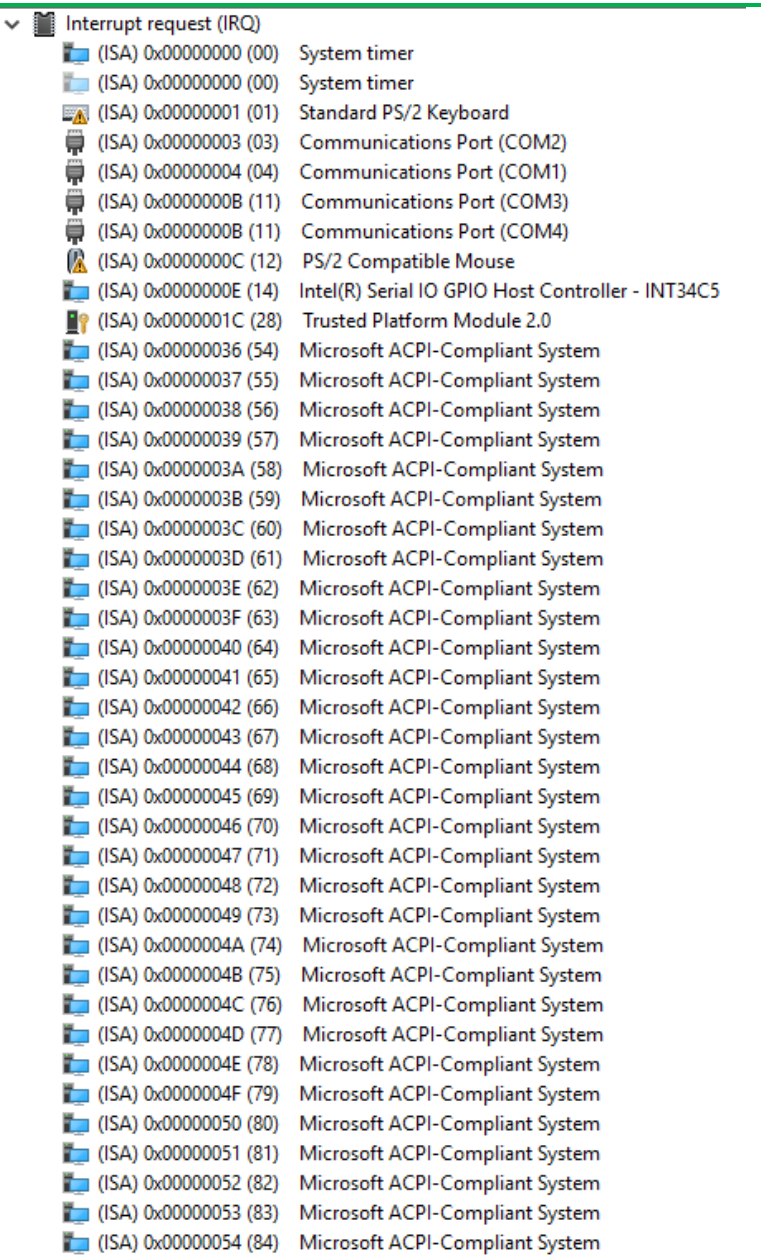


A.2 Memory Address Map



[00000000000A0000 - 00000000000BFFFF] PCI Express Root Complex
[000000004F400000 - 00000000BFFFFFFF] PCI Express Root Complex
[00000000C0000000 - 00000000CFFFFFFF] Motherboard resources
[00000000FD000000 - 00000000FD68FFFF] Motherboard resources
[00000000FD690000 - 00000000FD69FFFF] Intel(R) Serial IO GPIO Host Controller - INT34C5
[00000000FD6A0000 - 00000000FD6AFFFF] Intel(R) Serial IO GPIO Host Controller - INT34C5
[00000000FD6B0000 - 00000000FD6CFFFF] Motherboard resources
[00000000FD6D0000 - 00000000FD6DFFFF] Intel(R) Serial IO GPIO Host Controller - INT34C5
[00000000FD6E0000 - 00000000FD6EFFFF] Intel(R) Serial IO GPIO Host Controller - INT34C5
[00000000FD6F0000 - 00000000FDFFFFFF] Motherboard resources
[00000000FE000000 - 00000000FE01FFFF] Motherboard resources
[00000000FE04C000 - 00000000FE04FFFF] Motherboard resources
[00000000FE050000 - 00000000FE0AFFFF] Motherboard resources
[00000000FE0D0000 - 00000000FE0FFFFF] Motherboard resources
[00000000FE200000 - 00000000FE7FFFFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED20000 - 00000000FED7FFFF] Motherboard resources
[00000000FED45000 - 00000000FED8FFFF] Motherboard resources
[00000000FED90000 - 00000000FED93FFF] Motherboard resources
[00000000FEDA0000 - 00000000FEDA0FFF] Motherboard resources
[00000000FEDA1000 - 00000000FEDA1FFF] Motherboard resources
[00000000FEDC0000 - 00000000FEDC7FFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF] Motherboard resources
[0000004000000000 - 000000400FFFFFFF] Intel(R) Iris(R) Xe Graphics
[0000006000000000 - 0000006000FFFFFF] Intel(R) Iris(R) Xe Graphics
[0000006001100000 - 000000600110FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
[0000006001110000 - 000000600111FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
[0000006001128000 - 00000060011280FF] Intel(R) SMBus - A0A3
[0000006001420000 - 000000600142FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
[0000006001430000 - 000000600143FFFF] Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
[0000006001440000 - 0000006001447FFF] PCI Data Acquisition and Signal Processing Controller
[0000007FFFEF4000 - 0000007FFFEF4FFF] Intel(R) Serial IO I2C Host Controller - A0C6
[0000007FFFEF5000 - 0000007FFFEF5FFF] Intel(R) Serial IO I2C Host Controller - A0C5
[0000007FFFEF6000 - 0000007FFFEF6FFF] Intel(R) Serial IO I2C Host Controller - A0EB
[0000007FFFEF7000 - 0000007FFFEF7FFF] Intel(R) Serial IO I2C Host Controller - A0EA
[0000007FFFEF8000 - 0000007FFFEF8FFF] Intel(R) Serial IO I2C Host Controller - A0E8
[0000007FFFEF9000 - 0000007FFFEF9FFF] Intel(R) Serial IO UART Host Controller - A0A8
[0000007FFFEFA000 - 0000007FFFEFAFFF] Intel(R) Serial IO I2C Host Controller - A0D8
[0000007FFFEFB000 - 0000007FFFEFBFFF] Intel(R) Serial IO SPI Host Controller - A0AB
[0000007FFFEFC000 - 0000007FFFEFFFFF] High Definition Audio Controller
[0000007FFFF00000 - 0000007FFFFFFFFF] High Definition Audio Controller

A.3 IRQ Mapping Chart



(ISA) 0x000001E7 (487) Microsoft ACPI-Compliant System
(ISA) 0x000001E8 (488) Microsoft ACPI-Compliant System
(ISA) 0x000001E9 (489) Microsoft ACPI-Compliant System
(ISA) 0x000001EA (490) Microsoft ACPI-Compliant System
(ISA) 0x000001EB (491) Microsoft ACPI-Compliant System
(ISA) 0x000001EC (492) Microsoft ACPI-Compliant System
(ISA) 0x000001ED (493) Microsoft ACPI-Compliant System
(ISA) 0x000001EE (494) Microsoft ACPI-Compliant System
(ISA) 0x000001EF (495) Microsoft ACPI-Compliant System
(ISA) 0x000001F0 (496) Microsoft ACPI-Compliant System
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0x00000010 (16) Intel(R) Serial IO UART Host Controller - A0A8
(PCI) 0x00000012 (18) Intel(R) Serial IO I2C Host Controller - A0D8
(PCI) 0x0000001B (27) Intel(R) Serial IO I2C Host Controller - A0E8
(PCI) 0x0000001D (29) Intel(R) Serial IO I2C Host Controller - A0EA
(PCI) 0x0000001E (30) Intel(R) Serial IO I2C Host Controller - A0EB
(PCI) 0x0000001F (31) Intel(R) Serial IO I2C Host Controller - A0C5
(PCI) 0x00000020 (32) Intel(R) Serial IO I2C Host Controller - A0C6
(PCI) 0x00000025 (37) Intel(R) Serial IO SPI Host Controller - A0AB
(PCI) 0xFFFFFFF8 (-8) Intel(R) Ethernet Connection (13) I219-LM
(PCI) 0xFFFFFFF9 (-7) Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFFA (-6) Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFFB (-5) Intel(R) Iris(R) Xe Graphics
(PCI) 0xFFFFFFFC (-4) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFD (-3) Intel(R) PCI Express Root Port #1 - A0B8
(PCI) 0xFFFFFFFE (-2) Intel(R) PCI Express Root Port #8 - A0BF

Appendix B

Mating Connectors and Cables

B.1 Mating Connectors and Cables

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
JP1	Front Panel Connector	Flyingway	FWAA-1049	LED cable	1709100108
CN1	+5Vout Connector	PINREX	PHR-2	2 Pins for HDD Power	1702150155
CN2	SATA Connector	Molex	887505318	SATA Cable	1709070460
CN3	+9~36V Vin Connector	N/A	N/A	Power Cable	170204010R
CN5	Audio Connector	ACES	50247-012H0 H0-001	Audio Cable	170X000156
CN6	External +5VSB Power Input and PS_ON#	JST	PHR-3	ATX Cable	170220020B
CN8	COM Port 3/4 Connector	ACES	50247-020H0 H0-001	Serial Port Cable	170X000231
CN13	COM Port 1/2 Connector	ACES	50247-020H0 H0-001	Serial Port Cable	170X000231
CN15	Touch Screen Connector	JST	SHR-9V-S-B	N/A	N/A
CN16	I2C/SM BUS/Debug Connector	Molex	51021-1200	I2C/SM BUS Cable	1703120130

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN17	Digital I/O Connector	Neltron	2026B-10	N/A	N/A
CN18	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN21	USB Port Connector	Aces	50238-01041-003	USB Wafer Cable	170010010D
CN22	LVDS Inverter Connector	Aces	50228-00671-001	Inverter cable	170X000152
CN23	CPU Fan Connector	Molex	22-01-2035	N/A	N/A
CN31	External RTC Connector	Molex	51021-0200	Battery Cable	175011901C