

GENE-SKU6

3.5" Subcompact Board

User's Manual 1st Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● GENE-SKU6 with heat spreader	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
18. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 此产品所标示之环保使用期限, 系指在一般正常使用状况下。</p>						

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
<p>O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.</p> <p>X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.</p> <p>Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only</p>						

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Chapter 1

Product Specifications

1.1 Specifications

System

● Form Factor	3.5"
● CPU	Intel® Core™ i3/i5/i7 processor SoC
● CPU Frequency	Up to 2.4/3.0 GHz
● Chipset	Intel® Core™ i3/i5/i7 processor SoC
● Memory Type	DDR4 1866/2133 SODIMM x 1
● Max Memory Capacity	16 GB
● BIOS	UEFI
● Wake On LAN	Yes
● Watchdog Timer	255 levels
● Power Requirement	+12 V or 9 ~ 36 V
● Power Supply Type	AT/ATX
● Power Consumption (Typical)	Intel® i7-6600U, DDR4 2133MHz 16G, 1.75A@ +12V
● Dimensions (L x W)	146 x 101.7 mm (5.75 x 4")
● Operating Temperature	0 ~ 60°C (32 ~ 140°F)
● Storage Temperature	-40 ~ 81°C (-40 ~ 176°F)
● Operation Humidity	10 ~ 90% relative humidity, non-condensing
● MTBF	123,000
● Certification	CE/FCC

Display

- **VGA/LCD Controller** Intel® Core™ i3/i5/i7 processor SoC
- **Video Output** DVI, CRT/DP, LVDS
(CRT is shared with DP, and default is DP)
- **Backlight Inverter Supply** Yes

I/O

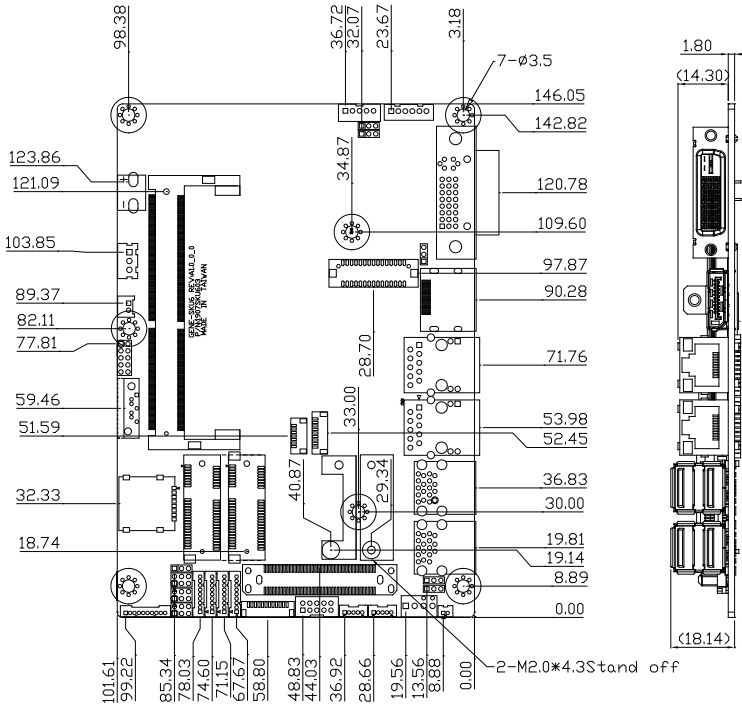
- **Ethernet** Intel I210, 10/100/1000Base , RJ-45 x 2 (supports EtherCAT)
- **Audio** High definition audio interface
- **USB** USB 3.0 x 4
USB 2.0 x 2
- **Serial Port** RS-232 x 1
RS-232/422/485 x 3
- **HDD Interface** SATA 3.0 Gb/s x 1
+5 SATA power connector x 1
- **SSD** mSATA (shared with half-size Mini-Card, select with BIOS)
- **Expansion Slot** 1. BIO x 1 (option)
2. Mini Card x 2 and default is
2.1. mSATA x 1 (half-size)
2.2. miniCard x 1(Full-size)
- **DI/O** 8-bit
- **TPM** TPM2.0 x 1(option)
- **Touch** 1

Chapter 2

Hardware Information

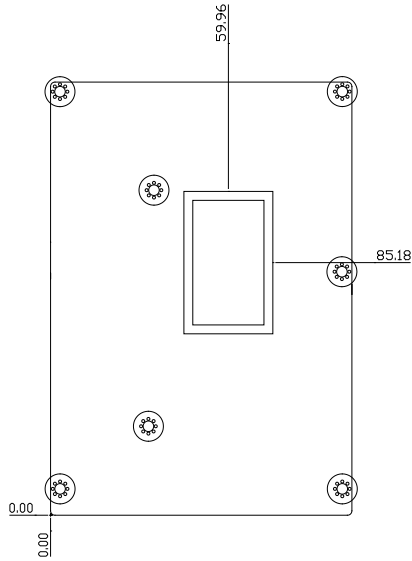
2.1 Dimensions

Component Side

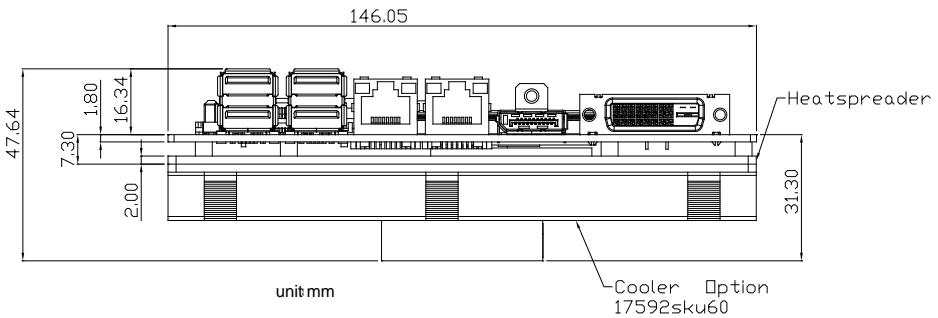


Component Side

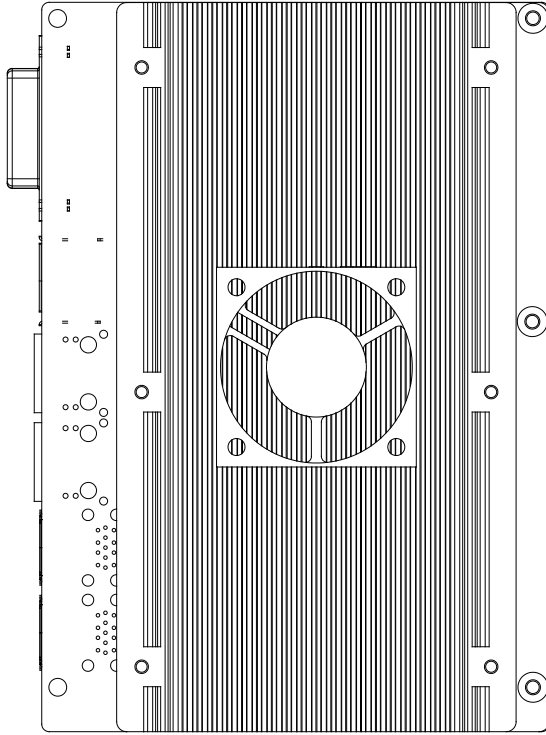
Solder Side (with heat spreader)



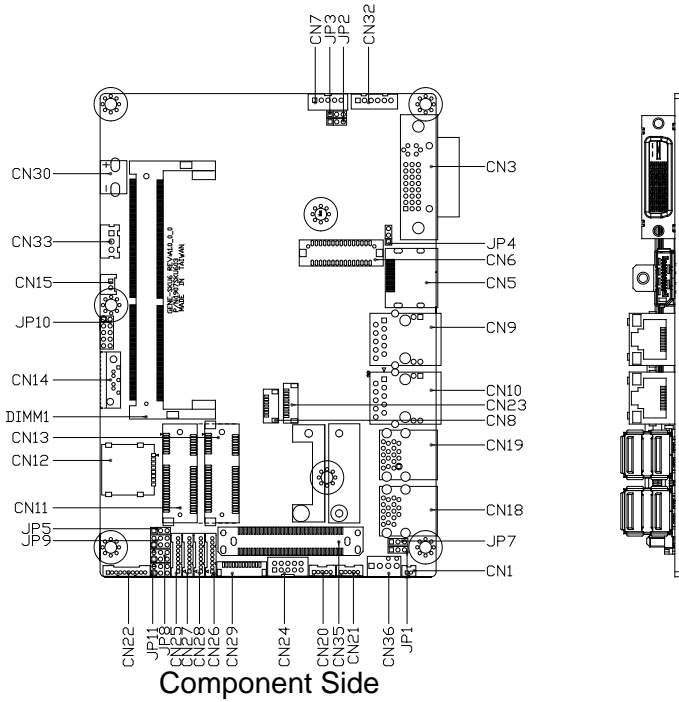
Solder Side



Cooler Option (Part Number: 17592SKU60)

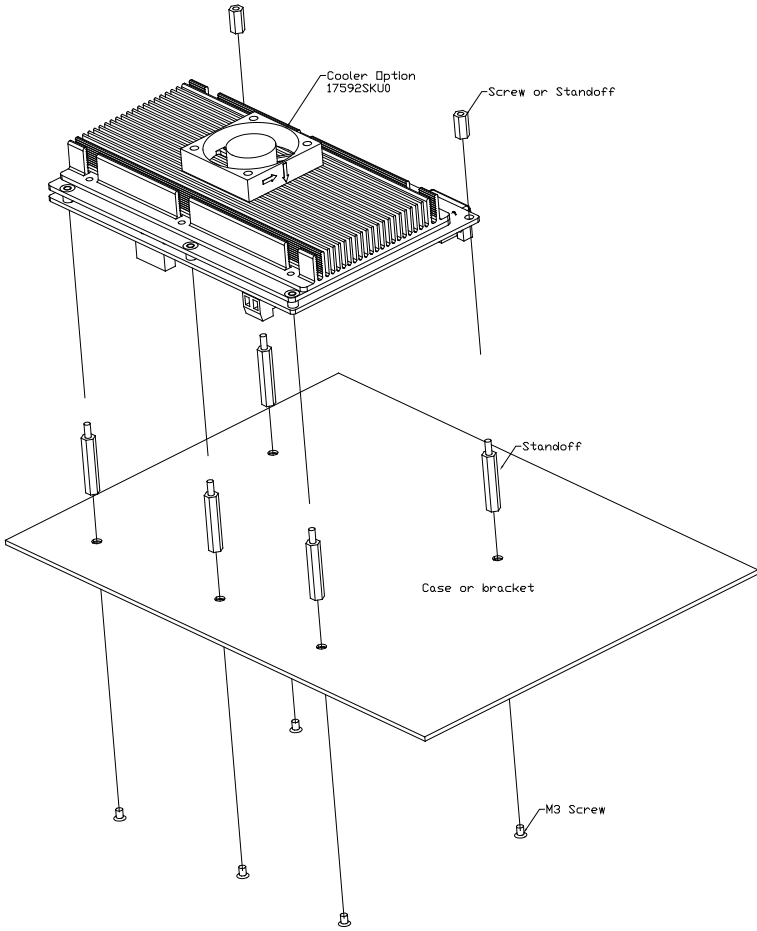


2.2 Jumpers and Connectors

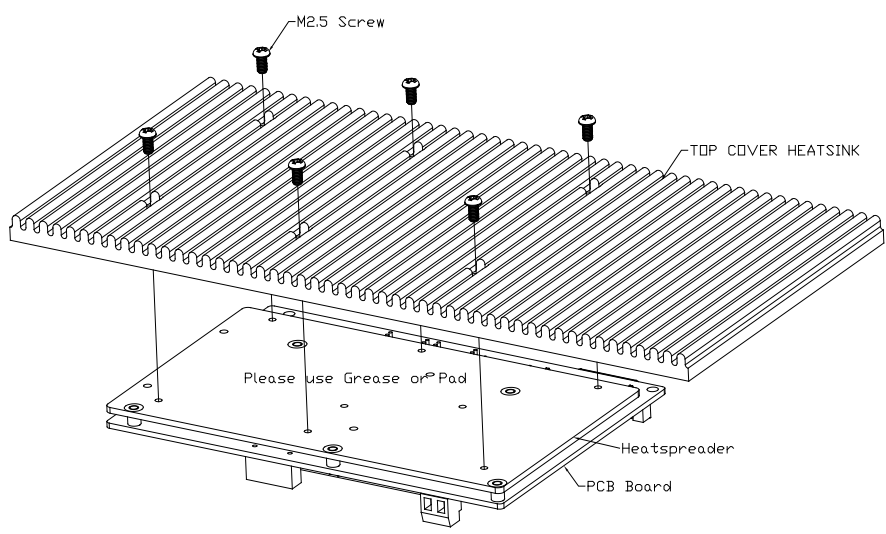


2.3 Assembly Options

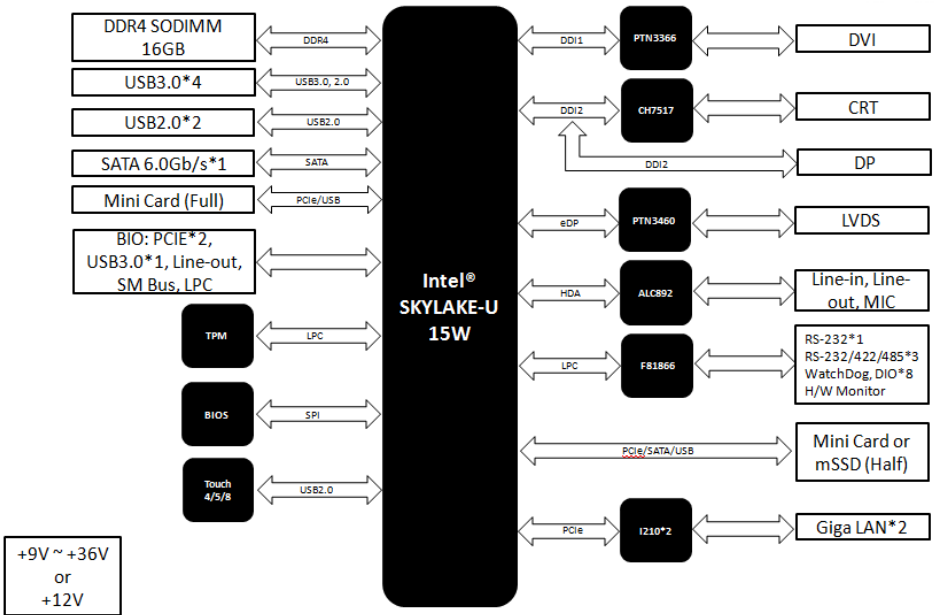
Option 1



Option 2



2.4 Block Diagram

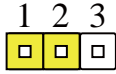


2.5 List of Jumpers

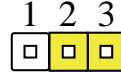
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	Clear CMOS Jumper
JP2	LVDS Port Backlight Inverter VCC Selection
JP3	LVDS Port Backlight Lightness Control Mode Selection
JP4	LVDS Port Operating VDD Selection
JP5	mSATA/Mini-Card Operating VCC Selection
JP6	Touch Screen 4/5/8-wire Mode Selection
JP7	Auto Power Button Enable/Disable Selection
JP8	COM3 Pin8 Function Selection
JP9	COM2 Pin8 Function Selection
JP10	Front Panel Connector
JP11	COM4 Pin8 Function Selection

2.5.1 Clear CMOS Jumper (JP1)

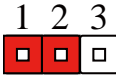


Normal (Default)

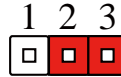


Clear CMOS

2.5.2 LVDS Port Backlight Inverter VCC Selection (JP2)

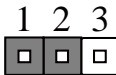


+12V

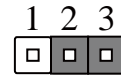


+5V (Default)

2.5.3 LVDS Port Backlight Lightness Control Mode Selection (JP3)

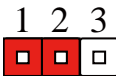


VR Mode (Default)

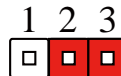


PWM Mode

2.5.4 LVDS Port Operating VDD Selection (JP4)

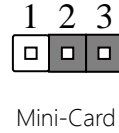
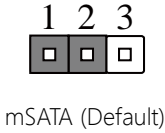


+5V

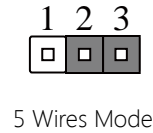
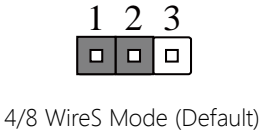


+3.3V (Default)

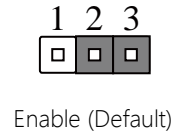
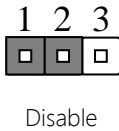
2.5.5 mSATA/ Mini-Card Operating VCC Selection (JP5)



2.5.6 Touch Screen 4,5,8 Wire Selection (JP6)

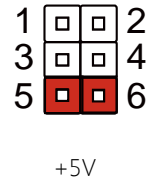
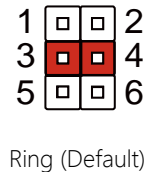
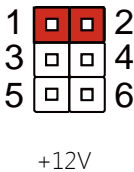


2.5.7 Auto Power Button Enable/Disable Selection (JP7)

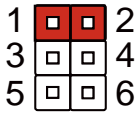


* When disabled, use power button JP10(1-2) to power on the system.

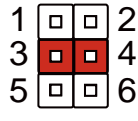
2.5.8 COM3 Pin8 Function Selection (JP8)



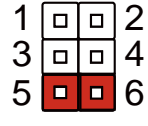
2.5.9 COM3 Pin8 Function Selection (JP9)



+12V

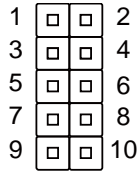


Ring (Default)



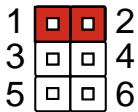
+5V

2.5.10 Front Panel Connector (JP10)

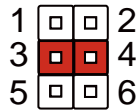


Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

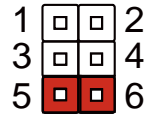
2.5.11 COM4 Pin8 Function Selection (JP11)



+12V



Ring (Default)



+5V

2.6 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	Battery
CN3	DVI-I (Digital and Analog)
CN5	DP Port
CN6	LVDS Port
CN7	LVDS Port Inverter / Backlight Connector
CN8	SPI Debug Port
CN9	LAN (RJ-45) Port1
CN10	LAN (RJ-45) Port2
CN11	Mini-Card Slot (Full-Mini Card)
CN12	Micro SIM Card Socket
CN13	Mini-Card Slot (Half-Mini Card)
CN14	SATA Port
CN15	+5V Output for SATA HDD
CN18	USB 3.0 Ports
CN19	USB 3.0 Ports
CN20	USB 2.0 Port
CN21	USB 2.0 Port
CN22	Audio I/O Port
CN23	Touch Screen Connector
CN24	Digital IO Port
CN25	COM Port 1
CN26	COM Port 4
CN27	COM Port 2

CN28	COM Port 3
CN29	LPC Port
CN30	External Power Input
CN32	+5VSB Output w/SMBus
CN33	External +5VSB Input
CN35	BIO Connector
CN36	CPU FAN

2.6.1 Battery (CN1)

Pin	Pin Name	Signal Type	Signal level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.6.2 DVI-I (Digital and Analog) (CN2)

Pin	Pin Name	Signal Type	Signal Level
1	DVI_D2-	OUT	
2	DVI_D2+	OUT	
3	GND	GND	
4	VGA_DDC_CLK	I/O	
5	VGA_DDC_DAT	I/O	
6	SCL	I/O	
7	SDA	I/O	
8	VGA_VSYNC	OUT	
9	DVI_D1-	OUT	
10	DVI_D1+	OUT	
11	GND	GND	
12	NC		
13	NC		
14	+5V	PWR	+5V
15	GND	GND	
16	HPD	IN	
17	DVI_D0-	OUT	
18	DVI_D0+	OUT	
19	GND	GND	

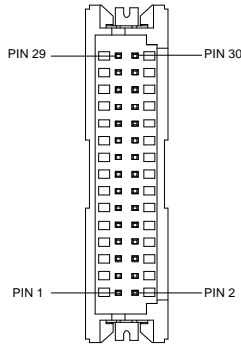
20	NC	
21	NC	
22	GND	GND
23	DVI_CLK+	OUT
24	DVI_CLK-	OUT
C1	VGA_RED	OUT
C2	VGA_GREEN	OUT
C3	VGA_BLUE	OUT
C4	VGA_HSYNC	OUT

2.6.3 DP Port (CN5)

Pin	Pin Name	Signal Type	Signal Level
1	DP_D0+	DIFF	
2	GND	GND	
3	DP_D0-	DIFF	
4	DP_D1+	DIFF	
5	GND	GND	
6	DP_D1-	DIFF	
7	DP_D2+	DIFF	
8	GND	GND	
9	DP_D2-	DIFF	
10	DP_D3+	DIFF	
11	GND	GND	
12	DP_D3-	DIFF	
13	GND	GND	
14	GND	GND	
15	DP_AUX+	DIFF	

16	GND	GND	
17	DP_AUX-	DIFF	
18	HPLG_DETECT	IN	
19	GND	GND	
20	+5V	I/O	+5V

2.6.4 LVDS Port (CN6)

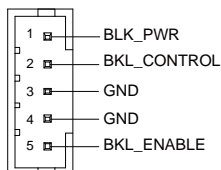


*LVDS LCD_PWR can be set to +3.3V or +5V by JP4

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	

11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.6.5 LVDS Port Inverter / Backlight Connector (CN7)



Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+5V

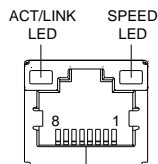
* LVDS BKL_PWR can be set to +5V or +12V by JP2

* LVDS BKL_CONTROL can be set by JP3

2.6.6 BIOS Debug Port (CN6)

Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

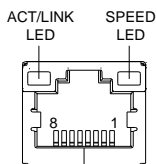
2.6.7 LAN (RJ-45) Port1 (CN9)



Pin	Pin Name	Signal Type	Signal level
1	MDIO+	DIFF	

2	MDI0-	DIFF
3	MDI1+	DIFF
4	MDI2+	DIFF
5	MDI2-	DIFF
6	MDI1-	DIFF
7	MDI3+	DIFF
8	MDI3-	DIFF

2.6.8 LAN (RJ-45) Port2 (CN10)



Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.6.9 Mini-Card Slot (Full-Mini Card) (CN11)

Pin	Pin Name	Signal Type	Signal level
1	PCIE_WAKE#	IN	

2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V

29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.6.10 Micro SIM Card Socket (CN12)

Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	NC		
5	GND	GND	
6	UIM_VPP	PWR	
7	UIM_DATA	I/O	
8	NC		

2.6.11 Mini-Card Slot (Full-Mini Card) (CN13)

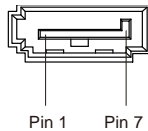
Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC		
9	GND	GND	
10	NC		
11	PCIE_REF_CLK-	DIFF	
12	NC		

13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC		
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-/mSATA_RX+	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+/mSATA_RX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-/mSATA_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+/mSATA_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V

40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

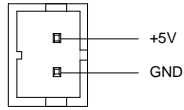
* CN13 can be selected for Mini-Card or mSATA by changing BIOS

2.6.12 SATA Port 1 (CN14)



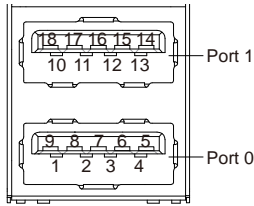
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.6.13 +5V Output for SATA HDD (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

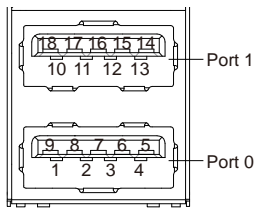
2.6.14 USB 3.0 Ports (CN18)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	USB_SSRX-	DIFF	
6	USB_SSRX+	DIFF	
7	GND	GND	
8	USB_SSTX-	DIFF	
9	USB_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB_D-	DIFF	
12	USB_D+	DIFF	

13	GND	GND
14	USB_SSRX-	DIFF
15	USB_SSRX+	DIFF
16	GND	GND
17	USB_SSTX-	DIFF
18	USB_SSTX+	DIFF

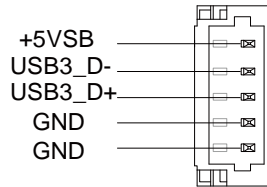
2.6.15 USB 3.0 Ports (CN19)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	USB_SSRX-	DIFF	
6	USB_SSRX+	DIFF	
7	GND	GND	
8	USB_SSTX-	DIFF	
9	USB_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB_D-	DIFF	
12	USB_D+	DIFF	
13	GND	GND	

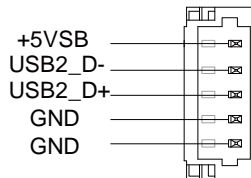
14	USB_SSRX-	DIFF
15	USB_SSRX+	DIFF
16	GND	GND
17	USB_SSTX-	DIFF
18	USB_SSTX+	DIFF

2.6.16 USB 2.0 Port (CN20)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	GND	GND	

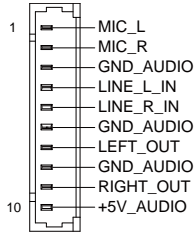
2.6.17 USB 2.0 Port (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V

2	USB_D-	DIFF
3	USB_D+	DIFF
4	GND	GND
5	GND	GND

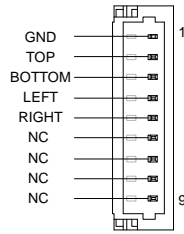
2.6.18 Audio I/O Port (CN22)



Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

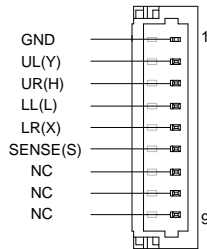
2.6.19 Touchscreen Connector (CN23)

* Touch mode can be set by JP6



4-Wire

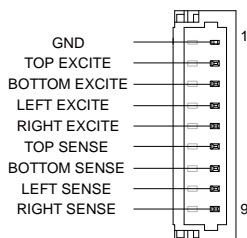
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		



5-Wire

Pin	Pin Name	Signal Type	Signal Level
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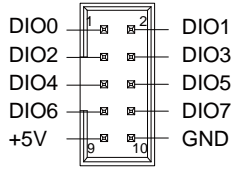
1	GND	GND
2	UL(Y)	IN
3	UR(H)	IN
4	LL(L)	IN
5	LR(X)	IN
6	SENSE(S)	IN
7	NC	
8	NC	
9	NC	



8-Wire

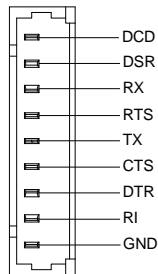
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	
8	LEFT SENSE	IN	
9	RIGHT SENSE	IN	

2.6.20 Digital I/O Port (CN24)



Pin	Pin Name	Signal Type	Signal Level
1	DIO0	I/O	+5V
2	DIO1	I/O	+5V
3	DIO2	I/O	+5V
4	DIO3	I/O	+5V
5	DIO4	I/O	+5V
6	DIO5	I/O	+5V
7	DIO6	I/O	+5V
8	DIO7	I/O	+5V
9	+5V	PWR	+5V
10	GND	GND	

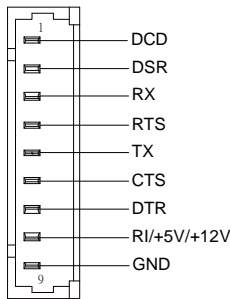
2.6.21 COM Port 1 (CN25)



Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	

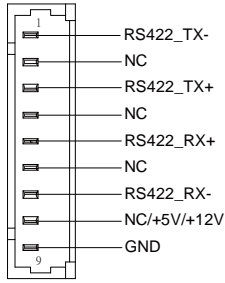
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.6.22 COM Port 4 (CN26)



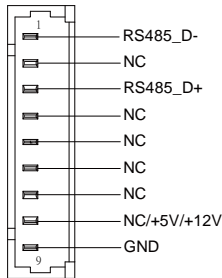
RS-232

Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



RS-485

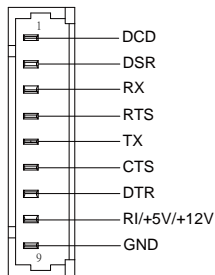
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		

3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM4 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

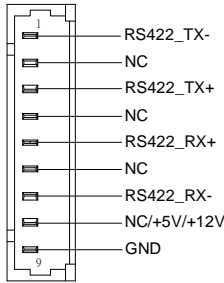
* Pin 8 function can be set by JP11.

2.6.23 COM Port 2 (CN27)



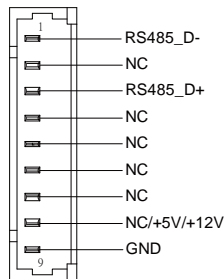
RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V

8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



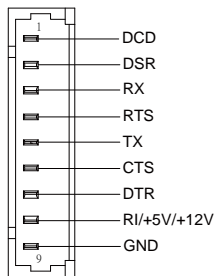
RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

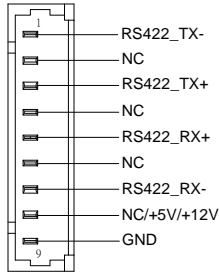
* Pin 8 function can be set by JP9.

2.6.24 COM Port 3 (CN28)



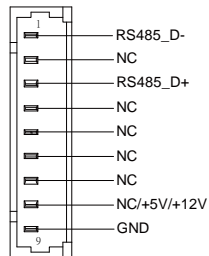
RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V

5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



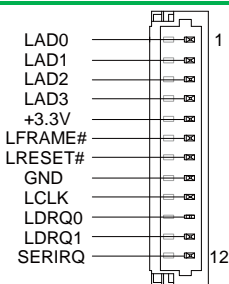
RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM3 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

* Pin 8 function can be set by JP8.

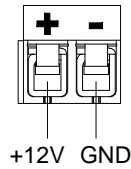
2.6.25 LPC Port (CN29)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V

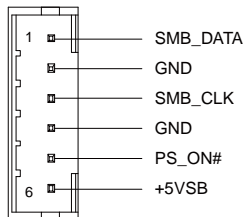
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.6.26 External Power Input (CN30)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+9~+24V (or +12V)
2	GND	GND	

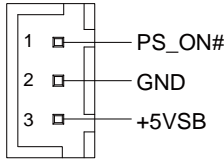
2.6.27 +5VSB Output w/SMBus (CN32)



Pin	Pin Name	Signal Type	Signal Level
1	SMB_DATA	I/O	+3.3V
2	GND	GND	
3	SMB_CLK	I/O	+3.3V

4	GND	GND	
5	PS_ON#	OUT	+3.3V
6	+5VSB	PWR	+5V

2.6.28 External +5VSB Input (CN33)



Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+3.3V
2	GND	GND	
3	+5VSB	PWR	+5V

2.6.29 BIO Connector (CN35)

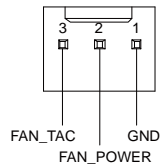
Pin	Pin Name	Signal Type	Signal Level
1	+12V_Dual	PWR	+12V
2	GND	GND	
3	GND	GND	
4	PCIE1_TX-	I/O	
5	PCIE1_RX-	I/O	
6	PCIE1_TX+	I/O	
7	PCIE1_RX+	I/O	
8	GND	GND	
9	GND	GND	
10	PCIE2_TX-	I/O	

11	PCIE2_RX-	I/O	
12	PCIE2_TX+	I/O	
13	PCIE2_RX+	I/O	
14	GND	GND	
15	GND	GND	
16	PS_ON#	OUT	
17	NC		
18	NC		
19	+5V_Dual	PWR	+5V
20	+5V_Dual	PWR	+5V
21	+5V_Dual	PWR	+5V
22	+5V_Dual	PWR	+5V
23	PCIE_CLK+	OUT	
24	PLT_RST#	OUT	
25	PCIE_CLK-	OUT	
26	GND	GND	
27	GND	GND	
28	NC		
29	NC		
30	NC		
31	NC		
32	GND	GND	
33	GND	GND	
34	NC		
35	NC		
36	NC		
37	NC		

38	GND	GND	
39	GND	GND	
40	NC		
41	NC		
42	GND	GND	
43	NC		
44	USB 3.0_TX-	I/O	
45	GND	GND	
46	USB 3.0_TX+	I/O	
47	USB 2.0_D-	I/O	
48	GND	GND	
49	USB 2.0_D+	I/O	
50	USB 3.0_RX-	I/O	
51	GND	GND	
52	USB 3.0_RX+	I/O	
53	SMB_CLK	I/O	
54	GND	GND	
55	SMB_DATA	I/O	
56	PCIE_WAKE#	IN	
57	GND	GND	
58	USB 2.0_OC#	IN	
59	+5V	PWR	+5V
60	USB 2.0_OC#	IN	
61	+5V	PWR	+5V
62	+5V	PWR	+5V
63	+5V	PWR	+5V
64	+5V	PWR	+5V

65	LPC_AD0	I/O
66	LPC_FRAME#	I/O
67	LPC_AD1	I/O
68	SERIRQ#	I/O
69	LPC_AD2	I/O
70	NC	
71	LPC_AD3	I/O
72	GPIO	I/O
73	GND	GND
74	Audio_GND	GND
75	LPC_CLK	OUT
76	Audio_OUT_L	OUT
77	PME#	IN
78	Audio_OUT_R	OUT
79	GND	GND
80	GND	GND

2.6.30 CPU Fan (CN36, Optional)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

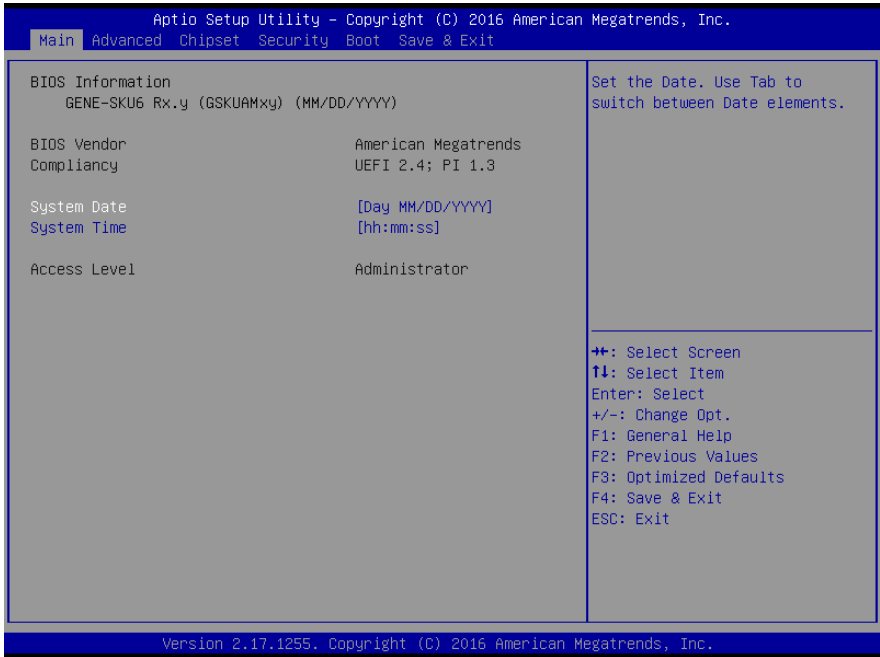
Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

3.3 Setup submenu: Main

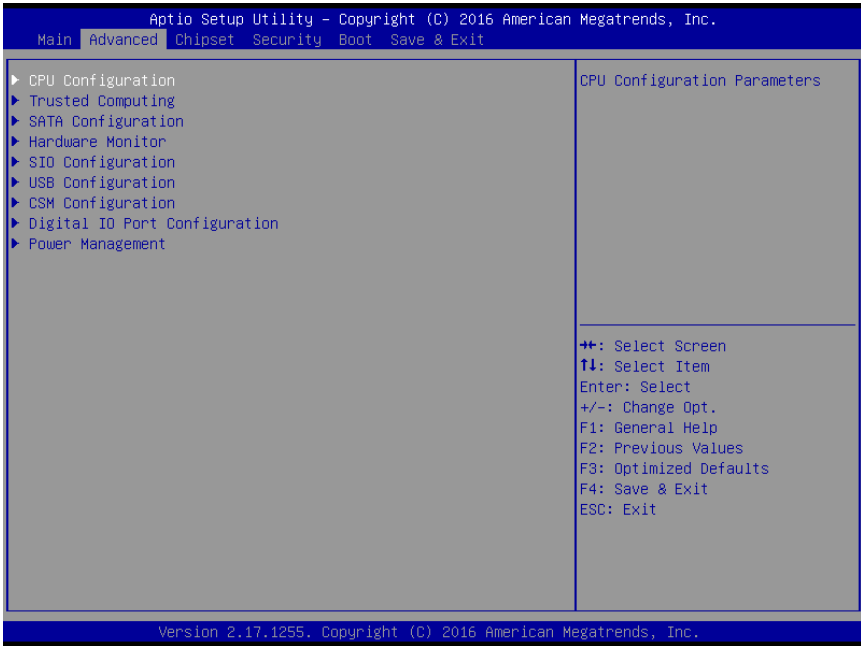
Press '*Delete*' Key to enter Setup



Options summary: (default setting)

System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH : MM : SS	
Change the clock of the system.		

3.4 Setup submenu: Advanced

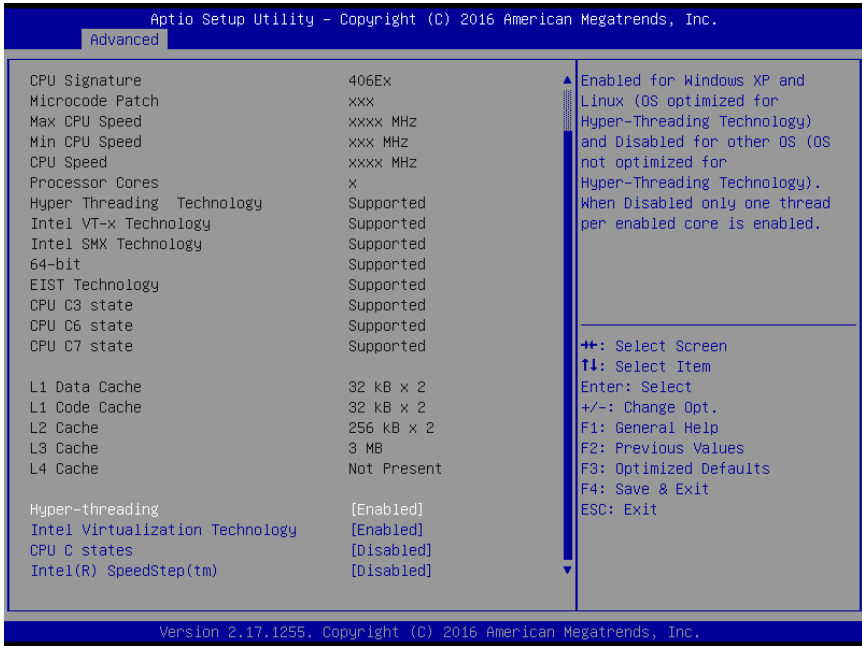


Options summary: **(default setting)**

CPU Configuration		
CPU Configuration Parameters		
Trusted Computing		
Trusted Computing Settings		
SATA Configuration		
SATA Device Options Settings		
Hardware Monitor		
Monitor hardware status		
SIO Configuration		
Super IO Configuration Parameters		

USB Configuration		
USB Configuration Parameters		
CSM Configuration		
CSM Enable/Disable, Option ROM execution setting.		
Digital IO Port Configuration		
DIO configuration		
Power Management		
System ACPI/Power Mode/Wake Event Configuration		

3.4.1 Advanced: CPU Management

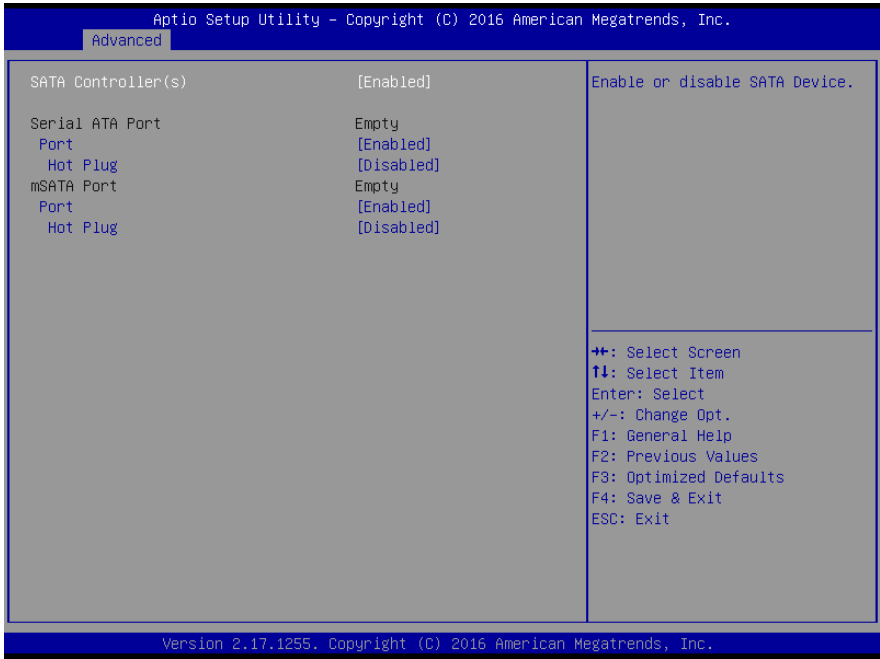


Options summary: (default setting)

Hyper-threading	Enabled	
	Disabled	
Enable/Disable Intel Hyper-threading(HT) feature.		
Intel Virtualization Technology	Enabled	
	Disabled	
When enabled, a VMM can utilize the additional hardware capabilities provide by Vanderpool Technology		
CPU C State Report	Enabled	
	Disabled	
Enable/Disable CPU C state report to OS		

Intel(R) SpeedStep(tm)	Enabled	
	Disabled	
Enable/Disable Intel SpeedStep feature.		
Turbo Mode	Enabled	
	Disabled	
En/Disable Turbo mode. This feature is only available when Intel SpeedStep enabled.		

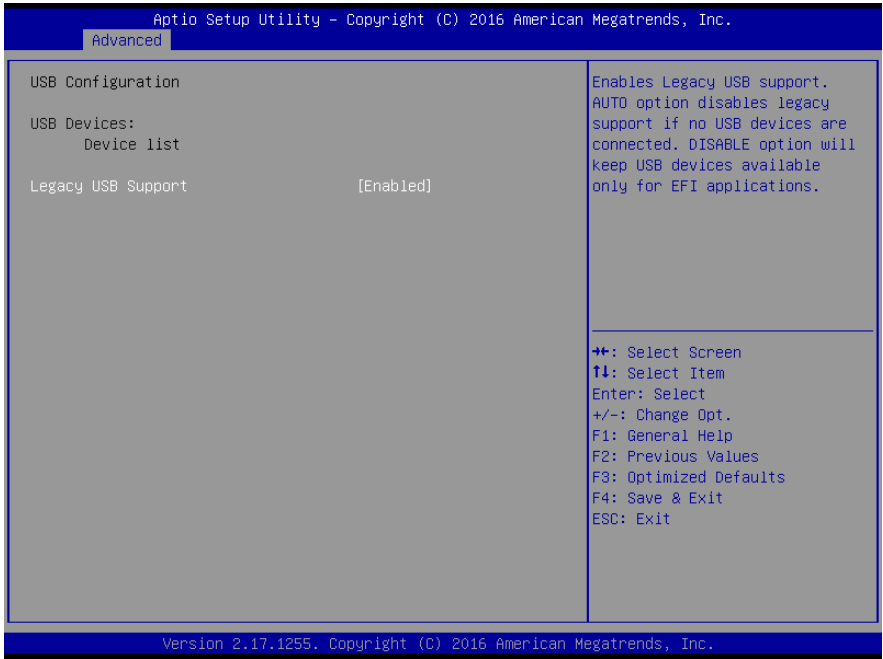
3.4.2 Advanced: SATA Configuration



Options summary: (default setting)

SATA Speed Support	Enabled	
	Disabled	
Enable or disable SATA Device		
Serial ATA Port/mSATA Port	Enabled	
	Disabled	
Enabled/Disabled Serial ATA Port/mSATA Port		
Serial ATA Port/mSATA Port	Enabled	
	Hot Plug	
Designated specified port as Hot Pluggable.		

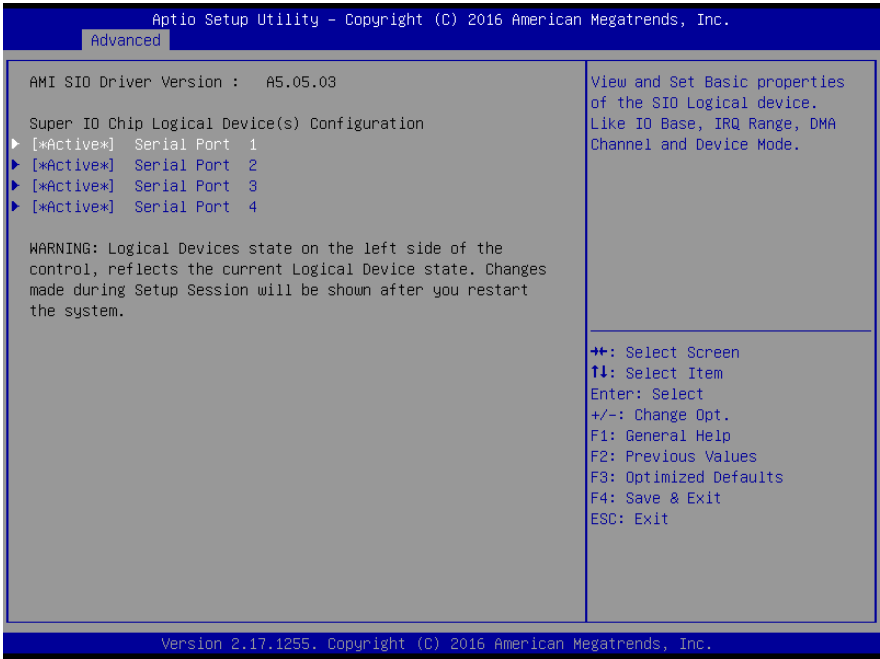
3.4.3 Advanced: USB Configuration



Options summary: (default setting)

Legacy USB Support	Enabled	
	Disabled	
	Auto	
<p>Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application</p>		

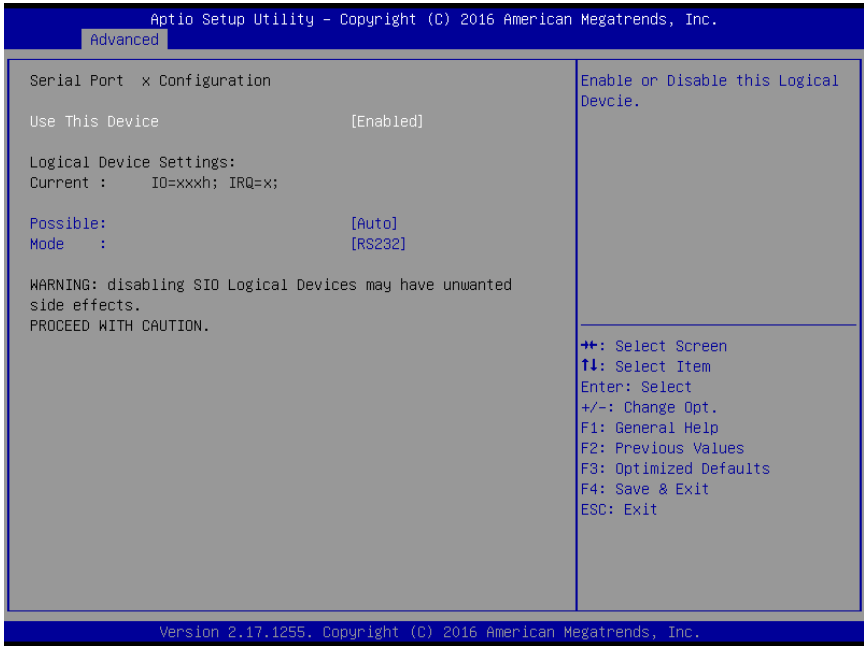
3.4.4 Advanced: SIO Configuration



Options summary: (default setting)

Serial Port 1/2/3/4		
Configuration		
Set Parameters of Serial Port 1/2/3/4		

3.4.4.1 SIO Configuration: Serial Port 1-4 Configuration

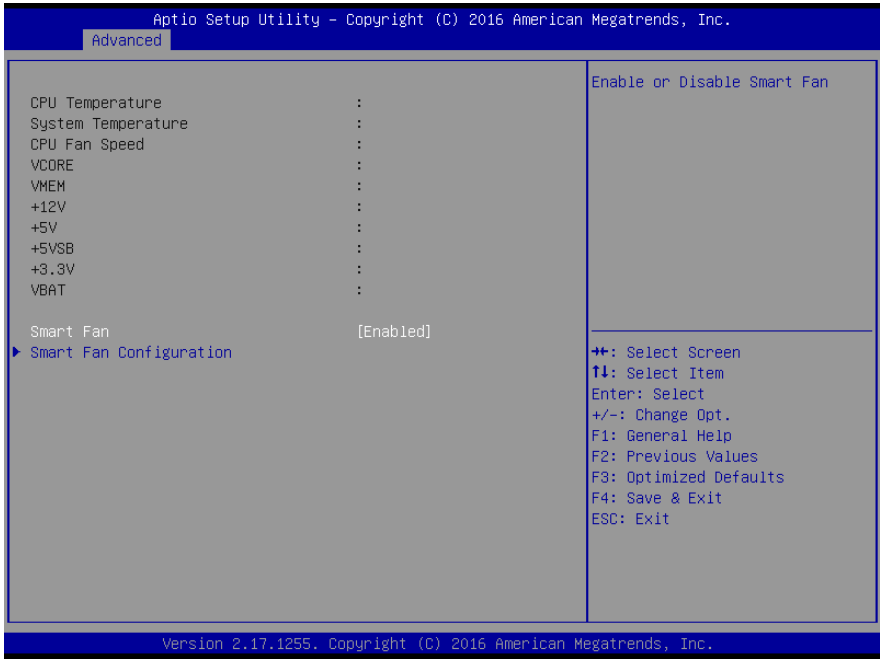


Options summary: (default setting)

Use This Device	Disabled	
	Enabled	
En/Disable specified serial port.		
Change Settings (COM1)	Use Automatic Settings	
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Change Settings (COM2)	Use Automatic Settings	
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Change Settings	Use Automatic Settings	

(COM3)	IO=3E8h; IRQ=11;	
	IO=2E8h; IRQ=11;	
Change Settings	Use Automatic Settings	
(COM4)	IO=2E8h; IRQ=11;	
	IO=3E8h; IRQ=11;	
Select a resource setting for Super IO device.		
Mode	RS232	
	RS422	
	RS485	
Configure COM operated as RS232, RS422 or RS485. Only COM3 and COM4 support this function.		

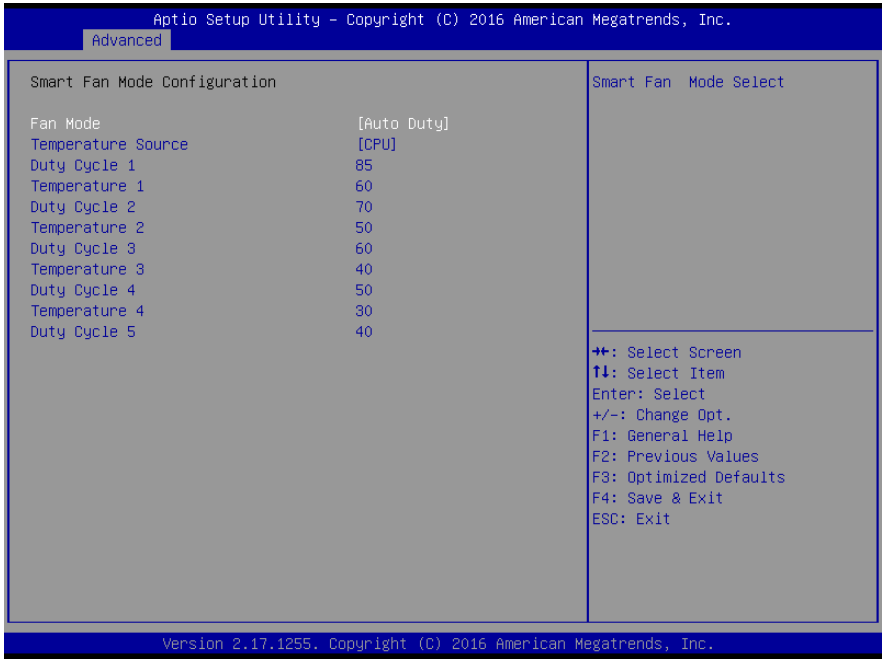
3.4.5 Advanced: Hardware Monitor



Options summary: (default setting)

Smart Fan	Disabled	
	Enabled	
En/Disable specified Smart Fan.		

3.4.5.1 Hardware Monitor: Smart Fan Configuration

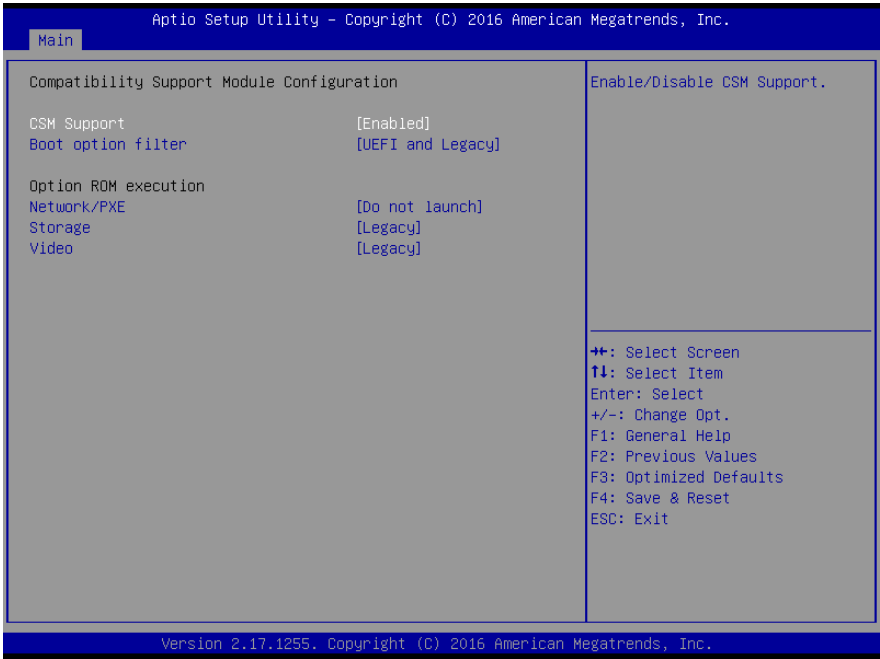


Options summary: (default setting)

Fan Mode	Manual Duty	
	Auto Duty	
Smart Fan Mode Select		
Manual Duty Mode	60	
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1 – 100		
Temperature Source	CPU	
Select the monitored temperature source for this fan. Only supports CPU(external) support for this board.		
Duty Cycle 1	85	
Duty Cycle 2	70	

Duty Cycle 3	60	
Duty Cycle 4	50	
Duty Cycle 5	40	
Fan speed control for each temperature region. User can write expected duty cycle (PWM fan type) 1 – 100		
Temperature 1	60	
Temperature 2	50	
Temperature 3	40	
Temperature 4	30	
Definition of temperature region. User can write expected temperature boundary 1 – 100		

3.4.6 Advanced: CSM Configuration

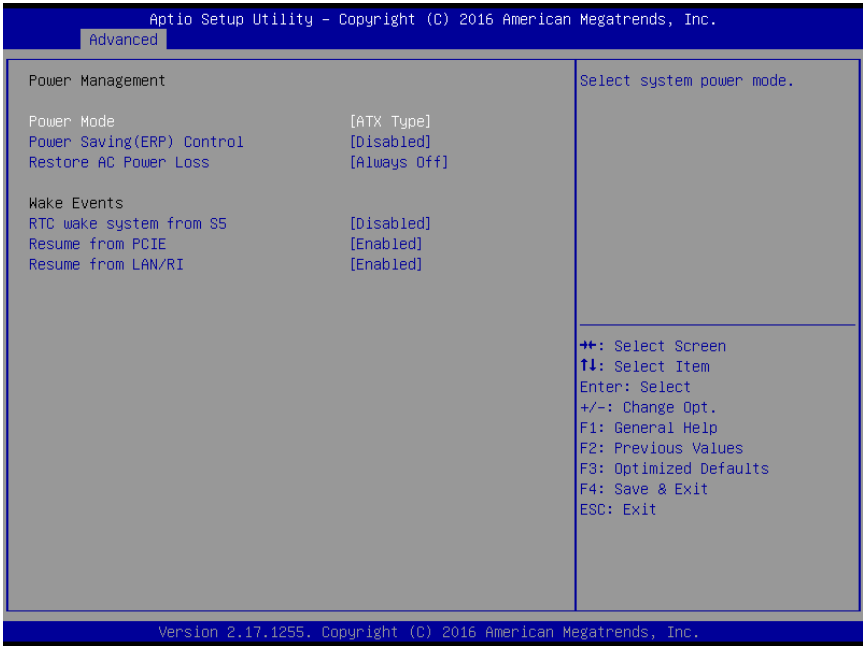


Options summary: (default setting)

CSM Support	Enabled	
	Disabled	
Enable/Disable for CSM Support		
Boot option filter	UEFI and Legacy	
	Legacy only	
	UEFI only	
This option controls Legacy/UEFI boot option priority		
Network/PXE	Do not launch	
	UEFI	
	Legacy	

Controls the execution of UEFI and Legacy PXE OpROM		
Storage	Do not launch	
	UEFI	
	Legacy	
Controls the execution of UEFI and Legacy Storage OpROM		
Video	Do not launch	
	UEFI	
	Legacy	
Controls the execution of UEFI and Legacy Video OpROM		

3.4.7 Advanced: Power Management

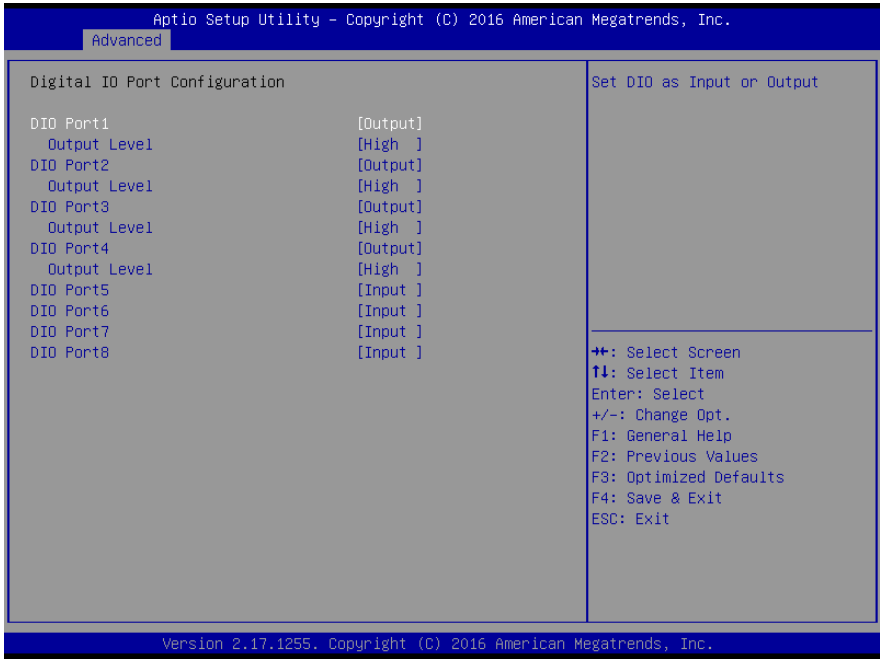


Options summary: (default setting)

Power Mode	ATX Type	
	AT Type	
Select system power mode		
Power Saving (ERP) Control	Enabled	
	Disabled	
Enabled or disabled ERP feature for power saving in S5 state.		
Restore AC Power Loss	Power Off	
	Power on	
	Late State	
Select AC power state when power is re-applied after a power failure		

RTC wake system from S5	Disabled	
	Fixed Time	
	Dynamic Time	
Enable system to wake from S5 using RTC alarm.		
Wake up day	0-31	
Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0-23	
Wake up minute	0-59	
Wake up second	0-59	
Wake up minute increase	1-5	
Resume from PCIE	Enabled	
	Disabled	
Enabled or disabled resume from PCIE WAKE#.		
Resume from LAN/RI	Enabled	
	Disabled	
Enabled or disabled resume from LAN/RI		

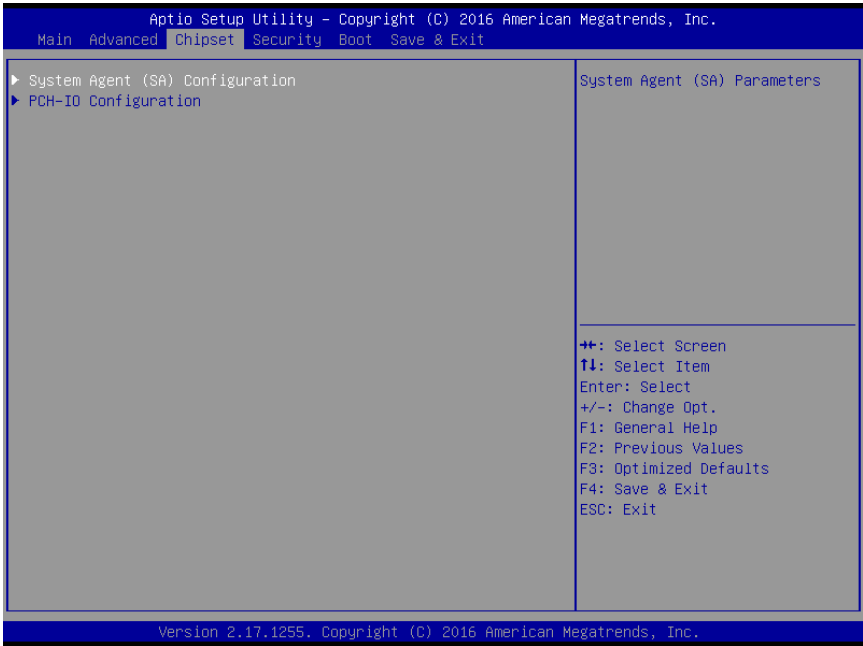
3.4.8 Advanced: Digital IO Port Configuration



Options summary: (default setting)

DIO Port1/2/3/4	Input	
	Output	
Set DIO Port1/2/3/4 as Input or Output		
DIO Port5/6/7/8	Input	
	Output	
Set GPIO3/GPIO4 as Input or Output		
Output Level	Hi	
	Low	
Set GPIO Level when used as Output		

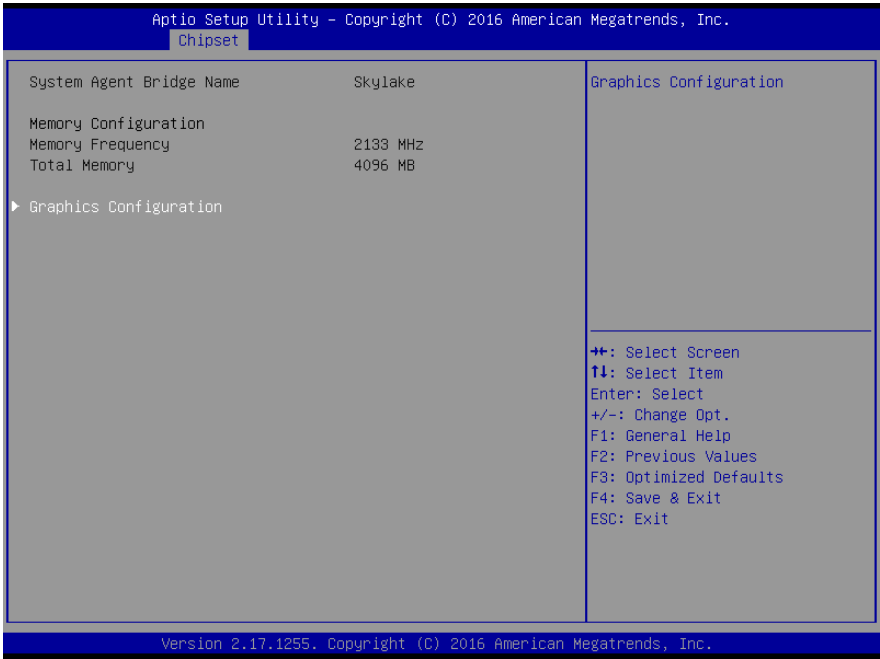
3.5 Setup submenu: Chipset



Options summary: **(default setting)**

System Agent (SA) Configuration		
System Agent (SA) Parameters.		
PCH-IO Configuration		
PCH Parameters		

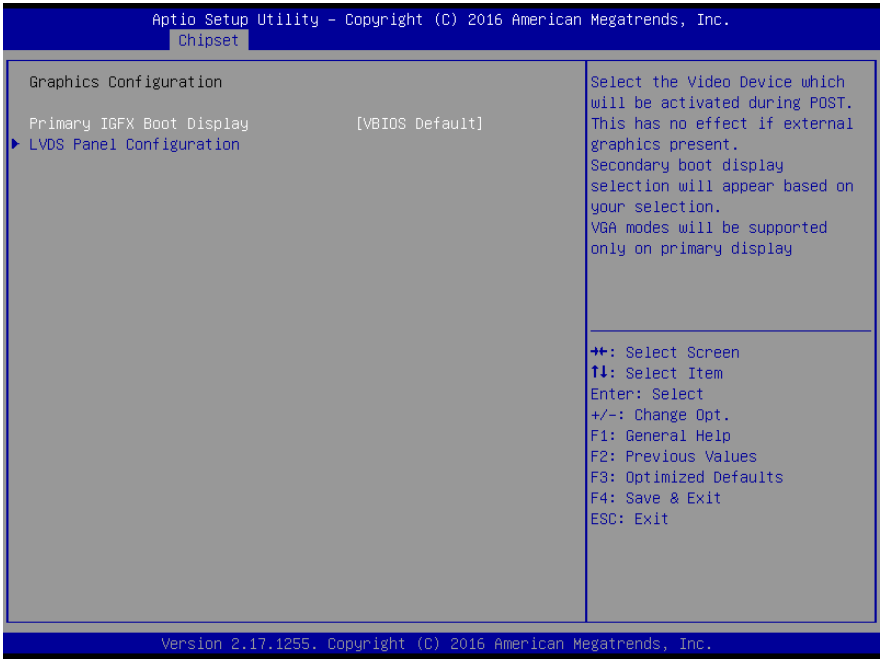
3.5.1 Chipset: System Agent (SA) Configuration



Options summary: (default setting)

Graphics Configuration		
Graphics Configuration		

3.5.1.1 System Agent (SA) Configuration: Graphics Configuration

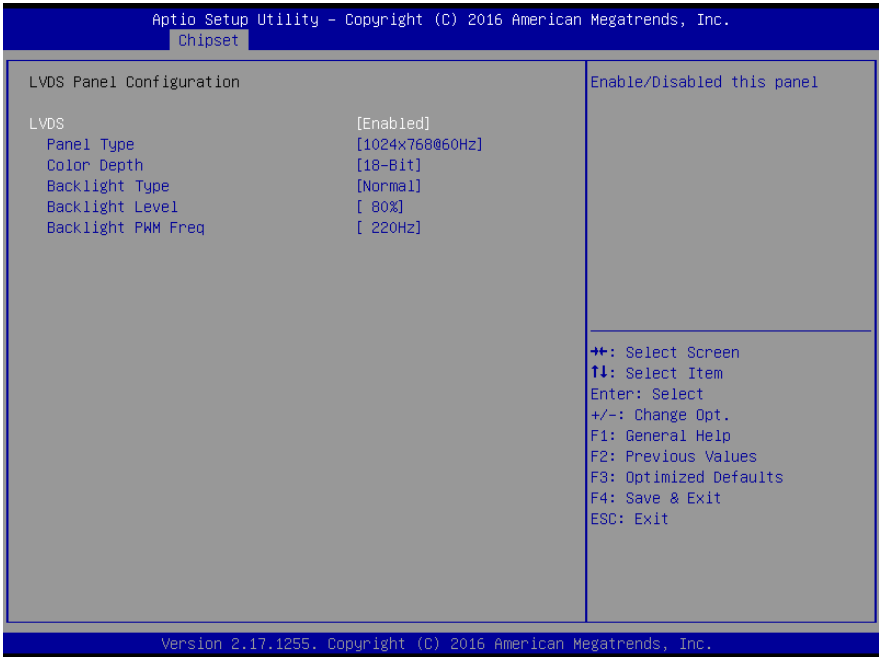


Options summary: (default setting)

Primary IGFX Boot Display	VBIOS Default	
	DVI	
	CRT/DP	
	LVDS	
Select Primary boot display device		
Secondary Boot Display	Disabled	
	DVI	
	CRT/DP	
	LVDS	
Select Primary boot display device		

LVDS Panel Configuration		
Config LVDS panel parameters.		

3.5.1.2 Graphics Configuration: LVDS Panel Configuration



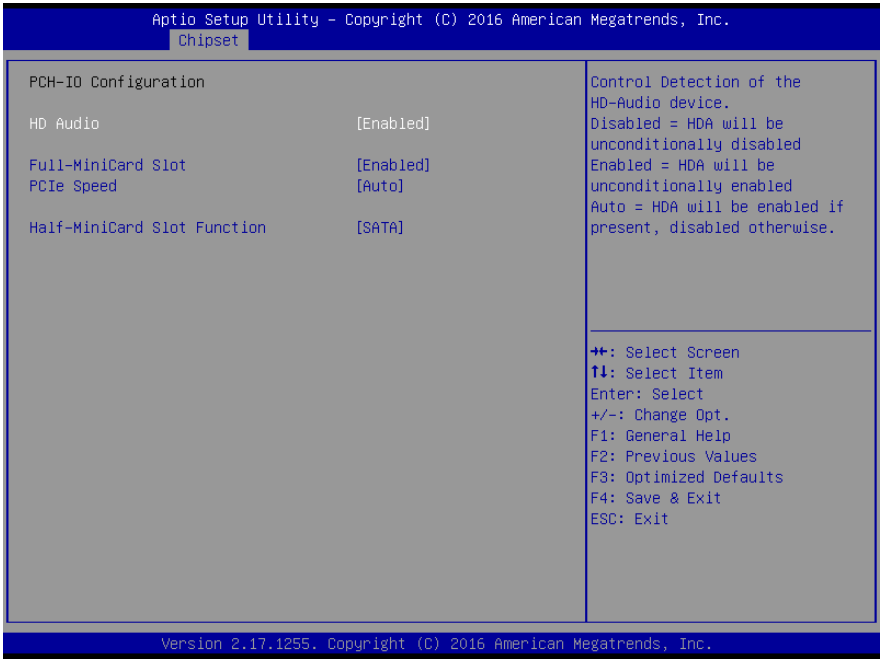
Options summary: (default setting)

LVDS	Disabled	
	Enabled	
Enable or Disable LVDS interface		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	

	1024x768@60Hz	
	1280x768@60Hz	
	1280x800@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	
Select panel resolution.		
Color Depth	18-Bit	
	24-Bit	
	36-Bit	
	48-Bit	
Select color depth of the panel		
Backlight Type	Inverted	
	Normal	
Select Backlight control type.		
Inverted: Brightest for low PWM duty cycle and low voltage.		
Normal: Brightest for high PWM duty cycle and high voltage.		
Backlight Level	100%	
	90%	
	80%	
	70%	
	60%	
	50%	
	40%	

	30%	
	20%	
	10%	
	0%	
Select Backlight Level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal.		

3.5.2 Chipset: PCH-IO Configuration

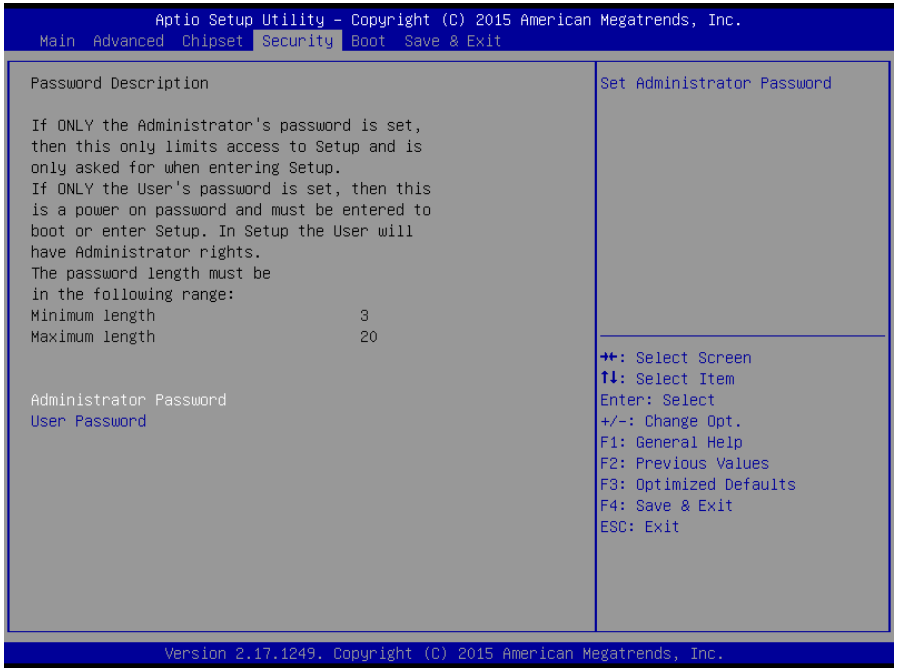


Options summary: (default setting)

HD Audio	Disabled	
	Enabled	
Enable or disabled Azalia device for audio function.		
Full-MiniCard Slot	Disabled	
	Enabled	
Control the full-size minicard slot		
PCIe Speed	Auto	
	Gen1	
	Gen2	
	Gen3	

PCIe Gen Speed for full-size minicard.		
Half-MiniCard Slot	mSATA	
Function	PCIe	
Select function enabled for Half-MiniCard(CN13) Slot		
Half-MiniCard Slot	Disabled	
	Enabled	
Control the full-size minicard slot		
PCIe Speed	Auto	
	Gen1	
	Gen2	
	Gen3	
PCIe Gen Speed for half-size minicard.		

3.6 Setup submenu: Security



Options summary: (default setting)

Administrator Password/	Not set	
User Password		

Change User/Administrator Password

If an Administrator Password is set, it will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

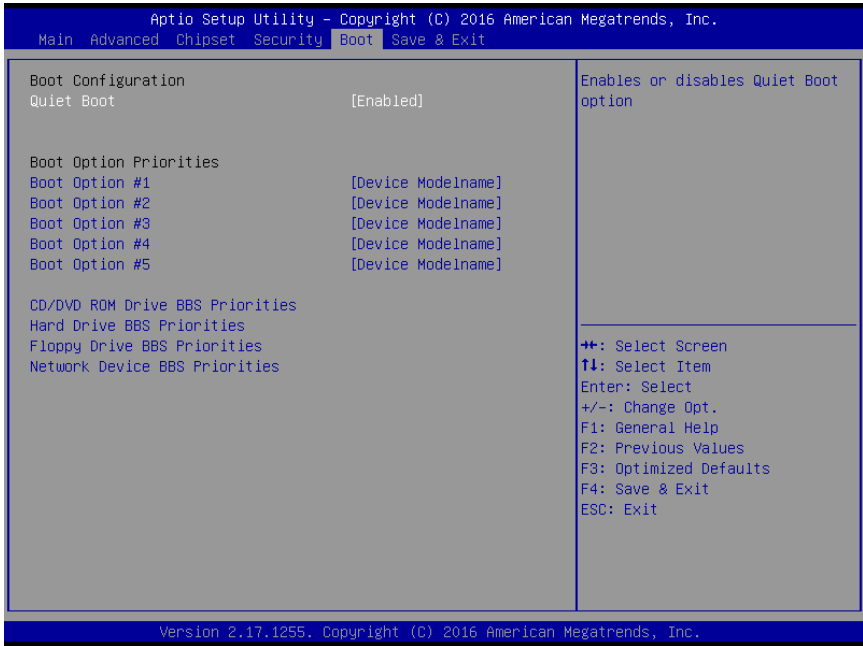
Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press

Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

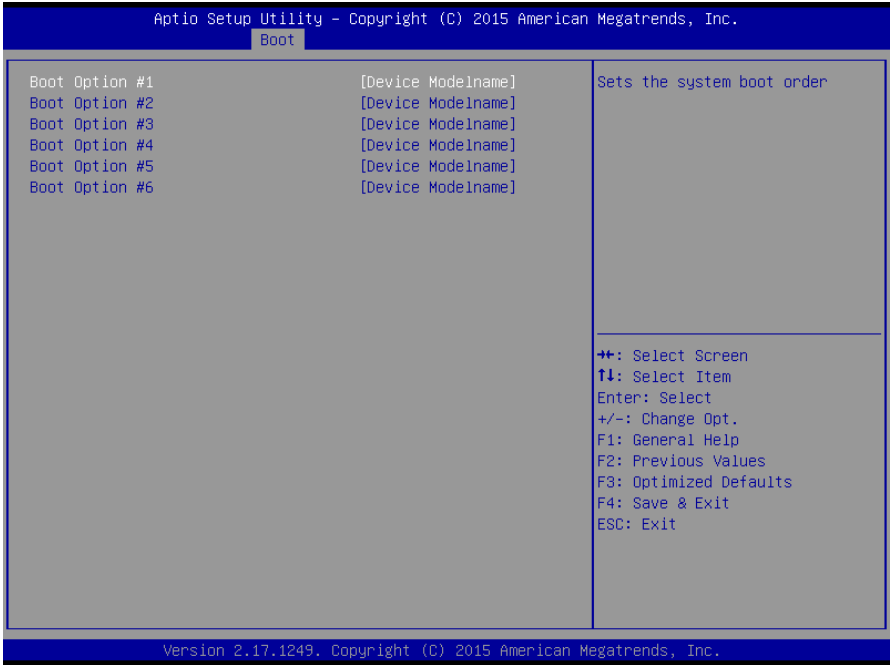
3.7 Setup submenu: Boot



Options summary: (default setting)

Quiet Boot	Disabled	
	Enabled	
En/Disable showing boot logo.		
Boot Option #X/ XXXX Drive BBS Priorities		
The order of boot priorities.		

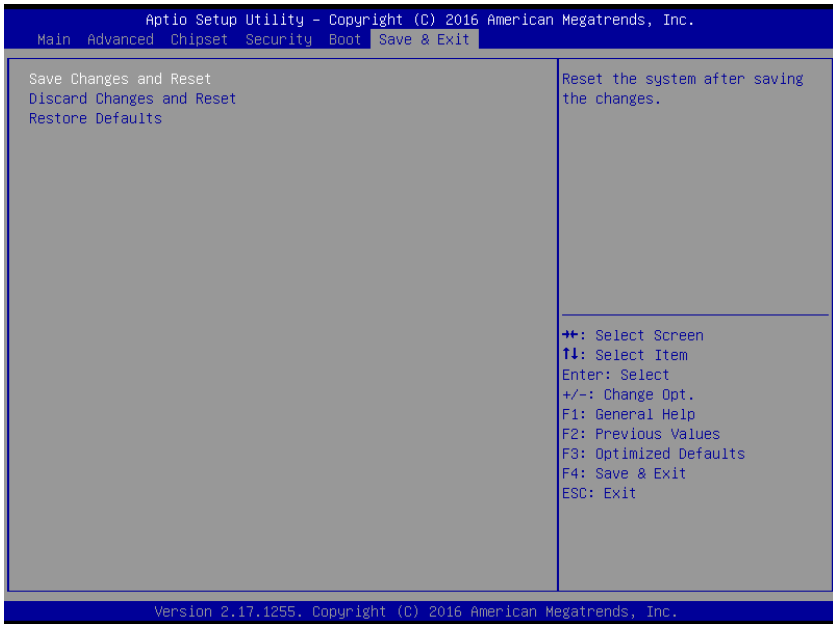
3.7.1 Boot: BBS Priorities



Options summary: **(default setting)**

Boot Option #x	Disabled	
	Device name	
Sets the system boot order		

3.8 Setup submenu: Save & Exit



Options summary: (default setting)

Save Changes and Reset		
Reset the system after saving the changes		
Discard Changes and Exit		
Reset system setup without saving any changes		
Restore Defaults		
Restore/Load Default values for all the setup options.		

Chapter 4

Drivers Installation

4.1 Product CD/DVD

The GENE-SKU6 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step2 - VGA** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Click on the **Step3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Step4 - Audio** folder and select your OS
2. Open the **.exe** file in the folder

3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **Step5 - USB3.0** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install TPM 2.0 Driver (Windows 7 only)

1. Open the **Step6 TPM 2.0** folder followed by the **.msu** file
2. Follow the instructions
3. Drivers will be installed automatically

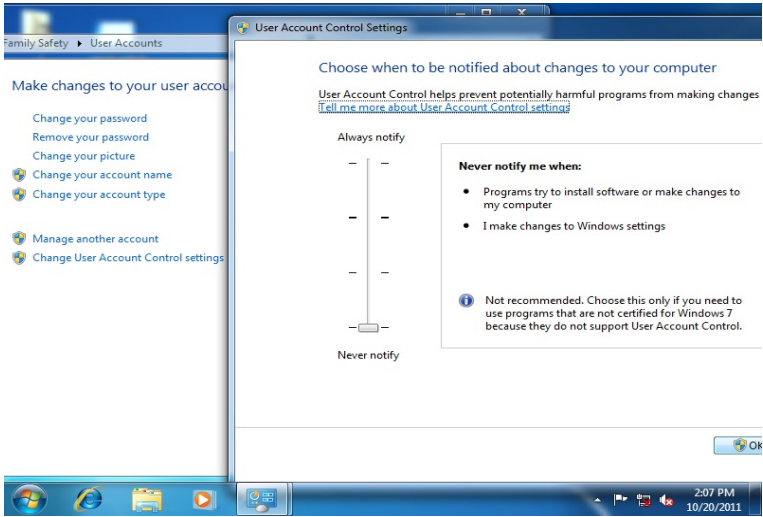
Step 7 – Install Touch Driver

1. Open the **Step7 - PenMount Touch 6000** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

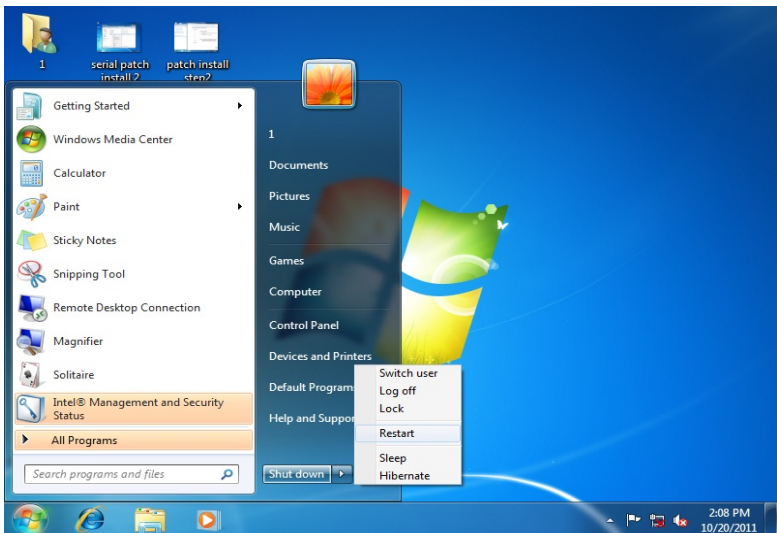
Step 8 – Install Serial Port Drivers

For Windows 7:

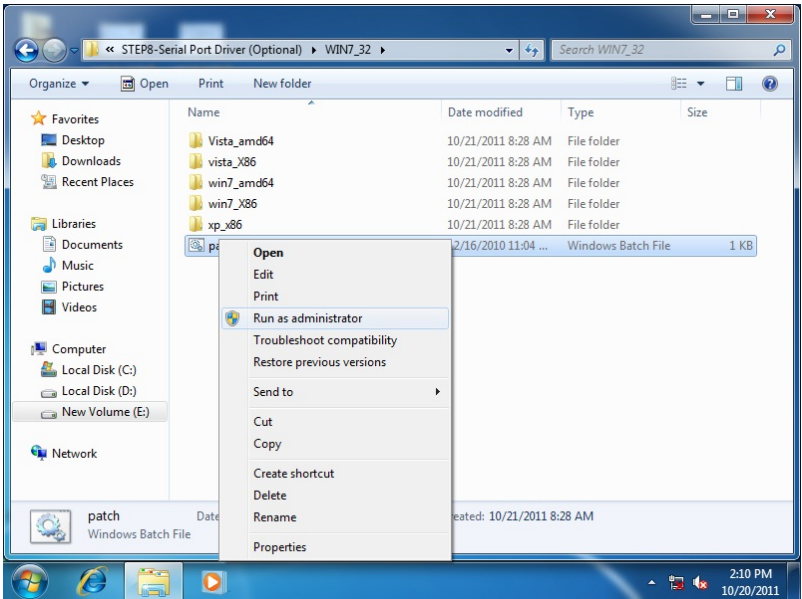
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator



3. Run patch.bat as administrator



For Windows 8/10:

1. Click on the **Step8 - Serial Port Driver (Optional)** folder and select your OS
2. Open the **setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

4.2 Note on EHCI

With the EHCI controller no longer available on the 6th Gen Intel® Core™ platforms, it is recommended to install Windows 7 through a SATA bus, eg SATA DVD-ROM, or patch the xHCI driver onto an installation media for Windows 7. More information can be found in the links below.

[Windows 7 USB 3.0 Creator Utility](#)

[Read me](#)

For input devices, please use an add-on standard EHCI controller expansion card, such as PCIe to USB 2.0 conversion card.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s Pulse width is must longer then 16ms.
Signal Polarity	0x05	2	0	0: low active 1: high active Must set this bit to 0
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse Must set this bit to 1
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****
// WDT I/O operation relative definition (Please reference to Table 1)
#define WDTAddr    0x510 // WDT I/O base address
Void  WDTWriteByte(byte Register, byte Value);
byte  WDTReadByte(byte Register);
Void  WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define DevReg     0x00 // Device configuration register
    #define WDRstBit 0x80 // Watchdog WDTRST# (Bit7)
    #define WDRstVal 0x80 // Enabled WDTRST#
#define TimerReg   0x05 // Timer register
    #define PSWidthBit 0x00 // WDTRST# Pulse width (Bit0:1)
    #define PSWidthVal 0x01 // 25ms for WDTRST# pulse
    #define PolarityBit 0x02 // WDTRST# Signal polarity (Bit2)
    #define PolarityVal 0x00 // Low active for WDTRST#
    #define UnitBit    0x03 // Unit for timer (Bit3)
    #define ModeBit    0x04 // WDTRST# mode (Bit4)
    #define ModeVal    0x01 // 0:level 1: pulse
    #define EnableBit  0x05 // WDT timer enable (Bit5)
    #define EnableVal  0x01 // 1: enable
    #define StatusBit  0x06 // WDT timer status (Bit6)
#define CounterReg 0x06 // Timer counter register
*****

VOID  Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig(Counter, Unit);

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****

// Procedure : AaeonWDTEnable
```



```

VOID AaeonWDTEnable (){
    WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (byte Counter, BOOLEAN Unit){
    // Disable WDT counting
    WDTEnableDisable(0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting(Timer, Unit);
}

VOID WDTEnableDisable(byte Value){
    If (Value == 1)
        WDTSetBit(TimerReg, EnableBit, 1);
    else
        WDTSetBit(TimerReg, EnableBit, 0);
}

VOID WDTParameterSetting(byte Counter, BOOLEAN Unit){
    // Watchdog Timer counter setting
    WDTWriteByte(CounterReg, Counter);
    // WDT counting unit setting
    WDTSetBit(TimerReg, UnitBit, Unit);
    // WDT output mode set to pulse
    WDTSetBit(TimerReg, ModeBit, ModeVal);
    // WDT output mode set to active low
    WDTSetBit(TimerReg, PolarityBit, PolarityVal);
    // WDT output pulse width is 25ms
    WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
    // Watchdog WDTRST# Enable
    WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus() {
    WDTSetBit(TimerReg, StatusBit, 1);
}

*****
*****

```

```
VOID  WDTWriteByte(byte Register, byte Value){
    IOWriteByte(WDTAddr+Register, Value);
}

byte  WDTReadByte(byte Register){
    return IOReadByte(WDTAddr+Register);
}

VOID  WDTSetBit(byte Register, byte Bit, byte Val){
    byte TmpValue;

    TmpValue = WDTReadByte(Register);
    TmpValue &= ~(1 << Bit);
    TmpValue |= Val << Bit;
    WDTWriteByte(Register, TmpValue);
}
```

```
*****
```

Appendix B

I/O Information

B.1 I/O Address Map






























* There are no PS/2 ports on the GENE-SKU6, hence the exclamation marks.

Address Range	Device Name
[0000000000000000 - 00000000000000CF7]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000060 - 0000000000000060]	Standard PS/2 Keyboard
[0000000000000061 - 0000000000000061]	Motherboard resources
[0000000000000063 - 0000000000000063]	Motherboard resources
[0000000000000064 - 0000000000000064]	Standard PS/2 Keyboard
[0000000000000065 - 0000000000000065]	Motherboard resources
[0000000000000067 - 0000000000000067]	Motherboard resources
[0000000000000070 - 0000000000000070]	Motherboard resources
[0000000000000070 - 0000000000000077]	System CMOS/real time clock
[0000000000000080 - 0000000000000080]	Motherboard resources
[0000000000000092 - 0000000000000092]	Motherboard resources
[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[00000000000000B2 - 00000000000000B3]	Motherboard resources
[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
[00000000000002E8 - 00000000000002EF]	Communications Port (COM4)
[00000000000002F8 - 00000000000002FF]	Communications Port (COM2)
[00000000000003B0 - 00000000000003BB]	Intel(R) HD Graphics 520
[00000000000003C0 - 00000000000003DF]	Intel(R) HD Graphics 520
[00000000000003E8 - 00000000000003EF]	Communications Port (COM3)
[00000000000003F8 - 00000000000003FF]	Communications Port (COM1)
[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[0000000000000680 - 000000000000069F]	Motherboard resources
[0000000000000A00 - 0000000000000A0F]	Motherboard resources
[0000000000000A10 - 0000000000000A1F]	Motherboard resources
[0000000000000A20 - 0000000000000A2F]	Motherboard resources
[0000000000000D00 - 0000000000000FFF]	PCI Express Root Complex
[000000000000164E - 000000000000164F]	Motherboard resources
[0000000000001800 - 00000000000018FE]	Motherboard resources
[0000000000001854 - 0000000000001857]	Motherboard resources
[000000000000D000 - 000000000000DFFF]	Intel(R) 100 Series Chipset Family PCI Express Root Port #4 - 9D13
[000000000000E000 - 000000000000EFFF]	Intel(R) 100 Series Chipset Family PCI Express Root Port #3 - 9D12
[000000000000E000 - 000000000000EFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #6 - A115
[000000000000F000 - 000000000000F03F]	Intel(R) HD Graphics 520
[000000000000F040 - 000000000000F05F]	Intel(R) 100 Series Chipset Family SMBUS - 9D23
[000000000000F060 - 000000000000F07F]	Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083]	Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097]	Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources

B.2 Memory Address Map

Memory	
[0000000000A0000 - 0000000000BFFFF]	Intel(R) HD Graphics 520
[0000000000A0000 - 0000000000BFFFF]	PCI Express Root Complex
[0000000090000000 - 00000000DFFFFFF]	PCI Express Root Complex
[00000000C0000000 - 00000000CFFFFFF]	Intel(R) HD Graphics 520
[00000000DE000000 - 00000000DEFFFFFF]	Intel(R) HD Graphics 520
[00000000DF000000 - 00000000DF01FFFF]	Intel(R) I210 Gigabit Network Connection #2
[00000000DF000000 - 00000000DF0FFFFF]	Intel(R) 100 Series Chipset Family PCI Express Root Port #4 - 9D13
[00000000DF020000 - 00000000DF023FFF]	Intel(R) I210 Gigabit Network Connection #2
[00000000DF100000 - 00000000DF11FFFF]	Intel(R) I210 Gigabit Network Connection
[00000000DF100000 - 00000000DF1FFFFF]	Intel(R) 100 Series Chipset Family PCI Express Root Port #3 - 9D12
[00000000DF120000 - 00000000DF123FFF]	Intel(R) I210 Gigabit Network Connection
[00000000DF200000 - 00000000DF20FFFF]	High Definition Audio Controller
[00000000DF210000 - 00000000DF21FFFF]	Intel(R) USB 3.0 Host Controller Adaptation Driver
[00000000DF220000 - 00000000DF223FFF]	High Definition Audio Controller
[00000000DF224000 - 00000000DF227FFF]	Intel(R) 100 Series Chipset Family PMC - 9D21
[00000000DF228000 - 00000000DF229FFF]	Standard SATA AHCI Controller
[00000000DF22A000 - 00000000DF22A0FF]	Intel(R) 100 Series Chipset Family SMBUS - 9D23
[00000000DF22B000 - 00000000DF22B7FF]	Standard SATA AHCI Controller
[00000000DF22C000 - 00000000DF22C0FF]	Standard SATA AHCI Controller
[00000000DF22E000 - 00000000DF22EFFF]	Intel(R) 100 Series Chipset Family Thermal subsystem - 9D31
[00000000DFFE0000 - 00000000DFFFFFFF]	Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000FD000000 - 00000000FDABFFFF]	Motherboard resources
[00000000FD000000 - 00000000FE7FFFFF]	PCI Express Root Complex
[00000000FDAC0000 - 00000000FDACFFFF]	Motherboard resources
[00000000FDAD0000 - 00000000FDADFFFF]	Motherboard resources
[00000000FDAE0000 - 00000000FDAEFFFF]	Motherboard resources
[00000000FDAF0000 - 00000000FDAFFFFF]	Motherboard resources
[00000000FDB00000 - 00000000FDBFFFFF]	Motherboard resources
[00000000FE000000 - 00000000FE01FFFF]	Motherboard resources
[00000000FE028000 - 00000000FE028FFF]	Motherboard resources
[00000000FE029000 - 00000000FE029FFF]	Motherboard resources
[00000000FE036000 - 00000000FE03BFFF]	Motherboard resources
[00000000FE03D000 - 00000000FE03FFFF]	Motherboard resources
[00000000FE40F000 - 00000000FE40FFFF]	Intel(R) Management Engine Interface
[00000000FE410000 - 00000000FE7FFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED10000 - 00000000FED17FFF]	Motherboard resources
[00000000FED18000 - 00000000FED18FFF]	Motherboard resources
[00000000FED19000 - 00000000FED19FFF]	Motherboard resources
[00000000FED20000 - 00000000FED3FFFF]	Motherboard resources
[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 2.0
[00000000FED45000 - 00000000FED8FFFF]	Motherboard resources
[00000000FED90000 - 00000000FED93FFF]	Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFFFF]	Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF]	Intel(R) 82802 Firmware Hub Device
[00000000FF000000 - 00000000FFFFFFFF]	Motherboard resources

B.3 IRQ Mapping Chart

▲		Interrupt request (IRQ)	
		(ISA) 0x00000000 (00)	System timer
		(ISA) 0x00000003 (03)	Communications Port (COM2)
		(ISA) 0x00000004 (04)	Communications Port (COM1)
		(ISA) 0x00000008 (08)	System CMOS/real time clock
		(ISA) 0x0000000B (11)	Communications Port (COM3)
		(ISA) 0x0000000B (11)	Communications Port (COM4)
		(ISA) 0x0000000E (14)	Motherboard resources
		(PCI) 0x0000000B (11)	Intel(R) 100 Series Chipset Family SMBUS - 9D23
		(PCI) 0x00000010 (16)	High Definition Audio Controller
		(PCI) 0x00000010 (16)	Standard SATA AHCI Controller
		(PCI) 0xFFFFFDED (-19)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDEE (-18)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDEF (-17)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDF0 (-16)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDF1 (-15)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDF2 (-14)	Intel(R) I210 Gigabit Network Connection #2
		(PCI) 0xFFFFFDF3 (-13)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF4 (-12)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF5 (-11)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF6 (-10)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF7 (-9)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF8 (-8)	Intel(R) I210 Gigabit Network Connection
		(PCI) 0xFFFFFDF9 (-7)	Intel(R) Management Engine Interface
		(PCI) 0xFFFFFDFA (-6)	Intel(R) USB 3.0 Host Controller Adaptation Driver
		(PCI) 0xFFFFDFB (-5)	Intel(R) HD Graphics 520
		(PCI) 0xFFFFDFC (-4)	Intel(R) 100 Series Chipset Family PCI Express Root Port #4 - 9D13
		(PCI) 0xFFFFDFD (-3)	Intel(R) 100 Series Chipset Family PCI Express Root Port #3 - 9D12
		(PCI) 0xFFFFDFE (-2)	Intel(R) 100 Series Chipset Family PCI Express Root Port #1 - 9D10

Appendix C

Electrical Specifications for I/O Ports

C.1 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
DVI Port	CN3	+5V	+5V/1A (reserved)
DP port	CN5	+3.3V	+3.3V/1A
eDP/LVDS Port	CN6	+3.3V/+5V	+3.3V/2A or +5V/2A
LVDS Port Inverter / Backlight Connector	CN7	+5V/+12V	+5V/1.5A or +12V/1.5A
Mini-Card Slot (Full-Mini Card)	CN11	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
Mini-Card Slot (Half-Mini Card)	CN13	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
+5V Output for SATA HDD	CN15	+5V	+5V/1A
USB 3.0 Ports	CN18	+5VSB	+5V/1A (per channel)
USB 3.0 Ports	CN19	+5VSB	+5V/1A (per channel)
USB 2.0 Ports	CN20	+5VSB	+5V/0.5A (per channel)
USB 2.0 Ports	CN21	+5VSB	+5V/0.5A (per channel)

Audio I/O Port	CN22	+5V	+5V/1A
Digital IO Port	CN24	+5V	+5V/1A
COM Port 4	CN26	+5V/+12V	+5V/1A or +12V/1A
COM Port 2	CN27	+5V/+12V	+5V/1A or +12V/1A
COM Port 3	CN28	+5V/+12V	+5V/1A or +12V/1A
LPC Port	CN29	+3.3V	+3.3V/0.5A
CPU FAN	CN36	+12V	+12V/0.5A

Appendix D

Digital I/O Ports

D.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification

Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO0	I/O	0.8	2.0	0	5	
DIO1	I/O	0.8	2.0	0	5	
DIO2	I/O	0.8	2.0	0	5	
DIO3	I/O	0.8	2.0	0	5	
DIO4	I/O	0.8	2.0	0	5	
DIO5	I/O	0.8	2.0	0	5	
DIO6	I/O	0.8	2.0	0	5	
DIO7	I/O	0.8	2.0	0	5	

Note: All DIO pins are 5V tolerant in input mode.

D.2 DI/O Programming

GENE-SKU6 utilizes FINTEK F81866D chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DI/O program is also attached, based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup:

- (1) Enter the MB PnP Mode
- (2) Modify the data of configuration registers
- (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

D.3 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	Register	Bit	Note
DIO0 Direction	0x06	0xA0	0	0:input, 1: output
DIO1 Direction	0x06	0xA0	1	
DIO2 Direction	0x06	0xA0	2	
DIO3 Direction	0x06	0xA0	3	
DIO4 Direction	0x06	0xA0	4	
DIO5 Direction	0x06	0xA0	5	
DIO6 Direction	0x06	0xA0	6	
DIO7 Direction	0x06	0xA0	7	
DIO0 Output Level	0x06	0xA1	0	0:low, 1: high
DIO1 Output Level	0x06	0xA1	1	
DIO2 Output Level	0x06	0xA1	2	
DIO3 Output Level	0x06	0xA1	3	
DIO4 Output Level	0x06	0xA1	4	
DIO5 Output Level	0x06	0xA1	5	
DIO6 Output Level	0x06	0xA1	6	
DIO7 Output Level	0x06	0xA1	7	
DIO0 Status	0x06	0xA2	0	0:low, 1: high
DIO1 Status	0x06	0xA2	1	
DIO2 Status	0x06	0xA2	2	
DIO3 Status	0x06	0xA2	3	
DIO4 Status	0x06	0xA2	4	
DIO5 Status	0x06	0xA2	5	
DIO6 Status	0x06	0xA2	6	
DIO7 Status	0x06	0xA2	7	

D.4 Digital I/O Sample Program

```

*****
// SuperIO relative definition (Please reference to Table 2)
#define SIOIndex 0x2E
#define SIOData 0x2F
#define DIOLDN 0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define DirReg 0xA0 // 0:input, 1: output
    #define InputPin 0x00
    #define OutputPin 0x01
#define OutputReg 0xA1 // 0:low, 1: high
#define StatusReg 0xA2 // 0:low, 1: high
    #define PinLow 0x00
    #define PinHigh 0x01
#define Pin0Bit 0x00
#define Pin1Bit 0x01
#define Pin2Bit 0x02
#define Pin3Bit 0x03
#define Pin4Bit 0x04
#define Pin5Bit 0x05
#define Pin6Bit 0x06
#define Pin7Bit 0x07
*****

*****

VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    // Example, Read Digital I/O Pin 3 status
    // Output :
    // InputStatus :
    // 0: Digital I/O Pin level is low
    // 1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(Pin3Bit);

    // Procedure : AaeonSetOutputLevel

```

```

// Input :
// Example, Set Digital I/O Pin 2 to high level
AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****

*****

Boolean AaeonReadPinStatus(byte PinBit){
    Boolean PinStatus ;
    PinStatus = SIOBitRead(DIOLDN, StatusReg, PinBit);
    Return PinStatus ;
}

VOID AaeonSetOutputLevel(byte PinBit, byte Value){
    ConfigDioMode(PinBit, OutputPin);
    SIOBitSet(DIOLDN, OutputReg, PinBit, Value);
}
*****

*****VOID
SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
}

```

```

        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
    }

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}

*****

*****

Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}

VOID  ConfigDioMode(byte PinBit, byte Mode){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(DIOLDN);
    IOWriteByte(SIOIndex, DirReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (Mode << PinBit);
    IOWriteByte(SIOData, DirReg);
    SIOExitMBPnPMode();
}

*****

```