GENE-KBU6

3.5" Subcompact Board

User's Manual 5th Ed

Last Updated: August 29, 2018

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● GENE-KBU6 with heat spreader	1
● Product DVD with drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	3.5'' SubCompact Board
CPU	7th Generation Intel® Core™ i7-7600U Processor SoC
CPU Frequency	Up to 3.9 GHz
Chipset	7th generation Intel® Processor SoC
Memory Type	DDR4 1866/2133, SODIMM x 1
Max. Memory Capacity	Up to 16 GB
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+9 ~ 36V or +12V
Power Supply Type	AT / ATX
Power Consumption (Typical)	Intel® i7-7600U, DDR4 2400MHz 16G, 1.85A@ +12V
Dimension (L x W)	5.75" x 4" (146mm x 101.7mm)
Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 81°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	123,000

- **Certification** CE/FCC

Display

- **VGA/LCD Controller** 7th Generation Intel® Processor SoC
- **Video Output** DVI-I, LVDS, DP (DP colay with VGA, default DP)
- **Backlight inverter supply** Yes

I/O

- **Ethernet** Intel® i210/i211, 10/100/1000Base-TX, RJ-45 x 2
- **Audio** High Definition Audio Interface
- **USB Port** USB 3.0 x 4, USB 2.0 x 2
- **Serial Port** RS-232 x 1, RS-232/422/485 x 3
- **Parallel Port** —
- **HDD Interface** SATA 3.0 x 1, +5V SATA power connector x 1
- **FDD Interface** —
- **SSD** mSATA (Shared with half-size MiniCard and Selected by BIOS)
- **Expansion Slot** BIO x 1,
  mSATA x 1 (Half-size), Mini-Card x 1 (Full-size)
- **DIO** 8-bit
- **SIM** x 1
- **TPM** TPM 2.0 x 1

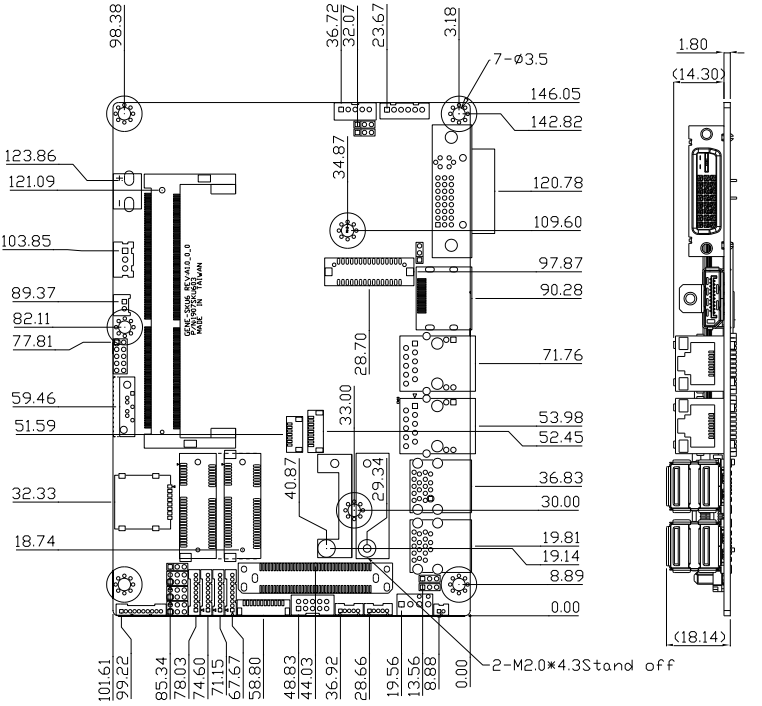
- Touch x 1

Chapter 2

Hardware Information

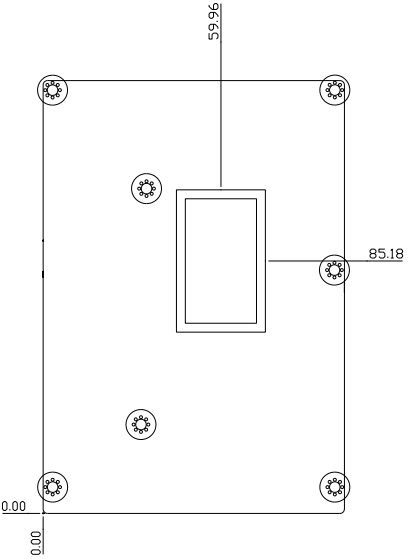
2.1 Dimensions

Component Side



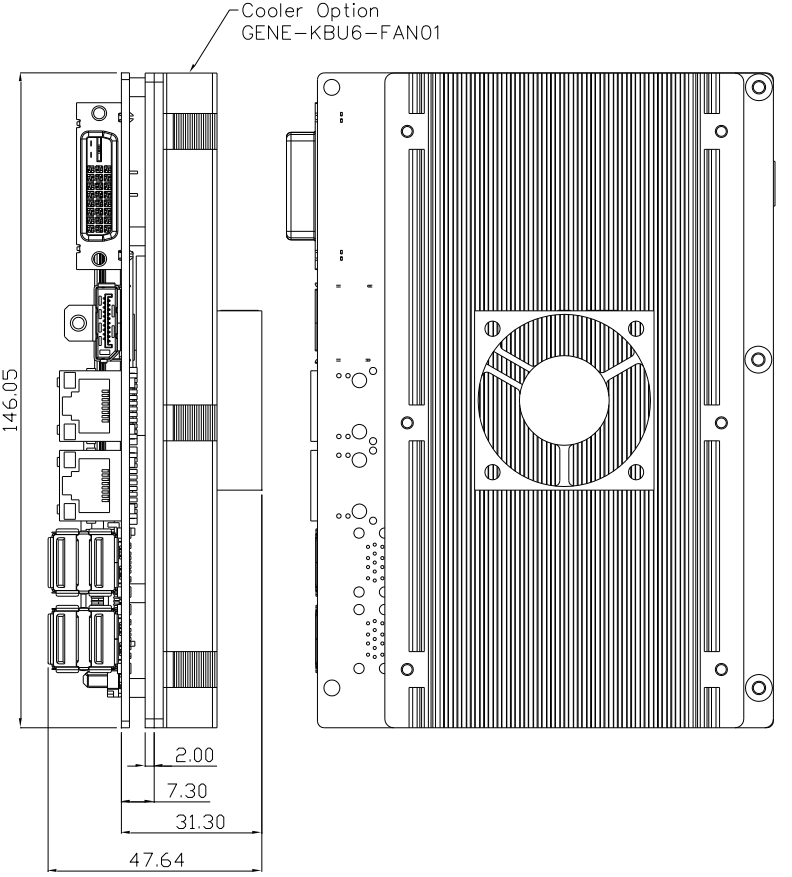
Component Side

Solder Side (with heat spreader)

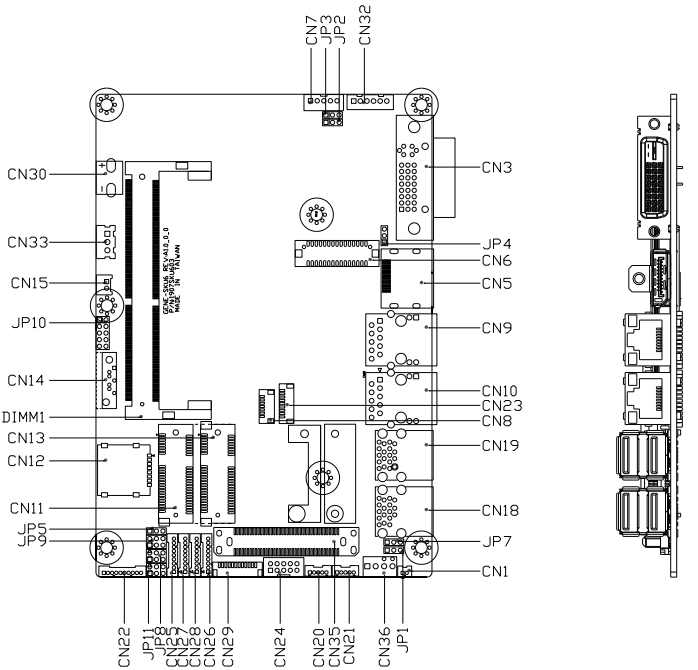


Solder Side

Cooler Option (Part Number: GENE-KBU6-FAN01)



2.2 Jumpers and Connectors

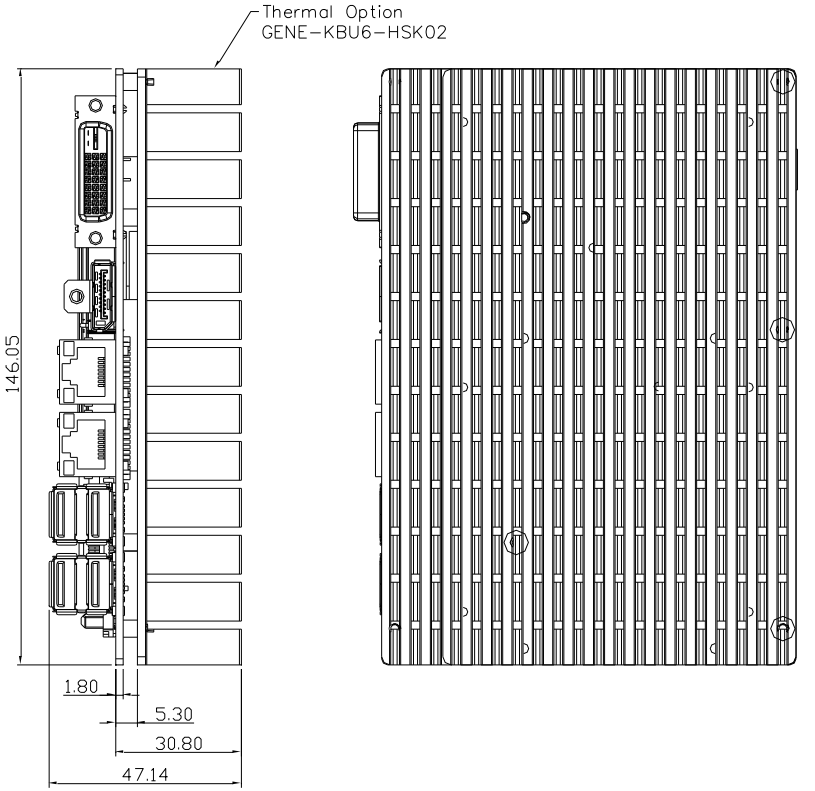


Component Side

2.3 Thermal solutions

GENE-KBU6-HSK02

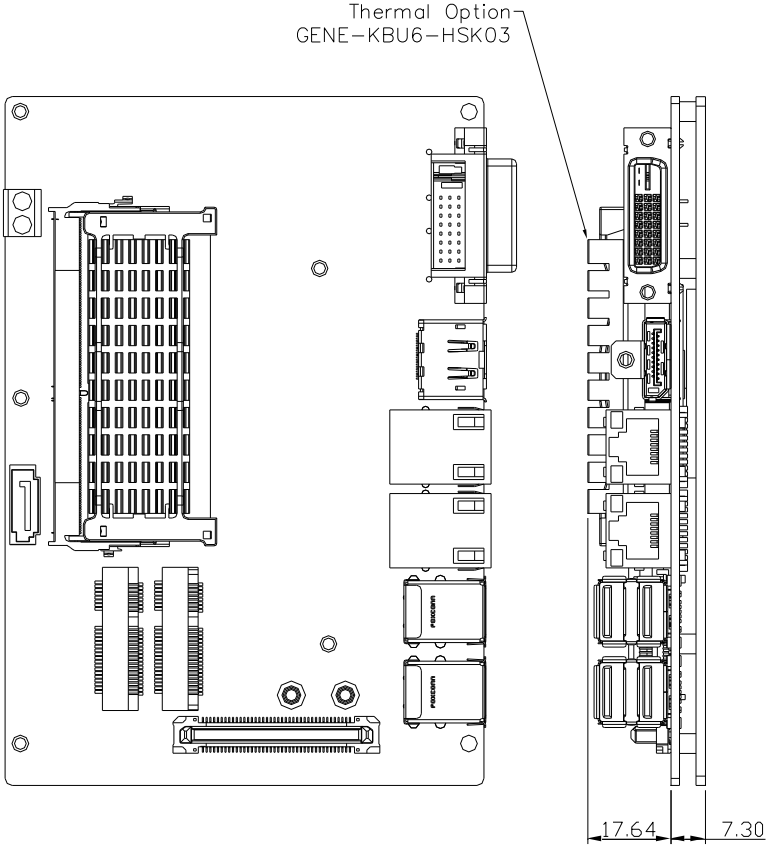
One shape Heatsink, no need to use a heatspreader.



Extended temperature SKUs are tested using GENE-SKU6-HSK02 thermal solution and under UEFI mode.

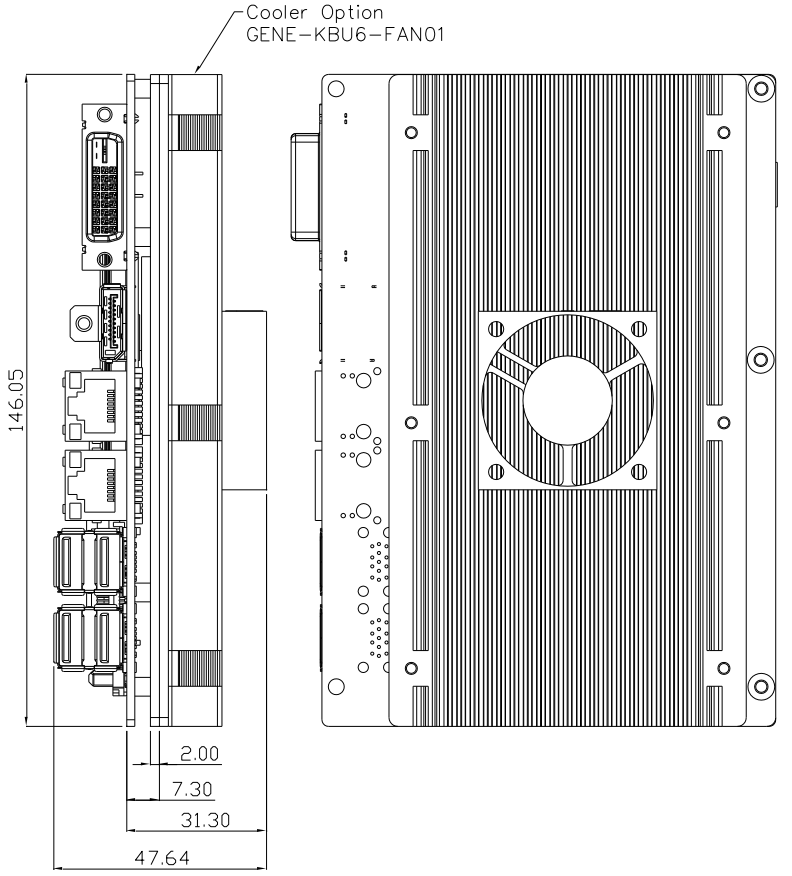
GENE-KBU6-HSK03

Heatsink for DRAM



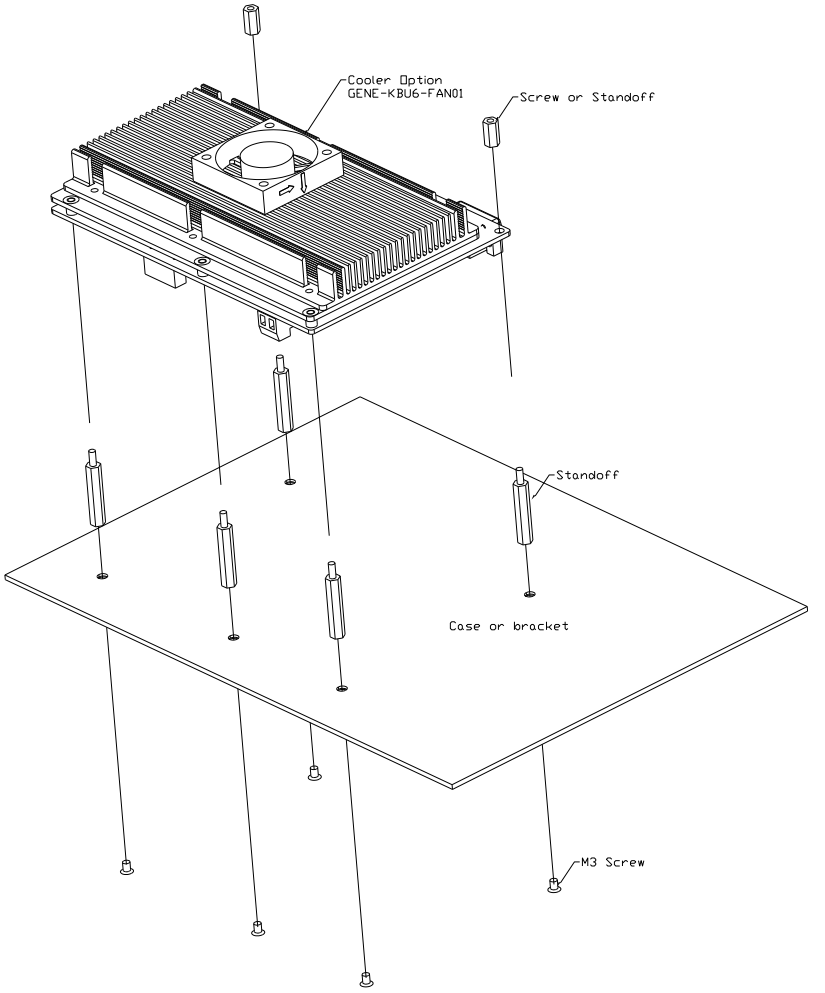
GENE-KBU6-FAN01

Cooler, used with Heatspreader

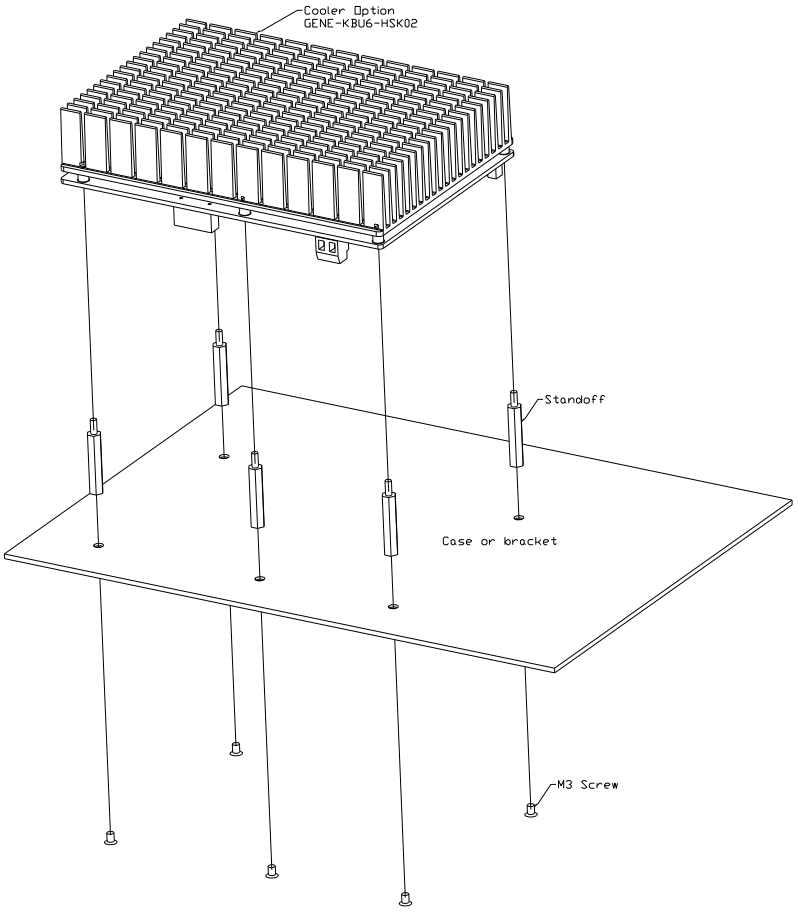


2.4 Assembly Options

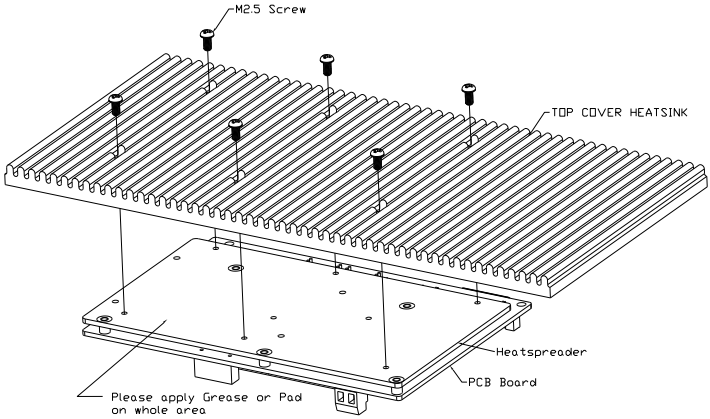
Option 1



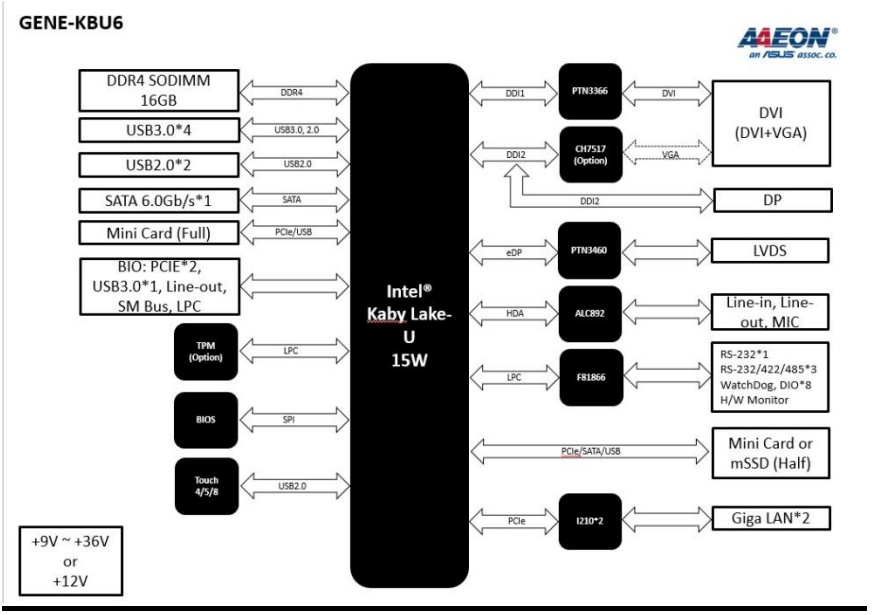
Option 2


Cooler Option
GENE-KBU6-HSK02
Standoff
Case or bracket
M3 Screw

Option 3


M2.5 Screw
TOP COVER HEATSINK
Heatspreader
PCB Board
Please apply Grease or Pad
on whole area

2.5 Block Diagram

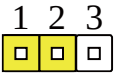


2.6 List of Jumpers

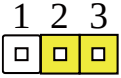
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	Clear CMOS Jumper
JP2	LVDS Port Backlight Inverter VCC Selection
JP3	LVDS Port Backlight Lightness Control Mode Selection
JP4	LVDS Port Operating VDD Selection
JP5	mSATA/Mini-Card Operating VCC Selection
JP6	Touch Screen 4/5/8-wire Mode Selection
JP7	Auto Power Button Enable/Disable Selection
JP8	COM3 Pin8 Function Selection
JP9	COM2 Pin8 Function Selection
JP10	Front Panel Connector
JP11	COM4 Pin8 Function Selection

2.6.1 Clear CMOS Jumper (JP1)

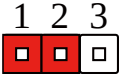


Normal (Default)

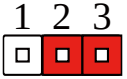


Clear CMOS

2.6.2 LVDS Port Backlight Inverter VCC Selection (JP2)

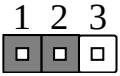


+12V

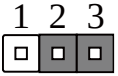


+5V (Default)

2.6.3 LVDS Port Backlight Lightness Control Mode Selection (JP3)

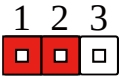


VR Mode (Default)

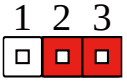


PWM Mode

2.6.4 LVDS Port Operating VDD Selection (JP4)

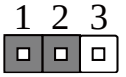


+5V

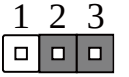


+3.3V (Default)

2.6.5 mSATA/ Mini-Card Operating VCC Selection (JP5)

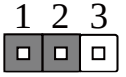


mSATA (Default)

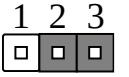


Mini-Card

2.6.6 Touch Screen 4, 5, 8 Wire Selection (JP6)

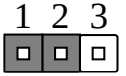


4/8 Wires Mode (Default)

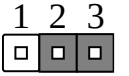


5 Wires Mode

2.6.7 Auto Power Button Enable/Disable Selection (JP7)



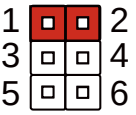
Disable



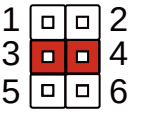
Enable (Default)

* When disabled, use power button JP10 (1-2) to power on the system.

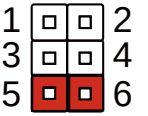
2.6.8 COM3 Pin8 Function Selection (JP8)



+12V

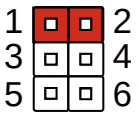


Ring (Default)

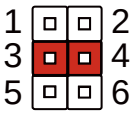


+5V

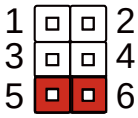
2.6.9 COM2 Pin8 Function Selection (JP9)



+12V

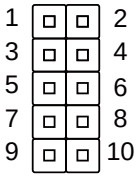


Ring (Default)



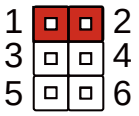
+5V

2.6.10 Front Panel Connector (JP10)

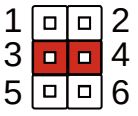


Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

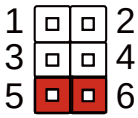
2.6.11 COM4 Pin8 Function Selection (JP11)



+12V



Ring (Default)



+5V

2.7 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application.

Label	Function
CN1	Battery
CN3	DVI-I (Digital and Analog)
CN5	DP Port
CN6	LVDS Port
CN7	LVDS Port Inverter / Backlight Connector
CN8	SPI Debug Port
CN9	LAN (RJ-45) Port1
CN10	LAN (RJ-45) Port2
CN11	Mini-Card Slot (Full-Mini Card)
CN12	Micro SIM Card Socket
CN13	Mini-Card Slot (Half-Mini Card)
CN14	SATA Port
CN15	+5V Output for SATA HDD
CN18	USB 3.0 Ports
CN19	USB 3.0 Ports
CN20	USB 2.0 Port
CN21	USB 2.0 Port
CN22	Audio I/O Port
CN23	Touch Screen Connector
CN24	Digital IO Port
CN25	COM Port 1
CN26	COM Port 4
CN27	COM Port 2

CN28	COM Port 3
CN29	LPC Port
CN30	External Power Input
CN32	+5VSB Output w/SMBus
CN33	External +5VSB Input
CN35	BIO Connector
CN36	CPU FAN

2.7.1 Battery (CN1)

Pin	Pin Name	Signal Type	Signal level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.7.2 DVI-I (Digital and Analog) (CN3)

Pin	Pin Name	Signal Type	Signal Level
1	DVI_D2-	OUT	
2	DVI_D2+	OUT	
3	GND	GND	
4	VGA_DDC_CLK	I/O	
5	VGA_DDC_DAT	I/O	
6	SCL	I/O	
7	SDA	I/O	
8	VGA_VSYNC	OUT	
9	DVI_D1-	OUT	
10	DVI_D1+	OUT	
11	GND	GND	
12	NC		
13	NC		
14	+5V	PWR	+5V
15	GND	GND	
16	HPD	IN	
17	DVI_D0-	OUT	
18	DVI_D0+	OUT	
19	GND	GND	

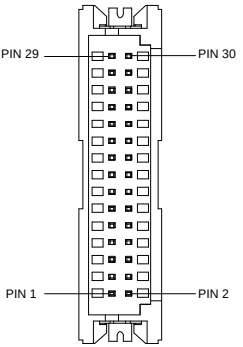
Pin	Pin Name	Signal Type	Signal Level
20	NC		
21	NC		
22	GND	GND	
23	DVI_CLK+	OUT	
24	DVI_CLK-	OUT	
C1	VGA_RED	OUT	
C2	VGA_GREEN	OUT	
C3	VGA_BLUE	OUT	
C4	VGA_HSYNC	OUT	

2.7.3 DP Port (CN5)

Pin	Pin Name	Signal Type	Signal Level
1	DP_D0+	DIFF	
2	GND	GND	
3	DP_D0-	DIFF	
4	DP_D1+	DIFF	
5	GND	GND	
6	DP_D1-	DIFF	
7	DP_D2+	DIFF	
8	GND	GND	
9	DP_D2-	DIFF	
10	DP_D3+	DIFF	
11	GND	GND	
12	DP_D3-	DIFF	
13	GND	GND	
14	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
15	DP_AUX+	DIFF	
16	GND	GND	
17	DP_AUX-	DIFF	
18	HPLG_DETECT	IN	
19	GND	GND	
20	+5V	I/O	+5V

2.7.4 LVDS Port (CN6)

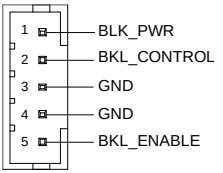


*LVDS LCD_PWR can be set to +3.3V or +5V by JP4

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	

Pin	Pin Name	Signal Type	Signal Level
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.7.5 LVDS Port Inverter / Backlight Connector (CN7)



Pin	Pin Name	Signal Type	Signal level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+5V

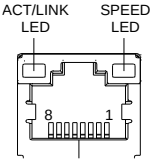
* LVDS BKL_PWR can be set to +5V or +12V by JP2

* LVDS BKL_CONTROL can be set by JP3

2.7.6 BIOS Debug Port (CN8)

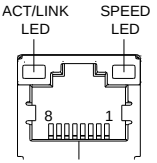
Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

2.7.7 LAN (RJ-45) Port1 (CN9)



Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.7.8 LAN (RJ-45) Port2 (CN10)



Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	

Pin	Pin Name	Signal Type	Signal level
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.7.9 Mini-Card Slot (Full-Mini Card) (CN11)

Pin	Pin Name	Signal Type	Signal level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V

Pin	Pin Name	Signal Type	Signal level
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		

Pin	Pin Name	Signal Type	Signal level
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.7.10 Micro SIM Card Socket (CN12)

Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	NC		
5	GND	GND	
6	UIM_VPP	PWR	
7	UIM_DATA	I/O	
8	NC		

2.7.11 Mini-Card Slot (Half-Mini Card) (CN13)

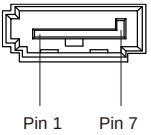
Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC		
9	GND	GND	
10	NC		
11	PCIE_REF_CLK-	DIFF	
12	NC		
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC		
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-/mSATA_RX+	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+/mSATA_RX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V

Pin	Pin Name	Signal Type	Signal Level
31	PCIE_TX-/mSATA_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+/mSATA_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

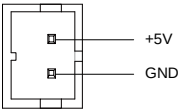
* CN13 can be selected for Mini-Card or mSATA by changing BIOS

2.7.12 SATA Port 1 (CN14)



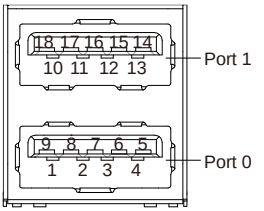
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.7.13 +5V Output for SATA HDD (CN15)



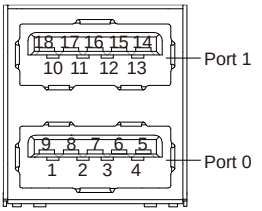
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

2.7.14 USB 3.0 Ports (CN18)



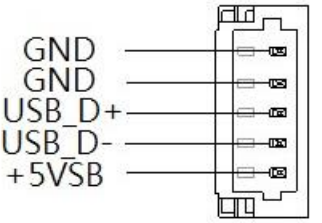
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	USB_SSRX–	DIFF	
6	USB_SSRX+	DIFF	
7	GND	GND	
8	USB_SSTX–	DIFF	
9	USB_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB_D-	DIFF	
12	USB_D+	DIFF	
13	GND	GND	
14	USB_SSRX–	DIFF	
15	USB_SSRX+	DIFF	
16	GND	GND	
17	USB_SSTX–	DIFF	
18	USB_SSTX+	DIFF	

2.7.15 USB 3.0 Ports (CN19)



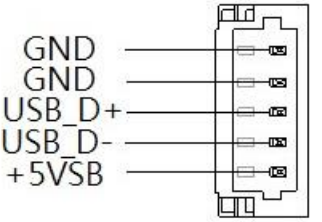
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	USB_SSRX–	DIFF	
6	USB_SSRX+	DIFF	
7	GND	GND	
8	USB_SSTX–	DIFF	
9	USB_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB_D-	DIFF	
12	USB_D+	DIFF	
13	GND	GND	
14	USB_SSRX–	DIFF	
15	USB_SSRX+	DIFF	
16	GND	GND	
17	USB_SSTX–	DIFF	
18	USB_SSTX+	DIFF	

2.7.16 USB 2.0 Port (CN20)



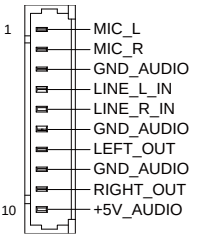
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.7.17 USB 2.0 Port (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	G ND	GND	

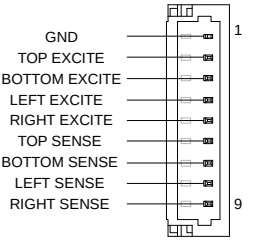
2.7.18 Audio I/O Port (CN22)



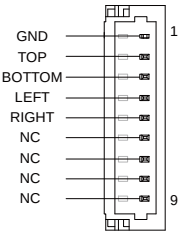
Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

2.7.19 Touchscreen Connector (CN23)

* Touch mode can be set by JP6

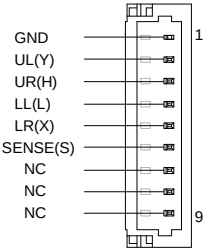


8-Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	
8	LEFT SENSE	IN	
9	RIGHT SENSE	IN	



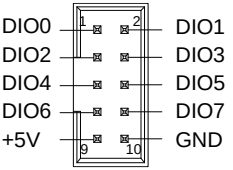
4-Wire

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		



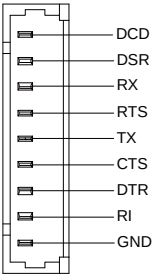
5-Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

2.7.20 Digital I/O Port (CN24)



Pin	Pin Name	Signal Type	Signal Level
1	DIO0	I/O	+5V
2	DIO1	I/O	+5V
3	DIO2	I/O	+5V
4	DIO3	I/O	+5V
5	DIO4	I/O	+5V
6	DIO5	I/O	+5V
7	DIO6	I/O	+5V
8	DIO7	I/O	+5V
9	+5V	PWR	+5V
10	GND	GND	

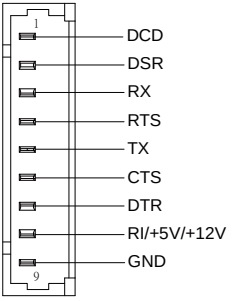
2.7.21 COM Port 1 (CN25)



Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	

Pin	Pin Name	Signal Type	Signal Level
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

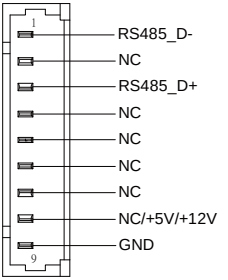
2.7.22 COM Port 4 (CN26)



RS-232

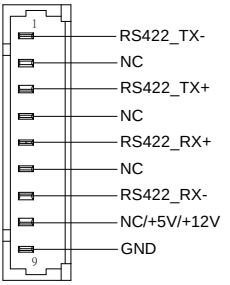
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V

Pin	Pin Name	Signal Type	Signal Level
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



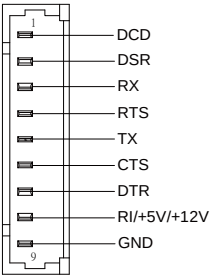
RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM4 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

* Pin 8 function can be set by JP11.

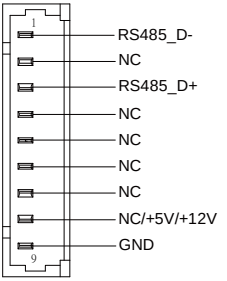
2.7.23 COM Port 2 (CN27)



RS-232

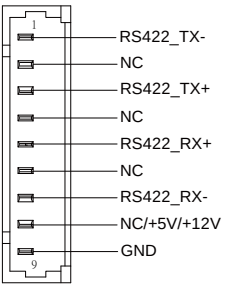
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	

Pin	Pin Name	Signal Type	Signal Level
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-485

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



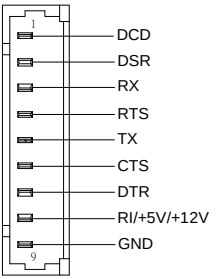
RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

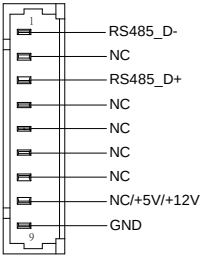
* Pin 8 function can be set by JP9.

2.7.24 COM Port 3 (CN28)



RS-232

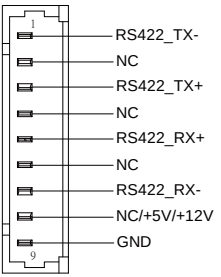
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±5V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	



RS-485

Pin	Pin Name	Signal Type	Signal Level

Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	



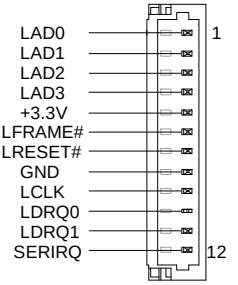
RS-422

Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

* COM3 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

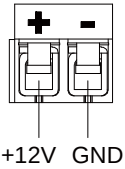
* Pin 8 function can be set by JP8.

2.7.25 LPC Port (CN29)



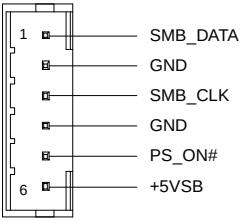
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.7.26 External Power Input (CN30)



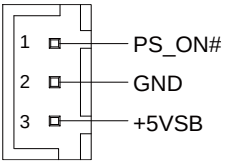
Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+9~+36V (or +12V)
2	GND	GND	

2.7.27 +5VSB Output w/SMBus (CN32)



Pin	Pin Name	Signal Type	Signal Level
1	SMB_DATA	I/O	+3.3V
2	GND	GND	
3	SMB_CLK	I/O	+3.3V
4	GND	GND	
5	PS_ON#	OUT	+3.3V
6	+5VSB	PWR	+5V

2.7.28 External +5VSB Input (CN33)



Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+3.3V
2	GND	GND	
3	+5VSB	PWR	+5V

2.7.29 BIO Connector (CN35)

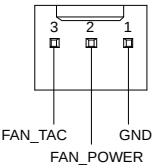
Pin	Pin Name	Signal Type	Signal Level
1	+12V_Dual	PWR	+12V
2	GND	GND	
3	GND	GND	
4	PCIE1_TX-	I/O	
5	PCIE1_RX-	I/O	
6	PCIE1_TX+	I/O	
7	PCIE1_RX+	I/O	
8	GND	GND	
9	GND	GND	
10	PCIE2_TX-	I/O	
11	PCIE2_RX-	I/O	
12	PCIE2_TX+	I/O	
13	PCIE2_RX+	I/O	
14	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
15	GND	GND	
16	PS_ON#	OUT	
17	NC		
18	NC		
19	+5V_Dual	PWR	+5V
20	+5V_Dual	PWR	+5V
21	+5V_Dual	PWR	+5V
22	+5V_Dual	PWR	+5V
23	PCIE_CLK+	OUT	
24	PLT_RST#	OUT	
25	PCIE_CLK-	OUT	
26	GND	GND	
27	GND	GND	
28	NC		
29	NC		
30	NC		
31	NC		
32	GND	GND	
33	GND	GND	
34	NC		
35	NC		
36	NC		
37	NC		
38	GND	GND	
39	GND	GND	
40	NC		

Pin	Pin Name	Signal Type	Signal Level
41	NC		
42	GND	GND	
43	NC		
44	USB 3.0_TX-	I/O	
45	GND	GND	
46	USB 3.0_TX+	I/O	
47	USB 2.0_D-	I/O	
48	GND	GND	
49	USB 2.0_D+	I/O	
50	USB 3.0_RX-	I/O	
51	GND	GND	
52	USB 3.0_RX+	I/O	
53	SMB_CLK	I/O	
54	GND	GND	
55	SMB_DATA	I/O	
56	PCIE_WAKE#	IN	
57	GND	GND	
58	USB 2.0_OC#	IN	
59	+5V	PWR	+5V
60	USB 2.0_OC#	IN	
61	+5V	PWR	+5V
62	+5V	PWR	+5V
63	+5V	PWR	+5V
64	+5V	PWR	+5V
65	LPC_AD0	I/O	
66	LPC_FRAME#	I/O	

Pin	Pin Name	Signal Type	Signal Level
67	LPC_AD1	I/O	
68	SERIRQ#	I/O	
69	LPC_AD2	I/O	
70	NC		
71	LPC_AD3	I/O	
72	GPIO	I/O	
73	GND	GND	
74	Audio_GND	GND	
75	LPC_CLK	OUT	
76	Audio_OUT_L	OUT	
77	PME#	IN	
78	Audio_OUT_R	OUT	
79	GND	GND	
80	GND	GND	

2.7.30 CPU Fan (CN36)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

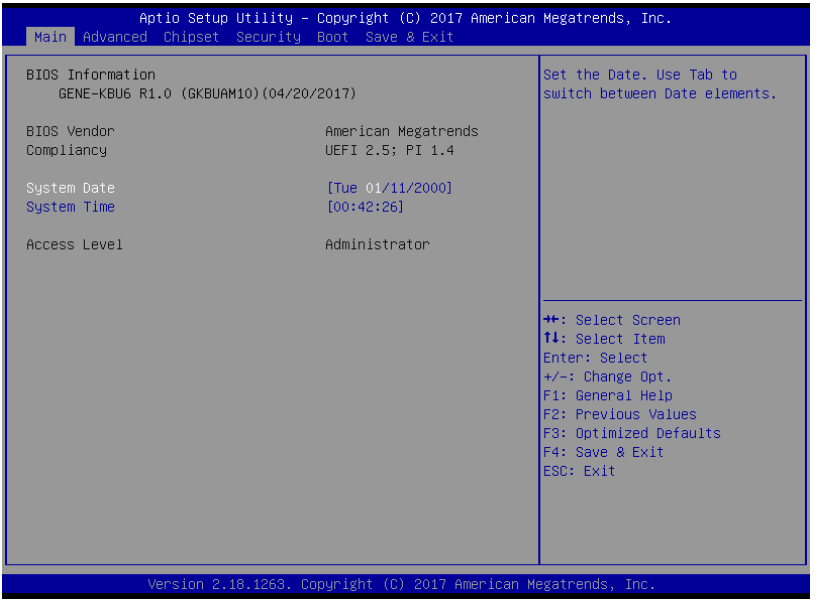
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

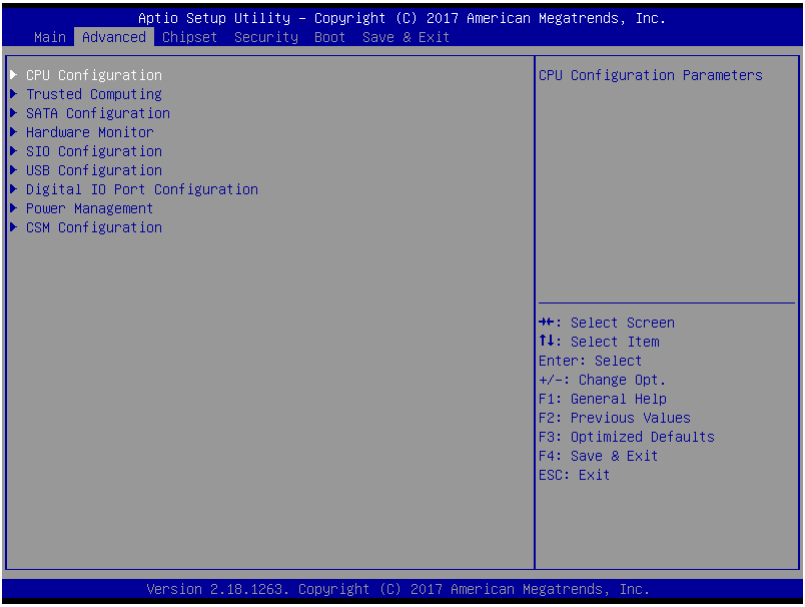
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

3.3 Setup submenu: Main



3.4 Setup submenu: Advanced



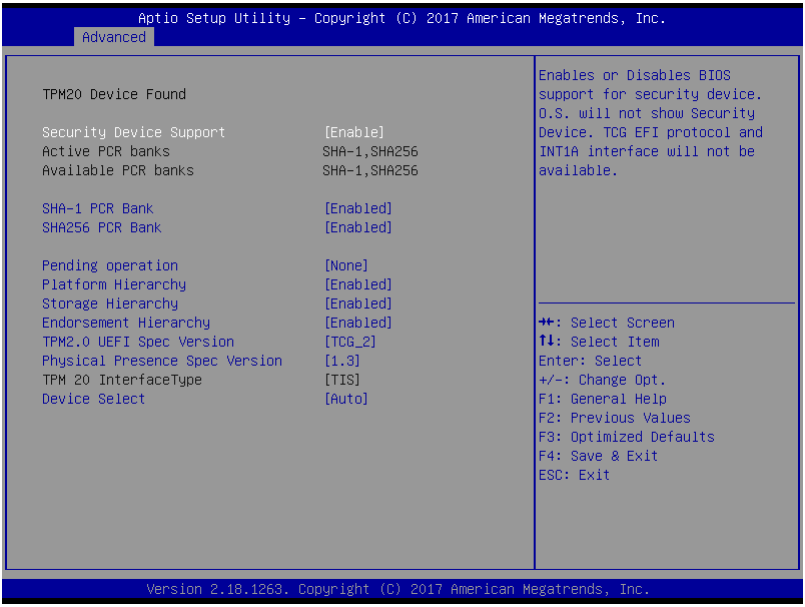
3.4.1 CPU Configuration

Options summary:

Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
CPU C states	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.		

Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled, unless max turbo ratio is bigger than 16 - SKL A0 W/A		

3.4.2 Trusted Computing

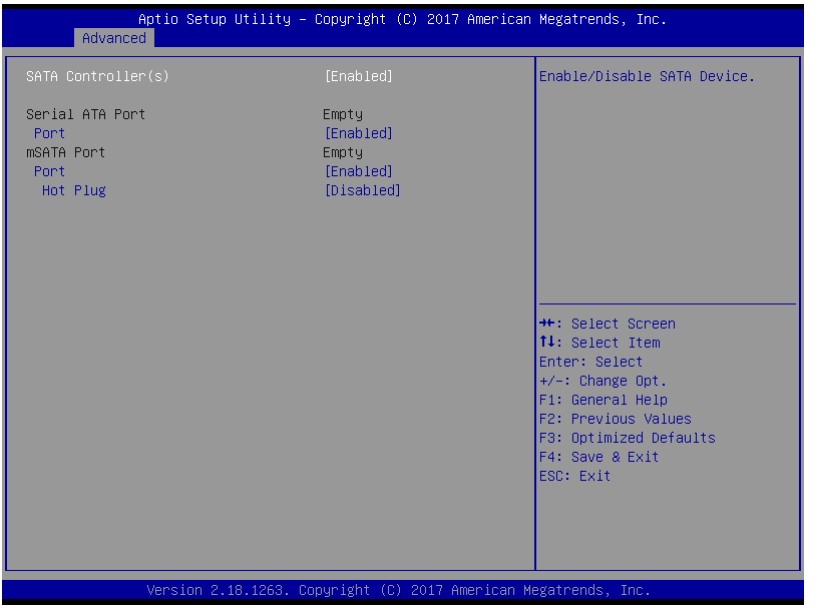


Options summary:

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		

Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

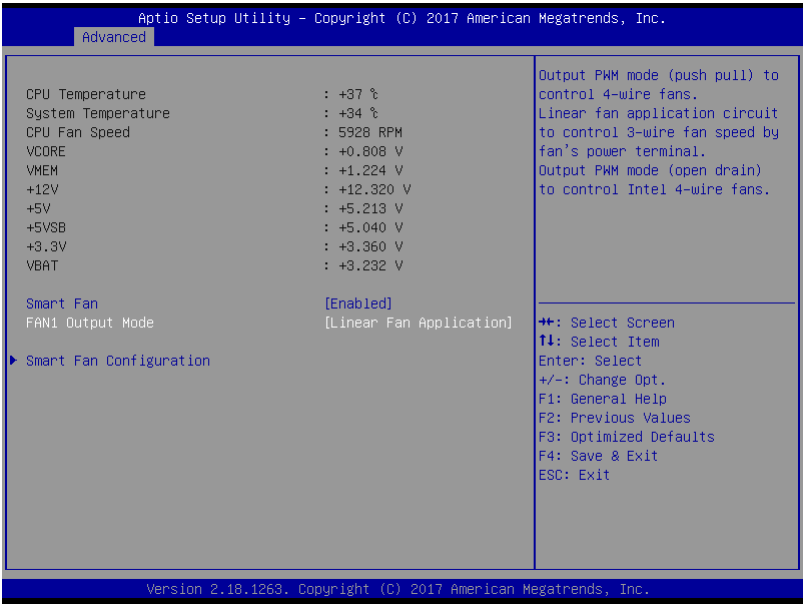
3.4.3 SATA Configuration



Options summary:

SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable SATA Device.		
SATA Mode	AHCI Mode	Optimal Default, Failsafe Default
	RAID Mode	
Determines how SATA controller(s) operate.		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.4 Hardware Monitor

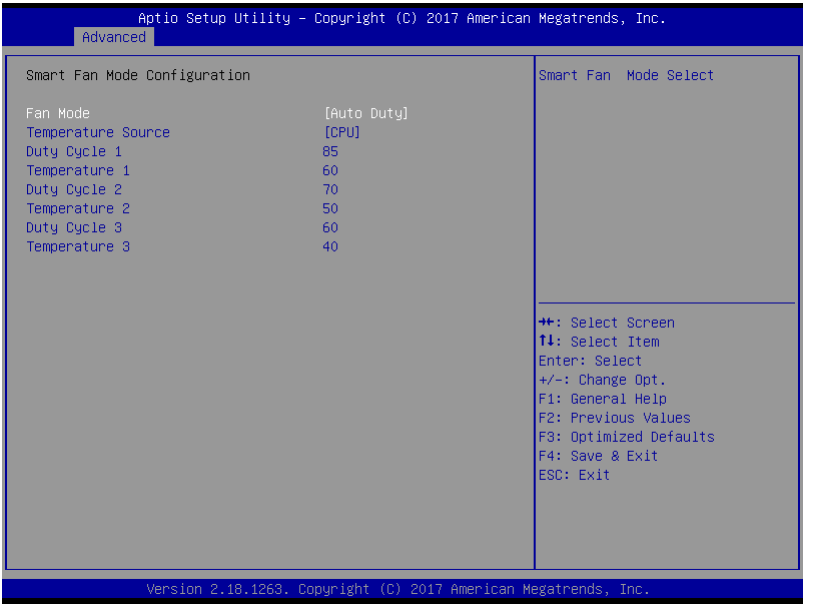


Options summary:

Smart Fan	Enabled	Enable or Disable Smart Fan
	Disabled	
FAN1 Output Mode	Output PWM mode (push pull)	
	Linear Fan Application	Optimal Default, Failsafe Default
	Output PWM mode (open drain)	
Output PWM mode (push pull) to control 4-wire fans. Linear fan application circuit to control 3-wire fan speed by fan's power terminal. Output PWM mode (open drain) to control Intel 4-wire fans.		

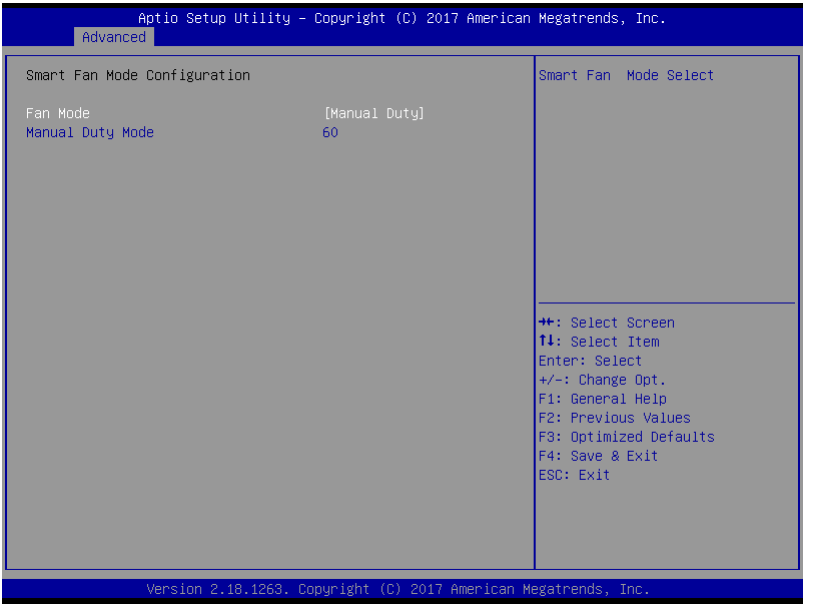
Note: Optional support for PWM mode is available on request.

3.4.4.1 Smart Fan Mode Configuration



Options summary:

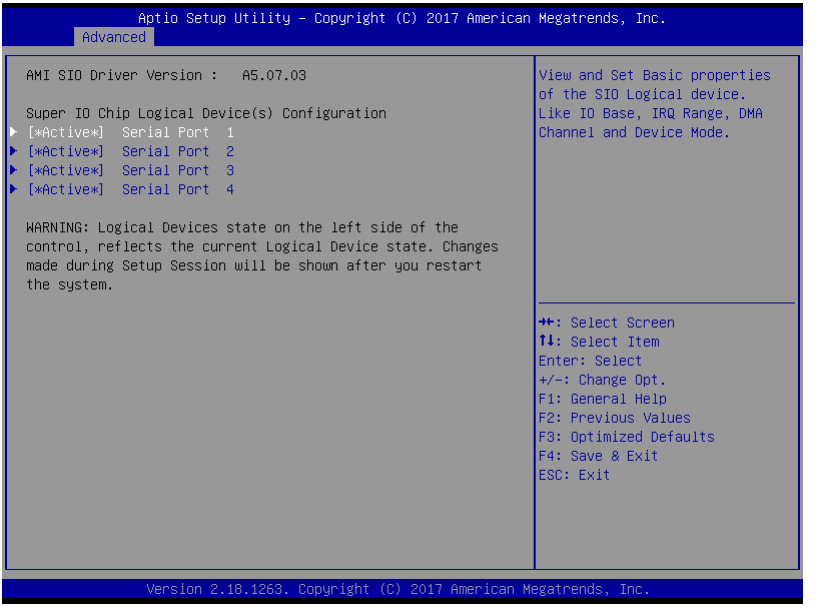
Fan Mode	Manual Duty	
	Auto Duty	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Duty Cycle	Auto fan speed control. Fan speed will follow different temperature by different duty cycle 60-100	
Temperature		



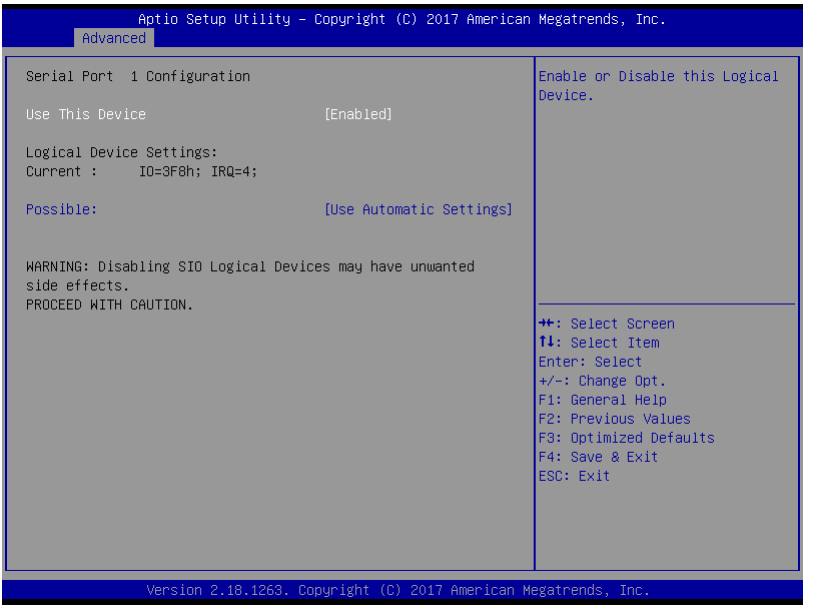
Options summary:

Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 60-100		

3.4.5 SIO Configuration



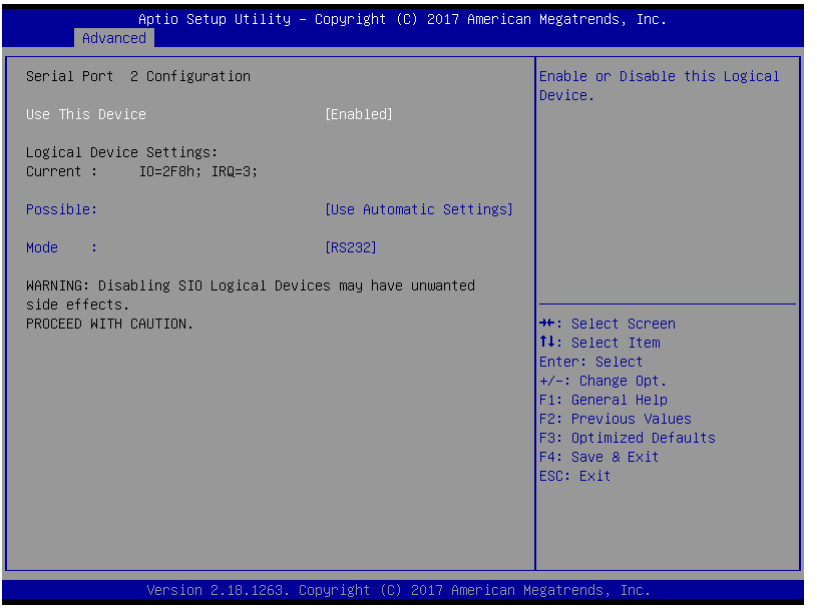
3.4.5.1 Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Select an optimal setting for IO device		

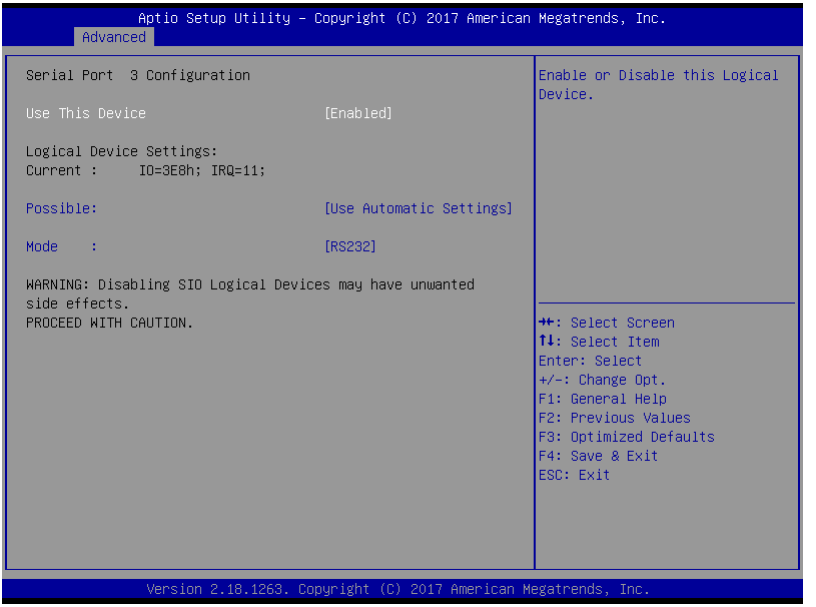
3.4.5.2 Serial Port 2 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Mode:	RS232	UART RS232, 422, 485 selection
	RS422	
	RS485	
Select an optimal setting for IO device		

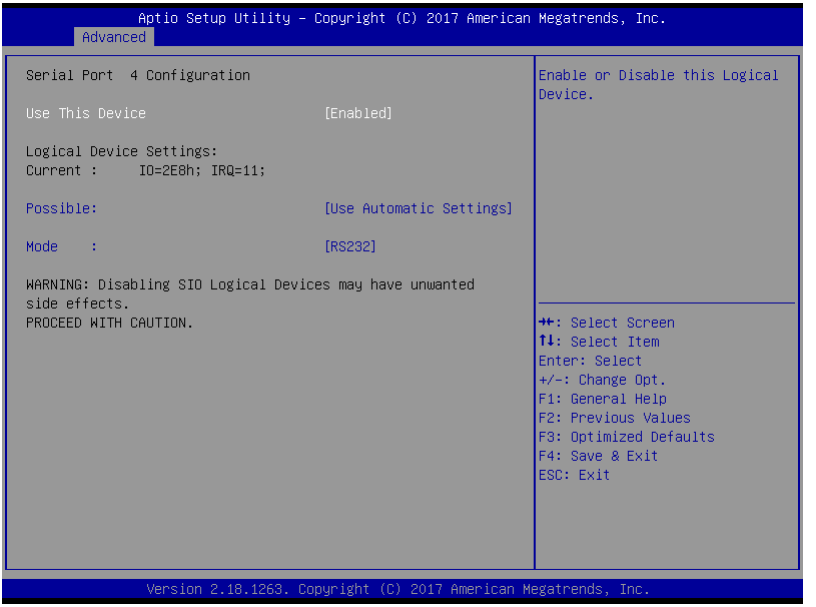
3.4.5.3 Serial Port 3 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8; IRQ=11;	
	IO=2E8; IRQ=11;	
Mode:	RS232	UART RS232, 422, 485 selection
	RS422	
	RS485	
Select an optimal setting for IO device		

3.4.5.4 Serial Port 4 Configuration



Options summary:

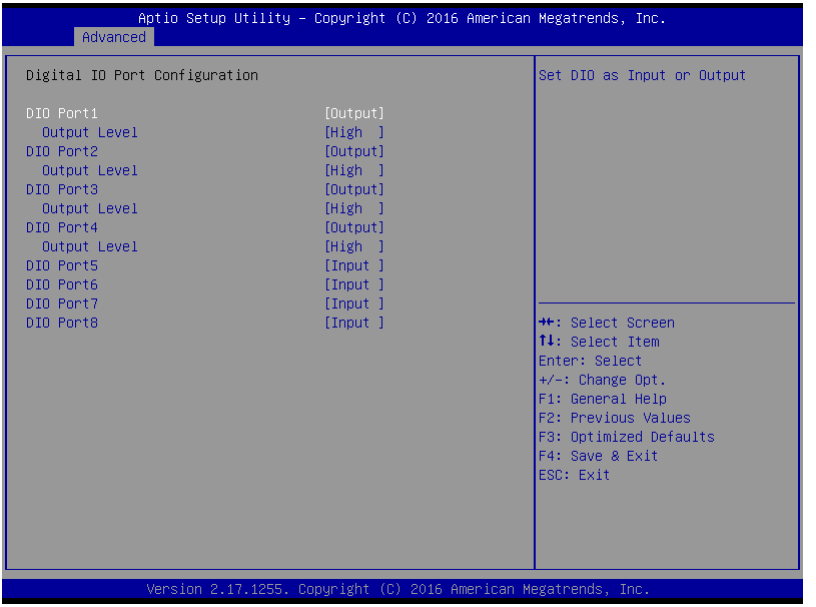
Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8; IRQ=11;	
	IO=3E8; IRQ=11;	
Mode:	RS232	UART RS232, 422, 485 selection
	RS422	
	RS485	
Select an optimal setting for IO device		

3.4.6 USB Configuration

Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		

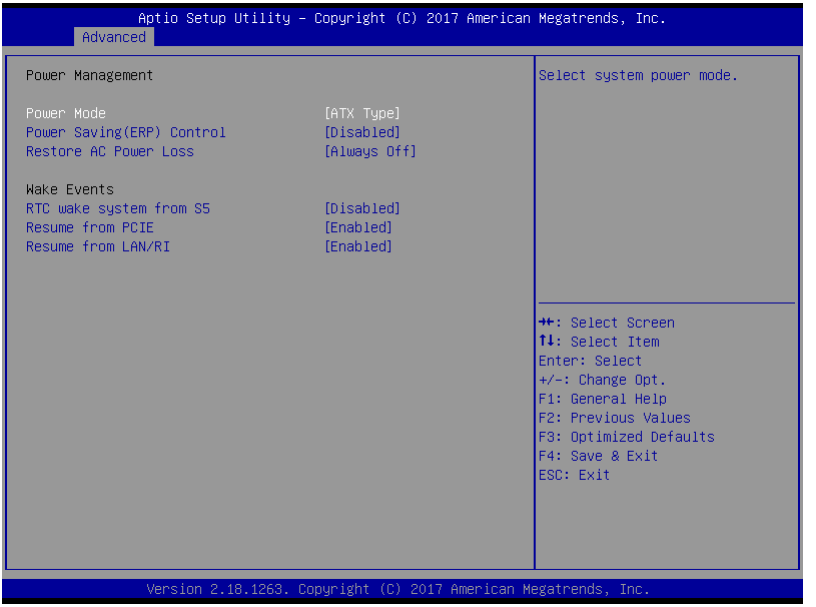
3.4.7 Digital IO Port Configuration



Options summary:

DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.4.8 Power Management

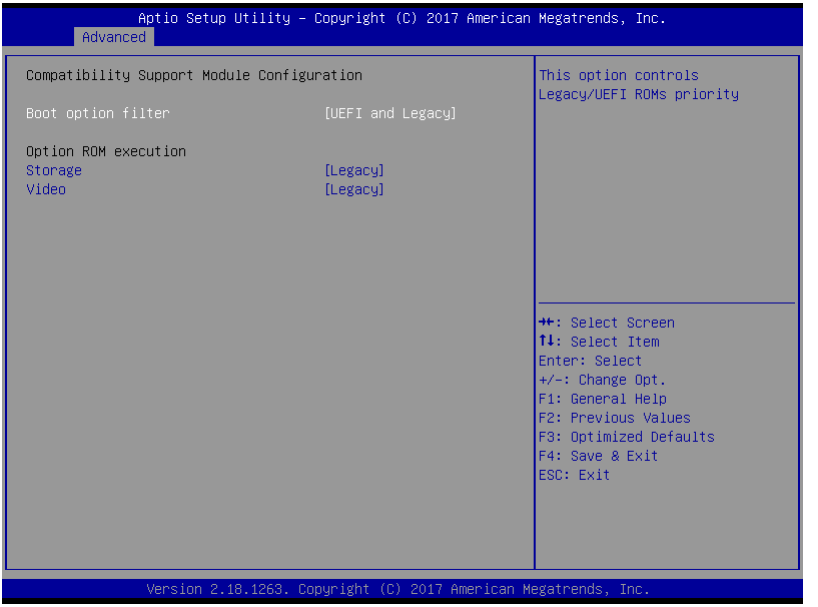


Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Power Saving(ERP) Control	Disabled	Optimal Default, Failsafe Default
	Enabled	
Configure power mode for power saving function.		
Restore on Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

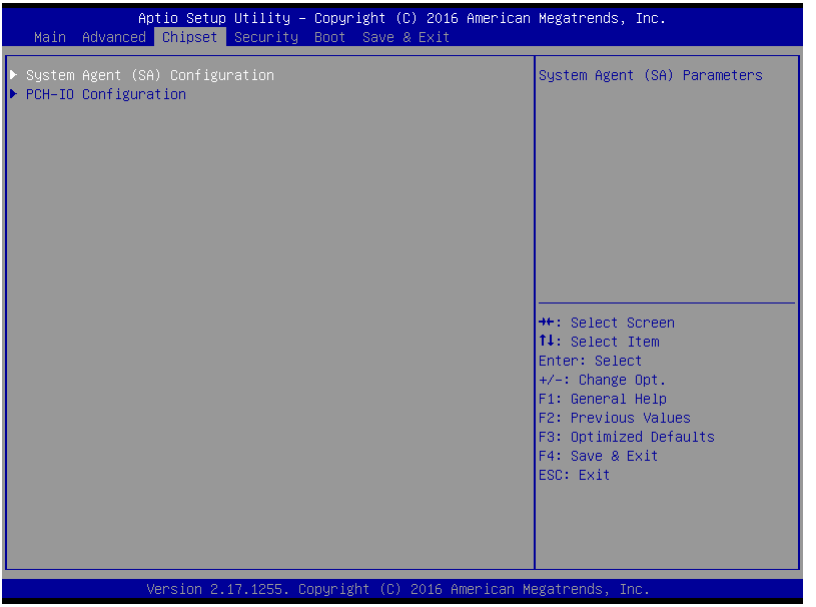
Resume from PCIE	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Resume from PCIE		
Resume from LAN/RI	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Resume from LAN/RI		

3.4.9 Compatibility Support Module Configuration



Boot option filter	UEFI and Legacy	Optimal Default, Failsafe Default
	Legacy only	
	UEFI only	
This option controls Legacy/UEFI ROMs priority		
Storage	Do not launch	
	UEFI	
	Legacy	Optimal Default, Failsafe Default
Controls the execution of UEFI and Legacy Storage OpROM		
Video	Do not launch	
	UEFI	
	Legacy	Optimal Default, Failsafe Default
Controls the execution of UEFI and Legacy Video OpROM		

3.5 Setup submenu: Chipset

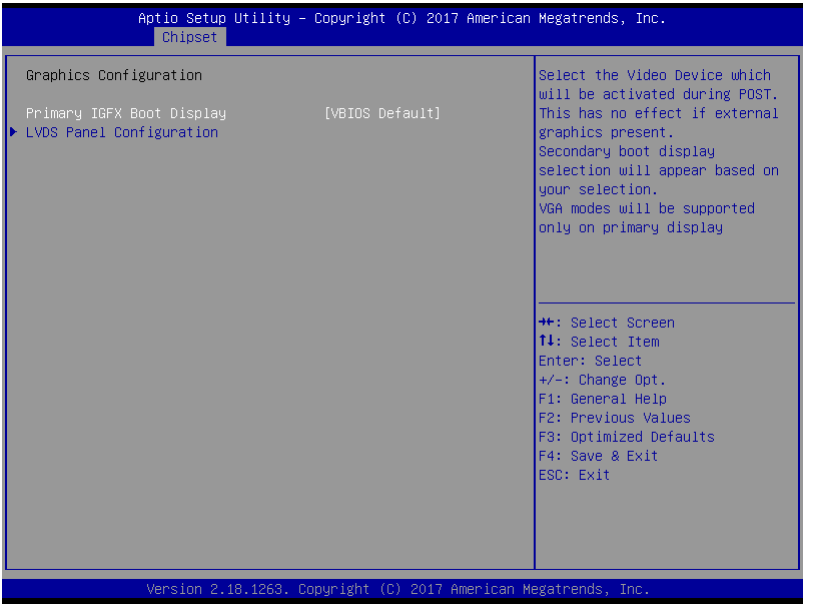


3.5.1 System Agent (SA) Configuration

Options summary:

Max TOLUD	Dynamic	Optimal Default, Failsafe Default
	1 GB	
	1.25 GB	
	1.5 GB	
	1.75 GB	
	2 GB	
	2.25 GB	
	2.5 GB	
	2.75 GB	
	3 GB	
	3.25 GB	
	3.5 GB	
Maximum Value of TOLUD Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.		

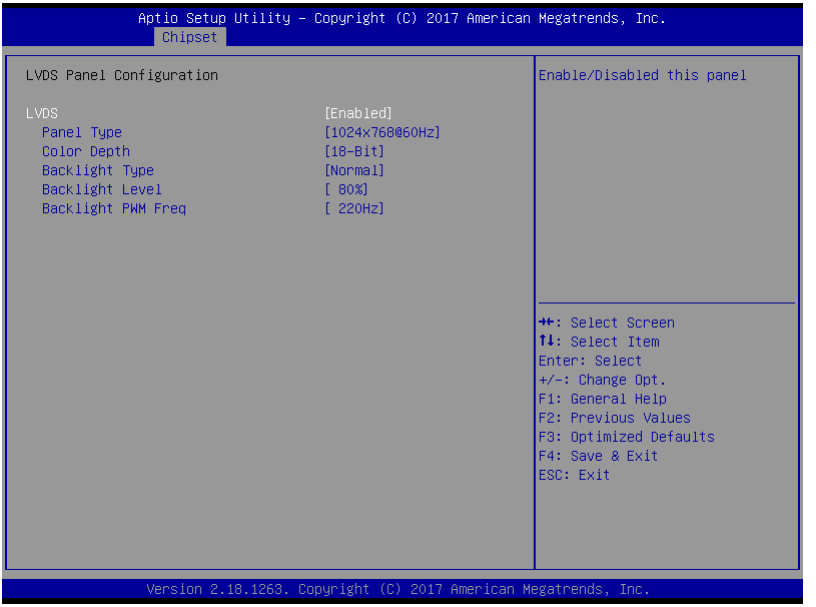
3.5.2 Graphics Configuration



Options summary:

Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	DVI	
	CRT/DP	
	LVDS	
Select the Video Device which will be activated during POST. This has no effect if external graphic present. Secondary boot display selection will appear based on your selection.		
Secondary IGFX Boot Display	Disabled	Optimal Default, Failsafe Default
	DDI1/DP	
	DDI2/VGA	
	LVDS/eDP	
Select Secondary Display Device		

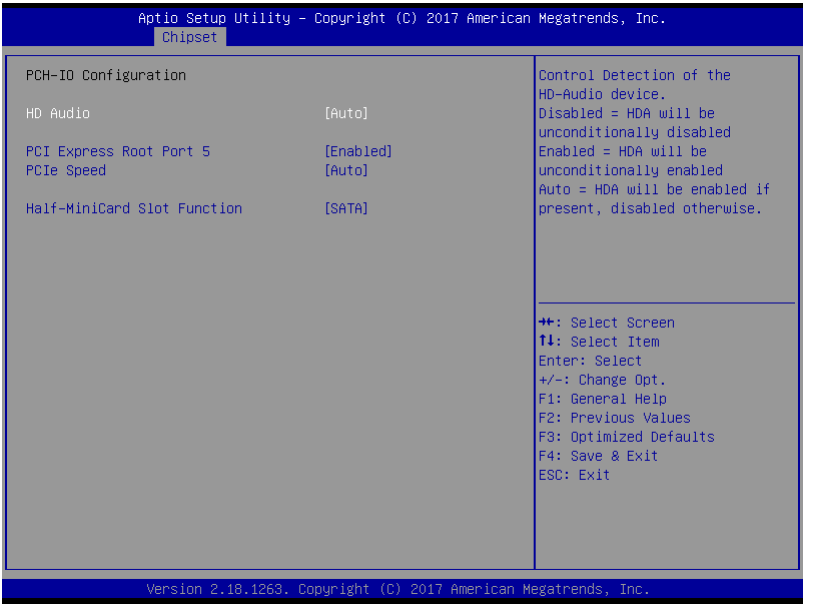
3.5.3 LVDS Panel Configuration



LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled this panel.		
LVDS Panel Type	640x480,18bit,60Hz	Optimal Default, Failsafe Default
	800x480,18bit,60Hz	
	800x600,18bit,60Hz	
	1024x600,18bit,60Hz	
	1024x768,18bit,60Hz	
	1024x768,24bit,60Hz	
	1280x768,24bit,60Hz	
	1280x1024,48bit,60Hz	
	1366x768,24bit,60Hz	
	1440x900,48bit,60Hz	
	1600x1200,48bit,60Hz	
	1920x1080,48bit,60Hz	
	1920x1200,48bit,60Hz	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	Optimal Default, Failsafe Default
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

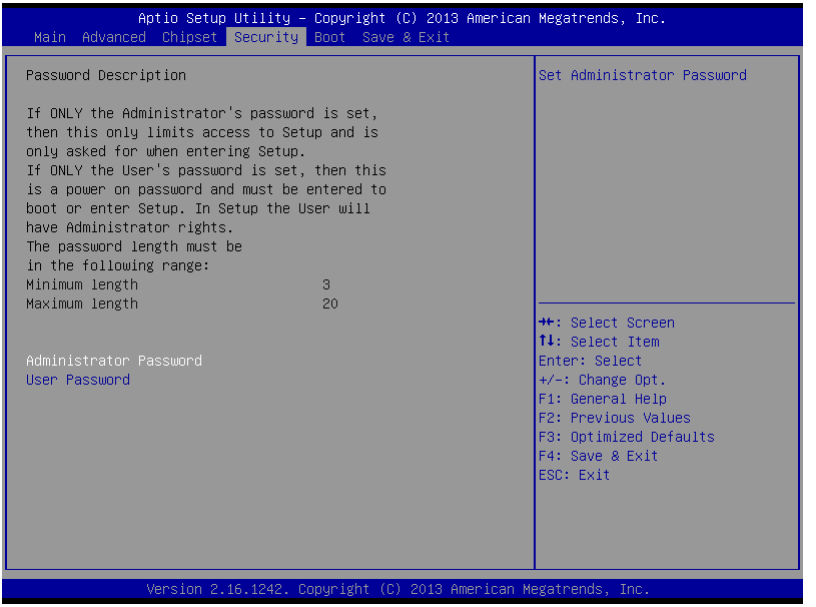
3.5.4 PCH-IO Configuration



Options summary:

HD Audio	Disabled	Optimal Default, Failsafe Default
	Enabled	
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled Auto = HDA will be enabled if present, disabled otherwise.		
PCI Express Root Port 5	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe speed.		
Half-MiniCard Slot	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Half-MiniCard(CN13) slot		

3.6 Security



Change User/Supervisor Password

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

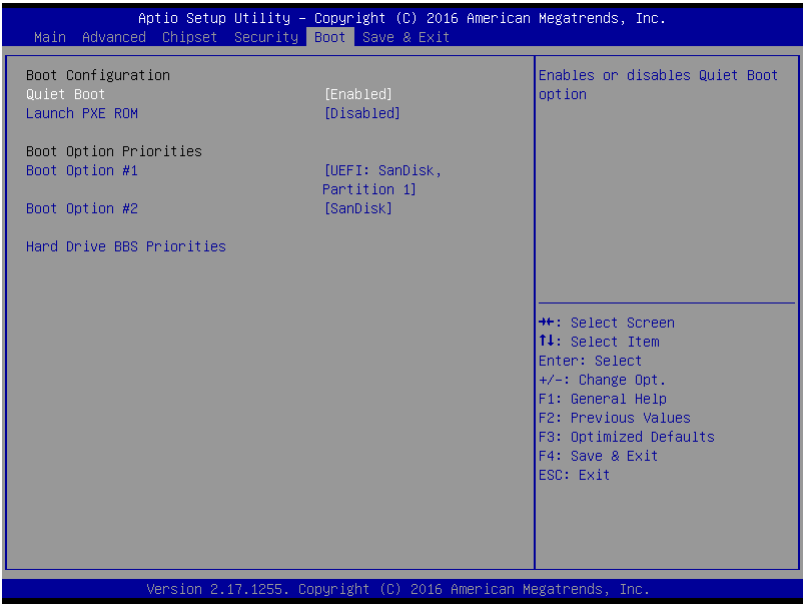
If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press

Enter to disable password protection.

3.7 Setup Submenu: Boot

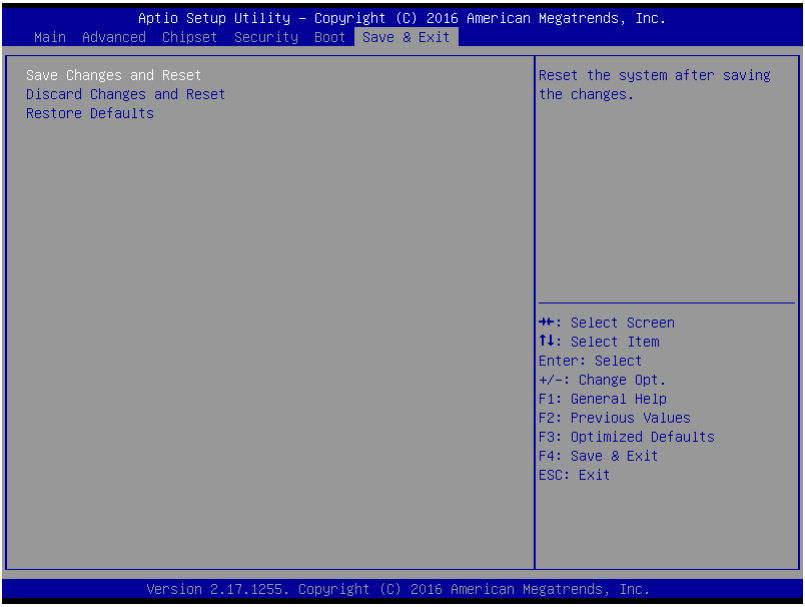


Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable showing boot logo.		
Launch PXE OpROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROm		

3.7.1 BBS Priorities

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The GENE-KBU6 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step2 - Graphic** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Click on the **Step3 - LAN** folder and select your OS
2. Open the**.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Step4 - Audio** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install PenMount Touch 6000 Driver

1. Open the **Step 5 - PenMount Touch 6000** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Serial Port Drivers (Optional)

1. Click on the **Step 6 - Serial Port Driver (Optional)** folder followed by **setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

4.2 Note on EHCI

With the EHCI controller no longer available on the 6th Gen Intel® Core™ platforms or later, it is recommended to install Windows 7 through a SATA bus, eg SATA DVD-ROM, or patch the xHCI driver onto an installation media for Windows 7. More information can be found in the links below.

Windows 7 USB 3.0 Creator Utility

Read me

For input devices, please use an add-on standard EHCI controller expansion card, such as PCIe to USB 2.0 conversion card.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s **Pulse width is must longer then 16ms.**
Signal Polarity	0x05	2	0	0: low active 1: high active **Must set this bit to 0**
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse **Must set this bit to 1**
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr        0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
      #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
      #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg       0x05   // Timer register
      #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
      #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
      #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
      #define   PolarityVal    0x00     // Low active for WDTRST#
      #define   UnitBit          0x03     // Unit for timer (Bit3)
      #define   ModeBit          0x04     // WDTRST# mode (Bit4)
      #define   ModeVal          0x01     // 0:level 1: pulse
      #define   EnableBit       0x05     // WDT timer enable (Bit5)
      #define   EnableVal       0x01     // 1: enable
      #define   StatusBit       0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*************************************************************************

*************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig(Counter, Unit);

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*************************************************************************

*************************************************************************
// Procedure : AaeonWDTEnable
```

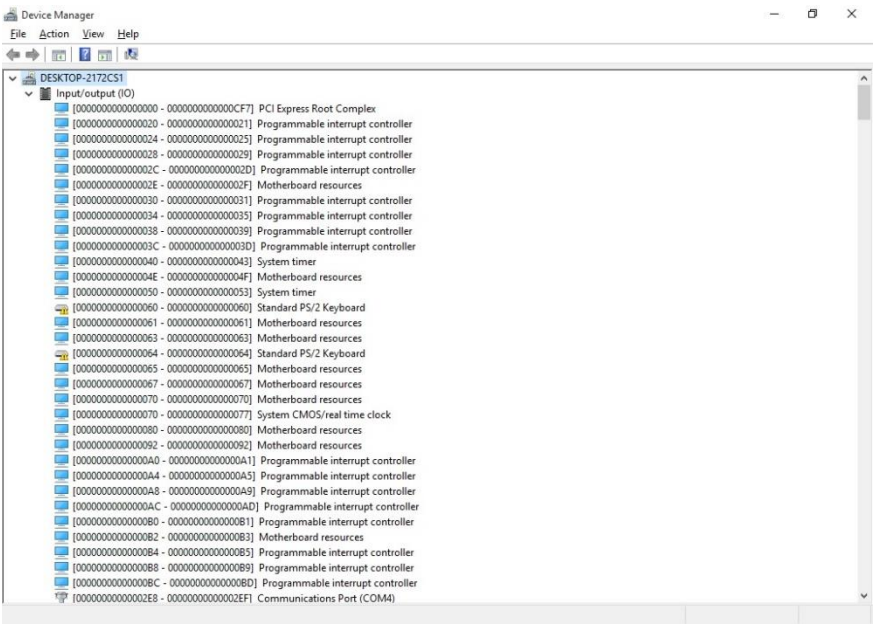
```
VOID    AaeonWDTEnable (){
          WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
          // Disable WDT counting
          WDTEnableDisable(0);
          // Clear Watchdog Timeout Status
          WDTClearTimeoutStatus();
          // WDT relative parameter setting
          WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
          If (Value == 1)
              WDTSetBit(TimerReg, EnableBit, 1);
          else
              WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
          // Watchdog Timer counter setting
         WDTWriteByte(CounterReg, Counter);
        // WDT counting unit setting
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
          // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
```

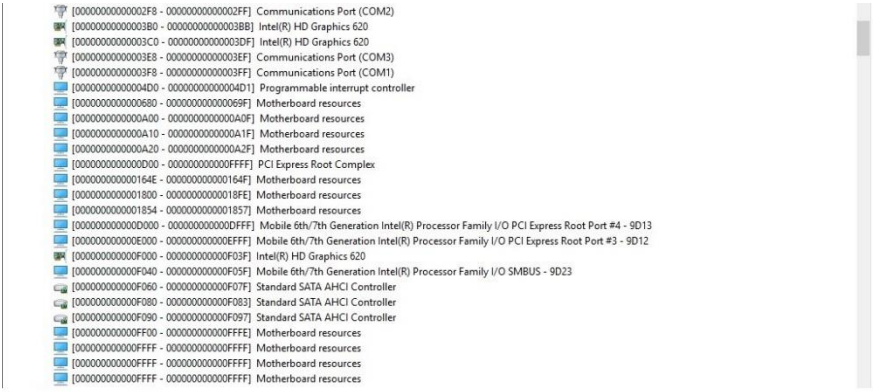
```
VOID   WDTWriteByte(byte Register, byte Value){
       IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
       return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
       byte TmpValue;

       TmpValue = WDTReadByte(Register);
       TmpValue &= ~(1 << Bit);
       TmpValue |= Val << Bit;
       WDTWriteByte(Register, TmpValue);
}

*******************************************************************************
```

Appendix B

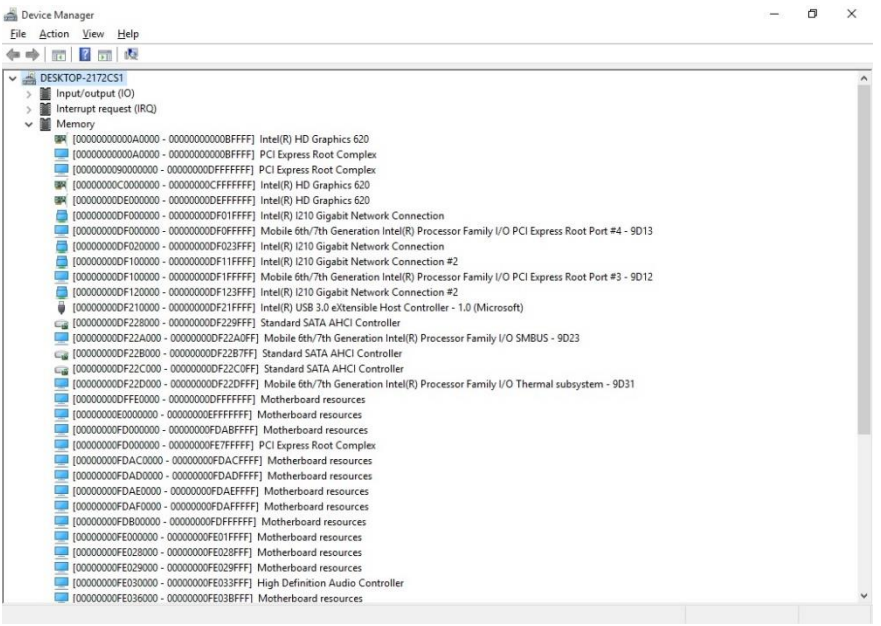
I/O Information

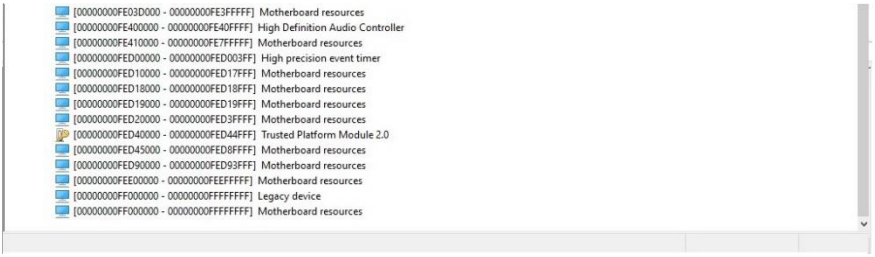
B.1 I/O Address Map



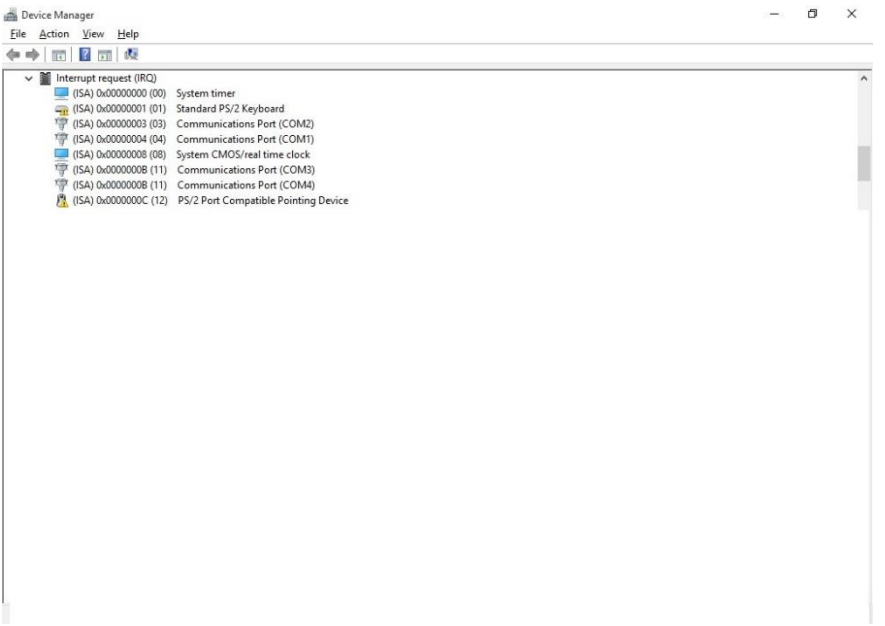

[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[00000000000003B0 - 00000000000003BB] Intel(R) HD Graphics 620
[00000000000003C0 - 00000000000003DF] Intel(R) HD Graphics 620
[00000000000003E8 - 00000000000003EF] Communications Port (COM3)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000680 - 0000000000000069F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 000000000000189FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[000000000000D000 - 000000000000DFFF] Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #4 - 9D13
[000000000000E000 - 000000000000EFFF] Mobile 6th/7th Generation Intel(R) Processor Family I/O PCI Express Root Port #3 - 9D12
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics 620
[000000000000F040 - 000000000000F05F] Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources

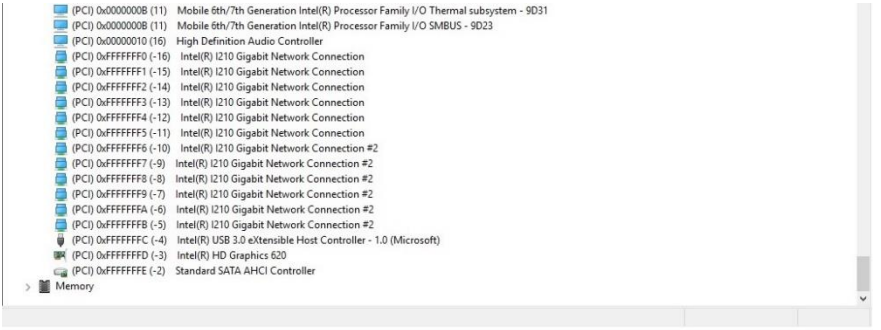
B.2 Memory Address Map




[00000000FE03D000 - 00000000FE3FFFFF] Motherboard resources
[00000000FE400000 - 00000000FE40FFFF] High Definition Audio Controller
[00000000FE410000 - 00000000FE7FFFFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED10000 - 00000000FED17FFF] Motherboard resources
[00000000FED18000 - 00000000FED18FFF] Motherboard resources
[00000000FED19000 - 00000000FED19FFF] Motherboard resources
[00000000FED20000 - 00000000FED3FFFF] Motherboard resources
[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
[00000000FED45000 - 00000000FED8FFFF] Motherboard resources
[00000000FED90000 - 00000000FED93FFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF] Legacy device
[00000000FF000000 - 00000000FFFFFFFF] Motherboard resources

B.3 IRQ Mapping Chart




(PCI) 0x0000000B (11) Mobile 6th/7th Generation Intel(R) Processor Family I/O Thermal subsystem - 9D31
(PCI) 0x0000000B (11) Mobile 6th/7th Generation Intel(R) Processor Family I/O SMBUS - 9D23
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0xFFFFFFF0 (-16) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF1 (-15) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF2 (-14) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF3 (-13) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF4 (-12) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF5 (-11) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFF6 (-10) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFF7 (-9) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFF8 (-8) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFF9 (-7) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFFA (-6) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFFB (-5) Intel(R) I210 Gigabit Network Connection #2
(PCI) 0xFFFFFFFC (-4) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFFD (-3) Intel(R) HD Graphics 620
(PCI) 0xFFFFFFFE (-2) Standard SATA AHCI Controller
Memory

Appendix C

Electrical Specifications for I/O Ports

C.1 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
DVI Port	CN3	+5V	+5V/1A (reserved)
DP port	CN5	+3.3V	+3.3V/1A
LVDS Port	CN6	+3.3V/+5V	+3.3V/2A or +5V/2A
LVDS Port Inverter / Backlight Connector	CN7	+5V/+12V	+5V/1.5A or +12V/1.5A
Mini-Card Slot (Full-Mini Card)	CN11	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
Mini-Card Slot (Half-Mini Card)	CN13	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
+5V Output for SATA HDD	CN15	+5V	+5V/1A
USB 3.0 Ports	CN18	+5VSB	+5V/1A (per channel)
USB 3.0 Ports	CN19	+5VSB	+5V/1A (per channel)
USB 2.0 Ports	CN20	+5VSB	+5V/0.5A (per channel)
USB 2.0 Ports	CN21	+5VSB	+5V/0.5A (per channel)

Audio I/O Port	CN22	+5V	+5V/1A
Digital IO Port	CN24	+5V	+5V/1A
COM Port 4	CN26	+5V/+12V	+5V/0.5A or +12V/0.5A
COM Port 2	CN27	+5V/+12V	+5V/0.5A or +12V/0.5A
COM Port 3	CN28	+5V/+12V	+5V/0.5A or +12V/0.5A
LPC Port	CN29	+3.3V	+3.3V/0.5A
CPU FAN	CN36	+12V	+12V/0.5A

Appendix D

Digital I/O Ports

D.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification						
Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO0	I/O	0.8	2.0	0	5	
DIO1	I/O	0.8	2.0	0	5	
DIO2	I/O	0.8	2.0	0	5	
DIO3	I/O	0.8	2.0	0	5	
DIO4	I/O	0.8	2.0	0	5	
DIO5	I/O	0.8	2.0	0	5	
DIO6	I/O	0.8	2.0	0	5	
DIO7	I/O	0.8	2.0	0	5	

Note: All DIO pins are 5V tolerant in input mode.

D.2 DI/O Programming

GENE-KBU6 utilizes FINTEK F81866D chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DI/O program is also attached, based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode

(2) Modify the data of configuration registers

(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

D.3 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	Register	Bit	Note
DIO0 Direction	0x06	0xA0	0	0:input, 1: output
DIO1 Direction	0x06	0xA0	1	
DIO2 Direction	0x06	0xA0	2	
DIO3 Direction	0x06	0xA0	3	
DIO4 Direction	0x06	0xA0	4	
DIO5 Direction	0x06	0xA0	5	
DIO6 Direction	0x06	0xA0	6	
DIO7 Direction	0x06	0xA0	7	
DIO0 Output Level	0x06	0xA1	0	0:low, 1: high
DIO1 Output Level	0x06	0xA1	1	
DIO2 Output Level	0x06	0xA1	2	
DIO3 Output Level	0x06	0xA1	3	
DIO4 Output Level	0x06	0xA1	4	
DIO5 Output Level	0x06	0xA1	5	
DIO6 Output Level	0x06	0xA1	6	
DIO7 Output Level	0x06	0xA1	7	
DIO0 Status	0x06	0xA2	0	0:low, 1: high
DIO1 Status	0x06	0xA2	1	
DIO2 Status	0x06	0xA2	2	
DIO3 Status	0x06	0xA2	3	
DIO4 Status	0x06	0xA2	4	
DIO5 Status	0x06	0xA2	5	
DIO6 Status	0x06	0xA2	6	
DIO7 Status	0x06	0xA2	7	

D.4 Digital I/O Sample Program

```
*****************************************************************************
// SuperIO relative definition (Please reference to Table 2)
#define   SIOIndex   0x2E
#define   SIOData    0x2F
#define   DIOLDN     0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define   DirReg          0xA0          // 0:input, 1: output
    #define   InputPin    0x00
    #define   OutputPin   0x01
#define   OutputReg       0xA1          // 0:low, 1: high
#define   StatusReg       0xA2          // 0:low, 1: high
    #define   PinLow      0x00
    #define   PinHigh     0x01
#define   Pin0Bit         0x00
#define   Pin1Bit         0x01
#define   Pin2Bit         0x02
#define   Pin3Bit         0x03
#define   Pin4Bit         0x04
#define   Pin5Bit         0x05
#define   Pin6Bit         0x06
#define   Pin7Bit         0x07

*****************************************************************************

*****************************************************************************
VOID   Main(){
      Boolean PinStatus ;

      // Procedure : AaeonReadPinStatus
      // Input :
      //      Example, Read Digital I/O Pin 3 status
       // Output :
       //     InputStatus :
       //              0: Digital I/O Pin level is low
       //              1: Digital I/O Pin level is High
      PinStatus = AaeonReadPinStatus(Pin3Bit);

      // Procedure : AaeonSetOutputLevel
```

```
        // Input :
        //      Example, Set Digital I/O Pin 2 to high level
        AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****************************************************************************

*****************************************************************************
Boolean   AaeonReadPinStatus(byte PinBit){
        Boolean PinStatus ;
        PinStatus = SIOBitRead(DIOLDN, StatusReg, PinBit);
        Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte PinBit, byte Value){
        ConfigDioMode(PinBit, OutputPin);
        SIOBitSet(DIOLDN, OutputReg, PinBit, Value);
}
*****************************************************************************

*****************************************************************************VOID
SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
```

```
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*****************************************************************************

*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigDioMode(byte PinBit, byte Mode){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(DIOLDN);
        IOWriteByte(SIOIndex, DirReg);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (Mode << PinBit);
        IOWriteByte(SIOData, DirReg);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix E

List of Mating Connectors and Cables

E.1 Electrical Specifications for I/O Ports

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no.		
CN1	External RTC Connector	Molex	51021-0200	Battery Cable	175011901C
CN6	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN7	LVDS Inverter Connector	JST	PHR-5	N/A	N/A
CN14	SATA Connector	Molex	88750-5318	SATA Cable	1709070500
CN15	+5Vout Connector	JST	PHR-2	2 Pins For HDD Power	1702150155
CN20	USB Port Connector	Molex	51021-0500	USB Wafer Cable	1700050207
CN21	USB Port Connector	Molex	51021-0500	USB Wafer Cable	1700050207
CN22	Audio Connector	Molex	51021-1000	Audio Cable	1709100254
CN23	Touch Screen Connector	JST	SHR-9V-S-B	N/A	N/A

CN24	Digital I/O Connector	Neltron	2026B-10	N/A	N/A
CN25	COM Port 1 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN26	COM Port 4 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN27	COM Port 2 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN28	COM Port 3 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN30	+9~24V Vin Connector	N/A	N/A	Power Cable	1702002010
CN32	External +5VSB Power output and PS_ON#	Catch Electronics	2418HJ-06	N/A	N/A
CN33	External +5VSB Power Input and PS_ON#	JST	PHR-3	ATX Cable	170220020B

CN36	CPU Fan Connector	Molex	22-01-2035	N/A	N/A