GENE-CML5

3.5" Subcompact Board

User's Manual 1st Ed

Last Updated: December 24, 2020

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Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
GENE-CML5	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	3.5" Subcompact Board
CPU	Intel® 10th Generation Core™ i7/i5/i3/Pentium/Celeron SoC i7-10700TE (8C, 2.0 GHz, up to 4.4 GHz) i5-10500TE (6C, 2.3 GHz, up to 3.7 GHz) i3-10100TE (4C, 2.3 GHz, up to 3.6 GHz) G6400TE (2C, 3.2 GHz) G5900TE (2C, 3.0 GHz)
CPU Frequency	Up to 4.4GHz
Chipset	Integrated SoC
Memory Type	DDR4 2933/2666/2400 MHz SODIMM x 2 (Dual Channel, Non-ECC)
Max. Memory Capacity	Up to 64GB
BIOS	AMI UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V
Power Supply Type	AT/ATX (Default: AT)
Power Consumption (Typical)	TBD
Dimension (L x W)	5.75" x 4" (146mm x 101.7mm)
Operating Temperature	32°F ~ 122°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 81°C)
Operating Humidity	0-90% @ 40°C, non-condensing
MTBF (Hours)	TBD
Certification	CE/FCC Class A

Display

VGA/LCD Controller	Intel® UHD Graphics 630 for 10th Gen Intel® Processors
Video Output	DP++ x 1
	VGA x 1
	LVDS x 1
Backlight Inverter supply	Max 12V, 2A

I/O

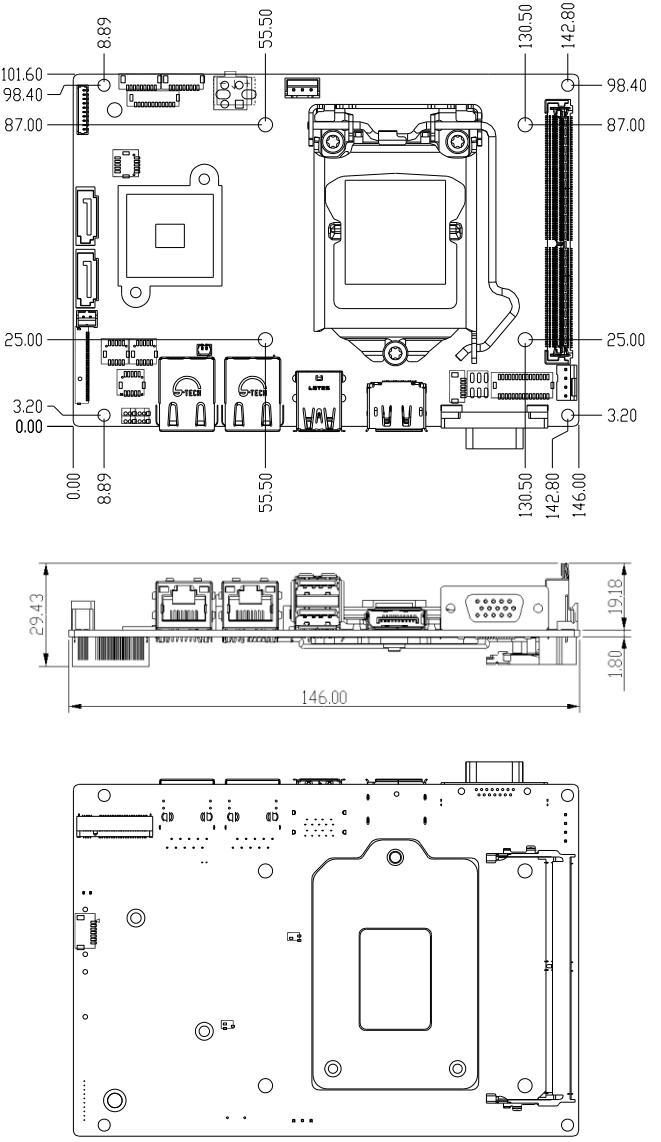
Ethernet	Intel® i210/i211,10/100/1000Base, RJ45 x1
	Intel® i219,10/100/1000Base, RJ45 x1 (Support vPro® only with i5/i7 + Q470/Q470E variant)
Audio	High Definition Audio Interface,
	Line-in/Line-out/MIC (Without Amplifier)
USB Port	USB3.2 Gen 2 x 2 (Rear I/O, Gen 2 for Q470/Q470E only)
	USB2.0 x 4 (Pin header)
Serial Port	RS-232/422/485 x 2
Parallel Port	—
HDD Interface	—
FDD Interface	—
SSD	SATA III (6.0 Gbps) x 2
	SATA power connector x 1 (+5V)
Expansion Slot	M.2 M Key 2280 PCIe [x4]/SATA x 1
	FPC x 1 (For Q470/Q470E only)
DIO	8bit
SIM	—

I/O	
TPM	TPM 2.0
Touch	—
Others	—

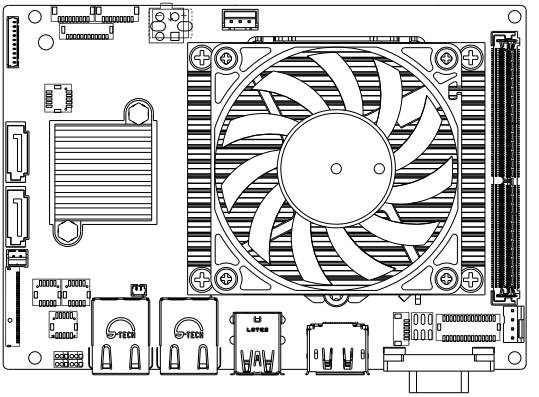
Chapter 2

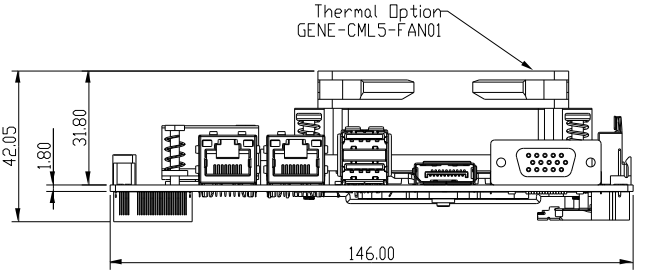
Hardware Information

2.1 Dimensions

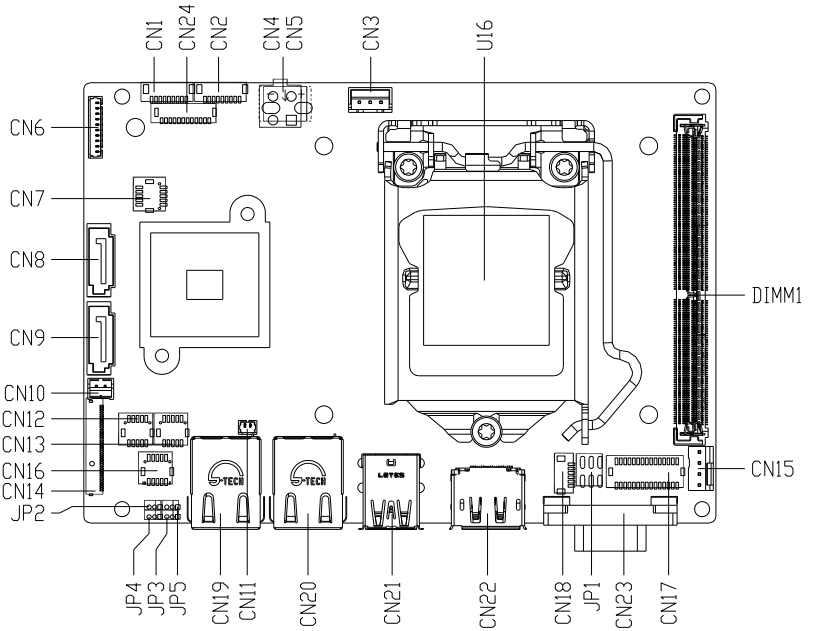


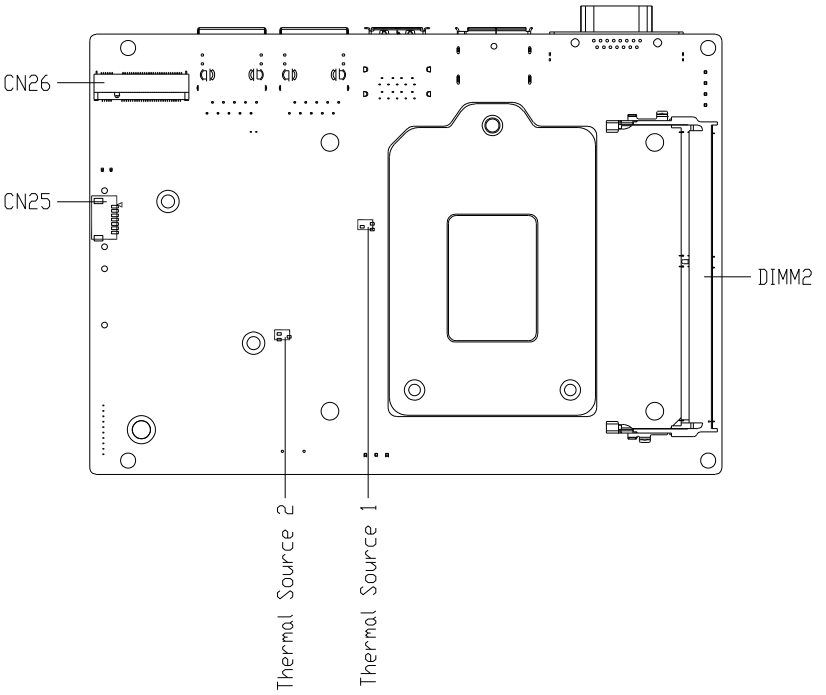
With Thermal Option (Part No. GENE-CML5-FAN01)





2.2 Jumpers and Connectors



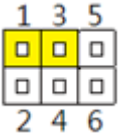

CN26
CN25
DIMM2
Thermal Source 2
Thermal Source 1

2.3 List of Jumpers

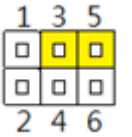
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	LVDS Operating VDD Selection & Backlight VCC Selection
JP2	Auto Power Button Enable/Disable Selection
JP3	LVDS Backlight (BKLT) Control Selection
JP5	Clear CMOS

2.3.1 LVDS Operating VDD Selection (JP1)



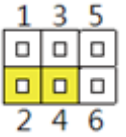
+3.3V (Default)



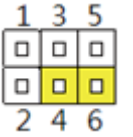
+5V

Note: To avoid damage to the system, do connect Pins 1,3,5 with Pins 2,4,6.

2.3.2 LVDS Backlight VCC Selection (JP1)



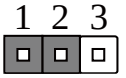
+12V



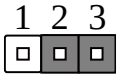
+5V (Default)

Note: To avoid damage to the system, do connect Pins 1,3,5 with Pins 2,4,6.

2.3.3 Auto Power Button Enable/Disable Selection (JP2)



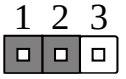
Disabled



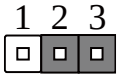
Enabled (**Default**)

Note: When disabled, Power Button must be used to power on the system.

2.3.4 LVDS Backlight Control Selection (JP3)

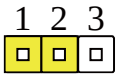


VR Mode

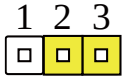


PWM Mode (**Default**)

2.3.5 Clear CMOS Jumper (JP5)



Normal (**Default**)



Clear CMOS

2.4 List of Connectors

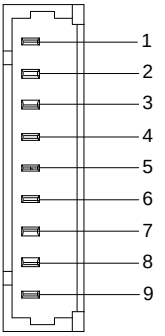
Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	COM Port 2
CN2	COM Port 1
CN3	External +5VSB Input
CN5	External Power Input
CN6	Audio I/O Port
CN7	Digital IO Port
CN8	SATA Port
CN9	SATA Port
CN10	+5V Output for SATA HDD
CN11	Battery Connector
CN12	USB 2.0 Port
CN13	USB 2.0 Port
CN14	FPC
CN15	FAN CONN
CN16	Front Panel header
CN17	LVDS Port
CN18	LVDS Port Inverter / Backlight Connector
CN19	LAN (RJ-45) Port 2
CN20	LAN (RJ-45) Port 1
CN21	USB3.2 Gen2 Port 1/ Port 2 (Dual Port)
CN22	DP++ Port
CN23	VGA Port
CN24	LPC Port

Label	Function
CN25	BIOS Debug Port
CN26	M.2 M-Key
DIMM1	DDR4 SO-DIMM Slot
DIMM2	DDR4 SO-DIMM Slot

2.4.1 COM Port 1/ Port 2 (CN1/CN2)

Note: CN1 is COM Port 2; and CN2 is COM Port 1.



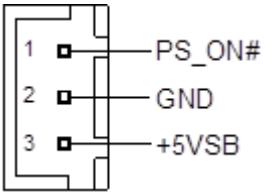
RS-232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	
5	TX	OUT	
6	CTS	IN	
7	DTR	OUT	
8	RI	IN	
9	GND	GND	

RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_ D-	I/O	
2	NC		
3	RS485_D+	I/O	
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	GND	GND	

RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	
2	NC		
3	RS422_TX+	OUT	
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC		
9	GND	GND	

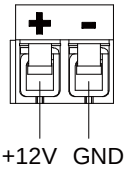
Note 1: COM Port RS-232/422/485 can be set by BIOS. Default is RS-232.

2.4.2 External +5VSB Input (CN3)



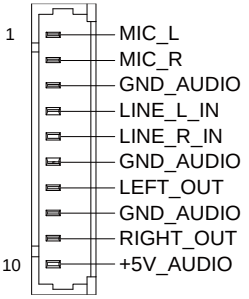
Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+5V
2	GND	GND	
3	+V5A_SB_IN	PWR	+5V

2.4.3 External Power Input (CN5)



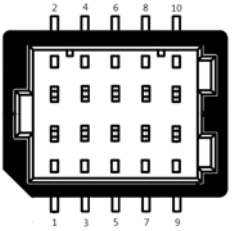
Pin	Pin Name	Signal Type	Signal Level
1	+VIN_EXT	PWR	12V
2	GND	GND	

2.4.4 Audio I/O Port (CN6)



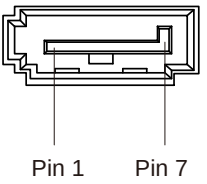
Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L	IN	
5	LINE_R	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

2.4.5 Digital I/O Port (CN7)



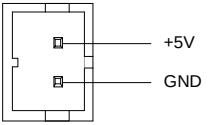
Pin	Pin Name	Signal Type	Signal Level
1	+V5S	PWR	+5V
2	DIO0	I/O	
3	DIO1	I/O	
4	DIO2	I/O	
5	DIO3	I/O	
6	DIO4	I/O	
7	DIO5	I/O	
8	DIO6	I/O	
9	DIO7	I/O	
10	GND	GND	

2.4.6 SATA Port (CN8/CN9)



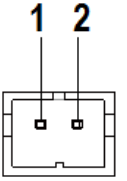
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.7 +5V Output for SATA HDD (CN10)



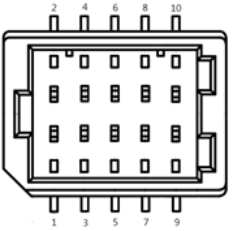
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

2.4.8 Battery Connector (CN11)



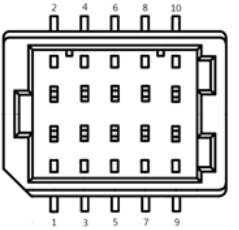
Pin	Pin Name	Signal Type	Signal level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.4.9 USB 2.0 Port (CN12)



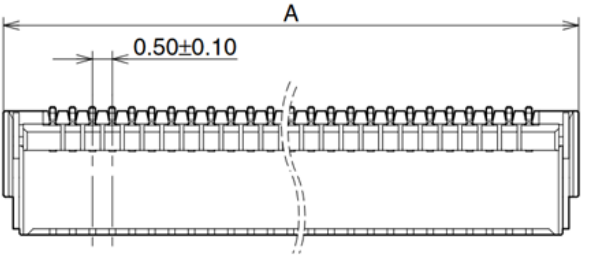
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_3	PWR	+5V
2	+V5A_USB_3	PWR	+5V
3	USBD5-	DIFF	
4	USBD6-	DIFF	
5	USBD5+	DIFF	
6	USBD6+	DIFF	
7	GND	GND	
8	GND	GND	
9	GND	GND	
10	GND	GND	

2.4.10 USB 2.0 Port (CN13)



Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_2	PWR	+5V
2	+V5A_USB_2	PWR	+5V
3	USBD3-	DIFF	
4	USBD4-	DIFF	
5	USBD3+	DIFF	
6	USBD4+	DIFF	
7	GND	GND	
8	GND	GND	
9	GND	GND	
10	GND	GND	

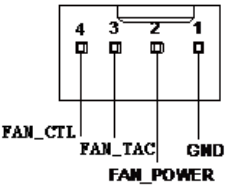
2.4.11 FPC (CN14)



Pin	Pin Name	Signal Type	Signal Level
1	+V3P3S	PWR	+3.3V
2	+V3P3S	PWR	+3.3V
3	+V3P3S	PWR	+3.3V
4	SMB_DATA	I/O	
5	SMB_CLK	I/O	
6	BUF_PLT_RST#	I/O	
7	+V3P3A	PWR	+3.3V
8	GND	GND	
9	PCIE_18_RXP	DIFF	
10	PCIE_18_RXN	DIFF	
11	GND	GND	
12	PCIE_20_RXP	DIFF	
13	PCIE_20_RXN	DIFF	
14	GND	GND	
15	PCIE_19_RXP	DIFF	
16	PCIE_19_RXN	DIFF	
17	GND	GND	

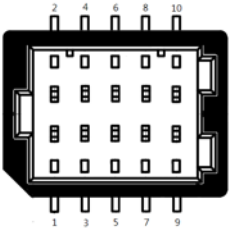
Pin	Pin Name	Signal Type	Signal Level
18	PCIE_17_RXP	DIFF	
19	PCIE_17_RXN	DIFF	
20	GND	GND	
21	PCIE_20_TXN	DIFF	
22	PCIE_20_TXP	DIFF	
23	GND	GND	
24	PCIE_19_TXN	DIFF	
25	PCIE_19_TXP	DIFF	
26	GND	GND	
27	PCIE_18_TXN	DIFF	
28	PCIE_18_TXP	DIFF	
29	GND	GND	
30	CLK_PCIE_FPC_N	DIFF	
31	CLK_PCIE_FPC_P	DIFF	
32	GND	GND	
33	PCIE_17_TXN	DIFF	
34	PCIE_17_TXP	DIFF	
35	GND	GND	
36	+V12S	PWR	
37	+V12S	PWR	
38	+V12S	PWR	
39	+V12S	PWR	
40	+V12S	PWR	

2.4.12 CPU Fan (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	OUT	
4	FAN_CTL	IN	

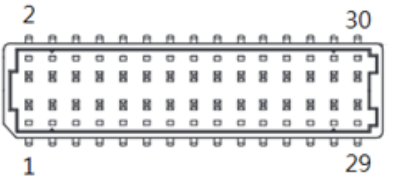
2.4.13 Digital I/O Port (CN16)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	EXT_PWRBTN#	I/O	
3	FP_HDLED-	I/O	
4	FP_HDLED+	I/O	
5	FP_SPKR-	I/O	

Pin	Pin Name	Signal Type	Signal Level
6	+V5S	PWR	
7	GND	GND	
8	PWRLED+	I/O	
9	GND	GND	
10	HWRST#	I/O	

2.4.14 LVDS Port (CN17)

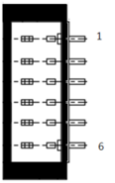


Note: LVDS Operating VDD can be set by JP1, reference Ch 2.3.1 for details

Pin	Pin Name	Signal Type	Signal Level
1	LVDS_BKLTEN	I/O	
3	+VDD_LVDS	PWR	
5	LVDSA_CLK#	DIFF	
7	+VDD_LVDS	PWR	
9	LVDSA_DATA0#	DIFF	
11	LVDSA_DATA1#	DIFF	
13	LVDSA_DATA2#	DIFF	
15	LVDSA_DATA3#	DIFF	
17	LVDS_DDC_DATA	I/O	
19	LVDSB_DATA0#	DIFF	

Pin	Pin Name	Signal Type	Signal Level
21	LVDSB_DATA1#	DIFF	
23	LVDSB_DATA2#	DIFF	
25	LVDSB_DATA3#	DIFF	
27	+VDD_LVDS	PWR	
29	LVDSB_CLK#	DIFF	
2	LVDS_BKLCTL	I/O	
4	GND	GND	
6	LVDSA_CLK	DIFF	
8	GND	GND	
10	LVDSA_DATA0	DIFF	
12	LVDSA_DATA1	DIFF	
14	LVDSA_DATA2	DIFF	
16	LVDSA_DATA3	DIFF	
18	LVDS_DDC_CLK	I/O	
20	LVDSB_DATA0	DIFF	
22	LVDSB_DATA1	DIFF	
24	LVDSB_DATA2	DIFF	
26	LVDSB_DATA3	DIFF	
28	GND	GND	
30	LVDSB_CLK	DIFF	

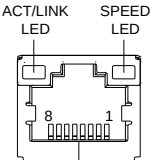
2.4.15 LVDS Port Inverter/ Backlight Connector (CN18)



Pin	Pin Name	Signal Type	Signal level
1	+VCC_LVDS_BKLT	PWR	
2	+VCC_LVDS_BKLT	PWR	
3	L_BKLTNESS	I/O	
4	GND	GND	
5	GND	GND	
6	LVDS_BKLTEN	I/O	

Note 1: LVDS Backlight VCC can be by JP1. (See Ch 2.3.2)

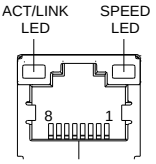
2.4.16 LAN (RJ-45) Port 2 (CN19)



Pin	Pin Name	Signal Type	Signal level
1	LAN2_MDI0+	DIFF	
2	LAN2_MDI0-	DIFF	
3	LAN2_MDI1+	DIFF	
4	LAN2_MDI2+	DIFF	
5	LAN2_MDI2-	DIFF	

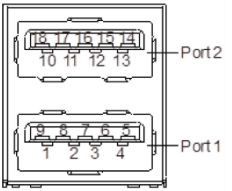
Pin	Pin Name	Signal Type	Signal level
6	LAN2_MDI1-	DIFF	
7	LAN2_MDI3+	DIFF	
8	LAN2_MDI3-	DIFF	

2.4.17 LAN (RJ-45) Port 2 (CN20)



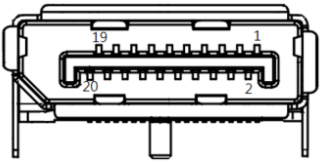
Pin	Pin Name	Signal Type	Signal level
1	LAN1_MDI0+	DIFF	
2	LAN1_MDI0-	DIFF	
3	LAN1_MDI1+	DIFF	
4	LAN1_MDI2+	DIFF	
5	LAN1_MDI2-	DIFF	
6	LAN1_MDI1-	DIFF	
7	LAN1_MDI3+	DIFF	
8	LAN1_MDI3-	DIFF	

2.4.18 USB 3.2 Gen 2 Port 1/ Port 2 (Dual Port) (CN21)



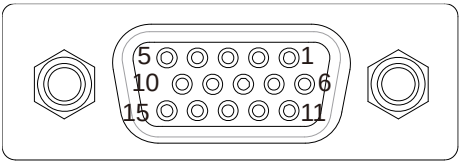
Pin	Pin Name	Signal Type	Signal Level
1	+V5A_USB_1	PWR	+5V
2	USBD2-	DIFF	
3	USBD2+	DIFF	
4	GND	GND	
5	USB3_RX2_CON_N	DIFF	
6	USB3_RX2_CON_P	DIFF	
7	GND	GND	
8	USB3_TX2_CON_N	DIFF	
9	USB3_TX2_CON_P	DIFF	
10	+V5A_USB_0	PWR	+5V
11	USBD1-	DIFF	
12	USBD1+	DIFF	
13	GND	GND	
14	USB3_RX1_CON_N	DIFF	
15	USB3_RX1_CON_P	DIFF	
16	GND	GND	
17	USB3_TX1_CON_N	DIFF	
18	USB3_TX1_CON_P	DIFF	

2.4.19 DP++ Port (CN22)



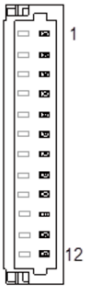
Pin	Pin Name	Signal Type	Signal Level
1	DDI1_TX0_DP	DIFF	
2	GND	GND	
3	DDI1_TX0_DN	DIFF	
4	DDI1_TX1_DP	DIFF	
5	GND	GND	
6	DDI1_TX1_DN	DIFF	
7	DDI1_TX2_DP	DIFF	
8	GND	GND	
9	DDI1_TX2_DN	DIFF	
10	DDI1_TX3_DP	DIFF	
11	GND	GND	
12	DDI1_TX3_DN	DIFF	
13	DDI1_AUX_EN	IO	
14	GND	GND	
15	DDI1_DP_CTRLCLK_AUX_DP	DIFF	
16	GND	GND	
17	DDI1_DP_CTRLDATA_AUX_DN	DIFF	
18	DDI1_DP_HPD	DDI1_DP_HPD	
19	GND	GND	
20	+V3P3S	PWR	

2.4.20 VGA Port (CN23)



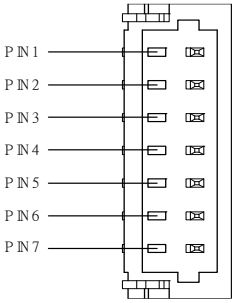
Pin	Pin Name	Signal Type	Signal Level
1	VGA_RED_CON	OUT	
2	VGA_GREEN_CON	OUT	
3	VGA_BLUE_CON	OUT	
4	NC		
5	GND	GND	
6	RED_GND_RTN	GND	
7	GREEN_GND_RTN	GND	
8	BLUE_GND_RTN	GND	
9	+5V	PWR	+5V
10	NC		
11	NC		
12	VGA_DDCDAT_CON	I/O	+5V
13	VGA_HSYNC_CON	OUT	
14	VGA_VSYNC_CON	OUT	
15	VGA_DDCCLK_CON	I/O	+5V

2.4.21 LPC Port (CN24)



Pin	Pin Name	Signal Type	Signal Level
1	LPC_AD0	I/O	
2	LPC_AD1	I/O	
3	LPC_AD2	I/O	
4	LPC_AD3	I/O	
5	+V3P3S	PWR	+3.3V
6	LPC_FRAME#	IN	
7	BUF_PLT_RST#	OUT	
8	GND	GND	
9	CLK_LPCC_25M	OUT	
10	I2C0_SDA	I/O	
11	I2C0_SCL	OUT	
12	INT_SERIRQ	GND	

2.4.22 BIOS Debug Port (CN25)



Pin	Pin Name	Signal Type	Signal Level
1	SPI_SO_F	OUT	
2	GND	GND	
3	SPI_CLK_F	IN	
4	+V3P3A_SPI	PWR	+3.3V
5	SPI_SI_F	IN	
6	SPI_CE0#_F	IN	
7	NC		

2.4.23 M.2 M-Key 2280 (CN26)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	+V3P3S	PWR	+3.3V
3	GND	GND	
4	+V3P3S	PWR	+3.3V
5	PCIE_8_RXN	DIFF	
6	CARD_PWR_OFF_R	IN	
7	PCIE_8_RXP	DIFF	

Pin	Pin Name	Signal Type	Signal Level
8	N.C		
9	GND	GND	
10	SSD_LED#	OUT	
11	PCIE_8_TXN_C	DIFF	
12	+V3P3S	PWR	+3.3V
13	PCIE_8_TXP_C	DIFF	
14	+V3P3S	PWR	+3.3V
15	GND	GND	
16	+V3P3S	PWR	+3.3V
17	PCIE_7_RXN	DIFF	
18	+V3P3S	PWR	+3.3V
19	PCIE_7_RXP	DIFF	
20	N.C		
21	GND	GND	
22	N.C		
23	PCIE_7_TXN_C	DIFF	
24	N.C		
25	PCIE_7_TXP_C	GND	
26	N.C		
27	GND	GND	
28	N.C		
29	PCIE_6_RXN	DIFF	
30	N.C		
31	PCIE_6_RXP	DIFF	
32	N.C		
33	GND	GND	

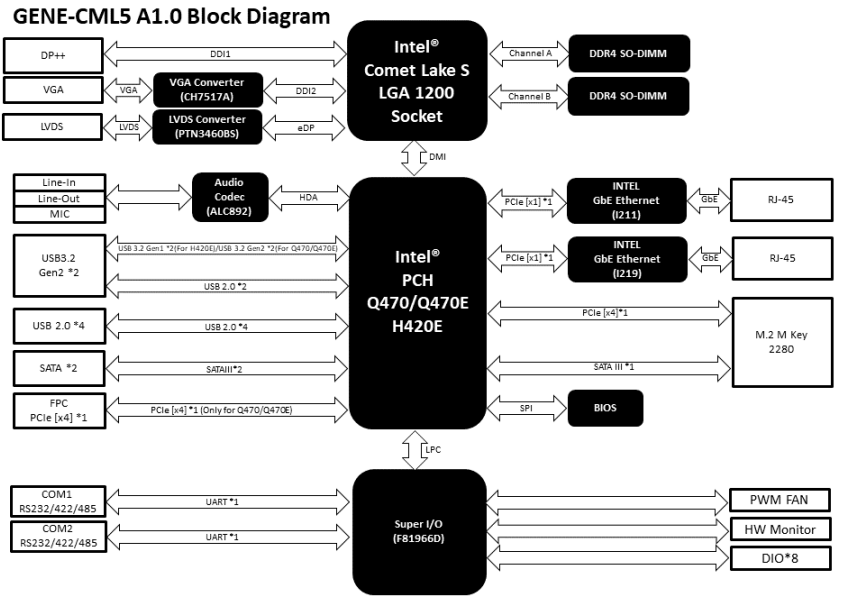
Pin	Pin Name	Signal Type	Signal Level
34	N.C		
35	PCIE_6_TXN_C	DIFF	
36	N.C		
37	PCIE_6_TXP_C	DIFF	
38	SATA_DEVSLP0	IN	
39	GND	GND	
40	SMB_CLK_KMB	IN	
41	M2M_A_RXP	DIFF	
42	N.C		
43	M2M_A_RXN	DIFF	
44	N.C		
45	GND	GND	
46	N.C		
47	M2M_A_TXN_C	DIFF	
48	N.C		
49	M2M_A_TXP_C	DIFF	
50	BUF_PLT_RST#	IN	
51	GND	GND	
52	M2M_CLKREQ#	IN	
53	CLK_PCIE_M2M_N_R		
54	PCIE_WAKE#	IN	
55	CLK_PCIE_M2M_P_R		
56	N.C		
57	GND	GND	
58	N.C		
67	N.C		

Pin	Pin Name	Signal Type	Signal Level
68	SUS_CLK_M2M	IN	
69	PEDET_R	OUT	
70	+V3P3S	PWR	+3.3V
71	GND	GND	
72	+V3P3S	PWR	+3.3V
73	GND	GND	
74	+V3P3S	PWR	+3.3V
75	GND	GND	

2.4.24 DDR4 SO-DIMM Slot (DIMM1/ DIMM2)

Standard Specifications

2.5 Block Diagram



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The GENE-CML5 board uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the module will output a few short beeps or display an error message. The module can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the module will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integral lithium battery backup for data retention. You will need to replace the battery unit when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <ESC> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access hardware monitor and advanced board features, options

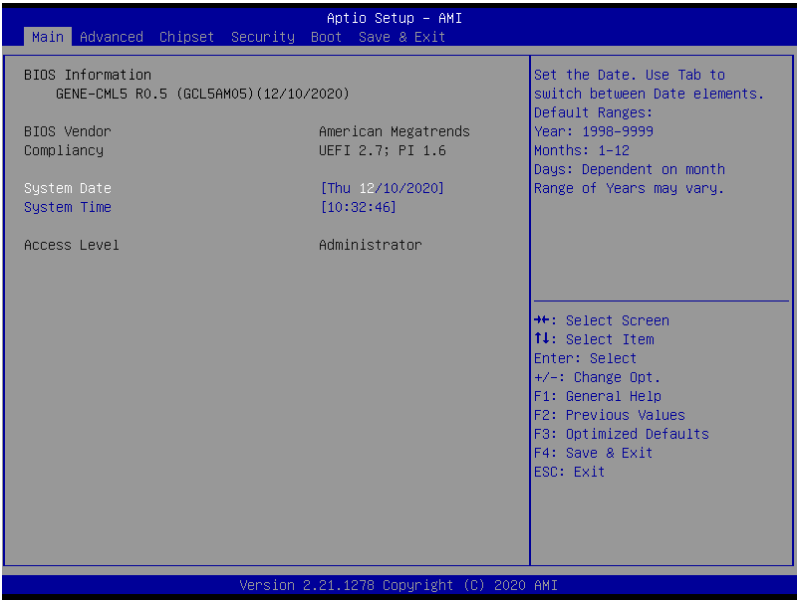
Chipset – Host bridge parameters

Security – The setup administrator password can be set here

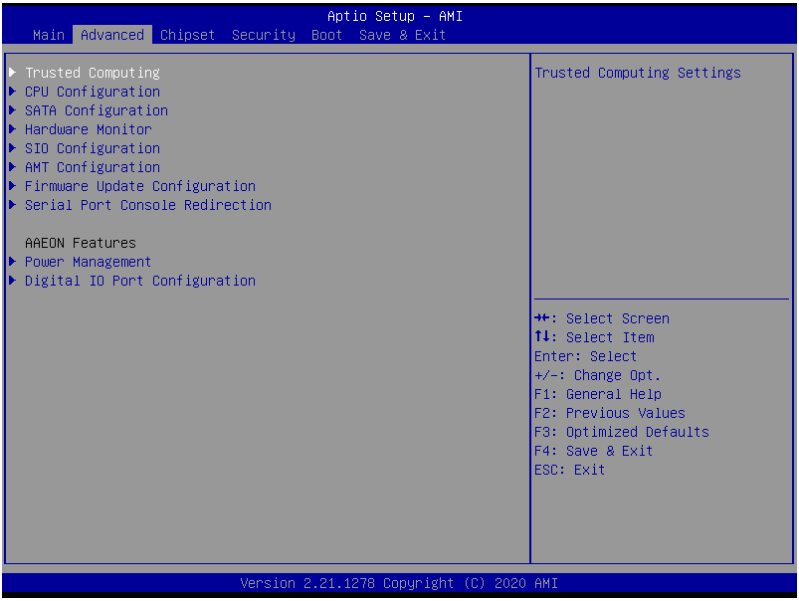
Boot – Enable/ Disable Quiet Boot option

Save & Exit –Save your changes and exit the program

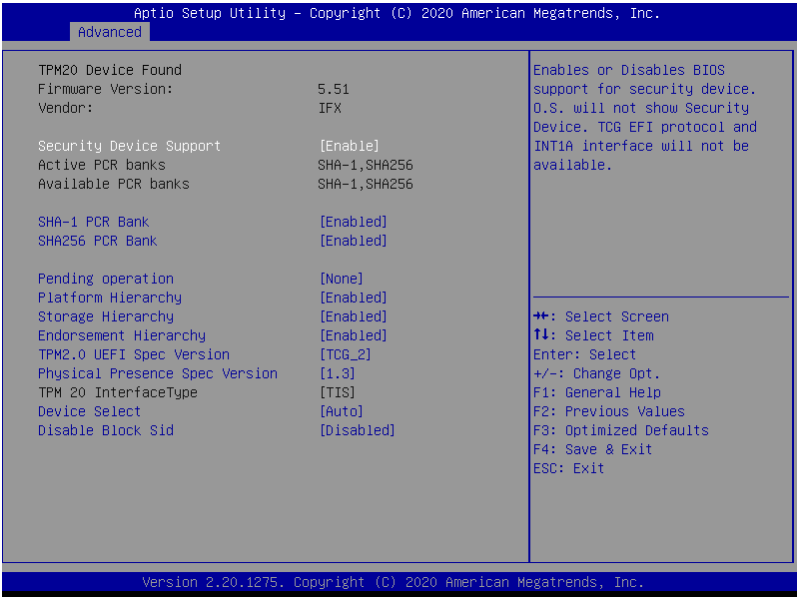
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



3.4.1 Trusted Computing

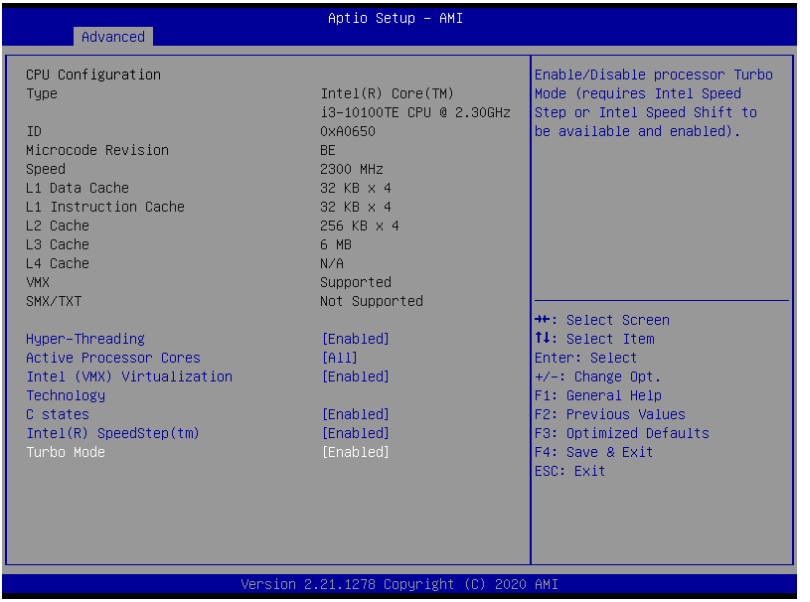


Options Summary		
Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Table Continues on next Page

Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

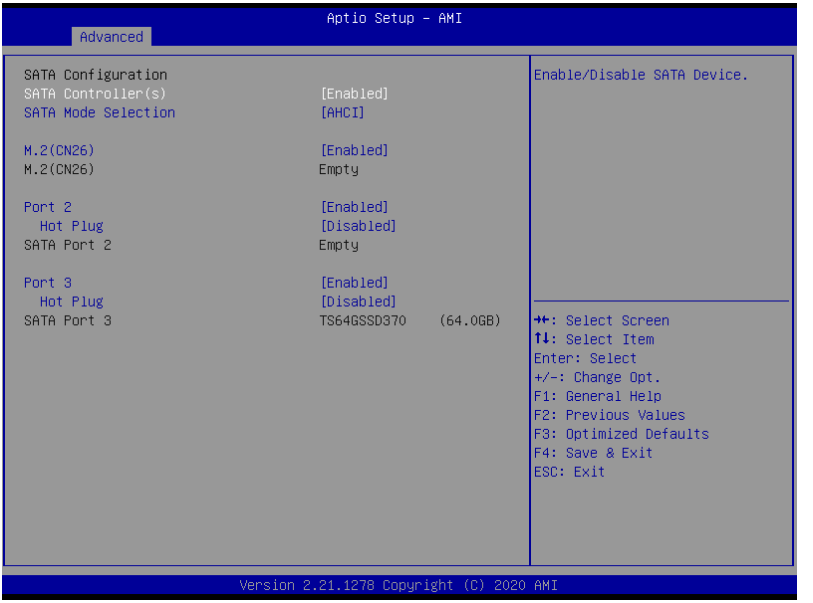
3.4.2 CPU Configuration



Options Summary		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disabled Hyper-Threading Technology		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		

Options Summary		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).		

3.4.3 SATA Configuration

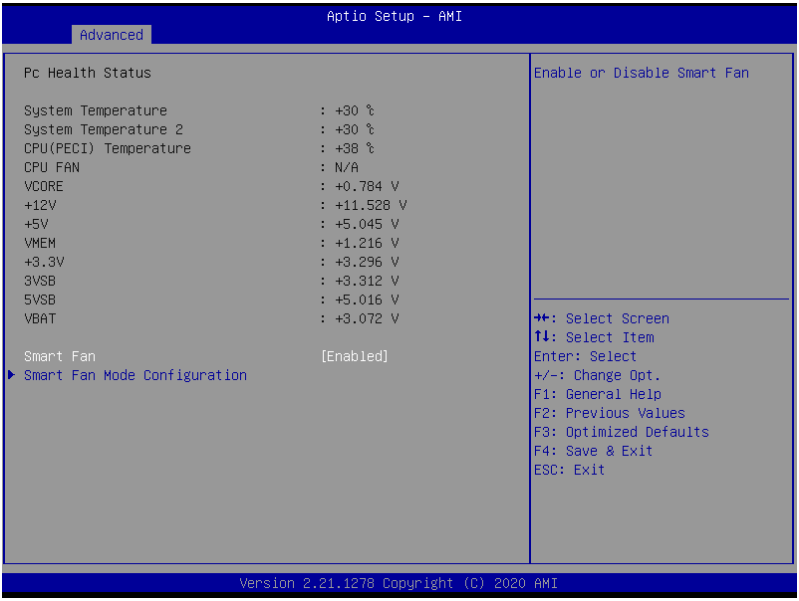


Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
SATA Mode Selection	AHCI	Optimal Default, Failsafe Default
	Intel RST Premium With Intel Optane System Acceleration	
Determines how SATA controller(s) operate		
M.2(CN26)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Port 2	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		

Table Continues on Next Page...

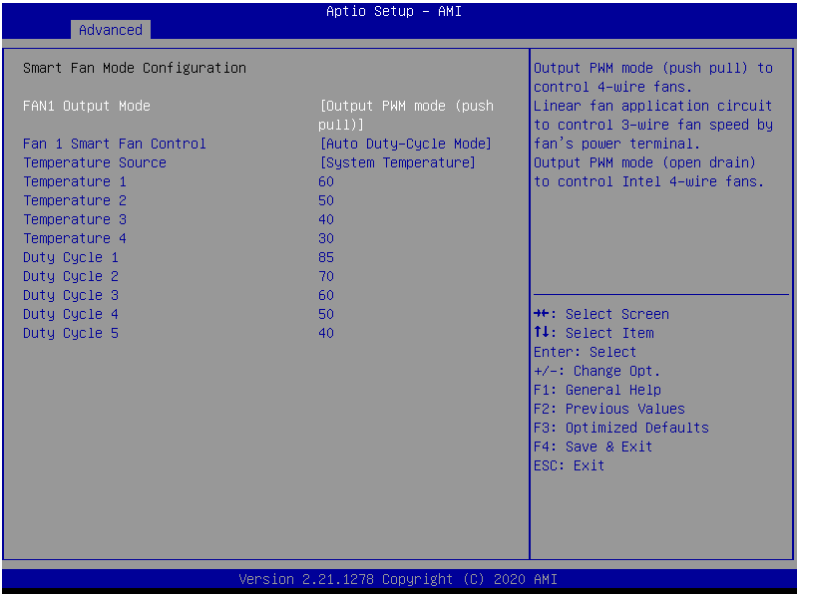
Options Summary		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable		
Port 3	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable		

3.4.4 Hardware Monitor



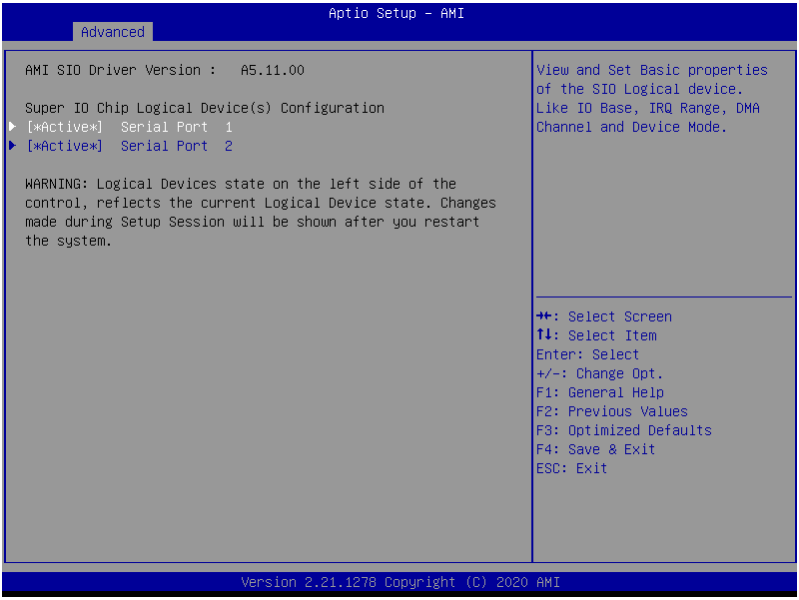
Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Smart Fan.		

3.4.4.1 Smart Fan Mode Configuration

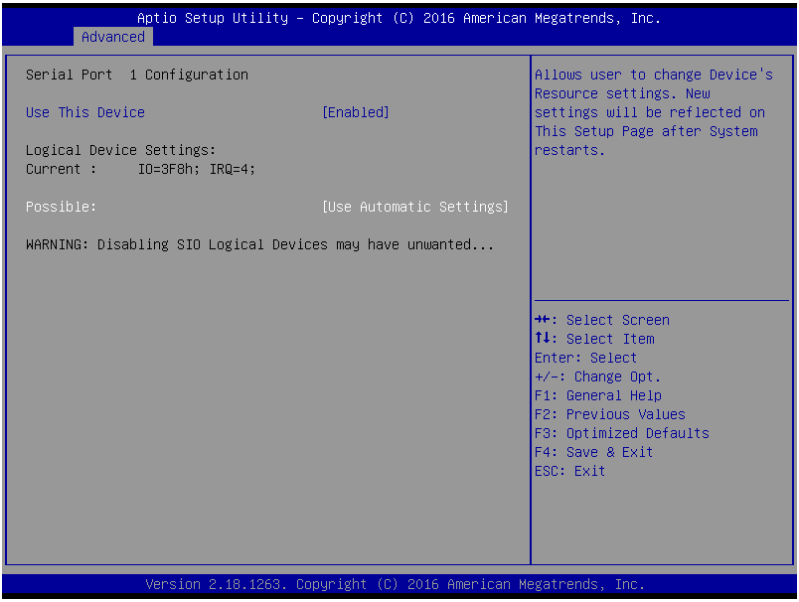


Options Summary		
FAN1 Output Mode	Output PWM mode (open drain)	
	Linear Fan Application	
	Output PWM mode (push pull)	Optimal Default, Failsafe Default
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU(PECI) Temperature	
	System Temperature	Optimal Default, Failsafe Default
	System Temperature 2	
Select the monitored temperature source for this fan.		
Temperature 1	60	
Duty Cycle 1	85	
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		

3.4.5 SIO Configuration

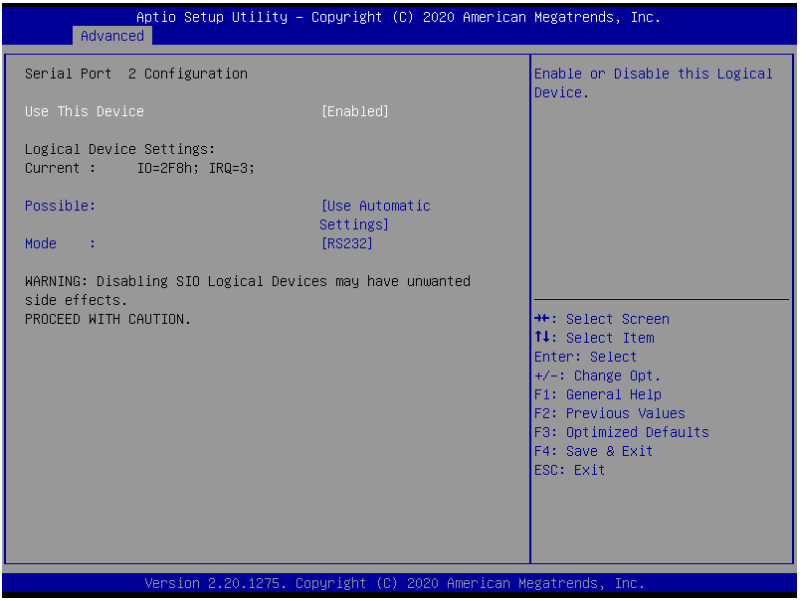


3.4.5.1 Serial Port 1 Configuration



Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.5.2 Serial Port 2 Configuration

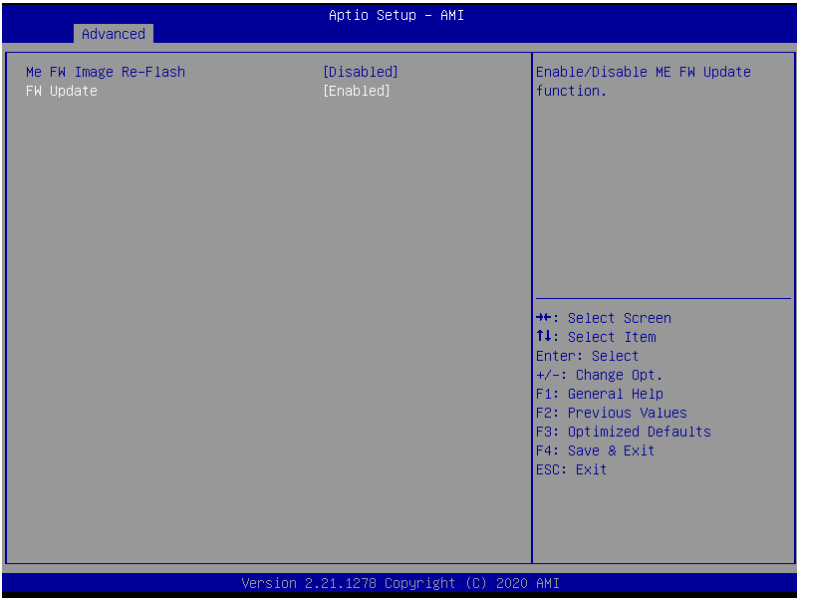


Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.6 AMT Configuration

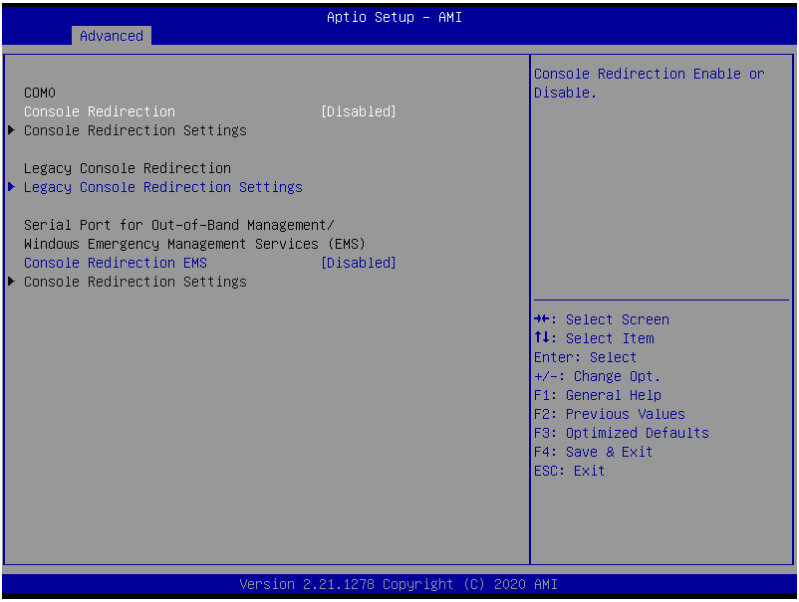
Options Summary		
AMT BIOS Features	Disable	
	Enable	Optimal Default, Failsafe Default
When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW		

3.4.7 Firmware Update Configuration



Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.8 Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.4.8.1 COM0 Console Redirection Settings

Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits Per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Parity	None	Optimal Default, Failsafe Default

Options Summary		
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.4.8.2 Legacy Console Redirection Settings

Options Summary		
Redirection Console COM Port	COM0	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection		
Redirect After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.		

3.4.8.3 Out-of-Band Mgmt Console Redirection Settings

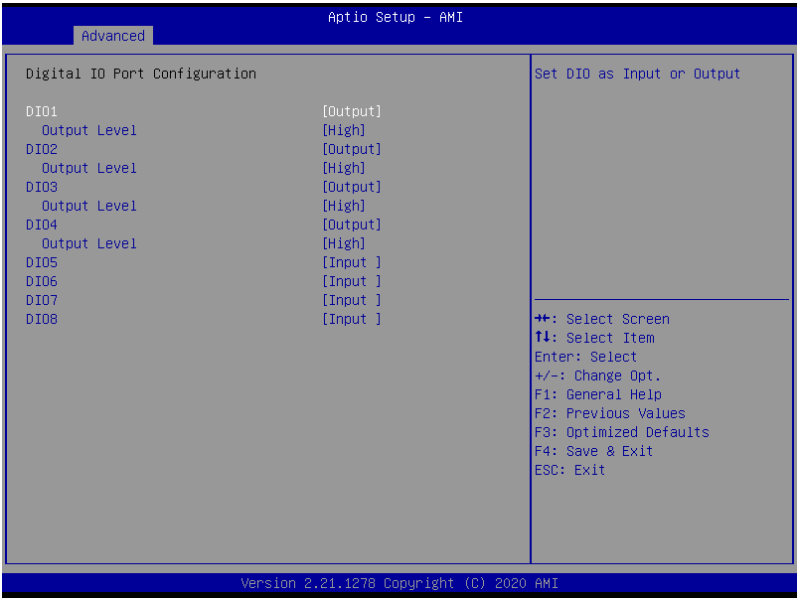
Options Summary		
Terminal Type EMS	VT100	
	VT100+	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits Per second EMS	9600	
	19200	
	57600	
	115200	Optimal Default, Failsafe Default
Flow Control EMS	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software xon/xoff	
Continued on Next Page…		

Options Summary
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.

3.4.9 Power Management

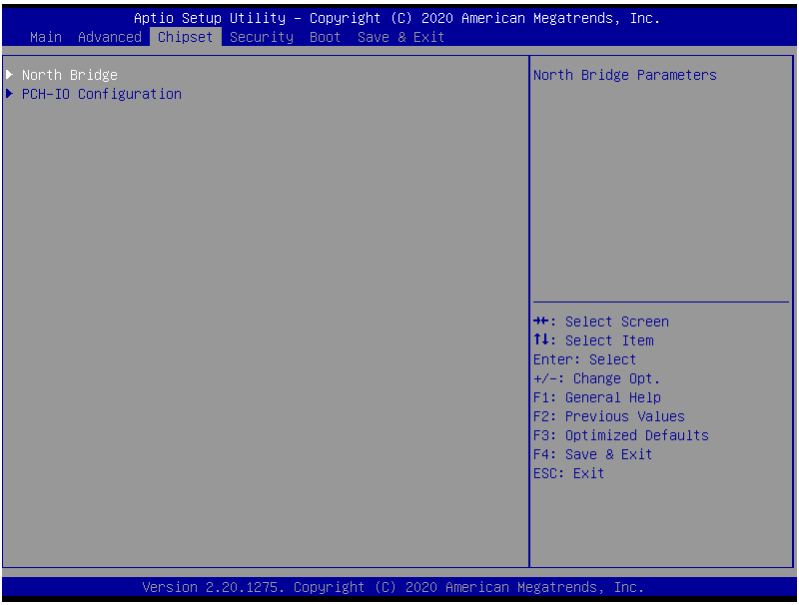
Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
State After G3	Always On	
	Always Off	
	Last State	Optimal Default, Failsafe Default
Specify what state to go to when power is re-applied after a power failure (G3 state).		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)		

3.4.10 Digital IO Port Configuration

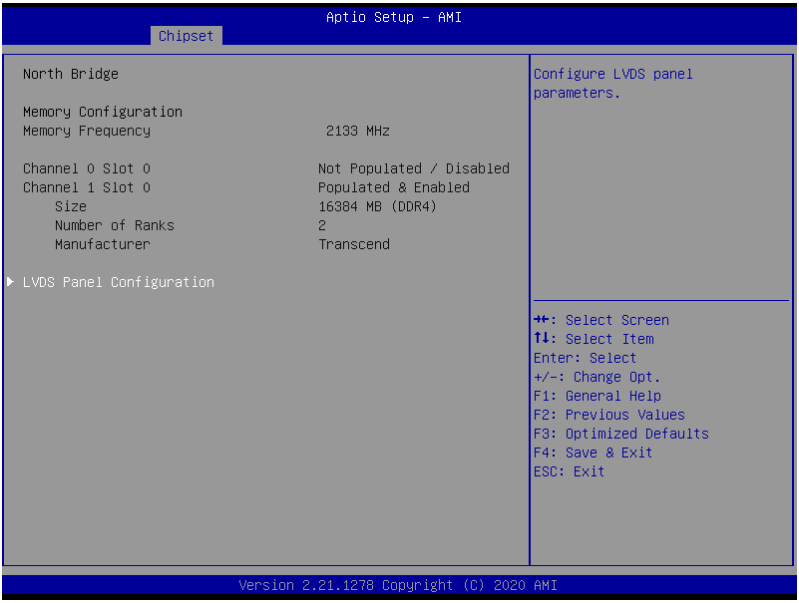


Options Summary		
DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.5 Setup Submenu: Chipset



3.5.1 North Bridge

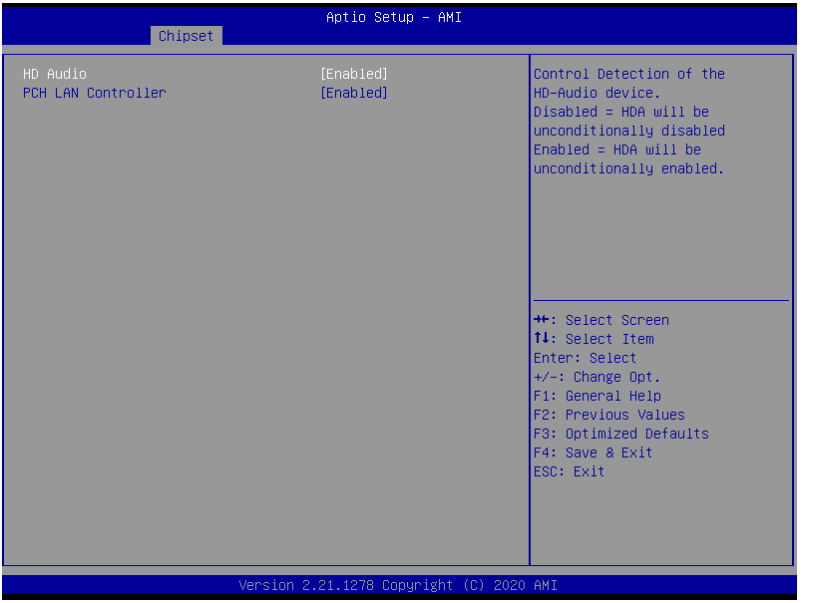


3.5.1.1 LVDS Panel Configuration

Options Summary		
LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled this panel.		
LVDS Panel Type	640x480,18bit,60Hz	
	800x480,18bit,60Hz	
	800x600,18bit,60Hz	
	1024x600,18bit,60Hz	
	1024x768,18bit,60Hz	
	1024x768,24bit,60Hz	Optimal Default, Failsafe Default
	1280x768,24bit,60Hz	
	1280x1024,48bit,60Hz	
	1366x768,24bit,60Hz	
	1440x900,48bit,60Hz	
	1600x1200,48bit,60Hz	
	1920x1080,48bit,60Hz	
	1920x1200,48bit,60Hz	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		

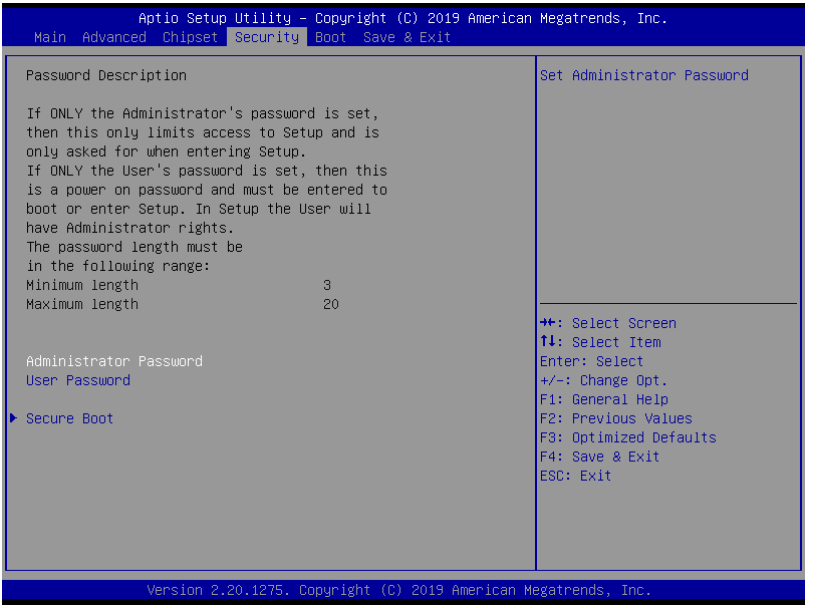
Options Summary		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.5.2 PCH IO Configuration



Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		
PCH Lan Controller	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable onboard NIC		

3.6 Setup Submenu: Security



Change User/Administrator Password

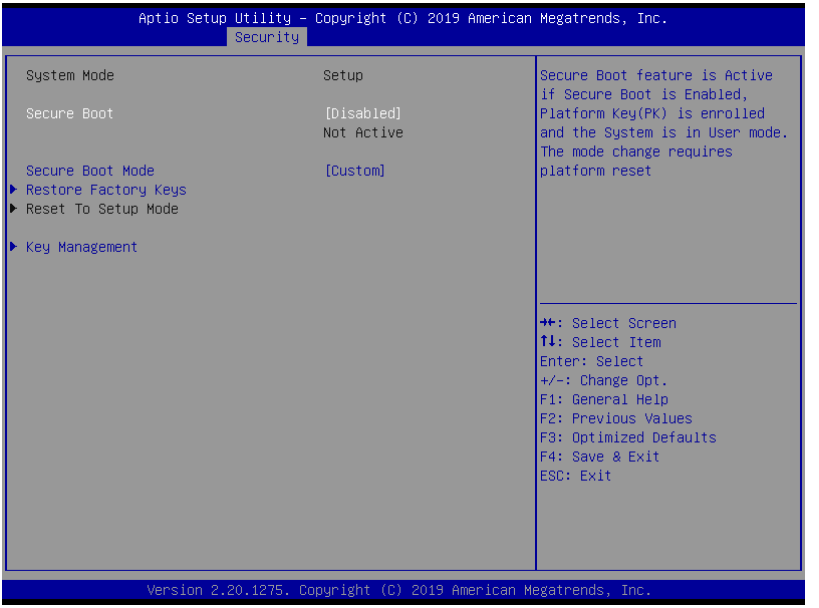
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

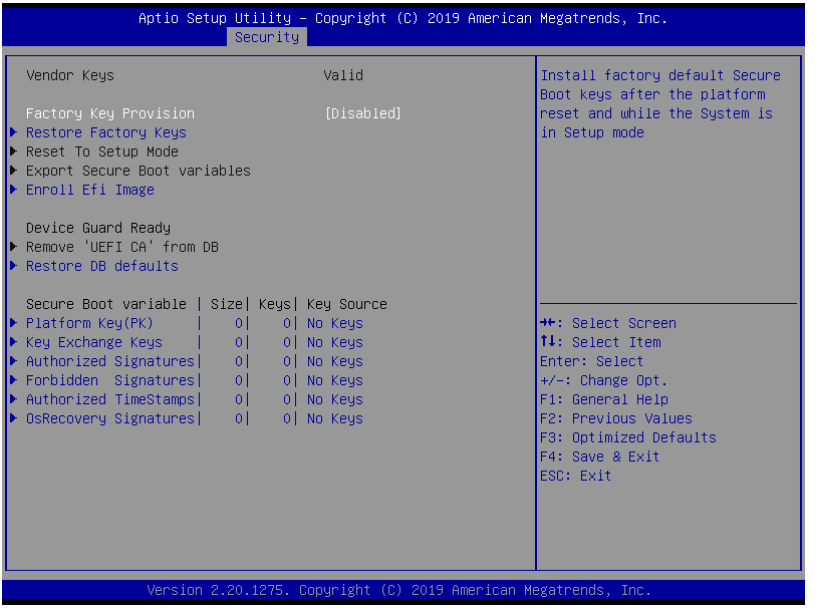
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		

3.6.1.1 Key Management

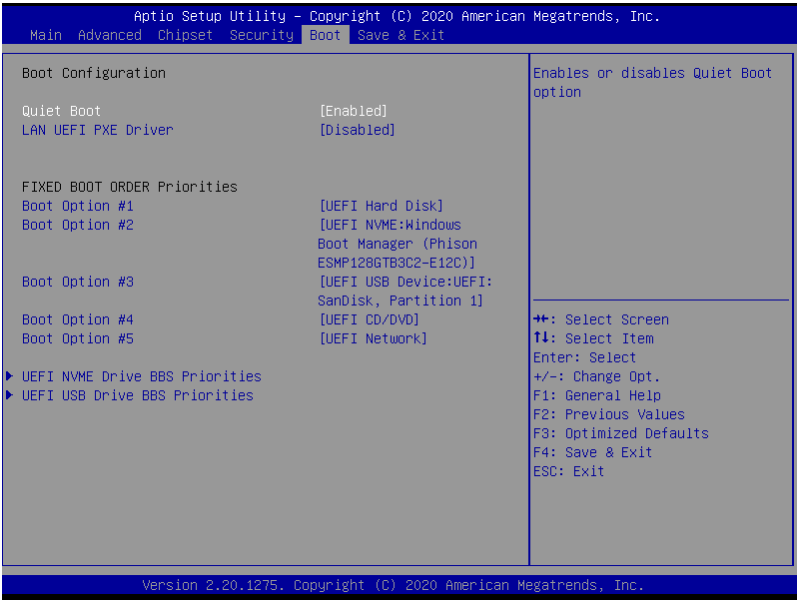


Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

Table Continues on Next Page…

Options Summary		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults		
Restore DB variable to factory defaults		
Platform Key (PK)	Details	
	Export	
	Update	
	Delete	
Key Exchange Keys	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Forbidden Signatures	Details	
	Export	
	Update	
	Append	
	Delete	
Authorized TimeStamps	Update	
	Append	
OsRecovery Signatures	Update	
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

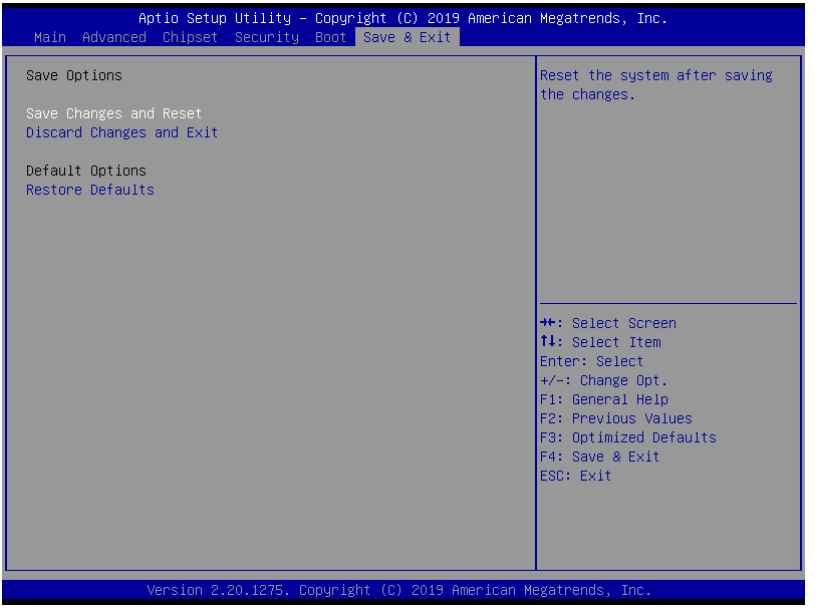
3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable showing boot logo.		
LAN UEFI Pxe Driver	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled/Disable LAN UEFI PXE Driver		

3.7.1 BBS Priorities

3.8 Setup Submenu: Save & Exit



Chapter 4

Driver Installation

4.1 Driver Download/Installation

Drivers for the GENE-CML5 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/subcompact-boards-gene-cml5

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 – Chipset** folder
2. Run the **SetupChipset.exe** in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step 2 – Graphic** folder
2. Run the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install Network Driver

1. Open the **Step 3 – Network** folder
2. Run the **PROWinx64.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **Step 4 – Audio** folder
2. Run the **Win10_R281.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Serial IO Drivers

1. Open the **Step 5 – SerialIO** folder
2. Run the **SetupSerialIO.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

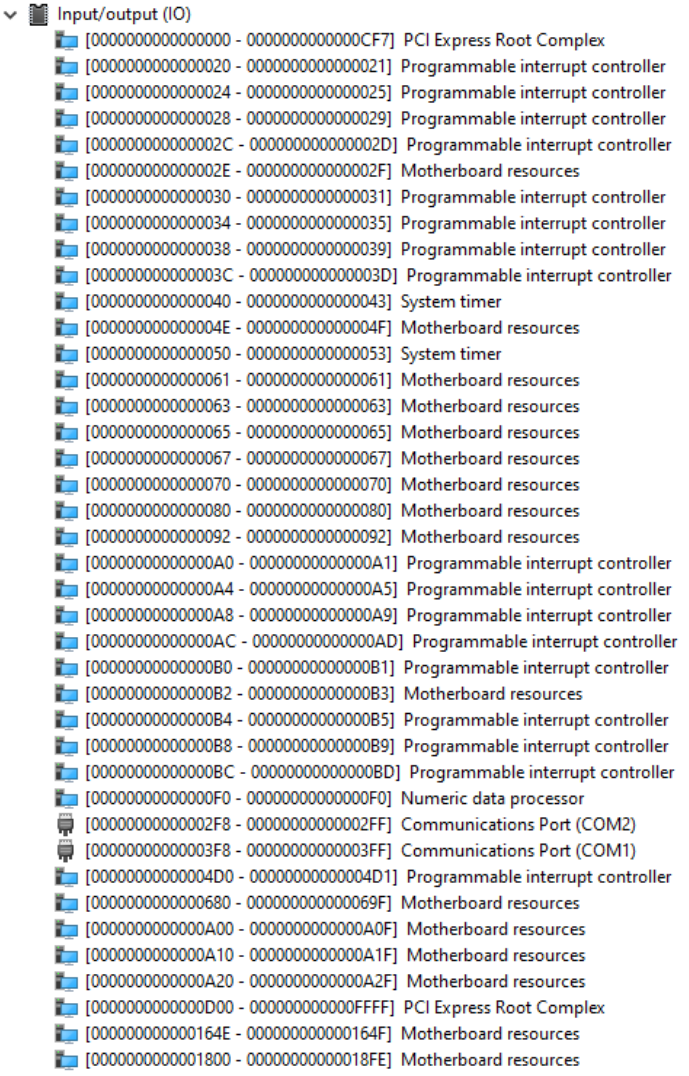
Step 6 – Install ME Drivers

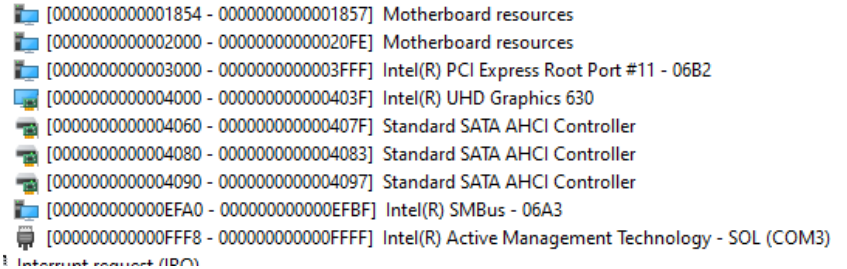
1. Click on the **Step 6 – ME** folder
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

I/O Information

A.1 I/O Address Map

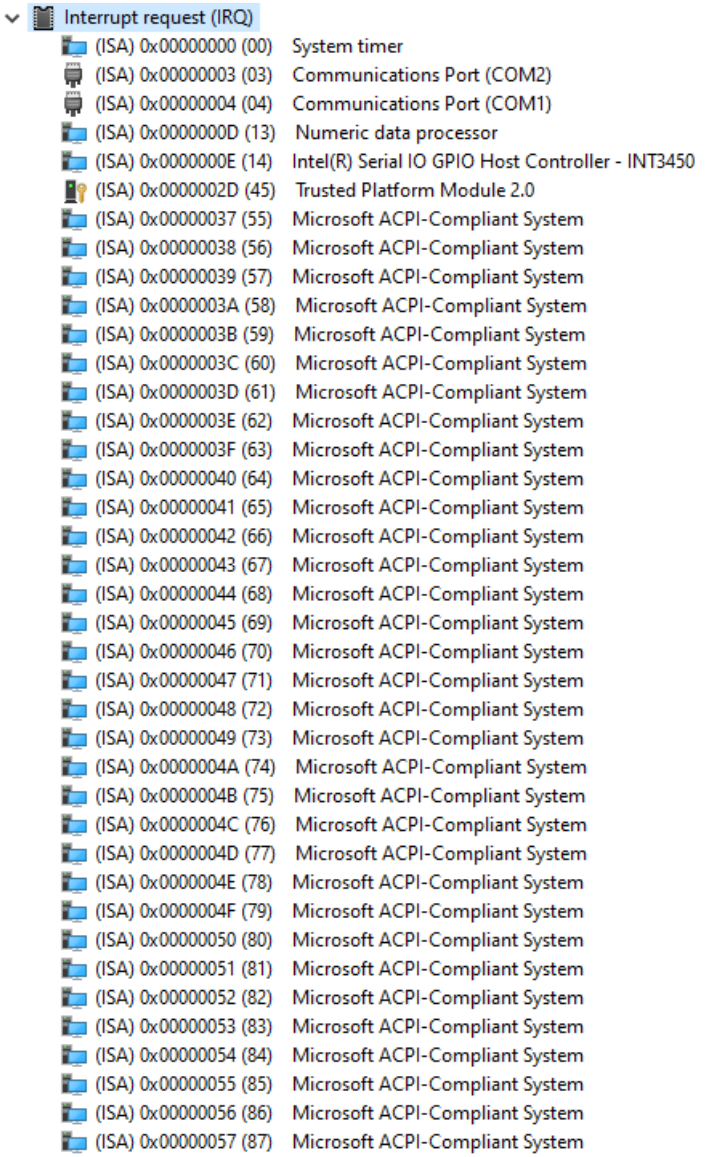


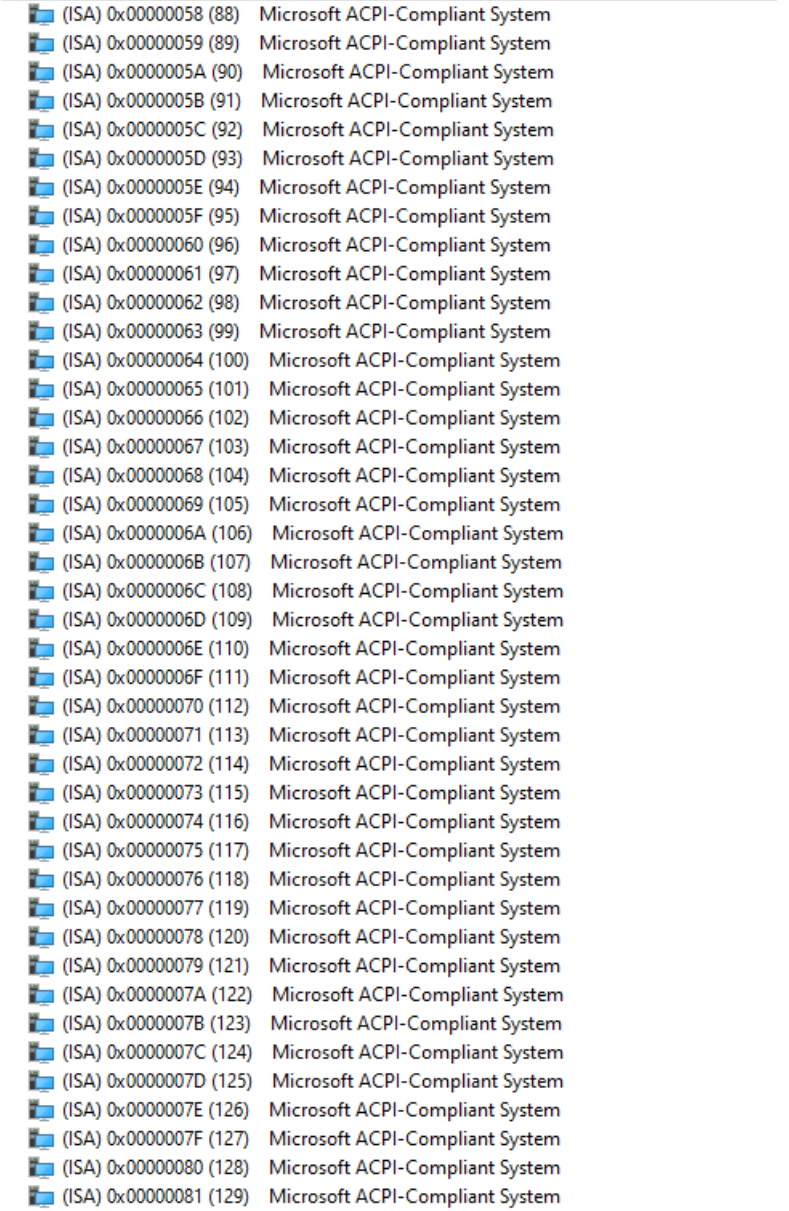

[0000000000001854 - 0000000000001857] Motherboard resources
[0000000000002000 - 00000000000020FE] Motherboard resources
[0000000000003000 - 0000000000003FFF] Intel(R) PCI Express Root Port #11 - 06B2
[0000000000004000 - 000000000000403F] Intel(R) UHD Graphics 630
[0000000000004060 - 000000000000407F] Standard SATA AHCI Controller
[0000000000004080 - 0000000000004083] Standard SATA AHCI Controller
[0000000000004090 - 0000000000004097] Standard SATA AHCI Controller
[000000000000EFA0 - 000000000000EFBF] Intel(R) SMBus - 06A3
[000000000000FFF8 - 000000000000FFFF] Intel(R) Active Management Technology - SOL (COM3)

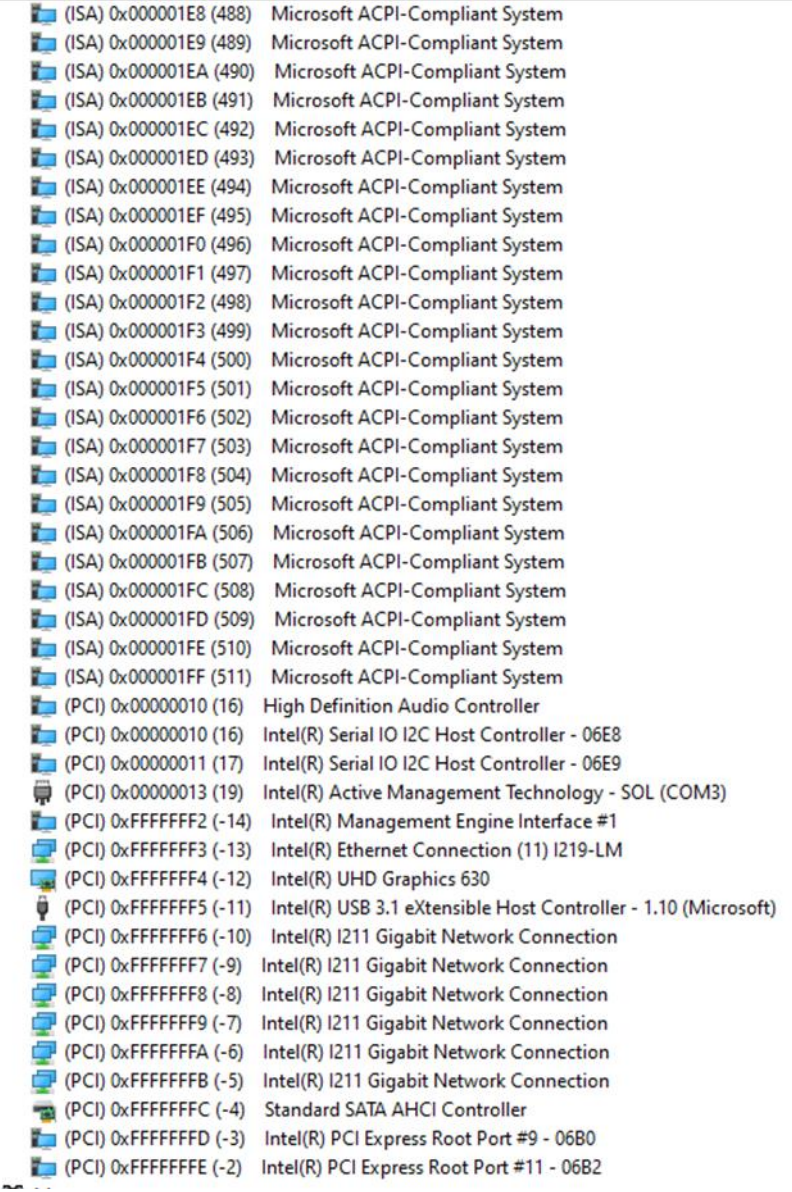
A.2 Memory Address Map

- Memory
  - [00000000000A0000 - 00000000000BFFFF] PCI Express Root Complex
  - [000000009F800000 - 00000000DFFFFFFF] PCI Express Root Complex
  - [00000000A0000000 - 00000000AFFFFFFF] Intel(R) UHD Graphics 630
  - [00000000B0000000 - 00000000B0FFFFFF] Intel(R) UHD Graphics 630
  - [00000000B1100000 - 00000000B111FFFF] Intel(R) I211 Gigabit Network Connection
  - [00000000B1100000 - 00000000B11FFFFF] Intel(R) PCI Express Root Port #11 - 06B2
  - [00000000B1120000 - 00000000B1123FFF] Intel(R) I211 Gigabit Network Connection
  - [00000000B1220000 - 00000000B122FFFF] Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
  - [00000000B1234000 - 00000000B1235FFF] Standard SATA AHCI Controller
  - [00000000B1238000 - 00000000B12380FF] Intel(R) SMBus - 06A3
  - [00000000B1239000 - 00000000B12397FF] Standard SATA AHCI Controller
  - [00000000B123A000 - 00000000B123A0FF] Standard SATA AHCI Controller
  - [00000000E0000000 - 00000000EFFFFFFF] Motherboard resources
  - [00000000FC800000 - 00000000FE7FFFFF] PCI Express Root Complex
  - [00000000FCF00000 - 00000000FCFFFFFF] High Definition Audio Controller
  - [00000000FD000000 - 00000000FD69FFFF] Motherboard resources
  - [00000000FD6A0000 - 00000000FD6AFFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
  - [00000000FD6B0000 - 00000000FD6BFFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
  - [00000000FD6C0000 - 00000000FD6CFFFF] Motherboard resources
  - [00000000FD6D0000 - 00000000FD6DFFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
  - [00000000FD6E0000 - 00000000FD6EFFFF] Intel(R) Serial IO GPIO Host Controller - INT3450
  - [00000000FD6F0000 - 00000000FDFFFFFF] Motherboard resources
  - [00000000FE000000 - 00000000FE01FFFF] Motherboard resources
  - [00000000FE010000 - 00000000FE010FFF] Intel(R) SPI (flash) Controller - 06A4
  - [00000000FE038000 - 00000000FE038FFF] Motherboard resources
  - [00000000FE1D8000 - 00000000FE1DBFFF] High Definition Audio Controller
  - [00000000FE1DC000 - 00000000FE1DCFFF] Intel(R) Management Engine Interface #1
  - [00000000FE1DD000 - 00000000FE1DDFFF] Intel(R) Serial IO I2C Host Controller - 06E9
  - [00000000FE1DE000 - 00000000FE1DEFFF] Intel(R) Serial IO I2C Host Controller - 06E8
  - [00000000FE1DF000 - 00000000FE1DFFFF] Intel(R) Active Management Technology - SOL (COM3)
  - [00000000FE1E0000 - 00000000FE1FFFFF] Intel(R) Ethernet Connection (11) I219-LM
  - [00000000FE200000 - 00000000FE7FFFFF] Motherboard resources
  - [00000000FED00000 - 00000000FED003FF] High precision event timer
  - [00000000FED10000 - 00000000FED17FFF] Motherboard resources
  - [00000000FED18000 - 00000000FED18FFF] Motherboard resources
  - [00000000FED19000 - 00000000FED19FFF] Motherboard resources
  - [00000000FED20000 - 00000000FED3FFFF] Motherboard resources
  - [00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
  - [00000000FED45000 - 00000000FED8FFFF] Motherboard resources
  - [00000000FED90000 - 00000000FED93FFF] Motherboard resources
  - [00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources

A.3 IRQ Mapping Chart




(ISA) 0x00000058 (88) Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89) Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90) Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91) Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103) Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System


(ISA) 0x000001E8 (488) Microsoft ACPI-Compliant System
(ISA) 0x000001E9 (489) Microsoft ACPI-Compliant System
(ISA) 0x000001EA (490) Microsoft ACPI-Compliant System
(ISA) 0x000001EB (491) Microsoft ACPI-Compliant System
(ISA) 0x000001EC (492) Microsoft ACPI-Compliant System
(ISA) 0x000001ED (493) Microsoft ACPI-Compliant System
(ISA) 0x000001EE (494) Microsoft ACPI-Compliant System
(ISA) 0x000001EF (495) Microsoft ACPI-Compliant System
(ISA) 0x000001F0 (496) Microsoft ACPI-Compliant System
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0x00000010 (16) Intel(R) Serial IO I2C Host Controller - 06E8
(PCI) 0x00000011 (17) Intel(R) Serial IO I2C Host Controller - 06E9
(PCI) 0x00000013 (19) Intel(R) Active Management Technology - SOL (COM3)
(PCI) 0xFFFFFFF2 (-14) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFF3 (-13) Intel(R) Ethernet Connection (11) I219-LM
(PCI) 0xFFFFFFF4 (-12) Intel(R) UHD Graphics 630
(PCI) 0xFFFFFFF5 (-11) Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
(PCI) 0xFFFFFFF6 (-10) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF7 (-9) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF8 (-8) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFF9 (-7) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFFA (-6) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFFB (-5) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFFC (-4) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFD (-3) Intel(R) PCI Express Root Port #9 - 06B0
(PCI) 0xFFFFFFFE (-2) Intel(R) PCI Express Root Port #11 - 06B2

Appendix B

Mating Connectors and Cables

B.1 Mating Connectors and Cables

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	COM Port Connector	PINREX	710-H73-095 WE1	Serial Port Cable	1701090122
CN2	COM Port Connector	PINREX	710-H73-095 WE1	Serial Port Cable	1701090122
CN3	ATX Connector	PINREX	753-71-03TW 01	ATX Cable	170220020B
CN6	Audio Connector	PINREX	712-71-10TW 01	Audio Cable	1709100254
CN8	SATA Connector	TechBest	007-01-00757	SATA Cable	1709070460
CN9	SATA Connector	TechBest	007-01-00757	SATA Cable	1709070460
CN10	SATA Power Connector	PINREX	721-81-02TW 00	SATA Power Cable	1702150155
CN12	USB2.0 Connector	Aces	50238-01041-003	USB2.0 Cable	170010010D
CN13	USB2.0 Connector	Aces	50238-01041-003	USB2.0 Cable	170010010D
CN14	FPC Connector	Panasonic	AYF534035	FPC Cable	1706400601
CN16	Front Panel Connector	Aces	50238-01041-001	Front Panel cable	1709100108
CN17	LVDS Connector	CATCH	1204-710-30SMP	LVDS Cable	1704300311
CN18	Inverter Connector	Aces	50228-00671-001	Inverter Cable	170X000152

Appendix C

Digital I/O Ports

C.1 Digital I/O Register

7.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

GPIO8 Output Enable Register — Index 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	LRESET#	0	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	LRESET#	0	0: GPIO86 is in input mode. 1: GPIO85 is in output mode.
5	GPIO85_OE	R/W	LRESET#	0	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	LRESET#	0	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	LRESET#	0	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	LRESET#	0	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.
1	GPIO81_OE	R/W	LRESET#	0	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	LRESET#	0	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

GPIO8 Output Data Register — Index 89h (This byte could be also written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_VAL	R/W	LRESET#	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_VAL	R/W	LRESET#	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_VAL	R/W	LRESET#	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_VAL	R/W	LRESET#	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.
3	GPIO83_VAL	R/W	LRESET#	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_VAL	R/W	LRESET#	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_VAL	R/W	LRESET#	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_VAL	R/W	LRESET#	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

GPIO8 Pin Status Register — Index 8Ah (This byte could be also read by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_IN	R	-	-	The pin status of GPIO87/PD7.
6	GPIO86_IN	R	-	-	The pin status of GPIO86/PD6.
5	GPIO85_IN	R	-	-	The pin status of GPIO85/PD5.
4	GPIO84_IN	R	-	-	The pin status of GPIO84/PD4.
3	GPIO83_IN	R	-	-	The pin status of GPIO83/PD3.
2	GPIO82_IN	R	-	-	The pin status of GPIO82/PD2.
1	GPIO81_IN	R	-	-	The pin status of GPIO81/PD1.
0	GPIO80_IN	R	-	-	The pin status of GPIO80/PD0.

C.2 Digital I/O Sample Code (4 in 4 out, 2 low 2 high)

```
Outportb(0x2E,0x87); //enter configuration Outportb(0x2E,0x87);
Outportb(0x2E,0x07); //set LDN
Outportb(0x2F,0x06);
Outportb(0x2E,0x88); //GPIO set 8x Output enable register
Outportb(0x2F,0xF0);
Outportb(0x2E,0x89); //GPIO 8x output data register
Outportb(0x2F,0x30);
Outportb(0x2E,0xAA); //exit configuration
```