GENE-BSW5

3.5" Subcompact Board

User's Manual 7th Ed

Last Updated: August 20, 2021

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● GENE-BSW5 MB	1
● Heatsink	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O： The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	3.5'' SubCompact Board
CPU	Intel® Celeron® N Processor: Intel® Celeron® N3160 (4C/4T, 1.60 GHz, up to 2.24 GHz)
CPU TDP	N3160: 6W
Chipset	Integrated with Intel® SoC
Memory Type	DDR3L up to 1600 MHz, SODIMM x 1
ECC Support	Non-ECC
Max. Memory Capacity	8 GB
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Security	—
RTC Battery	Lithium Battery 3V/240mAH

Power	
Power Requirement	12V Only
Power Supply Type	AT/ATX
Connector	Phoenix 2-pin Connector
Power Consumption (Typical)	1.63A at +12V with Intel® N3160, DDR3L 1600MHz 8GB memory
Power Consumption (Max)	1.95A at +12V with Intel® N3160, DDR3L 1600MHz 8GB memory

Display

Controller	Intel® HD Graphics for Intel® Celeron® N3000 Series Processor
LVDS/eDP	LVDS1 Dual Channel 18/24 bit x 1 LVDS2 Dual Channel 18/24 bit x 1 (Optional: HDMI 1.4b)
Display Interface	VGA x 1
Multiple Display Support	Up to 3 Simultaneous Displays

Audio

Codec	Realtek ALC897/892
Audio interface	Line-in/ Line-out/ Mic
Speaker	—

External I/O

Ethernet	Realtek RTL8119-CG, 10/100/1000Base-TX, RJ-45 x 2
USB	USB3.2 Gen 1 x 2
Serial Port	COM1 (RS232)
Video	VGA x 1 HDMI x 1 (optional)
Power Input	Phoenix 2-pin Connector
Other	—

Internal I/O

USB	USB2.0 x 3
Serial Port	COM2, COM 3 (RS232/422/485, supports 5V/12V/RI)
	COM4, COM5, COM6 (RS232)
Video	LVDS1 x 1
	LVDS2/HDMI x 1 (Default: LVDS2)
SATA	SATA III x 1
	+5V SATA Power Connector x 1
Audio	Audio Header x 1
DIO/GPIO	8-bit
SMBus/I2C	SMBus/I2C x 1 (Default: SMBus)
Touch	4/5/8-wire Touch Controller x 1 (optional)
Fan	3-pin DC Fan Connector x 1
SIM	—
Front Panel	HDD LED
	PWR LED
	Power Button
	Buzzer
	Reset
Other	—

Expansion

Mini PCIe/mSATA	Full-Size mPCIe x 1
	Half-Size mSATA/mPCIe x 1 (Defualt mSATA, BOM option: mPCIe)
M.2	—
BIO	—

Expansion

Other	—

Mechanical

Dimensions (L x W)	5.75" x 4" (146mm x 101.7mm)

Environment

Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	325,391

Certification

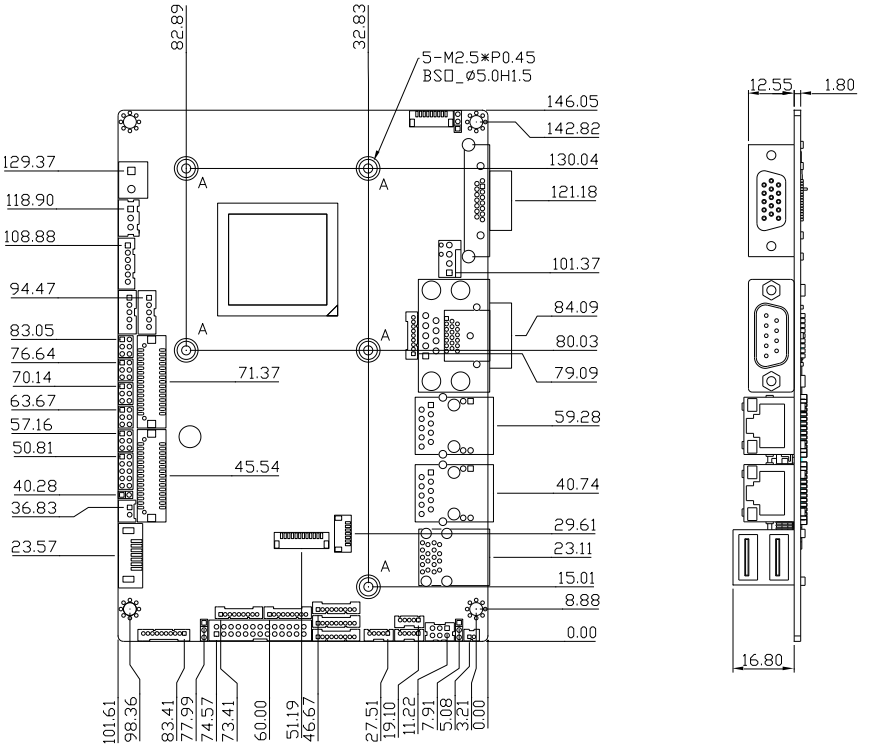
EMC	CE/FCC

Chapter 2

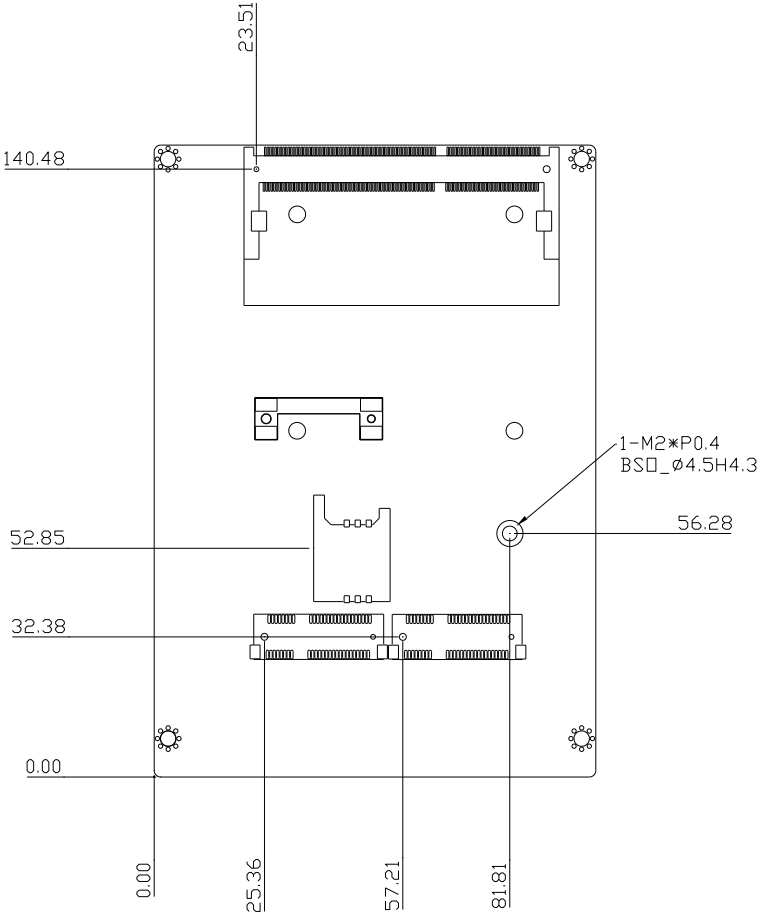
Hardware Information

2.1 Dimensions

Component Side

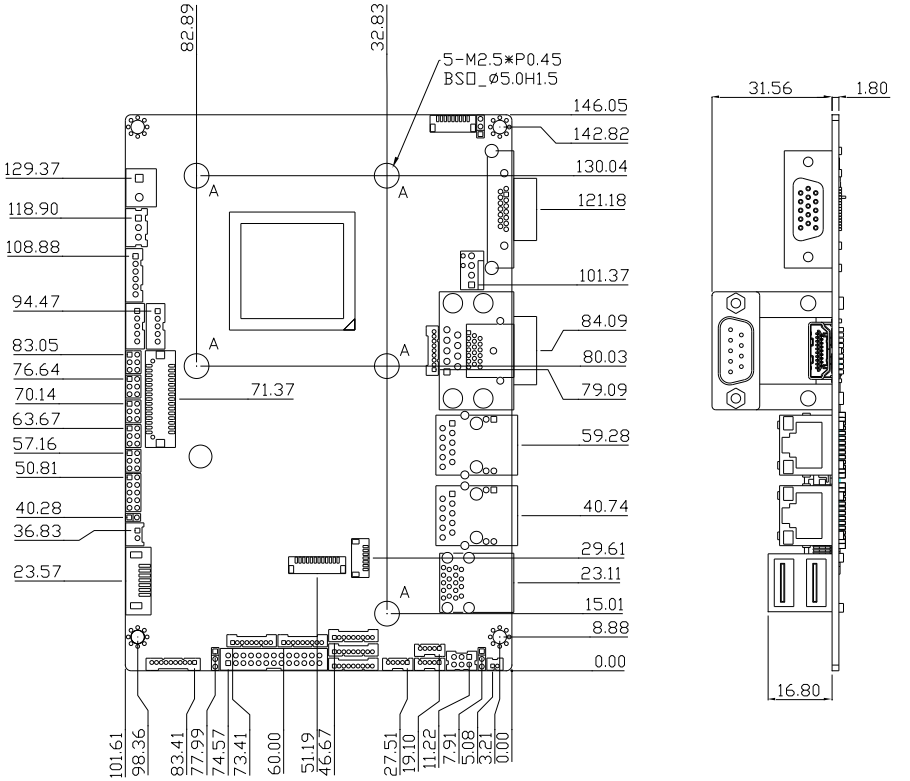


Solder Side

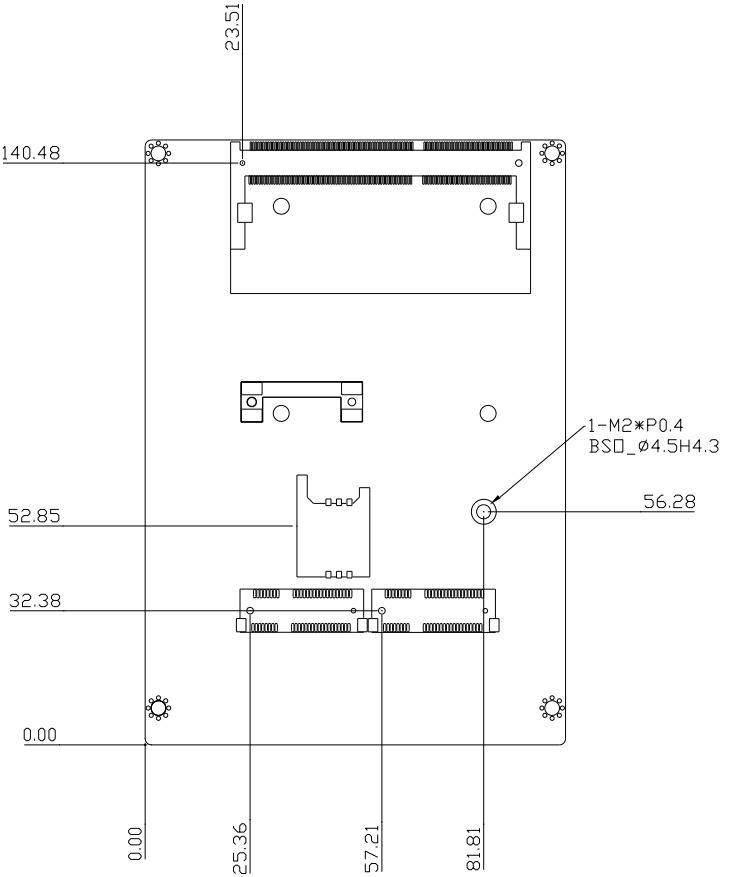

23.51
140.48
1-M2*P0.4
BS□_ø4.5H4.3
56.28
52.85
32.38
0.00
0.00
25.36
57.21
81.81

2.1.1 Dimensions (Optional HDMI SKU)

Component Side

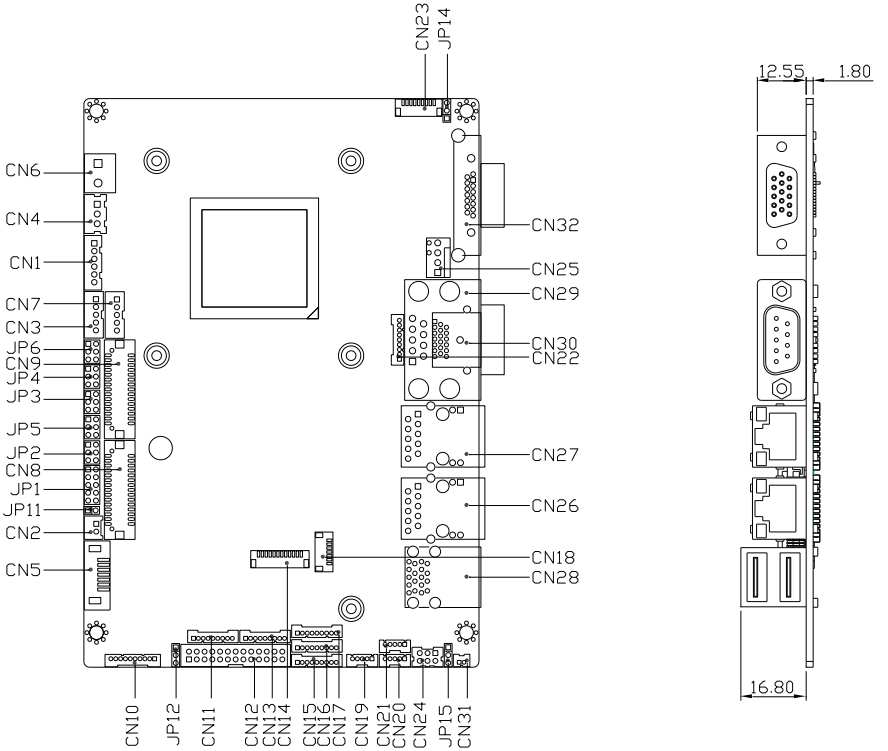


Solder Side

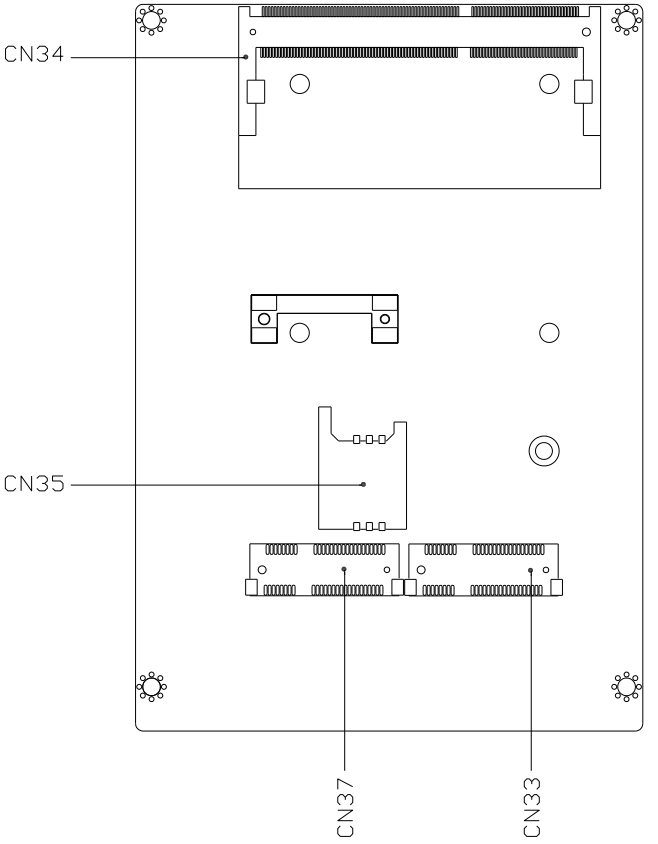

23.51
140.48
1-M2*P0.4
BS□_ø4.5H4.3
56.28
52.85
32.38
0.00
0.00
25.36
57.21
81.81

2.2 Jumpers and Connectors

Component Side

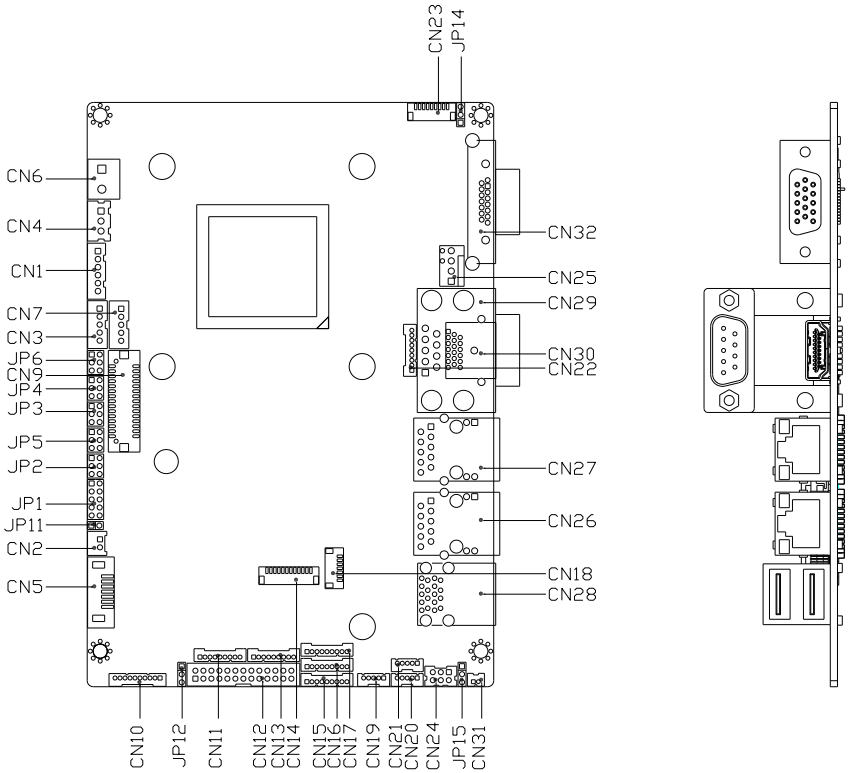


Solder Side

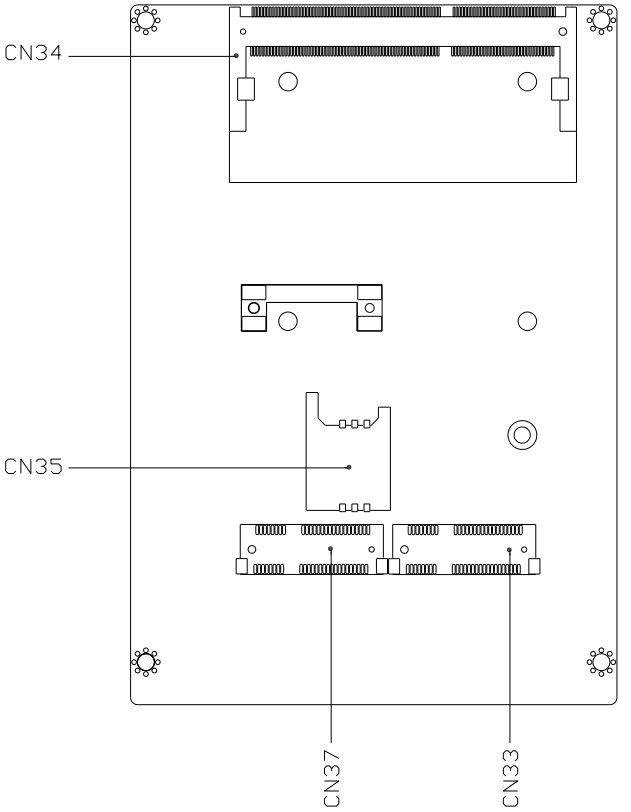


2.2.1 Jumpers and Connectors (Optional HDMI SKU)

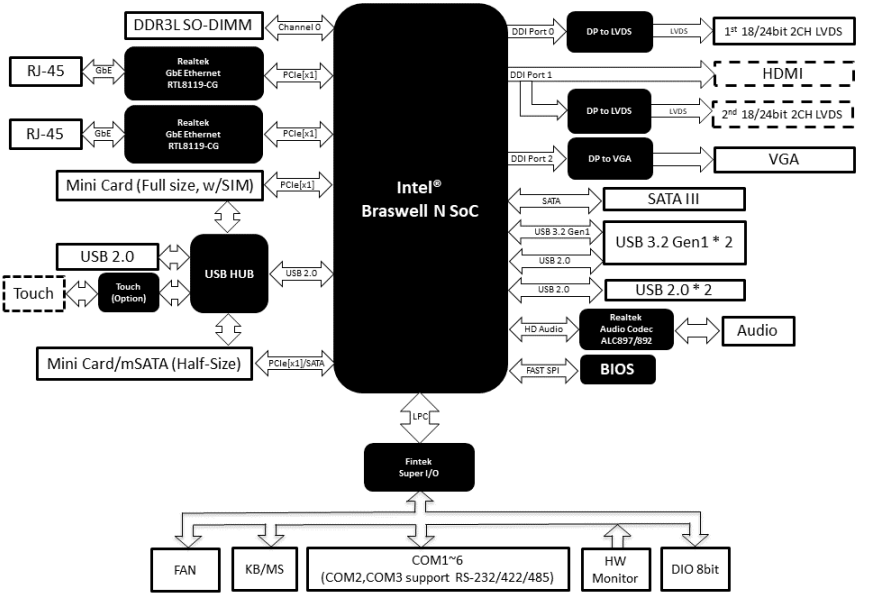
Component Side



Solder Side



2.3 Block Diagram

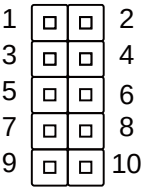


2.4 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

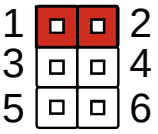
Label	Function
JP1	Front Panel Connector
JP2	COM3 Pin8 Function Selection
JP3	LVDS Port Backlight Inverter VCC Selection
JP4	LVDS Port Operating VDD Selection
JP5	COM2 Pin8 Function Selection
JP6	LVDS Port Backlight Lightness Control Mode Selection
JP11	Flash Descriptor Security
JP12	Auto Power Button Enable/Disable Selection
JP14	Touch Screen 4/5/8-wire Mode Selection
JP15	Clear CMOS Jumper

2.4.1 Front Panel Connector (JP1)

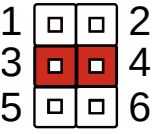


Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	BUZZER-	6	BUZZER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

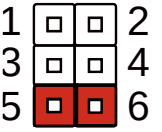
2.4.2 COM3 Function Selection (JP2)



+12V

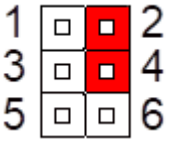
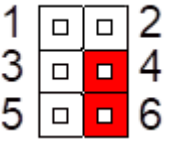
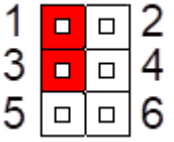
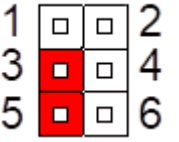


Ring (**Default**)

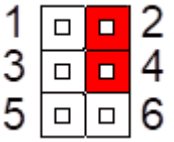
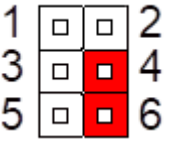
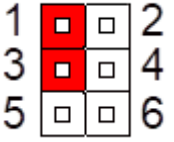
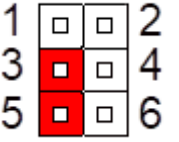


+5V

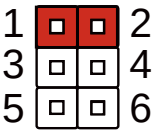
2.4.3 LVDS Port Backlight Inverter VCC Selection (JP3)

LVDS1	
	
LVDS1 +12V	LVDS1 +5V (**Default**)
LVDS2	
	
LVDS2 +12V	LVDS2 +5V (**Default**)

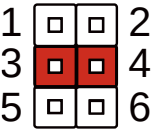
2.4.4 LVDS Port Operating VDD Selection (JP4)

LVDS1	
	
LVDS1 +5V	LVDS1 +3.3V (**Default**)
LVDS2	
	
LVDS2 +5V	LVDS2 +3.3V (**Default**)

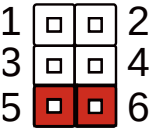
2.4.5 COM2 Function Selection (JP5)



+12V



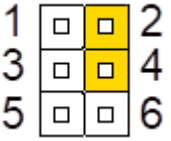
Ring (**Default**)



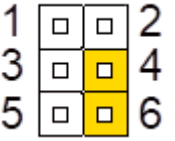
+5V

2.4.6 LVDS Port Backlight Lightness Control Selection (JP6)

LVDS1

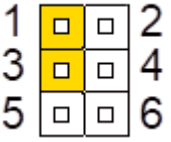


LVDS1
LVDS_BKLCTL_CON

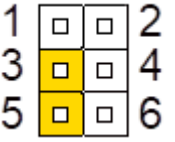


LVDS1
BKLT_CTRL_VR (**Default**)

LVDS2

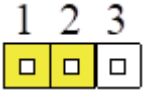


LVDS2
LVDS_BKLCTL_CON

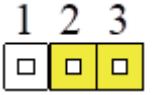


LVDS2
BKLT_CTRL_VR (**Default**)

2.4.7 Auto Power Button Enable/Disable Selection (JP12)

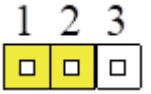


ATX Mode

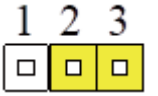


AT Mode (**Default**)

2.4.8 Touchscreen 4/5/8-wire Selection (JP14)

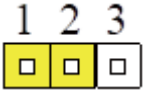


4/8-Wire Mode (**Default**)

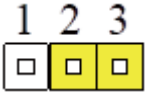


5-Wire Mode

2.4.9 Clear CMOS Jumper (JP15)



Normal (**Default**)



Clear CMOS

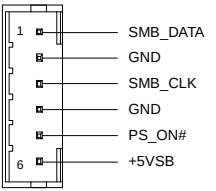
2.5 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	+5VSB Output w/SMBus
CN2	+5V Output for SATA HDD
CN3	LVDS Port Inverter / Backlight Connector
CN4	PSON# Port
CN5	SATA III Port
CN6	External +12V Input
CN7	LVDS2 Port Inverter / Backlight Connector
CN8	LVDS2 Port
CN9	LVDS1 Port
CN10	Audio I/O Port
CN11	COM Port 2
CN12	LPT Port / 8bit DIO
CN13	COM Port 3
CN14	LPC Port
CN15	COM Port 6
CN16	COM Port 5
CN17	COM Port 4
CN18	SPI Debug Port
CN19	USB2.0 Port 3
CN20	USB2.0 Port 2
CN21	USB2.0 Port 4
CN22	COM Port 1
CN23	Touch Screen Connector

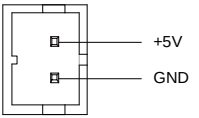
Label	Function
CN24	PS/2 Keyboard/Mouse Combo Port
CN25	CPU FAN (Optional)
CN26	LAN (RJ-45) Port 1
CN27	LAN (RJ-45) Port 2
CN28	USB3.2 Gen 1 Ports 0 and 1 Dual Connector
CN29	COM Port 1 (D-SUB 9)
CN30	HDMI Port
CN31	Battery
CN32	VGA Port
CN33	Mini Card Slot (Half-Sized Mini Card)
CN34	DDR3L SO-DIMM Slot
CN35	UIM Card Socket
CN37	Mini Card Slot (Full-Size Mini Card)

2.5.1 +5 VSB Output w/SMBus (CN1)



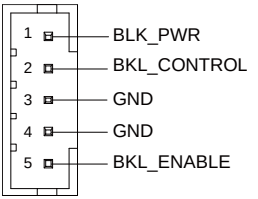
Pin	Pin Name	Signal Type	Signal level
1	SMB_DATA	I/O	+3.3V
2	GND	GND	
3	SMB_CLK	I/O	+3.3V
4	GND	GND	
5	PS_ON#	OUT	+3.3V
6	+5VSB	PWR	+5V

2.5.2 +5V Output for SATA HDD (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	GND	GND	

2.5.3 LVDS Port Inverter / Backlight Connector (CN3)

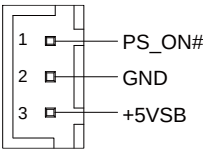


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

Note 1: LVDS BKL_PWR can be set to +5V or +12V by JP3. Driving current supported up to 1.5A

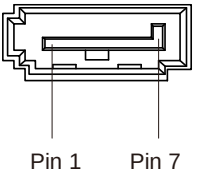
Note 2: LVDS BKL_CONTROL can be set by JP6.

2.5.4 PSON# Port (CN4)



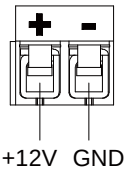
Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+3.3V
2	GND	GND	
3	+5VSB	PWR	+5V

2.5.5 SATA III Port (CN5)



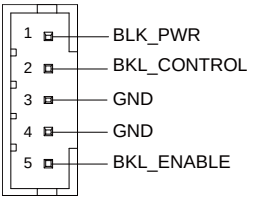
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.5.6 External +12V Input (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	

2.5.7 LVDS2 Port Inverter / Backlight Connector (CN7)

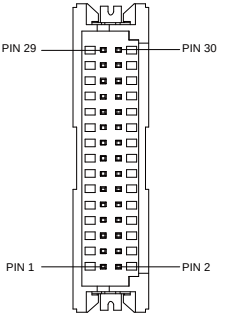


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+3.3V

Note 1: LVDS BKL_PWR can be set to +5V or +12V by JP3. Driving current supported up to 1.5A

Note 2: LVDS BKL_CONTROL can be set by JP6.

2.5.8 LVDS2 Port (CN8)

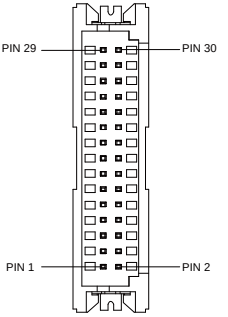


Note: LVDS LCD_PWR (Pin 3) can be set to +3.3V or +5V by JP4. Driving current supports up to 1.5A

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.5.9 LVDS1 Port (CN9)

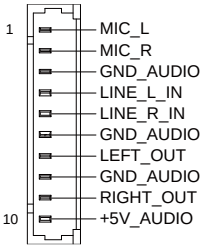


Note: LVDS LCD_PWR (Pin 3) can be set to +3.3V or +5V by JP4. Driving current supports up to 1.5A

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	
2	BKL_CONTROL	OUT	
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS_A_CLK-	DIFF	
6	LVDS_A_CLK+	DIFF	
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS_DA0-	DIFF	
10	LVDS_DA0+	DIFF	
11	LVDS_DA1-	DIFF	
12	LVDS_DA1+	DIFF	
13	LVDS_DA2-	DIFF	
14	LVDS_DA2+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
15	LVDS_DA3-	DIFF	
16	LVDS_DA3+	DIFF	
17	DDC_DATA	I/O	+3.3V
18	DDC_CLK	I/O	+3.3V
19	LVDS_DB0-	DIFF	
20	LVDS_DB0+	DIFF	
21	LVDS_DB1-	DIFF	
22	LVDS_DB1+	DIFF	
23	LVDS_DB2-	DIFF	
24	LVDS_DB2+	DIFF	
25	LVDS_DB3-	DIFF	
26	LVDS_DB3+	DIFF	
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS_B_CLK-	DIFF	
30	LVDS_B_CLK+	DIFF	

2.5.10 Audio I/O Port (CN10)



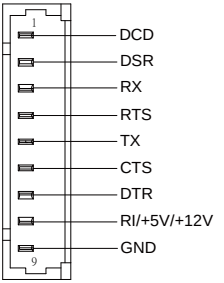
Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	
7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

2.5.11 COM Port 2 (CN11)

Note 1: COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

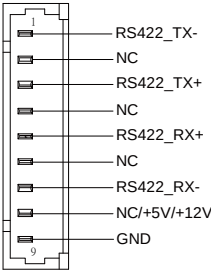
Note 2: Pin 8 function can be set by JP5. Maximum driving current in power supply mode is 0.5A

RS-232



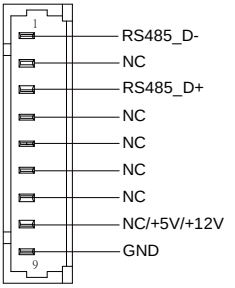
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

RS-422



Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

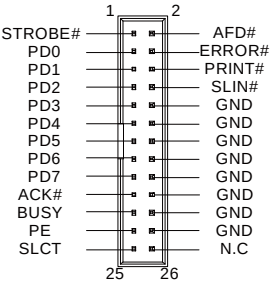
RS-485



Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

2.5.12 LPT Port / 8-bit DIO (CN12)

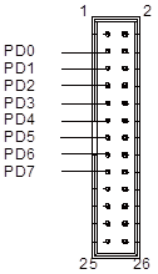
LPT Port:



Pin	Pin Name	Signal Type	Signal Level
1	STROBE#	IN	
2	AFD#	I/O	
3	PD0	I/O	
4	ERROR#	IN	
5	PD1	I/O	
6	PRINT#	I/O	
7	PD2	I/O	
8	SLIN#	I/O	
9	PD3	I/O	
10	GND	GND	
11	PD4	I/O	
12	GND	GND	
13	PD5	I/O	
14	GND	GND	
15	PD6	I/O	
16	GND	GND	
17	PD7	I/O	

Pin	Pin Name	Signal Type	Signal Level
18	GND	GND	
19	ACK#	IN	
20	GND	GND	
21	BUSY	IN	
22	GND	GND	
23	PD8	IN	
24	GND	GND	
25	SLCT	IN	
26	NC		

8-bit DIO:



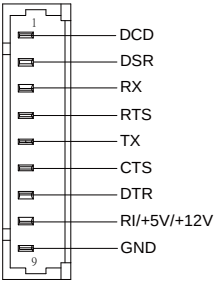
Pin	Pin Name	Signal Type	Signal Level
3	GPIO0	I/O	
5	GPIO1	I/O	
7	GPIO2	I/O	
9	GPIO3	I/O	
11	GPIO4	I/O	
13	GPIO5	I/O	
15	GPIO6	I/O	
17	GPIO7	I/O	

2.5.13 COM Port 3 (CN13)

Note 1: COM3 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

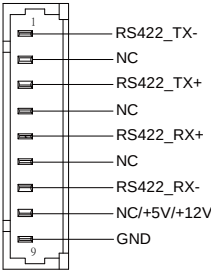
Note 2: Pin 8 function can be set by JP2. Maximum driving current in power supply mode is 0.5A

RS-232



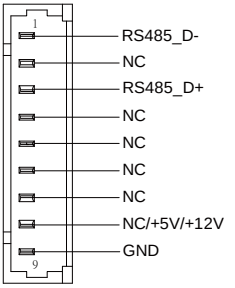
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI/+5V/+12V	IN/ PWR	+5V/+12V
9	GND	GND	

RS-422



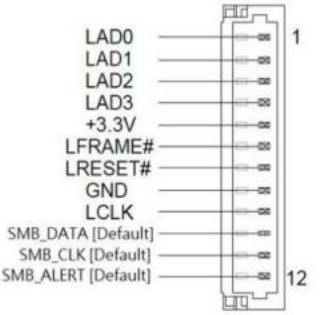
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	
6	NC		
7	RS422_RX-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

RS-485



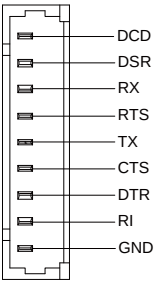
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	I/O	±5V
2	NC		
3	RS485_D+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

2.5.14 LPC Port (CN14)



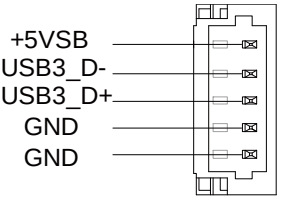
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	SMB_DATA [Default]/ I2C_DATA	IN	+3.3V
11	SMB_CLK [Default]/ I2C_CLK	OUT	+3.3V
12	SMB_ALERT [Default]/ INT_SERIRQ	I/O	+3.3V

2.5.15 COM Port 4, 5, 6 (CN15/ CN16/ CN17)



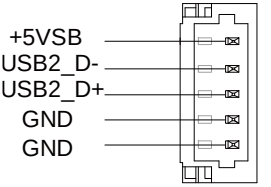
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	
4	RTS	OUT	±9V
5	TX	OUT	±9V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.5.16 USB2.0 Port 3 (CN19)



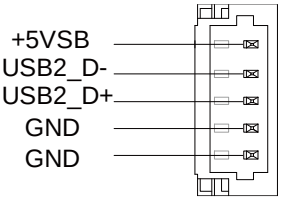
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB3_D-	DIFF	
3	USB3_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.17 USB2.0 Port 2 (CN20)



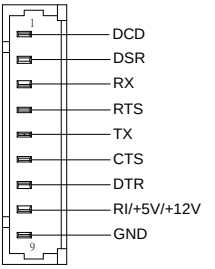
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_D-	DIFF	
3	USB2_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.20 USB2.0 Port 4 (CN21)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB4_D-	DIFF	
3	USB4_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.21 COM Port 1 (CN22)



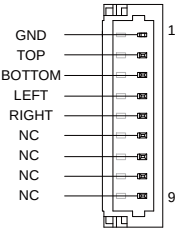
Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	DSR	IN	
3	RX	IN	

Pin	Pin Name	Signal Type	Signal Level
4	RTS	OUT	±5V
5	TX	OUT	±5V
6	CTS	IN	
7	DTR	OUT	±9V
8	RI	IN	
9	GND	GND	

2.5.22 Touchscreen Connector (CN23)

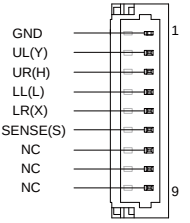
Note: Touch Mode can be set by JP14

4 Wires



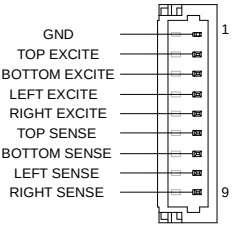
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		

5 Wires



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

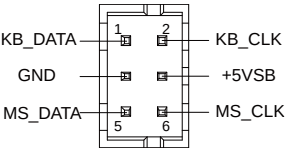
8 Wires



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	

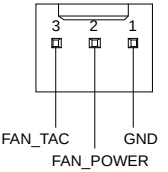
Pin	Pin Name	Signal Type	Signal Level
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	
8	LEFT SENSE	IN	
9	RIGHT SENSE	IN	

2.5.23 PS/2 Keyboard/Mouse Combo Port (CN24)



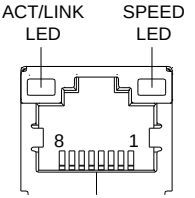
Pin	Pin Name	Signal Type	Signal Level
1	KB_DATA	I/O	+5V
2	KB_CLK	I/O	+5V
3	GND	GND	
4	+5VSB	PWR	+5V
5	MS_DATA	I/O	+5V
6	MS_CLK	I/O	+5V

2.5.24 CPU Fan (CN25)



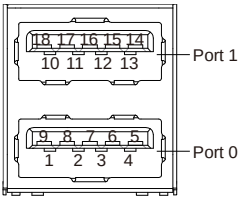
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	

2.5.25 LAN (RJ-45) Port 1/ Port 2 (CN26/CN27)



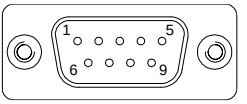
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.5.27 USB3.2 Dual Connector Ports 0 and 1 (CN28)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−		
15	USB1_SSRX+		
16	GND	GND	
17	USB1_SSTX−		
18	USB1_SSTX+		

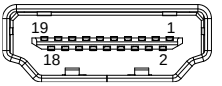
2.5.28 COM Port 1 (D-SUB 9) (CN29)



Note: COM port1 can be selected for D-SUB9 or Wafer BOX connector (CN22)

Pin	Pin Name	Signal Type	Signal Level
1	DCD	IN	
2	RX	IN	
3	TX	OUT	±9V
4	DTR	OUT	±9V
5	GND	GND	
6	DSR	IN	
7	RTS	OUT	±9V
8	CTS	IN	
9	RI	IN	

2.5.29 HDMI Port (CN30)



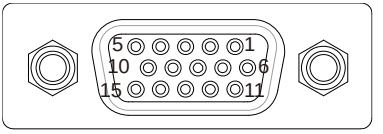
Pin	Pin Name	Signal Type	Signal Level
1	TMDS_DAT2+	DIFF	
2	GND	GND	
3	TMDS_DAT2-	DIFF	

Pin	Pin Name	Signal Type	Signal Level
4	TMDS_DAT1+	DIFF	
5	GND	GND	
6	TMDS_DAT1-	DIFF	
7	TMDS_DAT0+	DIFF	
8	GND	GND	
9	TMDS_DAT0-	DIFF	
10	TMDS_CLK+	DIFF	
11	GND	GND	
12	TMDS_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	I/O	+5V
19	HPLG_DETECT	IN	

2.5.30 Battery (CN31)

Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	3.3V
2	GND	GND	

2.5.31 VGA Port (CN32)



Pin	Pin Name	Signal Type	Signal Level
1	RED	OUT	
2	GREEN	OUT	
3	BLUE	OUT	
4	NC		
5	GND	GND	
6	RED_GND_RTN	GND	
7	GREEN_GND_RTN	GND	
8	BLUE_GND_RTN	GND	
9	+5V	PWR	+5V
10	CRT_PLUG#		
11	NC		
12	DDC_DATA	I/O	+5V
13	HSYNC	OUT	
14	VSYNC	OUT	
15	DDC_CLK	I/O	+5V

2.5.32 Mini Card Slot (Half-Size) (CN33)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V

Pin	Pin Name	Signal Type	Signal Level
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
51	NC		
52	+3.3VSB	PWR	+3.3V

2.5.33 DDR3L SO-DIMM (CN34)

Standard Specifications

2.5.34 UIM Card Socket (CN35)

Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	GND	GND	
5	UIM_VPP	PWR	
6	UIM_DATA	I/O	

2.5.35 Mini Card Slot (Full-Size) (CN36)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	

Pin	Pin Name	Signal Type	Signal Level
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory lost power and the configuration information was erased

The board's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access advanced hardware settings and options including Hardware Monitor

Chipset – Chipset settings and options

Security – Set admin and user passwords

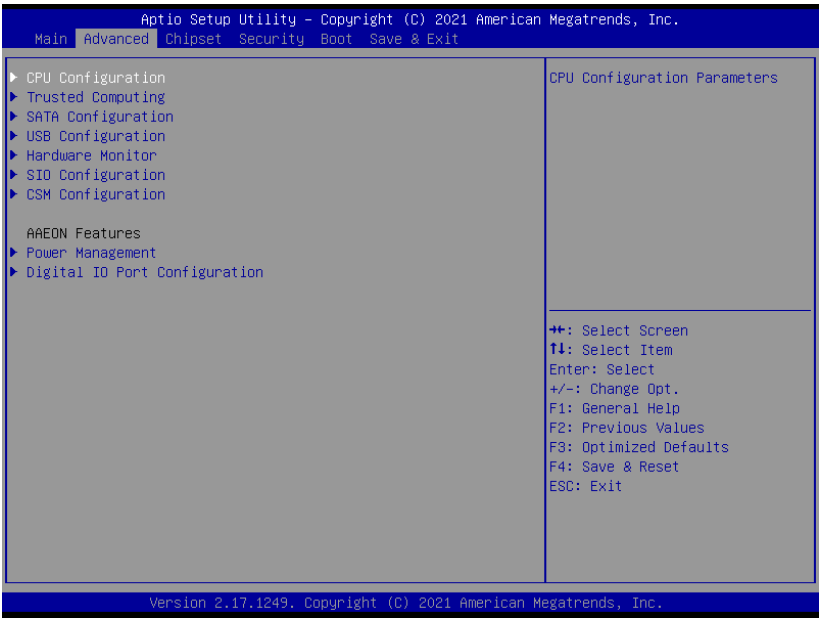
Boot – Boot options including BBS priority and Quiet Boot options

Save & Exit –Save changes and exit the program

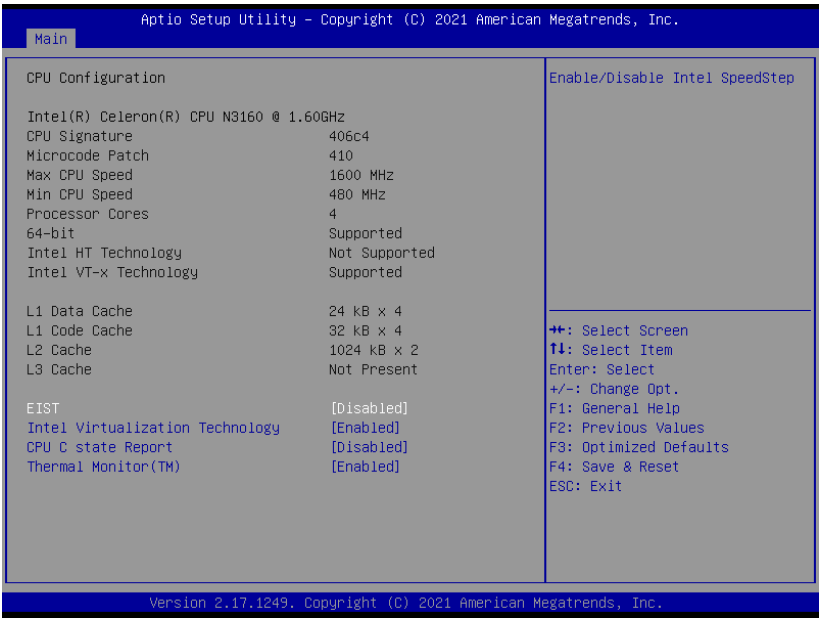
3.3 Setup Submenu: Main

Options Summary		
System Date	Day MM:DD:YYYY	
Change the month, year and century. The 'Day' is changed automatically.		
System Time	HH:MM:SS	
Change the clock of the system.		

3.4 Setup Submenu: Advanced

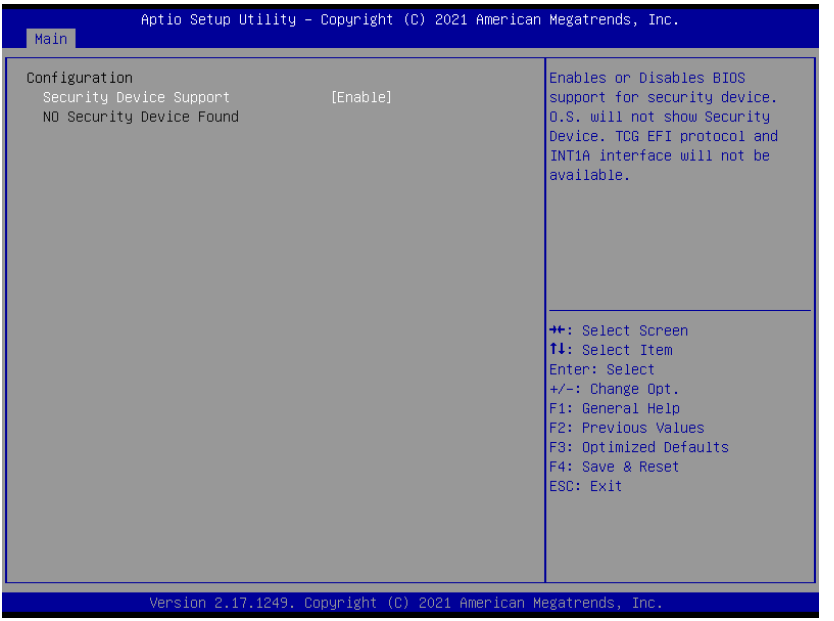


3.4.1 CPU Configuration



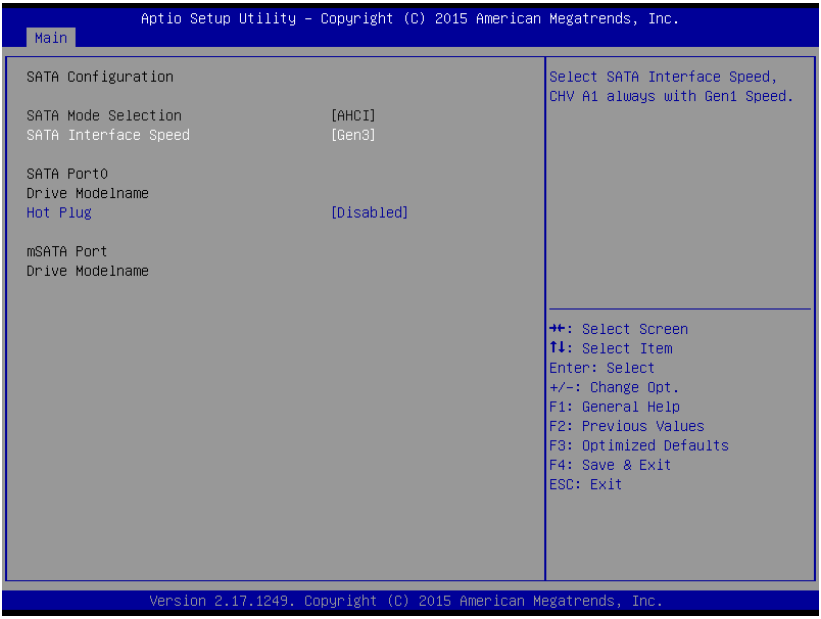
Options Summary		
EIST	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enable/Disable Intel SpeedStep feature.		
Intel Virtualization Technology	Enabled	Optimal Default; Failsafe Default
	Disabled	
When enabled, a VMM can utilize the additional hardware capabilities provide by Vanderpool Technology		
CPU C State Report	Enabled	
	Disabled	Optimal Default; Failsafe Default
Enable/Disable CPU C state report to OS		
Thermal Monitor (TM)	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enable/Disable CPU Thermal Monitor		

3.4.2 Trusted Computing



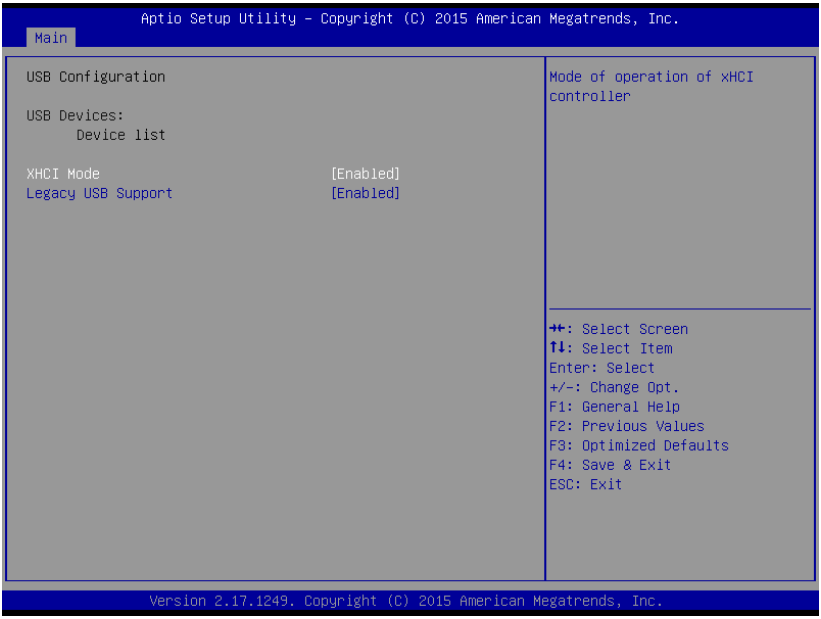
Options Summary		
Security Device Support	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		

3.4.3 SATA Configuration



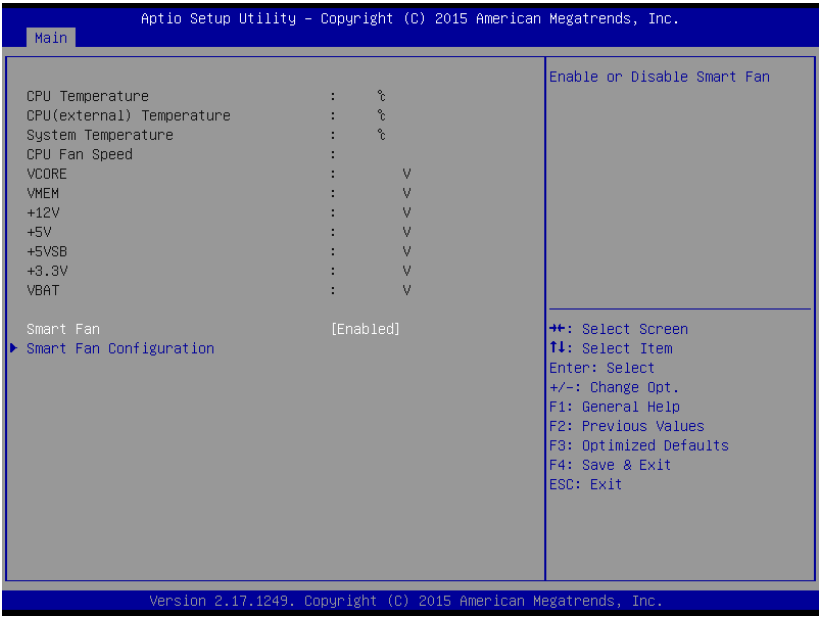
Options Summary		
SATA Speed Support	Gen3	Optimal Default; Failsafe Default
	Gen2	
	Gen1	
SATA Speed Support Gen3, Gen2 or Gen1		
SATA Mode	AHCI Mode	Optimal Default; Failsafe Default
Only AHCI mode support on this platform		
SATA Port0/Port1 Hot Plug	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enabled/Disabled SATA Port0/Port1 Hot Plug function		

3.4.4 USB Configuration



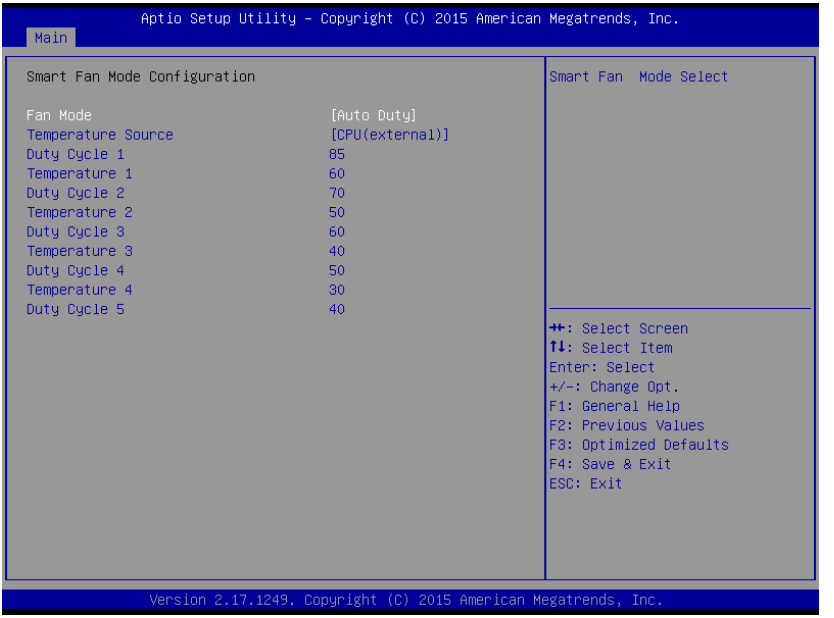
Options Summary		
XHCI Mode	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enable/Disable for xHCI controller.		
Legacy USB Support	Enabled	Optimal Default; Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI application		

3.4.5 Hardware Monitor



Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable specified Smart Fan.		

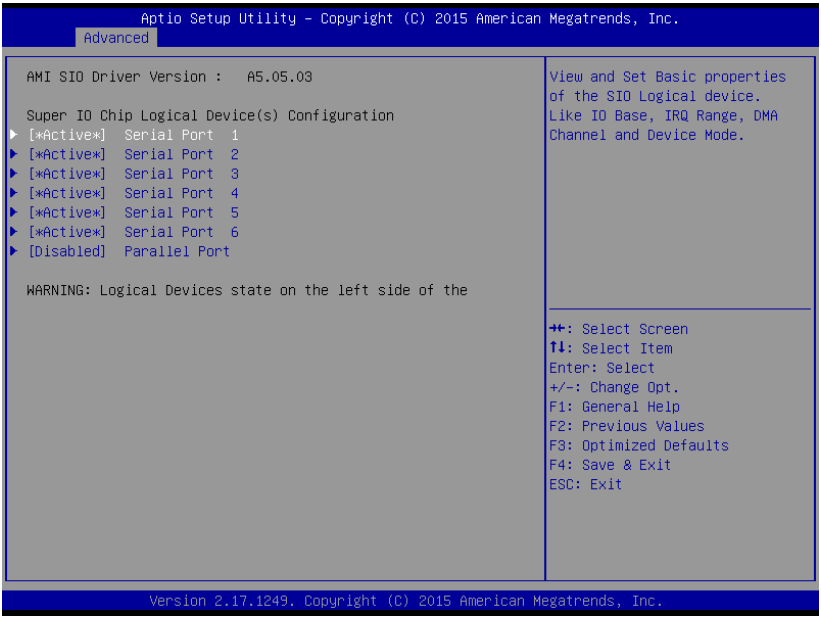
3.4.4.1 Smart Fan Configuration



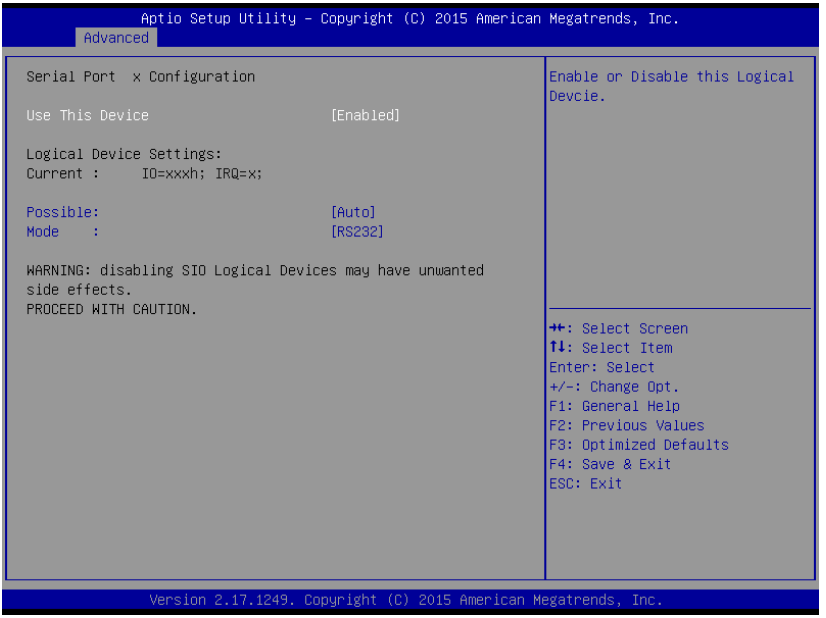
Options Summary		
Fan Mode	Manual Duty	
	Auto Duty	Optimal Default; Failsafe Default
Smart Fan Mode Select		
Manual Duty Mode	60	Optimal Default; Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1 – 100		
Temperature Source	CPU (external)	Optimal Default; Failsafe Default
Select the monitored temperature source for this fan. Only supports CPU (external) support for this board.		
Duty Cycle 1	85	Optimal Default; Failsafe Default
Duty Cycle 2	70	Optimal Default; Failsafe Default
Duty Cycle 3	60	Optimal Default; Failsafe Default
Duty Cycle 4	50	Optimal Default; Failsafe Default
Duty Cycle 5	40	Optimal Default; Failsafe Default
Fan speed control for each temperature region. User can write expected duty cycle (PWM fan type) 1 – 100		

Options Summary		
Temperature 1	60	Optimal Default; Failsafe Default
Temperature 2	50	Optimal Default; Failsafe Default
Temperature 3	40	Optimal Default; Failsafe Default
Temperature 4	30	Optimal Default; Failsafe Default
Definition of temperature region. User can write expected temperature boundary 1 – 100		

3.4.6 SIO Configuration



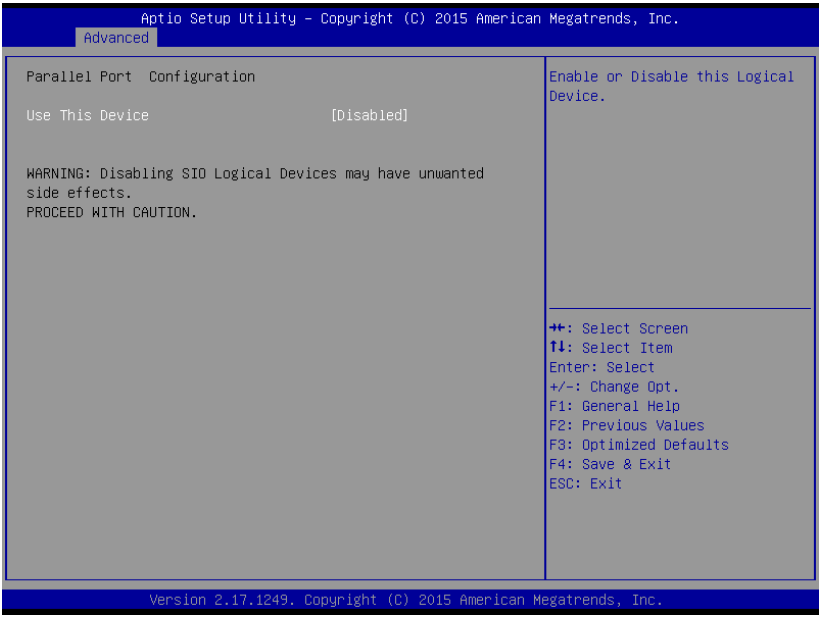
3.4.6.1 Serial Port 1-6 Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable specified serial port.		
Change Settings (COM1)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Change Settings (COM2)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Change Settings (COM3)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=3E8h; IRQ=11;	
	IO=2E8h; IRQ=11;	
Change Settings (COM4)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=2E8h; IRQ=11;	
	IO=3E8h; IRQ=11;	

Options Summary		
Change Settings (COM5)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=2D0h; IRQ=11;	
	IO=2C0h; IRQ=11;	
Change Settings (COM6)	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=2C0h; IRQ=11;	
	IO=2D0h; IRQ=11;	
Select a resource setting for Super IO device.		
Mode	RS232	
	RS422	
	RS485	
Configure COM operated as RS232, RS422 or RS485. Only COM2 and COM3 support this function.		

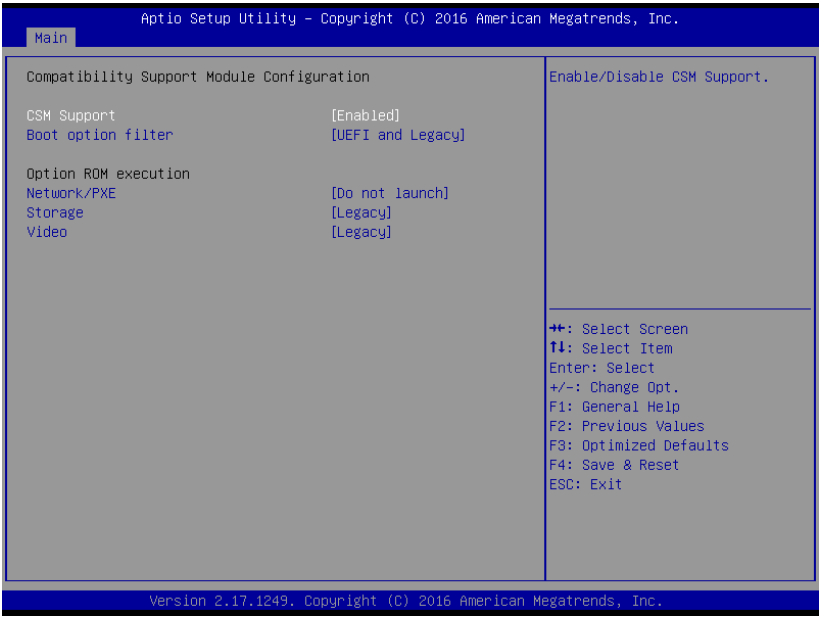
3.4.6.2 Parallel Port Configuration



Options Summary		
Use This Device	Disabled	Optimal Default; Failsafe Default
	Enabled	
En/Disable specified this Logical Device Note: LPT and DIO feature share the same interface on the board. When LPT disabled, the interface works in DIO mode and vice versa.		
Possible	Use Automatic Settings	Optimal Default; Failsafe Default
	IO=378h; IRQ=5;	STD Printer
	IO=378h; IRQ=5,6,7,9,10,11,12;	SPP
	IO=278h; IRQ=5,6,7,9,10,11,12;	EPP and SPP
	IO=3BCh; IRQ=5,6,7,9,10,11,12;	
	IO=378h; IO=778h; IRQ=5; DMA=3;	ECP
	IO=378h; IO=778h; IRQ=5,6,7,9,10,11,12; DMA=1,3;	ECP and EPP
	IO=278h; IO=678h; IRQ=5,6,7,9,10,11,12; DMA=1,3;	

Options Summary		
	IO=3BCh; IO=7BCh; IRQ=5,6,7,9,10,11,12; DMA=1,3;	
Select a resource setting for Super IO device		
Mode	STD Print Mode	Optimal Default; Failsafe Default
	SPP Mode	
	EPP-1.9 and SPP Mode	
	EPP-1.7 and SPP Mode	
	ECP Mode	
	ECP and EPP 1.9 Mode	
	ECP and EPP 1.7 Mode	
Change Parallel Port mode		

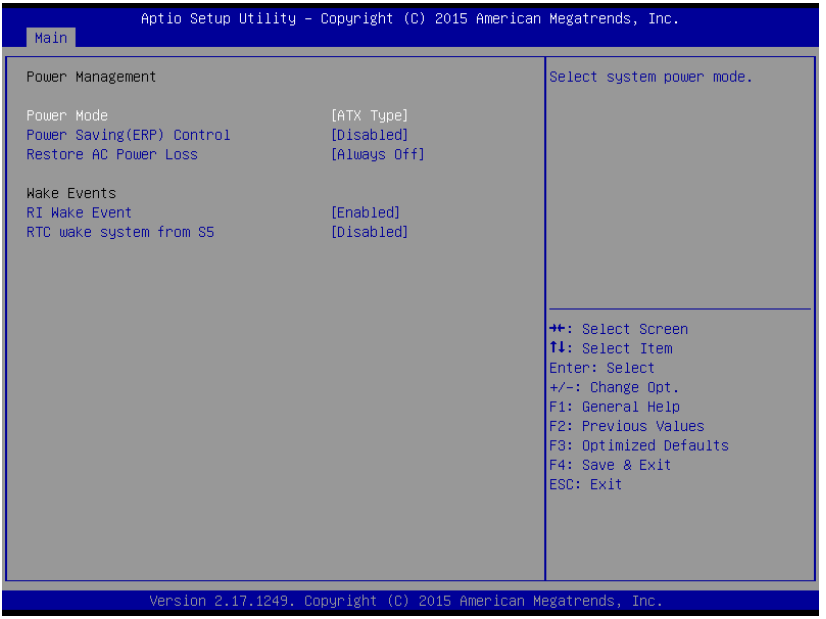
3.4.7 CSM Configuration



Options Summary		
CSM Support	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enable/Disable for CSM Support		
Boot option filter	UEFI and Legacy	Optimal Default; Failsafe Default
	Legacy only	
	UEFI only	
This option controls Legacy/UEFI boot option priority		
Network/PXE	Do not launch	Optimal Default; Failsafe Default
	UEFI	
	Legacy	
Controls the execution of UEFI and Legacy PXE OpROM		
Storage	Do not launch	
	UEFI	
	Legacy	Optimal Default; Failsafe Default
Controls the execution of UEFI and Legacy Storage OpROM		

Options Summary		
Video	Do not launch	
	UEFI	
	Legacy	Optimal Default; Failsafe Default
Controls the execution of UEFI and Legacy Video OpROM		

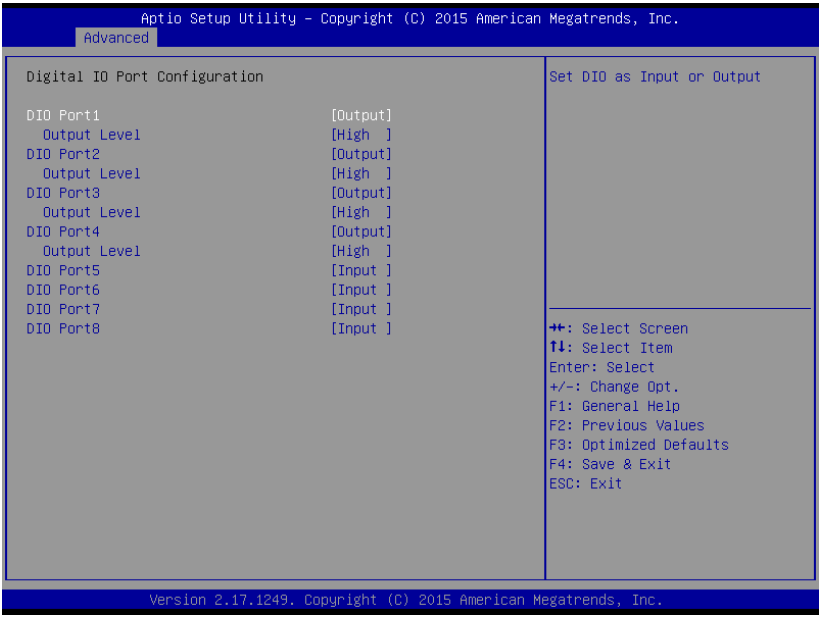
3.4.8 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default; Failsafe Default
	AT Type	
Select system power mode		
Power Saving (ERP) Control	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enabled or disabled ERP feature for power saving in S5 state.		
Restore AC Power Loss	Power Off	Optimal Default; Failsafe Default
	Power on	
	Late State	
Select AC power state when power is re-applied after a power failure		
RI Wake Event	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enabled or disabled wake on ring function.		
RTC wake system from S5	Disabled	Optimal Default; Failsafe Default
	Fixed Time	
	Dynamic Time	

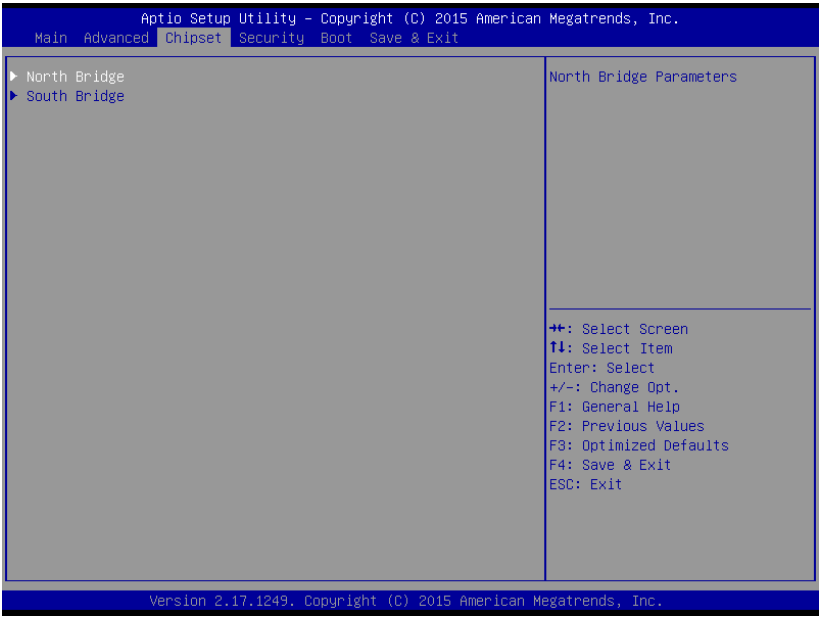
Options Summary		
Enable system to wake from S5 using RTC alarm.		
Wake up day	0-31	
Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0-23	
Wake up minute	0-59	
Wake up second	0-59	
Wake up minute increase	1-5	

3.4.9 Digital IO Port Configuration



Options Summary		
DIO Port1/2/3/4	Input	Optimal Default; Failsafe Default
	Output	
Set DIO Port1/2/3/4 as Input or Output		
DIO Port5/6/7/8	Input	Optimal Default; Failsafe Default
	Output	
Set GPIO3/GPIO4 as Input or Output		
Output Level	Hi	Optimal Default; Failsafe Default
	Low	
Set GPIO Level when used as Output		

3.5 Setup Submenu: Chipset

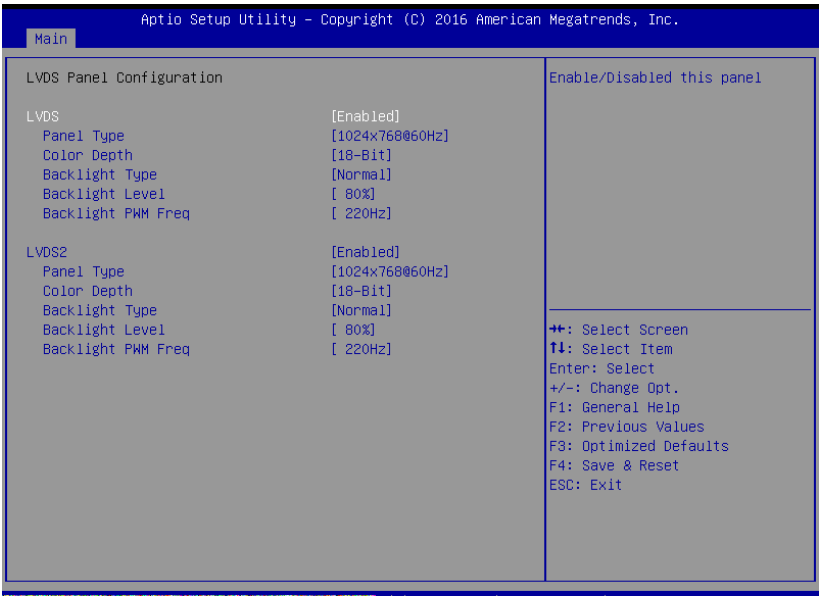


3.5.1 North Bridge Configuration

Options Summary		
Max TOLUD	2 GB	Optimal Default; Failsafe Default
	2.25 GB	
	2.5 GB	
	2.75 GB	
Maximum Value of TOLUD		
Primary Boot Display	Auto	Optimal Default; Failsafe Default
	CRT	
	LVDS1	
	LVDS2	
Select Primary boot display device		
Secondary Boot Display	Disabled	Optimal Default; Failsafe Default
	CRT	
	LVDS1	
	LVDS2/HDMI	
Select Primary boot display device		

Options Summary		
DVMT Pre-Allocated	32MB	Optimal Default; Failsafe Default
	32MB~512MB	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128MB	Optimal Default; Failsafe Default
	256MB	
	Max	
Select DVMT 5.0 Total Graphic Memory size used by the IGD.		

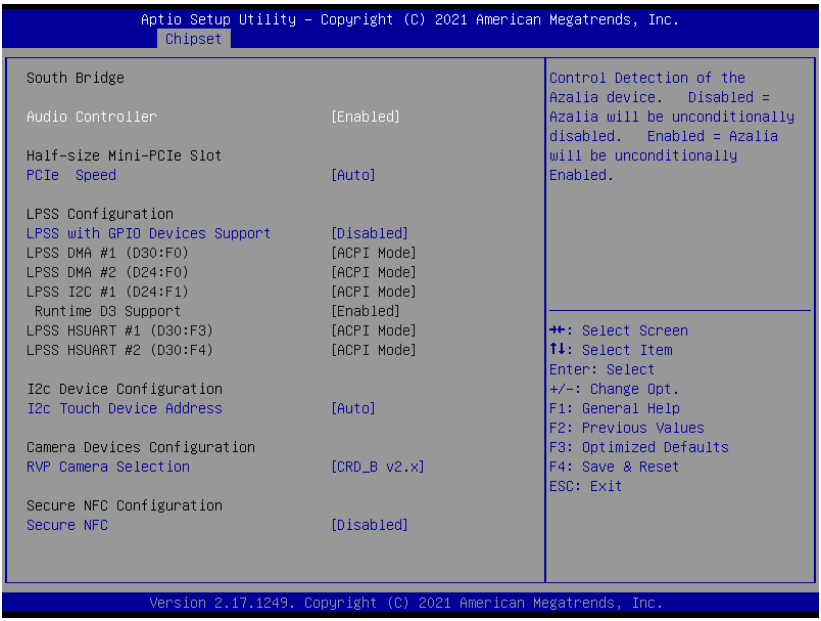
3.5.1.1 LVDS Panel Configuration



Options Summary		
LVDS	Disabled	
	Enabled	Optimal Default; Failsafe Default
LVDS2	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable LVDS interface		
Panel Type	640x480	
	800x480	
	800x600	
	1024x600	
	1024x768	Optimal Default; Failsafe Default
	1280x768	
	1280x1024	
	1366x768	
	1440x900	
	1600x1200	
	1920x1080	
	1920x1200	

Options Summary		
Select panel resolution.		
Color Depth	18-Bit	Optimal Default; Failsafe Default
	24-Bit	
	36-Bit	
	48-Bit	
Select color depth of the panel		
Backlight Type	Inverted	
	Normal	Optimal Default; Failsafe Default
Select Backlight control type. Inverted: Brightest for low PWM duty cycle and low voltage. Normal: Brightest for high PWM duty cycle and high voltage.		
Backlight Level	100%	
	90%	
	80%	Optimal Default; Failsafe Default
	70%	
	60%	
	50%	
	40%	
	30%	
	20%	
	10%	
	0%	
Select Backlight Level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default; Failsafe Default
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal.		

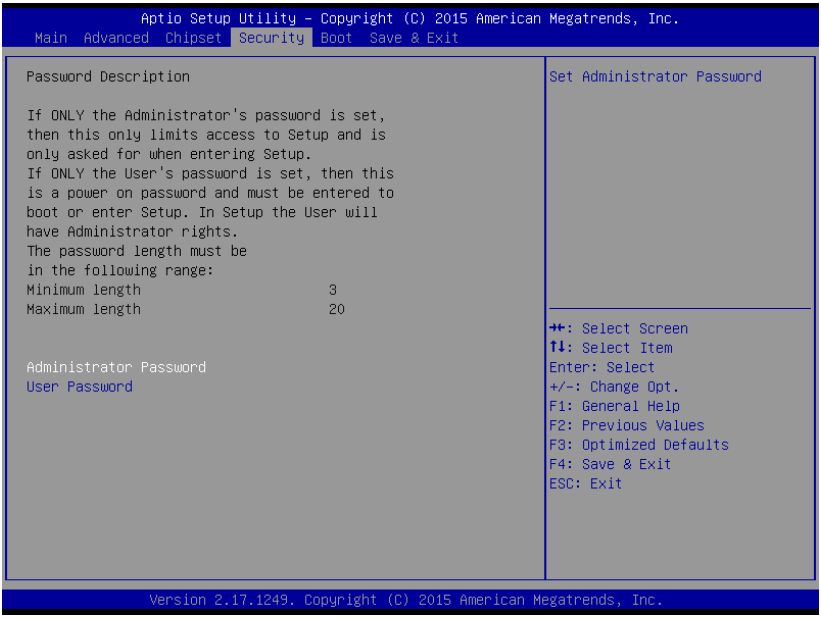
3.5.2 South Bridge



Options Summary		
Audio Controller	Disabled	Optimal Default; Failsafe Default
	Enabled	
Enable or disabled Azalia device for audio function.		
PCIe Speed	Auto	Optimal Default; Failsafe Default
	Gen 2	
	Gen 1	
Configure PCIe Speed. CHV A1 always with Gen2 Speed.		
LPSS with GPIO Devices Support	Disabled	Optimal Default; Failsafe Default
	Enabled	
Enable/Disable GPIO ACPI Devices Support, disable it will disable all LPSS device.		
LPSS DMA #1 (D30:F0)	ACPI Mode	Optimal Default; Failsafe Default
	PCI Mode	
	Disable	
Enable/Disable LPSS DMA #1 Support		
LPSS DMA #2 (D24:F0)	ACPI Mode	Optimal Default; Failsafe Default
	PCI Mode	

Options Summary		
	Disable	
Enable/Disable LPSS DMA #2 Support		
LPSS I2C #1 (D24:F1)	ACPI Mode	Optimal Default; Failsafe Default
	PCI Mode	
	Disable	
Enable/Disable LPSS I2C #1 Support		
Runtime D3 Support	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable/Disable Runtime D3 Support.		
LPSS HSUART #1 (D30:F3)	ACPI Mode	Optimal Default; Failsafe Default
	PCI Mode	
	Disable	
Enable/Disable LPSS HSUART #1 Support		
LPSS HSUART #1 (D30:F4)	ACPI Mode	Optimal Default; Failsafe Default
	PCI Mode	
	Disable	
Enable/Disable LPSS HSUART #2 Support		
I2c Touch Device Address	Auto	Optimal Default; Failsafe Default
	0x4C	
	0x4A	
I2c Touch Device Address: CHIMEI(0x4C)/SHARP(0x4A)		
RVP Camera	Cynthiana_A	
	CRD_B V2.x	Optimal Default; Failsafe Default
Select Camera Device		
Secure NFC	Enabled	
	Disabled	Optimal Default; Failsafe Default
Secure NFC - Enable/Disable		

3.6 Setup Submenu: Security



Change User/Administrator Password

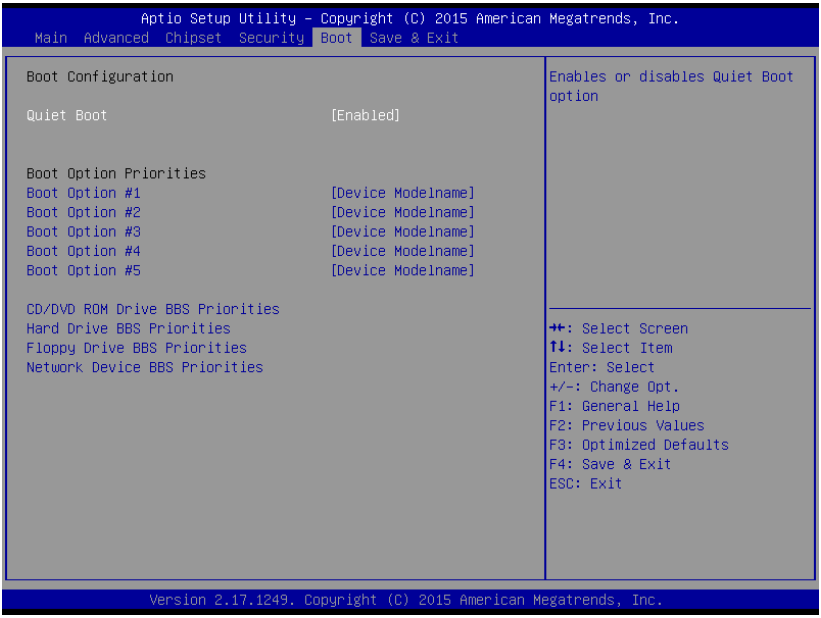
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

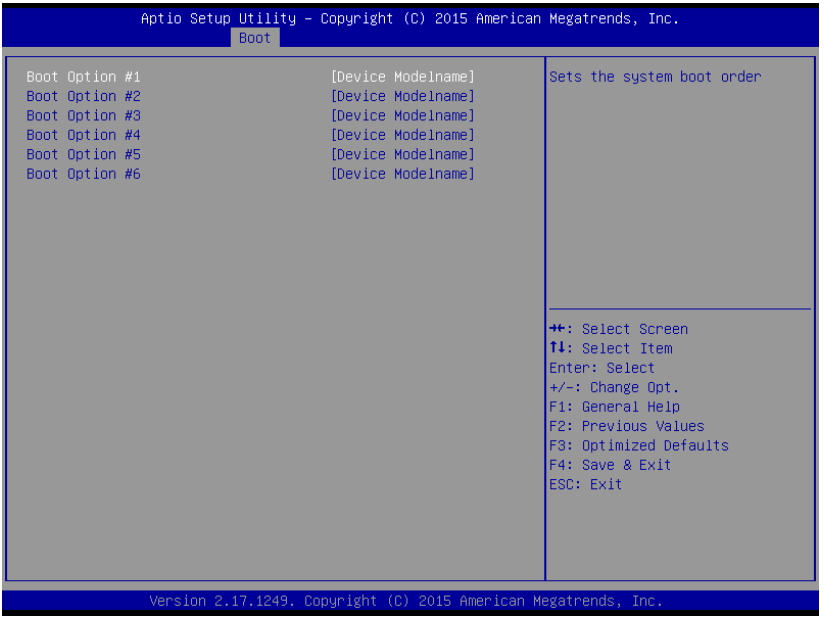
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup Submenu: Boot



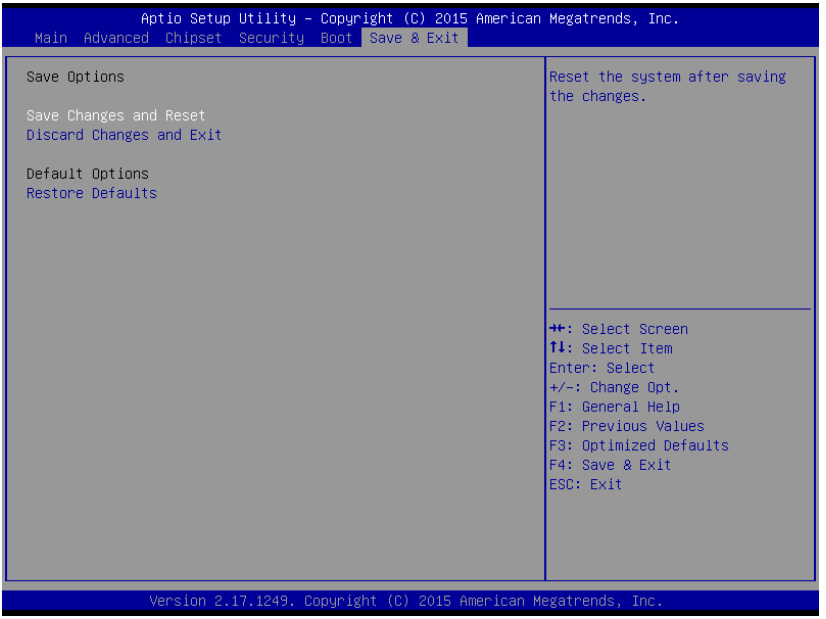
Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default; Failsafe Default
Enable or Disable showing boot logo.		
Boot Option #X/ XXXX Drive Priorities		
The order of boot priorities.		

3.7.1 BBS Priorities



Options Summary		
Boot Option #x	Disabled	
	Device Name	
Sets the system boot order.		

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the GENE-APL6 A11 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/3-and-a-half-inch-subcompact-board-gene-bsw5

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step1 - Chipset** folder and select your OS
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step2 - VGA** folder and select your OS
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Note 1: After graphics drivers are installed, LVDS1 will be set as the default video output, not VGA. Users can change this by disabling LVDS1/LVDS2 in BIOS to make VGA the default output. Desktop display modes can be changed using the hotkey "Win + P".

Note 2: There is a known issue in Windows 8.1 where running Direct3D graphic tools such as BurnIn Test will cause the system to freeze. Microsoft has provided the KB2979265 hotfix to address this issue. To apply the hotfix without dependency issues, it is recommended to be installed via Windows Update.

Step 3 – Install Audio Drivers

1. Click on the **Step3 - Audio** folder and select your OS
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install LAN Drivers

1. Open the **Step4 - LAN** folder and select your OS
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Touch Panel Driver

1. Open the **Step5 - TOUCHPANEL** folder and run the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install TXE Driver

1. Open the **Step6 - TXE** folder and run the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

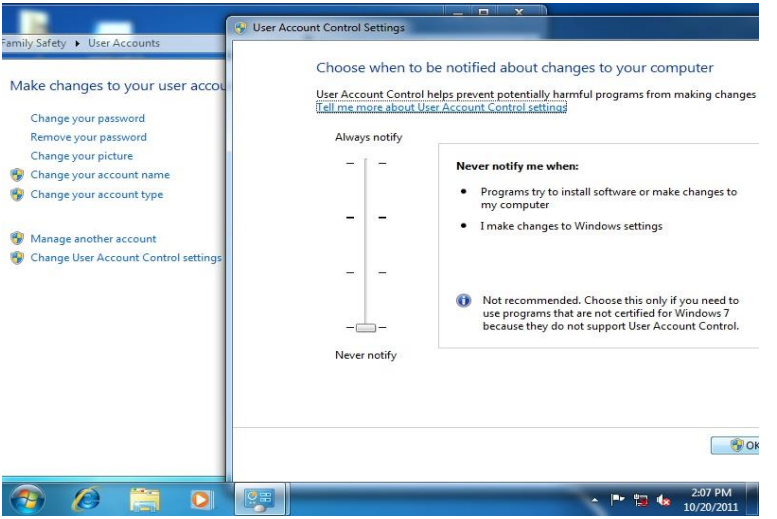
Step 7 – Install USB 3.0 Driver (Windows 7/8.1 Only)

1. Open the **Step5 - USB3.0** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

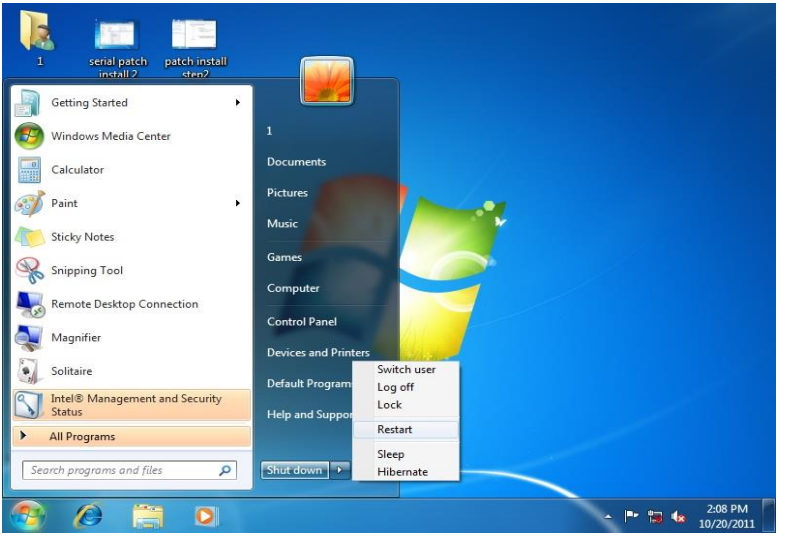
Step 8 – Install Serial Port Drivers

For Windows 7:

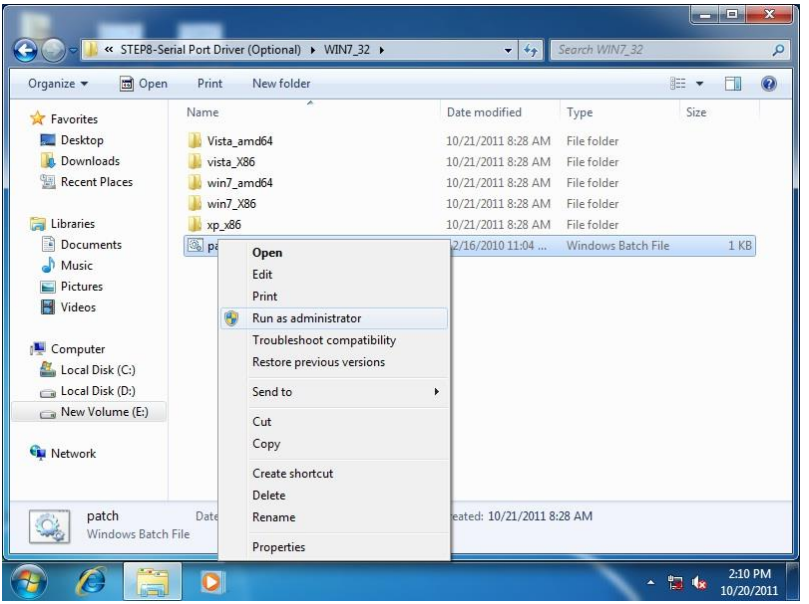
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator

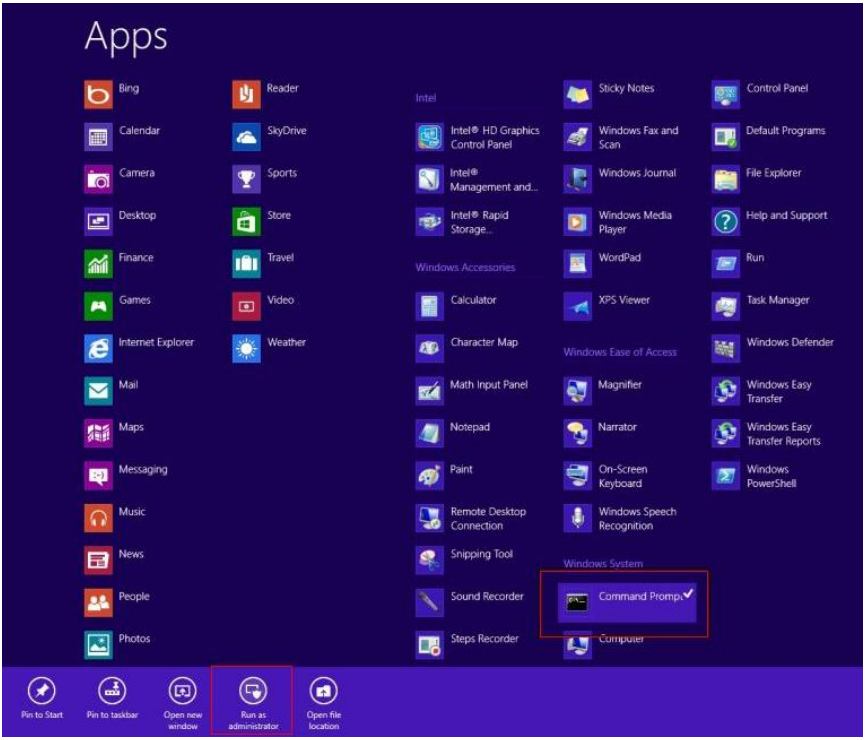


3. Run patch.bat as administrator


« STEP8-Serial Port Driver (Optional) ▸ WIN7_32 ▸
Search WIN7_32
Organize
Open
Print
New folder
Favorites
Desktop
Downloads
Recent Places
Libraries
Documents
Music
Pictures
Videos
Computer
Local Disk (C:)
Local Disk (D:)
New Volume (E:)
Network
Name
Date modified
Type
Size
Vista_amd64 10/21/2011 8:28 AM File folder
vista_X86 10/21/2011 8:28 AM File folder
win7_amd64 10/21/2011 8:28 AM File folder
win7_X86 10/21/2011 8:28 AM File folder
xp_x86 10/21/2011 8:28 AM File folder
Windows Batch File 1 KB
Open
Edit
Print
Run as administrator
Troubleshoot compatibility
Restore previous versions
Send to
Cut
Copy
Create shortcut
Delete
Rename
Properties
patch
Windows Batch File
eated: 10/21/2011 8:28 AM
2:10 PM
10/20/2011

For Windows 8:

1. Open the Apps Screen, right click on the **Command Prompt** tile and select **Run as Administrator**



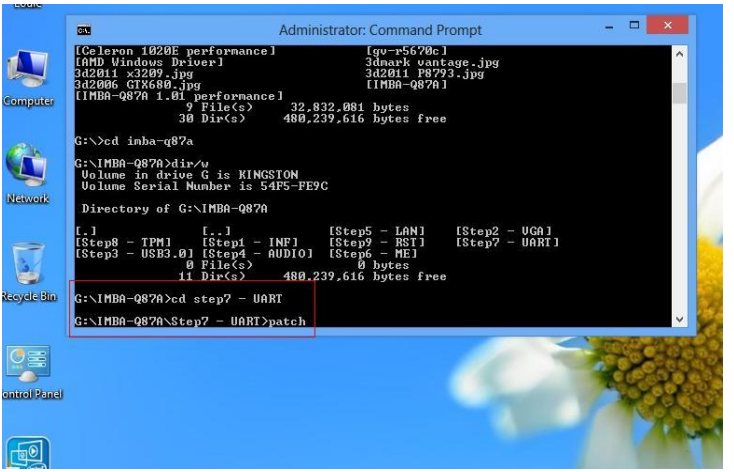
2. Locate the file in command prompt by using the command:

```
cd [file path]
```

For example, if you saved the driver to C:\ABC then enter the following:

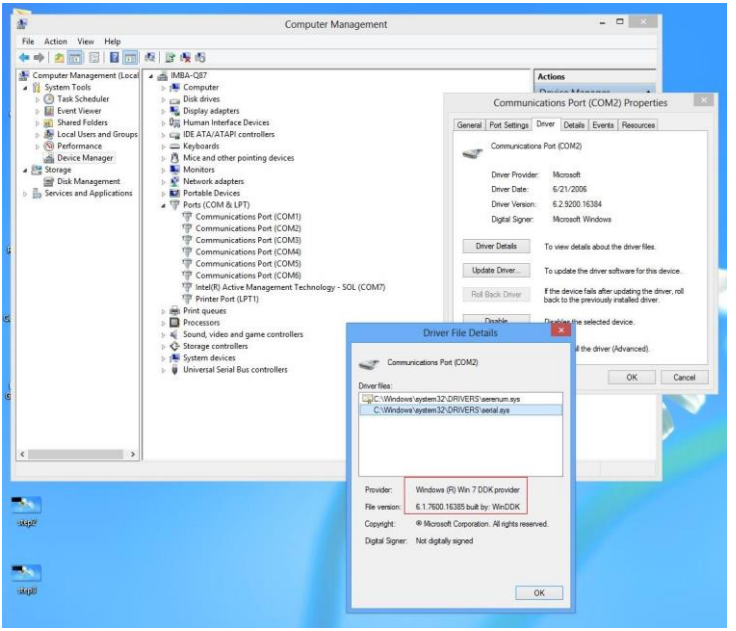
```
cd c:\ABC
```

3. Enter `patch.bat` into the command line to install the drivers:



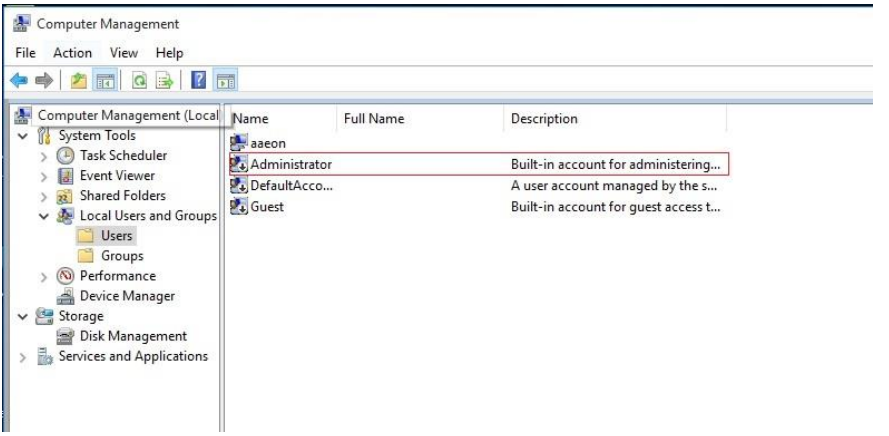
4. Reboot after installation completes.

5. To confirm the installation, go to Device Manager, expand the Ports (COM & LPT) tree and double click on any of the COM ports to open its properties. Go to the Driver tab, select Driver Details and click on **serial.sys**. You should see its provider as **Windows (R) Win 7 DDK Provider**.

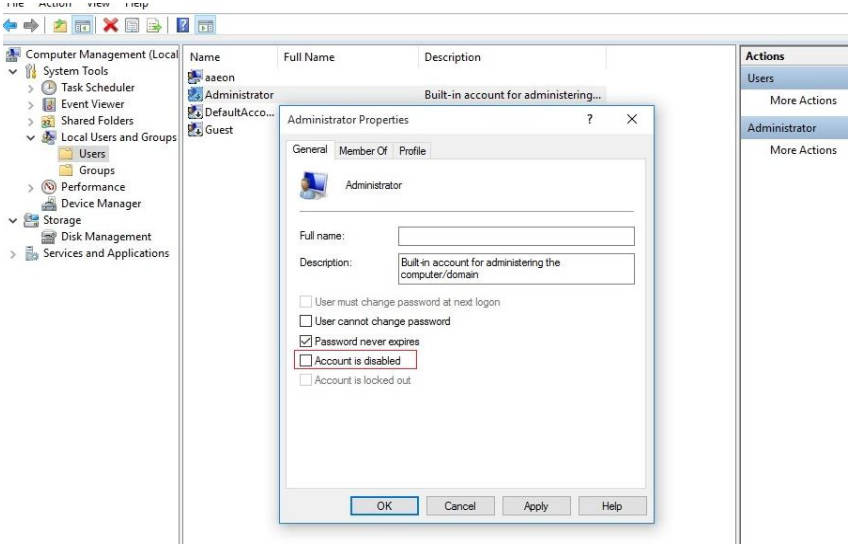


For Windows 10:

1. You will need administrator rights to install the drivers. To set them, first go to **Computer Management** in **Control Panel** and double-click on **Administrator**

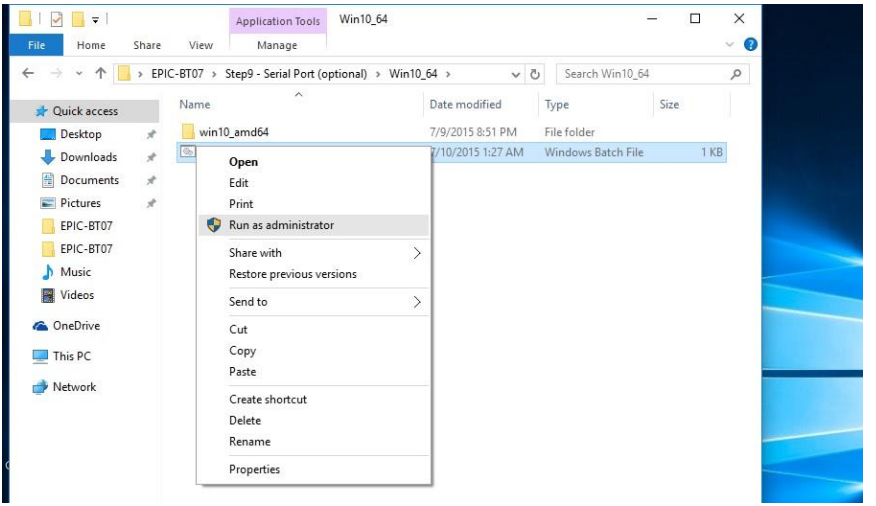


2. In the dialog box, **uncheck** the **Account is disabled** option to enable administrator account.



3. Restart and sign in as the administrator (not password-protected by default)

4. Go back to the Windows 10 Serial Port drivers directory and **run patch.bat as administrator.**



4.2 Note on EHCI

With the EHCI controller no longer available on the Intel® Pentium® N3000 platforms, it is recommended to install Windows 7 through a SATA bus, i.e., SATA DVD-ROM. For input devices, PS/2 keyboard and mouse should be used.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s *Pulse width is must longer then 16ms.*
Signal Polarity	0x05	2	0	0: low active 1: high active *Must set this bit to 0*
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse *Must set this bit to 1*
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*****************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr         0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
      #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
      #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg        0x05   // Timer register
      #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
      #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
      #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
      #define   PolarityVal    0x00     // Low active for WDTRST#
      #define   UnitBit        0x03     // Unit for timer (Bit3)
      #define   ModeBit        0x04     // WDTRST# mode (Bit4)
      #define   ModeVal        0x01     // 0:level 1: pulse
      #define   EnableBit      0x05     // WDT timer enable (Bit5)
      #define   EnableVal      0x01     // 1: enable
      #define   StatusBit      0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*****************************************************************************

*****************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig(Counter, Unit);

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*****************************************************************************
```

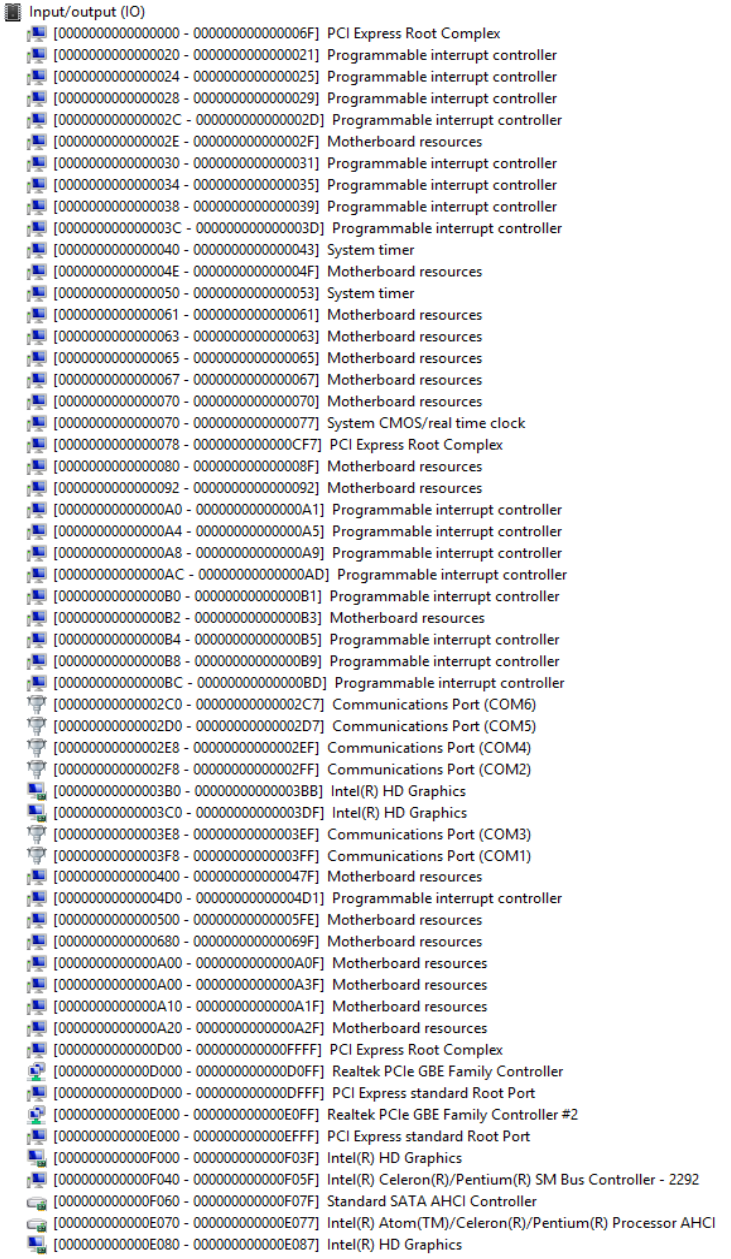
```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
        // Disable WDT counting
        WDTEnableDisable(0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
        If (Value == 1)
            WDTSetBit(TimerReg, EnableBit, 1);
        else
            WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
        // Watchdog Timer counter setting
        WDTWriteByte(CounterReg, Counter);
      // WDT counting unit setting
      WDTSetBit(TimerReg, UnitBit, Unit);
      // WDT output mode set to pulse
      WDTSetBit(TimerReg, ModeBit, ModeVal);
      // WDT output mode set to active low
      WDTSetBit(TimerReg, PolarityBit, PolarityVal);
      // WDT output pulse width is 25ms
      WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
        // Watchdog WDTRST# Enable
        WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
      WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************
```

```
*************************************************************************
VOID   WDTWriteByte(byte Register, byte Value){
       IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
       return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
       byte TmpValue;

       TmpValue = WDTReadByte(Register);
       TmpValue &= ~(1 << Bit);
       TmpValue |= Val << Bit;
       WDTWriteByte(Register, TmpValue);
}

*************************************************************************
```

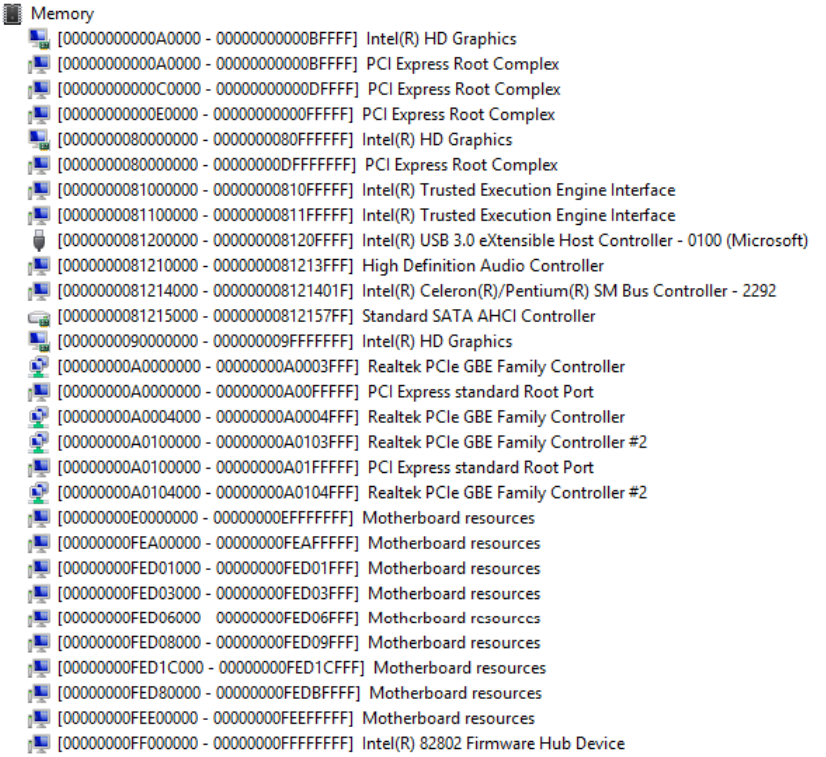
Appendix B

I/O Information

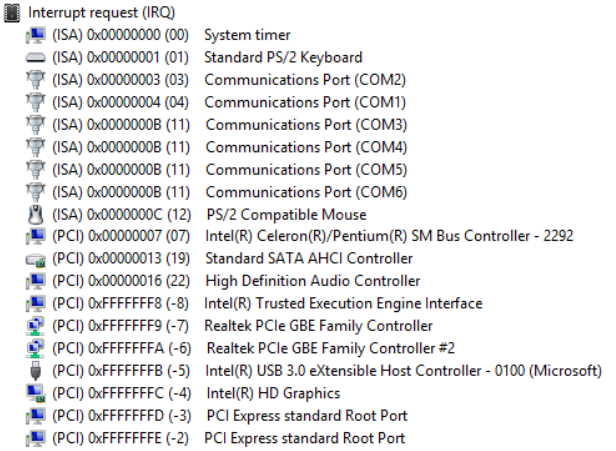
B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart



Appendix C

Digital I/O Ports

C.1 Electrical Specifications for Digital I/O Ports

Table 1 : Digital Input/Output Pin Electrical Specification						
Pin	Type	Input Threshold Voltage		Output Voltage		Note
		Low	High	Low	High	
DIO0	I/O	0.8	2.0	0	5	
DIO1	I/O	0.8	2.0	0	5	
DIO2	I/O	0.8	2.0	0	5	
DIO3	I/O	0.8	2.0	0	5	
DIO4	I/O	0.8	2.0	0	5	
DIO5	I/O	0.8	2.0	0	5	
DIO6	I/O	0.8	2.0	0	5	
DIO7	I/O	0.8	2.0	0	5	

Note: All DIO pins are 5V tolerant in input mode.

C.2 DI/O Programming

GENE-BSW5 utilizes FINTEK F81801U chipset as its Digital I/O controller. Below are the procedures to complete its configuration and the AAEON initial DI/O program is also attached, based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode

(2) Modify the data of configuration registers

(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

C.3 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 3 : Digital Input/Output relative register table				
	LDN	Register	Bit	Note
GPIO0 Direction	0x06	0x88	0	0:input, 1: output
GPIO1 Direction	0x06	0x88	1	
GPIO2 Direction	0x06	0x88	2	
GPIO3 Direction	0x06	0x88	3	
GPIO4 Direction	0x06	0x88	4	
GPIO5 Direction	0x06	0x88	5	
GPIO6 Direction	0x06	0x88	6	
GPIO7 Direction	0x06	0x88	7	
GPIO0 Output Level	0x06	0x89	0	0:low, 1: high
GPIO1 Output Level	0x06	0x89	1	
GPIO2 Output Level	0x06	0x89	2	
GPIO3 Output Level	0x06	0x89	3	
GPIO4 Output Level	0x06	0x89	4	
GPIO5 Output Level	0x06	0x89	5	
GPIO6 Output Level	0x06	0x89	6	
GPIO7 Output Level	0x06	0x89	7	
GPIO0 Status	0x06	0x8A	0	0:low, 1: high
GPIO1 Status	0x06	0x8A	1	
GPIO2 Status	0x06	0x8A	2	
GPIO3 Status	0x06	0x8A	3	
GPIO4 Status	0x06	0x8A	4	
GPIO5 Status	0x06	0x8A	5	
GPIO6 Status	0x06	0x8A	6	
GPIO7 Status	0x06	0x8A	7	

C.4 Digital I/O Sample Program

```
//************************************************************************
// SuperIO relative definition (Please reference to Table 2)
#define   SIOIndex   0x2E
#define   SIOData    0x2F
#define   DIOLDN     0x06
IOWriteByte(byte IOPort, byte Value);
IOReadByte(byte IOPort);
// DIO relative definition (Please reference to Table 3)
#define   DirReg_L          0x88          // 0:input, 1: output
#define   DirReg_H          0x80          // 0:input, 1: output
      #define   InputPin      0x00
      #define   OutputPin     0x01
#define   OutputReg_L       0x89          // 0:low, 1: high
#define   OutputReg_H       0x81          // 0:low, 1: high
#define   StatusReg_L       0x8A          // 0:low, 1: high
#define   StatusReg_H       0x82          // 0:low, 1: high
      #define   PinLow        0x00
      #define   PinHigh       0x01
#define   Pin0Bit       0x00
#define   Pin1Bit       0x01
#define   Pin2Bit       0x02
#define   Pin3Bit       0x03
#define   Pin4Bit       0x04
#define   Pin5Bit       0x05
#define   Pin6Bit       0x06
#define   Pin7Bit       0x07

//************************************************************************
```

```
*****************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //      Example, Read Digital I/O Pin 3 status
        // Output :
        //      InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(Pin3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //      Example, Set Digital I/O Pin 2 to high level
       AaeonSetOutputLevel(Pin2Bit, PinHigh);
}
*****************************************************************************

*****************************************************************************
Boolean   AaeonReadPinStatus(byte PinBit){
       Boolean PinStatus ;
       PinStatus = SIOBitRead(DIOLDN, StatusReg_L, PinBit);
       Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte PinBit, byte Value){
       ConfigDioMode(PinBit, OutputPin);
       SIOBitSet(DIOLDN, OutputReg_L, PinBit, Value);
}
*****************************************************************************
```

```
*****************************************************************************VOID
SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigDioMode(byte PinBit, byte Mode){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(DIOLDN);
        IOWriteByte(SIOIndex, DirReg_L);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (Mode << PinBit);
        IOWriteByte(SIOData, DirReg_L);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix D

Notes for Users

D.1 Notes for Users

Please observe the following items to ensure optimal performance:

1. To achieve SATA III (6.0 Gbps) transfer speeds, please use a SATA III SSD with a SATA III cable not longer than 60 cm in length.

Appendix E

Mating Connectors

E.1 List of Mating Connectors and Cables

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	External AUX Power and PS_ON#	JST	PHR-6	N/A	N/A
CN2	+5Vout Connector	JST	PHR-2	2 Pins For SATA HDD Power	1702150155
CN3	LVDS Inverter Connector	JST	PHR-5	N/A	N/A
CN4	External +5VSB Power Input and PS_ON#	JST	XHP-3	ATX Cable	170220020B
CN5	SATA Connector	Molex	887505318	SATA Cable	1709070500
CN6	+12V Vin Connector	Molex	19211-0003	Power Cable	170204010R
CN7	LVDS Inverter Connector	JST	PHR-5	N/A	N/A
CN8	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN9	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN10	Audio Connector	Molex	51021-1000	Audio Cable	1709100254
CN11	COM Port #3 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN12	LPT Connector	Molex	51110-2650	Parallel Port Cable	1701260200
CN13	COM Port #4 Connector	Molex	51021-0900	Serial Port Cable	1701090150

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN14	LPC Connector	JST	SHR-12V-S-B	AAEON LPC Cable	1703120130
CN15	COM Port #3 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN16	COM Port #4 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN17	COM Port #3 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN19	USB Port #3 Connector	Molex	51021-0500	USB Cable	1700050207
CN20	USB Port #2 Connector	Molex	51021-0500	USB Cable	1700050207
CN21	USB Port #2 Connector	Molex	51021-0500	USB Cable	1700050207
CN22	COM Port #4 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN23	Touch Screen Connector	JST	SHR-9V-S-B	N/A	N/A
CN24	PS/2 KB/MS Connector	JST	PHDR-06VS	PS/2 KB/MS Cable	1700060152
CN25	CPU Fan Connector	Molex	22-01-2035	N/A	N/A
CN31	External RTC Connector	Molex	51021-0200	Battery Cable	175011901M