GENE-APL6

3.5" Subcompact Board

User's Manual 3rd Ed

Last Updated: June 13, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● GENE-APL6 with heat spreader	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	3.5'' SubCompact Board
CPU	Intel® Pentium® N4200/ Celeron® N3350 Processor SoC
CPU Frequency	up to 2.5GHz
Chipset	Intel® Pentium® N4200/ Celeron® N3350 Processor SoC
Memory Type	DDR3L 1866MHz, SODIMM x 1
Max. Memory Capacity	Up to 8GB
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+9~36V or +12V
Power Supply Type	AT/ ATX
Power Consumption (Typical)	Intel® N4200, DDR3L 1600MHz 8G, 1.55A@ +12V
Dimension (L x W)	5.75" x 4" (146mm x 101.7mm)
Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 81°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	128,793

System

Certification	CE/FCC

I/O

Ethernet	Intel® i210/I211, 10/100/1000Base-TX, RJ-45 x 2
Audio	High Definition Audio Interface
USB Port	USB 3.0 x 2 USB 2.0 x 2
Serial Port	RS-232 x 2 , RS-232/422/485 x 2
Parallel Port	SPP/EPP/ECP x 1 (Option, Shared with DIO)
HDD Interface	SATA 3.0 x 1 +5V SATA power connector x 1
FDD Interface	—
SSD	eMMC 16G/32G/64G (optional)
Expansion Slot	Mini Card x 1 (Full-size) mSATA x 1 (Half-size)
DIO	8-bit
SIM	x 1 (uSIM)
TPM	TPM 2.0 x 1 (option)
Touch	x 1 (option)

Display

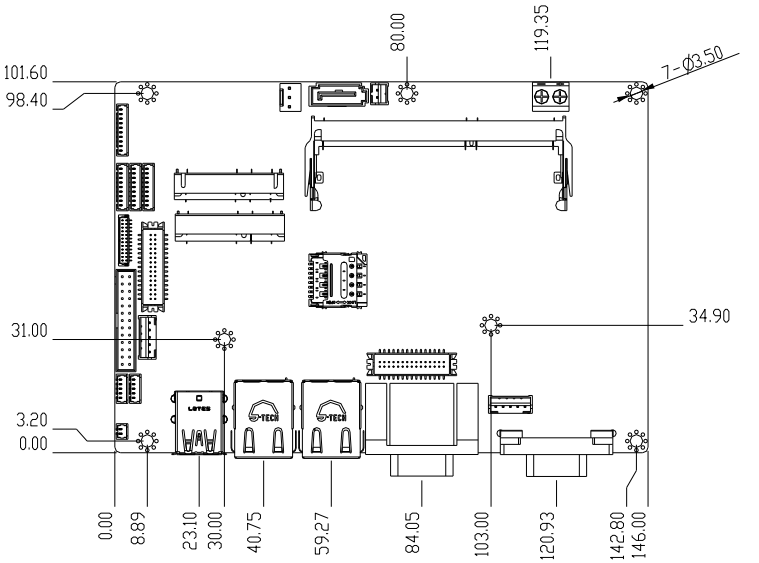
VGA/LCD Controller	Intel® Pentium® N4200/ Celeron® N3350 Processor SoC
Video Output	LVDS, LVDS2, VGA (HDMI is option, co-layout with LVDS2)
Backlight Inverter Supply	Yes

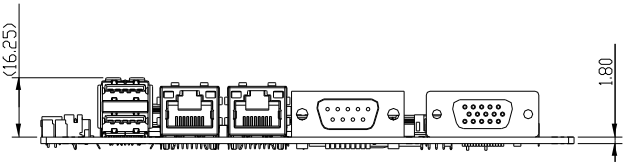
Chapter 2

Hardware Information

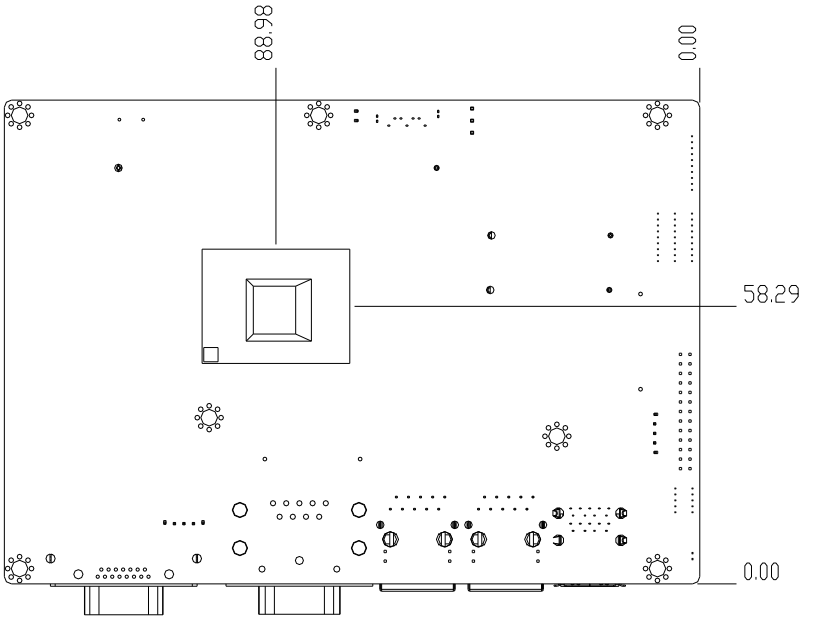
2.1 Dimensions

Component Side

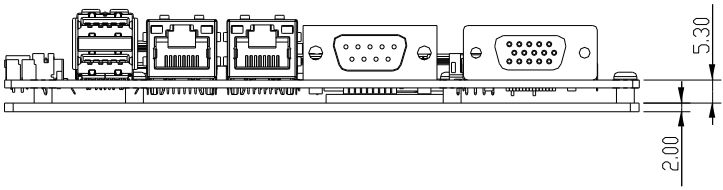


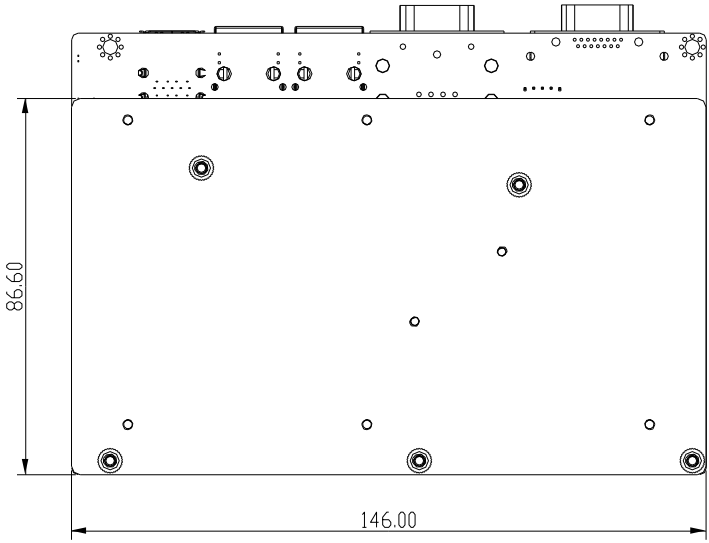


Solder Side



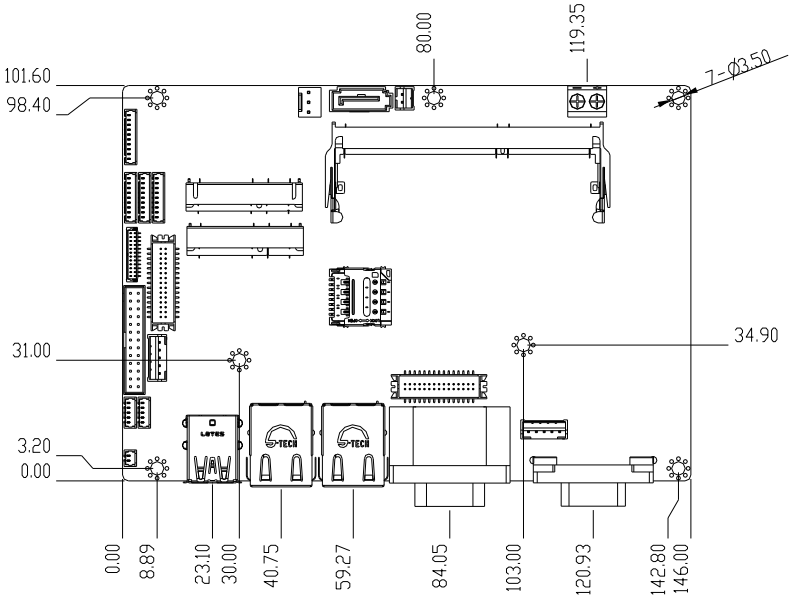
With Heat Spreader

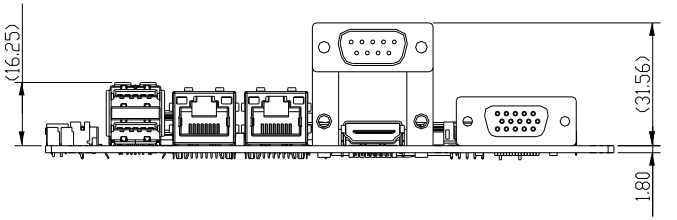




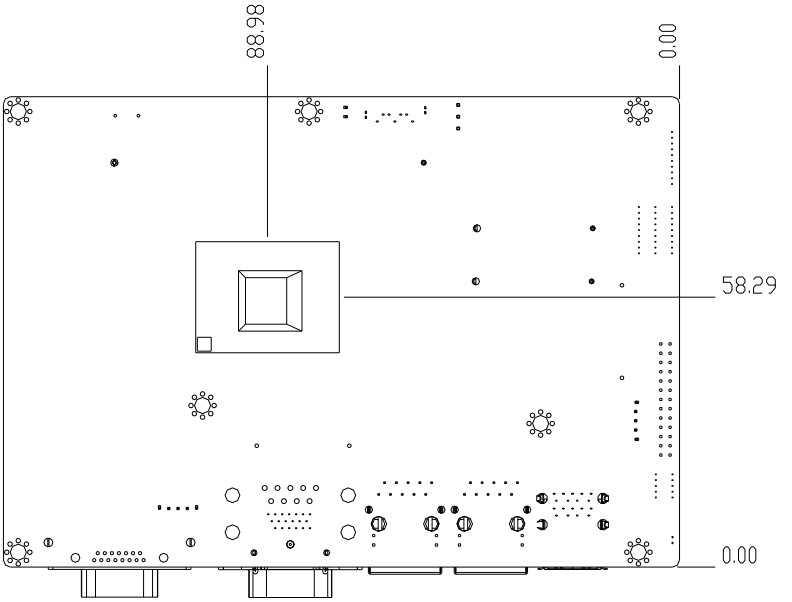
2.1.1 Dimensions (Optional HDMI SKU)

Component Side

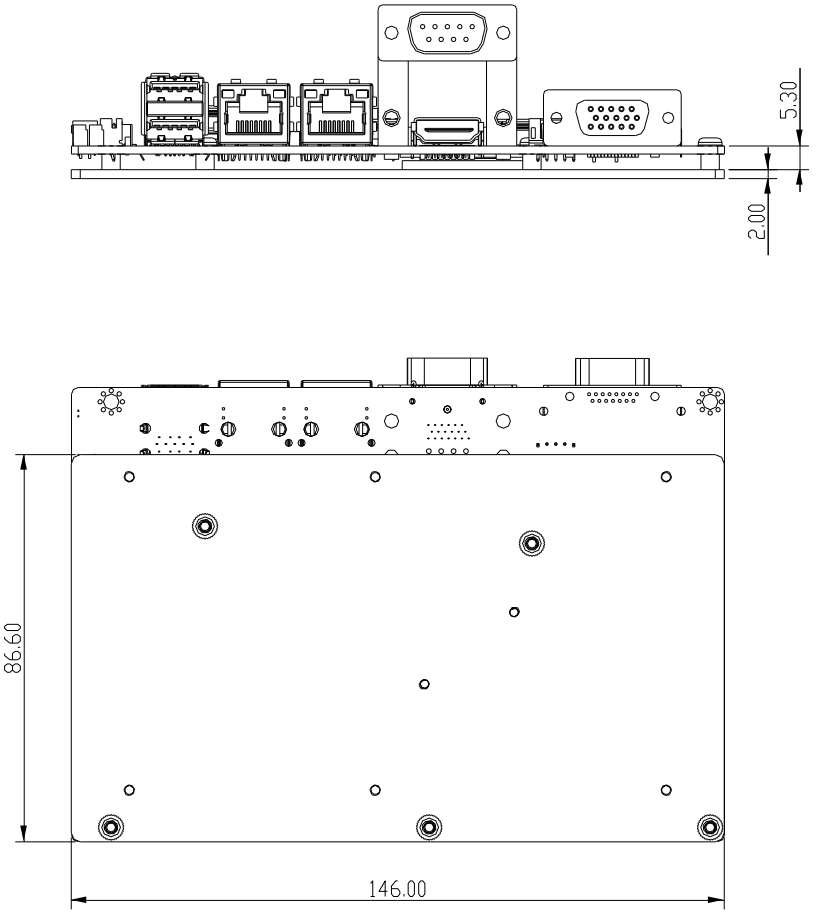




Solder Side

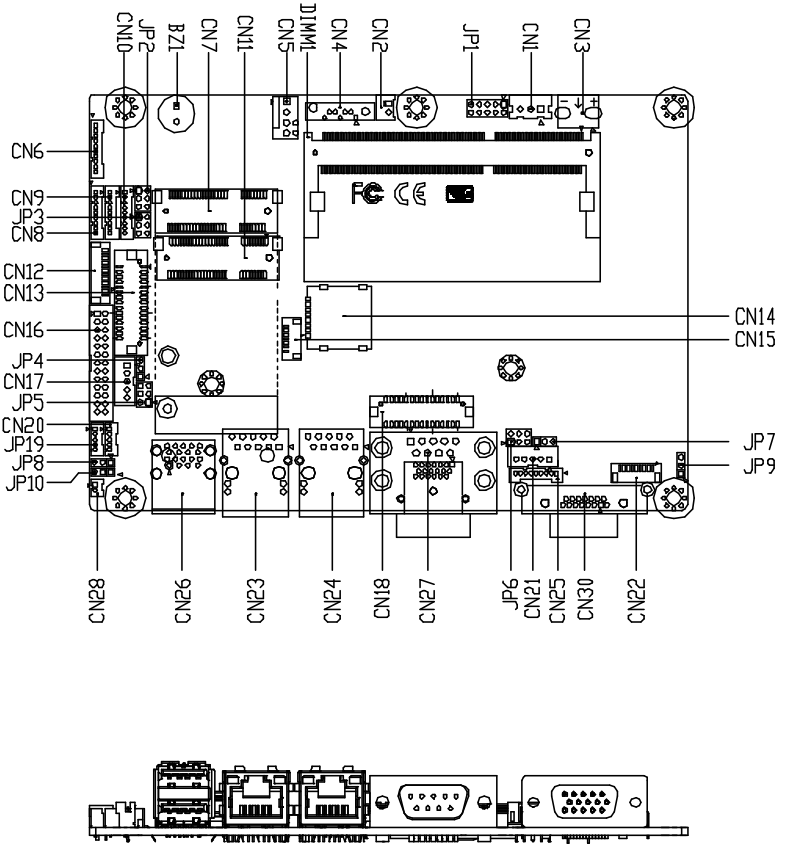


With Heat Spreader



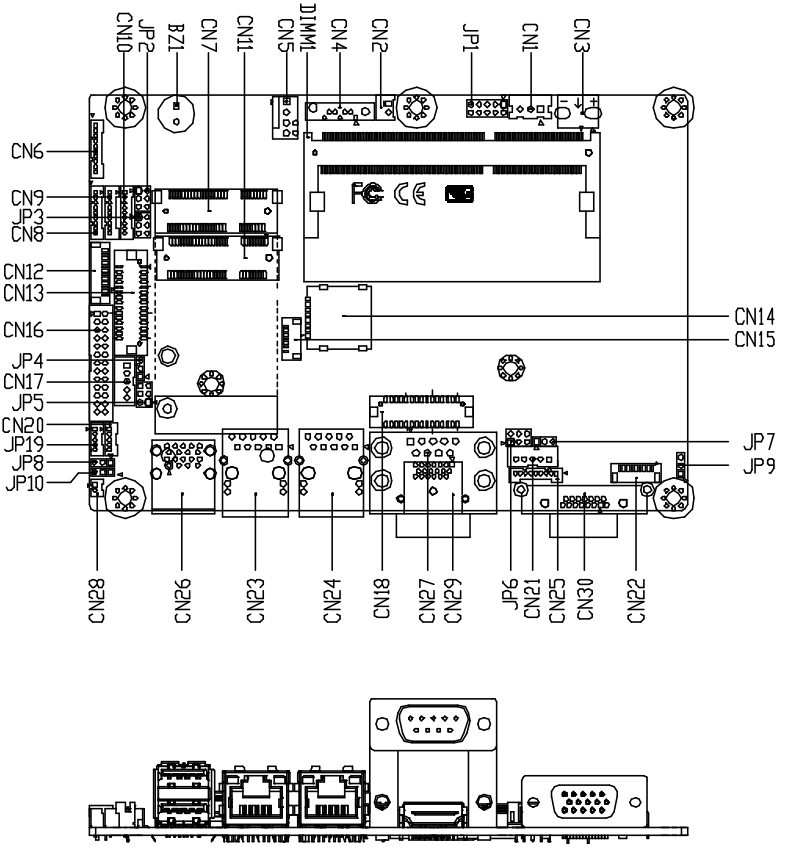
2.2 Jumpers and Connectors

Component Side



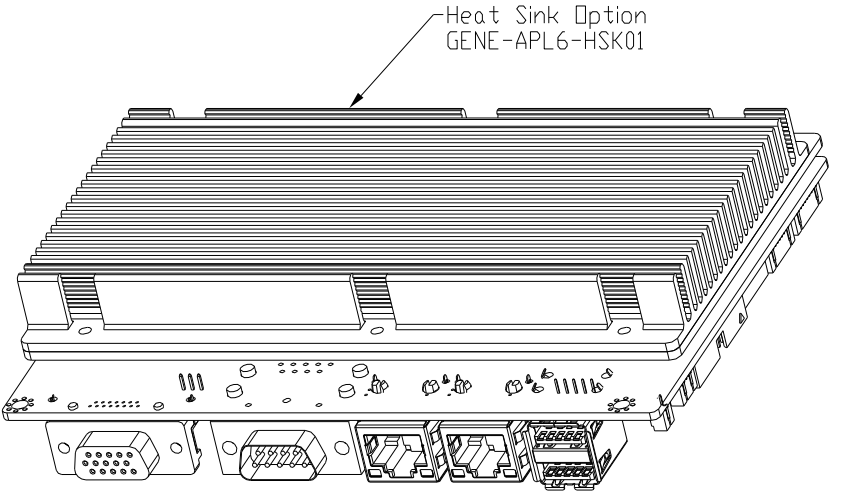
2.2.1 Jumpers and Connectors (Optional HDMI SKU)

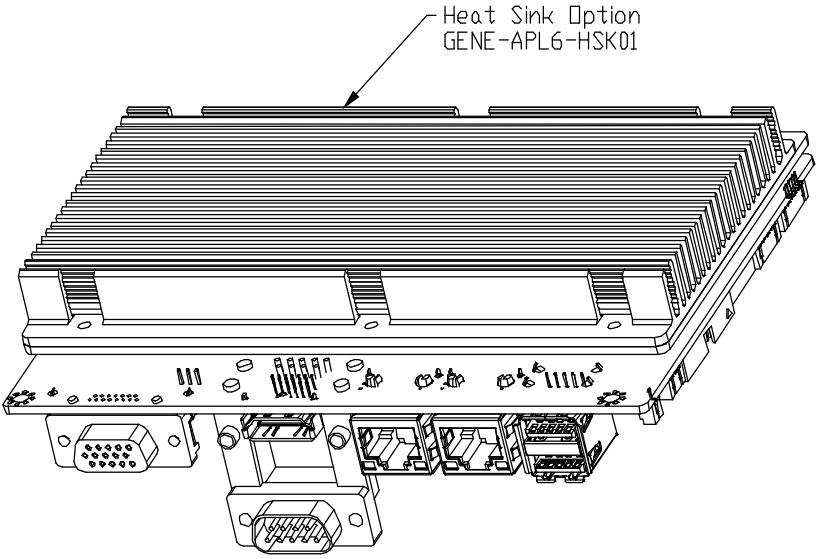
Component Side



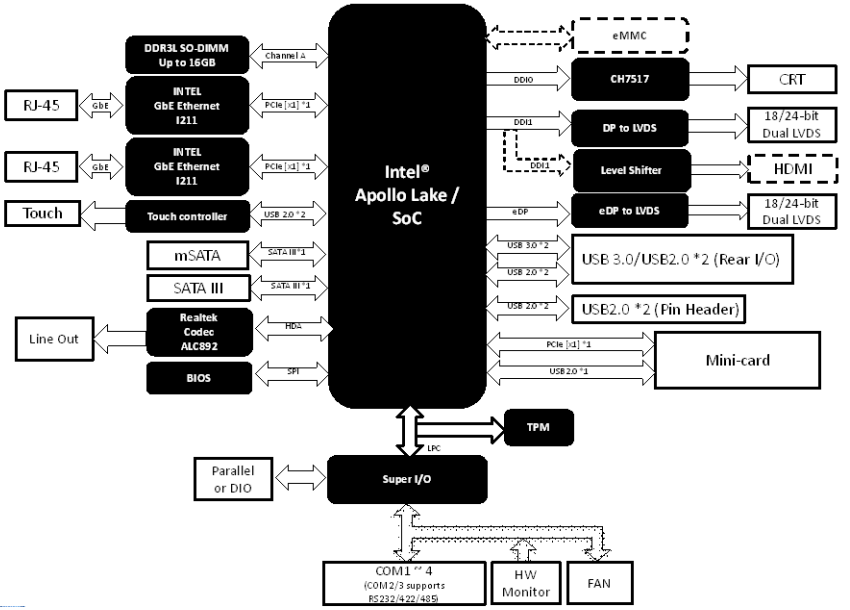
2.3 Assembly Options

Optional accessory for GENE-APL6-HSK01





2.4 Block Diagram

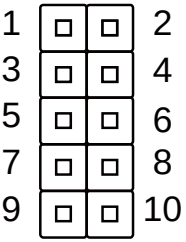

DDR3L SO-DIMM
Up to 16GB
Channel A
RJ-45
GbE
INTEL
GbE Ethernet
I211
PCIe [x1] *1
RJ-45
GbE
INTEL
GbE Ethernet
I211
PCIe [x1] *1
Touch
Touch controller
USB 2.0 *2
mSATA
SATA III *1
SATA III
SATA III *1
Line Out
Realtek
Codec
ALC892
HDA
BIOS
SPI
Intel®
Apollo Lake /
SoC
eMMC
DDI0
CH7517
CRT
DDI1
DP to LVDS
18/24-bit
Dual LVDS
DDI3
Level Shifter
HDMI
eDP
eDP to LVDS
18/24-bit
Dual LVDS
USB 3.0 *2
USB 2.0 *2
USB 3.0/USB2.0 *2 (Rear I/O)
USB 2.0 *2
USB2.0 *2 (Pin Header)
PCIe [x1] *1
USB 2.0 *1
Mini-card
TPM
LPC
Parallel
or DIO
Super I/O
COM1 ~ 4
(COM2/3 supports
RS232/422/485)
HW
Monitor
FAN

2.4 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

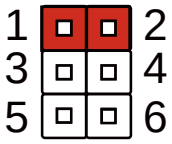
Label	Function
JP1	Front Panel Connector
JP2	COM2 Pin8 Function Selection
JP3	COM3 Pin8 Function Selection
JP4	LVDS Port2 Backlight Lightness Control Mode Selection
JP5	LVDS Port2 Backlight Inverter VCC Selection
JP6	LVDS Port1 Backlight Inverter VCC Selection
JP7	LVDS Port2 Backlight Lightness Control Mode Selection
JP8	Auto Power Button Enable/Disable Selection
JP9	Touch Screen 4/5/8-wire Mode Selection
JP10	Clear CMOS Jumper

2.4.1 Front Panel Connector (JP1)

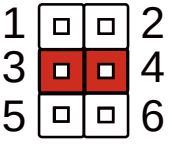


Pin	Pin Name	Pin	Pin Name
1	PWR_BTN-	2	PWR_BTN+
3	HDD_LED-	4	HDD_LED+
5	SPEAKER-	6	SPEAKER+
7	PWR_LED-	8	PWR_LED+
9	H/W RESET-	10	H/W RESET+

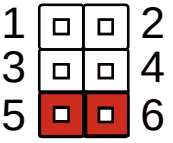
2.4.2 COM2 Pin8 Function Selection (JP2)



+12V

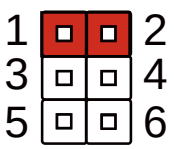


Ring(Default)

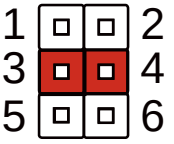


+5V

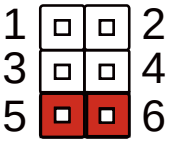
2.4.3 COM3 Pin8 Function Selection (JP3)



+12V

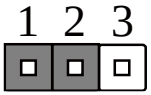


Ring(Default)

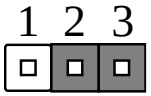


+5V

2.4.4 LVDS Port2 Backlight Lightness Control Mode Selection (JP4)

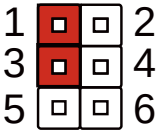


VR Mode (Default)

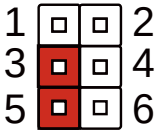


PWM Mode

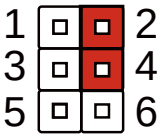
2.4.5 VDS Port2 Backlight Inverter VCC Selection (JP5)



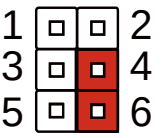
+12V



+5V (Default)

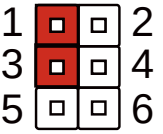


+3.3V (Default)

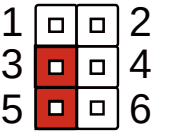


+5V

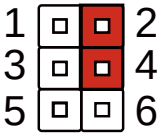
2.4.6 VDS Port1 Backlight Inverter VCC Selection (JP6)



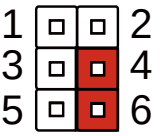
+12V



+5V (Default)

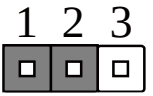


+3.3V (Default)

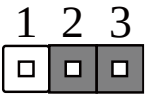


+5V

2.4.7 LVDS Port1 Backlight Lightness Control Mode Selection (JP7)

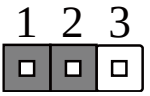


VR Mode (Default)

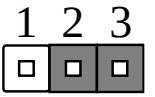


PWM Mode

2.4.8 Auto Power Button Enable/Disable Selection (JP8)



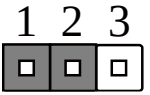
Disable/ATX



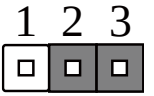
Enable/AT (Default)

※ When disabled, the power button of JP5 (1-2) will be used to power on the system

2.4.9 Touch Screen 4,5,8 Wire Selection (JP9)

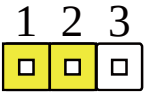


4/8 Wires Mode (Default)

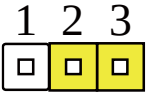


5 Wires Mode

2.4.10Clear CMOS Jumper (JP10)



Normal (Default)



Clear CMOS

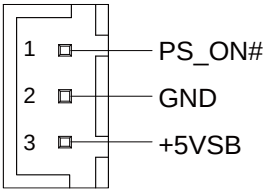
2.5 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	External +5VSB Input
CN2	+5V Output for SATA HDD
CN3	External Power Input
CN4	SATA Port
CN5	CPU FAN (Optional)
CN6	Audio I/O Port
CN7	Mini-Card Slot (Full-Size)
CN8	COM Port 2 RS232/422/485
CN9	COM Port 3 RS232/422/485
CN10	COM Port 4
CN11	m-SATA A lot (Half size)
CN12	LPC Port
CN13	LVDS Port2
CN14	Micro SIM Card Socket
CN15	SPI Debug Port
CN16	LPT Port or Digital I/O Port
CN17	LVDS Port2 Inverter / Backlight Connector
CN18	LVDS Port1
CN19	USB 2.0 Port 4
CN20	USB 2.0 Port 5
CN21	LVDS Port1 Inverter / Backlight Connector
CN22	Touch Screen Connector (Optional)
CN23	LAN (RJ-45) Port1

Label	Function
CN24	LAN (RJ-45) Port2
CN25	COM Port 1 (Wafer, Optional)
CN26	USB3.0 Port 0 / Port 1
CN27	COM Port 1(D-SUB 9)
CN28	Battery CONN
CN29	HDMI CONN
CN30	VGA Port
DIMM1	DDR3L SO-DIMM Slot

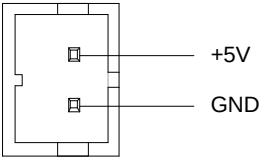
2.5.1 External +5VSB Input (CN1)



Pin	Pin Name	Signal Type	Signal level
1	PS_ON#	OUT	+5V
2	GND	GND	
3	+5VSB	PWR	+5V

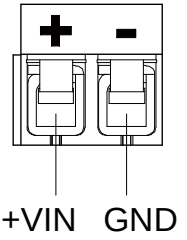
※ Since every power supply discharge design is different, we recommend restarting 3 seconds after powering off to make sure ATX power is fully discharged. Or, make sure 5V standby power has been discharged under 2V.

2.5.2 +5V Output for SATA HDD (CN2)



Pin	Pin Name	Signal Type	Signal level
1	+5V	PWR	+5V
2	GND	GND	

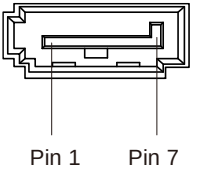
2.5.3 External Power Input (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	+VIN	PWR	9V~36V or 12V
2	GND	GND	

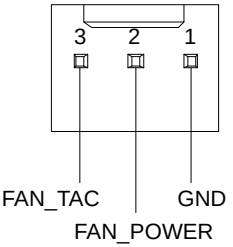
※There are two types of power input, 9V~36V or 12V only, by BOM Change

2.5.4 SATA Port (CN4)



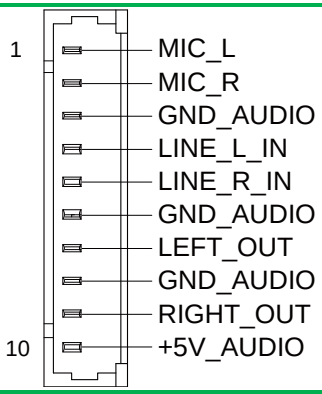
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.5.5 CPU FAN (Optional) (CN5)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	

2.5.6 Audio I/O Port (CN6)



Pin	Pin Name	Signal Type	Signal Level
1	MIC_L	IN	
2	MIC_R	IN	
3	GND_AUDIO	GND	
4	LINE_L_IN	IN	
5	LINE_R_IN	IN	
6	GND_AUDIO	GND	

7	LEFT_OUT	OUT	
8	GND_AUDIO	GND	
9	RIGHT_OUT	OUT	
10	+5V_AUDIO	PWR	+5V

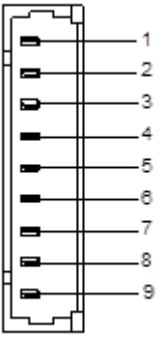
2.5.7 Mini-Card Slot (Full-Size) (CN7)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	
14	UIM_RST	IN	
15	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	

Pin	Pin Name	Signal Type	Signal Level
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.5.8 COM Port 2 (CN8)



RS232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD2	IN	
2	DSR2	IN	
3	RX2	IN	
4	RTS2	OUT	±5V
5	TX2	OUT	±5V
6	CTS2	IN	
7	DTR2	OUT	±5V
8	RI2/+5V/+12V	IN	+5V/+12V
9	GND	GND	

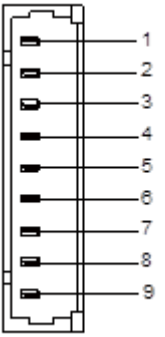
RS485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_ D2-	I/O	±5V
2	NC		
3	RS485_D2+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

RS422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX2-	OUT	±5V
2	NC		
3	RS422_TX2+	OUT	±5V
4	NC		
5	RS422_RX2+	IN	
6	NC		
7	RS422_RX2-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

※ COM2 RS-232/422/485 can be set by BIOS setting. Default is RS-232.

※ Pin 8 function can be set by JP2.

2.5.9 COM Port 3 (CN9)



RS232			
Pin	Pin Name	Signal Type	Signal Level
1	DCD3	IN	
2	DSR3	IN	
3	RX3	IN	
4	RTS3	OUT	±5V
5	TX3	OUT	±5V
6	CTS3	IN	
7	DTR3	OUT	±5V
8	RI2/+5V/+12V	IN	+5V/+12V
9	GND	GND	

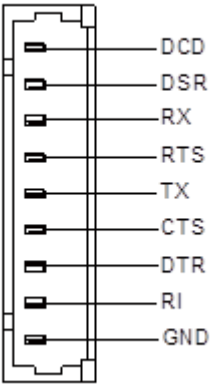
RS485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_ D3-	I/O	±5V
2	NC		
3	RS485_D3+	I/O	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

RS422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX3-	OUT	±5V
2	NC		
3	RS422_TX3+	OUT	±5V
4	NC		
5	RS422_RX3+	IN	
6	NC		
7	RS422_RX3-	IN	
8	NC/+5V/+12V	PWR	+5V/+12V
9	GND	GND	

※ COM3 RS-232/422/485 can be set by BIOS setting. Default is RS-232

※ Pin 8 function can be set by JP2

2.5.10COM Port 4 (CN10)



Pin	Pin Name	Signal Type	Signal Level
1	DCD4	IN	
2	DSR4	IN	
3	RX4	IN	
4	RTS4	OUT	±9V
5	TX4	OUT	±9V
6	CTS4	IN	
7	DTR4	OUT	±9V
8	RI4	IN	
9	GND	GND	

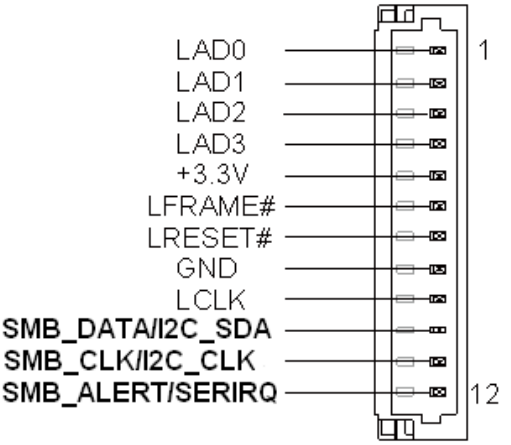
2.5.11 mSATA Slot (Half-Size) (CN11)

Pin	Pin Name	Signal Type	Signal Level
1	NC		
2	+3.3V	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	NC		
7	NC		
8	NC		
9	GND	GND	
10	NC		
11	NC		
12	NC		
13	NC		
14	NC		
15	GND	GND	
16	NC		
17	NC		
18	GND	GND	
19	NC		
20	NC		
21	GND	GND	
22	NC		
23	SRXP_PRXN	DIFF	

24	+3.3V	PWR	+3.3V
25	SRXN_PRXP	DIFF	
26	GND	GND	
27	GND	GND	
28	NC		
29	GND	GND	
30	NC		
31	STXN_PTXN	DIFF	
32	NC		
33	STXP_PTXP	DIFF	
34	GND	GND	
35	GND	GND	
36	NC		
37	GND	GND	
38	NC		
39	+3.3V	PWR	+3.3V
40	GND	GND	
41	+3.3V	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	NC		

49	NC		
50	GND	GND	
51	NC		
52	+3.3V	PWR	+3.3V

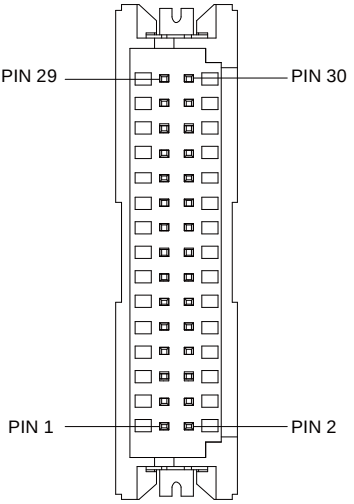
2.5.12LPC Port (CN12)



Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	

10	SMB_DATA/I2C_SDA	I/O	
11	SMB_CLK/I2C_CLK	OUT	
12	SMB_ALERT/SERIRQ	IN	+3.3V

2.5.13 LVDS Port2 (CN13)

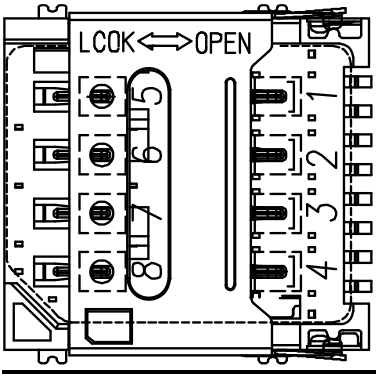


※ LVDS LCD_PWR2 can be set to +3.3V or +5V by JP5

Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE2	OUT	
2	BKL_CONTROL2	OUT	
3	LCD_PWR2	PWR	+3.3V/+5V
4	GND	GND	
5	LVDS2_A_CLK-	DIFF	

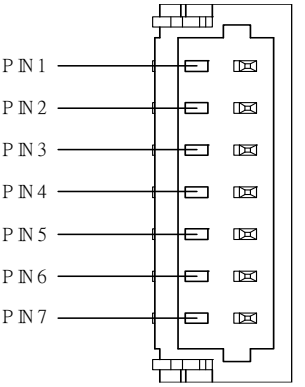
6	LVDS2_A_CLK+	DIFF	
7	LCD_PWR2	PWR	+3.3V/+5V
8	GND	GND	
9	LVDS2_DA0-	DIFF	
10	LVDS2_DA0+	DIFF	
11	LVDS2_DA1-	DIFF	
12	LVDS2_DA1+	DIFF	
13	LVDS2_DA2-	DIFF	
14	LVDS2_DA2+	DIFF	
15	LVDS2_DA3-	DIFF	
16	LVDS2_DA3+	DIFF	
17	DDC2_DATA	I/O	+3.3V
18	DDC2_CLK	I/O	+3.3V
19	LVDS2_DB0-	DIFF	
20	LVDS2_DB0+	DIFF	
21	LVDS2_DB1-	DIFF	
22	LVDS2_DB1+	DIFF	
23	LVDS2_DB2-	DIFF	
24	LVDS2_DB2+	DIFF	
25	LVDS2_DB3-	DIFF	
26	LVDS2_DB3+	DIFF	
27	LCD_PWR2	PWR	+3.3V/+5V
28	GND	GND	
29	LVDS2_B_CLK-	DIFF	
30	LVDS2_B_CLK+	DIFF	

2.5.14Micro SIM Card Socket (CN14)



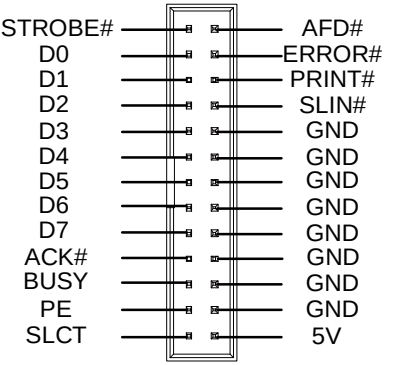
Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	NC		
5	GND	GND	
6	UIM_VPP	PWR	
7	UIM_DATA	I/O	
8	NC		

2.5.15 BIOS Debug Port (CN15)



Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

2.5.16LPT Port or Digital I/O Port (CN16)

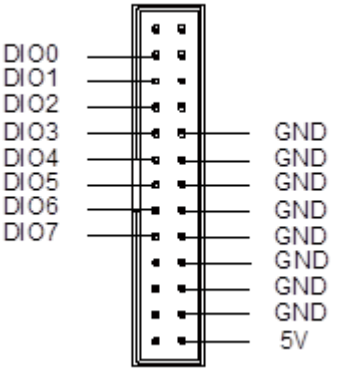


※ LPT or Digital I/O function can be selected by BIOS setting.

Default is LPT port

LPT Port			
Pin	Pin Name	Signal Type	Signal Level
1	STROBE#	IN	
2	AFD#	I/O	
3	PD0	I/O	
4	ERROR#	IN	
5	PD1	I/O	
6	PRINT#	I/O	
7	PD2	I/O	
8	SLIN#	I/O	
9	PD3	I/O	
10	GND	GND	
11	PD4	I/O	

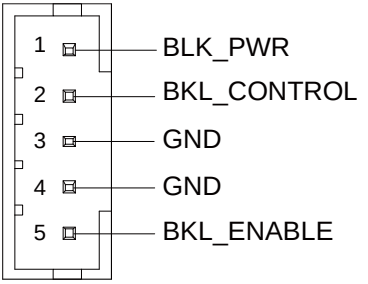
12	GND	GND	
13	PD5	I/O	
14	GND	GND	
15	PD6	I/O	
16	GND	GND	
17	PD7	I/O	
18	GND	GND	
19	ACK#	IN	
20	GND	GND	
21	BUSY	IN	
22	GND	GND	
23	PE	IN	
24	GND	GND	
25	SLCT	IN	
26	5V	PWR	+5V



Digital I/O Port			
Pin	Pin Name	Signal Type	Signal Level
1	NC		
2	NC		
3	DIO0	I/O	+5V
4	NC		
5	DIO1	I/O	+5V
6	NC		
7	DIO2	I/O	+5V
8	NC		
9	DIO3	I/O	+5V
10	GND	GND	
11	DIO4	I/O	+5V
12	GND	GND	
13	DIO5	I/O	+5V
14	GND	GND	
15	DIO6	I/O	+5V
16	GND	GND	

17	DIO7	I/O	+5V
18	GND	GND	
19	NC		
20	GND	GND	
21	NC		
22	GND	GND	
23	NC		
24	GND	GND	
25	NC		
26	5V	PWR	+5V

2.5.17 LVDS Port2 Inverter / Backlight Connector (CN17)

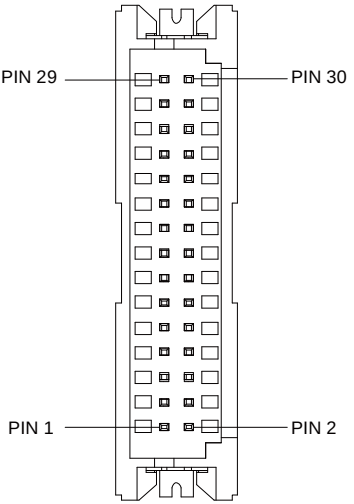


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+5V

※ LVDS2 BKL_PWR can be set to +5V or +12V by JP5

※ LVDS2 BKL_CONTROL can be set by JP4

2.5.18 LVDS Port1 (CN18)

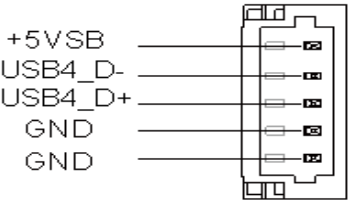


※ LVDS1 LCD_PWR can be set to +3.3V or +5V by JP1.

Pin	Pin Name		Signal Type	Signal Level
1	BKL_ENABLE	OUT		
2	BKL_CONTROL	OUT		
3	LCD_PWR	PWR	+3.3V/+5V	
4	GND	GND		
5	LVDS_A_CLK-	DIFF		
6	LVDS_A_CLK+	DIFF		
7	LCD_PWR	PWR	+3.3V/+5V	
8	GND	GND		
9	LVDS_DA0-	DIFF		
10	LVDS_DA0+	DIFF		
11	LVDS_DA1-	DIFF		
12	LVDS_DA1+	DIFF		

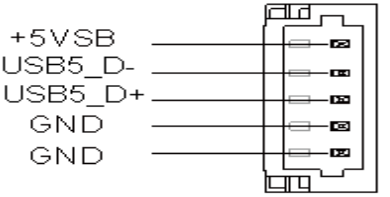
Pin	Pin Name		Signal Type	Signal Level
13	LVDS_DA2-	DIFF		
14	LVDS_DA2+	DIFF		
15	LVDS_DA3-	DIFF		
16	LVDS_DA3+	DIFF		
17	DDC_DATA	I/O	+3.3V	
18	DDC_CLK	I/O	+3.3V	
19	LVDS_DB0-	DIFF		
20	LVDS_DB0+	DIFF		
21	LVDS_DB1-	DIFF		
22	LVDS_DB1+	DIFF		
23	LVDS_DB2-	DIFF		
24	LVDS_DB2+	DIFF		
25	LVDS_DB3-	DIFF		
26	LVDS_DB3+	DIFF		
27	LCD_PWR	PWR	+3.3V/+5V	
28	GND	GND		
29	LVDS_B_CLK-	DIFF		
30	LVDS_B_CLK+	DIFF		

2.5.19USB 2.0 Port 4 (CN19)



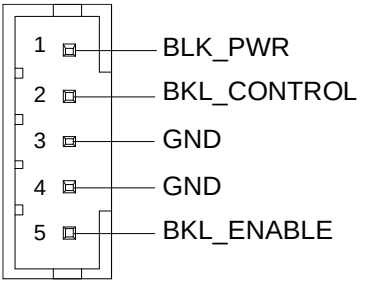
Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.20 USB 2.0 Port 5 (CN20)



Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	GND	GND	

2.5.21LVDS Port1 Inverter / Backlight Connector (CN21)



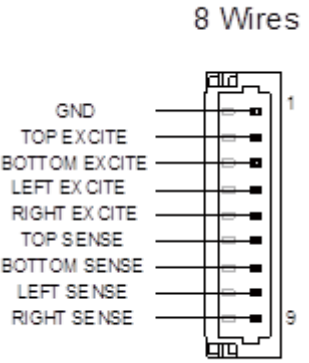
Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V / +12V
2	BKL_CONTROL	OUT	

Pin	Pin Name	Signal Type	Signal Level
3	GND	GND	
4	GND	GND	
5	BKL_ENABLE	OUT	+5V

※ LVDS1 BKL_PWR can be set to +5V or +12V by JP6

※ LVDS1 BKL_CONTROL can be set by JP7

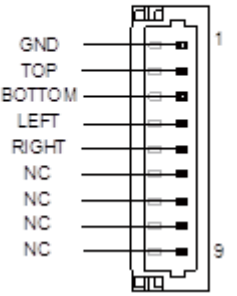
2.5.22 Touch Screen Connector (Optional) (CN22)



8-Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP EXCITE	IN	
3	BOTTOM EXCITE	IN	
4	LEFT EXCITE	IN	
5	RIGHT EXCITE	IN	
6	TOP SENSE	IN	
7	BOTTOM SENSE	IN	

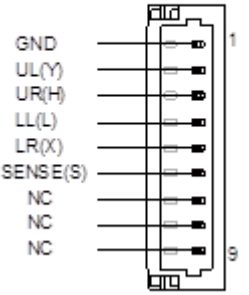
8	LEFT SENSE	IN
9	RIGHT SENSE	IN

4 Wires



4-Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	TOP	IN	
3	BOTTOM	IN	
4	LEFT	IN	
5	RIGHT	IN	
6	NC		
7	NC		
8	NC		
9	NC		

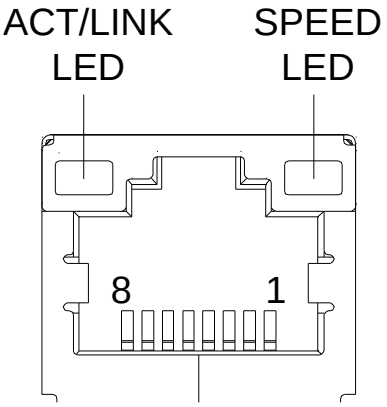
5 Wires



5-Wire			
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	UL(Y)	IN	
3	UR(H)	IN	
4	LL(L)	IN	
5	LR(X)	IN	
6	SENSE(S)	IN	
7	NC		
8	NC		
9	NC		

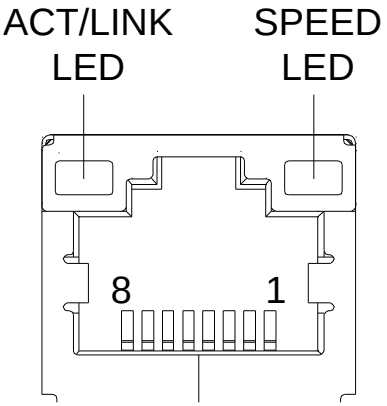
※ Touch mode can be set by BIOS setting

2.5.23 LAN (RJ-45) Port1 (CN23)



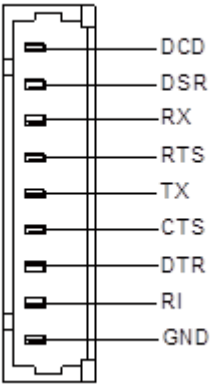
Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.5.24 LAN (RJ-45) Port2 (CN24)



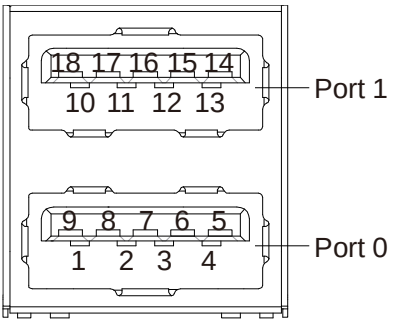
Pin	Pin Name	Signal Type	Signal level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.5.25 COM Port 1 (Wafer, Optional) (CN25)



Pin	Pin Name	Signal Type	Signal Level
1	DCD1	IN	
2	DSR1	IN	
3	RX1	IN	
4	RTS1	OUT	±9V
5	TX1	OUT	±9V
6	CTS1	IN	
7	DTR1	OUT	±9V
8	RI1	IN	
9	GND	GND	

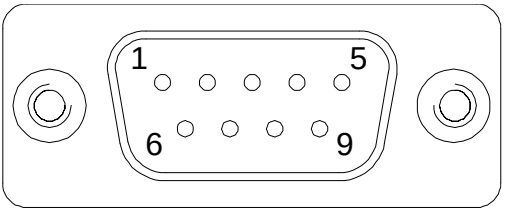
2.5.26 USB Ports 0 and 1 (CN26)



Pin	Pin Name	Signal Type	Signal level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	

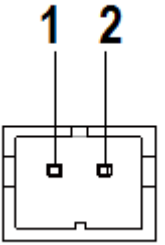
17	USB1_SSTX−	DIFF	
18	USB1_SSTX+	DIFF	

2.5.27 COM Port 1 (D-SUB 9) (CN27)



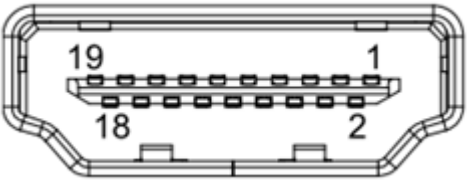
Pin	Pin Name	Signal Type	Signal level
1	DCD	IN	
2	RX	IN	
3	TX	OUT	±9V
4	DTR	OUT	±9V
5	GND	GND	
6	DSR	IN	
7	RTS	OUT	±9V
8	CTS	IN	
9	RI	IN	

2.5.28 Battery CONN (CN28)



Pin	Pin Name	Signal Type	Signal level
1	+3.3V	PWR	3.3V
2	GND	GND	

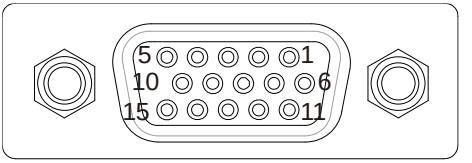
2.5.29 HDMI (CN29)



Pin	Pin Name	Signal Type	Signal level
1	HDMI_TX2+	DIFF	
2	GND	GND	
3	HDMI_TX2-	DIFF	
4	HDMI_TX1+	DIFF	
5	GND	GND	
6	HDMI_TX1-	DIFF	
7	HDMI_TX0+	DIFF	
8	GND	GND	

9	HDMI_TX0-	DIFF	
10	HDMI_CLK+	DIFF	
11	GND	GND	
12	HDMI_CLK-	DIFF	
13	NC		
14	NC		
15	DDC_CLK	I/O	+5V
16	DDC_DATA	I/O	+5V
17	GND	GND	
18	+5V	PWR	+5V
19	HDMI_HPD		

2.5.30 VGA Port (CN30)



Pin	Pin Name	Signal Type	Signal level
1	RED	OUT	
2	GREEN	OUT	
3	BLUE	OUT	
4	NC		
5	GND	GND	
6	RED_GND_RTN	GND	
7	GREEN_GND_RTN	GND	
8	BLUE_GND_RTN	GND	

9	+5V	PWR	+5V
10	NC		
11	NC		
12	DDC_DATA	I/O	+5V
13	HSYNC	OUT	
14	VSYNC	OUT	
15	DDC_CLK	I/O	+5V

2.5.31 DDR3L SO-DIMM Slot (DIMM1)

Standard specification

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

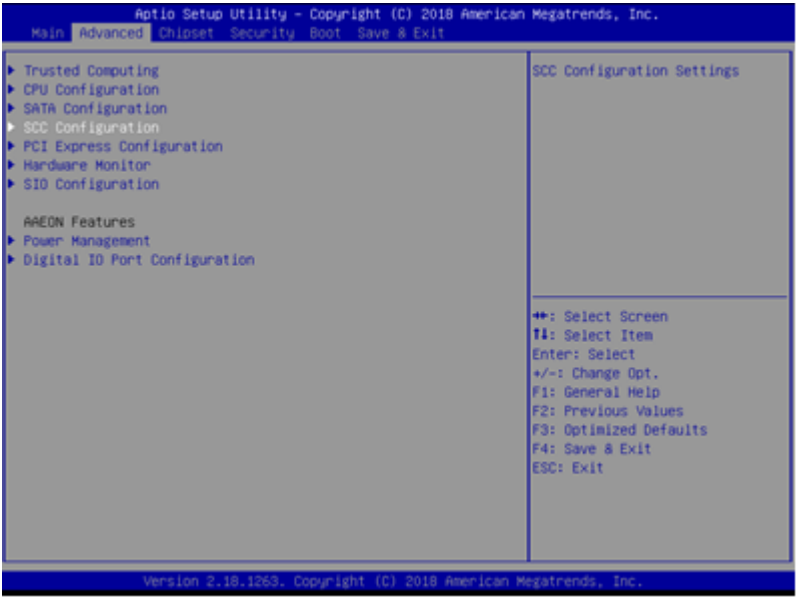
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

3.3 Setup submenu: Main

Press '*Delete*' to enter Setup

3.4 Setup submenu: Advanced



3.4.1 Advanced: Trusted Computing

Options summary:

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable SHA256 PCR Bank		

Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		

3.4.2 Advanced: CPU Configuration

Options summary:

C-States	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable C States.		
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode		
Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	

Enable/Disable Power Limit 1		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CP VT-d		
Thermal Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Thermal Monitor		

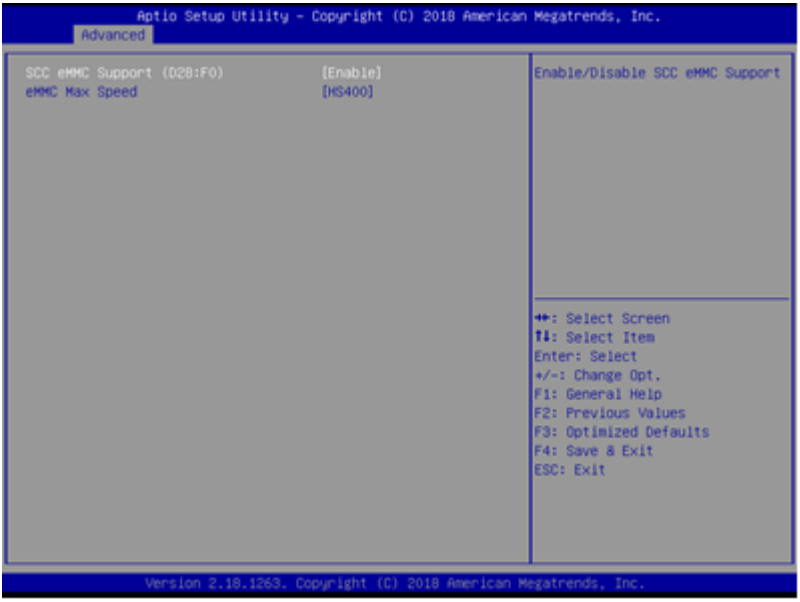
3.4.3 Advanced: SATA Configuration

Options summary:

Chipset SATA	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

Port 1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port		
SATA Port 1 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

3.4.4 Advanced: SCC Configuration



Options summary:

SCC eMMC Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SCC eMMC Support		
eMMC Max Speed	HS400	Optimal Default, Failsafe Default
	HS200	
	DDR50	
Select the eMMC max Speed allowed.		

3.4.5 Advanced: PCI Express Configuration

Options summary:

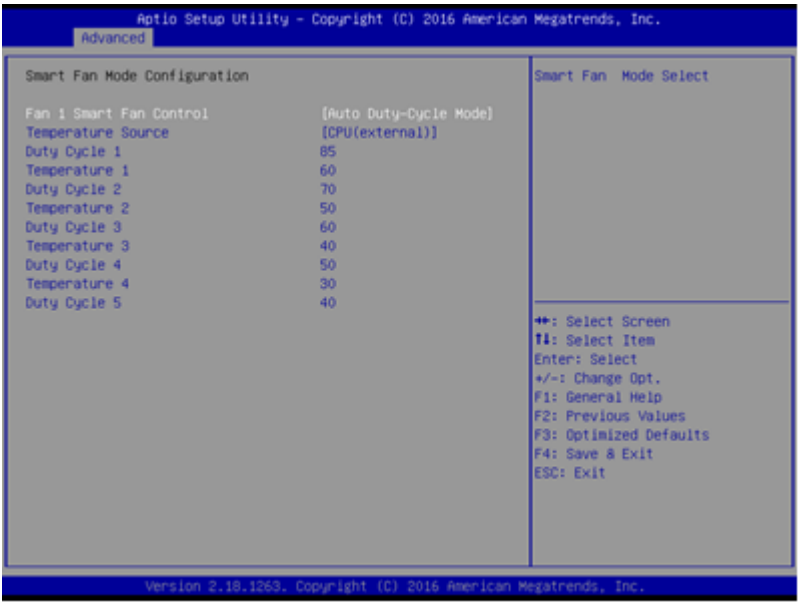
PCIE Slot(CN7)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control PCIE Slot (CN7)		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe Speed		

3.4.6 Advanced: Hardware Monitor

Options summary:

Smart Fan	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables Smart Fan.		

3.4.6.1Hardware Monitor: CPU Smart Fan Mode Configuration

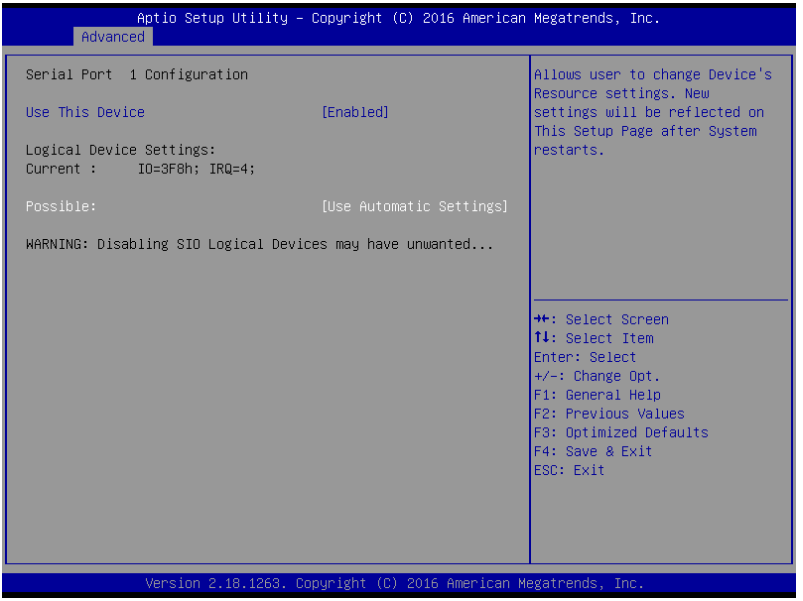


Options summary:

Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU(external)	Optimal Default, Failsafe Default
	System	
Select the monitored temperature source for this fan.		
Duty Cycle 1	85	
Temperature 1	60	
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		

3.4.7 Advanced: SIO Configuration

3.4.7.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.7.2 SIO Configuration: Serial Port 2 Configuration

Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.7.3 SIO Configuration: Serial Port 3 Configuration

Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=11	
	IO=2E8h; IRQ=11	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.4.7.4 SIO Configuration: Serial Port 4 Configuration

Options summary:

Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=10	
	IO=3E8h; IRQ=10	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.7.5 SIO Configuration: Parallel Port Configuration

Options summary:

Use This Device	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable this Logical Device.		

3.4.8 Advanced: Power Management

Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Power Saving(ERP) Control	Disabled	Optimal Default, Failsafe Default
	Enabled	
Configure power mode for power saving function.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system	Disable	Optimal Default, Failsafe Default

from S5	Fixed Time	
Select system power mode		

3.4.9 Advanced: Digital IO Port Configuration

Options summary:

DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

3.5 Setup submenu: Chipset

3.5.1 Chipset: North Bridge

3.5.1.1 North Bridge: LVDS Panel Configuration(LVDS2 only available for 2 LVDS Sku)

Options summary:

LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disabled this panel.		
LVDS Panel Type	640x480@60Hz	Optimal Default, Failsafe Default
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	
	1280x768@60Hz	
	1280x800@60Hz	

	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	

Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.6 Setup submenu: Security

Change User/Supervisor Password

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup submenu: Boot

Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
EnableDisable showing boot logo.		
Monitor Mwait	Disable	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Enable/Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.		

3.8 Setup submenu: Exit

Chapter 4

Drivers Installation

4.1 Driver Download/Installation

Drivers for the GENE-APL6 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/embedded-single-board-computers-gene-apl6

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

1. Open the **Step1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

1. Open the **Step2 - VGA** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 3 – Install LAN Drivers

1. Click on the **Step3 - LAN** folder and select your OS
2. Open the**.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Drivers

1. Open the **Step4 - Audio** folder followed by **0006-64bit_Win7_Win8_Win81_Win10_R279.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install TXE Driver

1. Open the **Step5 - TXE** folder followed by **SetupTXE.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Touch Driver

1. Open the **Step6 - Touch** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 7 – Install GPIO Driver

1. Open the **Step6 - GPIO** folder followed by **SetupSerialIO.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address		
	Default Value	Note
I/O Base Address	0xA10	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7, register 0x60-0x61.

Table 2 : Watchdog relative register table				
Register	Offset	BitNum	Value	Note
Watchdog WDTRST# Enable	0x00	7	1	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s **Pulse width is must longer then 16ms.**
Signal Polarity	0x05	2	0	0: low active 1: high active **Must set this bit to 0**
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse **Must set this bit to 1**
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

A.2 Watchdog Sample Program

```
*************************************************************************************
// WDT I/O operation relative definition (Please reference to Table 1)
#define   WDTAddr         0x510   // WDT I/O base address
Void   WDTWriteByte(byte Register, byte Value);
byte   WDTReadByte(byte Register);
Void   WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define   DevReg          0x00   // Device configuration register
      #define   WDTRstBit   0x80   // Watchdog WDTRST# (Bit7)
      #define   WDTRstVal   0x80   // Enabled WDTRST#
#define   TimerReg        0x05   // Timer register
      #define   PSWidthBit     0x00     // WDTRST# Pulse width (Bit0:1)
      #define   PSWidthVal     0x01     // 25ms for WDTRST# pulse
      #define   PolarityBit    0x02     // WDTRST# Signal polarity (Bit2)
      #define   PolarityVal    0x00     // Low active for WDTRST#
      #define   UnitBit        0x03     // Unit for timer (Bit3)
      #define   ModeBit        0x04     // WDTRST# mode (Bit4)
      #define   ModeVal        0x01     // 0:level 1: pulse
      #define   EnableBit      0x05     // WDT timer enable (Bit5)
      #define   EnableVal      0x01     // 1: enable
      #define   StatusBit      0x06     // WDT timer status (Bit6)
#define   CounterReg   0x06   // Timer counter register
*************************************************************************************

*************************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig(Counter, Unit);

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*************************************************************************************

*************************************************************************************
// Procedure : AaeonWDTEnable
```

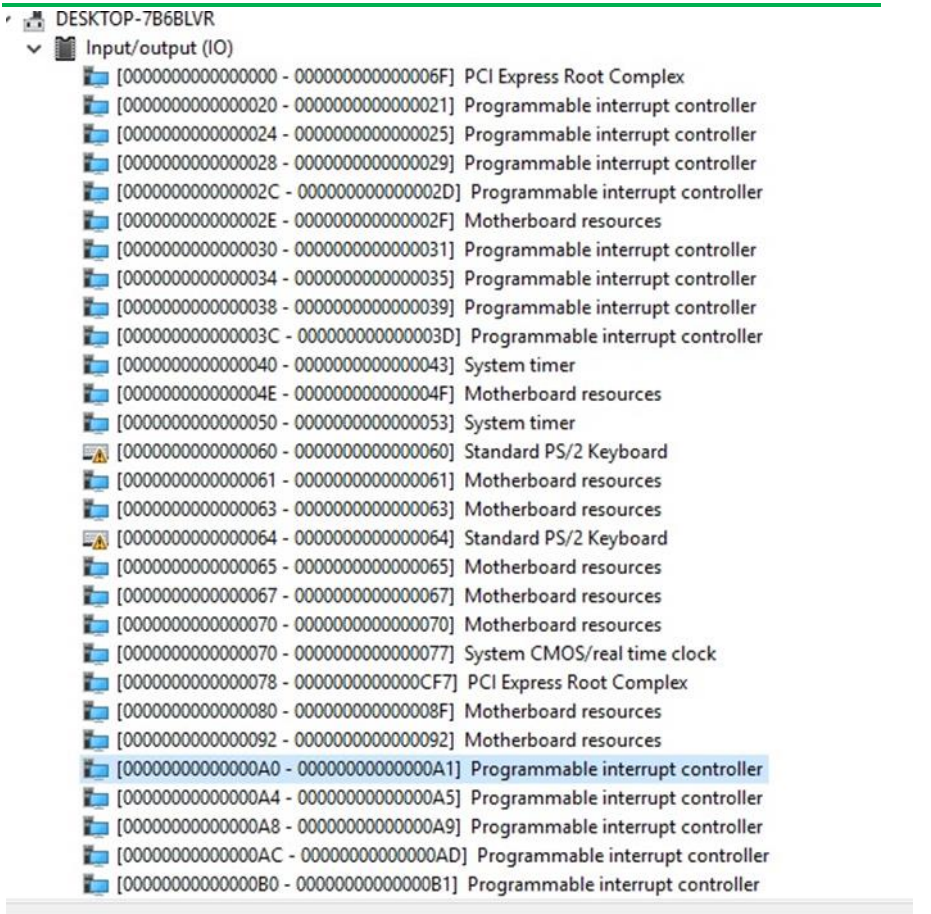
```
VOID    AaeonWDTEnable (){
          WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (byte Counter, BOOLEAN Unit){
          // Disable WDT counting
          WDTEnableDisable(0);
          // Clear Watchdog Timeout Status
          WDTClearTimeoutStatus();
          // WDT relative parameter setting
          WDTParameterSetting(Timer, Unit);
}

VOID    WDTEnableDisable(byte Value){
          If (Value == 1)
              WDTSetBit(TimerReg, EnableBit, 1);
          else
              WDTSetBit(TimerReg, EnableBit, 0);
}

VOID    WDTParameterSetting(byte Counter, BOOLEAN Unit){
          // Watchdog Timer counter setting
         WDTWriteByte(CounterReg, Counter);
        // WDT counting unit setting
        WDTSetBit(TimerReg, UnitBit, Unit);
        // WDT output mode set to pulse
        WDTSetBit(TimerReg, ModeBit, ModeVal);
        // WDT output mode set to active low
        WDTSetBit(TimerReg, PolarityBit, PolarityVal);
        // WDT output pulse width is 25ms
        WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
          // Watchdog WDTRST# Enable
         WDTSetBit(DevReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        WDTSetBit(TimerReg, StatusBit, 1);
}
*****************************************************************************

*****************************************************************************
```

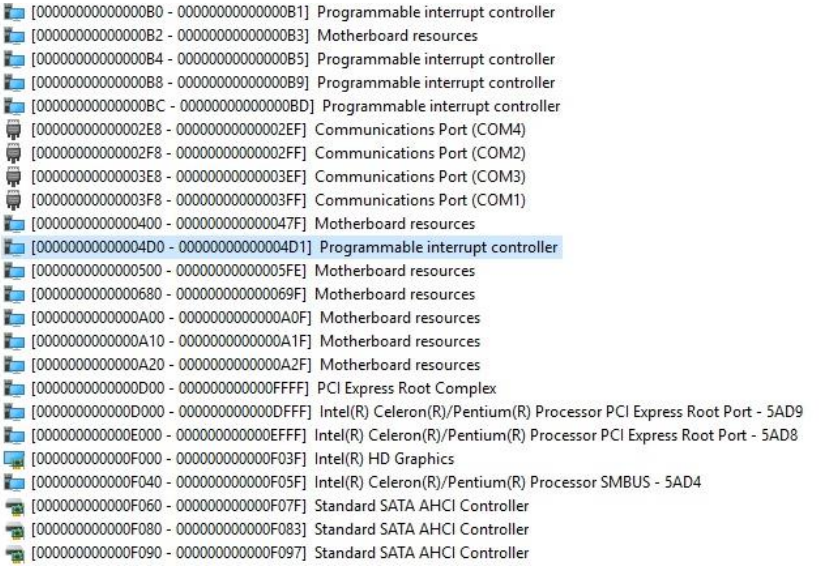
```
VOID   WDTWriteByte(byte Register, byte Value){
       IOWriteByte(WDTAddr+Register, Value);
}

byte   WDTReadByte(byte Register){
       return IOReadByte(WDTAddr+Register);
}

VOID   WDTSetBit(byte Register, byte Bit, byte Val){
       byte TmpValue;

       TmpValue = WDTReadByte(Register);
       TmpValue &= ~(1 << Bit);
       TmpValue |= Val << Bit;
       WDTWriteByte(Register, TmpValue);
}

********************************************************************************
```

Appendix B

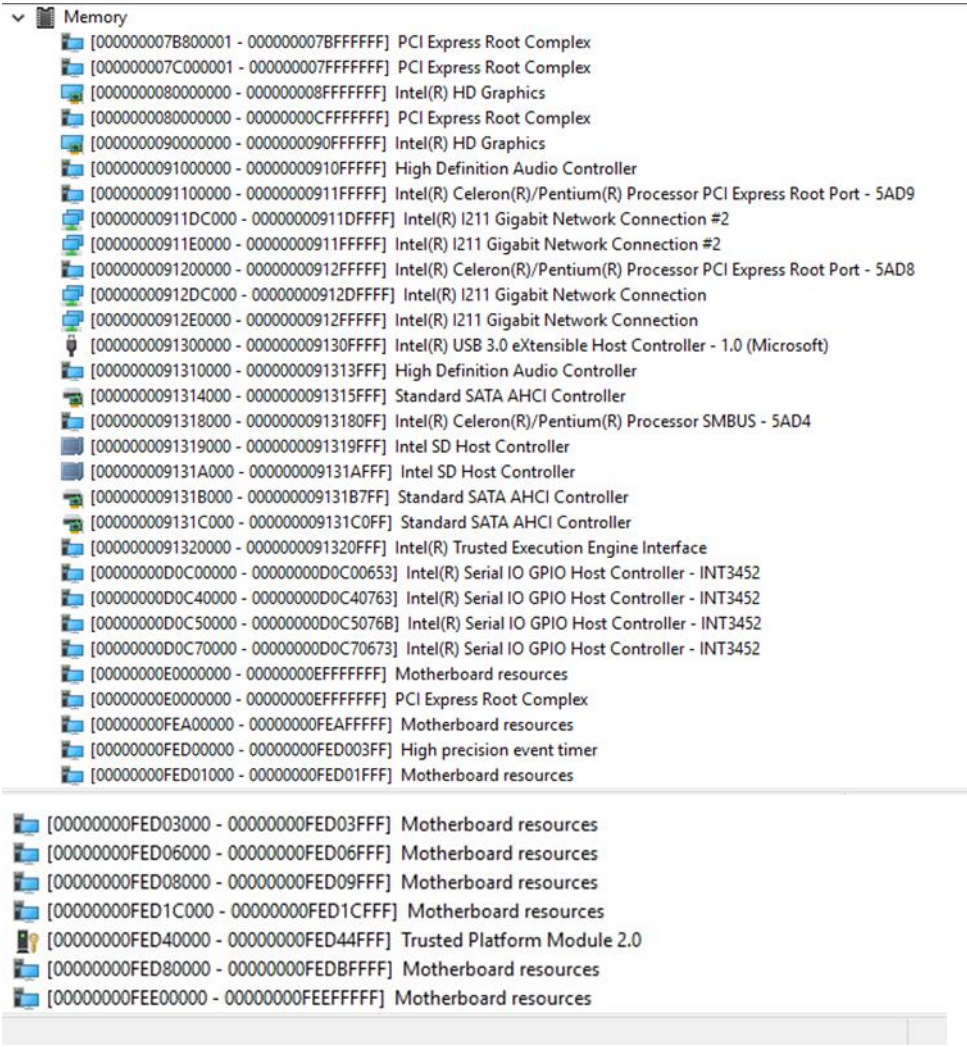
I/O Information

B.1 I/O Address Map

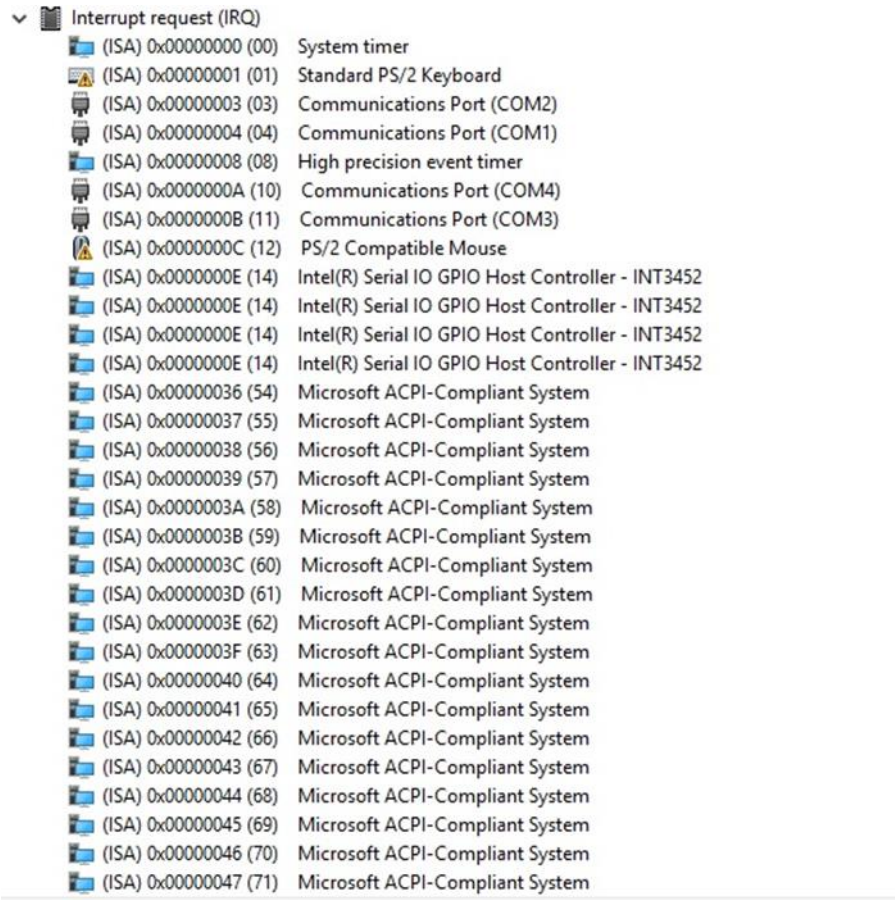



[00000000000000B0 - 00000000000000B1] Programmable interrupt controller
[00000000000000B2 - 00000000000000B3] Motherboard resources
[00000000000000B4 - 00000000000000B5] Programmable interrupt controller
[00000000000000B8 - 00000000000000B9] Programmable interrupt controller
[00000000000000BC - 00000000000000BD] Programmable interrupt controller
[00000000000002E8 - 00000000000002EF] Communications Port (COM4)
[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[00000000000003E8 - 00000000000003EF] Communications Port (COM3)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[0000000000000400 - 000000000000047F] Motherboard resources
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000500 - 000000000000005FE] Motherboard resources
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 0000000000000FFFF] PCI Express Root Complex
[0000000000000D000 - 0000000000000DFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[0000000000000E000 - 0000000000000EFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller

B.2 Memory Address Map

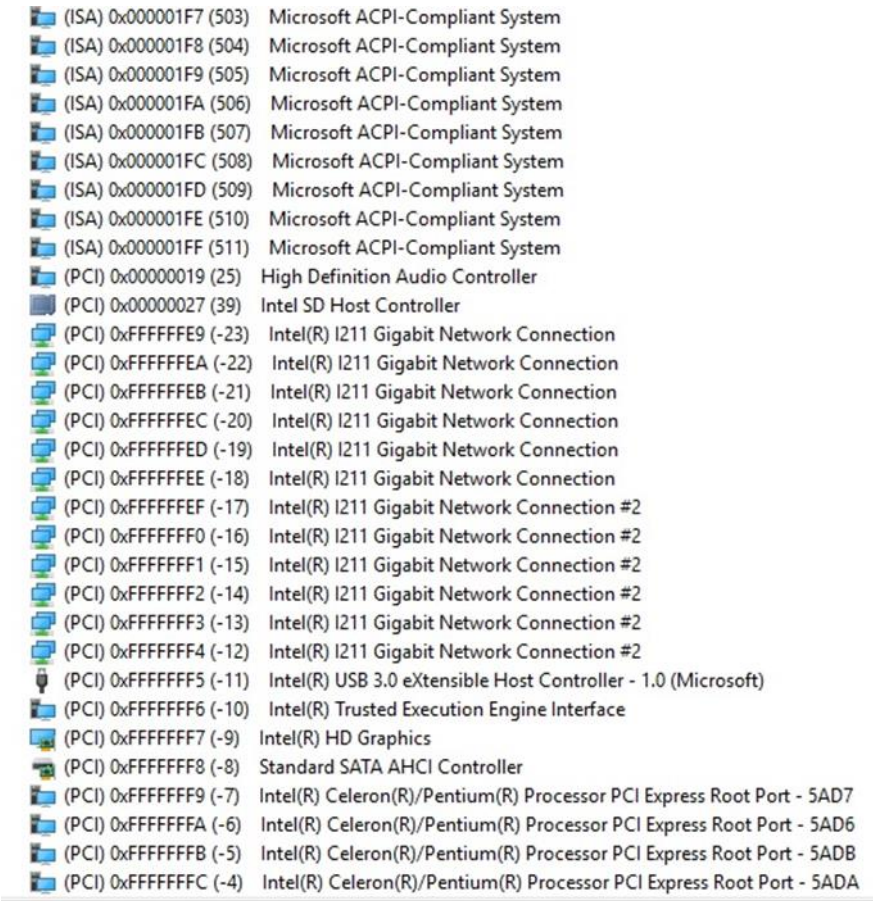


B.3 IRQ Mapping Chart



(ISA) 0x00000047 (71) Microsoft ACPI-Compliant System
(ISA) 0x00000048 (72) Microsoft ACPI-Compliant System
(ISA) 0x00000049 (73) Microsoft ACPI-Compliant System
(ISA) 0x0000004A (74) Microsoft ACPI-Compliant System
(ISA) 0x0000004B (75) Microsoft ACPI-Compliant System
(ISA) 0x0000004C (76) Microsoft ACPI-Compliant System
(ISA) 0x0000004D (77) Microsoft ACPI-Compliant System
(ISA) 0x0000004E (78) Microsoft ACPI-Compliant System
(ISA) 0x0000004F (79) Microsoft ACPI-Compliant System
(ISA) 0x00000050 (80) Microsoft ACPI-Compliant System
(ISA) 0x00000051 (81) Microsoft ACPI-Compliant System
(ISA) 0x00000052 (82) Microsoft ACPI-Compliant System
(ISA) 0x00000053 (83) Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84) Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85) Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86) Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87) Microsoft ACPI-Compliant System
(ISA) 0x00000058 (88) Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89) Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90) Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91) Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System

(ISA) 0x00000065 (101)	Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102)	Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103)	Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104)	Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105)	Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106)	Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107)	Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108)	Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109)	Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110)	Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111)	Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112)	Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113)	Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114)	Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115)	Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116)	Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117)	Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118)	Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119)	Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120)	Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121)	Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122)	Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123)	Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124)	Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125)	Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126)	Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127)	Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128)	Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129)	Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130)	Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131)	Microsoft ACPI-Compliant System


(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System
(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000019 (25) High Definition Audio Controller
(PCI) 0x00000027 (39) Intel SD Host Controller
(PCI) 0xFFFFFFE9 (-23) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEA (-22) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEB (-21) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEC (-20) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFED (-19) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEE (-18) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFEF (-17) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF0 (-16) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF1 (-15) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF2 (-14) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF3 (-13) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF4 (-12) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFF5 (-11) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFF6 (-10) Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFF7 (-9) Intel(R) HD Graphics
(PCI) 0xFFFFFFF8 (-8) Standard SATA AHCI Controller
(PCI) 0xFFFFFFF9 (-7) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD7
(PCI) 0xFFFFFFFA (-6) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD6
(PCI) 0xFFFFFFFB (-5) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
(PCI) 0xFFFFFFFC (-4) Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA

Appendix C

Mating Connectors

C.1 List of Mating Connectors and Cables

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	External +5VSB Power Input and PS_ON#	JST	PHR-3	ATX Cable	170220020B
CN2	+5Vout Connector	JST	PHR-2	2 Pins For HDD Power	1702150155
CN3	+9~24V Vin Connector	N/A	N/A	Power Cable	1702002010
CN4	SATA Connector	Molex	88750-5318	SATA Cable	1709070500
CN5	CPU Fan Connector	Molex	22-01-2035	N/A	N/A
CN6	Audio Connector	Molex	51021-1000	Audio Cable	1709100254
CN8	COM Port2 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN9	COM Port3 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN10	COM Port4 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN12	LPC Port	PINEX	710-74-12T WR6	AAEON LPC Cable	1703120130

CN13	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN16	Digital I/O Connector	Neltron	2026B-10	N/A	N/A
CN17	LVDS Inverter Connector	JST	PHR-5	NA	NA
CN18	LVDS Connector	HIROSE	DF13-30DS-1.25C	N/A	N/A
CN19	USB Port Connector	Molex	51021-0500	USB Wafer Cable	1700050207
CN20	USB Port Connector	Molex	51021-0500	USB Wafer Cable	1700050207
CN21	LVDS Inverter Connector	JST	PHR-5	NA	NA
CN22	Touch Screen Connector	JST	SHR-9V-S-B	N/A	N/A
CN25	COM Port 1 Connector	Molex	51021-0900	Serial Port Cable	1701090150
CN28	External RTC Connector	Molex	51021-0200	Battery Cable	175011901C

Appendix D

Digital I/O Ports

D.1 Digital I/O Register

7.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	00h: Select FDC device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. 10h: Select UART1 device configuration registers. 11h: Select UART2 device configuration registers. 12h: Select UART3 device configuration registers. 13h: Select UART4 device configuration registers. 14h: Select UART5 device configuration registers. 15h: Select UART6 device configuration registers. Otherwise: Reserved.

GPIO8 Output Enable Register — Index 88h

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_OE	R/W	LRESET#	0	0: GPIO87 is in input mode. 1: GPIO87 is in output mode.
6	GPIO86_OE	R/W	LRESET#	0	0: GPIO86 is in input mode. 1: GPIO85 is in output mode.
5	GPIO85_OE	R/W	LRESET#	0	0: GPIO85 is in input mode. 1: GPIO85 is in output mode.
4	GPIO84_OE	R/W	LRESET#	0	0: GPIO84 is in input mode. 1: GPIO84 is in output mode.
3	GPIO83_OE	R/W	LRESET#	0	0: GPIO83 is in input mode. 1: GPIO83 is in output mode.
2	GPIO82_OE	R/W	LRESET#	0	0: GPIO82 is in input mode. 1: GPIO82 is in output mode.
1	GPIO81_OE	R/W	LRESET#	0	0: GPIO81 is in input mode. 1: GPIO81 is in output mode.
0	GPIO80_OE	R/W	LRESET#	0	0: GPIO80 is in input mode. 1: GPIO80 is in output mode.

GPIO8 Output Data Register — Index 89h (This byte could be also written by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_VAL	R/W	LRESET#	1	0: GPIO87 outputs 0 when in output mode. 1: GPIO87 outputs 1 when in output mode.
6	GPIO86_VAL	R/W	LRESET#	1	0: GPIO86 outputs 0 when in output mode. 1: GPIO86 outputs 1 when in output mode.
5	GPIO85_VAL	R/W	LRESET#	1	0: GPIO85 outputs 0 when in output mode. 1: GPIO85 outputs 1 when in output mode.
4	GPIO84_VAL	R/W	LRESET#	1	0: GPIO84 outputs 0 when in output mode. 1: GPIO84 outputs 1 when in output mode.
3	GPIO83_VAL	R/W	LRESET#	1	0: GPIO83 outputs 0 when in output mode. 1: GPIO83 outputs 1 when in output mode.
2	GPIO82_VAL	R/W	LRESET#	1	0: GPIO82 outputs 0 when in output mode. 1: GPIO82 outputs 1 when in output mode.
1	GPIO81_VAL	R/W	LRESET#	1	0: GPIO81 outputs 0 when in output mode. 1: GPIO81 outputs 1 when in output mode.
0	GPIO80_VAL	R/W	LRESET#	1	0: GPIO80 outputs 0 when in output mode. 1: GPIO80 outputs 1 when in output mode.

GPIO8 Pin Status Register — Index 8Ah (This byte could be also read by base address + 2)

Bit	Name	R/W	Reset	Default	Description
7	GPIO87_IN	R	-	-	The pin status of GPIO87/PD7.
6	GPIO86_IN	R	-	-	The pin status of GPIO86/PD6.
5	GPIO85_IN	R	-	-	The pin status of GPIO85/PD5.
4	GPIO84_IN	R	-	-	The pin status of GPIO84/PD4.
3	GPIO83_IN	R	-	-	The pin status of GPIO83/PD3.
2	GPIO82_IN	R	-	-	The pin status of GPIO82/PD2.
1	GPIO81_IN	R	-	-	The pin status of GPIO81/PD1.
0	GPIO80_IN	R	-	-	The pin status of GPIO80/PD0.

D.2 Digital I/O Sample Code (4 in 4 out, 2 low 2 high)

```
Outportb(0x2E,0x87); //enter configuration
Outportb(0x2E,0x87);

Outportb(0x2E,0x07); //set LDN
Outportb(0x2F,0x06);

Outportb(0x2E,0xA0); //GPIO set 5 register
Outportb(0x2F,0xF0);

Outportb(0x2E,0xA1); //GPIO output data register
Outportb(0x2F,0x30);

Outportb(0x2E,0xAA); //exit configuration
```