FWS-8600

Network Appliance

User's Manual 1st Ed

Last Updated: September 23, 2019

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-8600	1
● Gift Box (Including Console Cable x 1, SATA Cable x 1, SATA Power Cable x 1, and Ear Bracket Kit x 1)	1
● CPU cooler	2

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量 AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext. Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

1.1 Specifications

Platform	
Form Factor	2U Rackmount Network Platform
Processor	Dual Intel® Xeon® Processor Skylake-SP & Cascade Lake-SP processor
Chipset	Intel®C621
System Memory	DDR4 2133/2400/2666 R-DIMM, Up to 512 GB

Network	
Ethernet	Intel® i211 Gigabit Ethernet x 2
Bypass	Depends on NIM module
NIM Slot	NIM x 4 (up to NIM x 8)

Display	
Graphic Controller	—
Connector	VGA Option

Storage	
HDDs	Internal 2.5" HDD x 2 or 3.5" HDD x 1 Option, M.2 x 1
CF/CFast/mSATA	(mSATAx1 Optional ,cannot use with Mini-Card)

Internal/Expansion Interface	
PCIe slot	PCIe [x16] slots x 2 (Optional) M.2 Slot (2260 M Key) x 1
Mini-Card slot	Mini Card x 1

Internal/Expansion Interface	
IPMI	—
Keyboard and Mouse	—
USB	USB 3.0 x 2 (USB 3.0 x 2 ,Box Header 2.0mm optional)

Miscellaneous	
RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	GPIO Programmable push button x 1
TPM	TPM 2.0 9665 (TPM v1.2 9660 optional)
GPIO	4 bits input, 4 bits output (optional)
FAN	5
MTBF (Hours)	TBD
Color	Black

Environmental Parameters and Dimension	
Power Requirement	550 ~ 600W Redundant Power
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10% ~ 80% relative humidity, non-condensing
Storage Humidity	10% ~ 80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz / operation (2.5" Hard Disk Drive) 1.5 Grms/ 5 ~ 500Hz / non operation
Shock	10 G peak acceleration (11 m sec. duration), operation 20 G peak acceleration (11 m sec. duration), non-operation

Environmental Parameters and Dimension

Dimension (W X D X H)	17.48" x 22.83" x3.46" (444mm x 580mm x 88mm)

I/O Interfaces

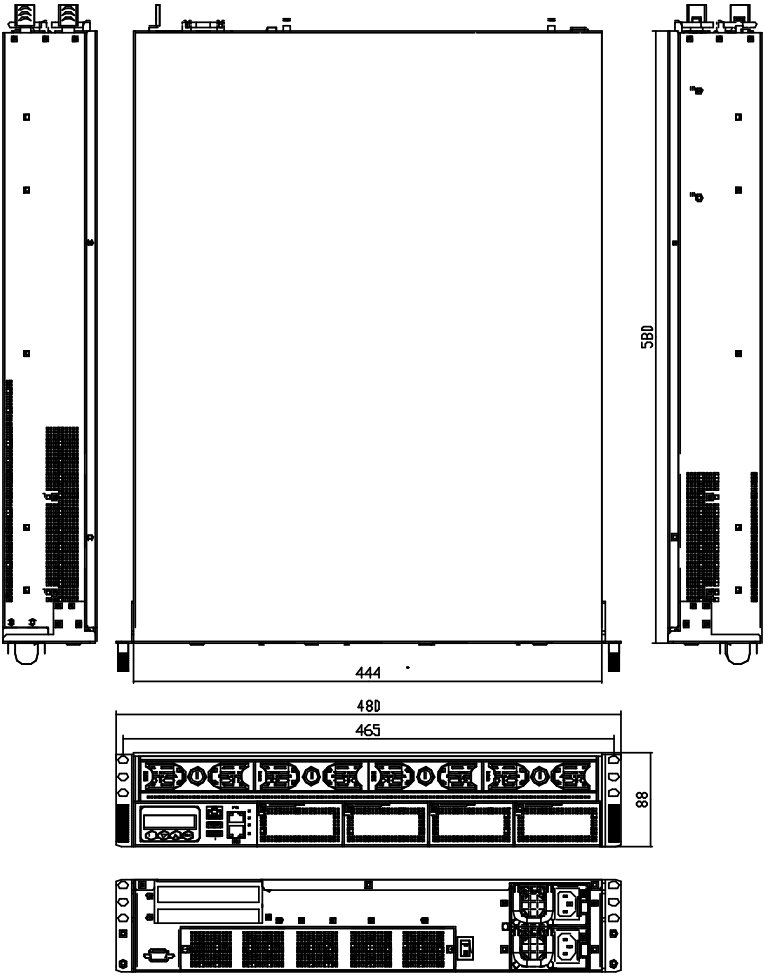
Front Panel	Power LED x 1
	Status LED x 1
	HDD Active LED x 1
	USB 3.0 Ports x 2
	RJ-45 Console x 1
	Parallel LCM display and 4 keypad x 1
	Software Programmable Button x1
	RJ-45 LAN x 2
Rear Panel	AC Power Input x 2
	Power Switch x 1
	VGA port (Optional)
	Rear Expansion Slot x 2 (PCIe [x16] Optional)

Chapter 2

Hardware Information

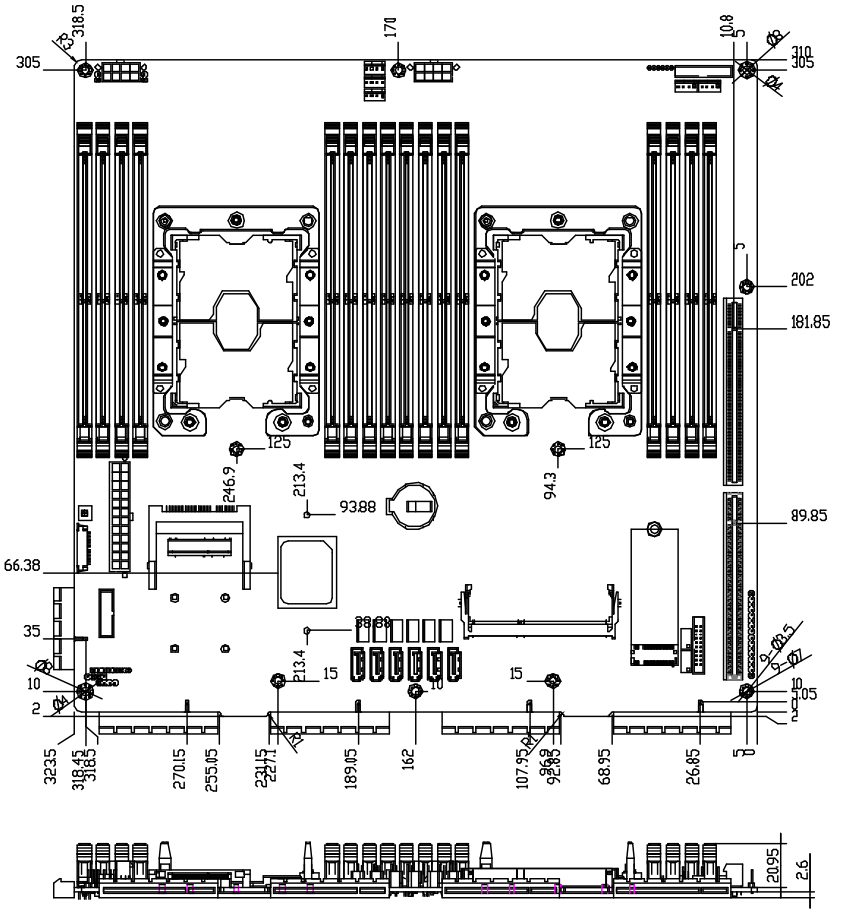
2.1 Dimensions

2.1.1 System

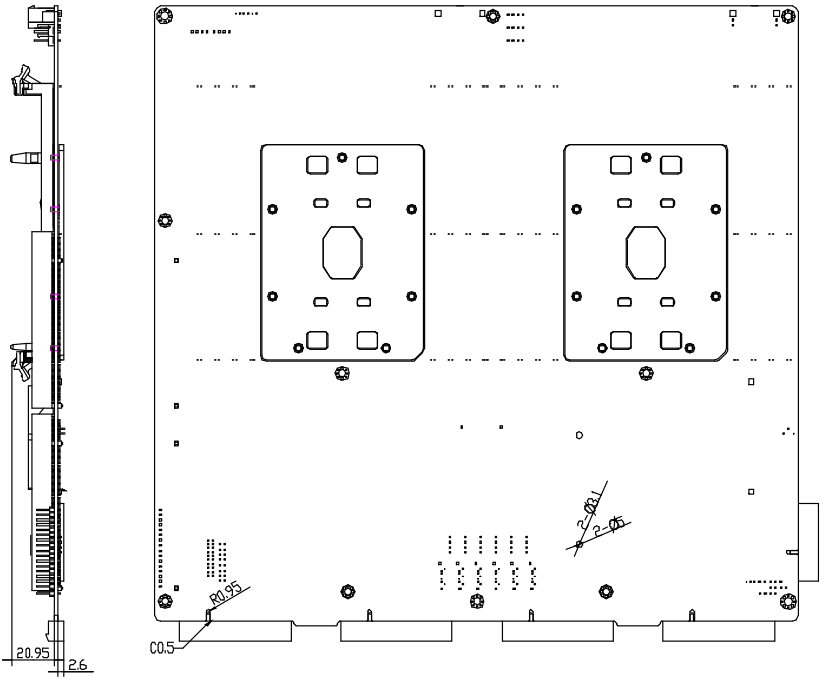


2.1.2 Board

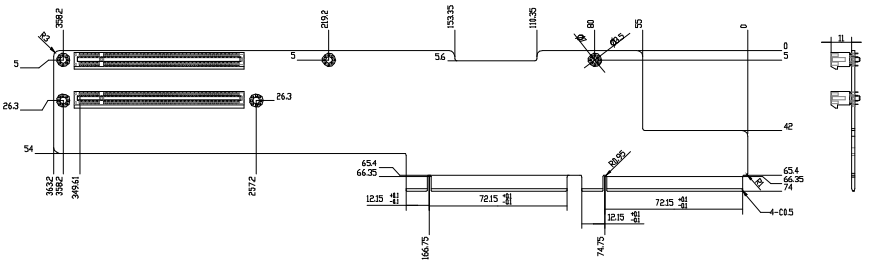
Top and Front

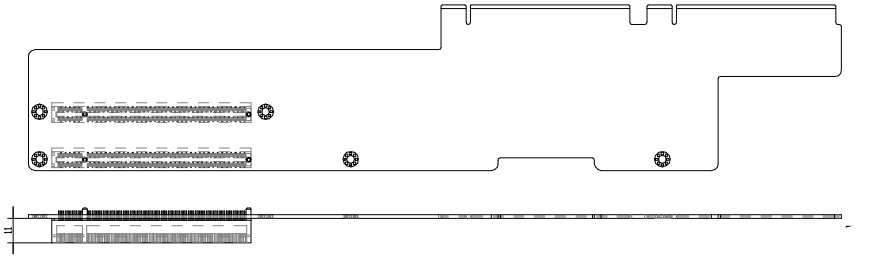


Bottom and Side

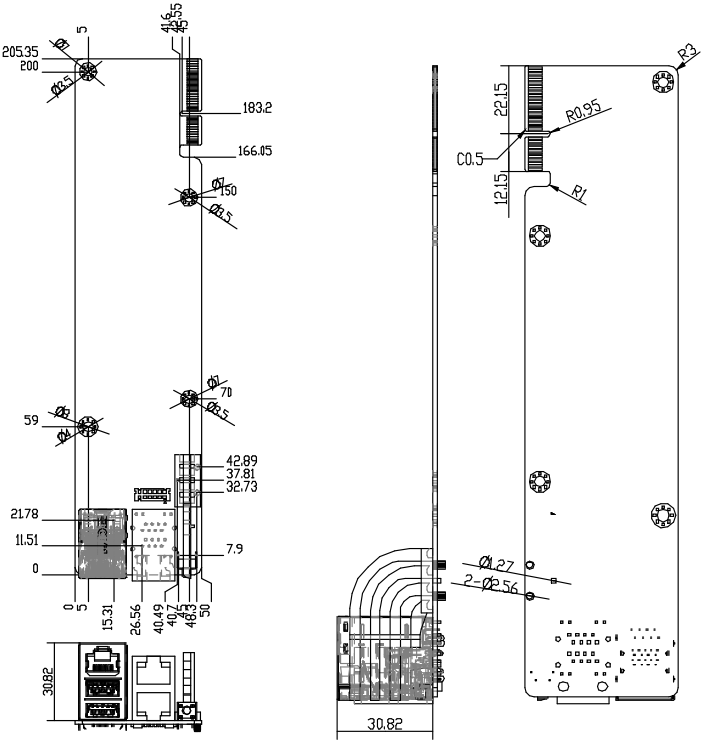


2.1.3 PER-T488 Expansion Riser





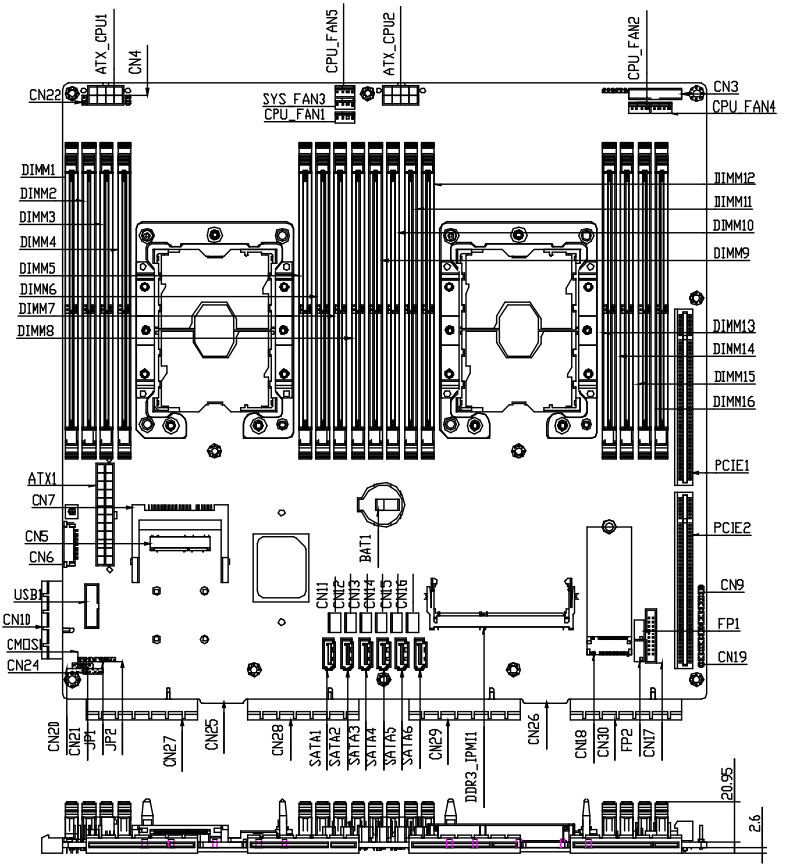
2.1.4 PER-T489 I/O Card



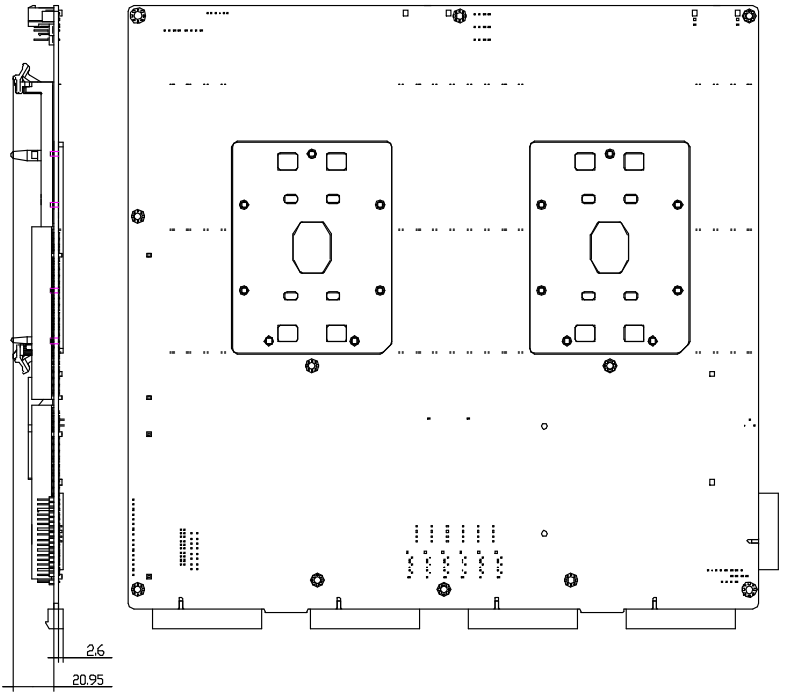
2.2 Jumpers and Connectors

2.2.1 Board

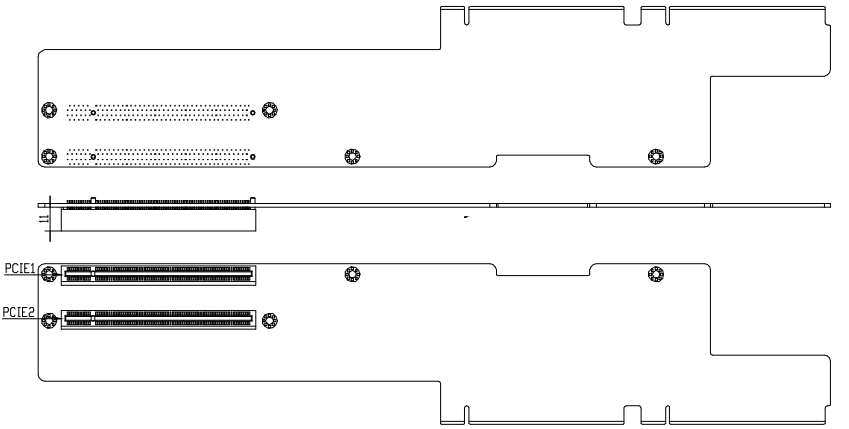
Top and Front



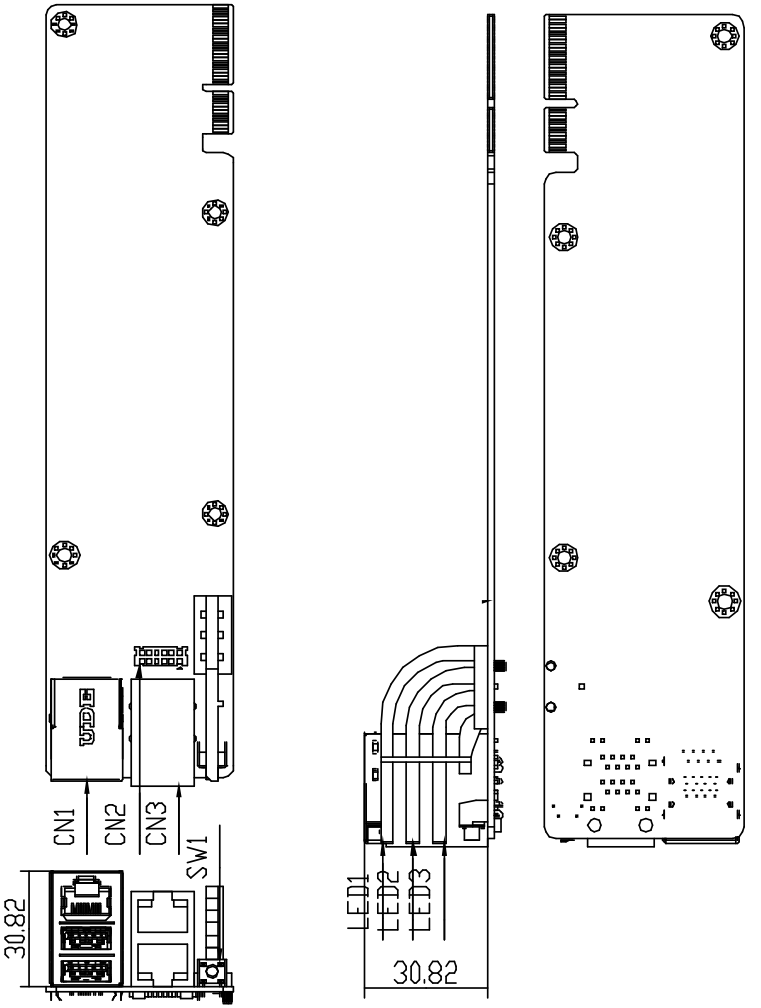
Bottom and Side



2.2.2 PER-T488 Expansion Riser



2.2.3 PER-T489 I/O Card

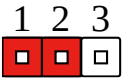


2.3 List of Jumpers

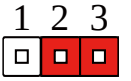
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CMOS1	RTC Reset
JP2	Auto Power Button

2.3.1 RTC Reset (CMOS1)

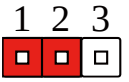


Normal (Default)

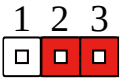


Clear CMOS

2.3.2 Auto Power Button (PWRBTN) Selection (JP2)



Disabled (Default)



Enabled

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
ATX1	24-pin ATX Power Connector
ATX_CPU1~2	8-pin 12V Power Connector
CN3	20-pin smart fan
CN5	Mini PCIe socket
CN6	LCM Connector
CN11~16	HDD Power Connector
CN18	M.2 M-Key Socket
CN21	State LED
CN22	Power Switch
CN24	Keypad Connector
DIO1	Digital I/O
FP1	Front Panel Connector 1
FP2	Front Panel Connector 2
SATA1~6	SATA Port Connector
SYS_FAN2, 4, 8	SYS FAN 1, 2, 3
SYS_FAN7	CPU FAN2
SYS_FAN10	CPU FAN1
USB1	USB 3.0 Port

2.4.1 Digital I/O (DIO1)

Pin	Signal	Signal Type
1	DIO0	Input/ Output
2	DIO1	Input/ Output
3	DIO2	Input/ Output
4	DIO3	Input/ Output
5	DIO4	Input/ Output
6	DIO5	Input/ Output
7	DIO6	Input/ Output
8	DIO7	Input/ Output
9	+3.3V	PWR
10	GND	GND

2.4.2 LCM Connector (CN6)

Pin	Signal	Signal Type
1	LCMGND	GND
2	LCMVCC	PWR
3	VEE	PWR
4	SLIN-	Output
5	INIT	Output
6	AFD-	Output
7	PTD0	Input/ Output
8	PTD1	Input/ Output
9	PTD2	Input/ Output
10	PTD3	Input/ Output
11	PTD4	Input/ Output
12	PTD5	Input/ Output
13	PTD6	Input/ Output
14	PTD7	Input/ Output
15	+5V	PWR
16	LCD-	Output

2.4.3 Keypad Connector (CN24)

Pin	Signal	Signal Type
1	KEY PAD Down	Input
2	KEY PAD Up	Input
3	KEY PAD Right	Input
4	KEY PAD Left	Input

2.4.4 HDD Power Connector (CN11~CN16)

Pin	Signal	Signal Type
1	+12V	PWR
2	GND	GND
3	GND	GND
4	+5V	PWR

2.4.5 USB 3.0 Port (USB1)

Pin	Signal	Signal Type	Pin	Signal	Signal Type
1	+5V_USB	PWR	9	USBP_0P	DIFF
2	USB3_RX1_DN	DIFF	10	NC	
3	USB3_RX1_DP	DIFF	11	USBP_1P	DIFF
4	GND	GND	12	USBP_1N	DIFF
5	USB3_TX1_DN	DIFF	13	GND	GND
6	USB3_TX1_DP	DIFF	14	USB3_TX2_DP	DIFF
7	GND	GND	15	USB3_TX2_DN	DIFF
8	USBP_0N	DIFF	16	GND	GND

2.4.7 Front Panel Connector 2 (FP2)

Pin	Signal	Signal Type
1	Power On Button(+)	Input
2	Power On Button(-)	GND
3	Reset Switch (+)	Input
4	Reset Switch (-)	GND
5	HDD LED (+)	Output
6	HDD LED (-)	Output
7	Power LED(+)	POWER
8	Power LED(-)	GND

2.4.8 Front Panel Connector 1 (FP1)

Pin	Signal	Signal Type
1		
2		
3		
4	GND	GND
5		
6	PMBUS_SML1_SCL	I/O
7		
8	PMBUS_SML1_SDA	I/O

2.5 Installing Chassis Mounted Hard Drive

This section details how to install the system chassis mounted hard drive assembly using either two 2.5" HDDs or one 3.5" HDD.

1. Remove the highlighted screws.

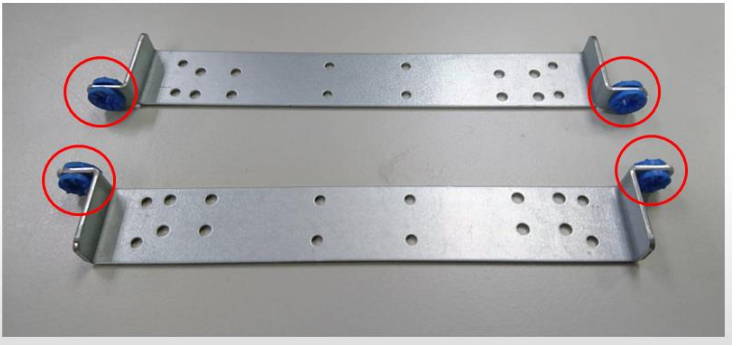
2. Slide lid towards back, then lift to remove.

3. Remove the five highlighted screws securing the HDD tray. Note, you must remove the leftmost HDD bay to access the screw located there.

4. Shift the HDD tray back, then lift to remove from the system.

(Step 4 Continued)

5. Attach cushions onto the hard disk drive brackets as shown.



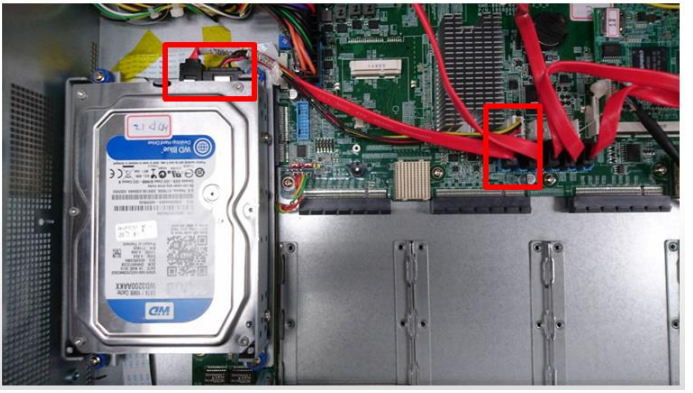
6. Attach the brackets to the hard drive(s) according to the following diagrams:

Two 2.5″ Hard Drives: Use eight screws to attach the brackets as shown.

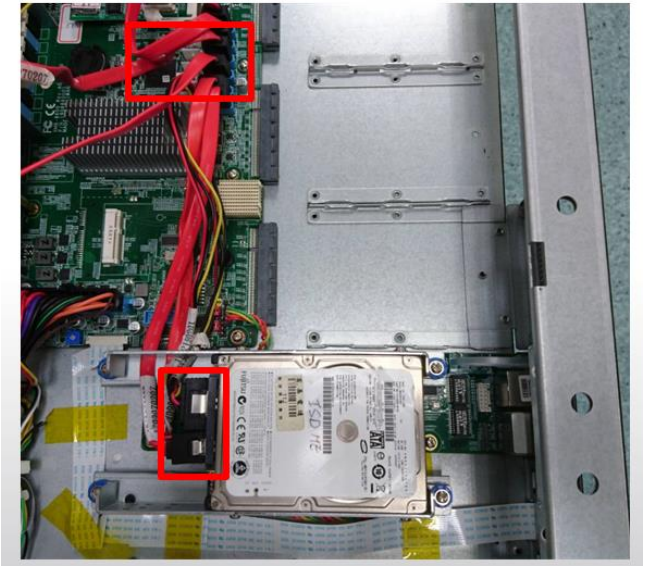
One 3.5″ Hard Drive: Use four screws to attach the brackets as shown.

7. Secure the hard drive assembly onto the chassis with four screws.

8. Connect the SATA and power cables to the hard drive(s).



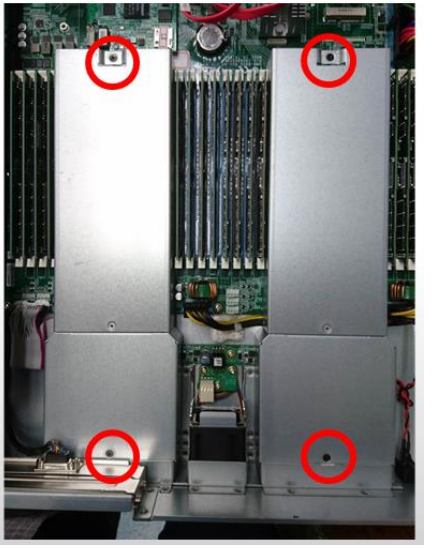
Note: Remember to attach SATA and power cables to both hard drives when installing two 2.5" HDD assembly.



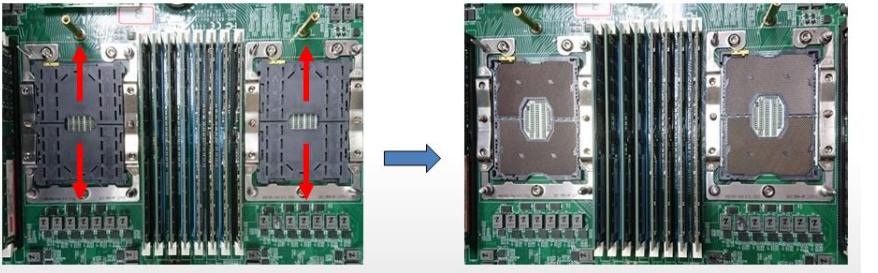
9. Follow steps in reverse order to reinstall hard drive tray and replace system lid cover.

2.6 Installing CPU and Heat Sink

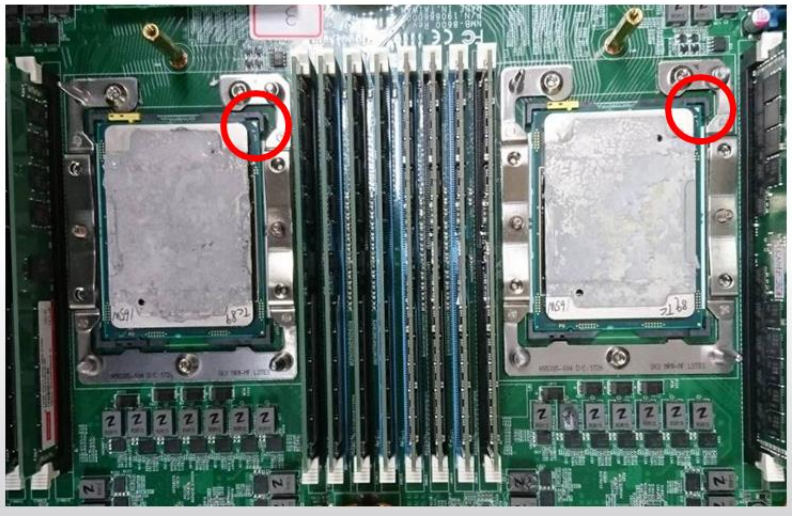
1. Remove the lid cover as per steps 1 and 2 in the previous section.
2. Loosen the four screws shown and remove the fan duct.



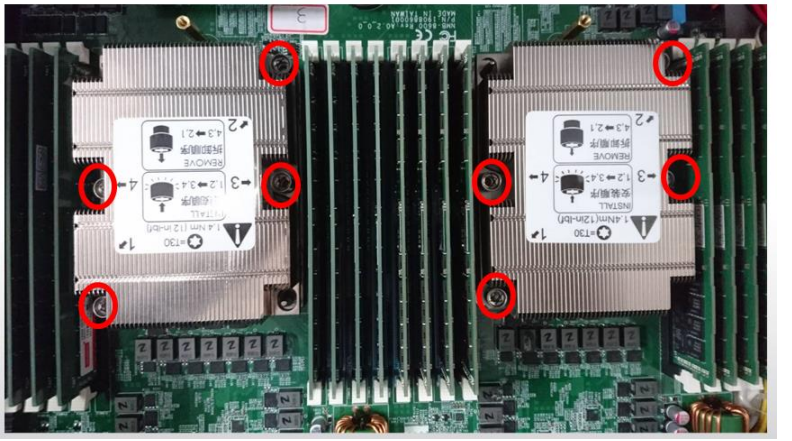
3. Remove the CPU lock cover.



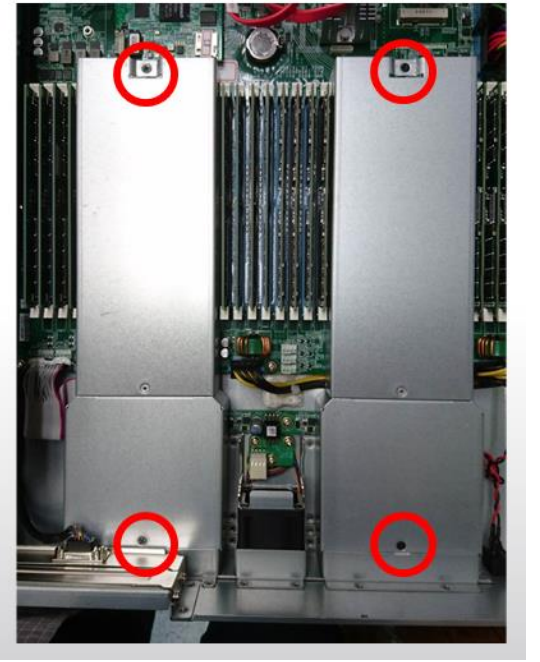
4. Place CPU onto socket. Ensure the CPU is oriented correctly by using the triangle marked on the CPU and board as highlighted in the picture. **Note:** Make sure a correct amount of thermal paste has been applied to the CPU before installing.



5. Install heat sinks. Follow the order of installation according to the instructions printed on your heat sink to avoid damaging the processor or the board.



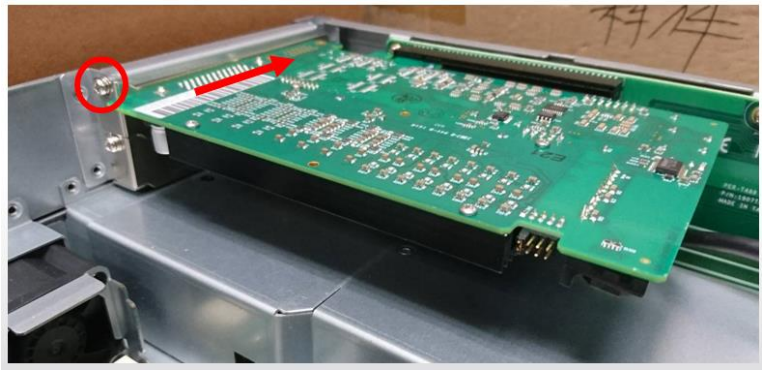
6. Replace the fan ducts and fasten the screws as shown.



2.7 Installing Expansion Card

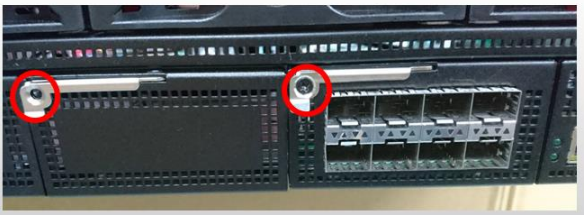
1. Remove the lid cover according to steps 1 and 2 in Chapter 2.5.
2. Remove the highlighted screw and I/O bracket.

3. Push expansion card into expansion slot. Secure to chassis using screw as shown.

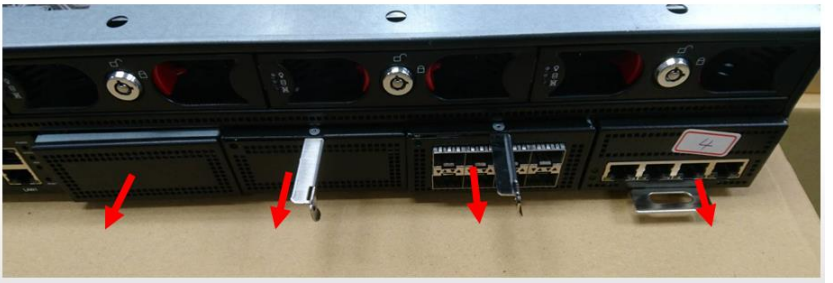


2.8 Installing Network Interface Module (NIM)

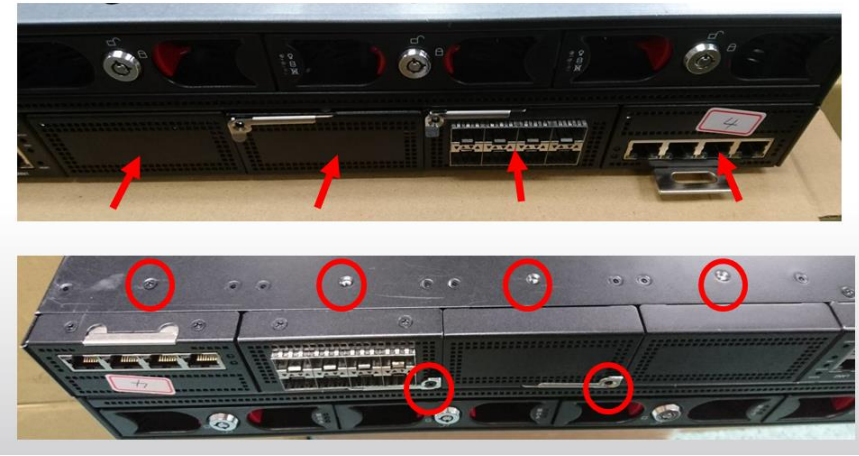
1. Remove the securing screws from the bottom and front of the chassis as shown.



2. Remove the Null Module Cover or existing NIM module.



3. Insert the NIM module or Null Module Cover. Secure with screws on bottom and front of chassis.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which are stored in the battery-backed CMOS RAM and BIOS NVRAM so the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Security – The setup administrator password can be set here

Boot – Enable/ Disable quiet Boot Option

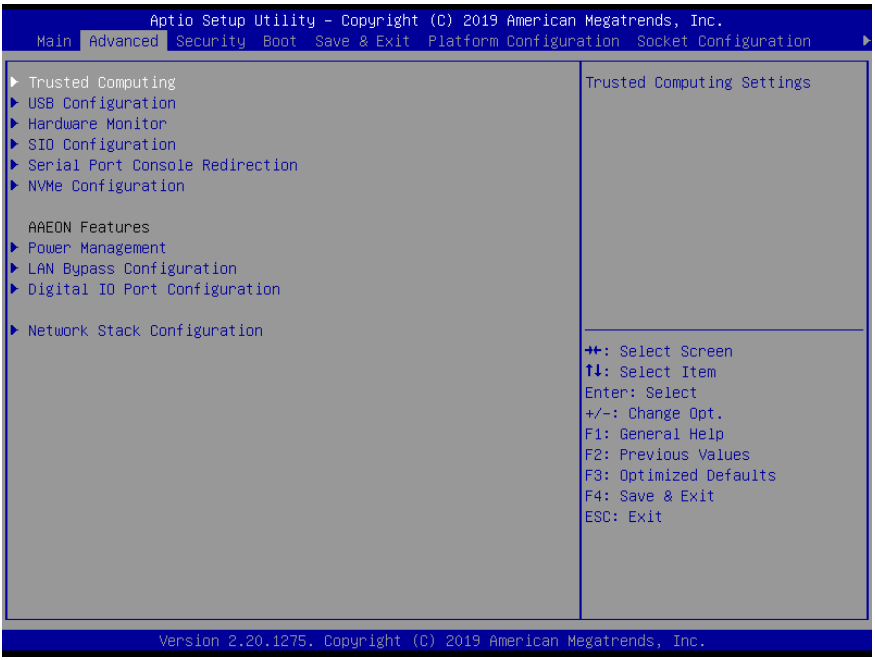
Save & Exit – Save your changes and exit the program

Platform Configuration – Displays and provides option to change the Platform System Settings

Socket Configuration - Displays and provides option to change the Socket Settings

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



3.4.1 Advanced: Trusted Computing

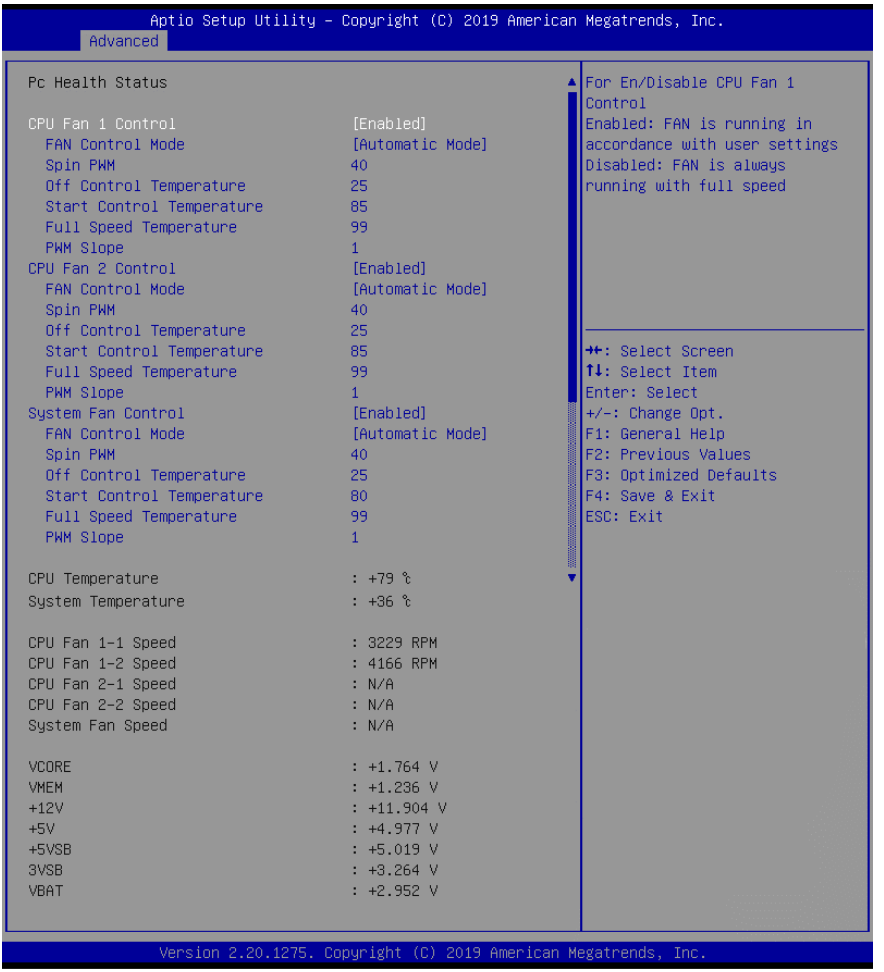
Options Summary		
Security Device Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or Disables BIOS support for security device. OS will not show Security Device. TCG EFI protocol and INT1A interface will not be available		
SHA-1 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or Disables Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or Disables Disable SHA256 PCR Bank		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Options Summary		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

3.4.2 Advanced: USB Configuration

Options Summary		
Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables Legacy USB Support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

3.4.3 Advanced: Hardware Monitor

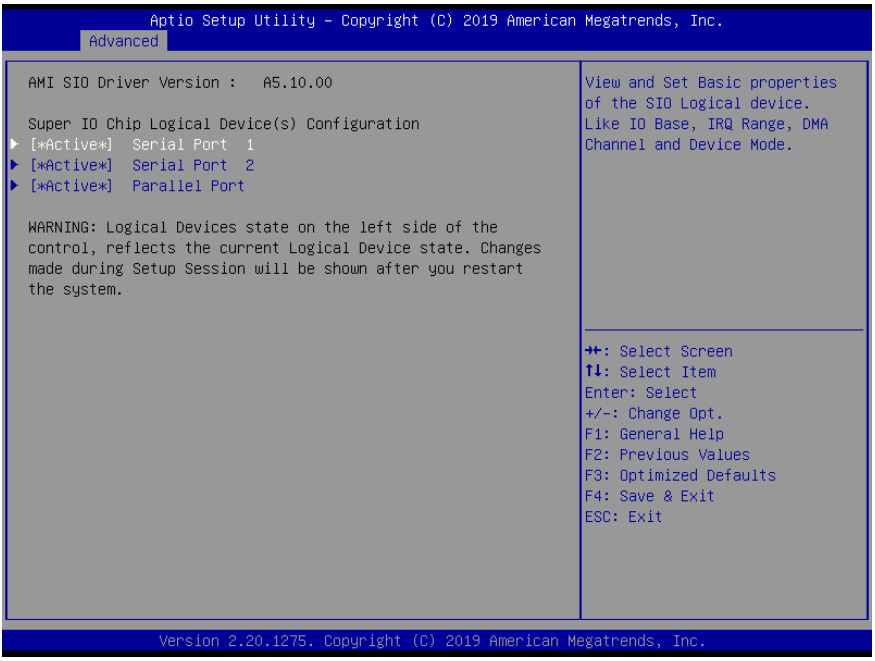


Options Summary on next Page

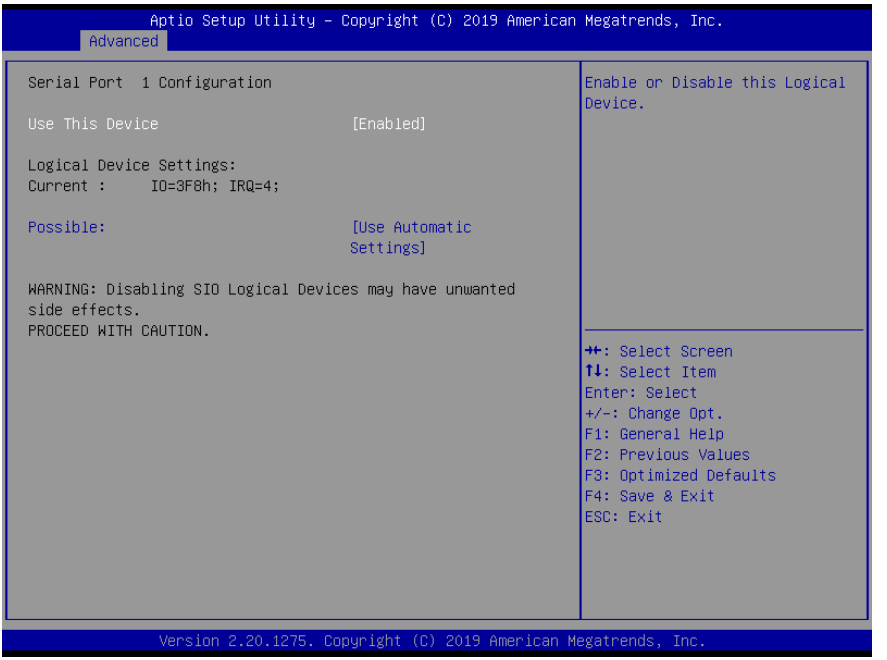
Options Summary		
CPU Fan 1 Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/ Disable CPU Fan 1 Control **Enabled:** FAN operates in accordance with user settings **Disabled:** FAN always operates at full speed		
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Manual Mode: Depends on PWM Duty Automatic Mode: FAN Speed depends on CPU Temperature		
Spin PWM	40	
The PWM Duty of FAN Spin Range: [0 - 255]		
Off Control Temperature	25	
Temperature Limit Value of Fan Off NOTE: Some fans have a minimum speed even if the PWM value is 0		
Start Control Temperature	85	
Temperature Limit Value of FAN Start Control		
Full Speed Temperature	99	
Temperature Limit Value of FAN Full Speed		
PWM Slope	1	
Slope PWM value/Degree C for FAN Speed Control. Range: [1-15]		
CPU Fan 2 Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/ Disable CPU Fan 2 Control **Enabled**: FAN operates in accordance with user settings **Disabled**: FAN always operates at full speed		
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Manual Mode: Depends on PWM Duty Automatic Mode: FAN Speed depends on CPU Temperature		
Spin PWM	40	
The PWM Duty of FAN Spin Range: [0 - 255]		
Off Control Temperature	25	
Temperature Limit Value of Fan Off NOTE: Some fans have a minimum speed even if the PWM value is 0		

Options Summary		
Start Control Temperature	85	
Temperature Limit Value of FAN Start Control		
Full Speed Temperature	99	
Temperature Limit Value of FAN Full Speed		
PWM Slope	1	
Slope PWM value/Degree C for FAN Speed Control Range: [1-15]		
System Fan Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/ Disable System Fan Control **Enabled**: FAN operates in accordance with user settings **Disabled**: FAN always operates at full speed		
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Manual Mode: Depends on PWM Duty Automatic Mode: FAN Speed depends on System Temperature		
Spin PWM	40	
The PWM Duty of FAN Spin Range: [0 - 255]		
Off Control Temperature	25	
Temperature Limit Value of Fan Off NOTE: Some fans have a minimum speed even if the PWM value is 0		
Start Control Temperature	80	
Temperature Limit Value of FAN Start Control		
Full Speed Temperature	99	
Temperature Limit Value of FAN Full Speed		
PWM Slope	1	
Slope PWM value/Degree C for FAN Speed Control Range: [1-15]		

3.4.4 Advanced: SIO Configuration

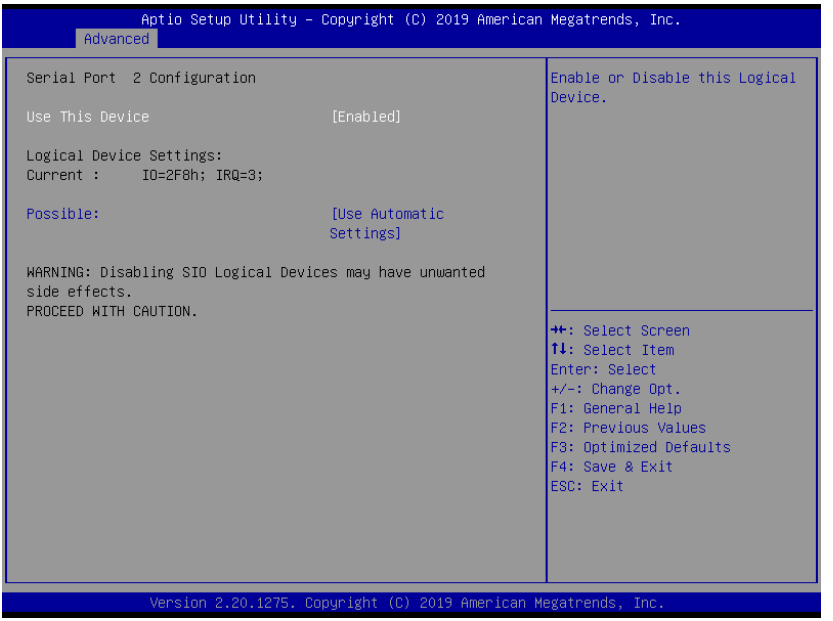


3.4.4.1 Serial Port 1 Configuration



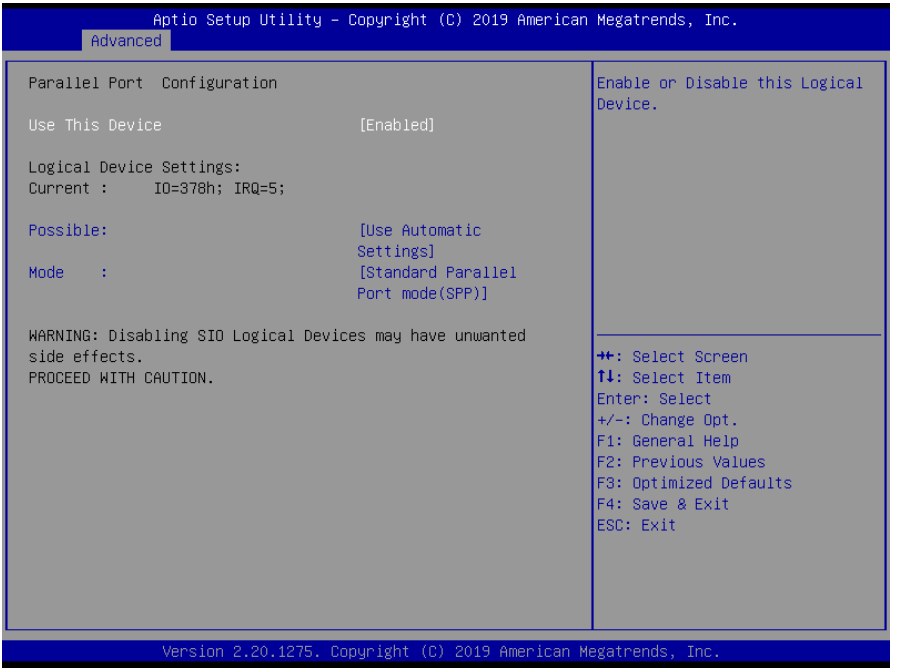
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.4.2 Serial Port 2 Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

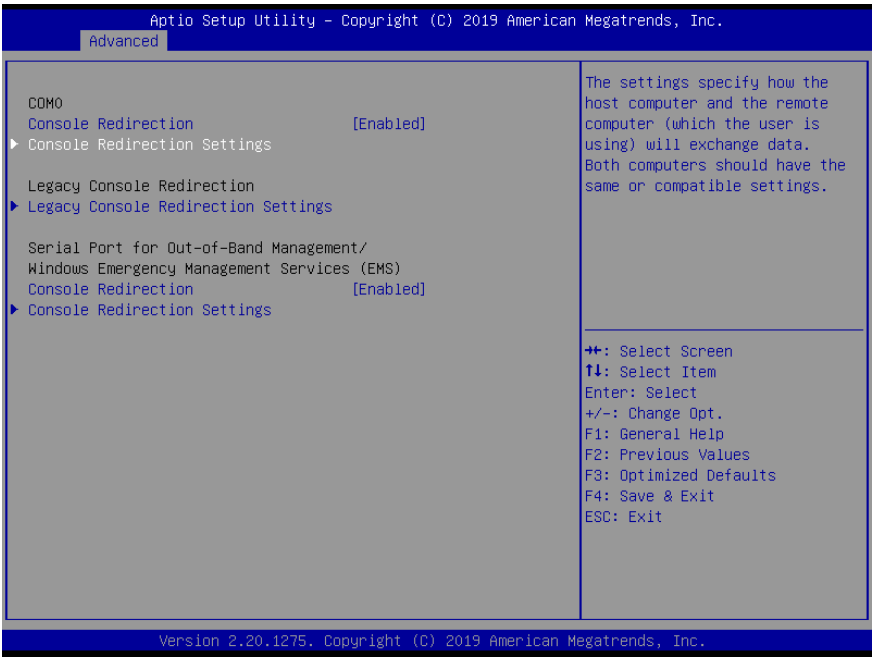
3.4.4.3 Parallel Port Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=378h; IRQ=5;	
	IO=378h; IRQ=5,6,7,9,10,11,12;	
	IO=278h; IRQ=5,6,7,9,10,11,12;	
	IO=3BCh; IRQ=5,6,7,9,10,11,12;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

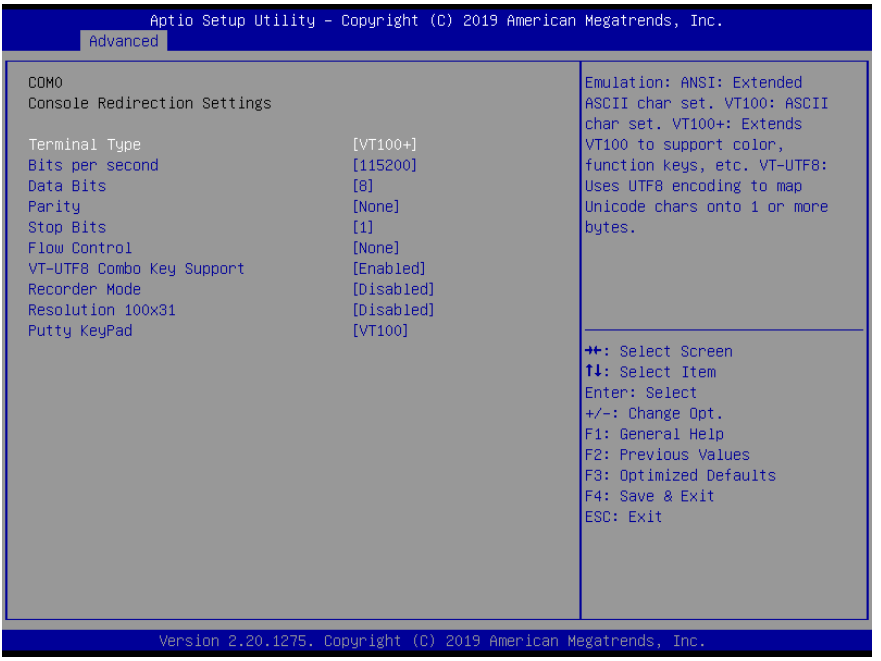
Options Summary		
Mode:	Standard Parallel Port mode (SPP)	Optimal Default, Failsafe Default
	EPP Mode	
	ECP Mode	
	EPP Mode & ECP mode	
Change Parallel Port mode. Some of the Modes required a DMA resource. After Mode changing, Reset the System to reflect actual device settings.		

3.4.5 Advanced: Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Console Redirection Settings		
The settings specify how the host computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.		
Legacy Console Redirection Settings		
Legacy Console Redirection Settings		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enabled or Disabled.		
Console Redirection Settings		
The settings specify how the host computer and remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.		

3.4.5.1 COM0 Console Redirection Settings



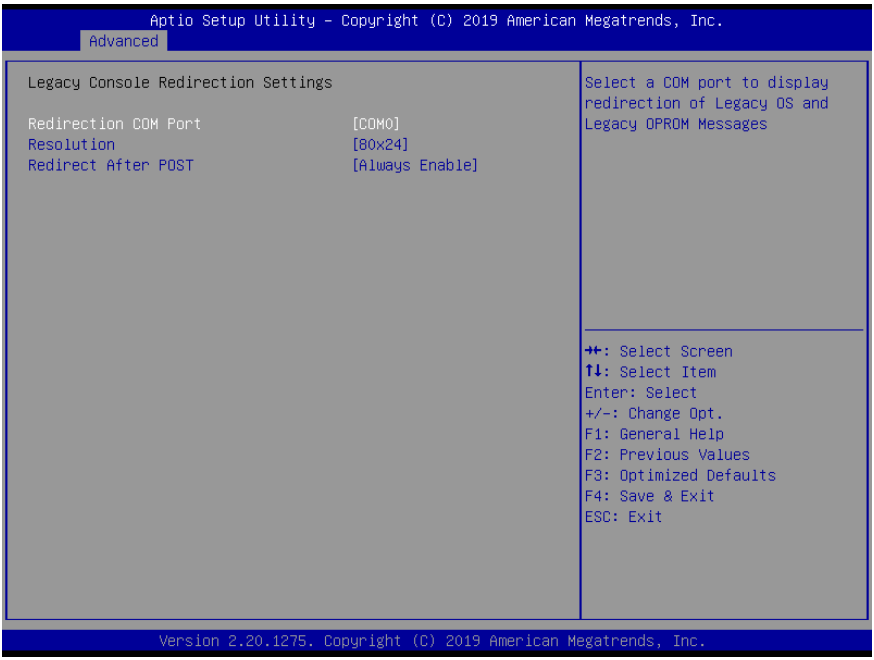
Options Summary		
Terminal Type	VT100	Optimal Default, Failsafe Default
	VT100+	
	VT-UTF8	
	ANSI	
Emulation: **ANSI**: Extended ASCII char set. **VT100**: ASCII char set. **VT100**+: Extends VT100 to support color, function keys, etc. **VT-UTF8**: Uses UTH8 encoding to map Unicode chars onto 1 or more bytes.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Options Summary		
Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. **Even**: parity bit is 0 if the number of 1's in the data bits is even. **Odd**: parity bit is 0 if the number of 1's in the data bits is odd. **Mark**: parity bit is always 1. **Space**: Parity bit is always 0. Mark and Space Parity do not allow for error detection.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled VT-UTF8 Combination key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution		

Table Continues on Next Page

Options Summary		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select Functionkey and keypad on Putty		

3.4.5.2 Legacy Console Redirection Settings



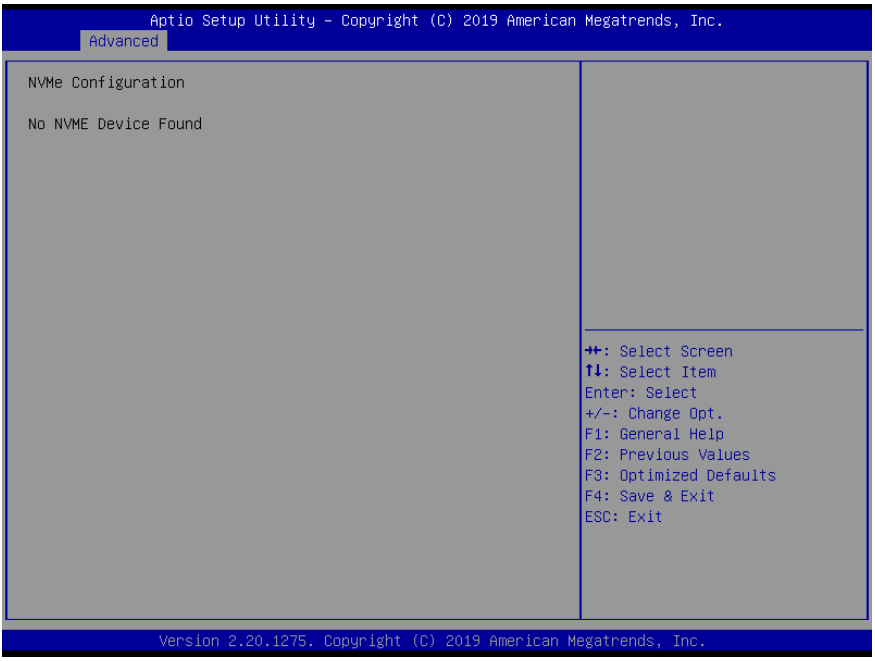
Options Summary		
Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection		
Redirect After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.		

3.4.5.3 Console Redirection Settings

Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits per second	9600	
	19200	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Options Summary		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software Xon/Xonff	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		

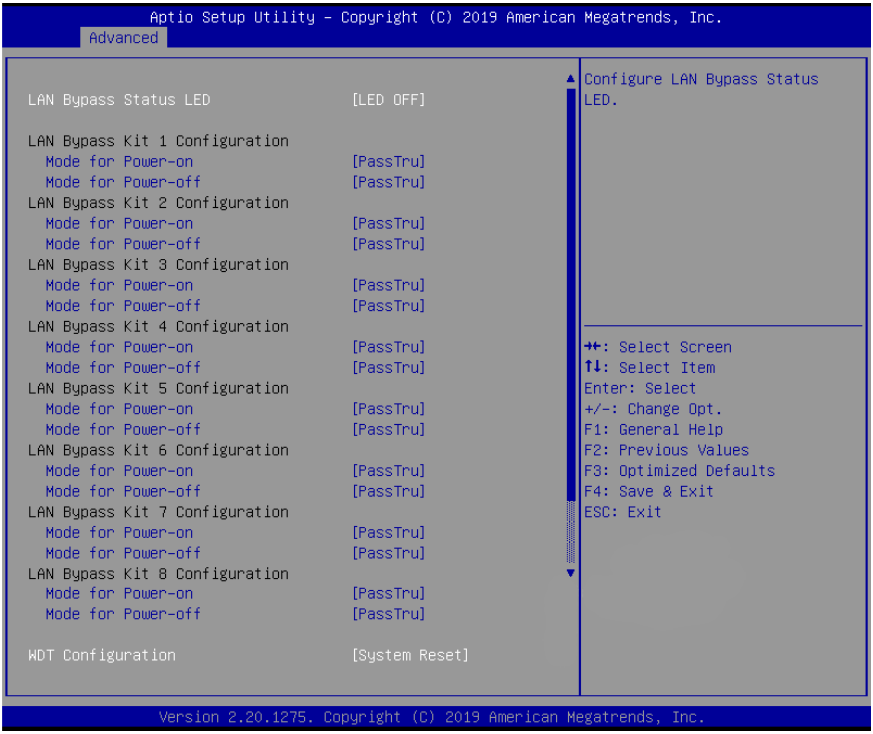
3.4.6 Advanced: NVMe Configuration



3.4.7 Advanced: Power Management

Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Enabled	
Fixed Time: System will wake on the hr::min::sec specified. **Dynamic Time**: System will wake on the current time + Increase minute(s)		

3.4.8 Advanced: LAN Bypass Configuration



Options Summary		
LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
Configure LAN Bypass Status LED.		
Mode for Power-on	PassTru	Optimal Default, Failsafe Default
	ByPass	
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through) Settings and Default apply for LAN Bypass Kit 1, 2, 3, 4, 5, 6, 7, and 8		

Options Summary		
Mode for Power-off	PassTru	Optimal Default, Failsafe Default
	ByPass	
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through) Settings and Default apply for LAN Bypass Kit 1, 2, 3, 4, 5, 6, 7, and 8		
WDT Configuration	Force ByPass	
	System Reset	Optimal Default, Failsafe Default
Configure WDT behavior , System Reset Force ByPass		

3.4.9 Advanced: Digital IO Port Configuration

Options Summary		
DIO Port1	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
DIO Port2	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		

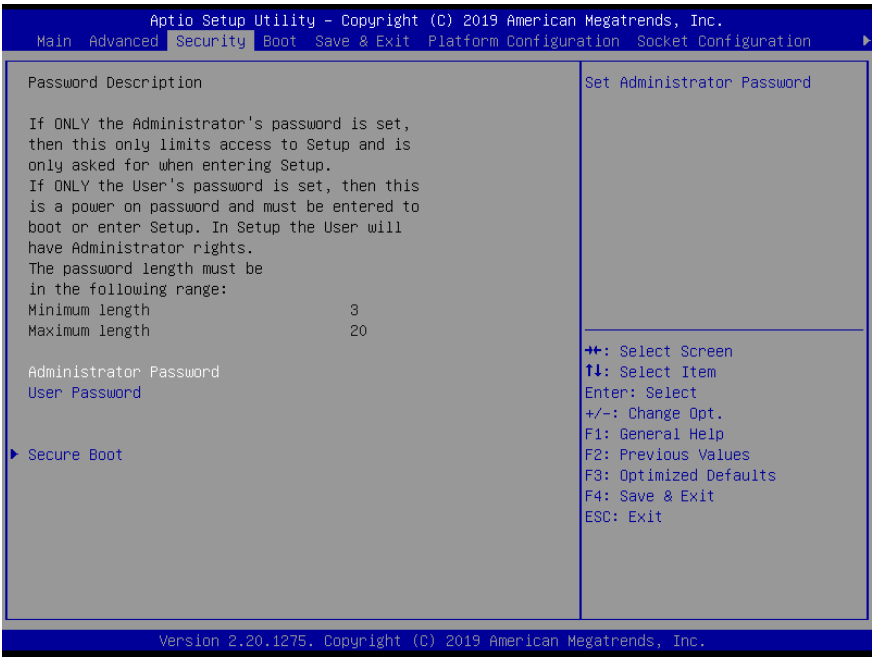
Options Summary		
DIO Port3	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
DIO Port4	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
DIO Port5	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
DIO Port6	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
DIO Port7	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
DIO Port8	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		

3.4.10 Advanced: Network Stack Configuration

Options Summary		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Set DIO as Input or Output		
Ipv4 PXE Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available		
Ipv4 HTTP Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available		
PXE boot wait time	0	Optimal Default, Failsafe Default
Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.		

Options Summary		
Media detect count	1	Optimal Default, Failsafe Default
Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.		

3.5 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

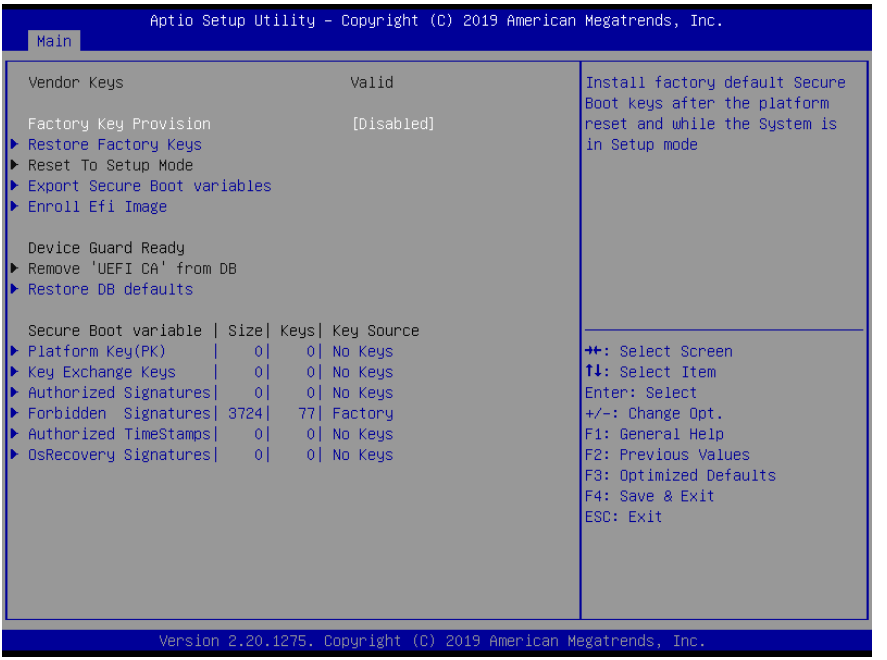
Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.5.1 Security: Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	YES	Optimal Default, Failsafe Default
	NO	
Force System to User Mode. Install factory default Secure Boot key databases		

3.5.1.1 Key Management



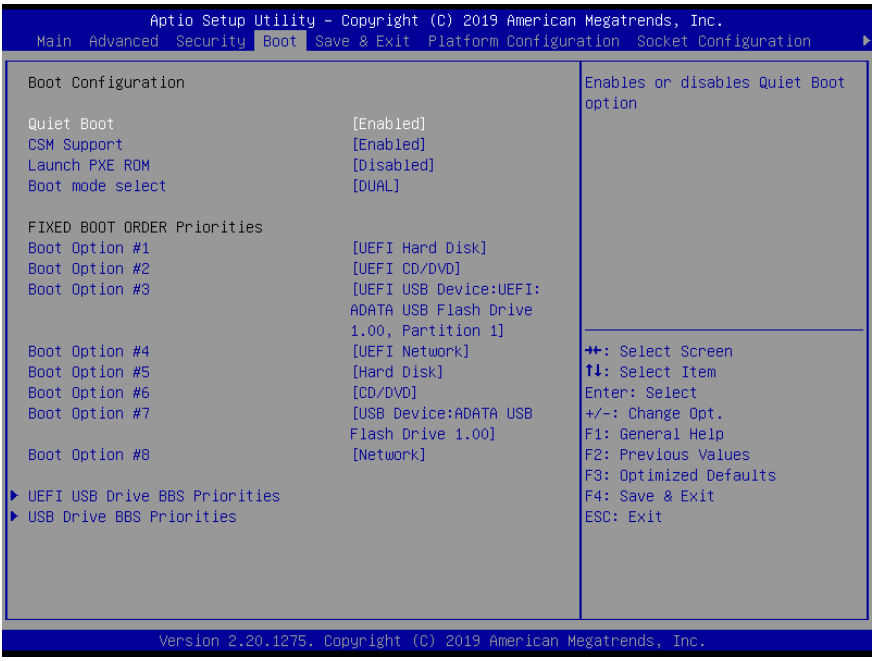
Options Summary		
Factory Keys Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot krys after the platform reset and while the System is in Setup mode		
Export Secure Boot variables	OK	Optimal Default, Failsafe Default
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image	OK	Optimal Default, Failsafe Default
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		
Restore DB defaults	YES	Optimal Default, Failsafe Default
	NO	
Restore DB variable to factory defaults		

Options Summary		
Platform Key(PK)	Update	Optimal Default, Failsafe Default
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory, External, Mixed		
Key Exchange Keys	Update	Optimal Default, Failsafe Default
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory, External, Mixed		
Authorized Signatures	Update	Optimal Default, Failsafe Default
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory, External, Mixed		

Table Continues on Next Page

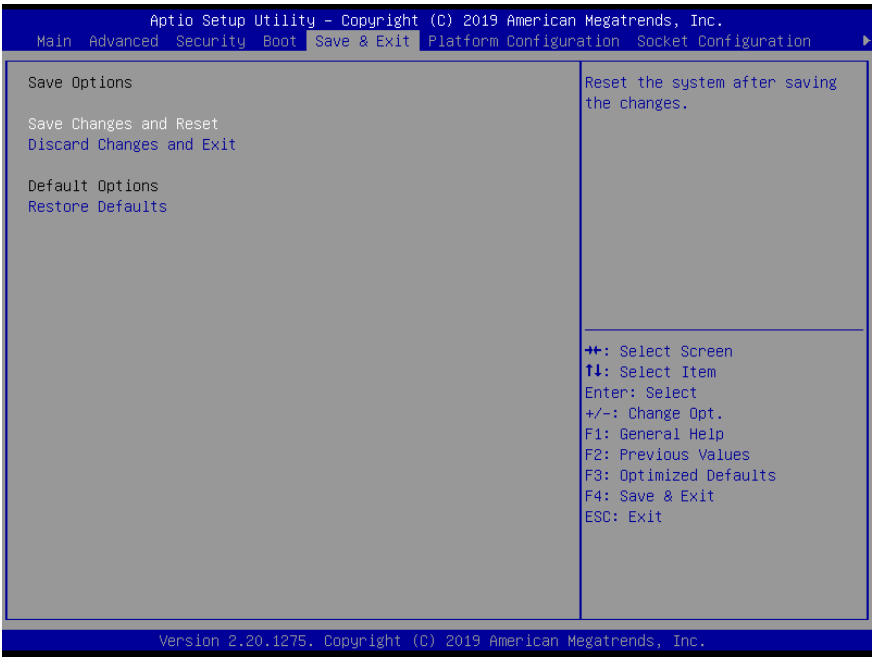
Options Summary		
Forbidden Signatures	Details	Optimal Default, Failsafe Default
	Export	
	Update	
	Append	
	Delete	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory, External, Mixed		
Authorized TimeStamps	Update	Optimal Default, Failsafe Default
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory, External, Mixed		
OsRecovery Signatures	Update	Optimal Default, Failsafe Default
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) b)EFI_CERT_RSA2048 (bin) b)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source Factory ,External, Mixed		

3.6 Setup Submenu: Boot

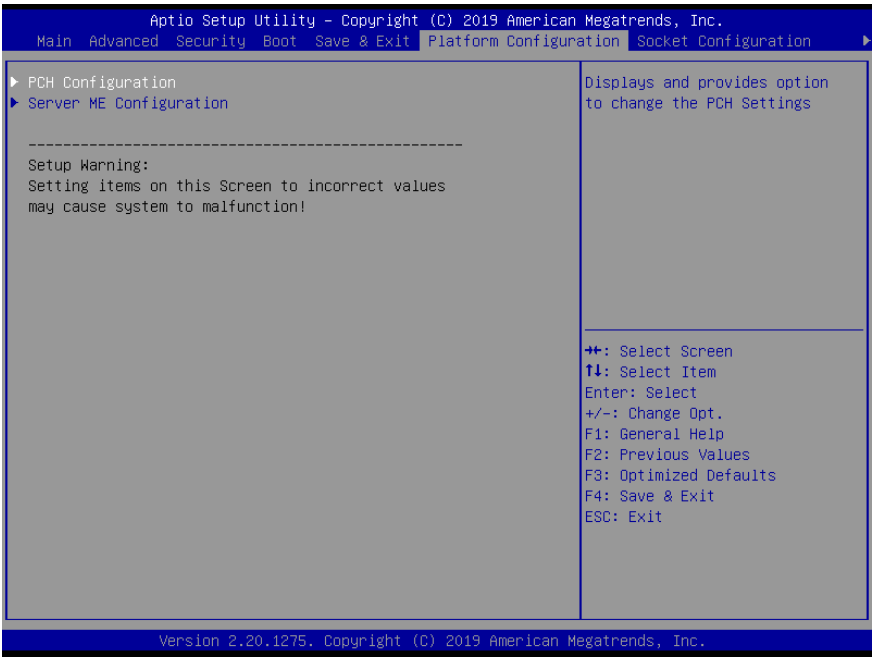


Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Quiet Boot option		
CSM Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CSM Support.		
Launch PXE ROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of Legacy Network OpROM Note: UEFI PXE boot is controlled by Network.		
Boot mode select	LEGACY	
	UEFI	
	DUAL	Optimal Default, Failsafe Default
Select boot mode LEGACY/UEFI		

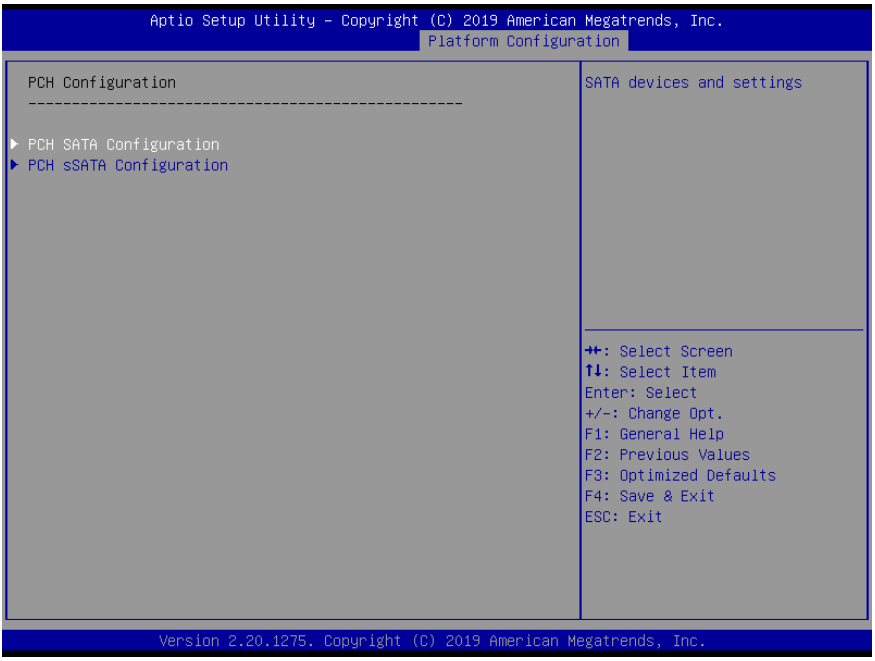
3.7 Setup Submenu: Save & Exit



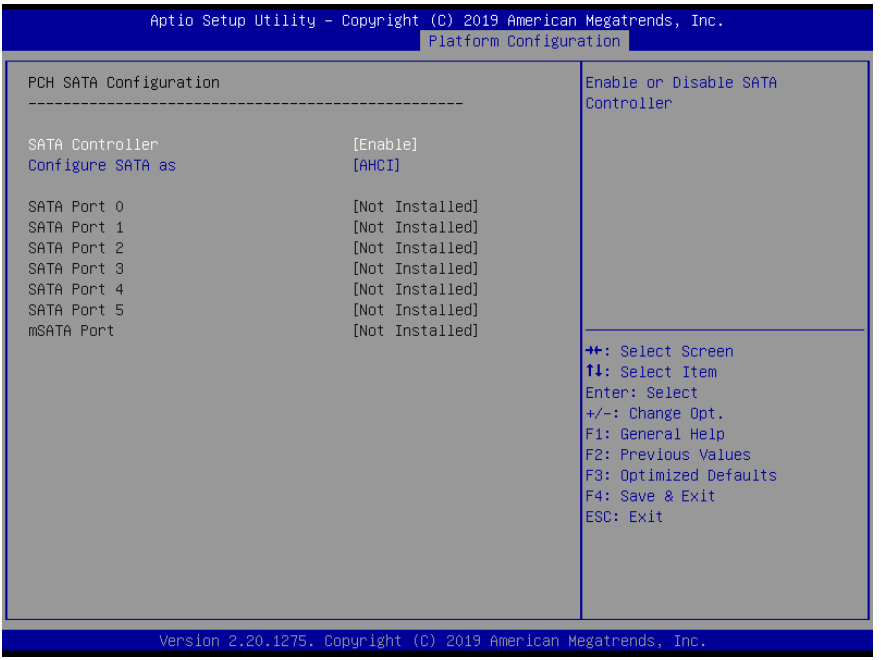
3.8 Setup Submenu: Platform Configuration



3.8.1 Platform Configuration: PCH Configuration

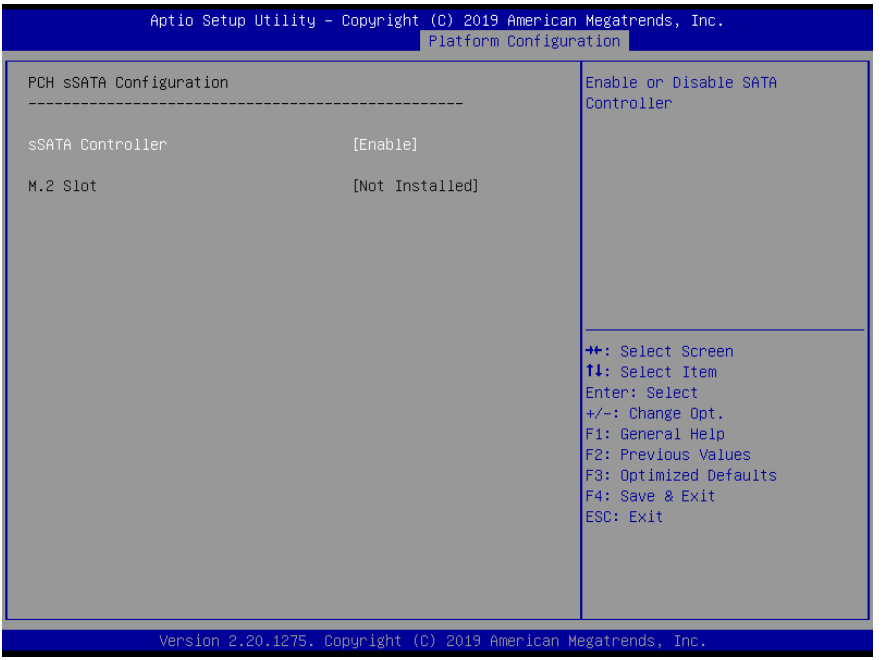


3.8.1.1 PCH SATA Configuration



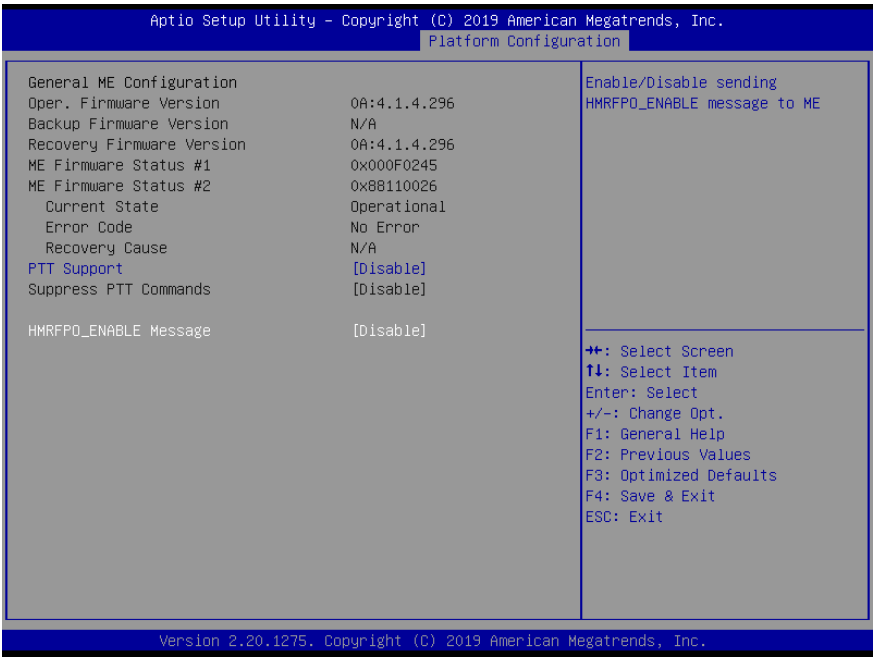
Options Summary		
SATA Controller	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables SATA Controller		
Configure SATA as	AHCI	Optimal Default, Failsafe Default
	RAID	
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive		

3.8.1.2 PCH sSATA Configuration



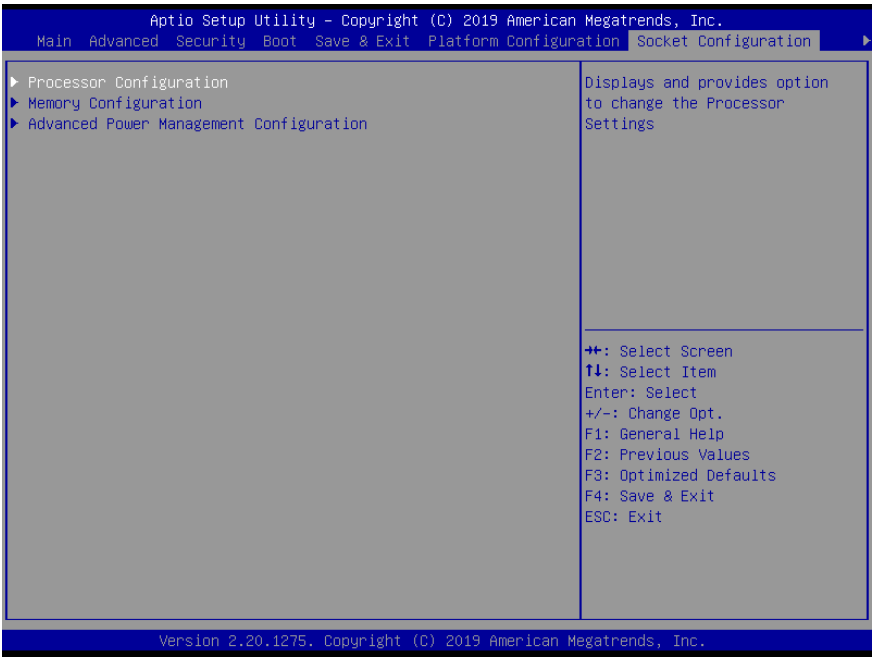
Options Summary		
sSATA Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enables or Disables SATA Controller		

3.8.2 Platform Configuration: Server ME Configuration



Options Summary		
PTT Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/ Disable Platform Trusted Technology (PTT) support		
HMRFPO_ENABLE Message	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/ Disable sending HMRFPO_ENABLE message to ME		

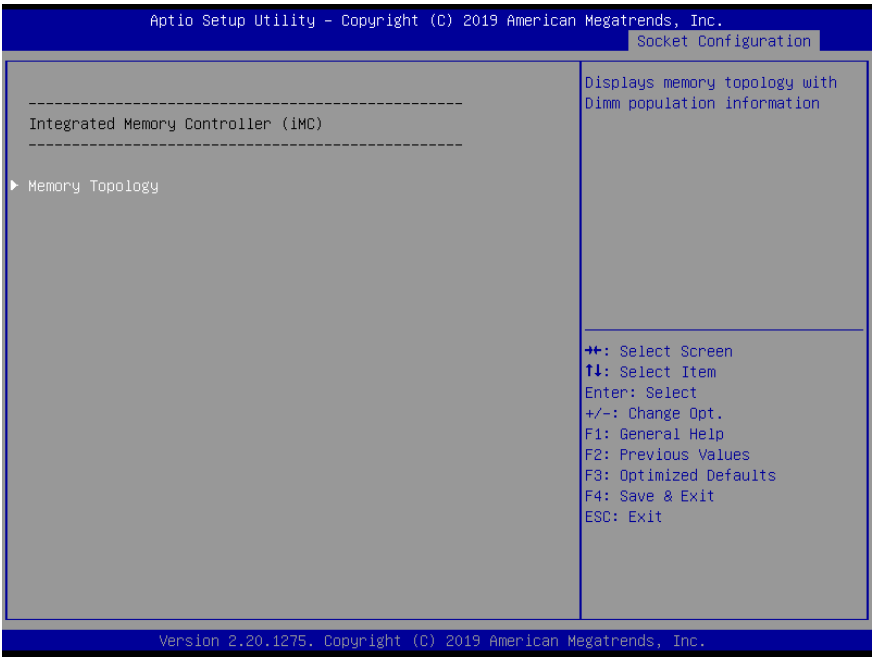
3.9 Setup Submenu: Socket Configuration



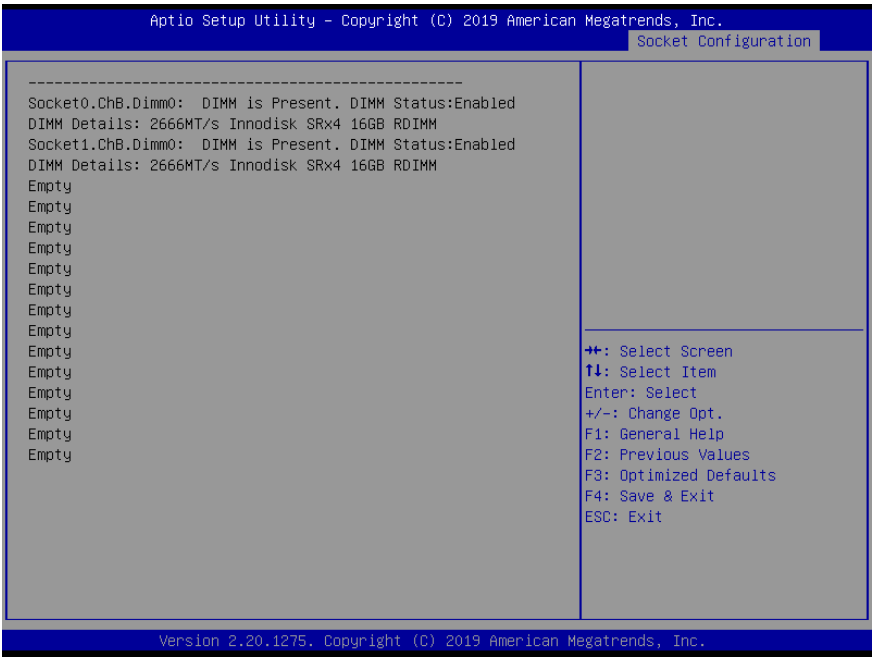
3.9.1 Socket Configuration: Processor Configuration

Options Summary		
Hyper-Threading [ALL]	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables Hyper Threading (Software Method to Enable/Disable Logical Processor threads.		

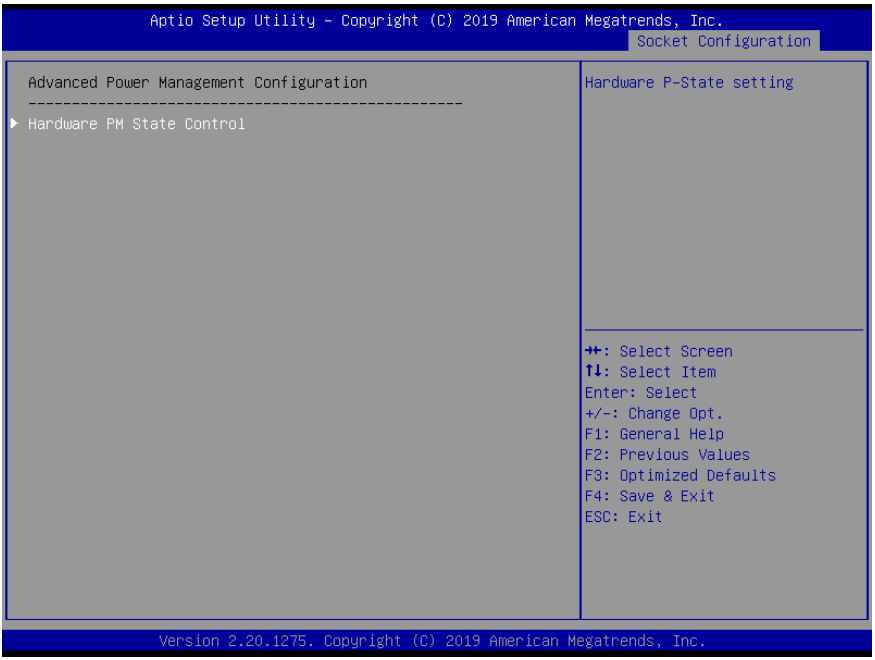
3.9.2 Socket Configuration: Memory Configuration



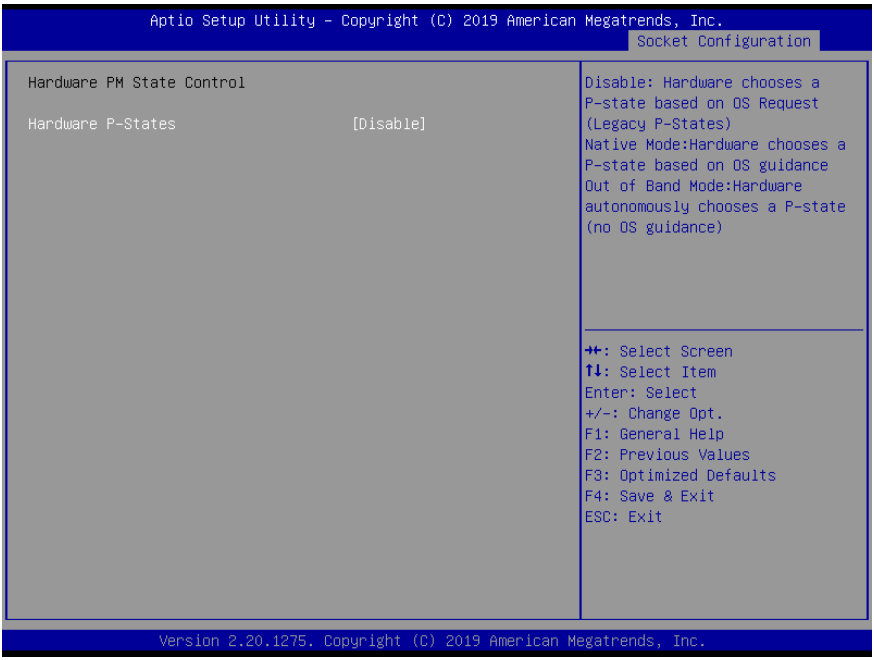
3.9.2.1 Memory Topology



3.9.3 Socket Configuration: Advanced Power Management Configuration



3.9.3.1 Hardware PM State Control



Options Summary		
Hardware	Disabled	Optimal Default, Failsafe Default
	Native Mode	

Disabled: Hardware chooses a P-state based on OS Request (Legacy P-States)
Native Mode: Hardware chooses a P-state based on OS guidance
Out of Band Mode: Hardware autonomously chooses a P-state (no OS guidance)

Chapter 4

Drivers Installation

4.1 Drivers Installation

The drivers can be found on the FWS-8600 product page at aaeon.com. Please follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers (Windows)

1. Open the folder **Step 1 – Chipset**
2. Open **SetupChipset.exe**
3. Follow the instructions
4. Drivers will be installed automatically

Step 1 – Install LAN Drivers (Linux)

1. Open the folder **Step 2 – LAN**
2. Open **README**
3. Follow the instructions to install LAN drivers

Appendix A

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	4(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*****************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*****************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig ( ){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       Switch(SIOIndex){
              Case 0x2E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0x55);
                        Break;
              Case 0x4E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0xAA);
                     Break;
       }
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0x02);
       IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}
*****************************************************************************
```

```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

B.1 Status LED

The FWS-8600 features a programmable LED status indicator. The LED can be programmed using the AAEON SDK.

B.1.1 Status LED Configuration

Table 1: Status LED Settings Table

STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table 2: Status LED Relative Register Mapping Table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

B.1.2 Sample Code

```
************************************************************
#define Byte  CPLD_SLAVE_ADDRESS     //This parameter is
represented from Note1
#define Byte  OFFSET             //This parameter is represented
from Note2
************************************************************
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
     //LED Off
     //BIT2=0, BIT1=0, BIT0=0
     bData = bData & 0xF8;
     break;
}
case 1:
{
     //Red LED On
     //BIT2=0, BIT1=0, BIT0=1
     bData = (bData & 0xF8) | 0x01;
     break;
}
case 2:
{
     //Red LED Blink
     //BIT2=0, BIT1=1, BIT0=0
     bData = (bData & 0xF8) | 0x02;
     break;
}
case 3:
{
     //Red LED Fast Blink
     //BIT2=0, BIT1=1, BIT0=1
     bData = (bData & 0xF8) | 0x03;
     break;
}
case 4:
```

```
{
     //Green LED On
     //BIT2=1, BIT1=1, BIT0=1
     bData = (bData & 0xF8) | 0x07;
     break;
}
case 5:
{
     //Green LED Blink
     //BIT2=1, BIT1=0, BIT0=1
     bData = (bData & 0xF8) | 0x05;
     break;
}
case 6:
{
     //Green LED Fast Blink
     //BIT2=1, BIT1=1, BIT0=0
     bData = (bData & 0xF8) | 0x06;
     break;
}
default:
     break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
************************************************************
```

B.2 LAN Bypass

The FWS-8600 features a LAN Bypass kit, allowing for uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

B.2.1 LAN Bypass Configuration

Table 1 : ID Select table of LAN kit				
LAN_ID3	LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	0	LAN Kit 1 Selected
0	0	0	1	LAN Kit 2 Selected
0	0	1	0	LAN Kit 3 Selected
...				...
1	1	1	1	LAN Kit 16 Selected

Table 2 : LAN Bypass relative register table	
Function	Description
LAN_ID3 LAN_ID2 LAN_ID1 LAN_ID0	Use for selecting which LAN kit will be configured, refer to Table 1 ID Select table of LAN kit. They should be set before ACT_EN.
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3 : LAN Bypass relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

B.2.2 Sample Code

```
************************************************************
#define Byte  CPLD_SLAVE_ADDRESS     //This parameter is
represented from Note1
#define Byte  OFFSET            //This parameter is represented
from Note2
************************************************************
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
     bData = bData | 0x08;
else
     bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
     bData = bData | 0x04;
else
     bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
     bData = bData | 0x02;
else
     bData = bData & 0xFD;
// Set Reg01h bit0
```

```
if(bLanSel & 0x01)
     bData = bData | 0x01;
else
     bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)  // Pass Through
     bData = bData & 0xBF;
else                  // Bypass
     bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)  // Pass Through
     bData = bData & 0xDF;
else                  // Bypass
     bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET) // Reset
     bData = bData & 0xEF;
else              // Bypass
     bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
************************************************************
```

B.3 Software Button (General Purpose Input)

The FWS-8600 system features a general purpose input button which can be programmed with the AAEON SDK.

B.3.1 Software Button Configuration

Table 1 : Software Button register mapping table				
	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

Table 2: Software Button register	
Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

B.3.2 Sample Code

```
************************************************************
#define Word  BTN_STS   //This parameter is represented from
Note1
#define Byte  BTN_STS_R     //This parameter is represented
from Note2
************************************************************
Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
     BYTE TmpValue;

     TmpValue = inportb (IoAddr);
return  (TmpValue & (1 << BitNum))
}
************************************************************
VOID  Main(){
     Byte RstBtn;

     RstBtn = GET_Value (BTN_STS, BTN_STS_R);     // Active
Low
}
************************************************************
```