

FWS-8500

Network Appliance

User's Manual 1st Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-8500	1
● EAR bracket kit	1
● Console cable	1
● SATA cable	1
● SATA power cable	1
● CPU cooler	2

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注： 一、此产品所标示之环保使用期限，系指在一般正常使用状况下。 二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。</p>						

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products
AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1 - Product Specifications	1
1.1 Specifications.....	2
Chapter 2 – Hardware Information	5
2.1 Dimensions	6
2.2 Jumpers and Connectors.....	10
2.3 List of Jumpers	12
2.3.1 Auto PWRBTN selection (JP1)	13
2.3.2 CF Power Selection (JP3)	13
2.3.3 CMOS Setting Selection (CMOS1)	13
2.4 List of Connectors.....	14
2.4.1 Power Switch Header (CN5)	15
2.4.2 LCM Connector (CN7)	15
2.4.3 State LED Header (CN11).....	15
2.4.4 20-pin Smart Fan (CN15)	16
2.4.5 State LED Header (CN25).....	16
2.4.6 Digital I/O (DIO1).....	16
2.4.7 Front Panel Connector 1 (FP1).....	18
2.4.8 Front Panel Connector 2 (FP2).....	18
2.5 Installing 2.5" Hard Disk Drives (2 Pieces)	19
2.6 Installing 3.5" Hard Disk (1 Piece)	23
2.7 Installing CPU and Heat Sink.....	26
2.8 Installing Network Interface Module	29
Chapter 3 - AMI BIOS Setup	31
3.1 System Test and Initialization	32
3.2 AMI BIOS Setup	33
3.3 Setup Submenu: Main.....	34

3.4	Setup Submenu: Advanced.....	35
3.4.1	Advanced: SATA Configuration.....	36
3.4.2	Advanced: USB Configuration	37
3.4.3	Advanced: Serial Port Console Redirection.....	38
3.4.3.1	Serial Port Console Redirection: COM0 Console Redirection Settings.....	39
3.4.3.2	Serial Port Console Redirection: Legacy Console Redirection Settings.....	42
3.4.4	Advanced: Hardware Monitor.....	43
3.4.5	Advanced: Smart Fan.....	44
3.4.6	Advanced: LAN Bypass Configuration	46
3.5	Setup submenu: IntelRCSetup.....	48
3.5.1	IntelRCSetup: Processor Configuration.....	49
3.5.2	IntelRCSetup: Memory Configuration.....	50
3.6	Setup submenu: Security	51
3.7	Setup submenu: Boot.....	52
3.8	Setup submenu: Exit	53
Chapter 4 – Drivers Installation.....		54
4.1	Drivers Installation	55
Appendix A - Watchdog Timer Programming.....		56
A.1	Watchdog Timer Initial Program	57

Chapter 1

Product Specifications

1.1 Specifications

System

- **Processor** Dual Intel® Xeon® E5 2600 v3 Series
- **System Memory** Dual 288-pin DDR4 1600/1866/2133 MHz
DIMM x 16 (8 DIMM per CPU), RDIMM, up to 512 GB
- **Chipset** Intel® Communications Chipset 8925
- **Ethernet** Onboard RJ-45 GbE port x 1 (optional up to 2)
Expandable up to 64 ports of GbE via network interface modules
- **BIOS** AMI BIOS
- **Serial ATA** SATA 3.0 Gb/s x 2
CompactFlash x 1
- **SSD** -
- **Expansion Interface** Mini-PCIe x 1
PCI [x8] slot x 2 (optional)
- **TPM** TPM v1.2
- **Watchdog Timer** System reset: 1 ~ 255 step software programming
- **RTC** Internal RTC
- **Storage** Internal 3.5" SATA HDD x 1 or 2.5" SATA HDD x 2
CompactFlash x 1
- **Cooling** Hot-swappable cooler with smart fan control x

	5
	Internal cooler without smart fan x 1
● Front Panel I/O	Power LED x 1
	Status LED x 1
	HDD active LED x 1
	USB port x 2
	RJ-45 GbE port x 1
	RJ-45 console x 1
	Parallel LCM display and 4-key keypad x 1
	Software programmable button x 1
● Rear Panel I/O	650 W redundant power x 1
	Power switch x 1
	Rear expansion slot (optional PCIe [x8]) x 2
● Color	Black
● Power Supply	650 W redundant power (AC power input)
● Power Requirement	24-pin ATX power connector compatible with
	4-pin ATX 12 V power connector x 1
	8-pin ATX 12 V power connector x 2
	4-pin DC power-out connector for HDD x 2
● Dimension	444 x 88 x 600 mm (16.93 x 3.46 x 23.62")

Display

- VGA Controller -

I/O

- Serial Port RJ-45 console x 1

- Keyboard and Mouse COM2: 5x2 box header (2.0 mm) x 1 (optional)
-
- USB USB 2.0 x 4: USB 2.0 type A x 2 (on I/O side), USB internal pin header x 2 (optional)
- GPIO 8-bit, BIOS default 4-bit input, 4-bit output

Environmental

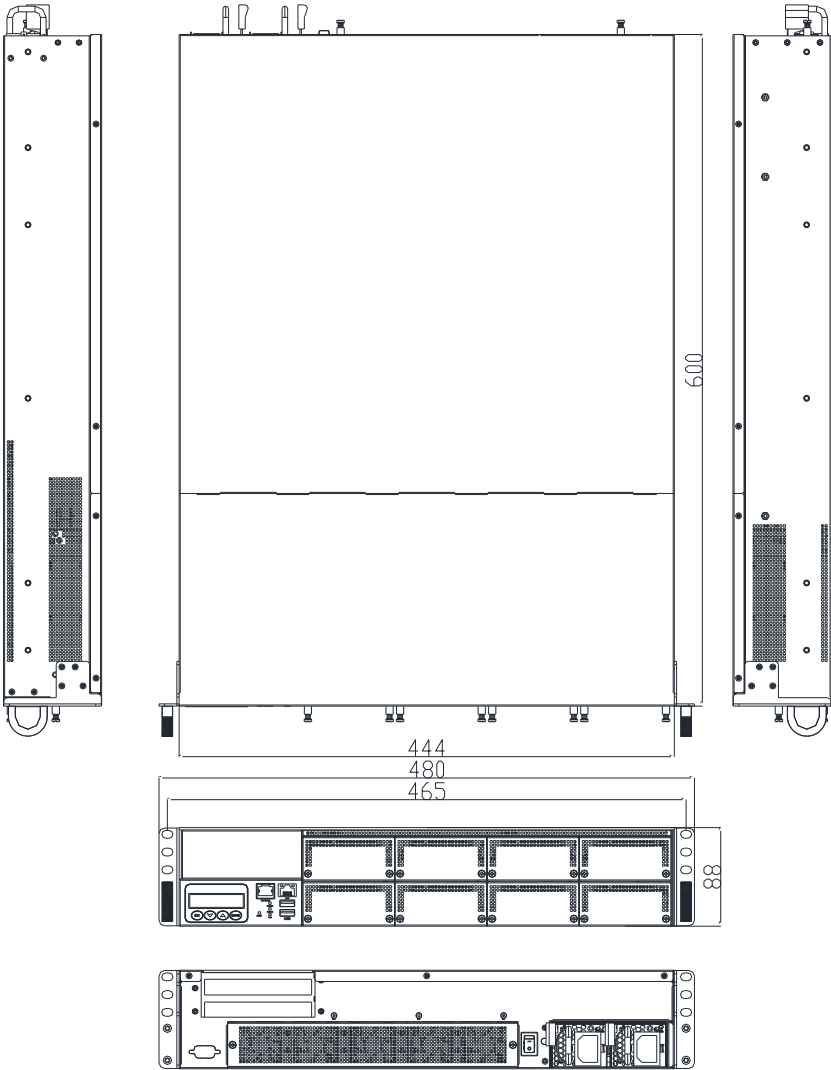
- Operating Temperature 0 ~ 40°C (32 ~ 104°F)
- Storage Temperature -20 ~ 60°C (-4 ~ -140°F)
- Operating Humidity 10 ~ 80% relative humidity, non-condensing
- Storage Humidity 10 ~ 80% @ 40°C, non-condensing
- Anti-Vibration 0.5 Grms/ 5 ~ 500 Hz/ operation (2.5" HDD)
1.5 Grms/ 5 ~ 500 Hz/ No operation
- Anti-Shock 10 G peak acceleration (11 msec. duration), operation
20 G peak acceleration (11 msec. duration), non-operation
- EMC CE/FCC class A

Chapter 2

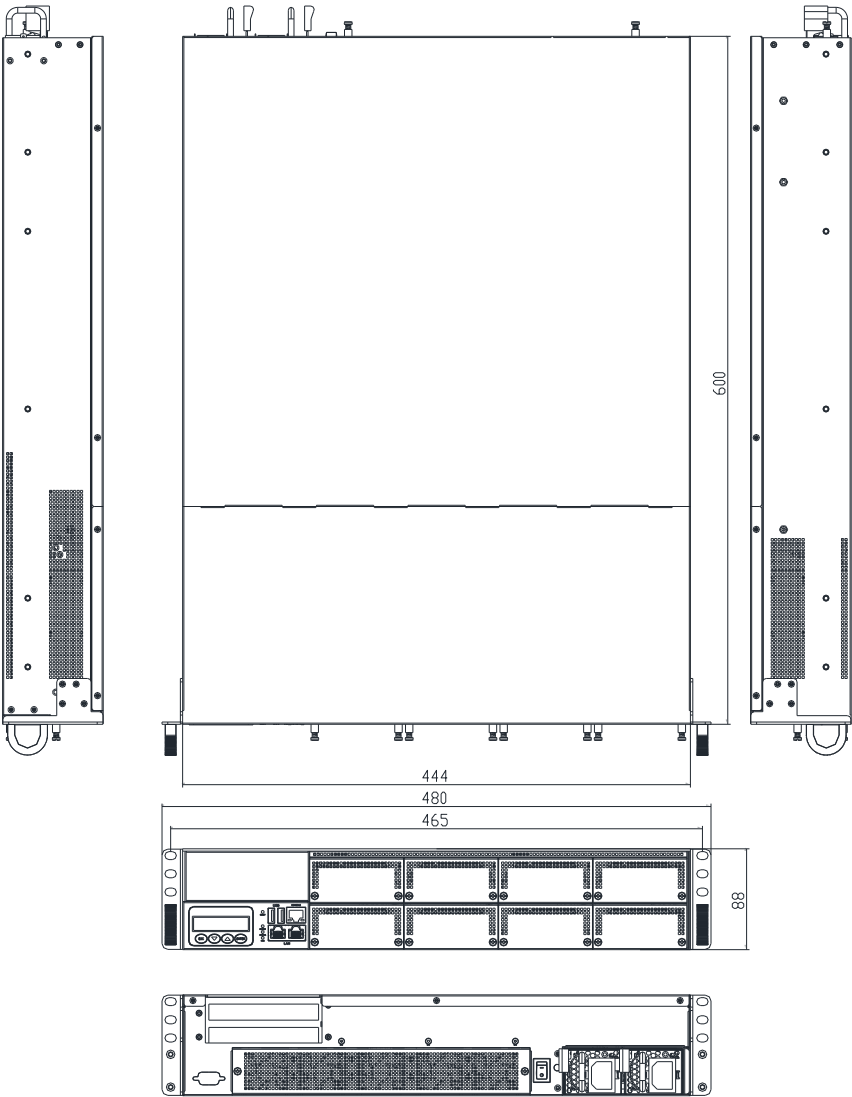
Hardware Information

2.1 Dimensions

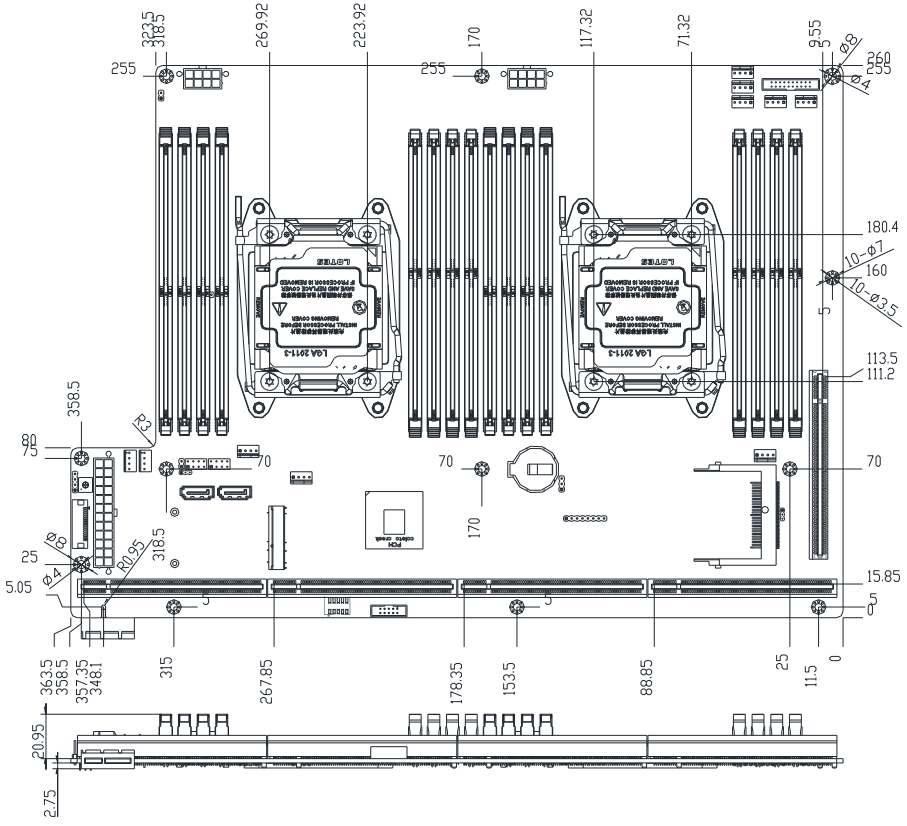
System - One onboard GbE LAN Model

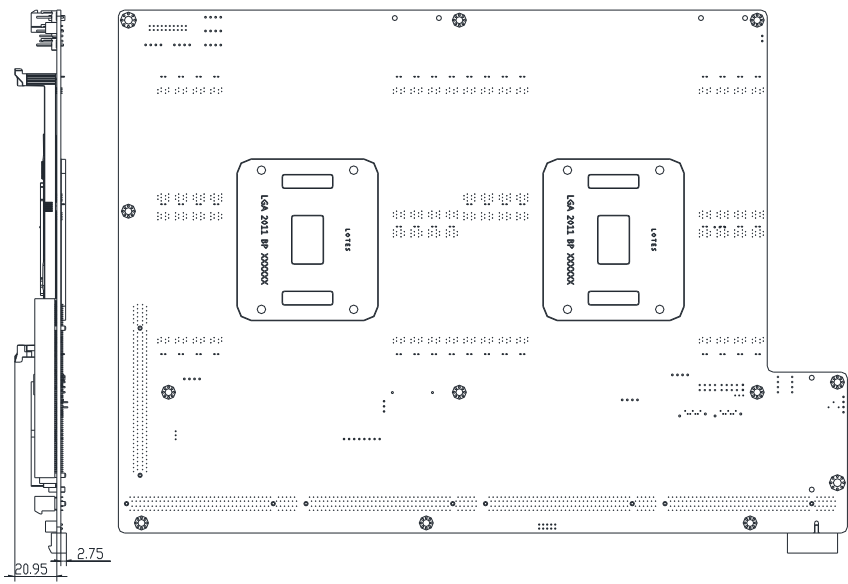


Two optional onboard GbE LAN model



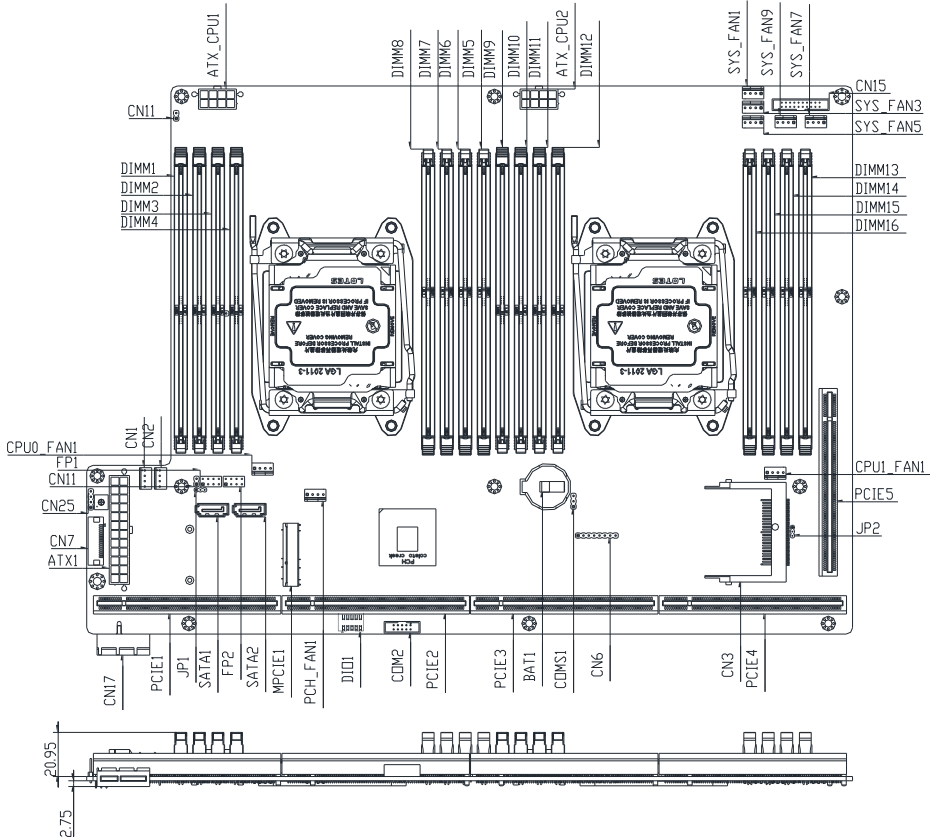
Board



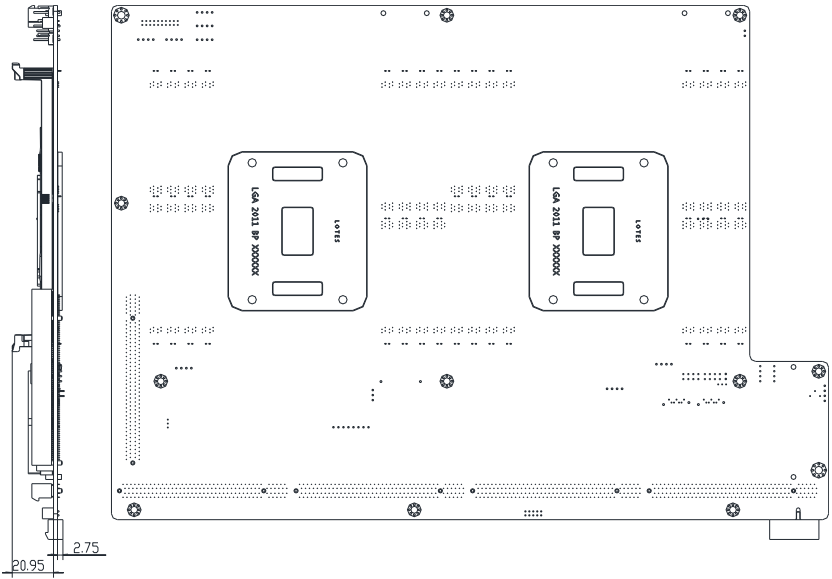


2.2 Jumpers and Connectors

Component Side



Solder Side

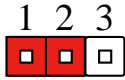


2.3 List of Jumpers

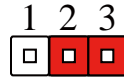
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	Auto PWRBTN selection
JP3	CF power selection
CMOS1	CMOS setting selection

2.3.1 Auto PWRBTN selection (JP1)

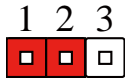


Disabled (Default)

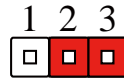


Enabled

2.3.2 CF Power Selection (JP3)

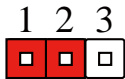


+5V (Default)

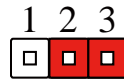


+3.3 V

2.3.3 CMOS Setting Selection (CMOS1)



Normal (Default)



Clear CMOS

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1~2	SATA power
CN3	CF card socket
CN5	Power switch header
CN7	LCM connector
CN11	State LED header
CN15	20-pin smart fan
CN25	Keypad connector
ATX1	24-pin ATX power supply input
ATX_CPU1~2	8P ATX power supply input
CPU0_FAN1	4-pin fan
CPU1_FAN1	4-pin fan
COM2	COM port
DIO1	Digital I/O
DIMM1~16	DDR4 RDIMM socket
FP1	Front panel connector 1
FP2	Front panel connector 2
MPCIE1	Mini PCIe socket
PCH_FAN1	4-pin FAN
SATA3G_1~2	SATA3G interface
SYS_FAN1,3,5,7,9	4-pin smart fan

2.4.1 Power Switch Header (CN5)

Pin	Signal	Pin	Signal
1	Power Button	2	GND

2.4.2 LCM Connector (CN7)

Pin	Signal	Pin	Signal
1	LCMGND	2	LCMVCC
3	VEE	4	SLIN-
5	INIT-	6	AFD-
7	PTD0	8	PTD1
9	PTD2	10	PTD3
11	PTD4	12	PTD5
13	PTD6	14	PTD7
15	+5V	16	LCD-

2.4.3 State LED Header (CN11)

Pin	Signal	Pin	Signal
1	SM_CLK	2	SM_DATA

2.4.4 20-pin Smart Fan (CN15)

Pin	Signal	Pin	Signal
1	+12V	2	N/A
3	+12V	4	GND
5	+12V	6	GND
7	FANCTL1	8	FANTAC1
9	FANCTL2	10	FANTAC2
11	FANCTL3	12	FANTAC3
13	FANCTL4	14	FANTAC4
15	FANCTL5	16	FANTAC5
17	GND	18	GND
19	GND	20	GND

2.4.5 State LED Header (CN25)

Pin	Signal	Pin	Signal
1	DOWN	2	UP
3	RIGHT	4	LEFT

2.4.6 Digital I/O (DIO1)

This connector offers 4-pair of digital I/O functions and address is 801H. The pin definitions are illustrated below:

Pin	Signal	Pin	Signal
1	Digital- IN/OUT(Port1 Bit 1)	2	Digital- IN/OUT (Port1 Bit 2)
3	Digital- IN/OUT (Port1 Bit 4)	4	Digital- IN/OUT (Port1 Bit 7)
5	Digital- IN/OUT (Port2 Bit 0)	6	Digital- IN/OUT (Port2 Bit 1)
7	Digital- IN/OUT (Port2 Bit 3)	8	Digital- IN/OUT (Port2 Bit 6)
9	+3.3V	10	GND

The pin definitions and registers mapping are illustrated below:

Address: 801H

4 in/ 4 out							
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
GPI 11	GPI 12	GPI 14	GPI 17	GPO 20	GPO 21	GPO 23	GPO 26

8 in							
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
GPI 11	GPI 12	GPI 14	GPI 17	GPO 20	GPO 21	GPO 23	GPO 26

8 out							
Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8
GPI 11	GPI 12	GPI 14	GPI 17	GPO 20	GPO 21	GPO 23	GPO 26

2.4.7 Front Panel Connector 1 (FP1)

Pin	Signal	Pin	Signal
1	Power On Button (+)	2	Reset Switch (+)
3	Power On Button (-)	4	Reset Switch (-)
5	HDD LED (+)	6	Power LED (+)
7	HDD LED (-)	8	Power LED (-)

2.4.8 Front Panel Connector 2 (FP2)

Pin	Signal	Pin	Signal
1	N/A	2	N/A
3	N/A	4	N/A
5	N/A	6	I2C Bus SMB Clock
7	N/A	8	I2C Bus SMB Data

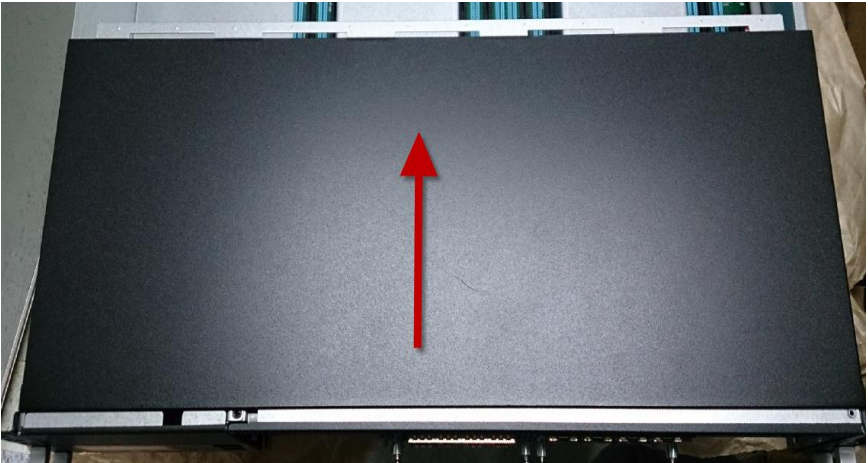
*Close Pin 5, 7 to enable internal buzzer

2.5 Installing 2.5" Hard Disk Drives (2 Pieces)

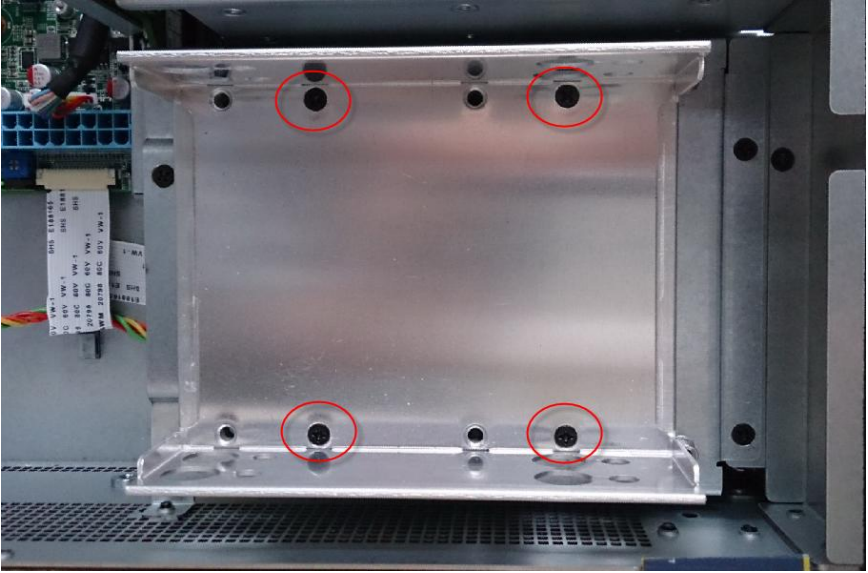
1. Remove the highlighted screws to remove the first lid



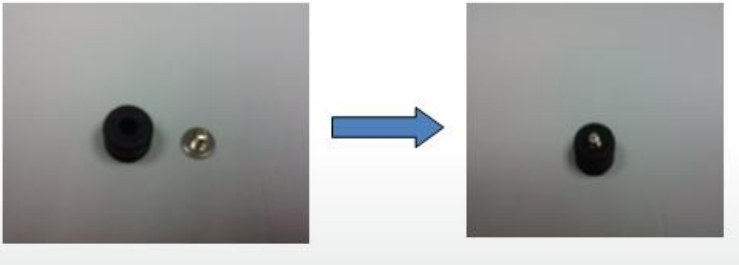
2. Remove the screws on the second lid, and, from the front of the system, slide it upwards to remove



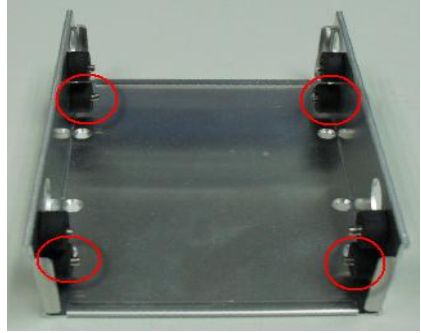
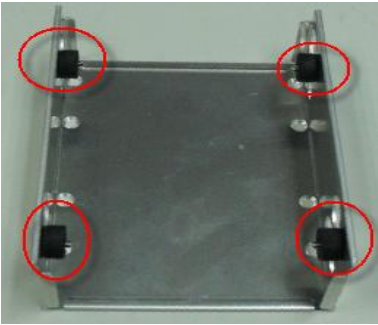
3. Remove the four highlighted screws to remove the HDD bracket



4. Put the provided screws (not the ones from step 3) into cushions



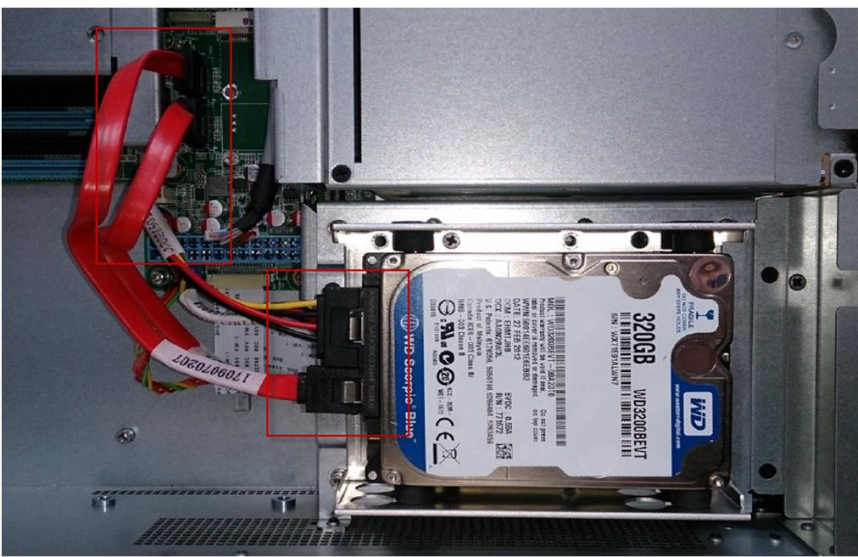
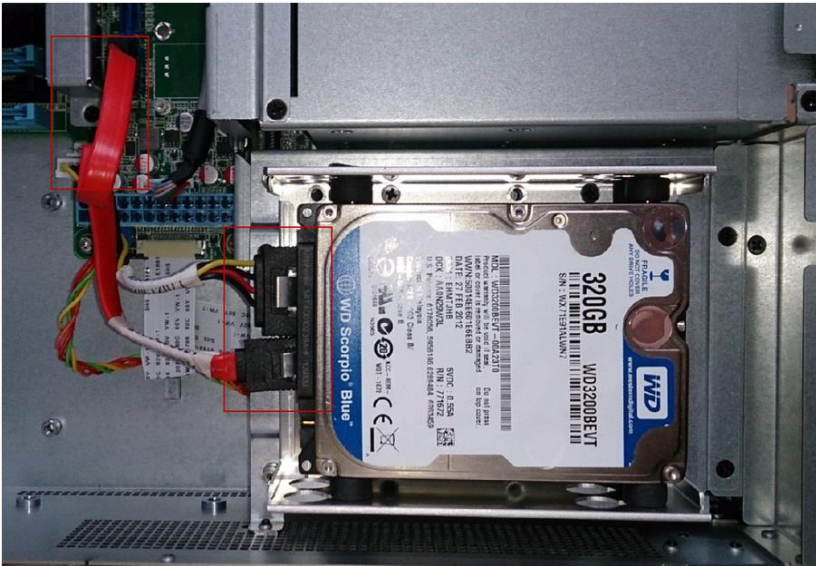
5. Attach the assembled screws to the top and bottom of the inside of the bracket



6. Place the HDDs into the bracket, tighten the screws to secure

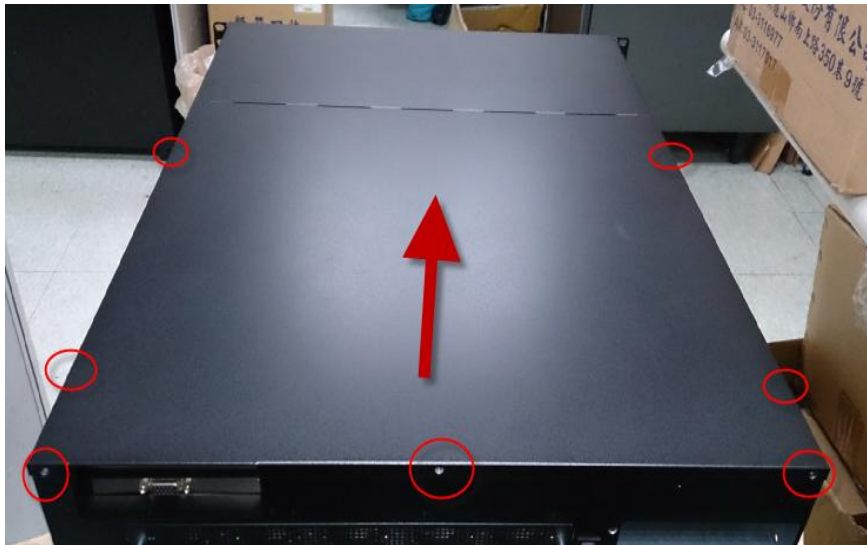


- 7. Place the assembled HDDs back into the system, secure with screws and reattach the SATA and power cables.

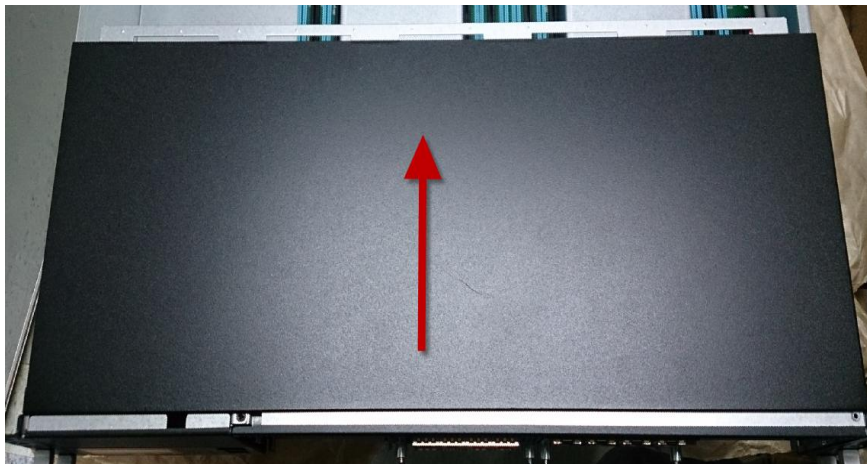


2.6 Installing 3.5" Hard Disk (1 Piece)

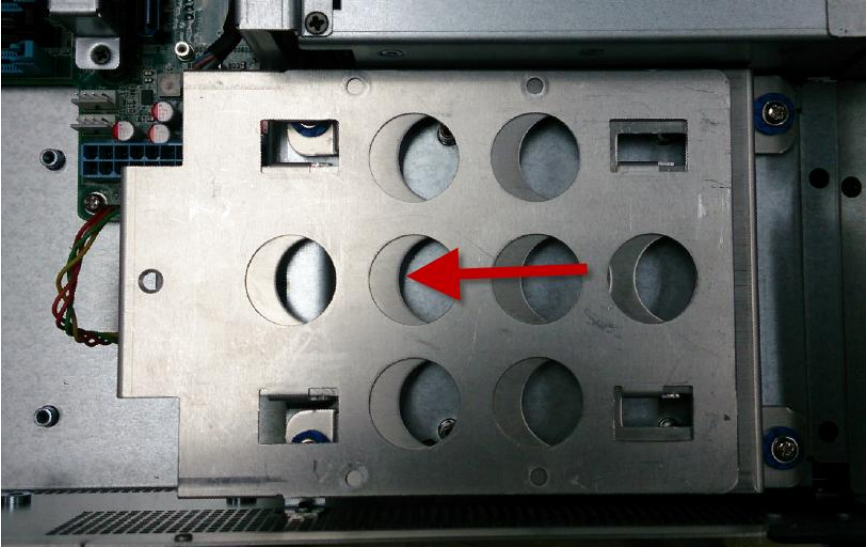
1. Remove the highlighted screws to remove the first lid



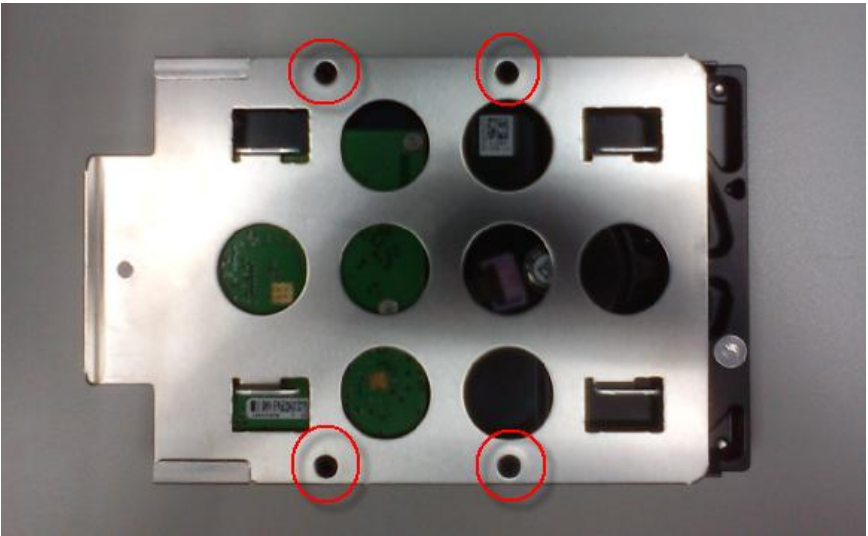
2. Remove the screws on the second lid, and, from the front of the system, slide it upwards to remove



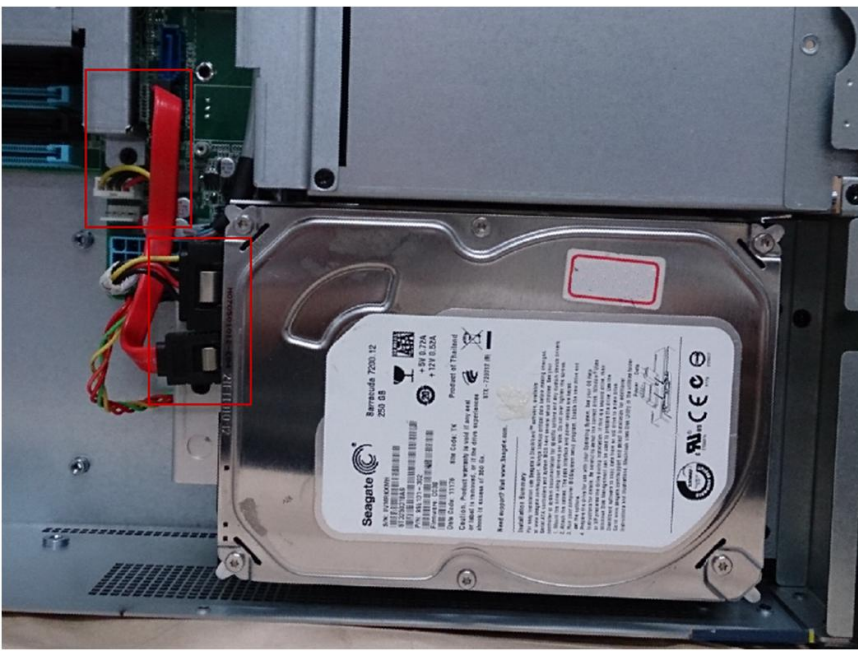
3. Remove the screw on the bracket and slide left to remove



4. Place the 3.5" HDD on the bracket, secure with screws on the underside

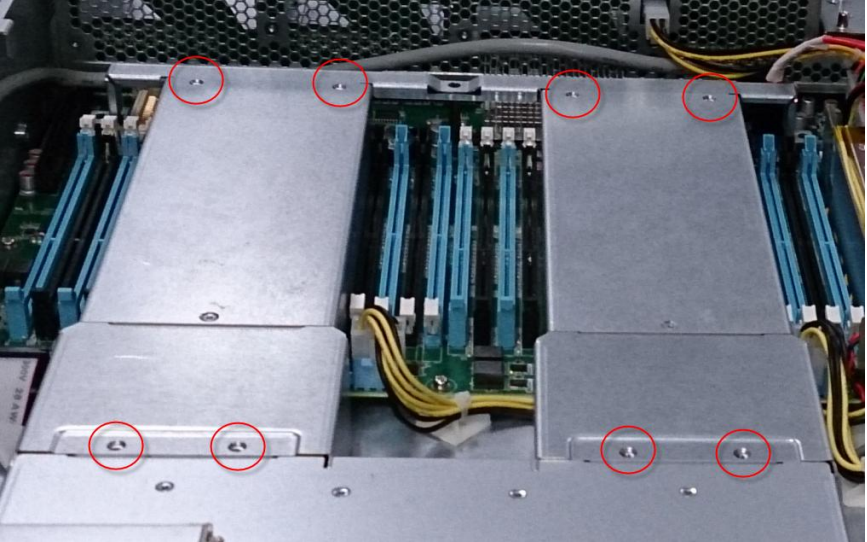


- 5. Slide the assembled HDD into the HDD bay, secure with screw and reattach the SATA and power cables

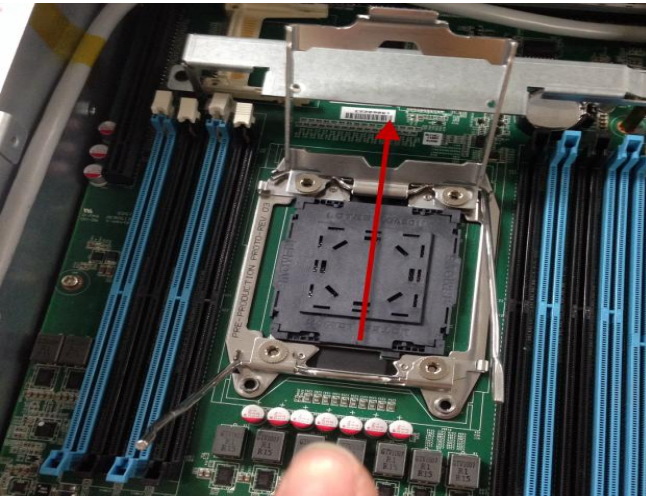


2.7 Installing CPU and Heat Sink

1. Remove the highlighted screws to remove the fan duct



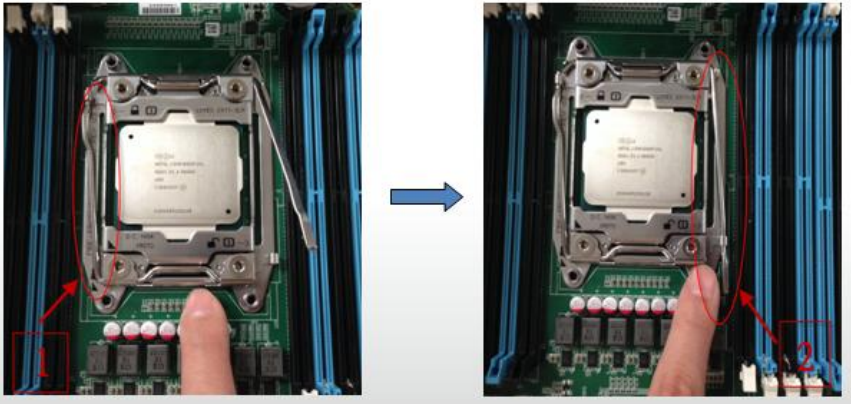
2. Lift the both the socket arms up to open the CPU socket



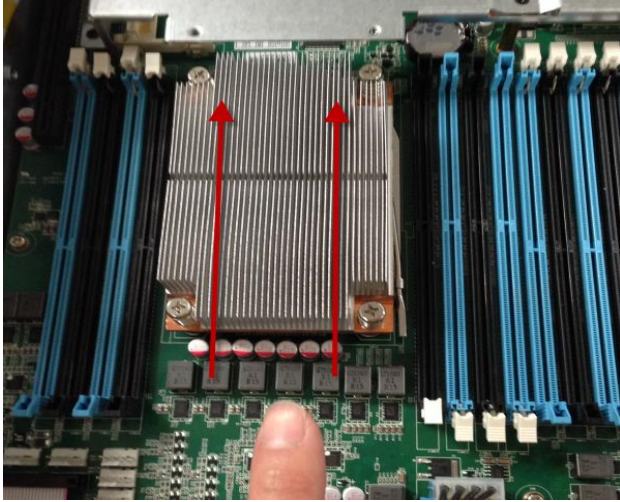
3. Remove the cover and place the CPU into the socket. Make sure the two fillisters are properly locked.



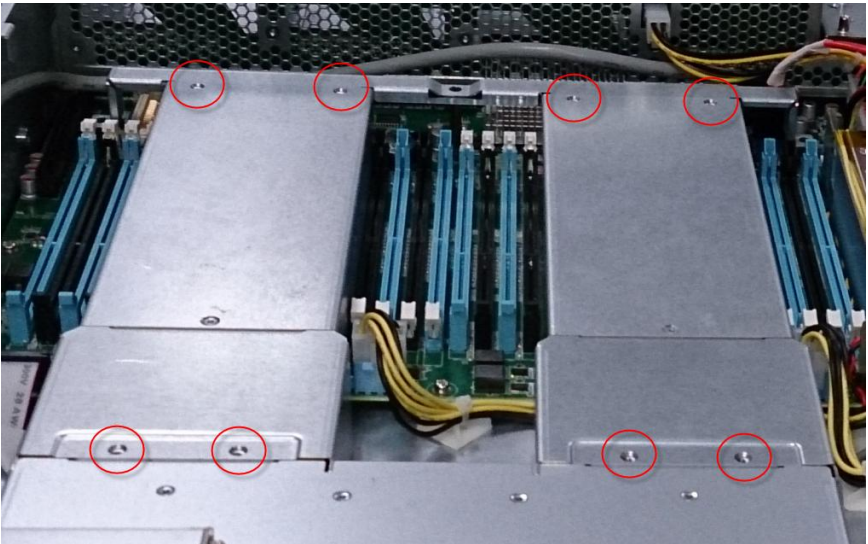
4. Push the arms down to lock the CPU into place



5. Place the heat sink onto the CPU. Make sure the direction of the heat sink is not against the airflow



6. Close the air duct and secure with screws



2.8 Installing Network Interface Module

1. Remove the highlighted screws to remove the NIM cover



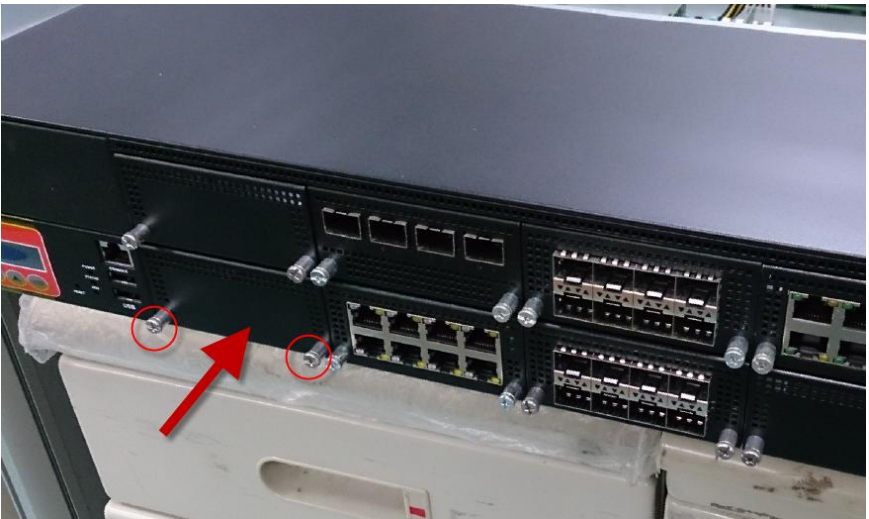
2. Remove the highlighted screws to remove the NIM



3. Insert the NIM and secure with screws



4. Close the NIM cover and secure with screws



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main

```
Aptio Setup Utility - Copyright (C) 2015 American Megatrends, Inc.
Main Advanced IntelRCSetup Security Boot Save & Exit

BIOS Information
FWS-8500 R1.4(K850AM14) (07/17/2015)

BIOS Vendor      American Megatrends
Core Version     5.010
Compliance      UEFI 2.4; PI 1.3
Project Version  0ACDR 1.2040807000 x64
Build Date and Time 07/17/2015 11:42:30

Memory Information
Total Memory     8192 MB

System Date      [Mon 10/19/2015]
System Time     [13:26:23]

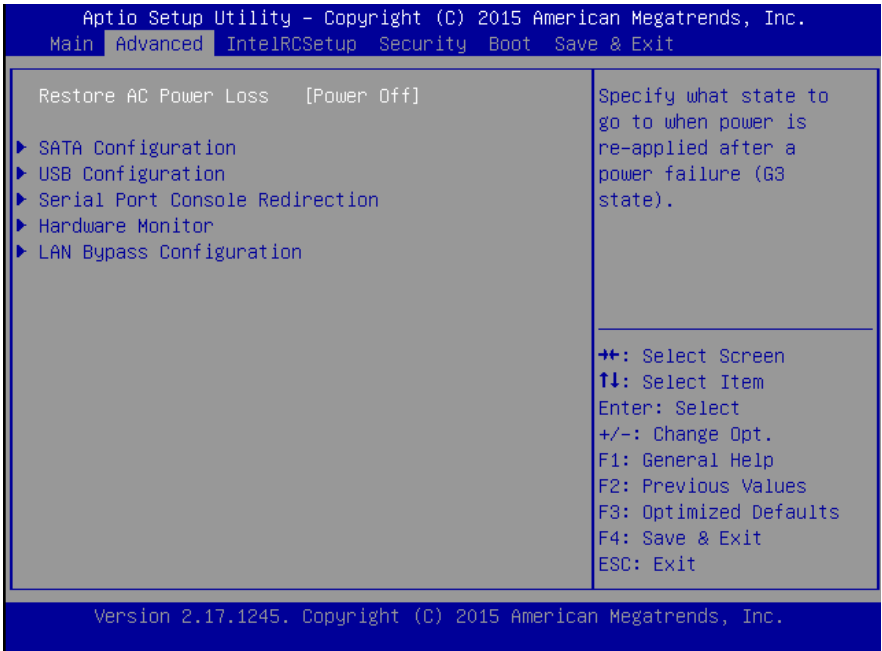
Access Level     Administrator

Set the Date. Use Tab to switch between Date elements.

+-: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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```

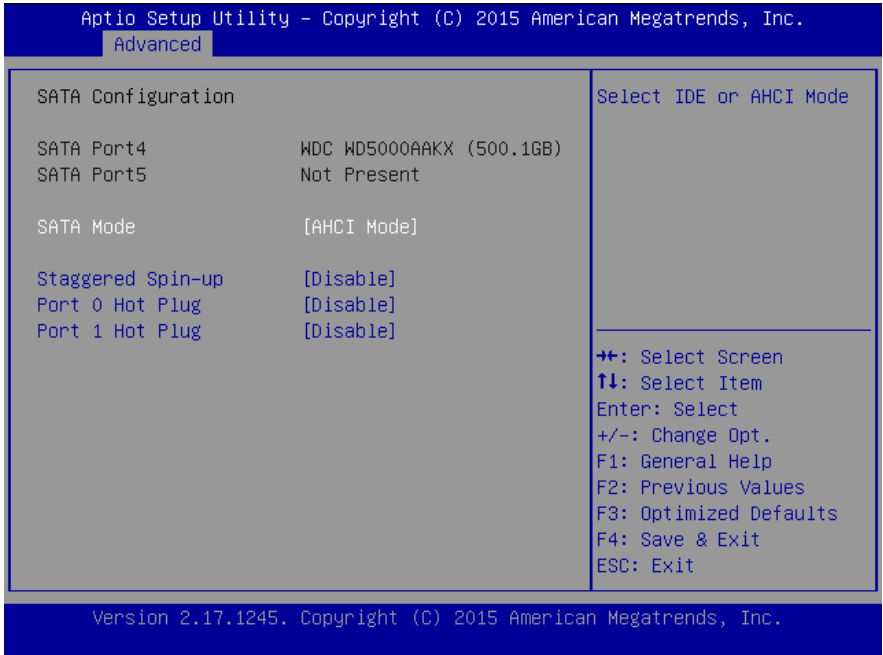
3.4 Setup Submenu: Advanced



Options summary:

Restore AC Power Loss	Power Off	Optimal Default, Failsafe Default
	Power On	
	Last State	
Specify what state to go to then power is re-applied after a power failure (G3 state).		

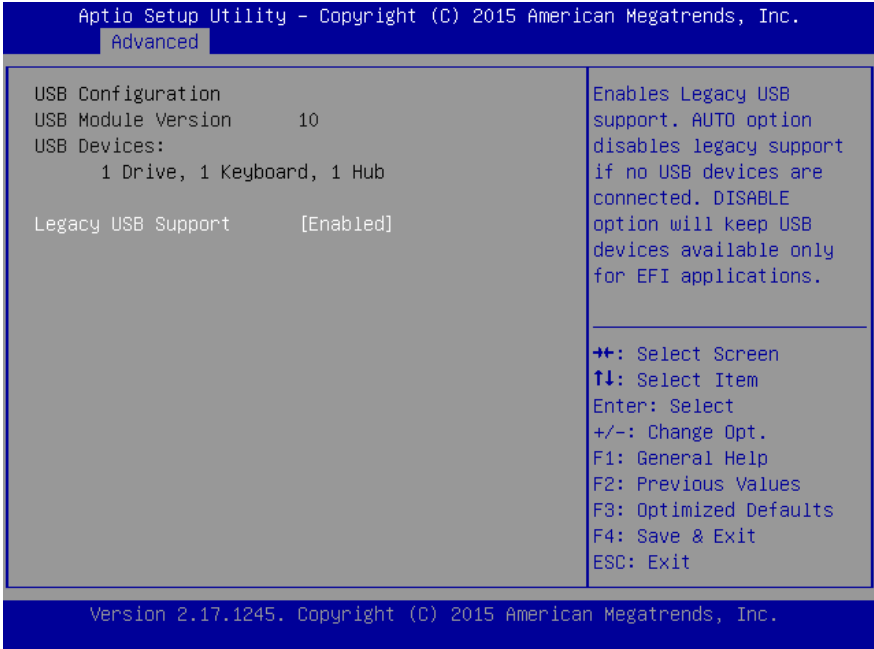
3.4.1 Advanced: SATA Configuration



Options summary:

SATA Mode	Disable	
	IDE	
	AHCI	Optimal Default, Failsafe Default
Select IDE or AHCI Mode		
Staggered Spin-up	Disable	Optimal Default, Failsafe Default
	Enable	
AHCI Supports Staggered Spin-up		
Port 0 Hot Plug	Disable	Optimal Default, Failsafe Default
	Enable	
SATA Ports Hot Plug Support		
Port 1 Hot Plug	Disable	Optimal Default, Failsafe Default
	Enable	
SATA Ports Hot Plug Support		

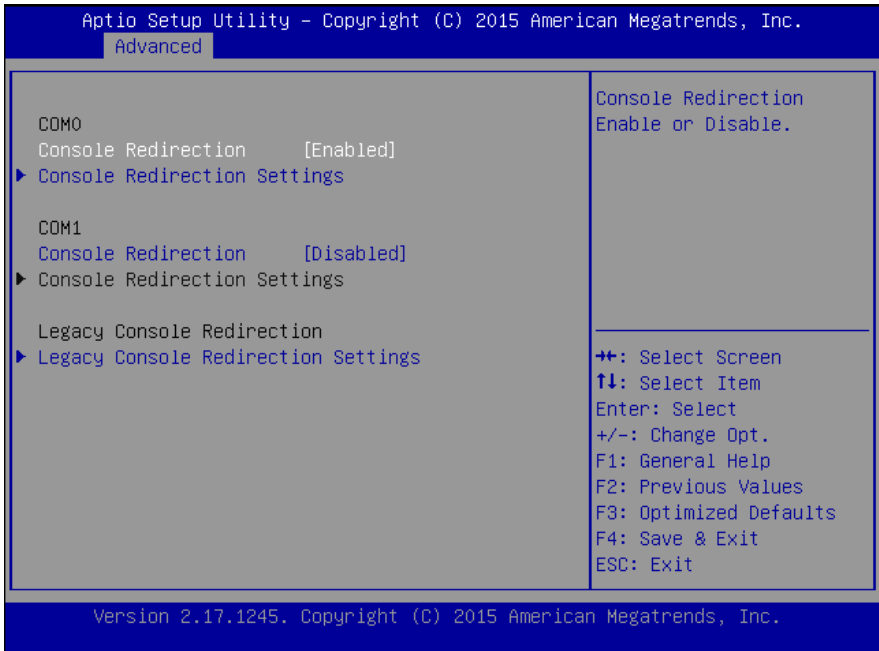
3.4.2 Advanced: USB Configuration



Options summary:

Legacy USB Support	Enable	Optimal Default, Failsafe Default
	Disable	
<p>Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.</p>		

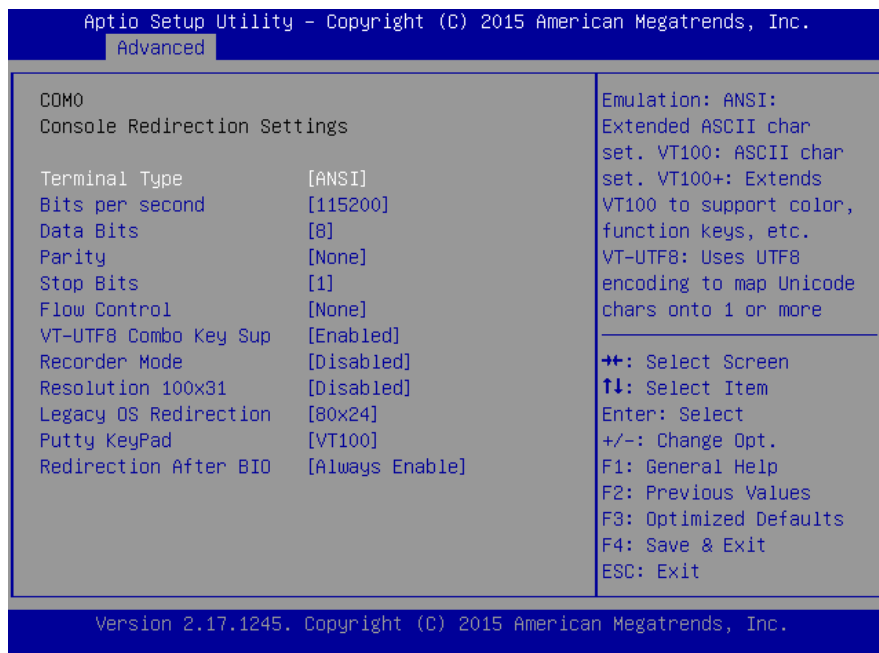
3.4.3 Advanced: Serial Port Console Redirection



Options summary:

COM0 Console Redirection	Enable	Optimal Default, Failsafe Default
	Disable	
Console Redirection Enable or Disable.		
COM1 Console Redirection	Enable	
	Disable	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		

3.4.3.1 Serial Port Console Redirection: COM0 Console Redirection Settings



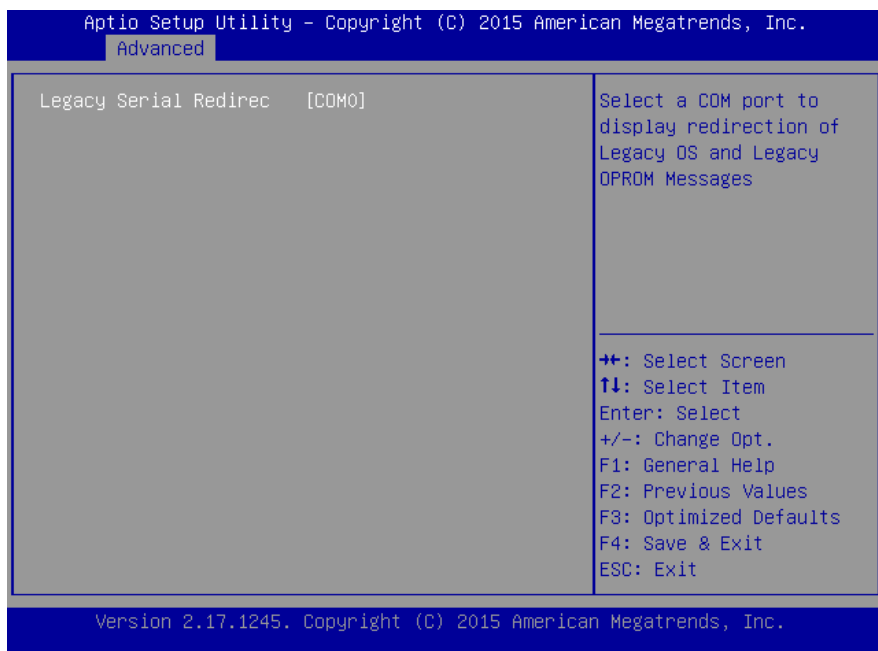
Options summary:

Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Data Bits	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Optimal Default, Failsafe Default
	Hardware RTC/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Sup	Enable	Optimal Default, Failsafe Default
	Disable	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Enable	
	Disable	Optimal Default, Failsafe Default
With this mode enabled only text will be send. This is to capture Terminal data.		
Resolution 100x31	Enable	
	Disable	Optimal Default, Failsafe Default
Enables or disables extended terminal resolution		
Legacy OS Redirection	80x24	Optimal Default, Failsafe Default
	80x24	
On Legacy OS, the Number of Rows and Columns supported redirection		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XRERM6	
	SCO	
	ESCN	

	VT400	
Select FunctionKey and KeyPad on Putty.		
Redirection After BIO	Always Enable	Optimal Default, Failsafe Default
	Boot Loader	
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.		

3.4.3.2 Serial Port Console Redirection: Legacy Console Redirection Settings



Options summary:

Legacy Serial Redirec	COM0	Optimal Default, Failsafe Default
	COM1	
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages		

3.4.4 Advanced: Hardware Monitor

```
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  Advanced

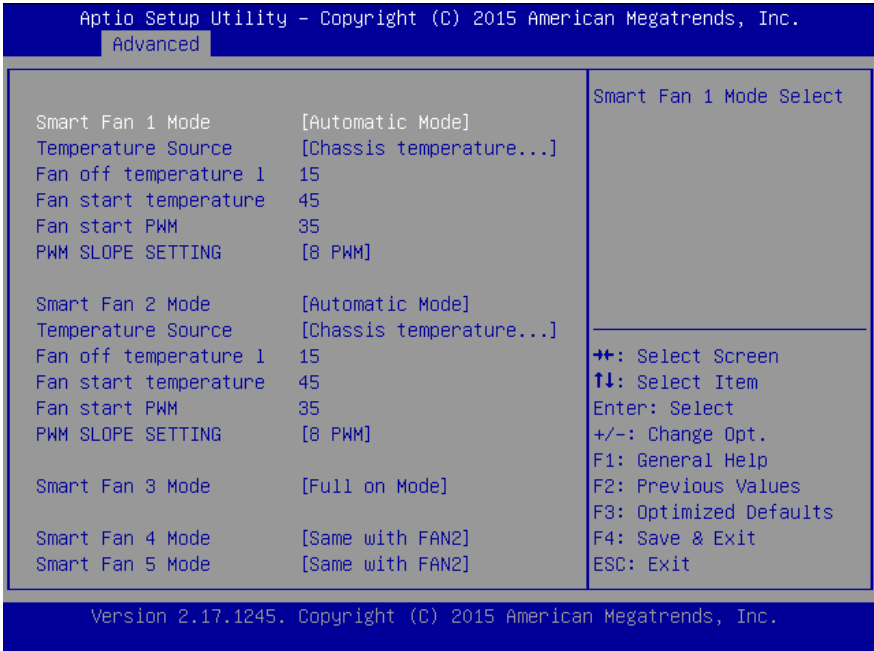
  Pc Health Status
  ▶ Smart Fan Function
    System temperature1      : +49 °C
    System temperature2     : +47 °C
    Fan1 Speed               : 6750 RPM
    Fan2 Speed               : 6818 RPM
    Fan3 Speed               : 15340 RPM
    Fan4 Speed               : 6617 RPM
    Fan5 Speed               : 6490 RPM
    CoreIn                   : +1.788 V
    VDDQ_AB                  : +1.200 V
    +12V                      : +12.048 V
    +5V                       : +5.019 V
    VIN5                      : +5.040 V
    VBAT                      : +2.976 V

    Smart Fan function
    setting

    ++: Select Screen
    ↑↓: Select Item
    Enter: Select
    +/-: Change Opt.
    F1: General Help
    F2: Previous Values
    F3: Optimized Defaults
    F4: Save & Exit
    ESC: Exit

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```

3.4.5 Advanced: Smart Fan



Options summary:

Smart Fan 1 Mode	Full on Mode	
	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Smart Fan 1 Mode Select		
Temperature Source	Chassis temperature(CPU)	Optimal Default, Failsafe Default
	Chassis temperature(SYS1)	
SMART Fan reference temperature source		
PWM SLOPE SETTING	0.125 PWM	
	0.25 PWM	
	0.5 PWM	
	1 PWM	
	2 PWM	
	4 PWM	
	8 PWM	Optimal Default, Failsafe Default

	15.875 PWM	
PWM SLOPE Selection		
Smart Fan 2 Mode	Full on Mode	
	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Smart Fan 2 Mode Select		
Temperature Source	Chassis temperature(CPU)	Optimal Default, Failsafe Default
	Chassis temperature(SYS1)	
SMART Fan reference temperature source		
PWM SLOPE SETTING	0.125 PWM	
	0.25 PWM	
	0.5 PWM	
	1 PWM	
	2 PWM	
	4 PWM	
	8 PWM	Optimal Default, Failsafe Default
	15.875 PWM	
PWM SLOPE Selection		
Smart Fan 3 Mode	Full on Mode	Optimal Default, Failsafe Default
	Automatic Mode	
	Manual Mode	
Smart Fan 3 Mode Select		
Smart Fan 4 Mode	Same with FAN1	
	Same with FAN2	Optimal Default, Failsafe Default
	Same with FAN3	
Smart Fan 4 Mode Select		
Smart Fan 5 Mode	Same with FAN1	
	Same with FAN2	Optimal Default, Failsafe Default
	Same with FAN3	
Smart Fan 5 Mode Select		

3.4.6 Advanced: LAN Bypass Configuration

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Advanced

Bypass function LAN KITS Setting ▲	
LAN BYPASS by BIOS	[Enabled]
MDT Mode Setting.	[Bypass Mode]
LAN Bypass LED Config	[LED OFF]
KIT00 Power On SETTIN [Bypass Through]	
KIT00 Power Off SETTI [Bypass]	
KIT01 Power On SETTIN [Bypass Through]	
KIT01 Power Off SETTI [Bypass]	
KIT02 Power On SETTIN [Bypass Through]	
KIT02 Power Off SETTI [Bypass]	
KIT03 Power On SETTIN [Bypass Through]	
KIT03 Power Off SETTI [Bypass]	
KIT04 Power On SETTIN [Bypass Through] ▼	

Main switch to enable whether config LAN BYPASS function by BIOS.

▲: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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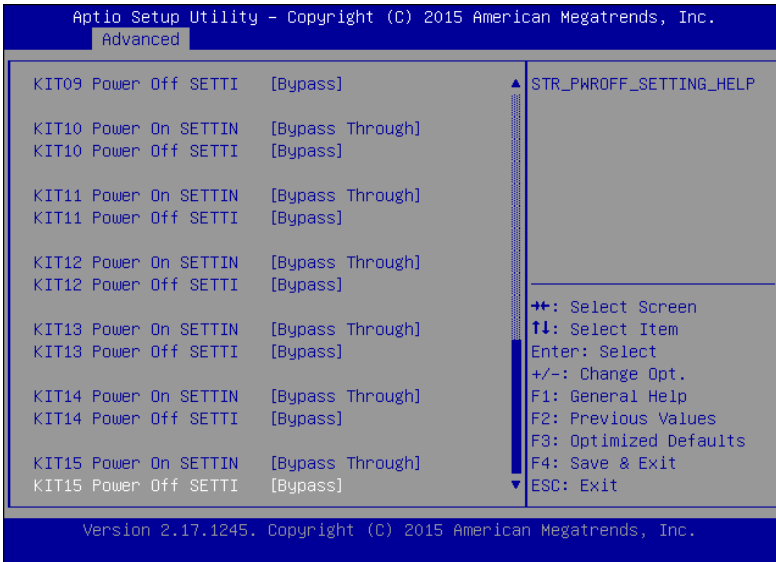
Aprio Setup Utility - Copyright (C) 2015 American Megatrends, Inc.
Advanced

KIT04 Power On SETTIN [Bypass Through] ▲	
KIT04 Power Off SETTI [Bypass]	
KIT05 Power On SETTIN [Bypass Through]	
KIT05 Power Off SETTI [Bypass]	
KIT06 Power On SETTIN [Bypass Through]	
KIT06 Power Off SETTI [Bypass]	
KIT07 Power On SETTIN [Bypass Through]	
KIT07 Power Off SETTI [Bypass]	
KIT08 Power On SETTIN [Bypass Through]	
KIT08 Power Off SETTI [Bypass]	
KIT09 Power On SETTIN [Bypass Through]	
KIT09 Power Off SETTI [Bypass]	
KIT10 Power On SETTIN [Bypass Through] ▼	

STR_PWRON_SETTING_HELP

▲: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

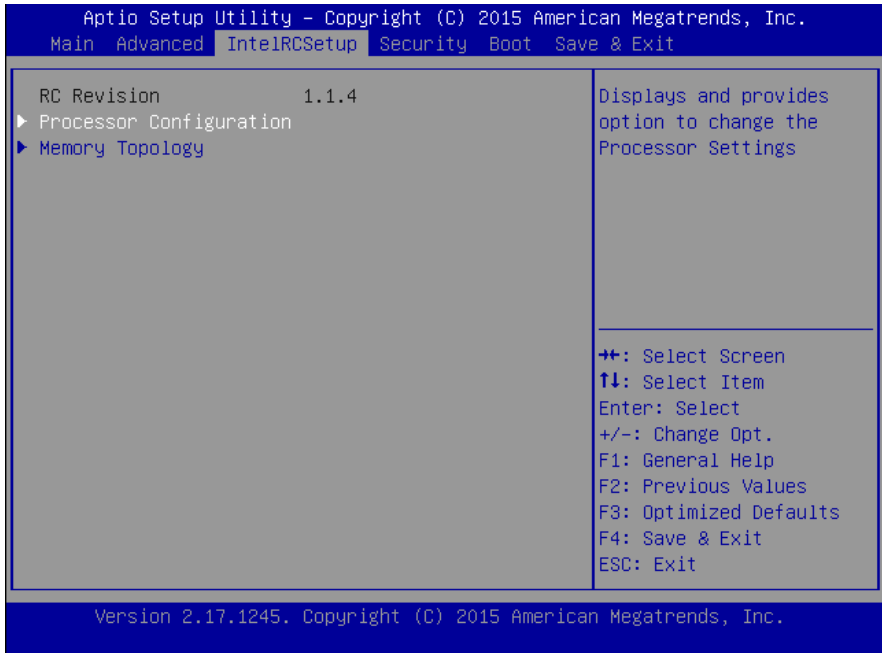
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Options summary :

LAN BYPASS by BIOS	Disable	
	Enable	Optimal Default, Failsafe Default
Main switch to enable whether config LAN BYPASS function by BIOS		
WDT Mode Setting	Reset Mode	
	Bypass Mode	Optimal Default, Failsafe Default
Setting mode with Reset or Bypass when WDT assert		
LAN Bypass LED Config	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED FAST BLINK	
Select LAN Bypass LED Indicator working mode		
KIT[0:15] Power On Setting	Bypass Through	Optimal Default, Failsafe Default
	Bypass	
STR_PWRON_SETTING_HELP		
KIT[0:15] Power Off Settings	Bypass Through	
	Bypass	Optimal Default, Failsafe Default
STR_PWROFF_SETTING_HELP		

3.5 Setup submenu: IntelRCSetup



3.5.1 IntelRCSetup: Processor Configuration

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IntelRCSetup

Processor Configuration			Enables Hyper Threading (Software Method to Enable/Disable Logical Processor threads.

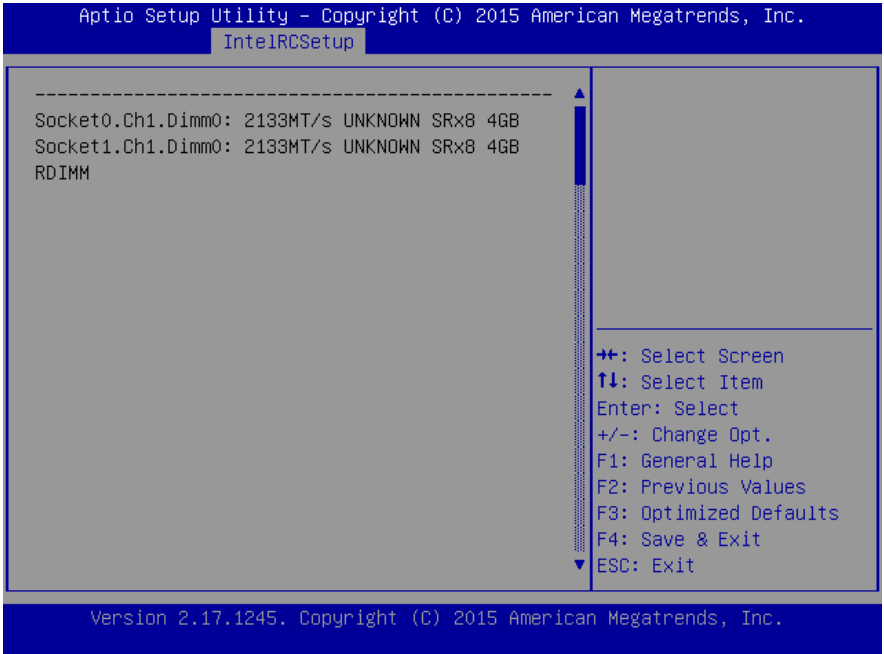
Processor Socket	Socket 0	Socket 1	++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Processor ID	000306F1*	000306F1	
Processor Frequency	2.200GHz	2.200GHz	
Processor Max Ratio	16H	16H	
Processor Min Ratio	0CH	0CH	
Microcode Revision	00000014	00000014	
L1 Cache RAM	768KB	768KB	
L2 Cache RAM	3072KB	3072KB	
L3 Cache RAM	30720KB	30720KB	
Processor 0 Version	Genuine Intel(R) CPU @ 2.20GHz		
Processor 1 Version	Genuine Intel(R) CPU @ 2.20GHz		
Hyper-Threading [ALL]	[Enable]		
Enable Intel TXT Supp	[Disable]		

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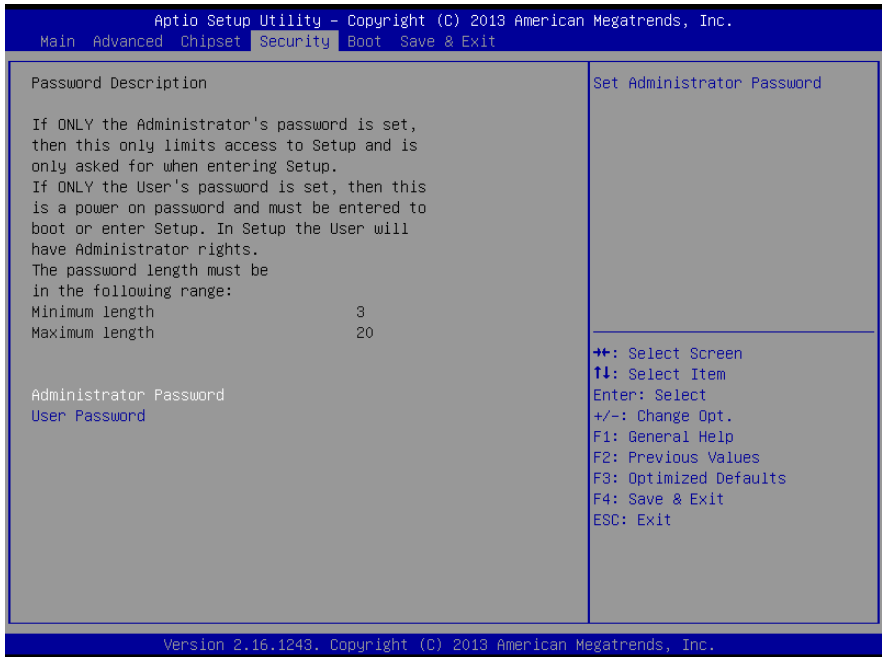
Options summary :

Hyper-threading[All]	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled Hyper-Threading (Software Method to Enable/Disable Logical Processor threads.)		
Enable Intel TXT Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables Intel Trusted Execution Technology Configuration. Please disable "EV DFX Features" when TXT is enabled.		

3.5.2 IntelRCSetup: Memory Configuration



3.6 Setup submenu: Security



Change User/Administrator Password

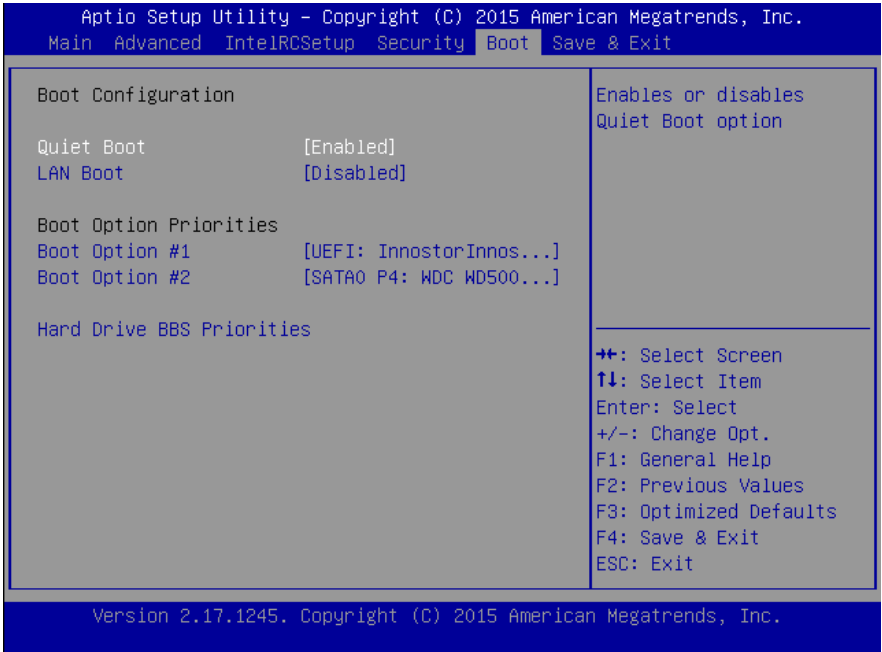
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

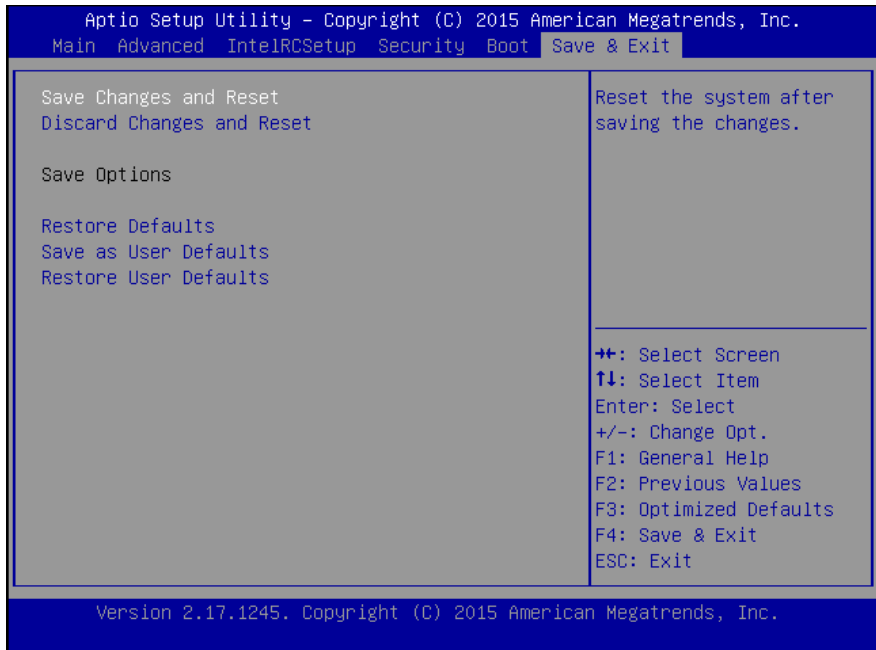
3.7 Setup submenu: Boot



Options summary :

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables Quiet Boot option.		
LAN Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Launch LAN PXE oprom		

3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Drivers Installation

The drivers can be found in the product page for FWS-8500 at aaeon.com. Please follow the sequence below to install the drivers.

Step 1 – Install LAN Drivers (Linux only)

1. Download the drivers for your version of Linux
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	4(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex //This parameter is represented from Note1
#define byte   SIOData //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN //This parameter is represented from Note3
#define byte   TimerReg //This parameter is represented from Note4
#define byte   TimerVal // This parameter is represented from Note24
#define byte   UnitLDN //This parameter is represented from Note5
#define byte   UnitReg //This parameter is represented from Note6
#define byte   UnitBit //This parameter is represented from Note7
#define byte   UnitVal //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
*****
```

```
*****
VOID  Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```
*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****
```



```
*****
VOID  SIOEnterMBPnPMode(){
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****
```

```
*****
```

```
VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){  
    Byte TmpValue;  
  
    SIOEnterMBPnPMode();  
    SIOSelectLDN(byte LDN);  
    IOWriteByte(SIOIndex, Register);  
    TmpValue = IOReadByte(SIOData);  
    TmpValue &= ~(1 << BitNum);  
    TmpValue |= (Value << BitNum);  
    IOWriteByte(SIOData, TmpValue);  
    SIOExitMBPnPMode();  
}
```

```
VOID SIOByteSet(byte LDN, byte Register, byte Value){  
    SIOEnterMBPnPMode();  
    SIOSelectLDN(LDN);  
    IOWriteByte(SIOIndex, Register);  
    IOWriteByte(SIOData, Value);  
    SIOExitMBPnPMode();  
}
```

```
*****
```