FWS-7830

Network Appliance

User's Manual 1st Ed

Last Updated: January 25, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7830	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O
外壳	O	O	O	O	O	O
中央处理器与内存	O	O	O	O	O	O
硬盘	O	O	O	O	O	O
电源	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	O	O	O	O	O	O
Hard Disk	O	O	O	O	O	O
PSU	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

Platform	
Form Factor	1U Rackmount Network Platform
Processor	Intel® 8th Generation Core™/ Xeon® Processors
Chipset	Intel® C246
System Memory	DDR4 2133/2400/2666 UDIMM Up to 64GB 288-pin DIMM x 4
Network	
Ethernet	Intel® I350 AM2 Gigabit Ethernet x 2
Bypass	Depend on NIM module
NIM Slot	NIM Slot x3
Display	
Graphic Controller	Intel® Integrated
Connector	VGA cable (Optional)
Storage	
HDDs	Internal 2.5" SATA HDD x 2 or 3.5" SATA HDD x 1 (Optional)
CF/CFast/mSATA	Default mSATA Slot (Optional CFast™ Socket)

Expansion / Internal Interface	
PCIe slot	NIM x 3 PCIe [x8] X1 slot by riser card Mini PCIe Slot x 1 or mSATA x 1
Mini-PCIe slot	Mini Card x 1
Keyboard and Mouse	Pin-header
Universal Serial Bus	USB 3.0 x 2, Box Header (2.0mm)

Miscellaneous	
RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable, 1 sec per step
Software Button	GPIO Programmable push button x 1
TPM	Optional TPM v2.0
GPIO	8bits, BIOS default 4 bits input, 4bits output.
FAN	2
MTBF (Hours)	TBD
Color	Black

Environmental Parameters and Dimension	
Power Requirement	220W ATX PSU
Operation Temp.	32°F ~ 104°F (0°C ~ 40°C)
Storage Temp.	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10% ~ 80%
Storage Humidity	10% ~ 80% @ 40°C, non-condensing

Vibration	0.5 Grms/ 5 ~ 500Hz/ operation (3.5" H.D.D) 1.5 Grms/ 5 ~ 500Hz/ no operation
Shock	10G peak acceleration (11 m sec. duration), operation 20G peak acceleration (11 m sec. duration), non-operation
Chassis Dimension (W x D x H)	16.93" x 18.7" x1.73"(430mm x 475mm x 44mm)

I/O Interface

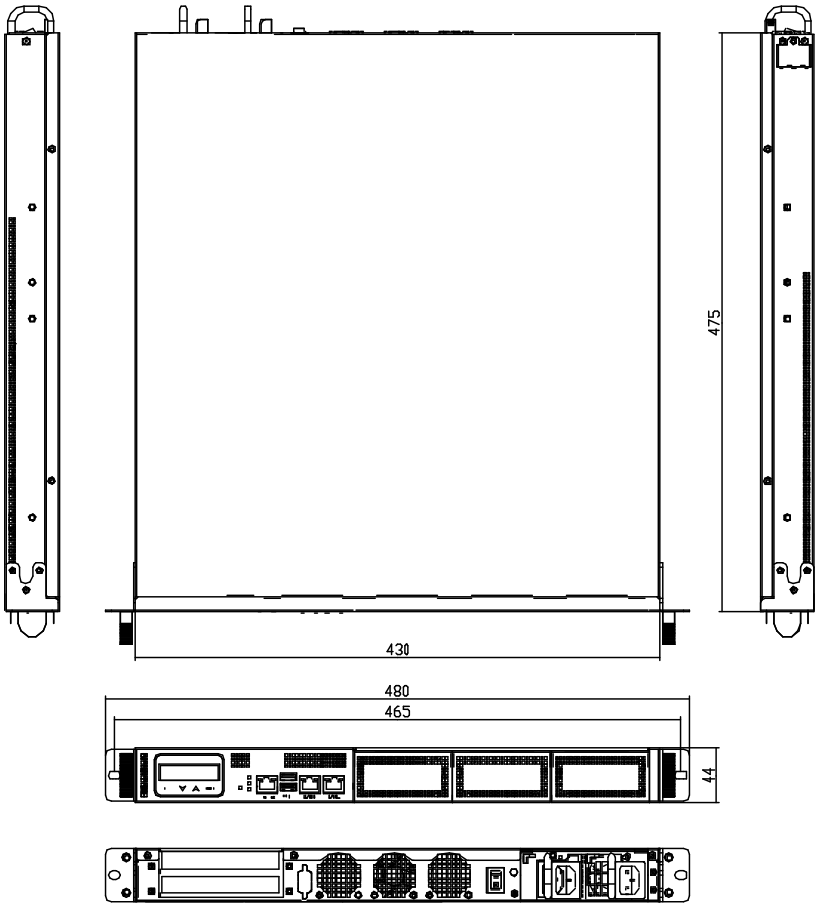
Front Panel	Power LED x 1 Status LED x 1 HDD Active LED x 1 USB 3.0 Ports x 2 RJ-45 Console x 1 Parallel LCM display and 4 keypad x 1 Software Programmable Switch x 1
Rear Panel	AC Power Input x 1 Power Switch x 1 VGA port (Optional) Rear Expansion Slot X 1

Chapter 2

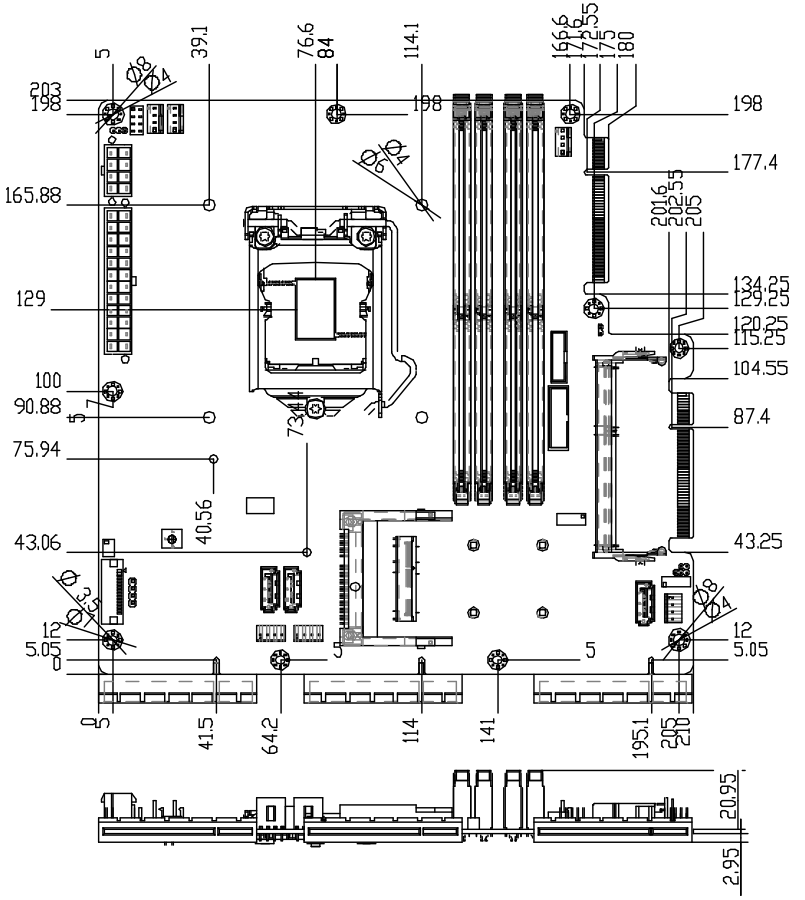
Hardware Information

2.1 Dimensions

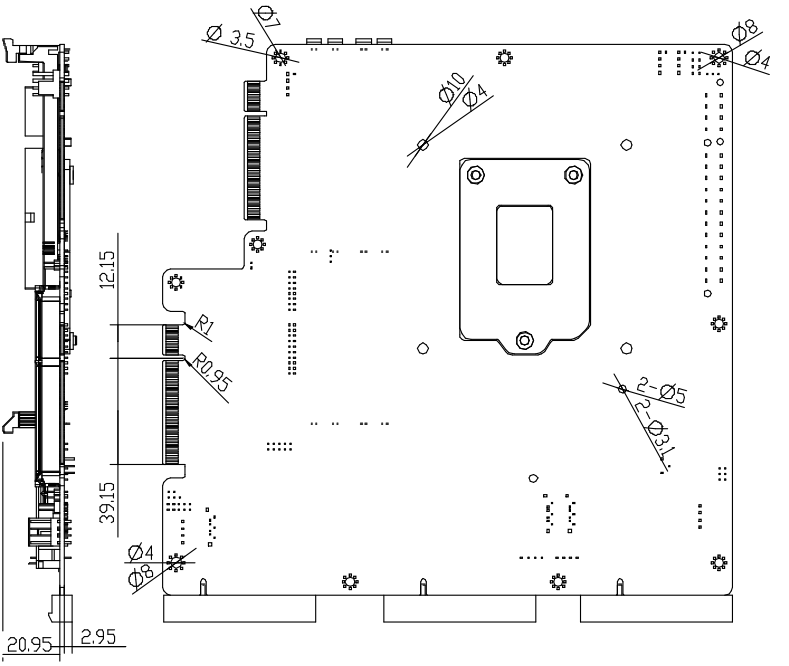
System



Component Side



Solder Side



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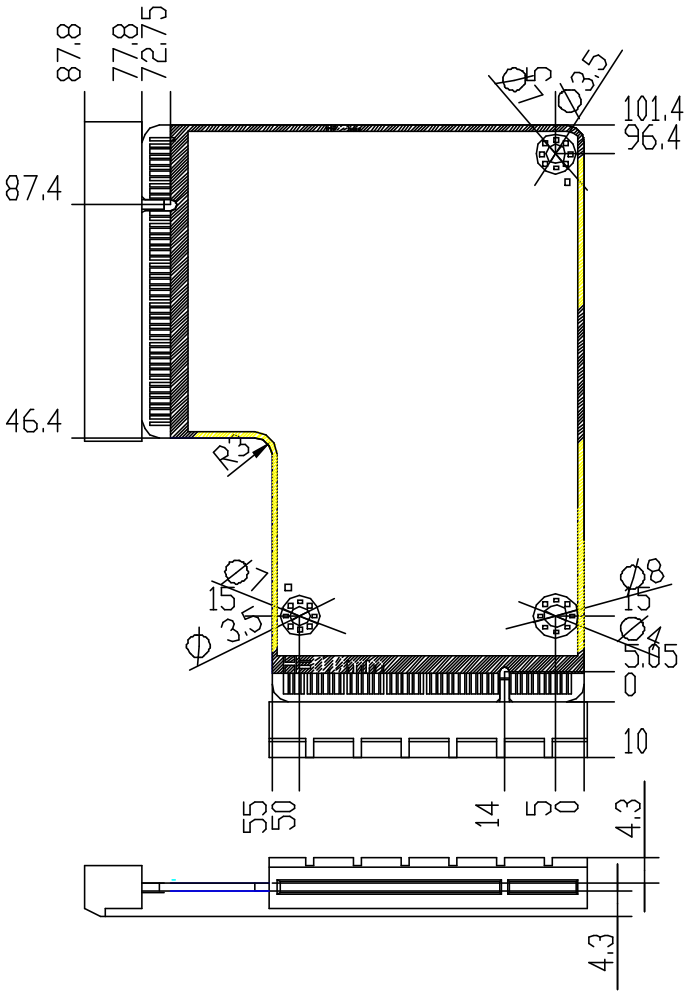
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87.4
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Ø5
Ø3.5
101.4
96.4
Ø7
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Ø8
15
Ø4
5.05
0
10
55
50
14
5
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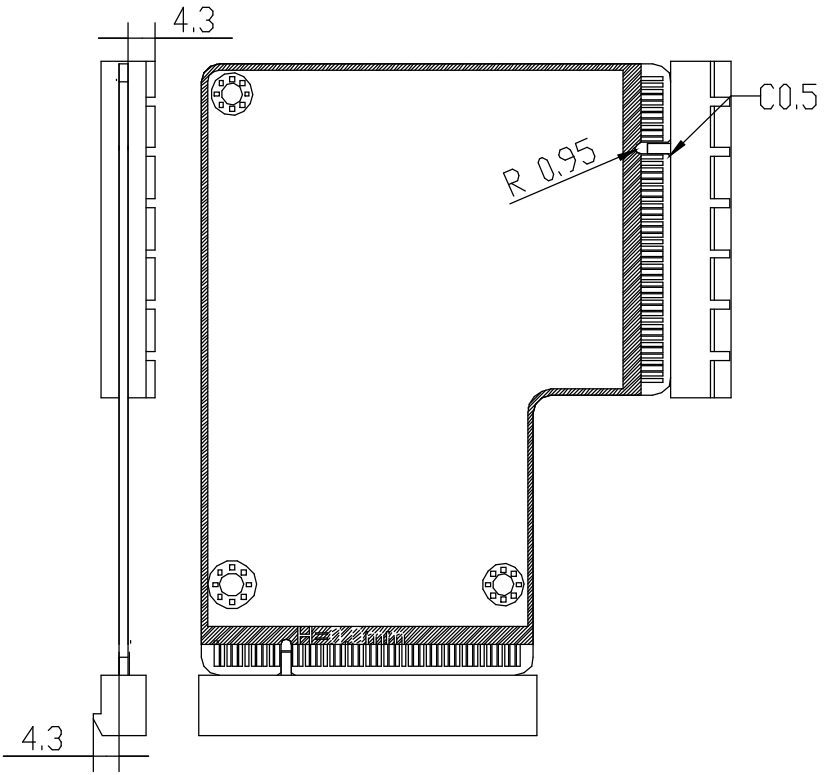
4.3
4.3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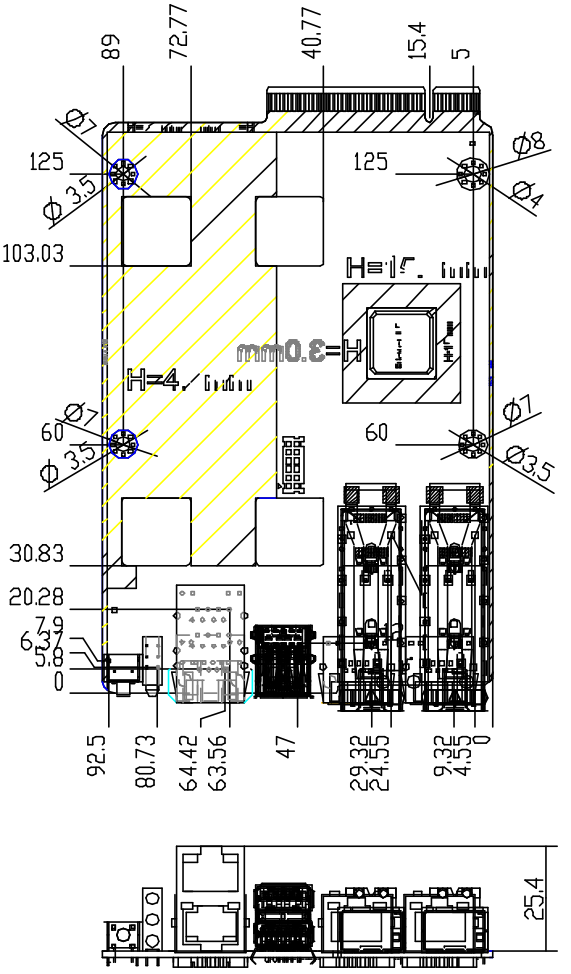
C0.5
R 0.95
4.3

PER-T507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125
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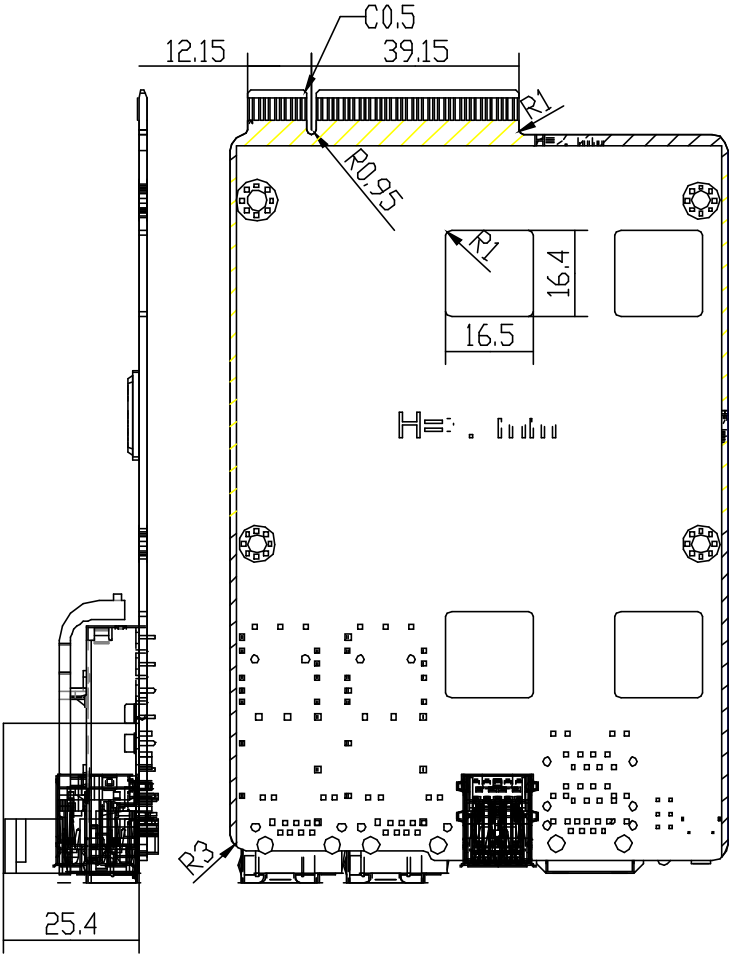
24.55
9.32
4.55
0
25.4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R1
R0.95
R1
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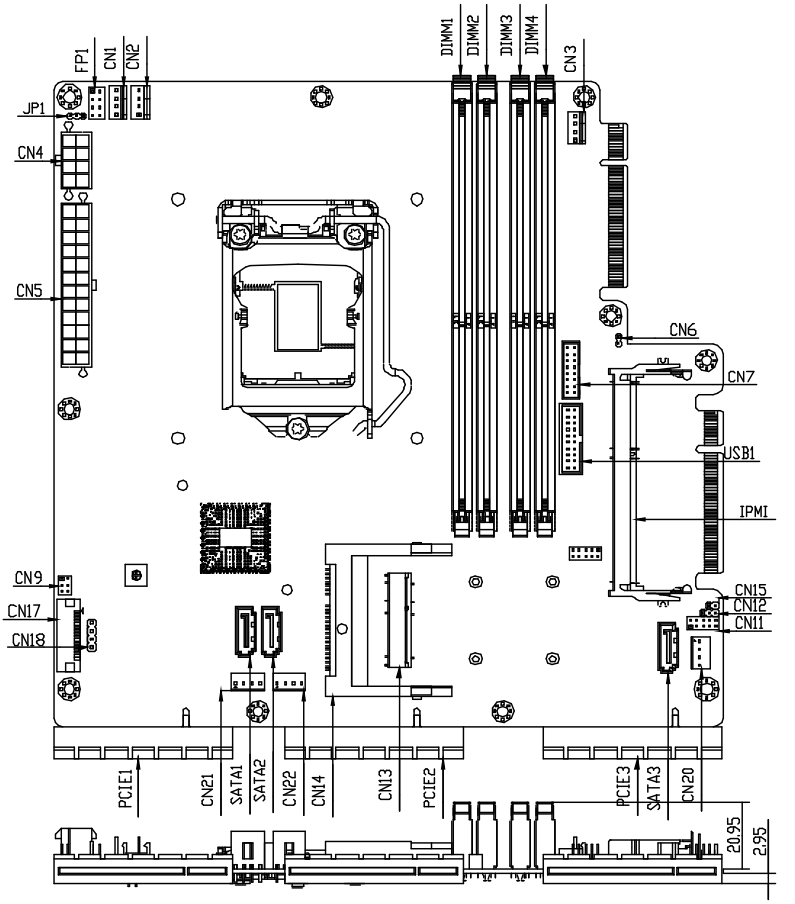
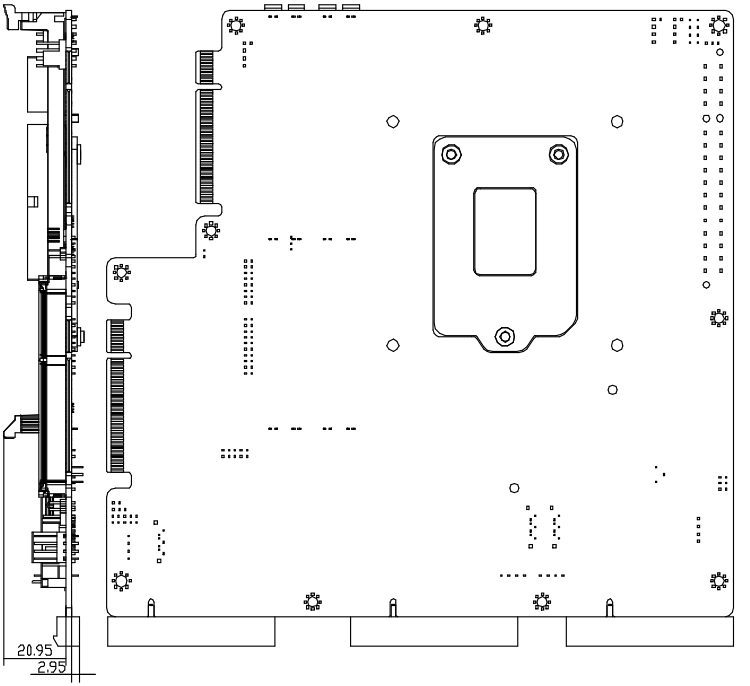
16.5
R3
25.4

2.2 Jumpers and Connectors

Component Side



Solder Side



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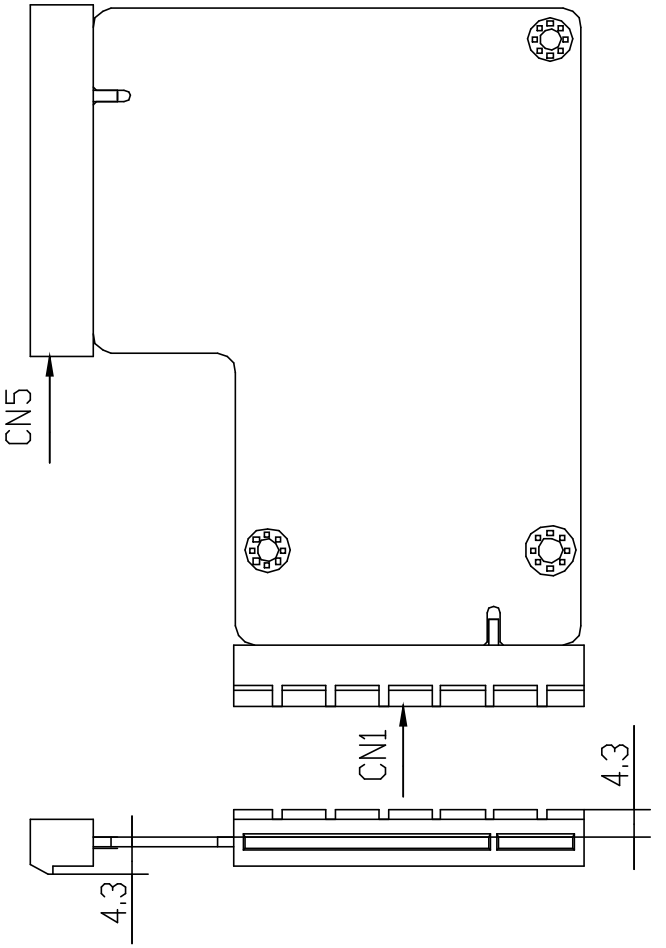

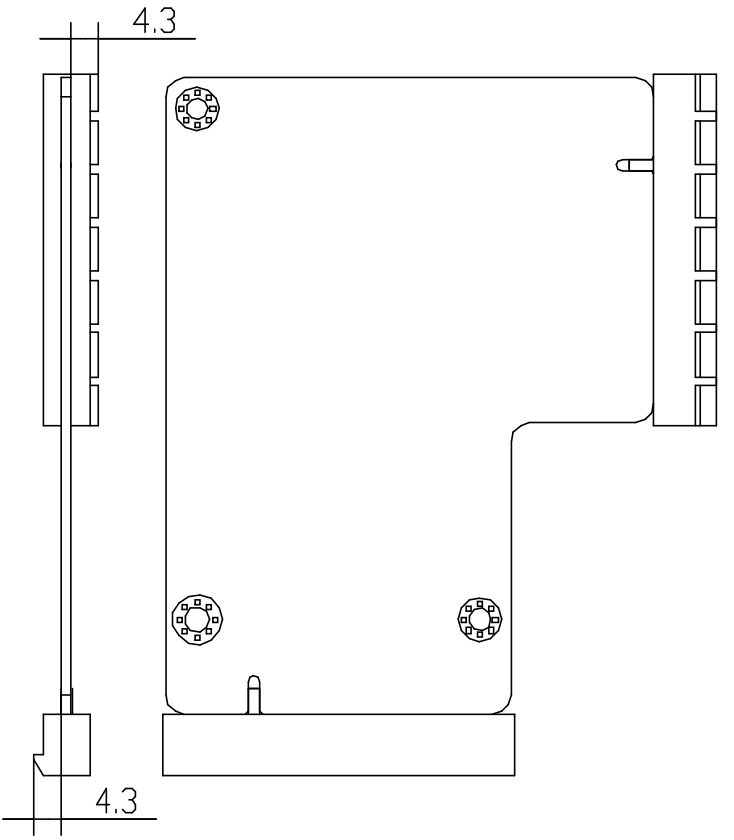
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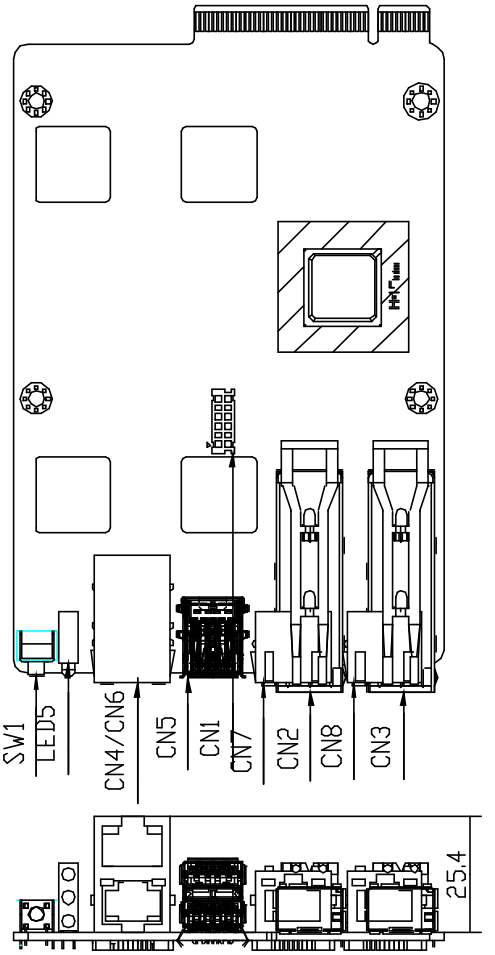
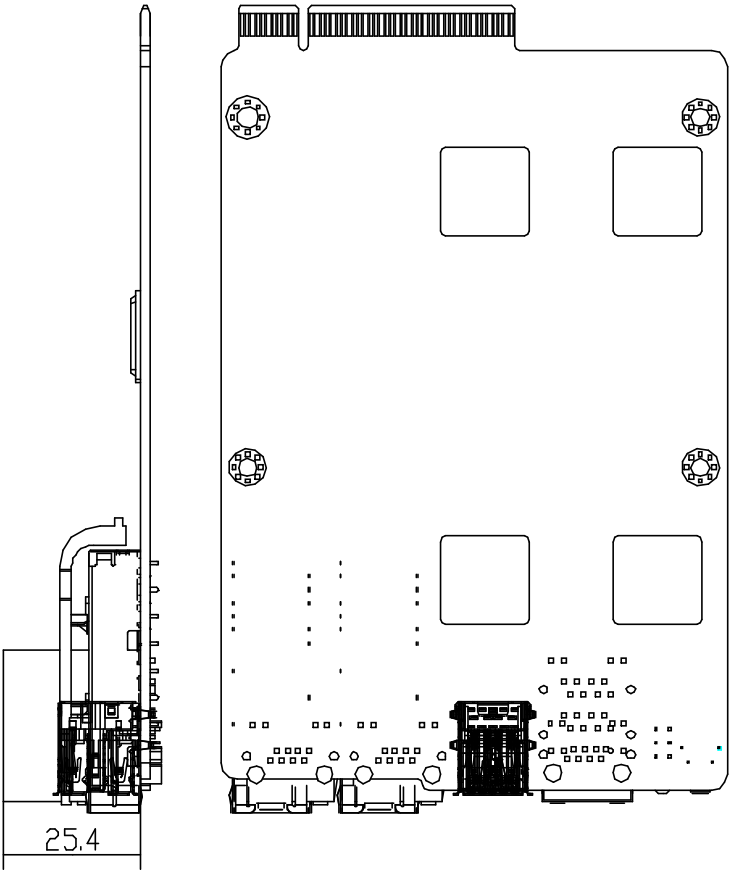



25.4

2.3 List of Jumpers

Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP1	Auto PWR Button
CN9	Clear CMOS
CN11	IPMI Button
JP2	SATA/PCIE selection For mSTAT1
CN12	CF voltage selection

2.3.1 Auto Power Button (JP1)

Normal	1-2
Auto power on	2-3

2.3.2 Clear CMOS (CN9)

Normal	1-3, 2-4
Clear CMOS	3-5, 4-6

2.3.3 CF Power SELECT (CN12)

3.3V	2-3
5V	1-2

2.3.4 SATA/PCIE selection For mSTAT1(JP2)

SATA	1-2
PCIE	2-3

2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
FP1	front panel
CN1, 2, 3	CPU FAN/SYS FAN1.2
DIMM1, 2, 3, 4	DDR4 UDIMM
CN7	VGA CON
USB1	USB3.0 EXT CON
CN4	ATX 8PIN CON
CN5	ATX 24PIN CON
CN16	HDMI CON
CN18	KAYPAD Header
CN20, 21, 22	SATA 4P POWER
CN17	LCM CON
SATA1, 2, 3	SATA CON
CN13	CFAST
CN14	CF
Msata1	MSATA CON / miniPCIe
COM1	UART2
CN15	DIO CON
CN24	BIOS Brunin
PCIE1	PER-T507
PCIE2,3	NIM Card
GF1	PER-R30X
GF2	PER-R51X

2.4.1 Front Panel (FP1)

Pin	Signal	Pin	Signal
1	PWR_SW#	2	GND
3	RESET	4	GND
5	PWR LED+	6	PWR LED-
7	HDD LED+	8	HDD LED-

2.4.2 RS232 (COM1)

Pin	Signal	Pin	Signal
1	DCD2	2	RXD2
3	TXD2	4	DTR2
5	GND2	6	DSR2
7	RTS2	8	CTS2
9	RI2		

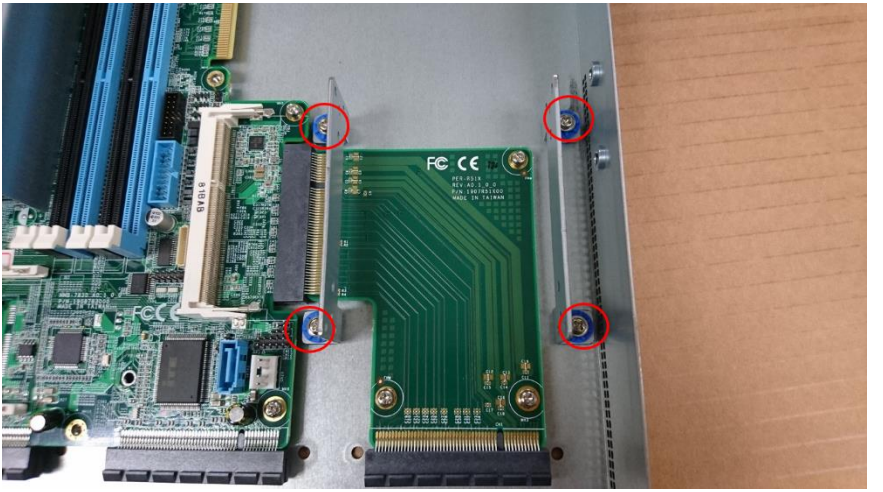
2.4.3 DIO (CN15)

Pin	Signal	Pin	Signal
1	DIO1	2	DIO2
3	DIO3	4	DIO4
5	DIO5	6	DIO6
7	DIO7	8	DIO8
9	3.3V	10	GND

2.6 Installing 3.5" Hard Disk Drive

1. Remove the highlighted screws and remove the top cover.

2. Remove the four highlighted screws to remove the HDD bracket



3. Place the HDD into the bracket, tighten the screws to secure

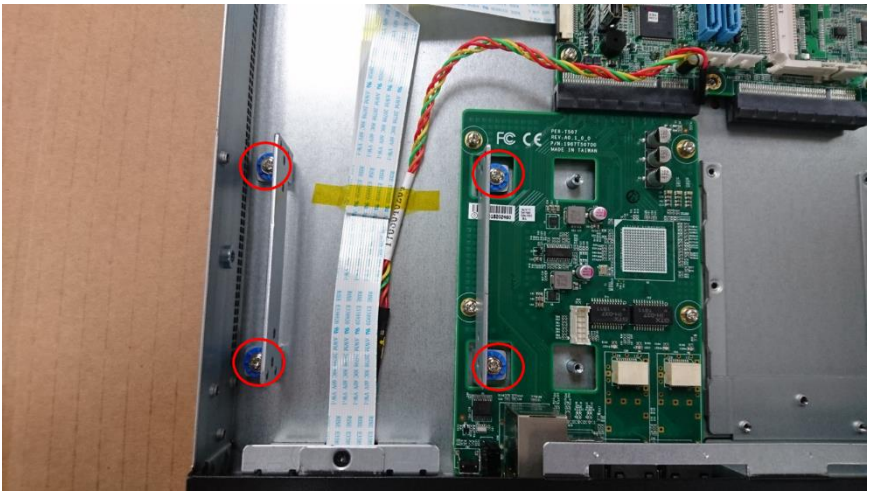
4. Place the assembled HDDs back into the system, secure with screws and reattach the SATA and power cables.


WD
320GB
WD3200BEVT
WD Scorpio Blue

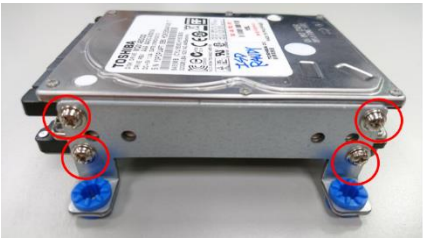
2.7 Installing 2.5" Hard Disk Drive (2 pieces)

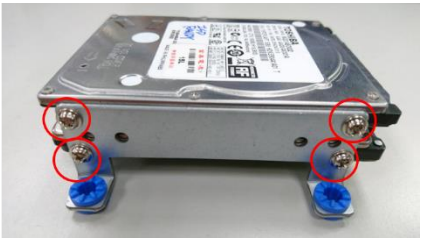
1. Remove the highlighted screws and remove the top cover.

2. Remove the four highlighted screws to remove the HDD bracket

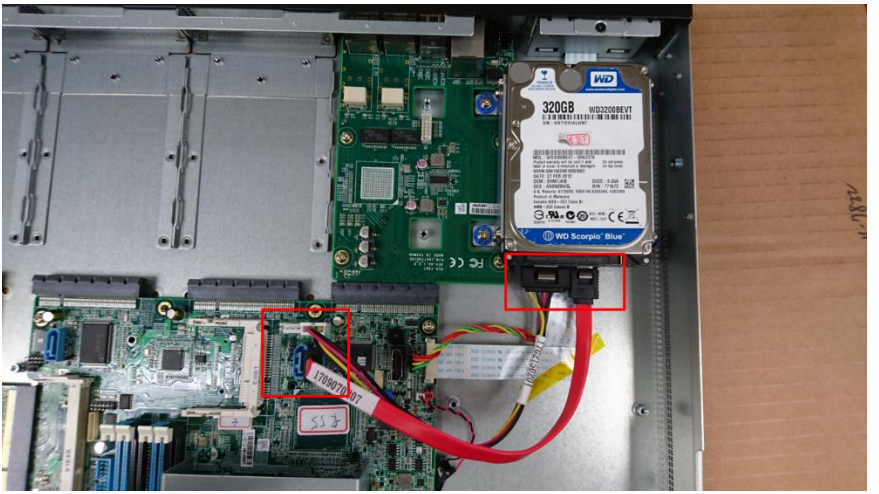


3. Place the HDDs into the bracket, tighten the screws to secure





4. Place the assembled HDDs back into the system, secure with screws and reattach the SATA and power cables.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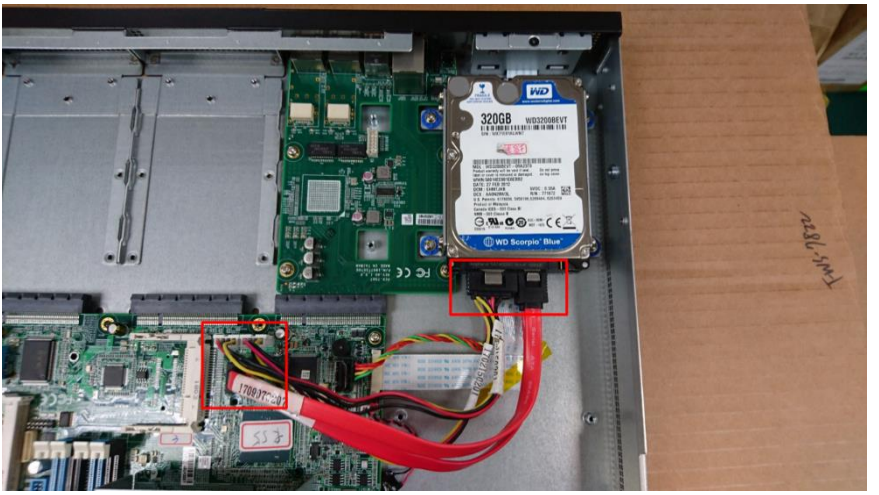
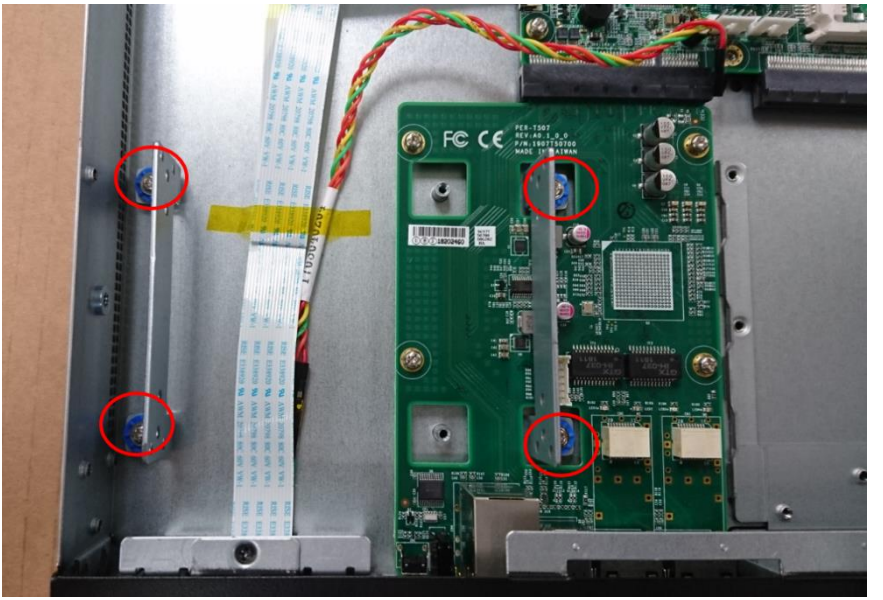
WD3200BEVT
WD Scorpio Blue


320GB
WD3200BEVT
WD Scorpio Blue

2.8 Installing 2.5" Hard Disk Drive (1 piece)

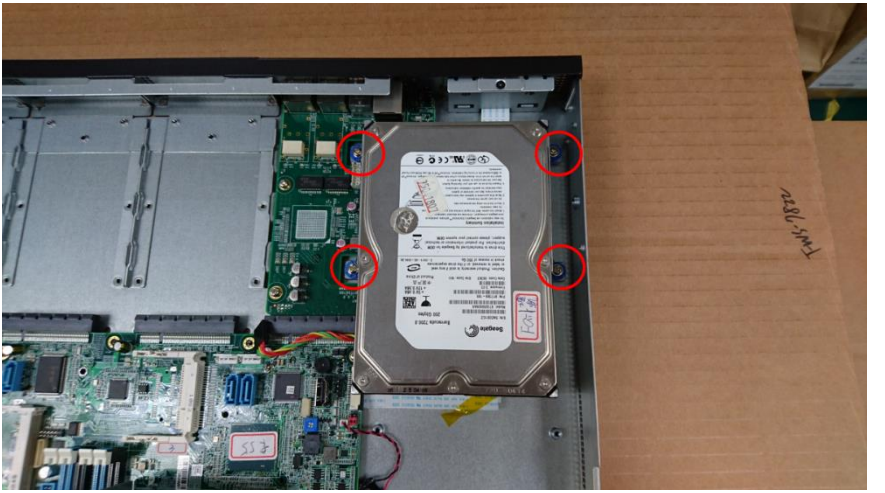
1. Remove the highlighted screws and remove the top cover.

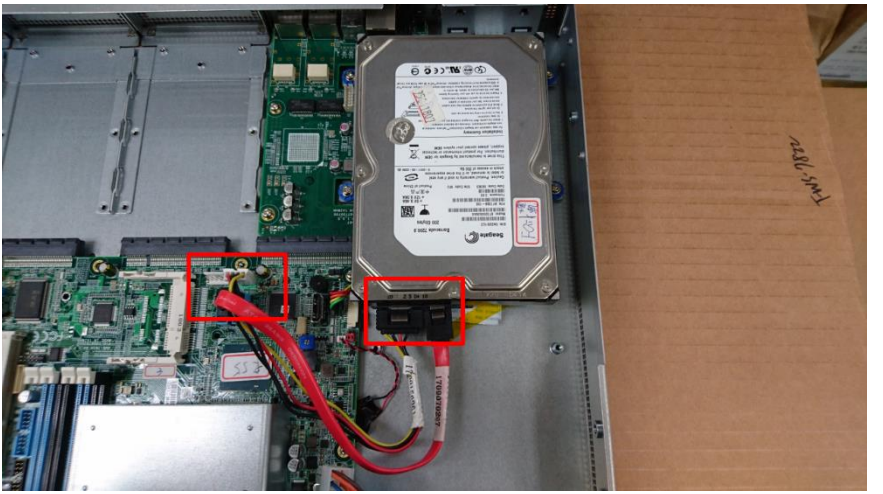
2. Remove the four highlighted screws to remove the HDD bracket



3. Place the HDDs into the bracket, tighten the screws to secure

4. Place the assembled HDDs back into the system, secure with screws and reattach the SATA and power cables.

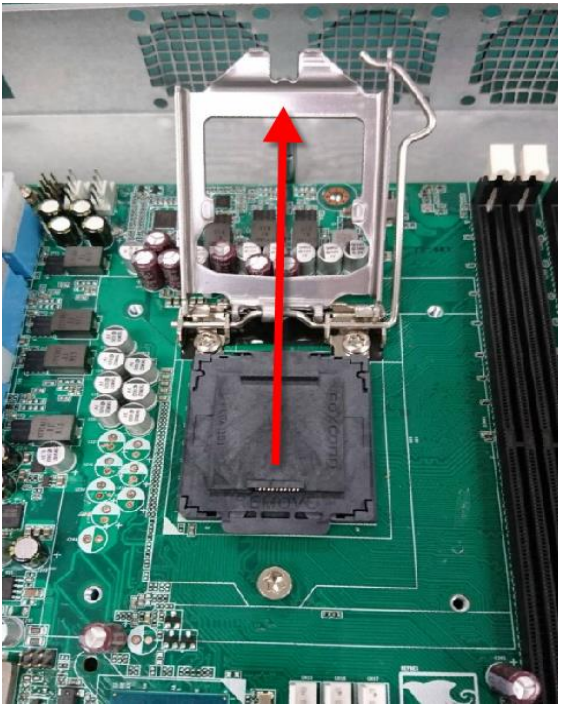




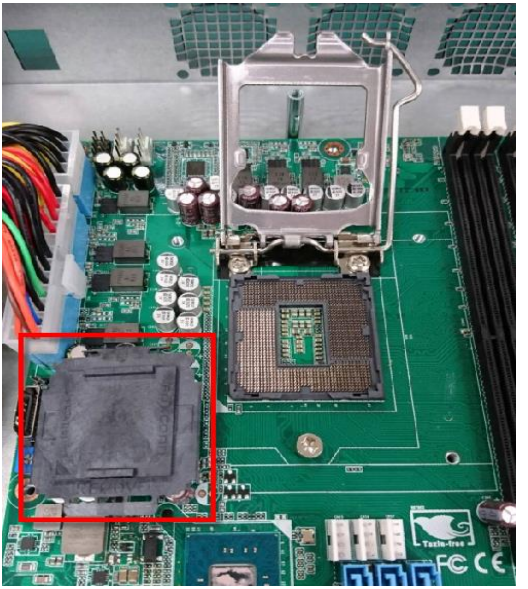
2.9 Installing CPU and Heat Sink

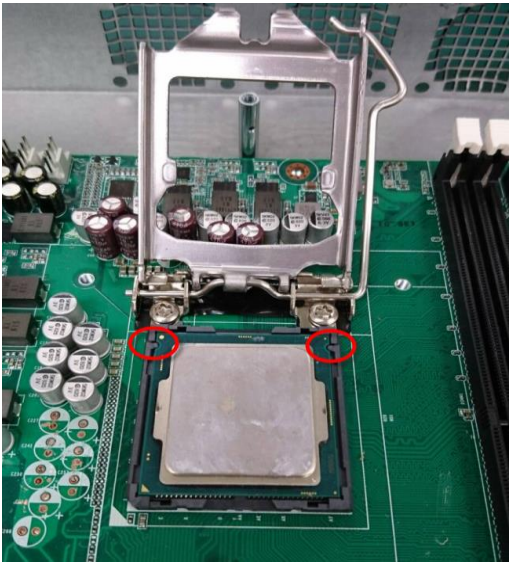
1. Remove the highlighted screws to remove the fan duct

2. Lift the socket arm up to open the CPU socket

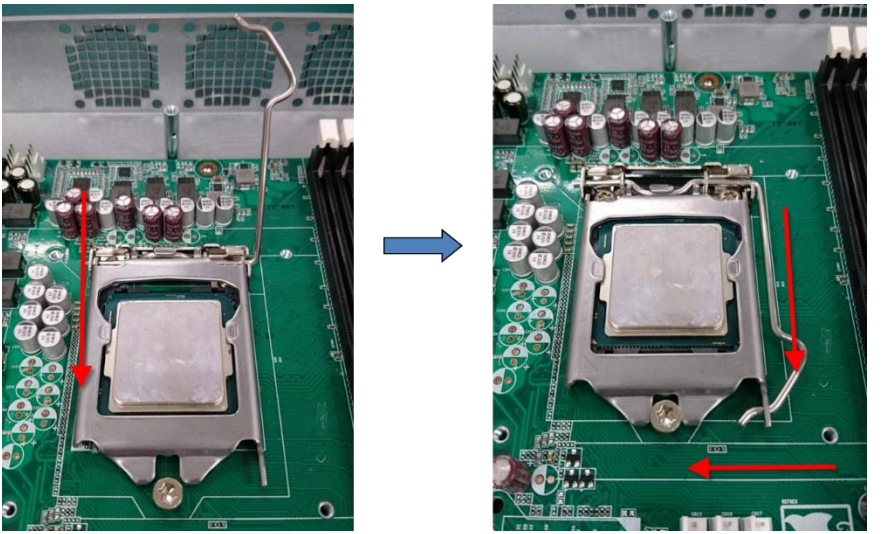


3. Remove the cover and place the CPU into the socket. Make sure the two fillisters are properly locked.

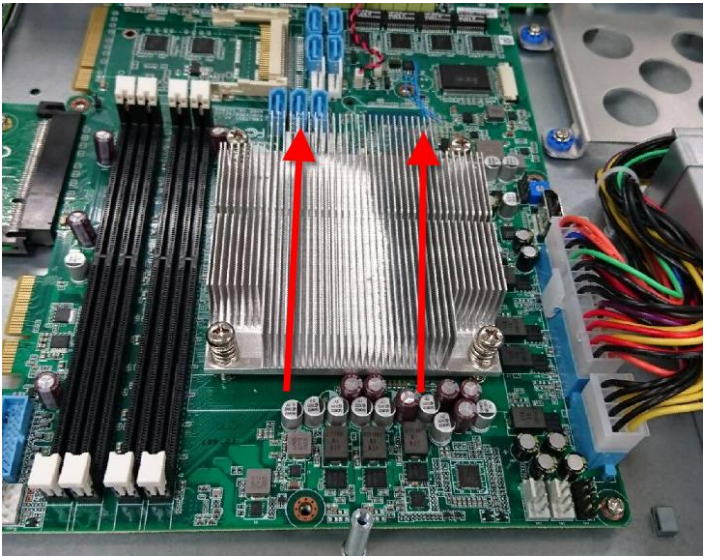




4. Push the arm down to lock the CPU into place



5. Place the heat sink onto the CPU. Make sure the direction of the heat sink is not against the airflow

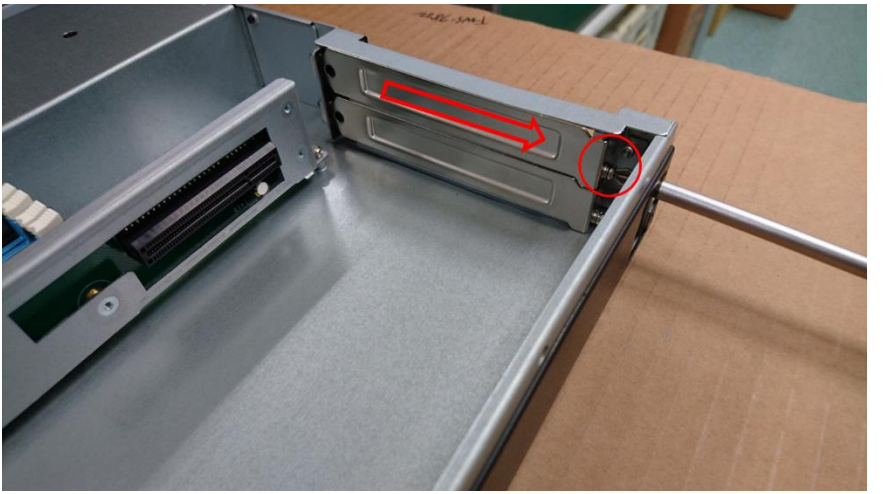


6. Close the air duct and secure with screw

2.10 Installing Expansion Card

1. Remove the highlighted screws and remove the top cover.

2. Remove the screw to remove the cover bracket

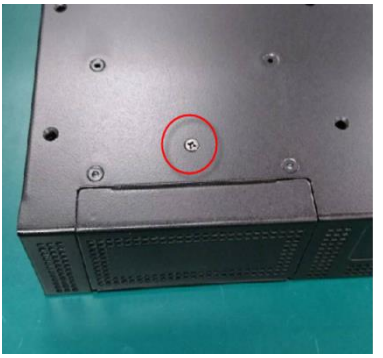


3. Firmly insert the expansion card into the slot and secure the screw.

4. Close the cover bracket and secure the screw.

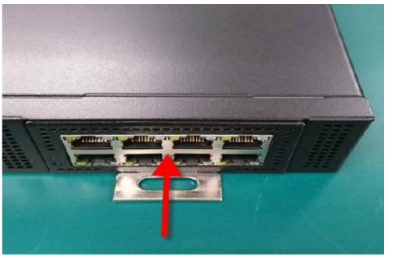
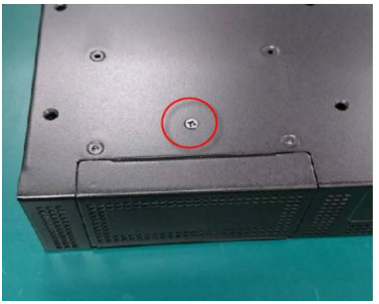
2.10 Installing NIM

1. Remove the highlighted screw on the chassis bottom.



2. Remove the null module cover or existing module.

3. Insert firmly the module and secure the screw.


Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset - Host bridge parameters.

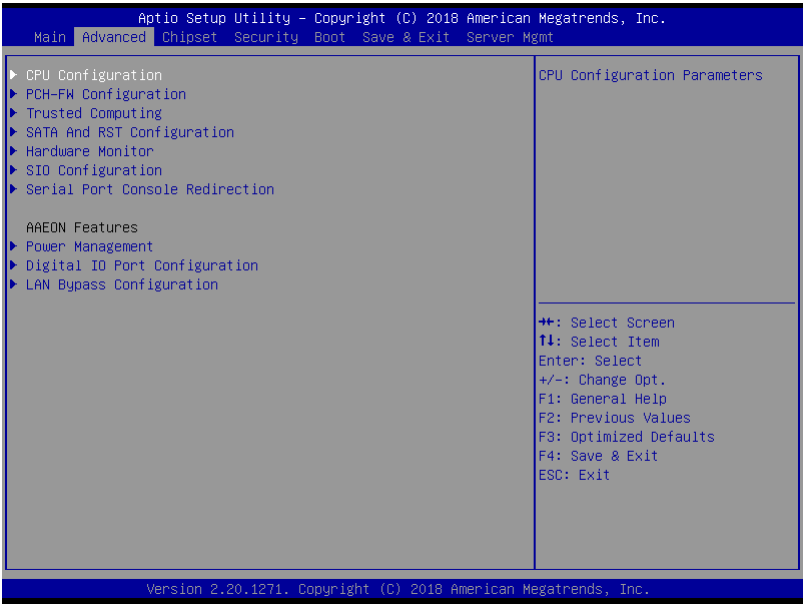
Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

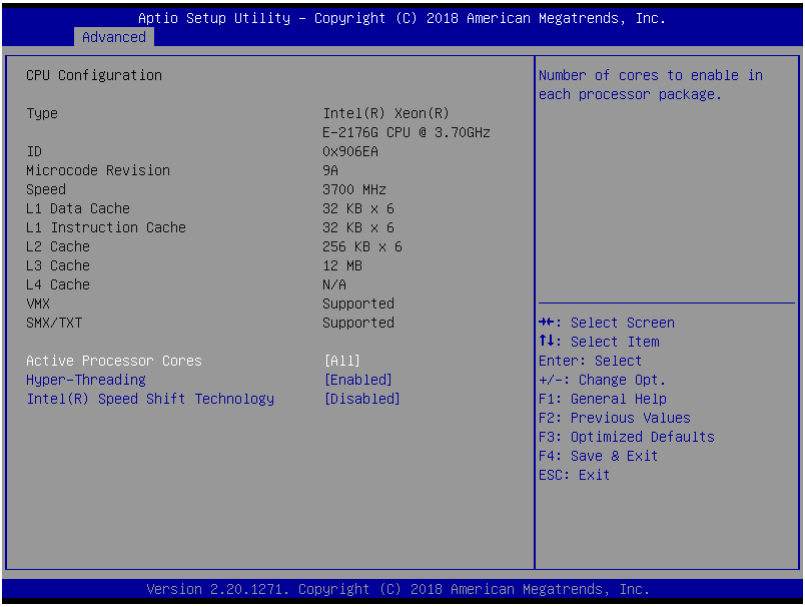
Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



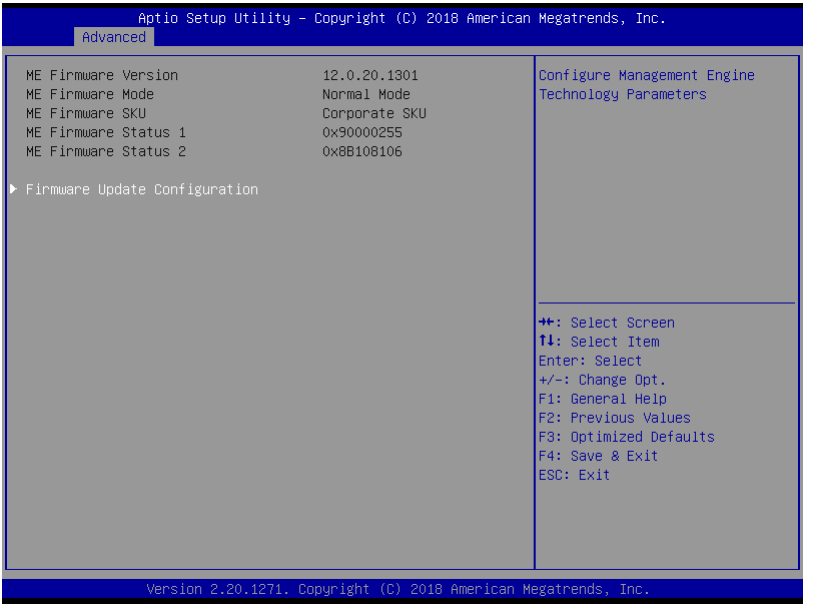
3.4.1 Advanced: CPU Configuration



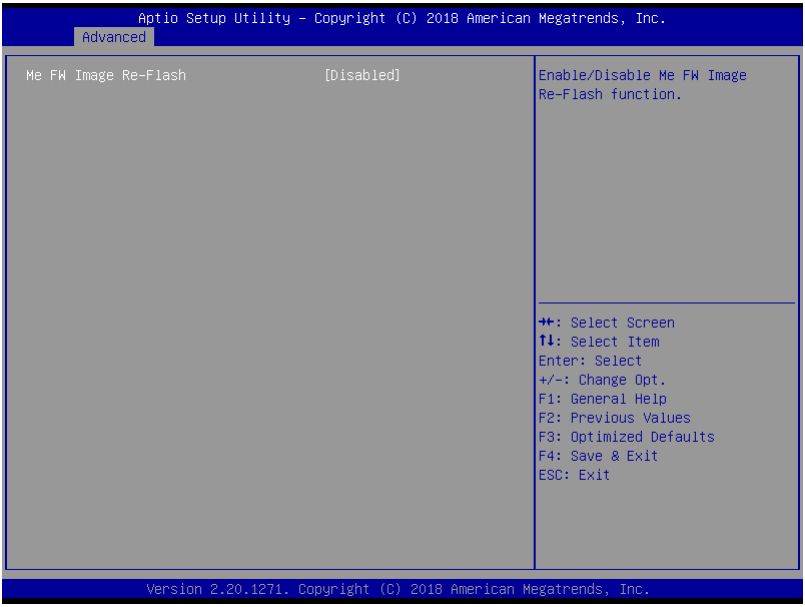
Options summary:

Active Processor Cores	All	Optimal Default, Failsafe Default
	Other Core numbers	
Number of cores to enable in each processor package.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Intel(R) Speed Shift Technology	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.		

3.4.2 Advanced: PCH-FW Configuration



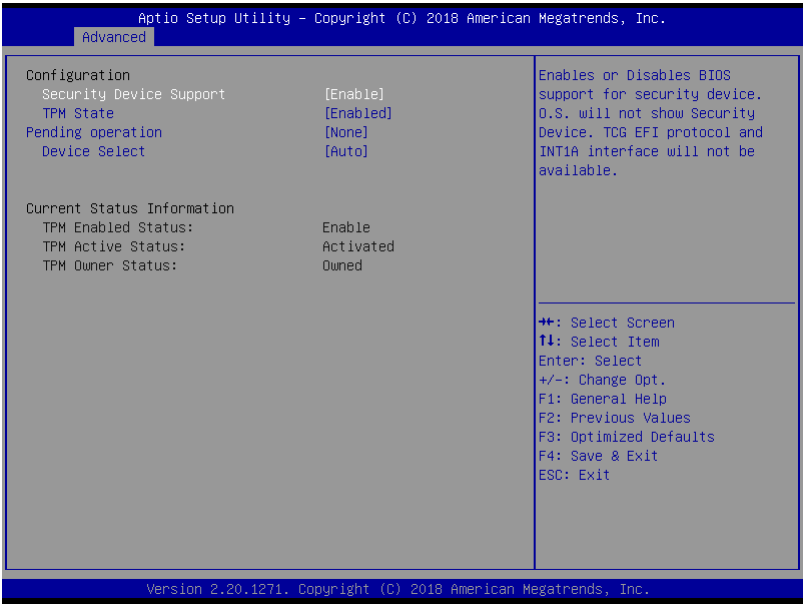
3.4.2.1 Firmware Update Configuration



Options summary:

Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Me FW Image Re-Flash function.		

3.4.3 Advanced: Trusted Computing

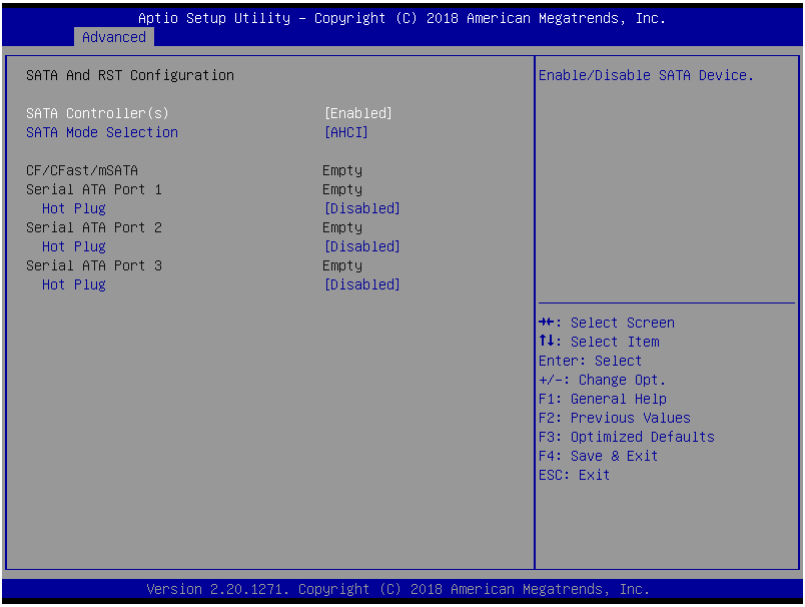


Options summary:

Security Device Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
TPM State	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default

TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

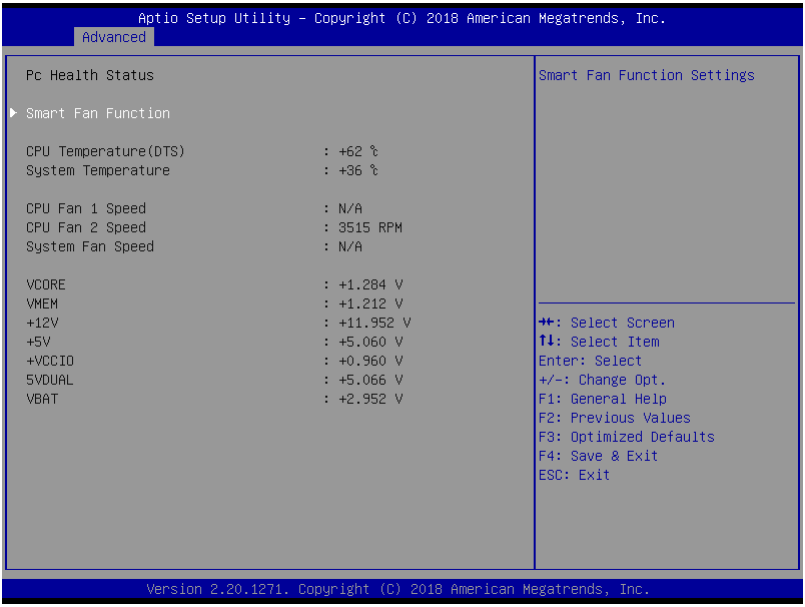
3.4.4 Advanced: SATA And RST Configuration



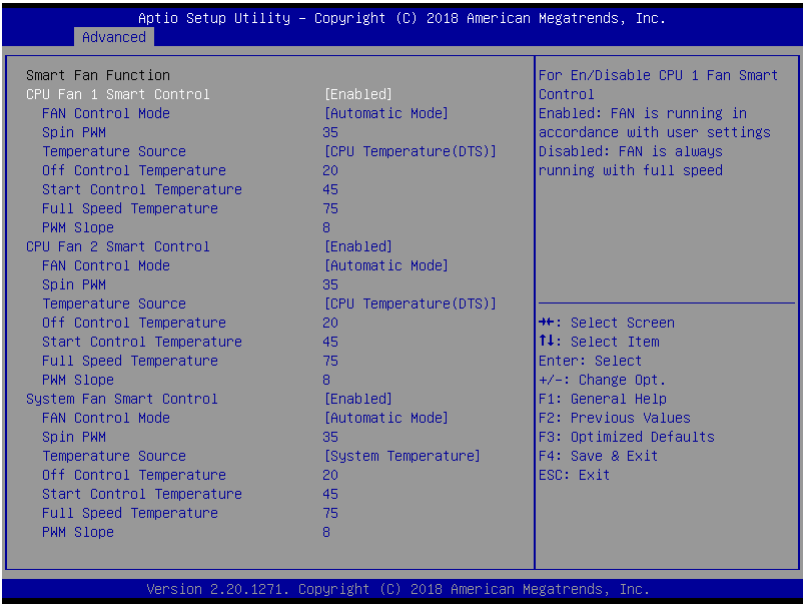
Options summary:

SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable SATA Device.		
SATA Mode Selection	AHCI	Optimal Default, Failsafe Default
	Intel RST Premium With Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		

3.4.5 Advanced: Hardware Monitor



3.4.5.1 Smart Fan Function

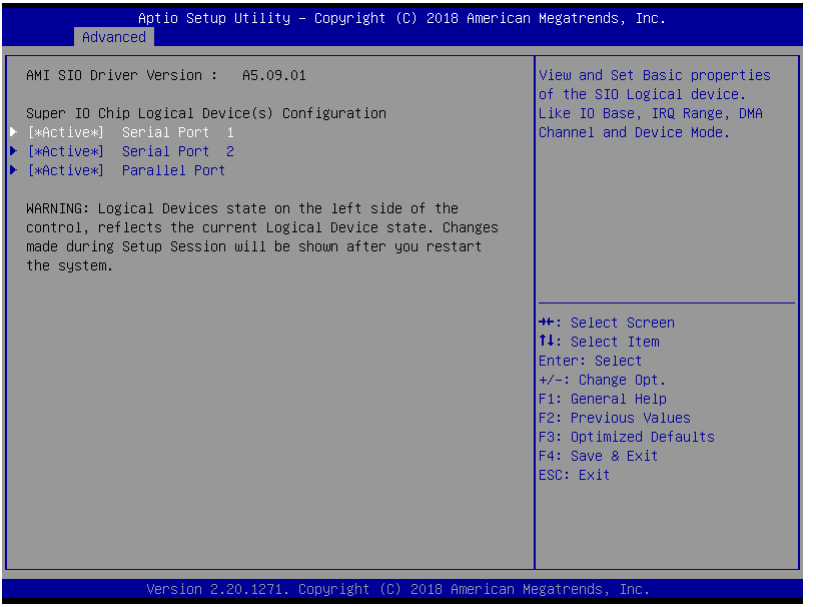


Options summary:

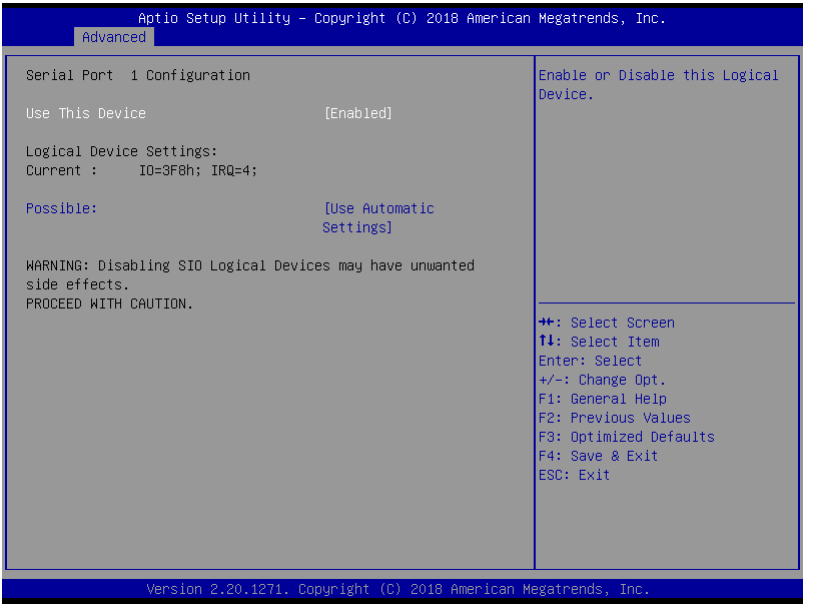
CPU Fan 1 / 2 Smart Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
For En/Disable CPU 1 Fan Smart Control Enabled: FAN is running in accordance with user settings Disabled: FAN is always running with full speed		
System Fan Smart Control	Disabled	
	Enabled	Optimal Default, Failsafe Default
For En/Disable System Fan 2 Smart Control Enabled: FAN is running in accordance with user settings Disabled: FAN is always running with full speed		
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Manual Mode: Depends on PWM Duty Automatic Mode: FAN Speed is depends on CPU Temperature.		
Spin PWM	35	Optimal Default, Failsafe Default
The PWM Dutey of FAN Spin Range: [0 - 255]		
Temperature Source	System Temperature	

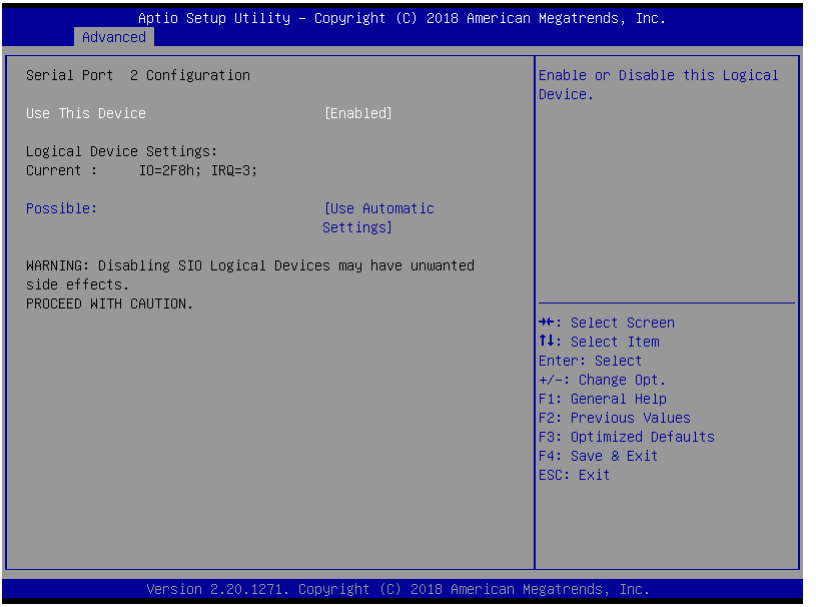
	CPU Temperature(DTS)	Optimal Default, Failsafe Default
Reference Temperature Intput Selection.		
Off Control Temperature	20	Optimal Default, Failsafe Default
Temperature Limit Value of Fan Off Note: Some fans have the minimum speed even if the PWM value is 0		
Start Control Temperature	45	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Start Control		
Full Speed Temperature	75	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Full Speed		
PWM Slope	8	Optimal Default, Failsafe Default
Slope PWM value/Degree C for FAN Speed Control Range:[1-15]		
PWM Duty	200	Optimal Default, Failsafe Default
Manual Mode PWM Duty value Range:[0 - 255]		

3.4.6 Advanced: SIO Configuration



3.4.6.1 Serial Port Configuration

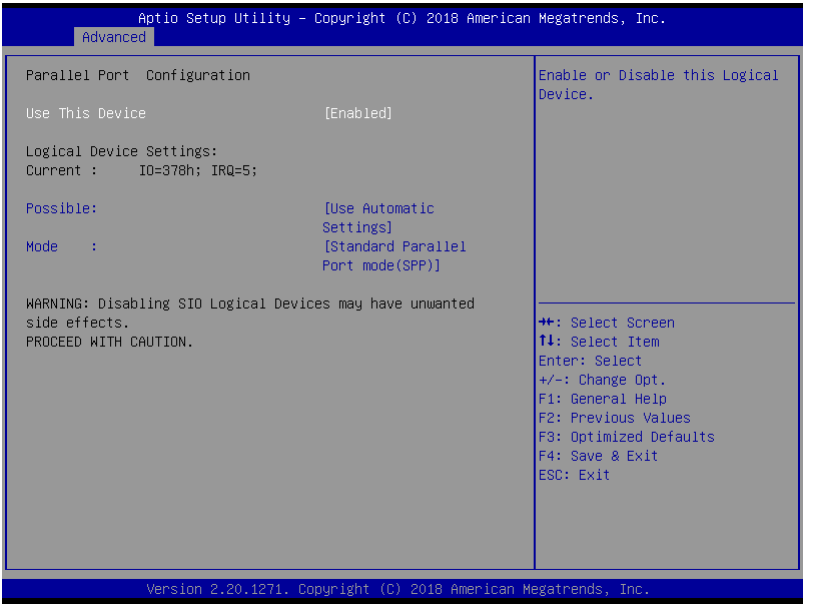




Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

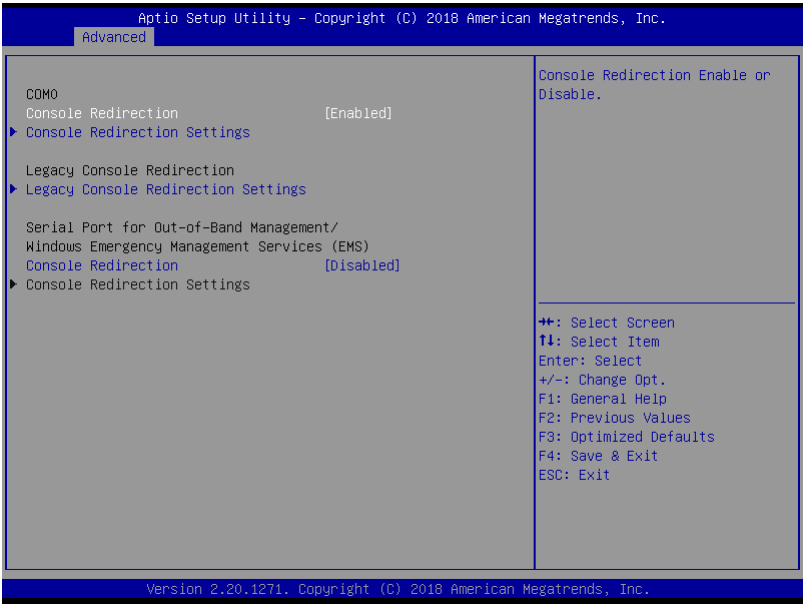
3.4.6.2 Parallel Port Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=378; IRQ=5;	
	IO=378; IRQ=5,6,7,9,10,11,12;	
	IO=278; IRQ=5,6,7,9,10,11,12;	
	IO=3BC; IRQ=5,6,7,9,10,11,12;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	Standard Parallel Port mode(SPP)	Optimal Default, Failsafe Default
	EPP Mode	
	ECP Mode	
	EPP mode & ECP mode	
Change Parallel Port mode. Some of the Modes required a DMA resource. After Mode changing, Reset the System to reflect actual device settings.		

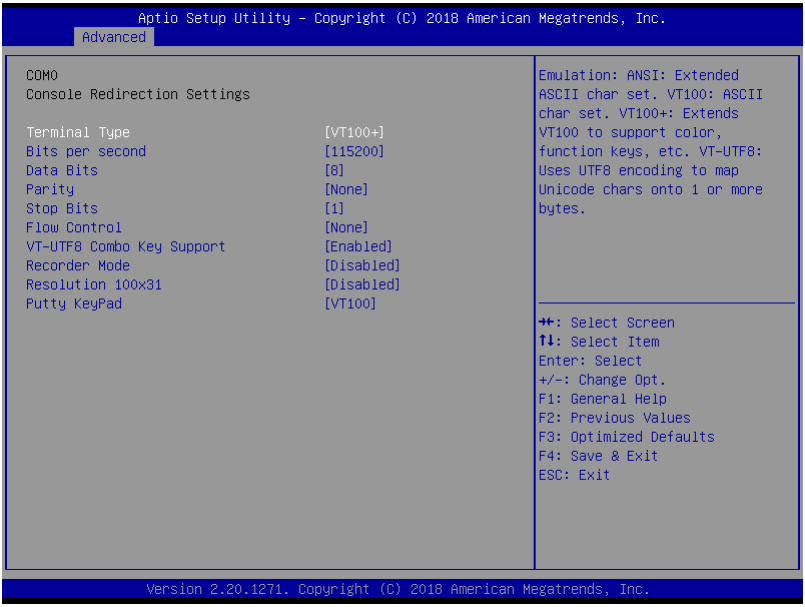
3.4.7 Advanced: Serial Port Console Redirection



Options summary:

COM0		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Serial Port for Out-of-Band Management / Windows Emergency Management Services		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.4.7.1 COM0 Console Redirection

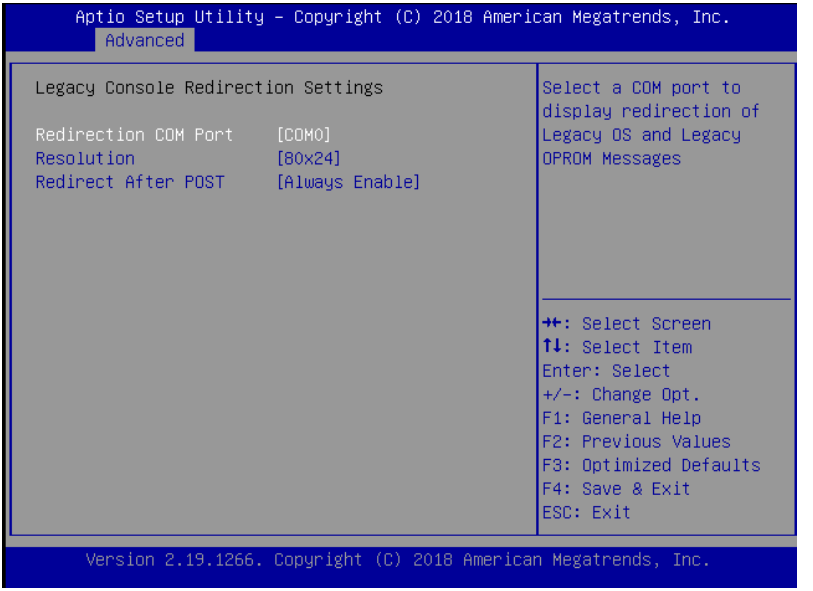


Options summary:

Terminal Type	VT100	
	VY100+	Optimal Default, Failsafe Default
	VT-UTF8	
	ANSI	
Emulation : ANSI : Extended ASCII char set. VT100 : ASCII char set. VT100+ : Extends VT100 to support color, function keys, etc. VT-UTF8 : Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	
	57600	
	11520	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data bit	7	

	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

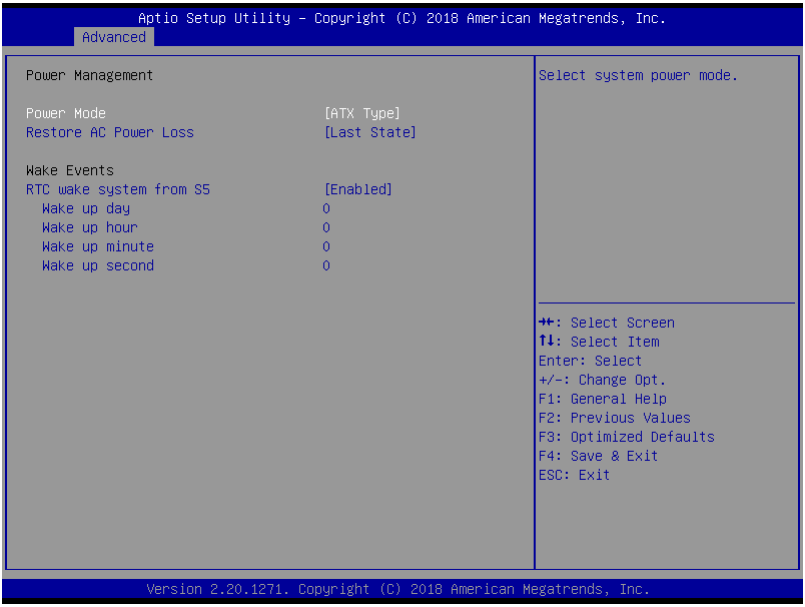
3.4.7.2 Legacy Console Redirection Settings



Options summary:

Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection.		
Redirection After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When BootLoader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is		

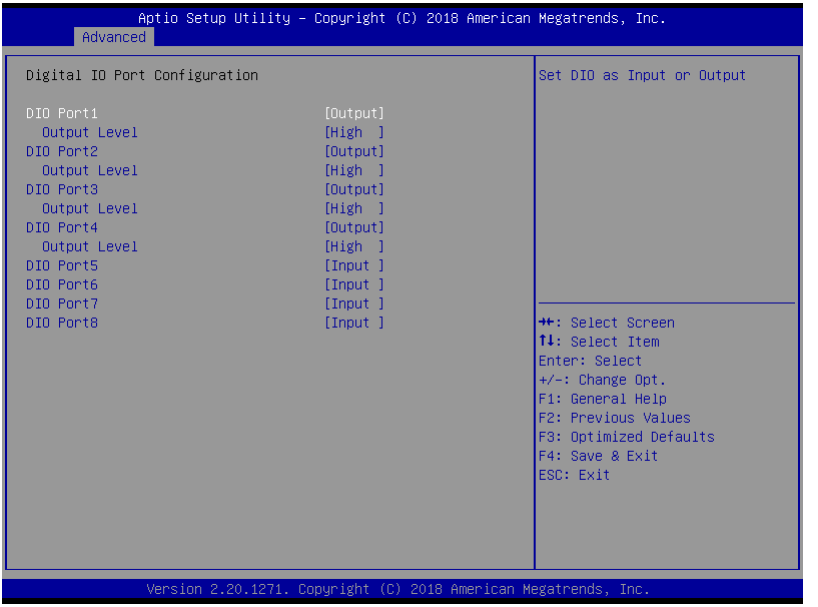
3.4.8 Advanced: Power Management



Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Enabled	
Fixed Time : System will wake on the hr :: min :: sec Specified Dynamic Time : System will wake on the current time + Increase minutes(s).		

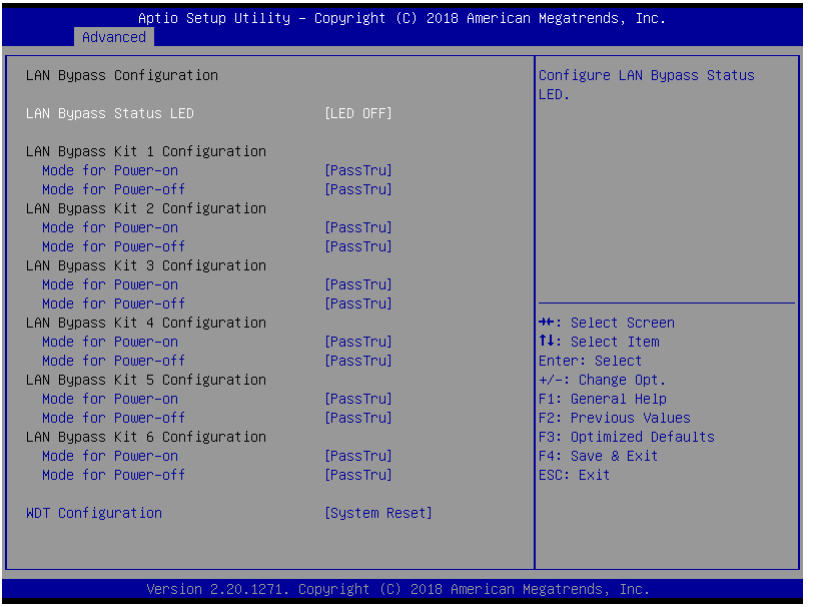
3.4.9 Advanced: Digital IO Port Configuration



Options summary:

DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input or Output		

3.4.10Advanced: LAN Bypass Configuration

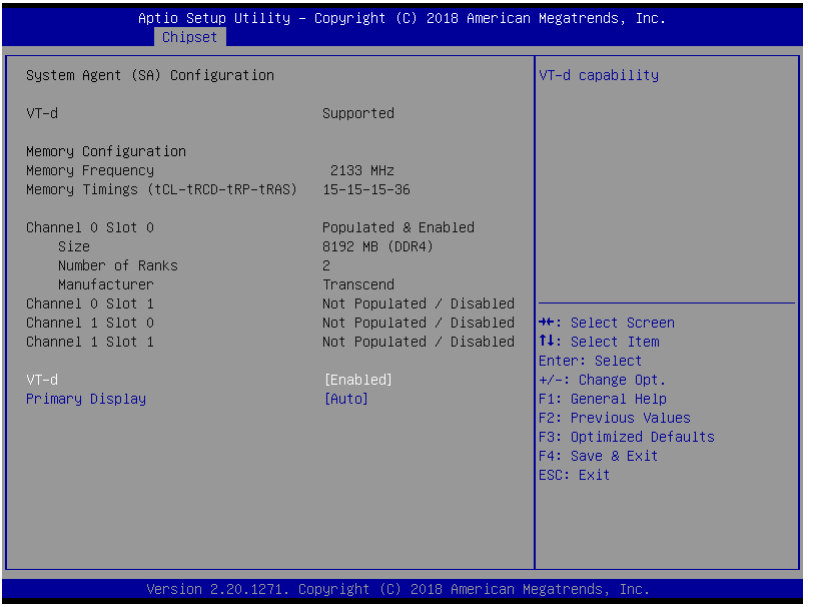


Options summary:

Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
LAN Bypass Status LED		
Mode for Power-on	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through)		
Mode for Power-off	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through)		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure LAN kit behavior when WDT is triggered. (Bypass/Pass Through)		

3.5 Setup submenu: Chipset

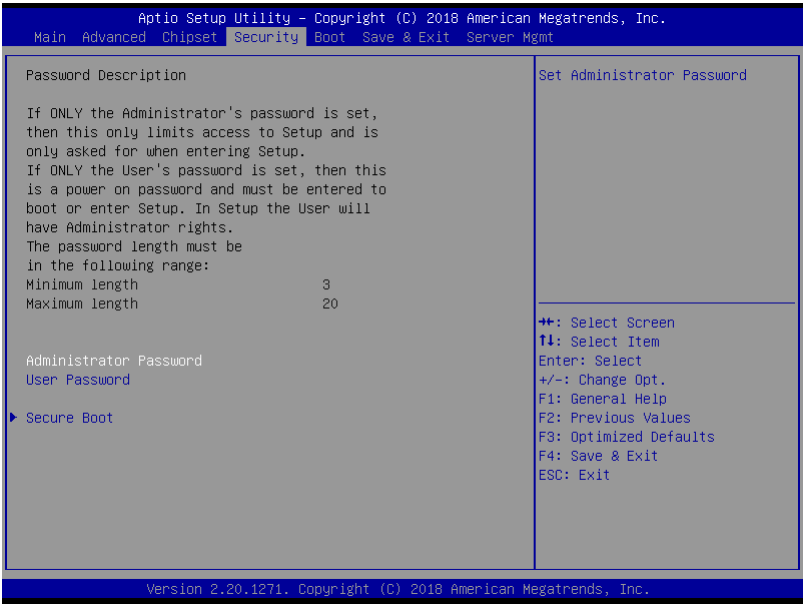
3.5.1 Chipset: System Agent (SA) Configuration



Options summary:

VT-d	Disabled	
	Enabled	Optimal Default, Failsafe Default
VT-d capability		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCI	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		

3.6 Setup submenu: Security



Change User/Administrator Password

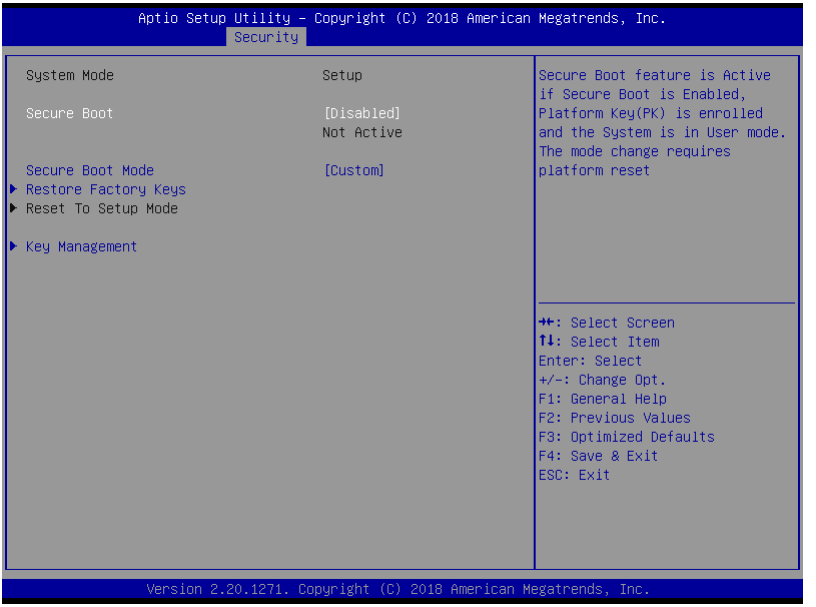
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

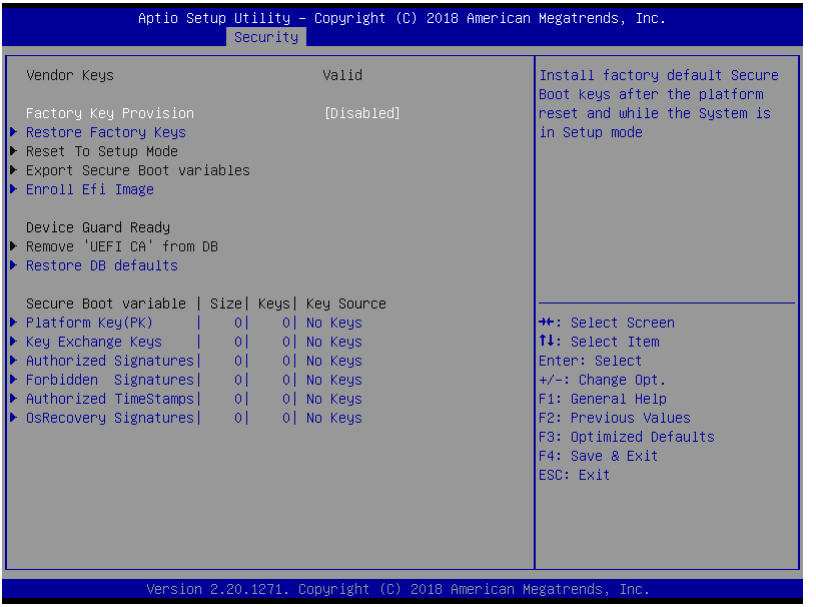
3.6.1 Security: Secure Boot



Options summary:

Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Customized	Optimal Default, Failsafe Default
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	No	Press 'Yes' to restore factory default keys
	Yes	
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode	No	Press 'Yes' to reset to setup mode
	Yes	
Delete all Secure Boot key databases from NVRAM		

3.6.2 Security: Key Management

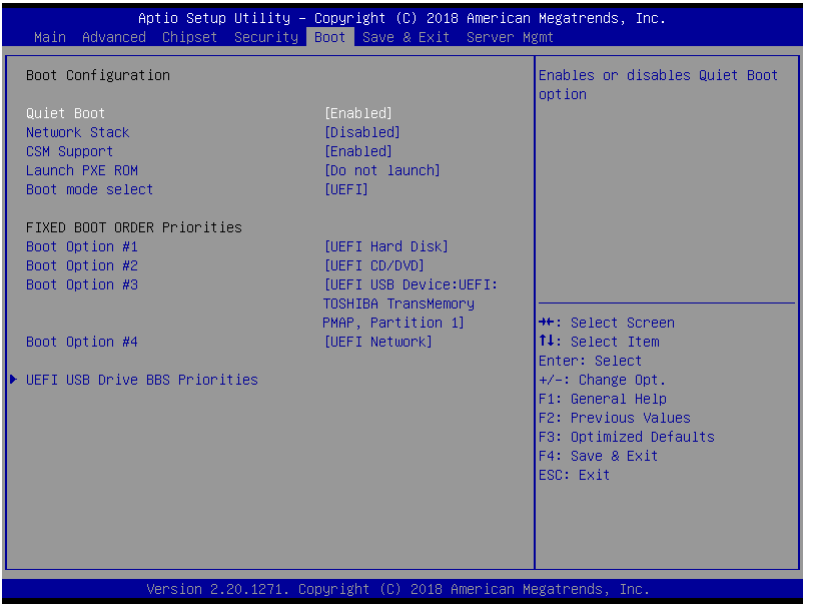


Options summary:

Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode		
Restore Factory Keys	No	Press 'Yes' to restore factory default keys
	Yes	
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode	No	Press 'Yes' to reset to setup mode
	Yes	
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables	Select a File system to export Secure Boot variables	
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image	Select a File system to enroll Efi image into Authorized Signature Database.	

Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	
Remove 'UEFI CA' from DB	
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)	
Restore DB defaults	Press 'Yes' to restore DB variable to factory defaults
Restore DB variable to factory defaults	

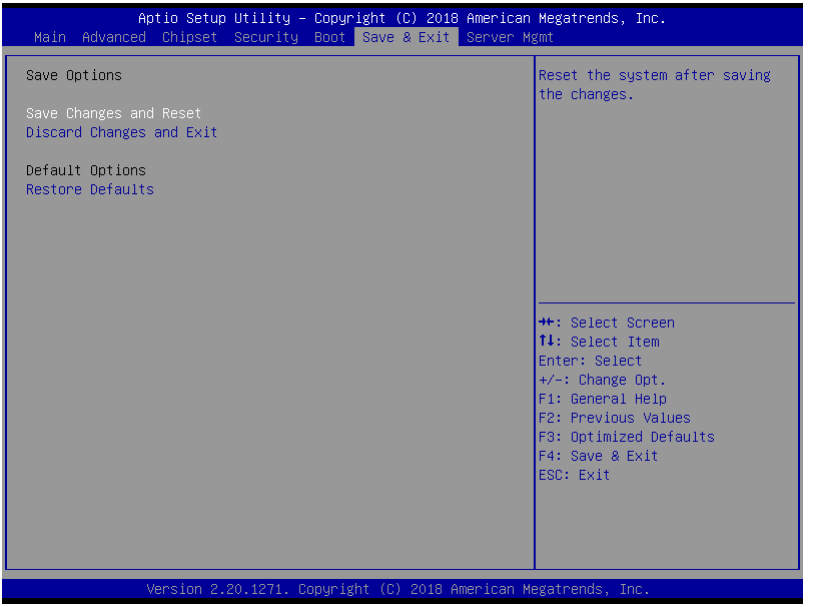
3.7 Setup submenu: Boot



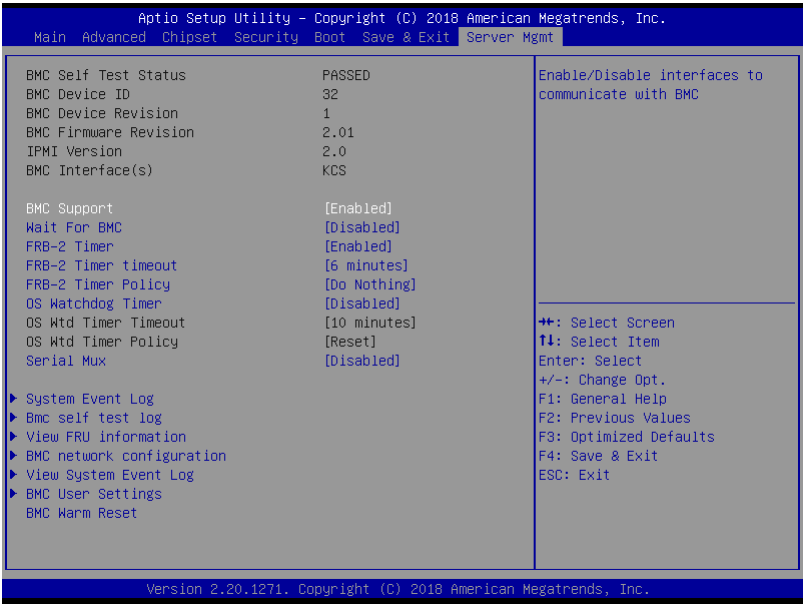
Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack (For UEFI PXE Support)		
CSM Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CSM Support.		
Launch PXE ROM	Do not launch	Optimal Default, Failsafe Default
	UEFI	
	Legacy	
Controls the execution of UEFI and Legacy Network OpROM Note: Network Stack should be enabled if select UEFI PXE boot.		
Boot mode select	Legacy	
	UEFI	Optimal Default, Failsafe Default
	DUAL	
Select boot mode LEGACY/UEFI		

3.8 Setup submenu: Save & Exit



3.9 Setup submenu: Server Mgmt



Options summary:

BMC Support	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable/Disable interfaces to communicate with BMC		
Wait For BMC	Enabled	
	Disabled	Optimal Default, Failsafe Default
Wait For BMC response for specified time out. BMC starts at the same time when BIOS starts during AC power ON. It takes around 30 seconds to initialize Host to BMC interfaces.		
FRB-2 Timer	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable FRB-2 timer(POST timer)		
FRB-2 Timer timeout	3 minutes	
	4 minutes	
	5 minutes	
	6 minutes	Optimal Default, Failsafe Default
Enter value Between 3 to 6 min for FRB-2 Timer Expiration value		
FRB-2 Timer Policy	Do Nothing	Optimal Default, Failsafe Default

	Reset	
	Power Down	
	Power Cycle	
Configure how the system should respond if the FRB-2 Timer expires. Not available if FRB-2 Timer is disabled.		
OS Watchdog Timer	Enabled	
	Disabled	Optimal Default, Failsafe Default
If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy.		
OS Wtd Timer Timeout	5 minutes	
	10 minutes	Optimal Default, Failsafe Default
	15 minutes	
	20 minutes	
Configure the length of the OS Boot Watchdog Timer. Not available if OS Boot Watchdog Timer is disabled.		
OS Wtd Timer Policy	Do Nothing	
	Reset	Optimal Default, Failsafe Default
	Power Down	
	Power Cycle	
Configure how the system should respond if the OS Boot Watchdog Timer expires. Not available if OS Boot Watchdog Timer is disabled.		
Serial Mux	Enabled	
	Disabled	Optimal Default, Failsafe Default
Press <Enter> to enable or disable Serial Mux configuration.		

Chapter 4

Drivers Installation

4.1 Drivers Installation

The drivers can be found in the product page for FWS-7830 at aaeon.com. Please follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **Step 1 - Chipset** folder followed by the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **Step 2 - Graphic** folder and select your OS
2. Open the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install ME Driver

1. Open the **Step 3 – ME** folder followed by the **MEISetup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install LAN Driver

1. Open the **Step 4 - LAN** folder followed by the **PROWinx64_23.5.1** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install Intel RST Driver

1. Open the **Step 5 – Intel RST** folder followed by the **SetupRST.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID   WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*********************************************************************************
```

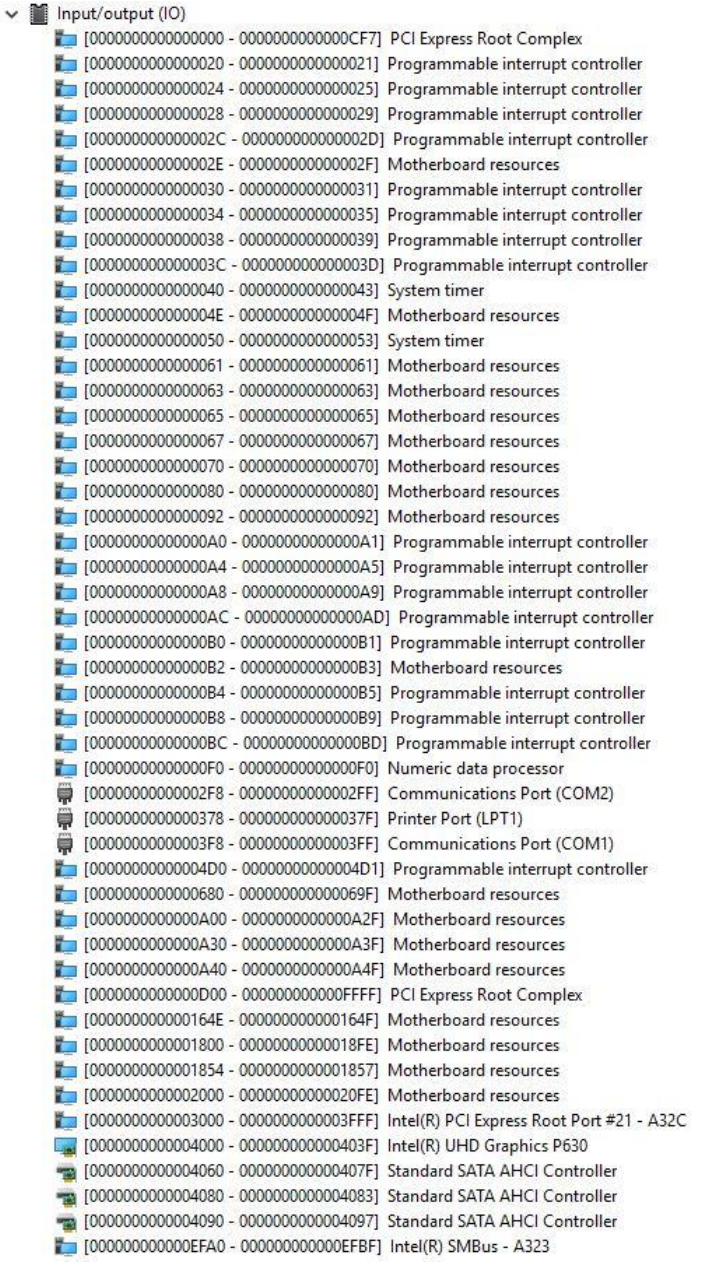
```
*****************************************************************************************
VOID   SIOEnterMBPnPMode(){
        Switch(SIOIndex){
                Case 0x2E:
                        IOWriteByte(SIOIndex, 0x87);
                        IOWriteByte(SIOIndex, 0x01);
                           IOWriteByte(SIOIndex, 0x55);
                           IOWriteByte(SIOIndex, 0x55);
                           Break;
                Case 0x4E:
                        IOWriteByte(SIOIndex, 0x87);
                        IOWriteByte(SIOIndex, 0x01);
                           IOWriteByte(SIOIndex, 0x55);
                           IOWriteByte(SIOIndex, 0xAA);
                        Break;
        }
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0x02);
        IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}
*****************************************************************************************
```

```
*********************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*********************************************************************************
```

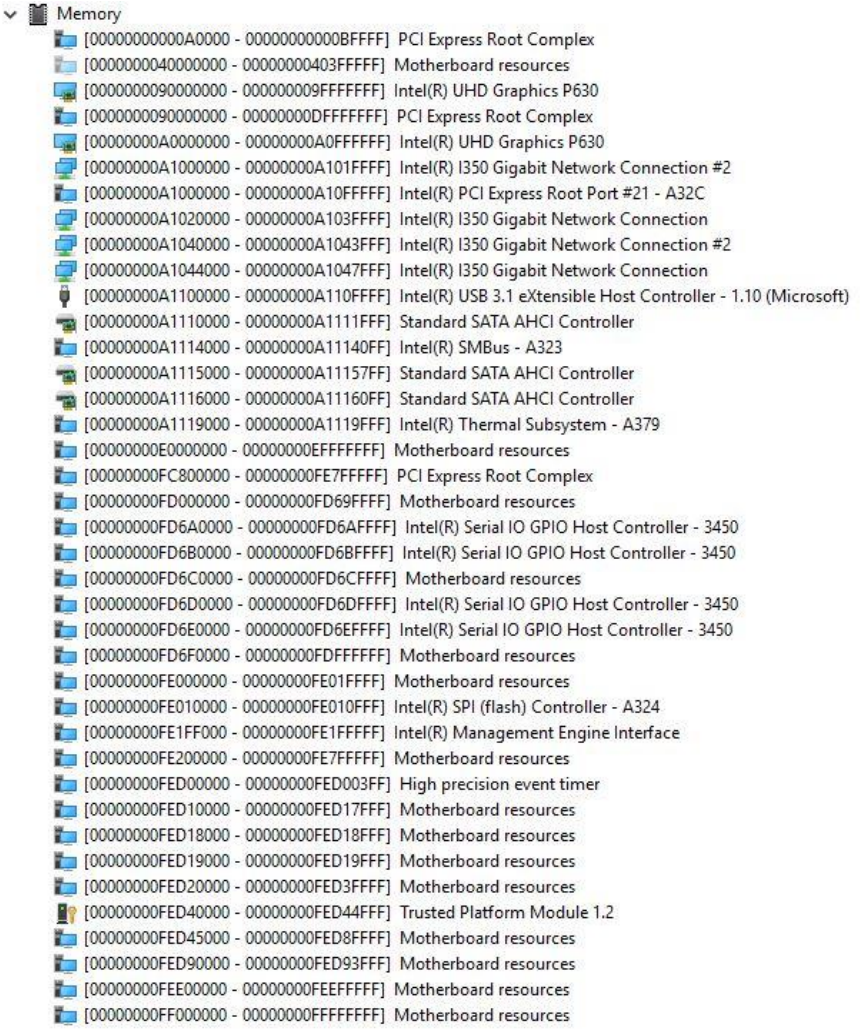
Appendix B

I/O Information

B.1 I/O Address Map



B.2 Memory Address Map



B.3 IRQ Mapping Chart

Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

C.1.1 Introduction

The FWS-7830 provides an LED indicator which can change the LED status by AAEON SDK. The user is able to program the LED status to express different status.

C.1.2 Status LED Configuration

Table 1 : Turth Table of Status LED			
STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table 2 : Status LED relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

C.1.3 Sample Code

```
*********************************************************************************************
#define Byte   CPLD_SLAVE_ADDRESS       //This parameter is represented from Note1
#define Byte   OFFSET                   //This parameter is represented from Note2
*********************************************************************************************
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
{
        //Green LED On
```

```
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*********************************************************************************************
```

C.2 LAN Bypass

C.2.1 Introduction

The FWS-7830 provides a LAN Bypass kit and allows uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

C.2.2 LAN Bypass Configuration

Table 1 : ID Select table of LAN kit				
LAN_ID3	LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	0	LAN Kit 1 Selected
0	0	0	1	LAN Kit 2 Selected
0	0	1	0	LAN Kit 3 Selected
...				...
1	1	1	1	LAN Kit 16 Selected

Table 2 : LAN Bypass relative register table	
Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refert to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge

	triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3 : LAN Bypass relative register mapping table				
CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

****

C.2.3 Sample Code

```
*********************************************************************************************
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*********************************************************************************************
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xBF;
else                                // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xDF;
else                                // Bypass
```

```
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
        bData = bData & 0xEF;
else                            // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*********************************************************************************
```

C.3 Software Reset button (General Propose Input)

C.3.1 Introduction

The FWS-7830 provides a general propose input button which gets its status by the AAEON SDK.

C.3.2 LAN Bypass Configuration

Table 2 : LAN Bypass relative register table	
Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1 : Soft Reset Button register mapping table				
	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

C.3.3 Sample Code

```
*********************************************************************************
#define Word        BTN_STS        //This parameter is represented from Note1
#define ByteBTN_STS_R              //This parameter is represented from Note2
*********************************************************************************
Byte    GET_Value (Word IoAddr, Byte BitNum,Byte Value){
        BYTE  TmpValue;

        TmpValue = inportb (IoAddr);
         return    (TmpValue & (1 << BitNum))
}
*********************************************************************************
VOID    Main(){
        Byte RstBtn;

        RstBtn = GET_Value (BTN_STS, BTN_STS_R);  // Active Low
}
*********************************************************************************
```