FWS-7820

Network Appliance

User's Manual 2nd Ed

Last Updated: January 29, 2019

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-7820	1
● EAR bracket kit	1
● Console cable	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O
外壳	O	O	O	O	O	O
中央处理器与内存	O	O	O	O	O	O
硬盘	O	O	O	O	O	O
电源	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	O	O	O	O	O	O
Hard Disk	O	O	O	O	O	O
PSU	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

Platform	
Form Factor	1U Rackmount Network Platform
Processor	Intel® 6th Generation Core™/ Xeon Processors
Chipset	Intel® C236
System Memory	- DDR4 1600/1866/2133 UDIMM/ECC - Up to 64GB - 288-pin DIMM x 4

Network	
Ethernet	Intel® i210 GbE x 2, Intel® 82580 x4
Bypass	Onboard 2 pairs bypass, others depend on NIM module
NIM Slot	4 (Max. 5 slots by project base)

Display	
Graphic Controller	Intel® Integrated
Connector	VGA cable (Optional)

Storage

HDDs	Internal 3.5" SATA HDD x 1 or 2.5" SATA HDD x 2 (Optional)* *(mSATA/ CF/ CFast will be disabled if 2nd SATA HDD is used)
CF/CFast/mSATA	CF socket x 1 (Optional BOM CFast™ socket or mSATA slot)

Expansion/Internal Interface

PCIe slot	PCIe [x4] signal use [x8] slot (3rd NIM slot will be disabled if PCIe Riser supported)
Mini-PCIe slot	—
Keyboard and Mouse	Pin-header
Universal Serial Bus	USB 3.0 x 2, Box Header (2.0mm)

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable, 1 sec per step
Software Button	GPIO Programmable push button x 1
TPM	TPM2.0 9665 (TPM v1.2 9660 optional)
GPIO	8bits, BIOS default 4 bits input, 4bits output.
FAN	2

Miscellaneous

MTBF (Hours)	71,852
Color	Black

Environmental Parameters and Dimension

Power Requirement	250W ATX PSU
Operation Temp.	32°F ~ 104°F (0°C ~ 40°C)
Storage Temp.	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10% ~ 80% relative humidity, non-condensing
Storage Humidity	10% ~ 80% @ 40°C, non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz/ operation (3.5" H.D.D) 1.5 Grms/ 5 ~ 500Hz/ no operation
Shock	10G peak acceleration (11 m sec. duration), operation 20G peak acceleration (11 m sec. duration), non-operation
Chassis Dimension (W x D x H)	16.93" x 18.7" x 1.73" (430mm x 475mm x 44mm)

I/O Interfaces

Front Panel	- Power LED x 1 - Status LED x 1 - HDD Active LED x 1 - USB 3.0 Ports x 2 - RJ-45 Console x 1 - Parallel LCM display and 4 keypad x 1 (Optional w/ NIM slot) - Software Programmable Switch x 1 - Bypass LED x 2
Rear Panel	- AC Power Input x 1 - Power Switch x 1 - VGA port (Optional) - Rear Expansion Slot x 1 (Optional PCIe [x4] signal use [x8] slot, 3rd NIM slot will be disabled if PCIe Riser supported)

Note 1: 2nd SATA is Co-layout with mSATA/CF/CFast. The default is CF and you can choose any one from the 4 options.

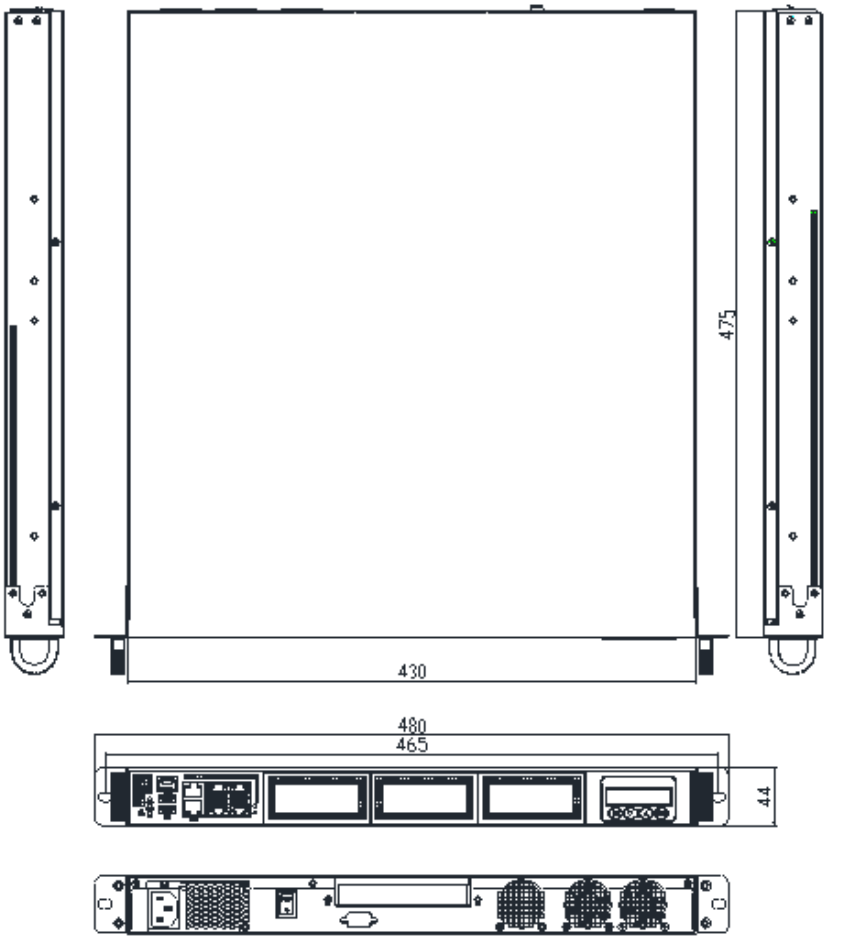
Note 2: PCIe[x4] riser card shares 1 NIM slot signal and the NIM slot next to LCM will be disabled.

Chapter 2

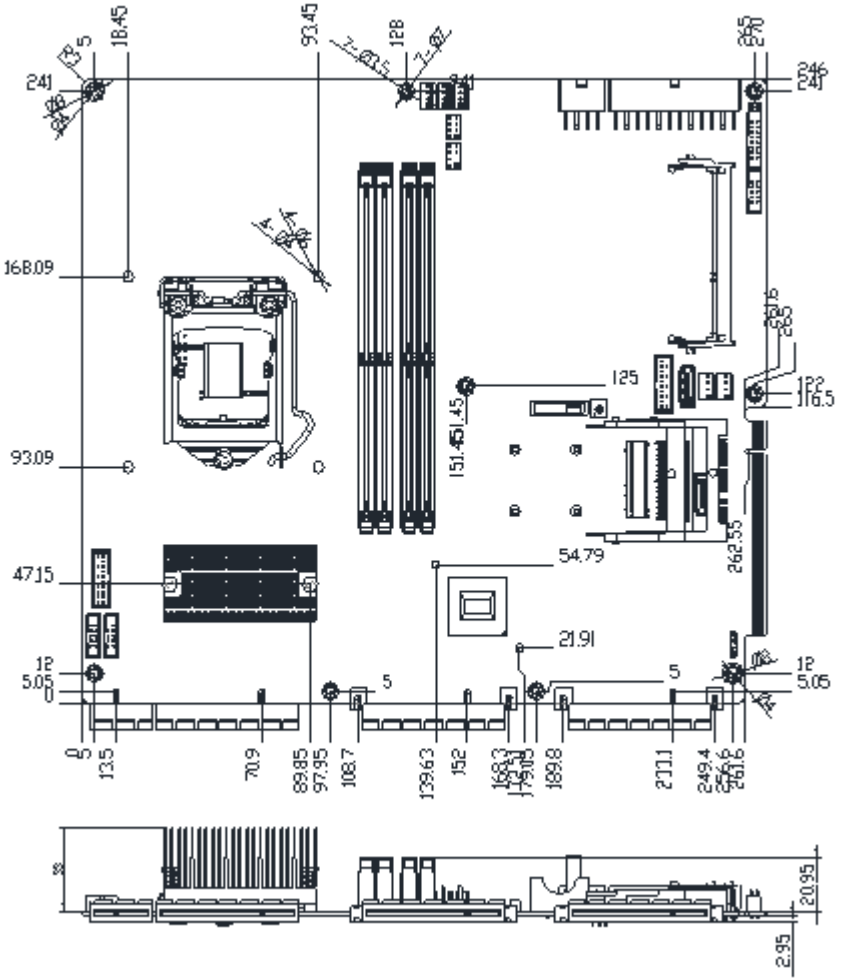
Hardware Information

2.1 Dimensions

System



Board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12.8
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125
151.45
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54.79
21.91
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13.5
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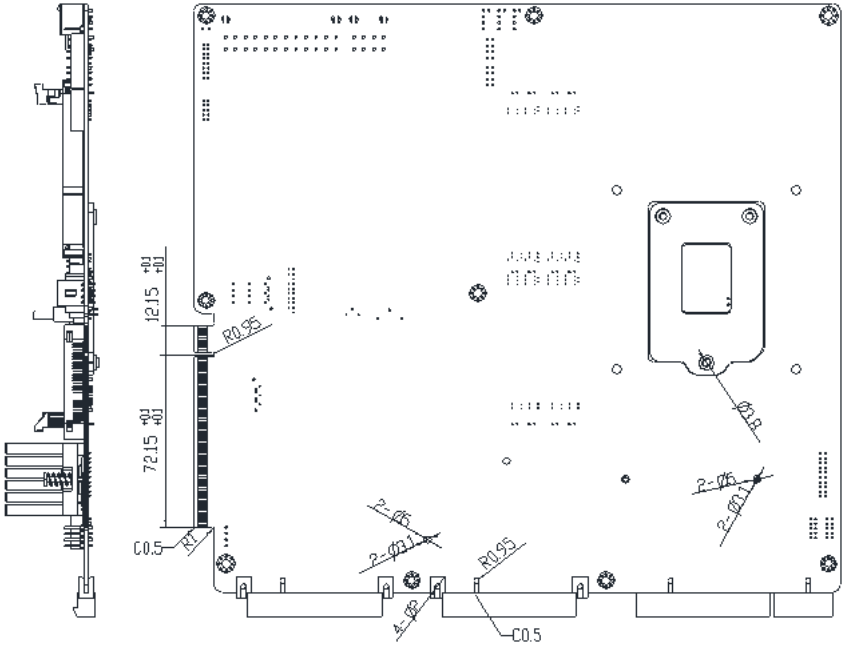
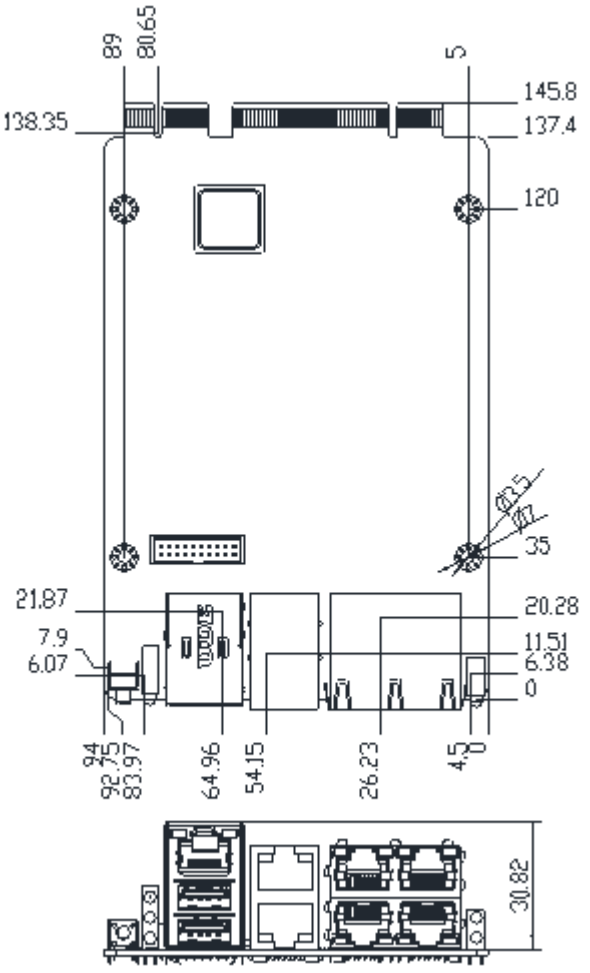
89.85
97.95
108.7
139.63
152
189.8
211.1
249.4
20.95
2.95


12.15 +0.1 -0.1
7.2.15 +0.1 -0.1
R0.95
C0.5
2-Ø6
2-Ø3.1
4-Ø2
R0.95
C0.5
Ø0.8
2-Ø6
2-Ø3.1

PER-T393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145.8
138.35
137.4
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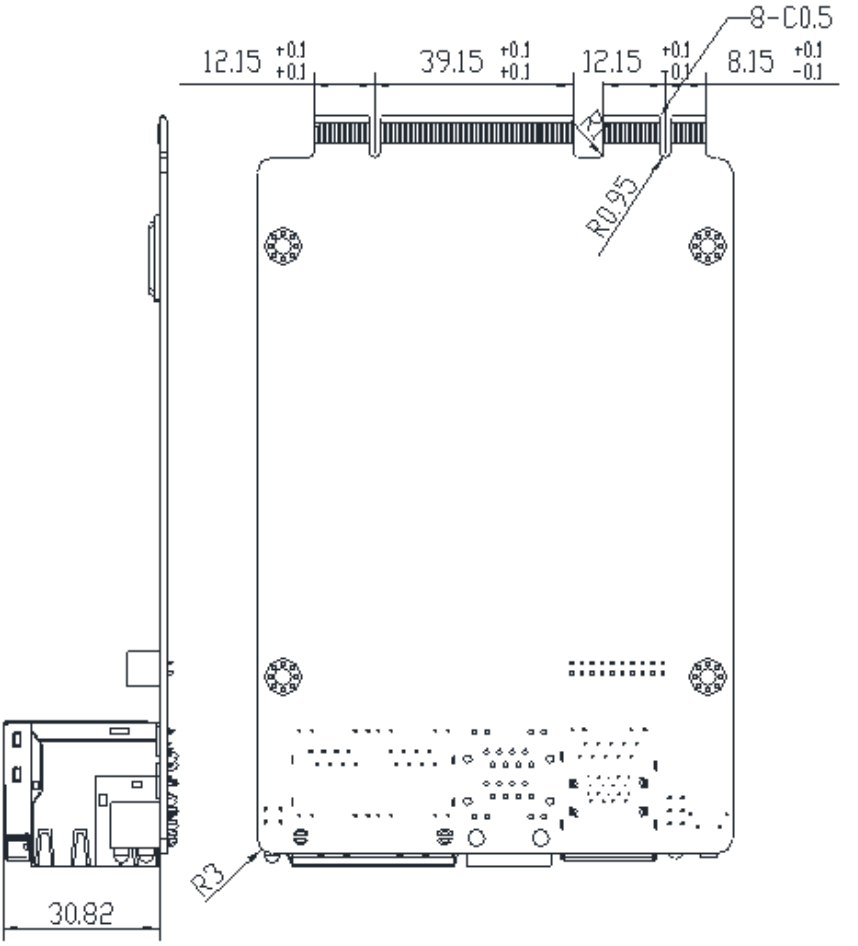
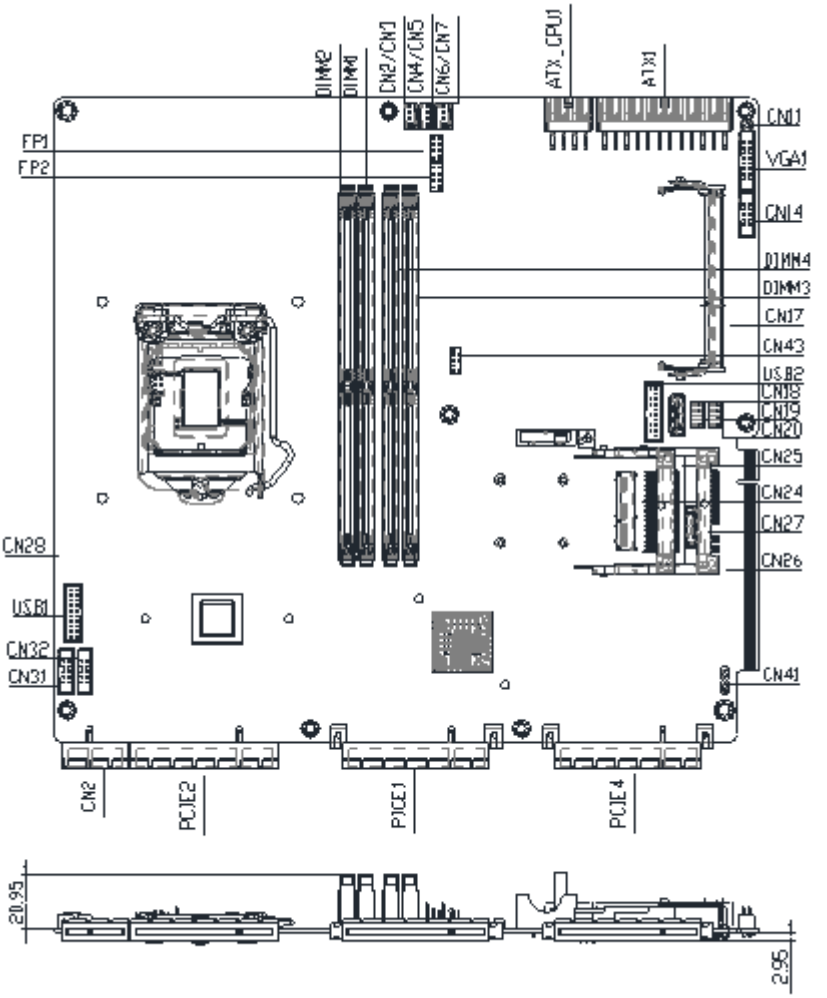
Ø2.5
Ø2
35
21.87
20.28
7.9
6.07
11.51
6.38
0
94
92.75
83.97
64.96
54.15
26.23
4.5
0
30.82

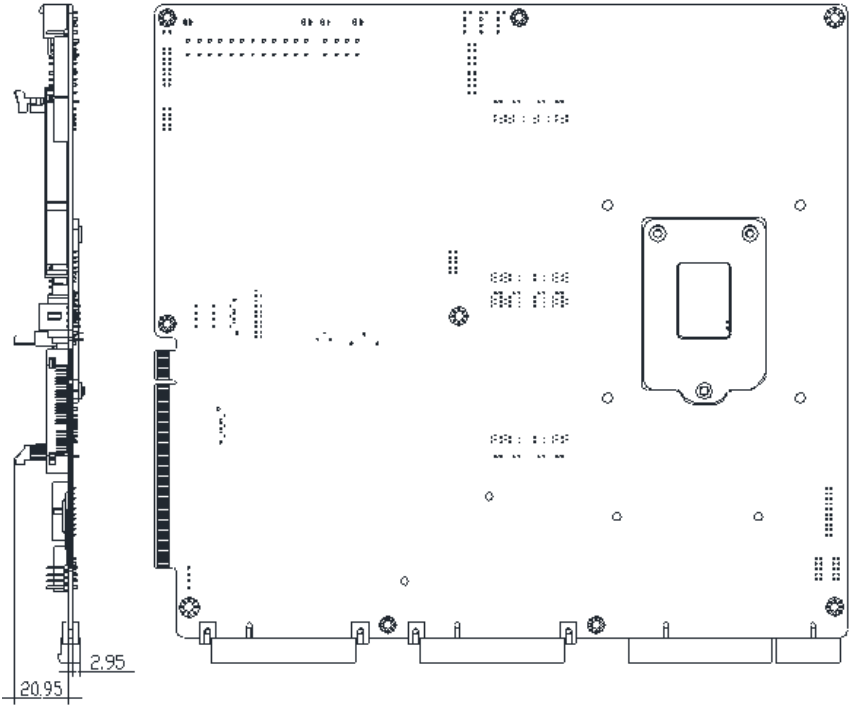

8-C0.5
12.15 +0.1 +0.1
39.15 +0.1 +0.1
12.15 +0.1 -0.1
8.15 +0.1 -0.1
R0.95
R3
30.82

2.2 Jumpers and Connectors

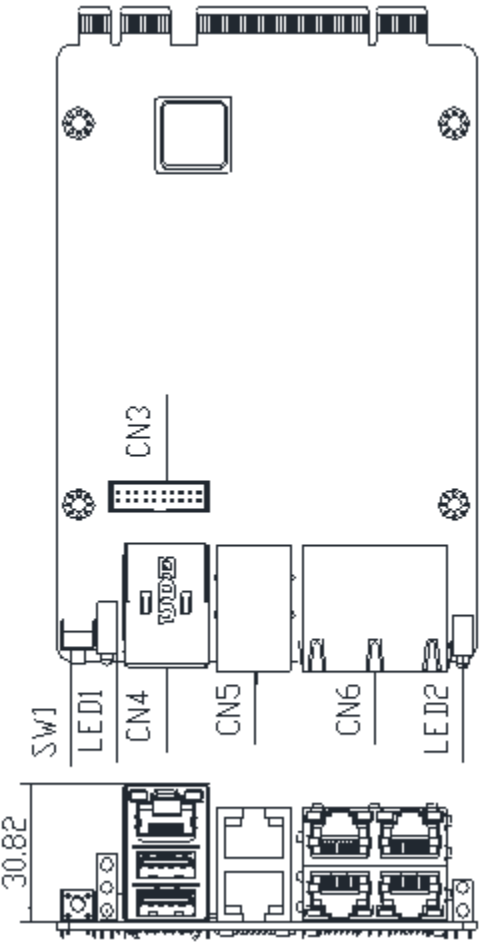
Component Side

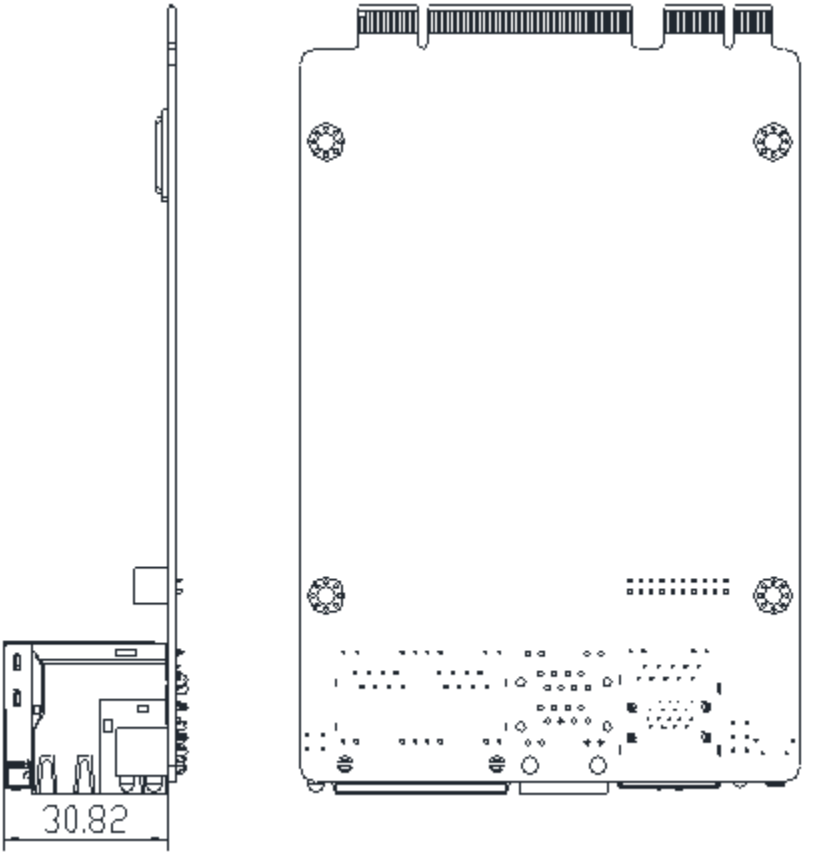


Solder Side



PER-T393



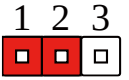

30.82

2.3 List of Jumpers

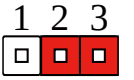
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN40	RTC Reset
CN39	Secondary RTC Reset
CN23	CF Power Selection
JP1	Auto Power Button

2.3.1 RTC Reset (CN40)

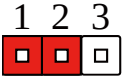


Normal (Default)

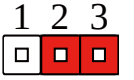


Clear CMOS

2.3.2 Secondary RTC Reset (CN39)

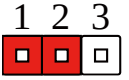


Normal (Default)

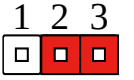


RTC TEST

2.3.3 Auto Power Button Selection (CN23)

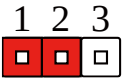


Don't use Auto PWRBTN (Default)

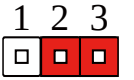


Use Auto PWRBTN

2.3.4 CFD Voltage 3.3/5V Selection (JP1)



+3.3 V (Default)



+5 V

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
ATX_CPU1	8-Pin 12V Power Connector
ATX1	24-Pin ATX Power Connector
CN1	PS/2 keyboard & Mouse Connector
CPU_FAN1	CPU_FAN1
CPU_FAN2	CPU_FAN2
SYS_FAN1	SYS_FAN1
CN11	Power button
CN12	PCIE Slot For FWS-7820 Pin Define
CN14	COM Port
CN17	LCM Connector
CN18&CN27	SATA Port Connector
CN19& CN20	HDD Power Connector
CN22	LPC Connector
CN24	Compact Flash SOCKET
CN25	mSATA SOCKET
CN26	CFAST SOCKET
CN28	HDMI Connector
CN30	CPLD Programming Pin Header
CN33	Battery Pin Header
CN41	Key PAD Connector
CN43	Digital I/O
DIMM1	Channel A DDR4 U-DIMM

DIMM2	Channel A DDR4 U-DIMM
DIMM3	Channel B DDR4 U-DIMM
DIMM4	Channel B DDR4 U-DIMM
FP1	Front Panel Pin Header
FP2	Front Panel Pin Header
PCIE1	NIM Card Connector
PCIE2	NIM Card Connector
PCIE4	NIM Card Connector
USB1& USB2	USB3.0 Port
VGA1	VGA Port

2.4.1 Digital I/O: 2.0mm Pin Header 2 x 5P (CN43)

Pin	Signal	Signal Type
1	DIO0	Input / Output
2	DIO1	Input / Output
3	DIO2	Input / Output
4	DIO3	Input / Output
5	DIO4	Input / Output
6	DIO5	Input / Output
7	DIO6	Input / Output
8	DIO7	Input / Output
9	+3.3V	PWR
10	GND	GND

2.4.2 LCM Connector: 1.0mm FPC 1 x 16P (CN17)

Pin	Signal	Signal Type
1	LCMGND	GND
2	LCMVCC	PWR
3	VEE	PWR
4	SLIN#	Output
5	INIT#	Output
6	AFD#	Output
7	DATA0	Input / Output
8	DATA1	Input / Output
9	DATA2	Input / Output
10	DATA3	Input / Output

11	DATA4	Input / Output
12	DATA5	Input / Output
13	DATA6	Input / Output
14	DATA7	Input / Output
15	+5V	PWR
16	LCD#	Output

2.4.3 Key PAD Connector: 2.54mm Pin Header 1 x 4P (CN41)

Pin	Signal	Signal Type
1	KEY PAD Down	Input
2	KEY PAD Up	Input
3	KEY PAD Right	Input
4	KEY PAD Left	Input

2.4.4 COM Port: 2.0mm BOX Header 2 x 5P (CN14)

RS232

Pin	Signal	Signal Type
1	DCD	Input
2	RXD	Input
3	TXD	Output
4	DTR	Output
5	GND	GND
6	DSR	Input
7	RTS	Output
8	CTS	Input

9	RI / +5V / +12V	Input / PWR
10	N.C.	

2.4.5 VGA Port: 2.0mm Box Header (VGA1)

Pin	Signal	Signal Type
1	Red	Output
2	+5V_CRT	PWR
3	Green	Output
4	GND	GND
5	Blue	Output
6	CRT_PLUG#	Input
7	NC.	
8	DDC_DATA	Input / Output
9	GND	GND
10	CRT_OHSYNCF	Output
11	GND	GND
12	CRT_OVSYNCF	Output
13	GND	GND
14	DDC_CLK	Input / Output
15	GND	GND
16	NC	

2.4.6 HDD Power Connector: 2.5mm Wafer 1 x 4P (CN19 & CN20)

Pin	Signal	Signal Type
1	+12V	PWR

2	GND	GND
3	GND	GND
4	+5V	PWR

2.4.7 USB 3.0 Port: 2.0mm Box Header 2 x 10P (USB1 & USB2)

Pin	Signal	Signal Type
1	+5V_USB	PWR
2	USB3_RX1_DN	DIFF
3	USB3_RX1_DP	DIFF
4	GND	GND
5	USB3_TX1_DN	DIFF
6	USB3_TX1_DP	DIFF
7	GND	GND
8	USBP_0N	DIFF
9	USBP_0P	DIFF
10	NC	
11	USBP_1P	DIFF
12	USBP_1N	DIFF
13	GND	GND
14	USB3_TX2_DP	DIFF
15	USB3_TX2_DN	DIFF
16	GND	GND
17	USB3_RX2_DP	DIFF
18	USB3_RX2_DN	DIFF
19	+5V_USB	PWR
20	NC	

2.4.8 PS/2 Keyboard & Mouse Connector: 2.54mm Pin Header 2 x 4P (CN1)

Pin	Signal	Signal Type
1	KB_DATA	Input / Output
2	KB_CLK	Output
3	GND	GND
4	+5V_KB	PWR
5	MS_DATA	Input / Output
6	MS_CLK	Output
7	NC	
8	Key	

2.4.9 Front Panel Pin Header (FP1)

Pin	Signal	Signal Type
1	External Speaker (+)	Output
2	Key Board Lock (+)	Output
3	NC	Floting
4	GND	POWER
5	External Speaker (-)	Output
6	I2C Bus SMB Clock	Input / Output
7	External Speaker (-)	Output
8	I2C Bus SMB Data	Input / Output

2.4.10Front Panel Pin Header (FP2)

Pin	Signal	Signal Type
1	Power On Button(+)	Input
2	Reset Switch (+)	Input
3	Power On Button(-)	POWER
4	Reset Switch (-)	POWER
5	HDD LED (+)	POWER
6	Power LED(+)	POWER
7	HDD LED (-)	Output
8	Power LED(-)	Output

2.4.11 LPC Connector: 1.0mm Box Wafer 1 x 12P (CN22)

Pin	Signal	Signal Type
1	LAD0	Input / Output
2	LAD1	Input / Output
3	LAD2	Input / Output
4	LAD3	Input / Output
5	+3.3V	PWR
6	LFRAME#	Input
7	LREST##	Output
8	GND	GND
9	LCLK	Output
10	LDRQ0	Input
11	LDRQ1	Input
12	SERIRQ	Input / Output

2.5 PER-T393 Front Panel Jumpers and Connectors List

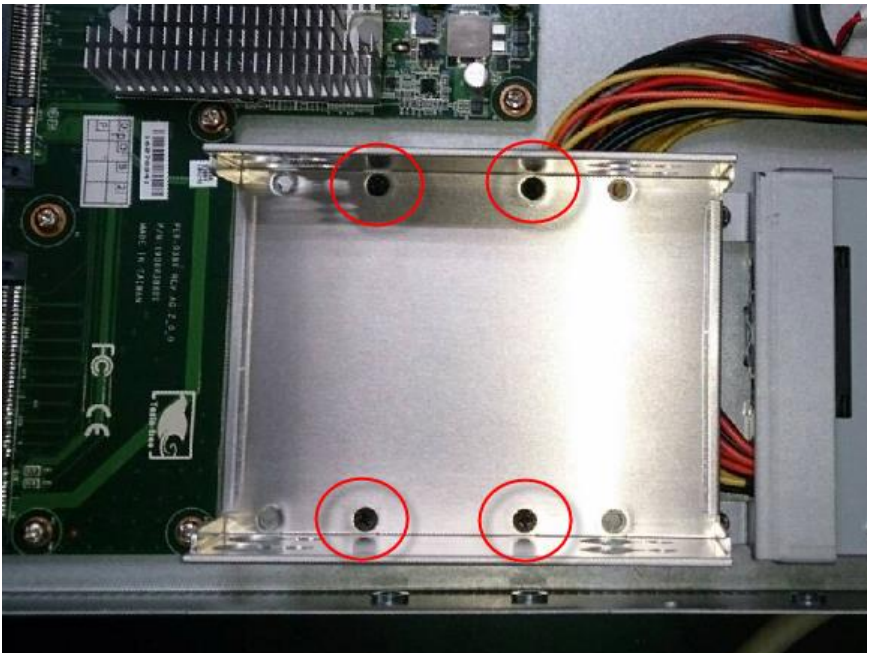
Label	Function
SW1	Software Reset
LED1	POWER+STATE+HDD LED Instruction
CN4	COMSOLE+ 2PORT USB3.0
CN5	2PORT RJ45 Management LAN PORT
CN6	4PORT RJ45 LAN PORT
LED2	BYPASS LED Instruction

2.6 Installing 2.5" Hard Disk Drives (2 pieces)

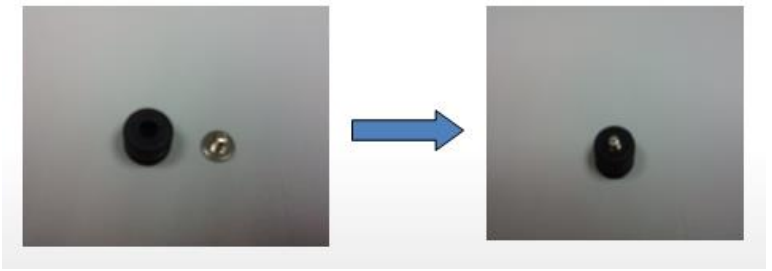
1. Remove the highlighted screws

2. From the front of the system, slide it upwards to remove

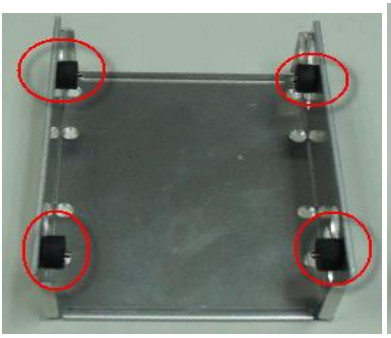
3. Remove the four highlighted screws to remove the HDD bracket

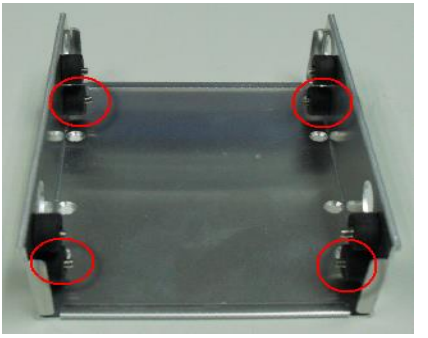


4. Put the provided screws (not the ones from step 3) into cushions

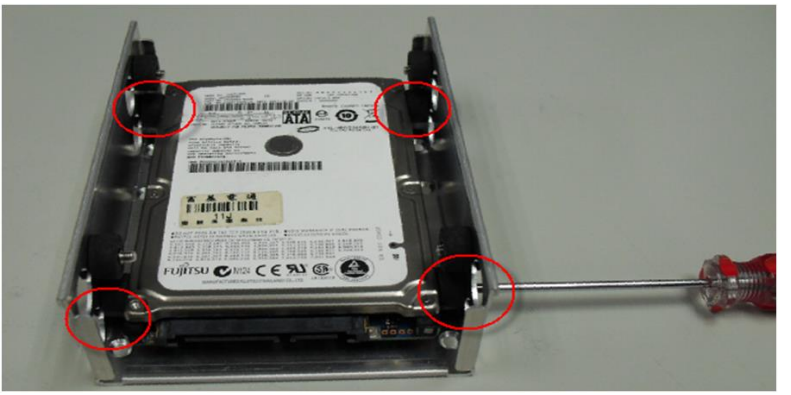


5. Attach the assembled screws to the top and bottom of the inside of the bracket

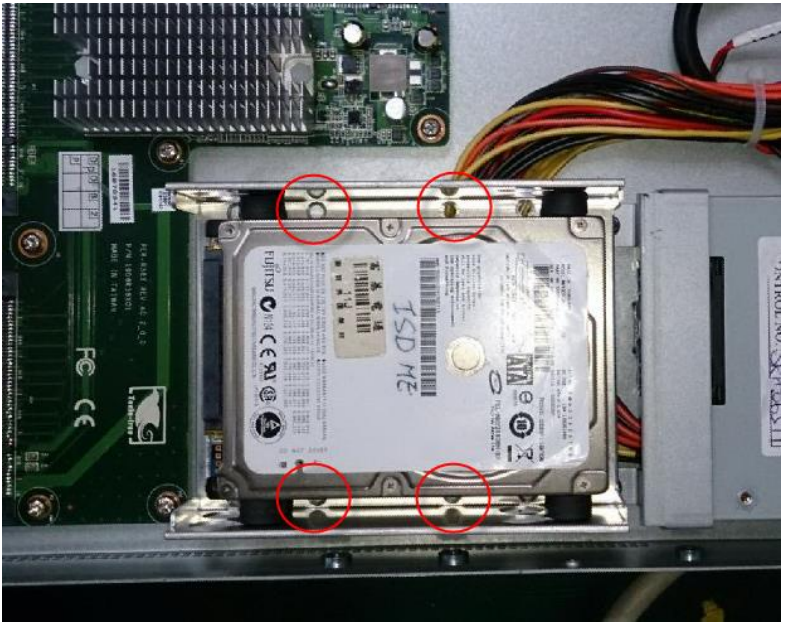


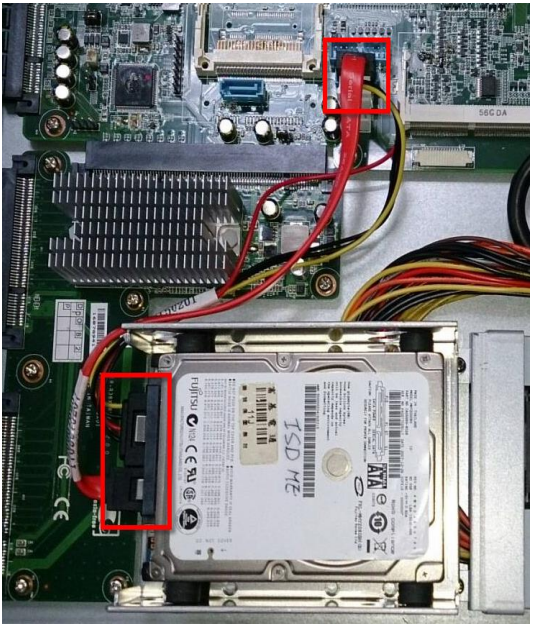


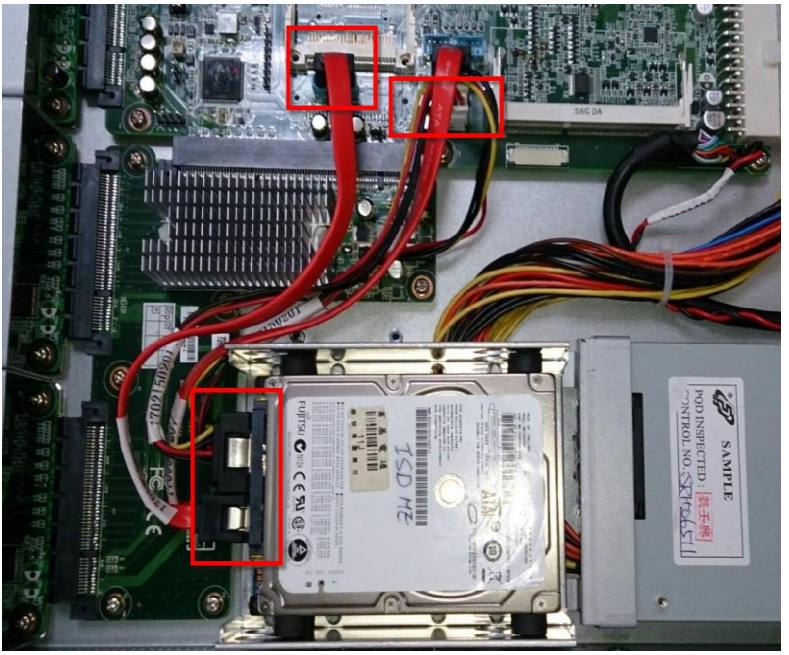
6. Place the HDDs into the bracket, tighten the screws to secure



7. Place the assembled HDDs back into the system, secure with screws and reattach the SATA and power cables.





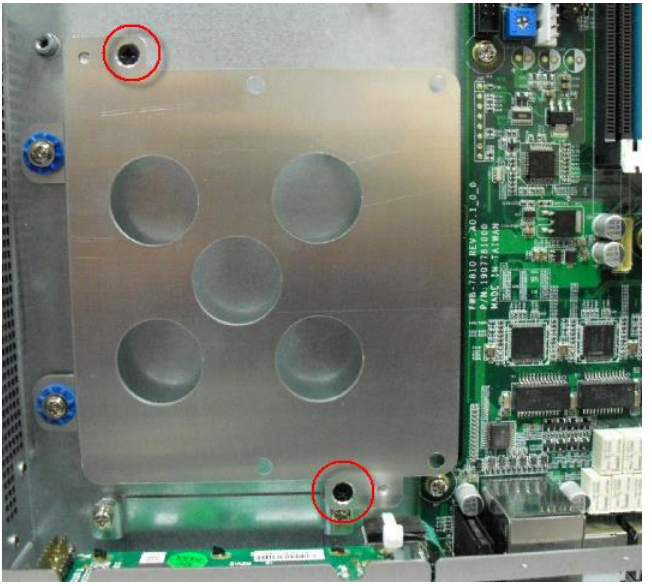

SAMPLE
FUJITSU

2.7 Installing 3.5" Hard Disk

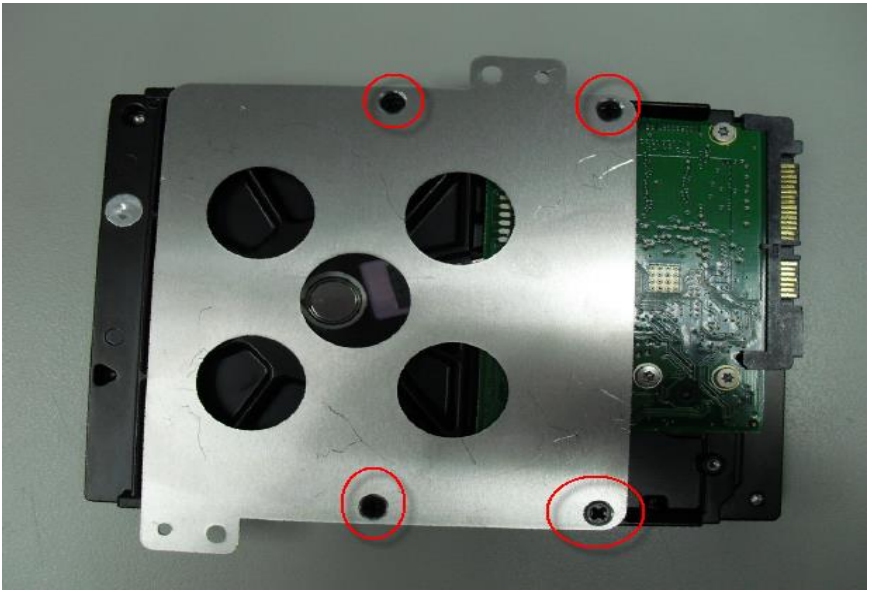
1. Remove the highlighted screws

2. From the front of the system, slide it upwards to remove

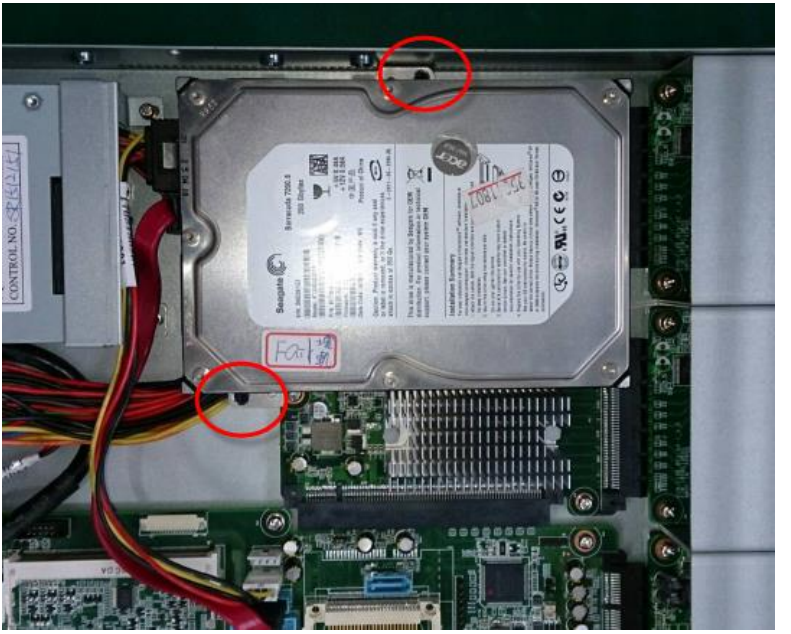
3. Remove the screws to remove the bracket



4. Place the 3.5" HDD on the bracket, secure with screws on the underside

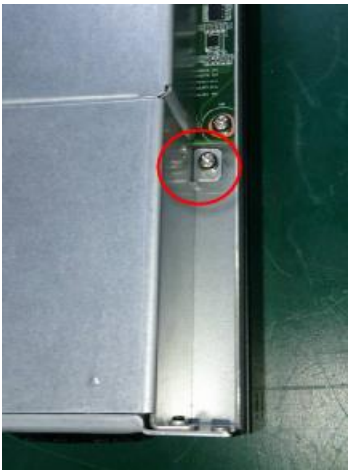


5. Put the assembled HDD on the HDD bay, secure with screws and reattach the SATA and power cables

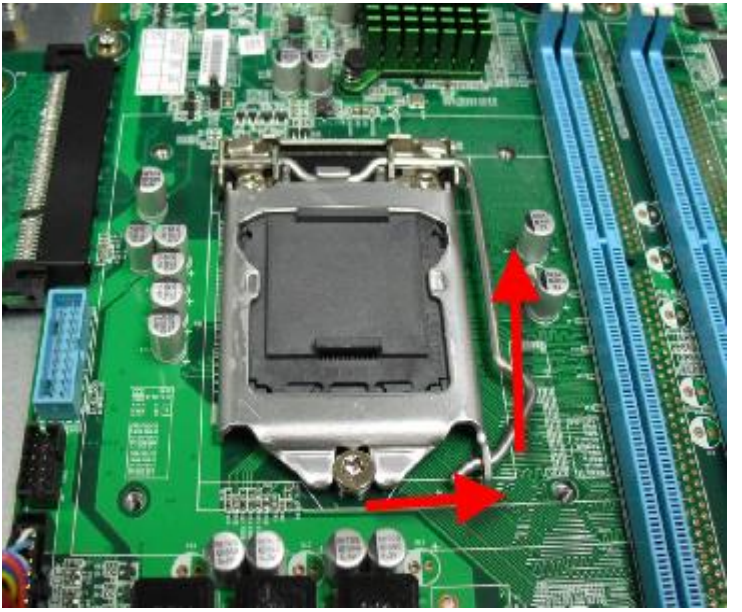


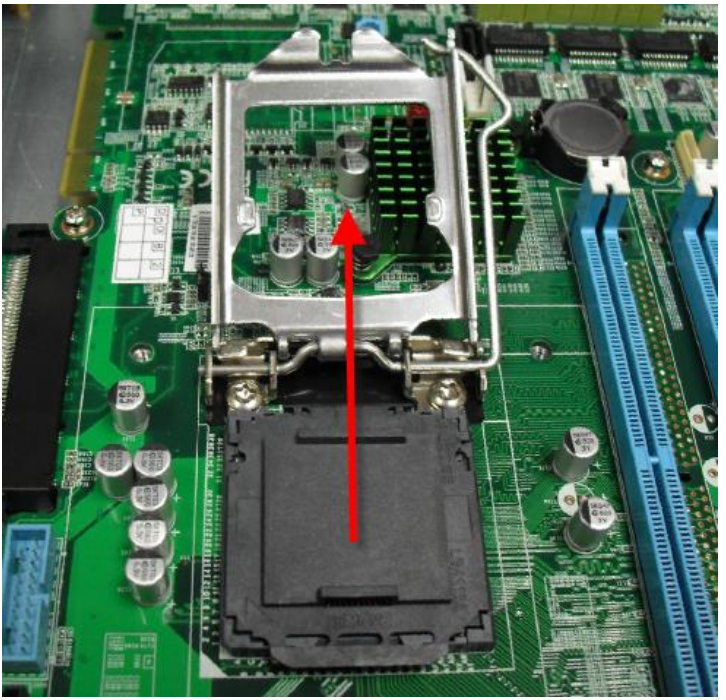
2.8 Installing CPU and Heat Sink

1. Remove the highlighted screws to remove the fan duct

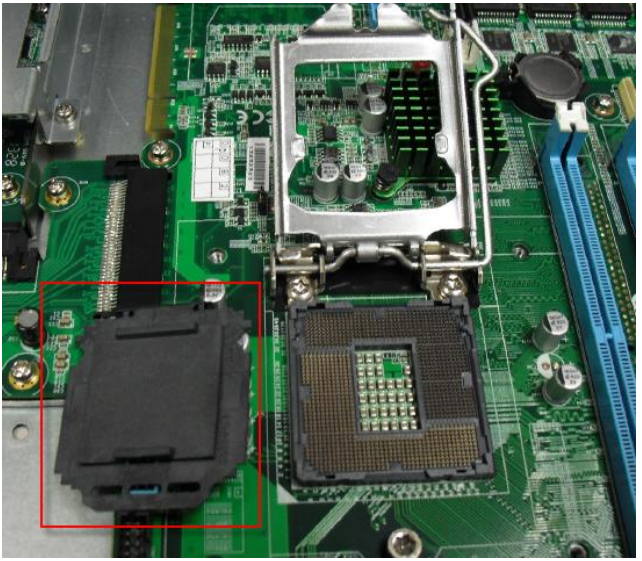


2. Lift the socket arm up to open the CPU socket

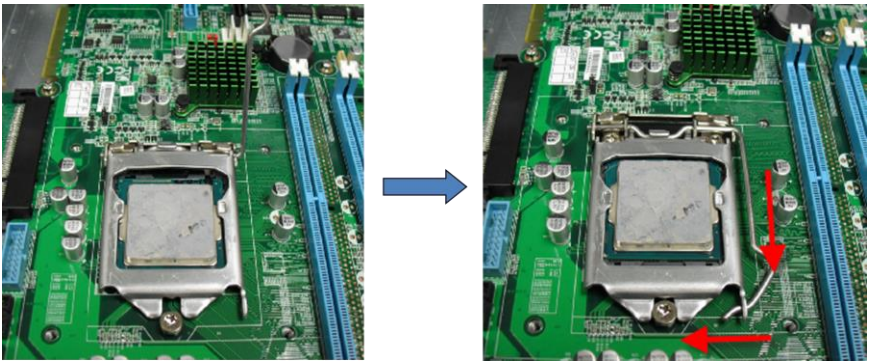




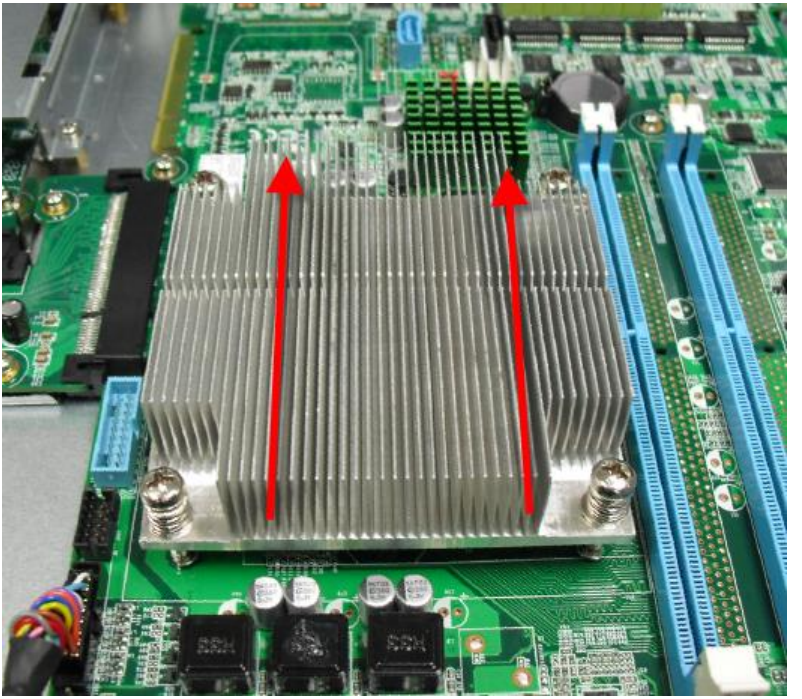
3. Remove the cover and place the CPU into the socket. Make sure the two fillisters are properly locked.



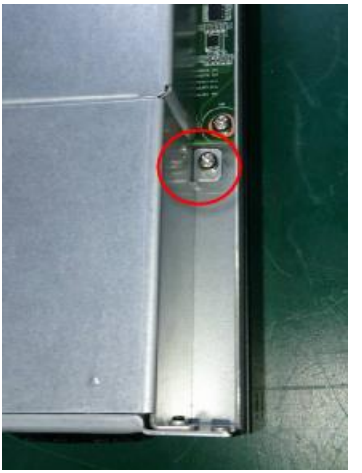
4. Push the arm down to lock the CPU into place



5. Place the heat sink onto the CPU. Make sure the direction of the heat sink is not against the airflow



6. Close the air duct and secure with screws

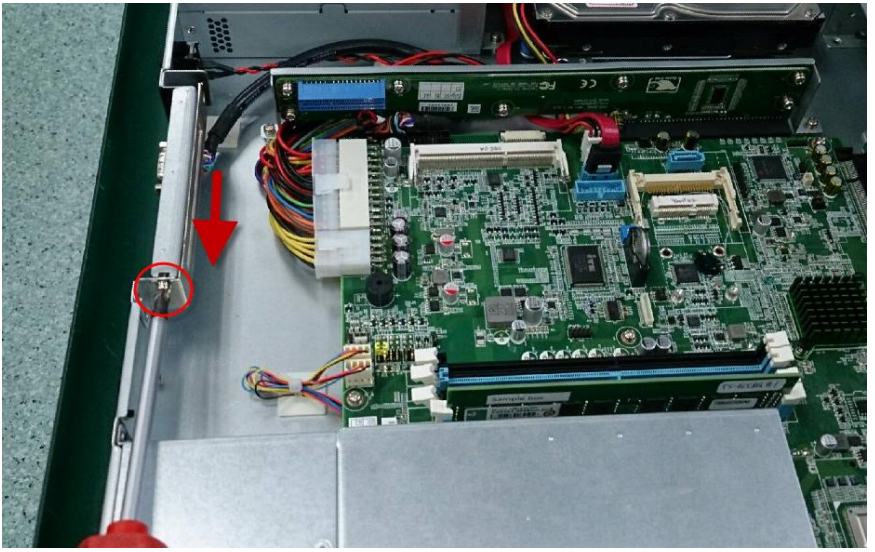


2.9 Installing Expansion Card

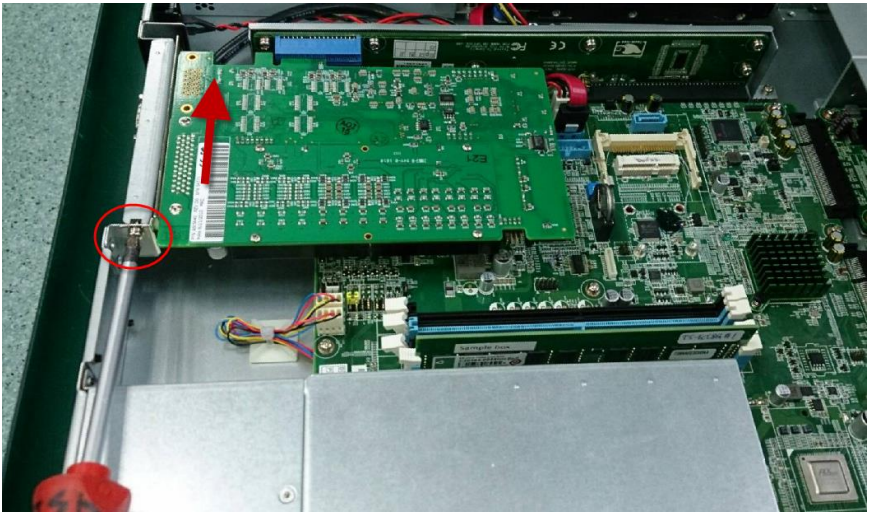
1. Remove the highlighted screws

2. From the front of the system, slide it upwards to remove

3. Remove the screw to remove the cover bracket



4. Firmly insert the expansion card into the slot and secure the screw.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Advanced setup parameters

Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

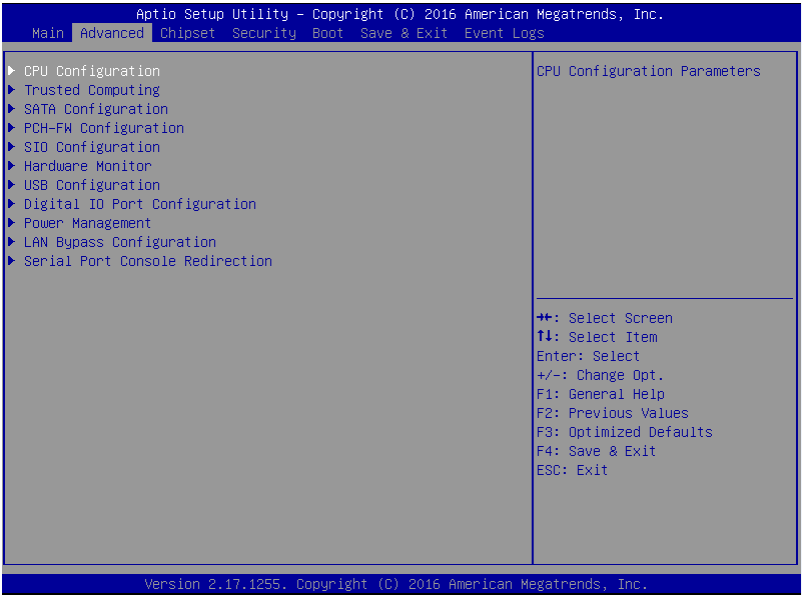
Boot – Enable/ Disable quiet Boot Option

Save & Exit –Save your changes and exit the program

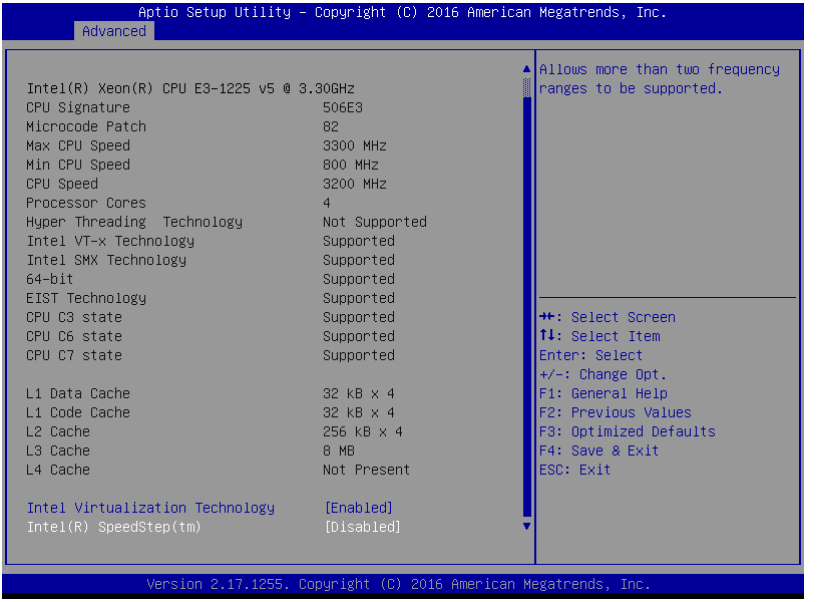
Event Logs – Smbios Event Log configuration

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



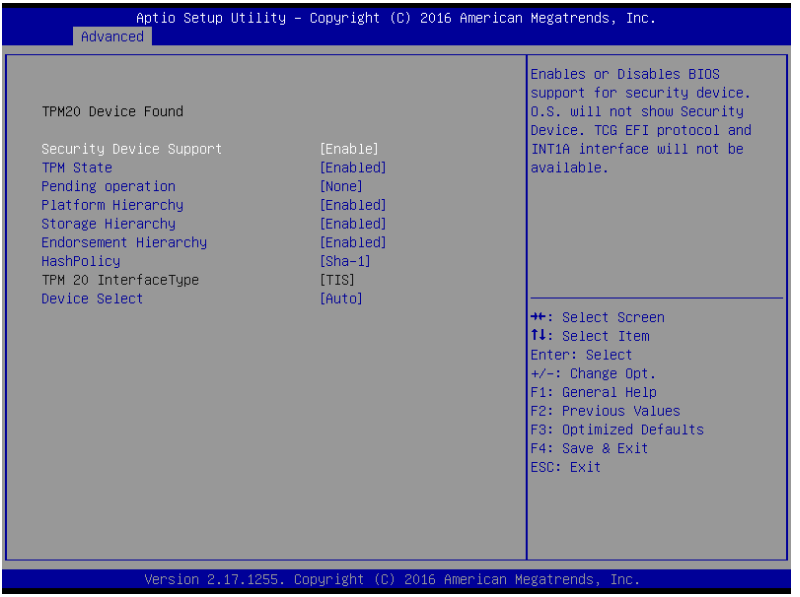
3.4.1 Advanced: CPU Configuration



Options summary:

Intel Virtualization Technology	Disabled	Default
	Enabled	
En/Disable CPU Virtualization Technology function		
Intel(R) SpeedStep(tm)	Disabled	Default
	Enabled	
When enabled, OS sets CPU frequency according load. When disabled, CPU frequency is set at max non-turbo.		

3.4.2 Advanced: Trusted Computing

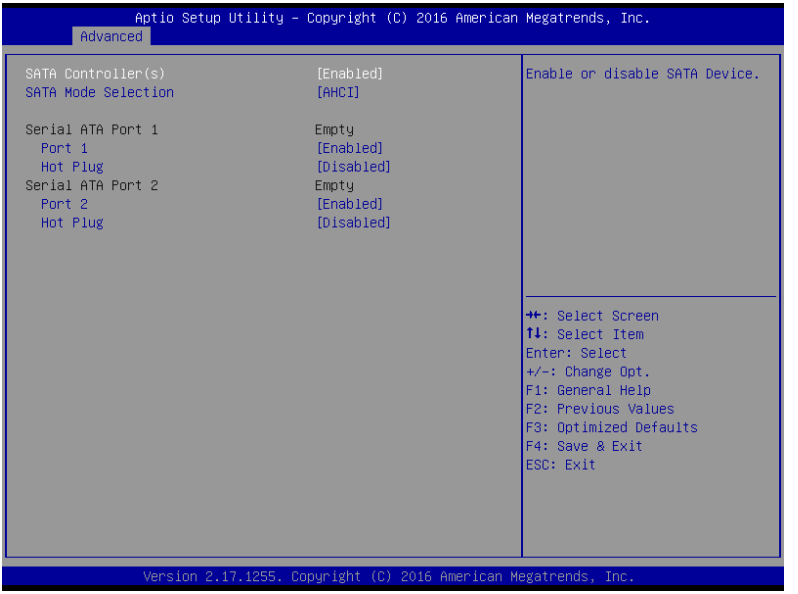


Options summary:

Security Device Support	Disable	
	Enable	Default
Enable or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
TPM State	Disable	
	Enable	Default
Enable or Disables security device.		
Pending operation	None	Default
	TPM clear	
Schedule an Operation for the Security Device.		
Platform Hierarchy	Disable	

	Enable	Default
Enable or Disables Platform Hierarchy.		
Storage Hierarchy	Disable	
	Enable	Default
Enable or Disables Storage Hierarchy.		

3.4.3 Advanced: SATA Configuration

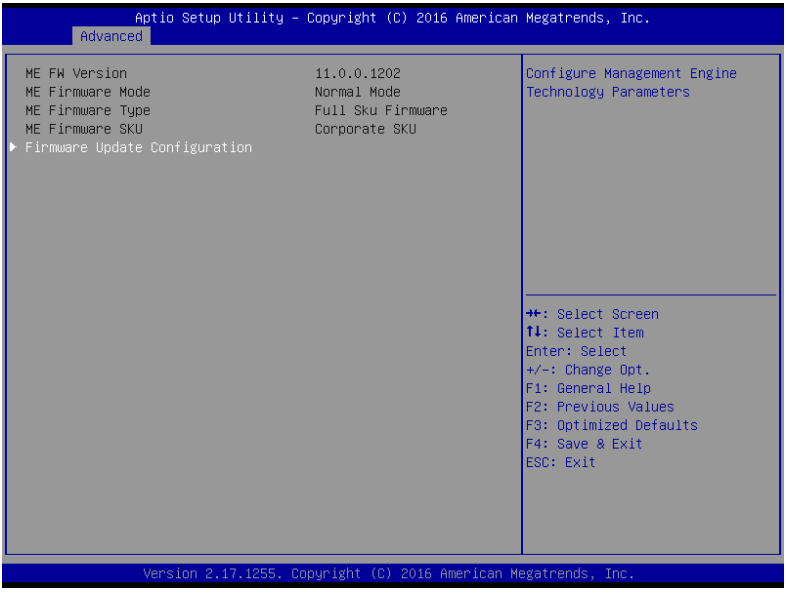


Options summary:

SATA Controllers	Disabled	
	Enabled	Default
En/Disable SATA Controller.		
SATA Mode Selection	AHCI	Default
	RAID	

AHCI: Configure SATA controllers to operate in AHCI mode		
Port	Disabled	
	Enabled	Default
En/Disable Port.		
Hot Plug	Disabled	Default
	Enabled	
En/Disable Hot Plug function		

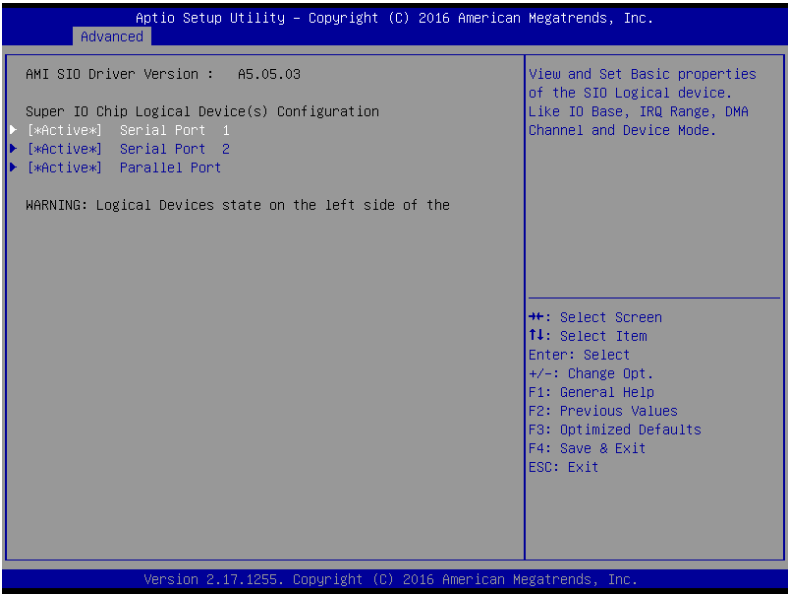
3.4.4 Advanced: PCH-FW Configuration



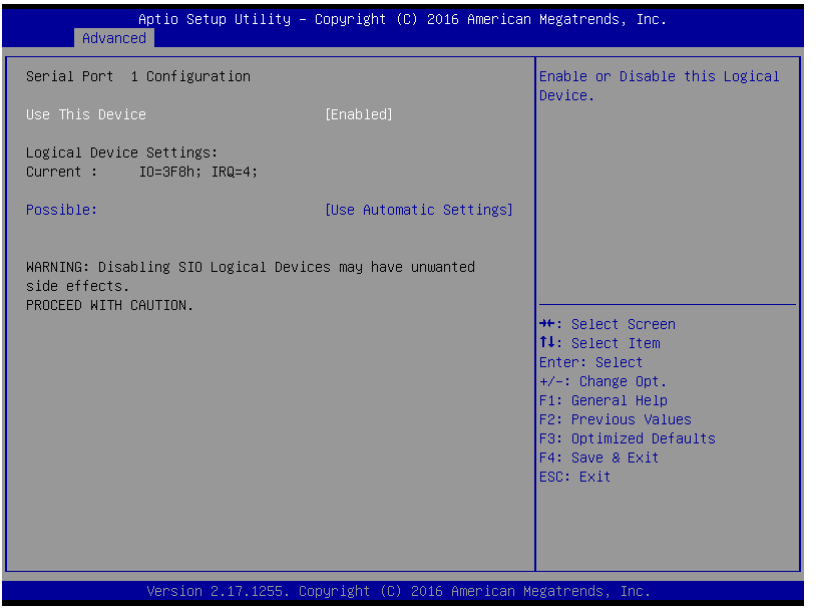
Options summary:

Firmware Update Configuration	Disabled	Default
	Enabled	
Enable/Disable Me FW image Re-Flash function.		

3.4.5 Advanced: SIO Configuration



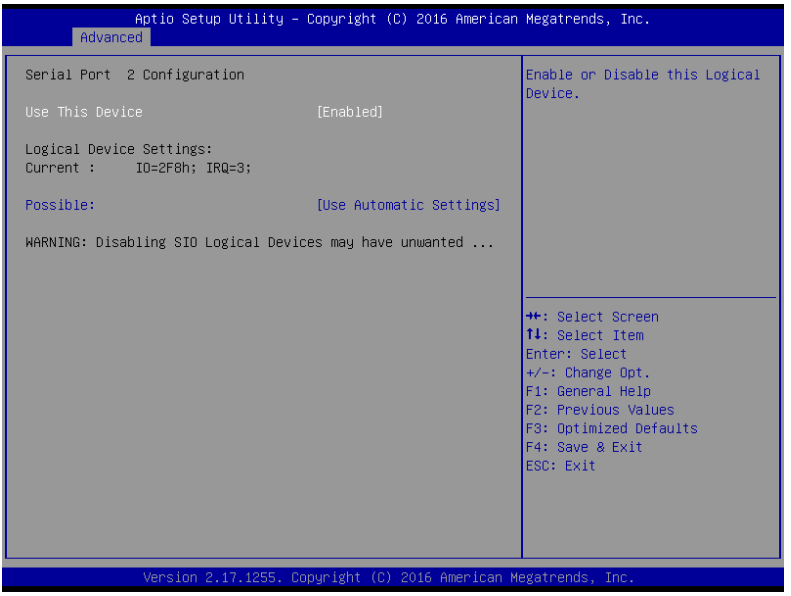
3.4.5.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Default
Enable or Disable this Logical Device.		
Possible:		
Change Settings	Auto	Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

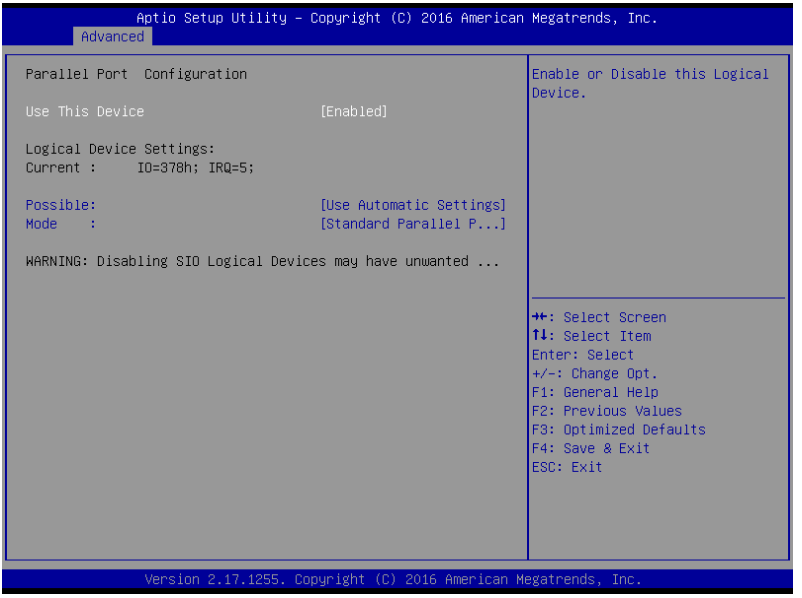
3.4.5.2 SIO Configuration: Serial Port 2 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Default
Enable or Disable this Logical Device.		
Possible:		
Change Settings	Auto	Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

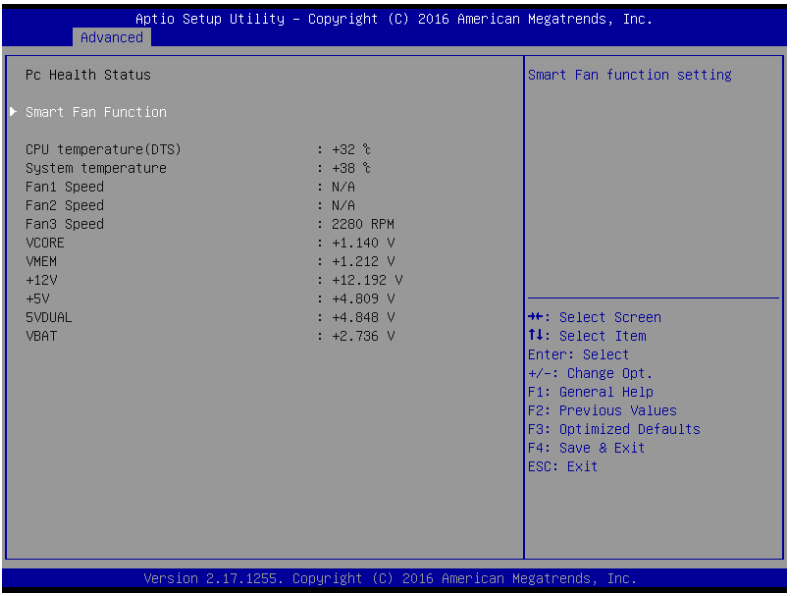
3.4.5.3 SIO Configuration: Parallel Port Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Default
Enable or Disable this Logical Device.		
Possible: (Parallel Port)	Auto	Default
	IO=378h; IRQ=5;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	SPP Mode	Default
	EPP Mode	
	ECP Mode	
	ECP mode & ECP mode	
Change the Printer Port mode.		

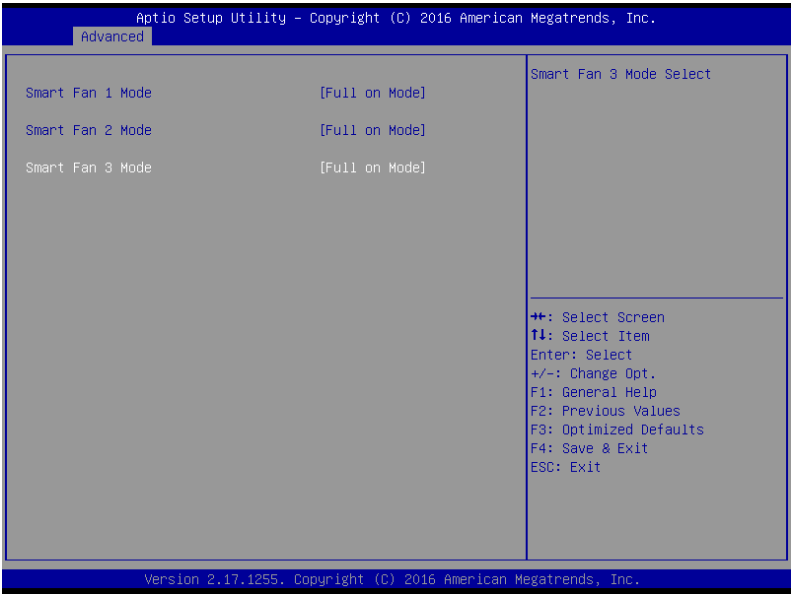
3.4.6 Advanced: Hardware Monitor



Options summary:

CPU Fan 1 Smart Control	Disabled	
	Enabled	Default
Allows BIOS to En/Disable CPU Fan 1 Smart Control		
CPU Fan 2 Smart Control	Disabled	
	Enabled	Default
Allows BIOS to En/Disable CPU Fan 2 Smart Control		
SYS Fan 1 Smart Control	Disabled	
	Enabled	Default
Allows BIOS to En/Disable System Fan 1 Smart Control		

3.4.6.1 Hardware Monitor: Smart Fan Function (Full on Mode)



Options summary:

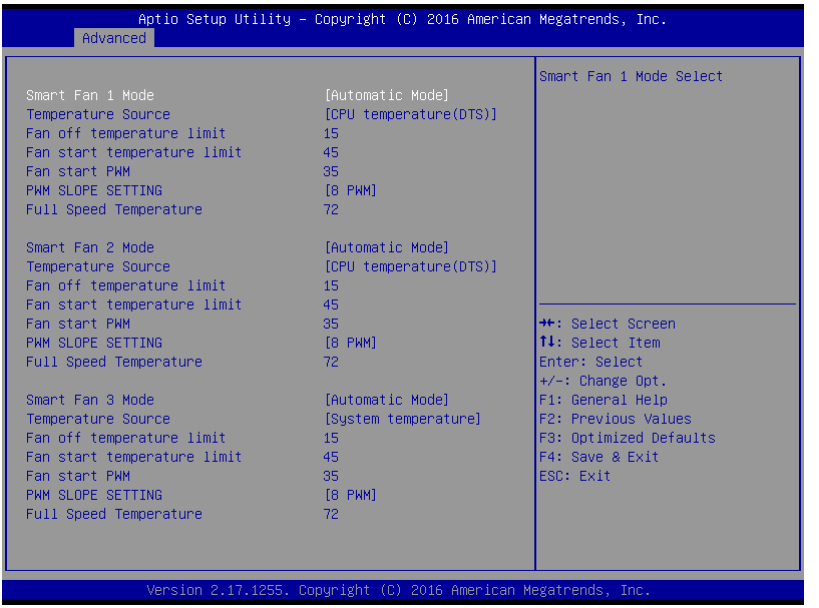
Smart Fan Mode	Full on Mode	Default
	Automatic Mode	
	Manual Mode	
Full on Mode: Always on. Manual Mode: Depends on PWM Duty. Automatic Mode: FAN Speed is depends on CPU Temperature.		

3.4.6.2 Hardware Monitor: Smart Fan Function (Manual Mode)

Options summary:

Smart Fan Mode	Full on Mode	Default
	Automatic Mode	
	Manual Mode	
Full on Mode: Always on. Manual Mode: Depends on PWM Duty. Automatic Mode: FAN Speed is depends on CPU Temperature.		
Manual PWM Setting	0 – 255	Default (35)
Manual Mode PWM Duty value Range:[0 - 255]		

3.4.6.3 Hardware Monitor: Smart Fan Function (Automatic Mode)



Options summary:

FAN Control Mode	Full on Mode	Default
	Automatic Mode	
	Manual Mode	
Smart Fan Mode Select.		
Temperature Source	CPU temperature	Default
	System temperature	
Select temperature Source.		
Fan off temperature limit	0 ~ 127	Default (15)
Temperature Limit Value of Fan Off. Note: Some fans have the minimum speed even if the PWM value is 0		
Fan start temperature limit	0 ~ 127	Default (45)
Temperature Limit Value of FAN Start Control		

Fan start PWM	0 ~ 255	Default (35)
Fan will start with this PWM value.		
PWM SLOPE SETTING	0 ~ 15	Default (8)
PWM SLOPE Selection		
Full Speed Temperature	0 ~ 127	Default (72)
Temperature Limit Value of FAN Full Speed		

3.4.7 Advanced: USB Configuration

Options summary:

Legacy USB Support	Enabled	Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		

3.4.8 Advanced: Digital IO Port Configuration

Options summary:

DIO_P#1~4	Input	
	Output	Default
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#5~8	Input	Default
	Output	
Allows BIOS to select input/output function to corresponding DIO ping.		
DIO_P#1~4 Direction	Low	
	Hi	Default
Allows BIOS to select high/low voltage level to output to corresponding DIO ping.		

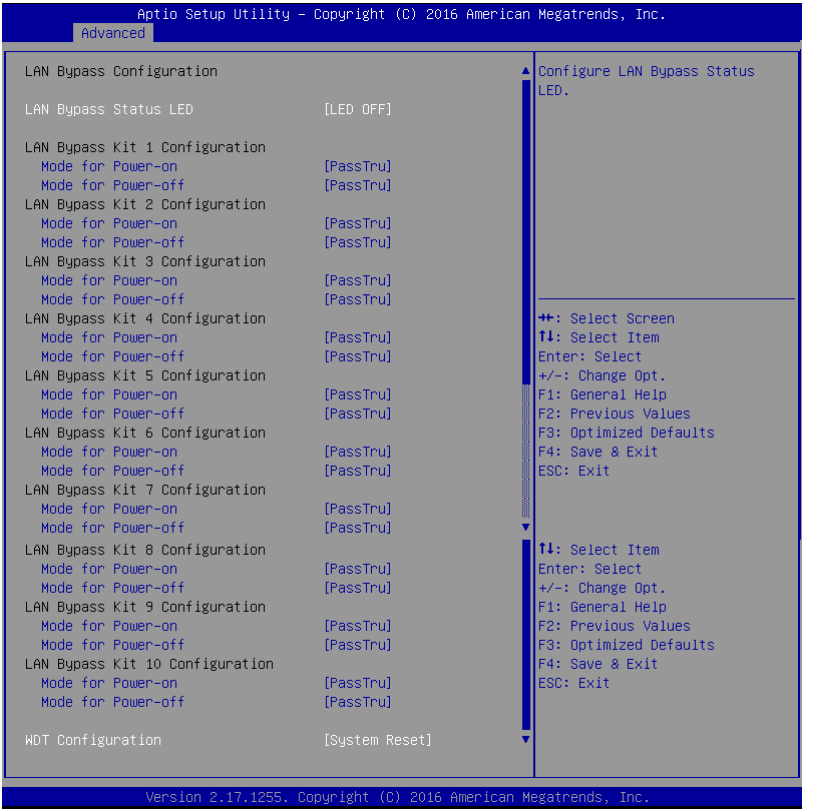
3.4.9 Advanced: Power Management

Options summary:

Power Mode	ATX Type	Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	Default
	Always on	
	Always off	
RTC wake system from S5	Disabled	Default
	Fixed Time	
	Dynamic Time	

Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)

3.4.10Advanced: LAN Bypass Configuration



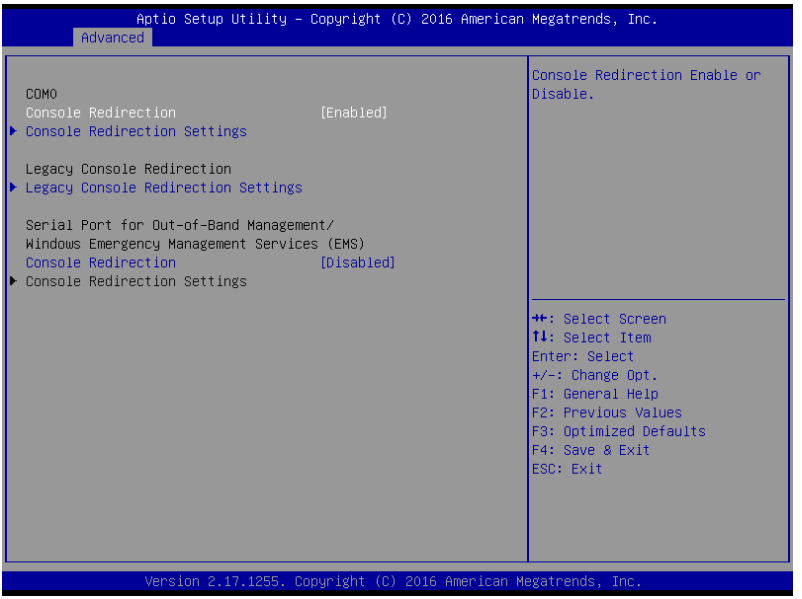
Options summary:

LAN Bypass Status LED Configuration	LED OFF	Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	

	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
Select LAN Bypass Status LED Configuration.		

LAN Bypass Kit Configuration		
Mode for power-on	PassTru	Default
	Bypass	
Mode for power-off	PassTru	Default
	Bypass	
Select LAN Bypass Kit Configuration.		
WDT Configuration	Force Bypass	
	System Reset	Default
Select WDT Configuration.		

3.4.11 Advanced: Serial Port Console Redirection



Options Summary:

Console Redirection	Enabled	Default
	Disabled	
Console Redirection Enable or Disable.		
Legacy Console Redirection	Com0	Default
Select Legacy Console Redirection port		
Console Redirection(EMS)	Enabled	
	Disabled	Default
Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.		

3.4.11.1 Serial Port Console Redirection: COM0 Console Redirection Settings

Options summary:

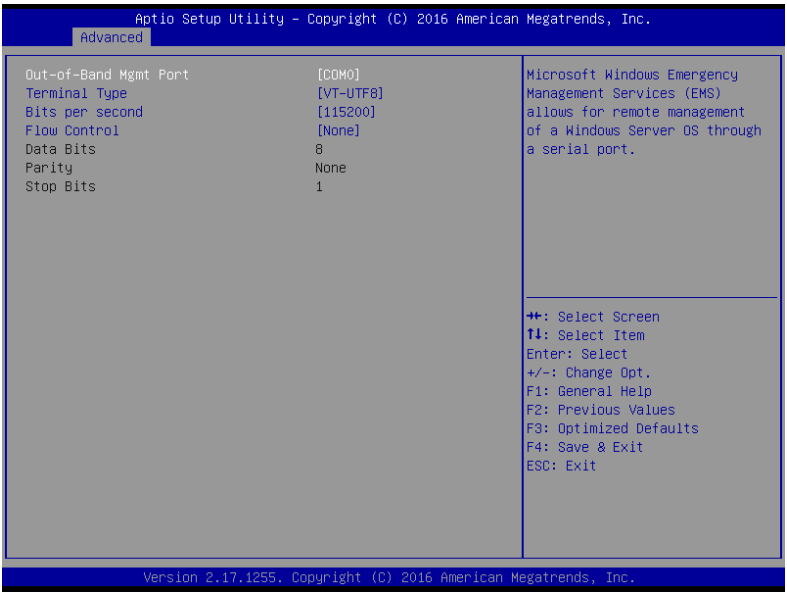
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Default
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Default

Data Bits	7	
	8	Default

Parity	None	Default
	Even	
	Odd	
	Mark	
	Space	
Stop Bits	1	Default
	2	
Flow Control	None	Default
	Hardware RTS/CTS	
VT-UTF8 Combo Key Support	Enabled	Default
	Disabled	
Recorder Mode	Enabled	
	Disabled	Default
Resolution 100x31	Enabled	
	Disabled	Default
Legacy OS Redirection Resolution	80x24	Default
	80x25	

Putty Keypad	VT100	Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Redirection After BIOS POST	Always Enabe	Default
	BootLoader	

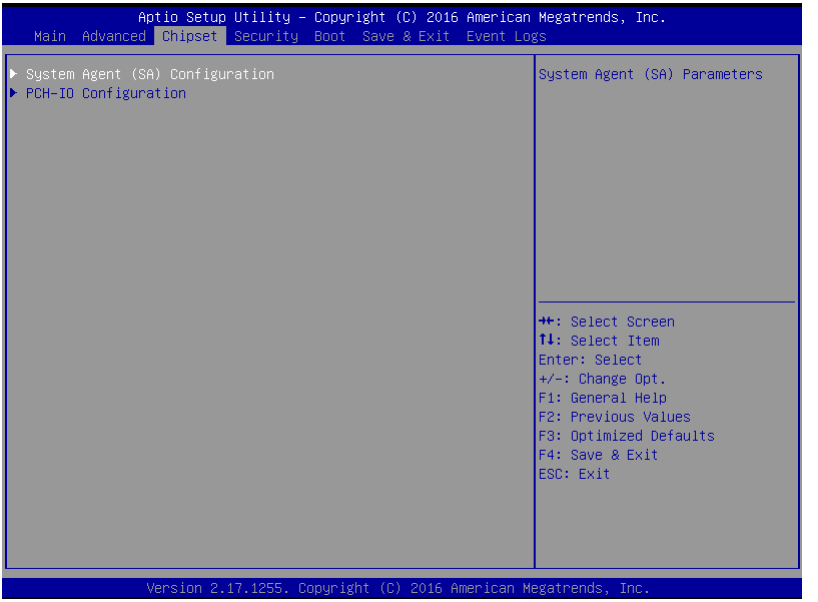
3.4.11.2 Serial Port Console Redirection: Console Redirection Settings



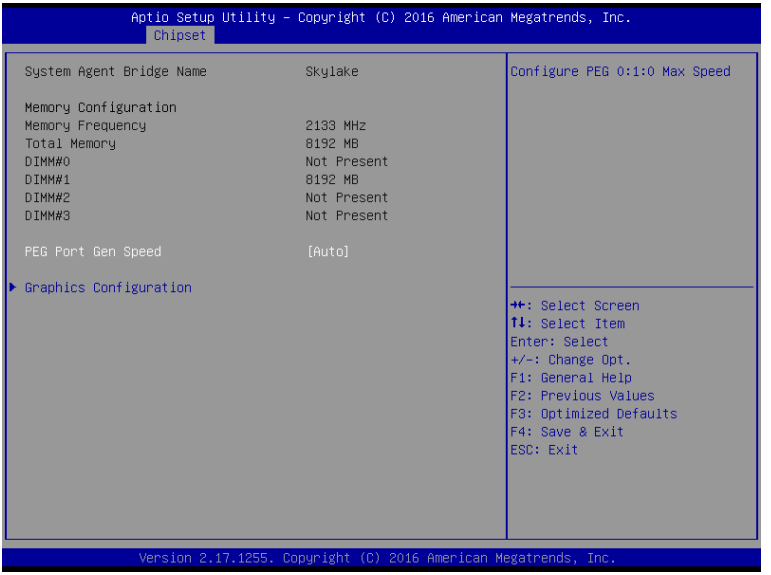
Options Summary:

Out-of-Band Mgmt Port	COM0	Default
	COM1	
Terminal Type	VT100	
	VT100+	
	VT-UTF8	Default
	ANSI	
Bits per second	9600	
	19200	
	57600	
	115200	Default
Flow Control	None	Default
	Hardware RTS/CTS	
	Software Xon/Xoff	

3.5 Setup submenu: Chipset



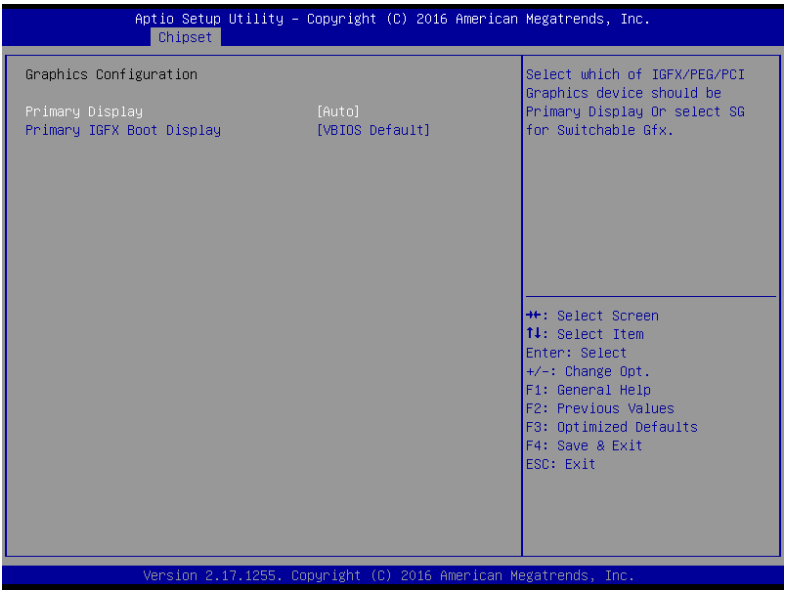
3.5.1 Chipset: System Agent (SA) Configuration



Options summary:

PEG Port Gen Speed	Auto	Default
	Gen1	
	Gen2	
	Gen3	
Configure PEG Port Gen Speed.		

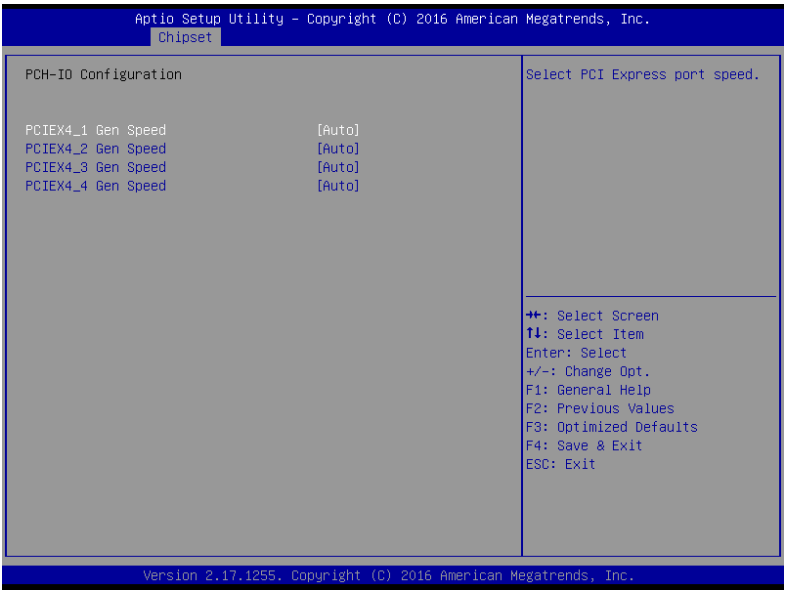
3.5.1.1 System Agent (SA) Configuration: Graphics Configuration



Options summary:

Primary Display	Auto	Default
	IGFX	
	PEG	
	PCIE	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Primary IGFX Boot Display	VBIOS Default	Default
	CRT	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.		

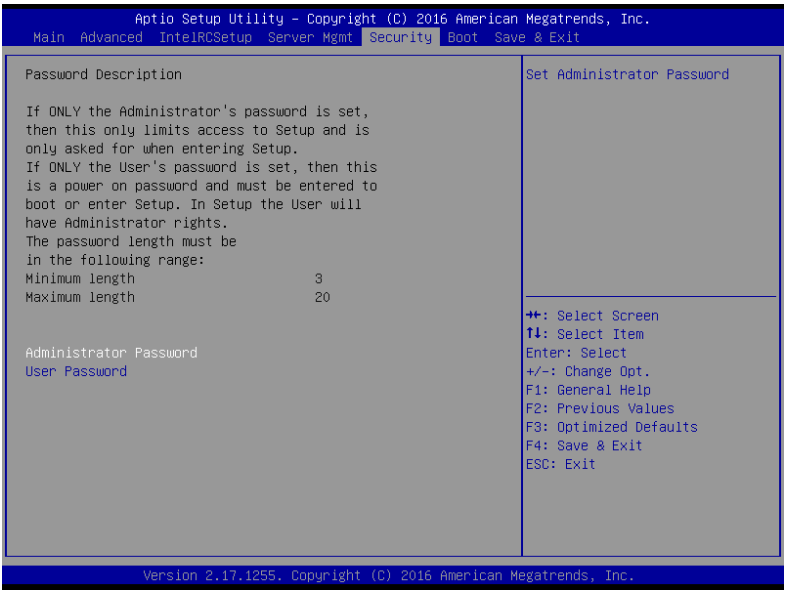
3.5.2 Chipset: PCH-IO Configuration



Options summary:

PCIEX4_1 Gen Speed	Auto	Default
	Gen1	
	Gen2	
	Gen3	
Select PCI Express port speed.		

3.6 Setup submenu: Security



Change User/Administrator Password

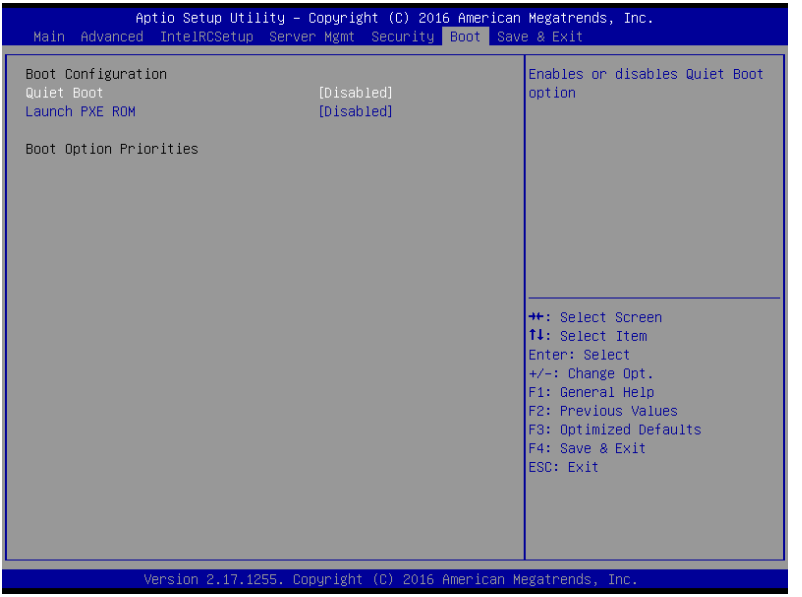
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

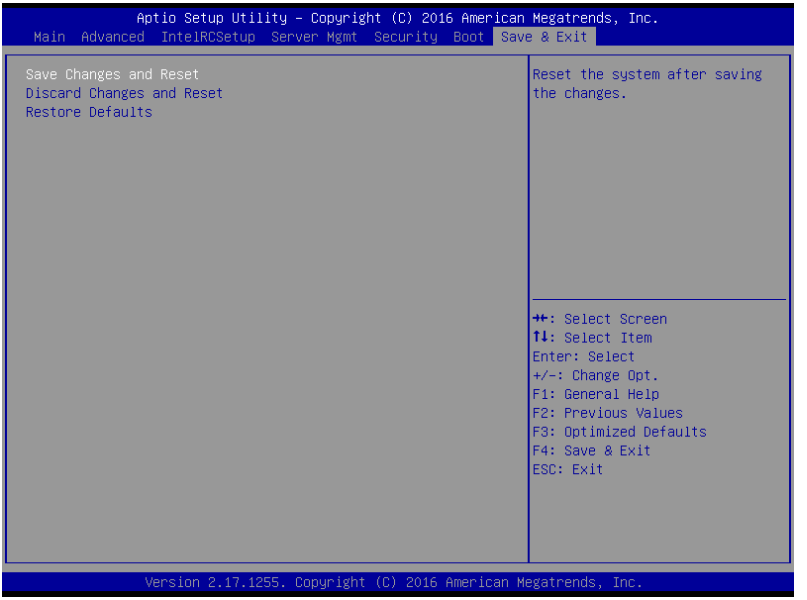
3.7 Setup submenu: Boot



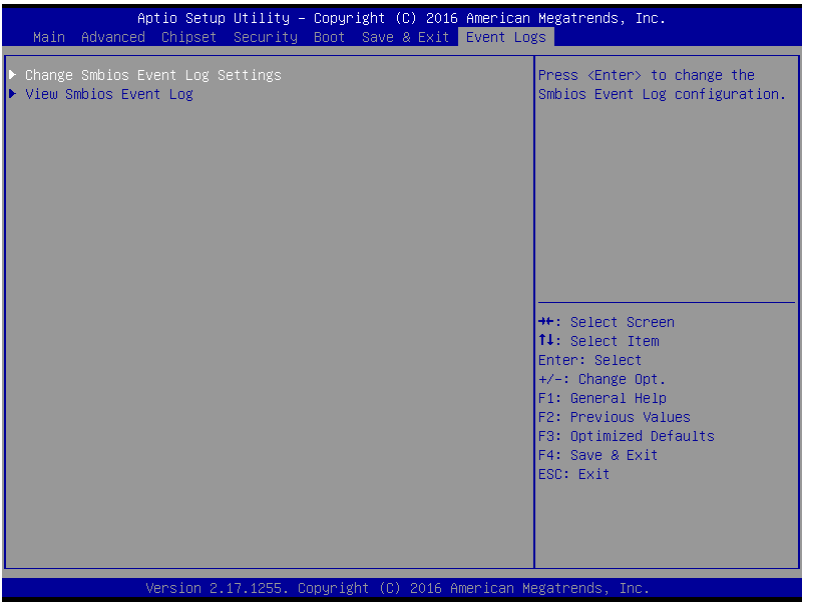
Options summary:

Quiet Boot	Disabled	Default
	Enabled	
En/Disable showing boot logo.		
Launch PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option.		

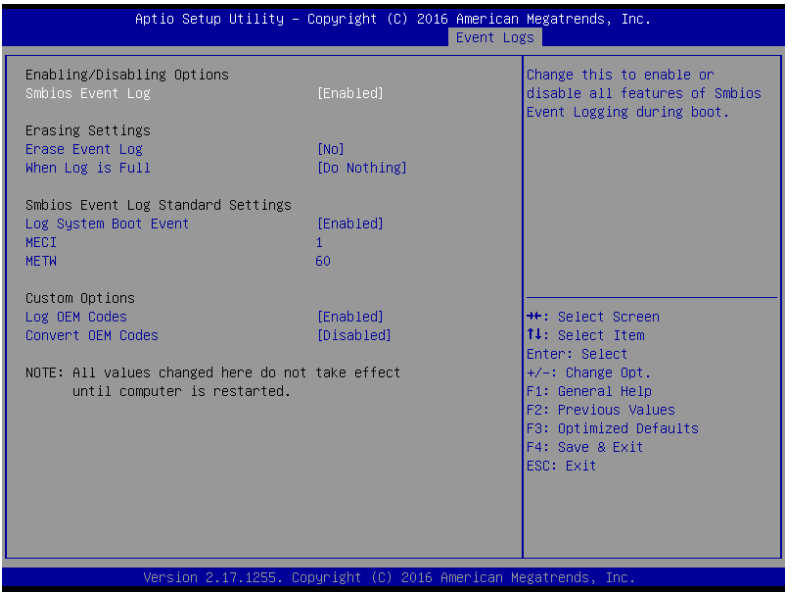
3.8 Setup submenu: Save & Exit



3.9 Setup submenu: Event Logs



3.9.1 Event Logs: Change Smbios Event Log Settings



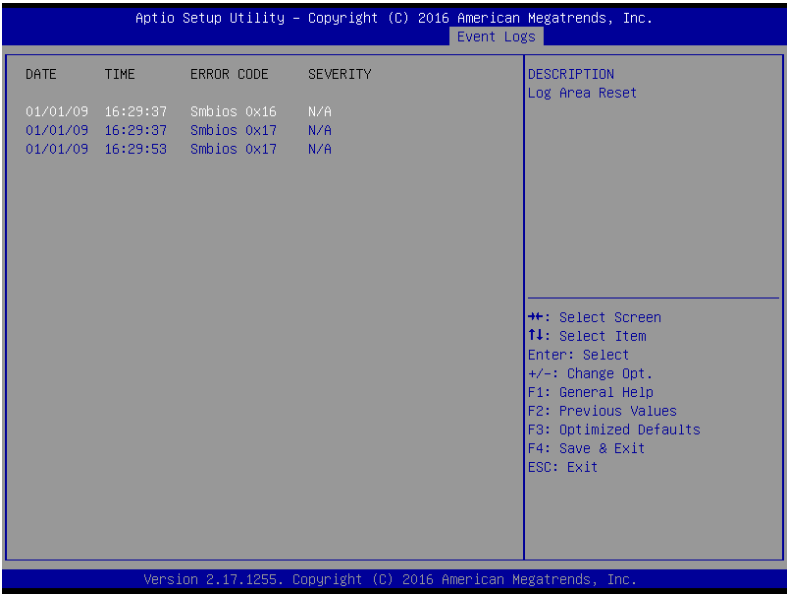
Options summary:

Smbios Event Log	Disabled	
	Enabled	Default
Change this to enable or disable all features of Smbios Event Logging during boot.		
Erase Event Log	No	Default
	Yes, Next reset	
	Yes, Every reset	
Choose options for erasing Smbios Event Log. Erasing is done prior to any logging activation during reset.		
When Log is Full	Do Nothing	Default
	Erase Immediately	
Choose options for reactions to a full Smbios Event Log.		

Log System Boot Event	Disabled	
	Enabled	Default
Choose option to enable/disable logging of System boot event.		

MECI	0-255	Default (1)
Mutiple Event Count Increment: The number of occurrences of a duplicate event that must pass before the multiple-event counter of log entry is updated.The value ranges from 1 to 255.		
METW	0-99	Default (60)
Mutiple Event Time Window: The number of minutes which must pass between duplicate log entries which utilize a multiple-event counter. The value ranges from 0 to 99 minutes.		
Log OEM Codes	Disabled	
	Enabled	Default
Enable or disable the logging of EFI Status Codes as OEM Codes (if not already converted to legacy).		
Log System Boot Event	Disabled	Default
	Enabled	
Enable or disable the converting of EFI Status Codes to Standard Smbios Types (Not all may be translated).		

3.9.2 Event Logs: View Smbios Event Log



Chapter 4

Drivers Installation

4.1 Drivers Installation

The drivers can be found in the product page for FWS-7820 at aaeon.com. Please follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **Step 1 - Chipset** folder followed by the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **Step 2 - Graphic** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Driver

1. Open the **Step 3 - LAN** folder and select your OS
2. Open the**.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install USB3.0 Driver

1. Open the **Step 4 – USB3.0** folder followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install ME Driver

1. Open the **Step 5 – ME** folder followed by the **SetupME.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 6 – Install Intel RST Driver

1. Open the **Step 6 – Intel RST** folder followed by the **SetupRST.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 7 – Install Serial Port Driver (Optional)

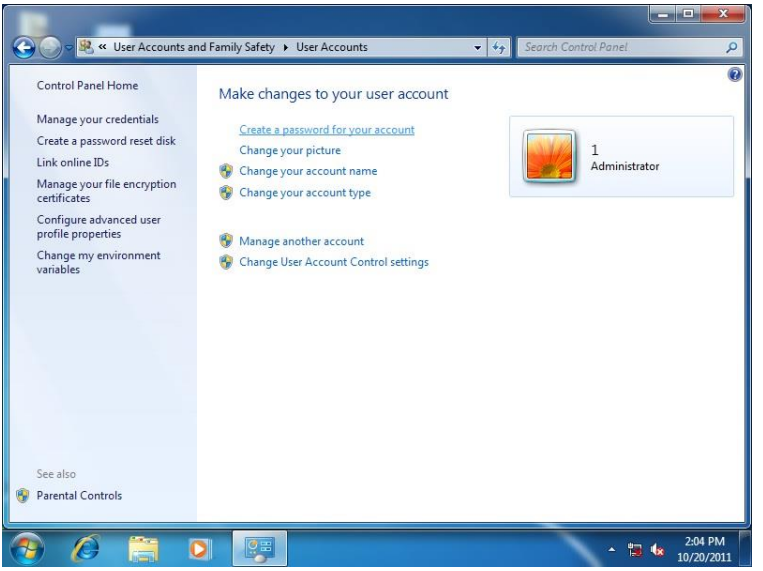
Note: Patch file for Serial port when encountering [time out error] during Burning test procedure

For Windows XP 32-bit

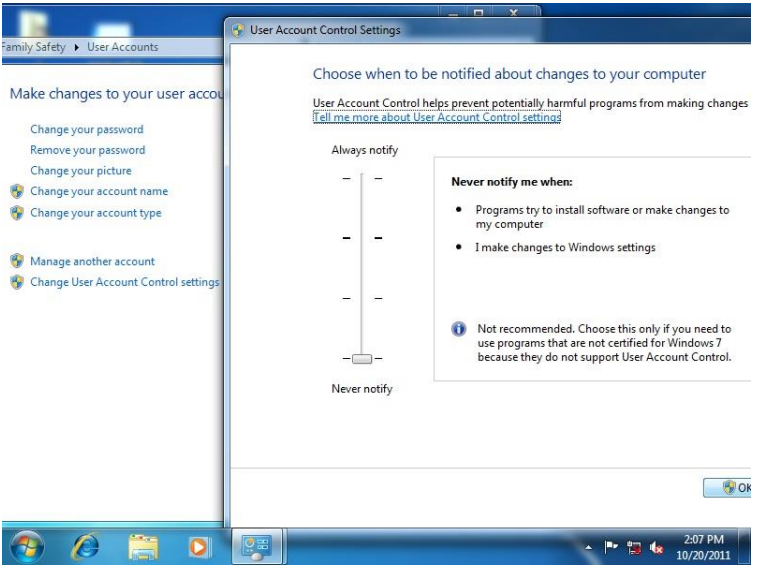
1. Open the **Step 7 –Serial Port Driver (Optional)** folder followed by the **patch.bat** file
2. Follow the instructions
3. Drivers will be installed automatically

For Windows 7 32/64-bit

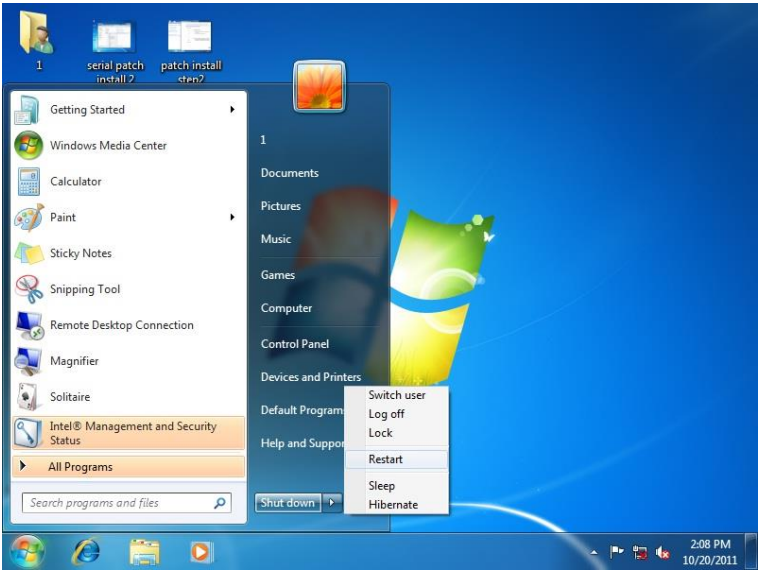
1. To run [Change User Account Control Settings] in Control panel\User Accounts and Family Safety



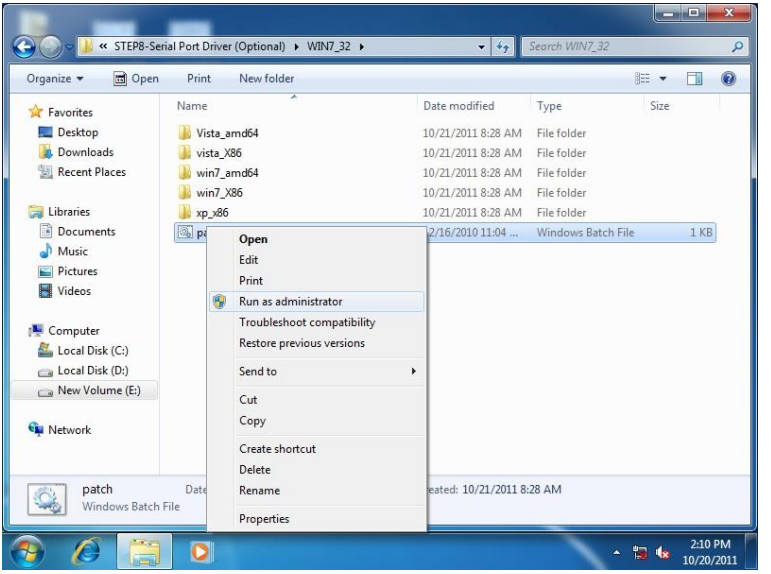
2. Change User Account Control Settings to [Never notify]

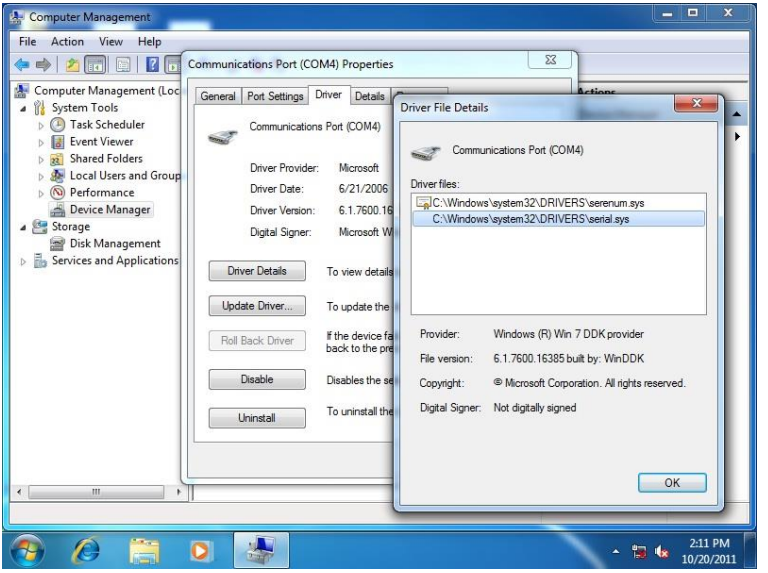


3. Reboot



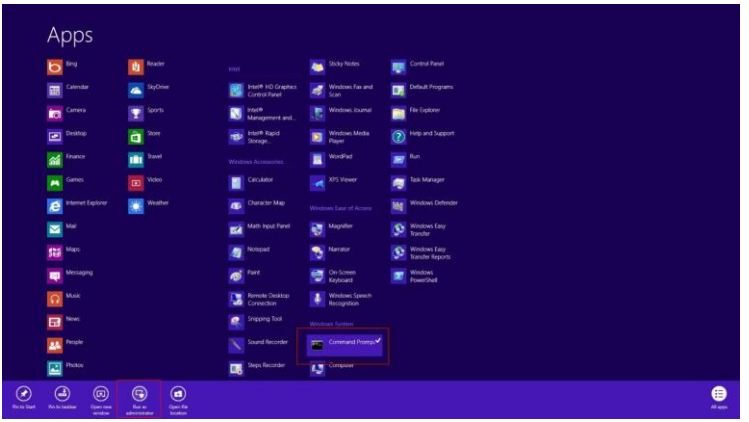
4. To run patch.bat with [Run as administrator].



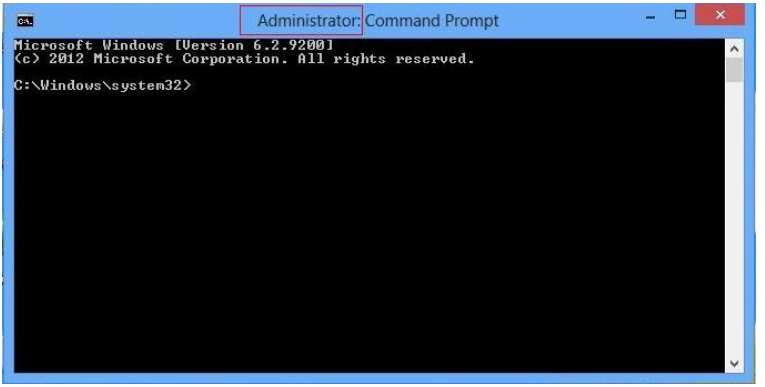


For Windows 8 32/64-bit

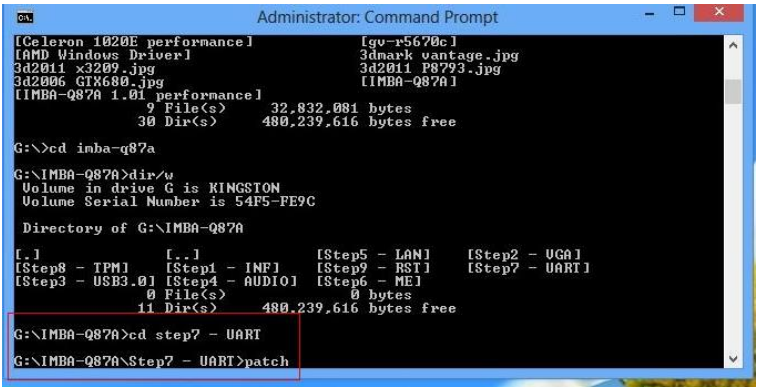
1. Right click [Command Prompt] and [run as administrator]



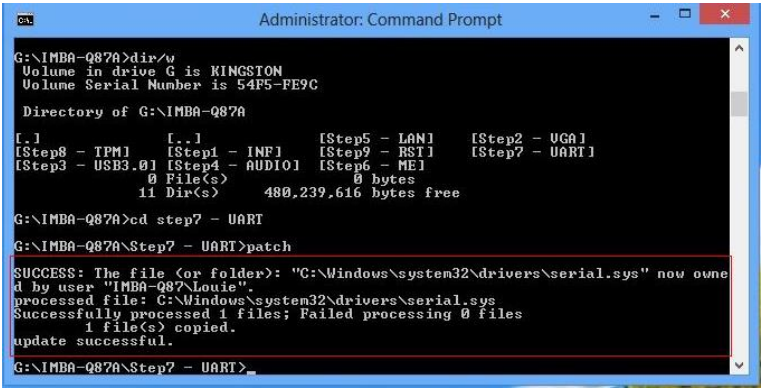
2. Run Command Prompt by administrator



3. To run patch.bat in UART driver folder path

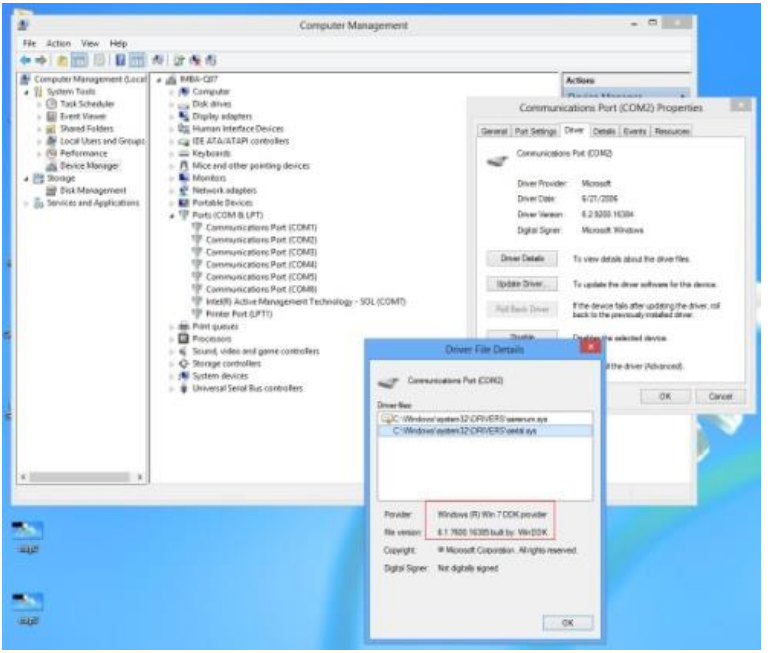


4. Update successful



5. Restart

6. Com port driver\serial.sys, provider will change to [Windows(R) Win7 DDK provider]



Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	4(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*******************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*******************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable ( ){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig ( ){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID   WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*********************************************************************************
```

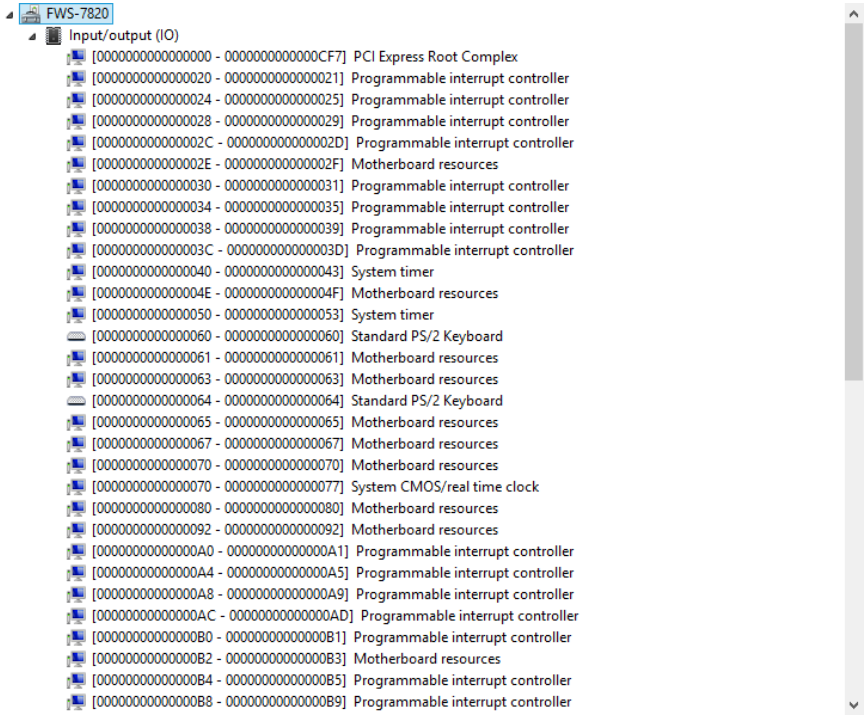
```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       Switch(SIOIndex){
              Case 0x2E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0x55);
                        Break;
              Case 0x4E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0xAA);
                     Break;
       }
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0x02);
       IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}
*****************************************************************************
```

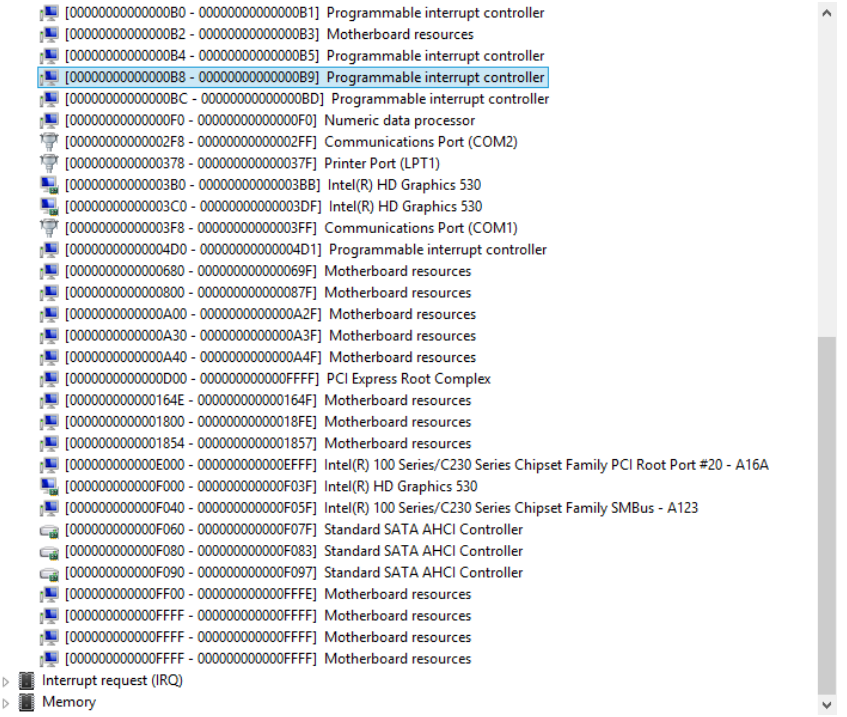
```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

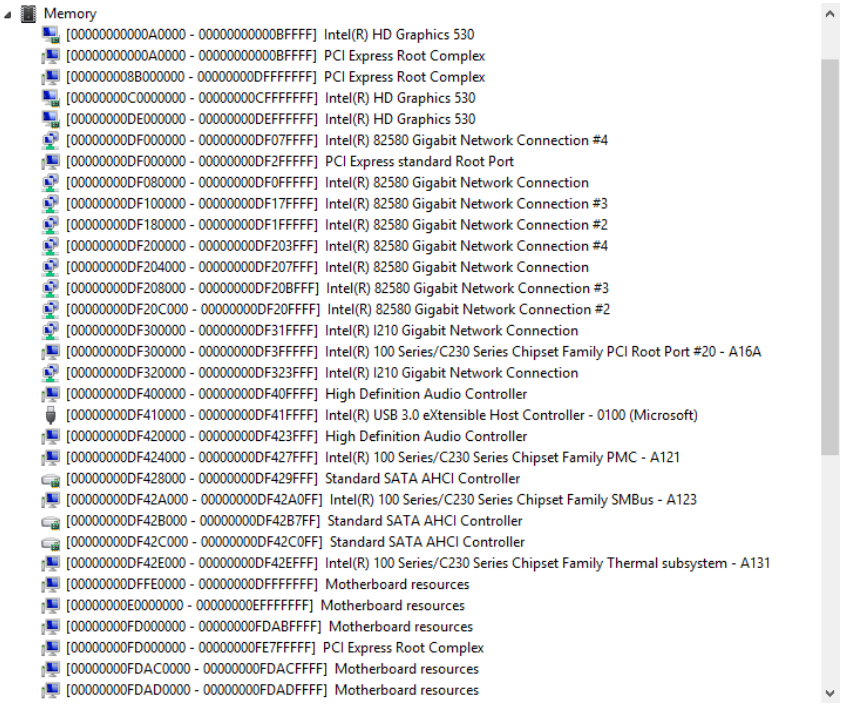
I/O Information

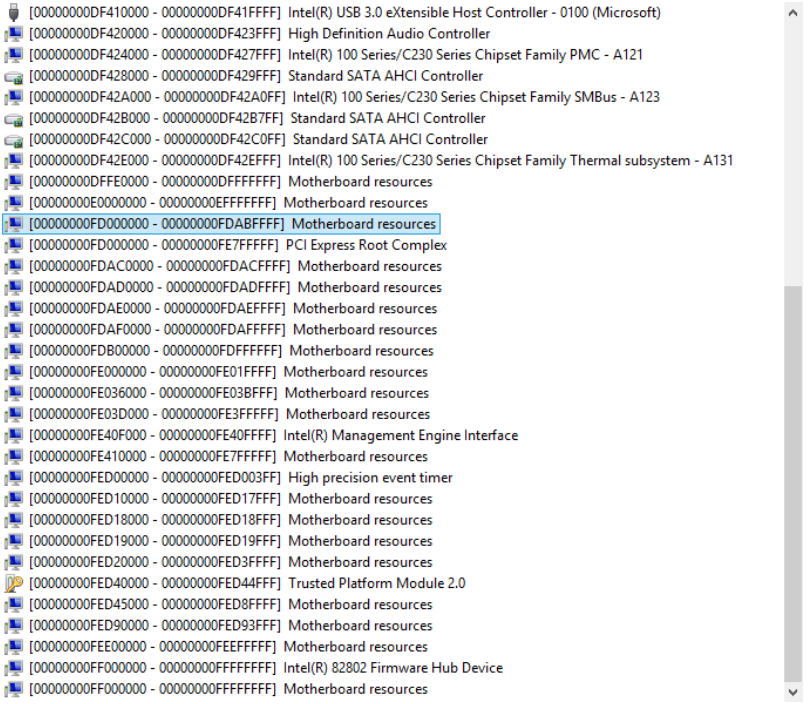
B.1 I/O Address Map



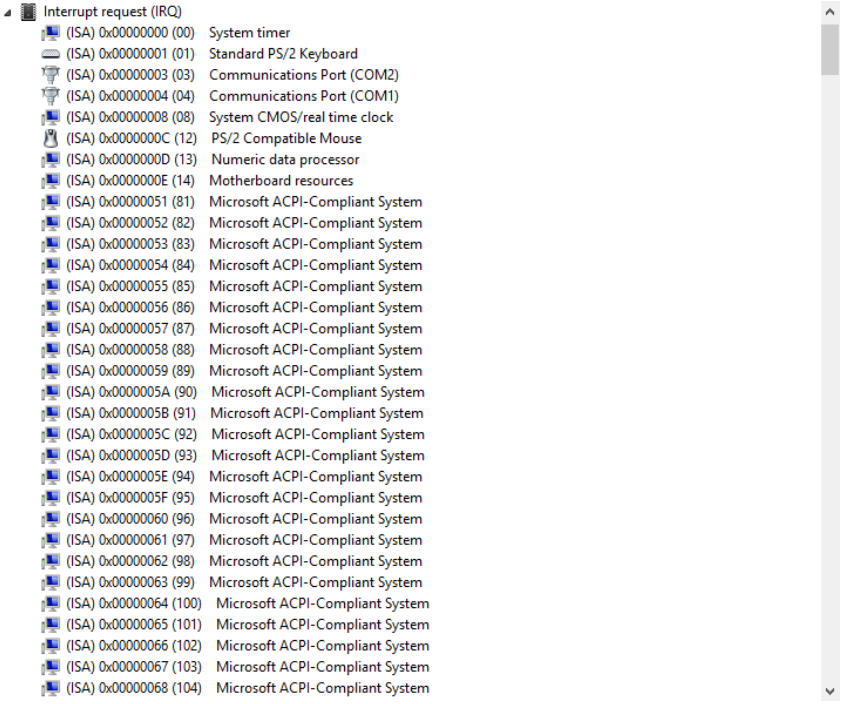

[00000000000000B0 - 00000000000000B1] Programmable interrupt controller
[00000000000000B2 - 00000000000000B3] Motherboard resources
[00000000000000B4 - 00000000000000B5] Programmable interrupt controller
[00000000000000B8 - 00000000000000B9] Programmable interrupt controller
[00000000000000BC - 00000000000000BD] Programmable interrupt controller
[00000000000000F0 - 00000000000000F0] Numeric data processor
[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[0000000000000378 - 000000000000037F] Printer Port (LPT1)
[00000000000003B0 - 00000000000003BB] Intel(R) HD Graphics 530
[00000000000003C0 - 00000000000003DF] Intel(R) HD Graphics 530
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000800 - 000000000000087F] Motherboard resources
[0000000000000A00 - 0000000000000A2F] Motherboard resources
[0000000000000A30 - 0000000000000A3F] Motherboard resources
[0000000000000A40 - 0000000000000A4F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 00000000000018FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[000000000000E000 - 000000000000EFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Root Port #20 - A16A
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics 530
[000000000000F040 - 000000000000F05F] Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
Interrupt request (IRQ)
Memory

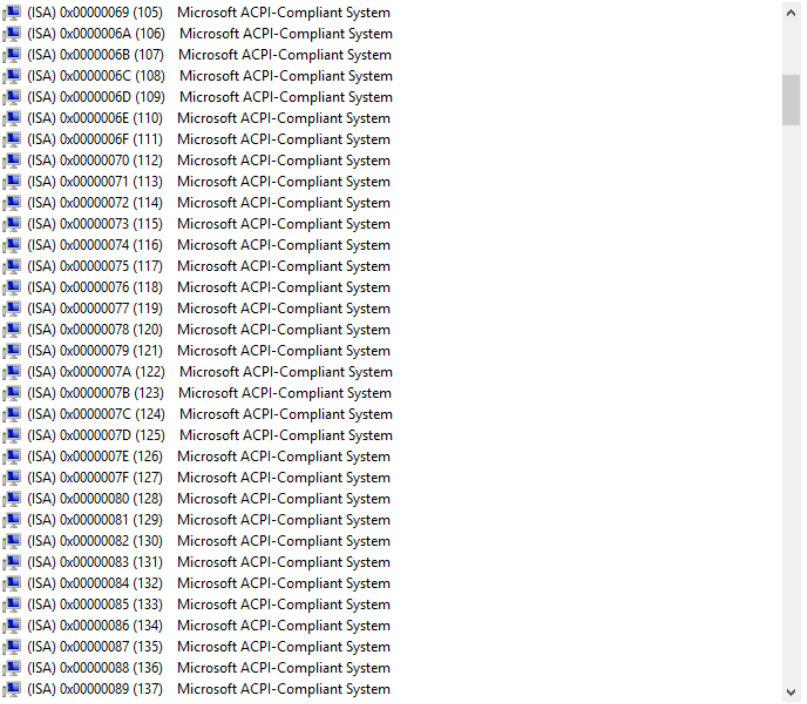
B.2 Memory Address Map




[00000000DF410000 - 00000000DF41FFFF] Intel(R) USB 3.0 eXtensible Host Controller - 0100 (Microsoft)
[00000000DF420000 - 00000000DF423FFF] High Definition Audio Controller
[00000000DF424000 - 00000000DF427FFF] Intel(R) 100 Series/C230 Series Chipset Family PMC - A121
[00000000DF428000 - 00000000DF429FFF] Standard SATA AHCI Controller
[00000000DF42A000 - 00000000DF42A0FF] Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[00000000DF42B000 - 00000000DF42B7FF] Standard SATA AHCI Controller
[00000000DF42C000 - 00000000DF42C0FF] Standard SATA AHCI Controller
[00000000DF42E000 - 00000000DF42EFFF] Intel(R) 100 Series/C230 Series Chipset Family Thermal subsystem - A131
[00000000DFFE0000 - 00000000DFFFFFFF] Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF] Motherboard resources
[00000000FD000000 - 00000000FDABFFFF] Motherboard resources
[00000000FD000000 - 00000000FE7FFFFF] PCI Express Root Complex
[00000000FDAC0000 - 00000000FDACFFFF] Motherboard resources
[00000000FDAD0000 - 00000000FDADFFFF] Motherboard resources
[00000000FDAE0000 - 00000000FDAEFFFF] Motherboard resources
[00000000FDAF0000 - 00000000FDAFFFFF] Motherboard resources
[00000000FDB00000 - 00000000FDFFFFFF] Motherboard resources
[00000000FE000000 - 00000000FE01FFFF] Motherboard resources
[00000000FE036000 - 00000000FE03BFFF] Motherboard resources
[00000000FE03D000 - 00000000FE3FFFFF] Motherboard resources
[00000000FE40F000 - 00000000FE40FFFF] Intel(R) Management Engine Interface
[00000000FE410000 - 00000000FE7FFFFF] Motherboard resources
[00000000FED00000 - 00000000FED003FF] High precision event timer
[00000000FED10000 - 00000000FED17FFF] Motherboard resources
[00000000FED18000 - 00000000FED18FFF] Motherboard resources
[00000000FED19000 - 00000000FED19FFF] Motherboard resources
[00000000FED20000 - 00000000FED3FFFF] Motherboard resources
[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
[00000000FED45000 - 00000000FED8FFFF] Motherboard resources
[00000000FED90000 - 00000000FED93FFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF] Intel(R) 82802 Firmware Hub Device
[00000000FF000000 - 00000000FFFFFFFF] Motherboard resources

B.3 IRQ Mapping Chart

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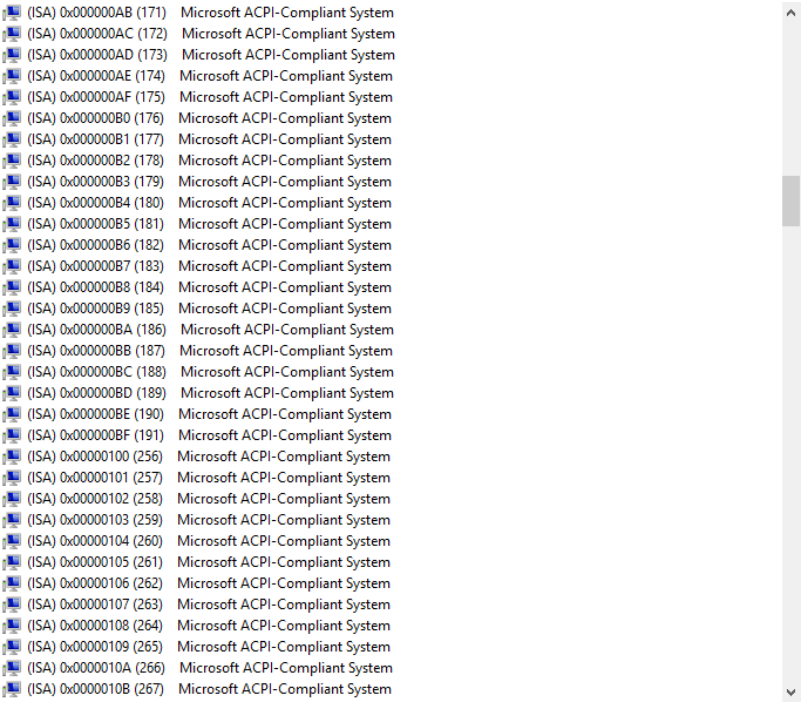
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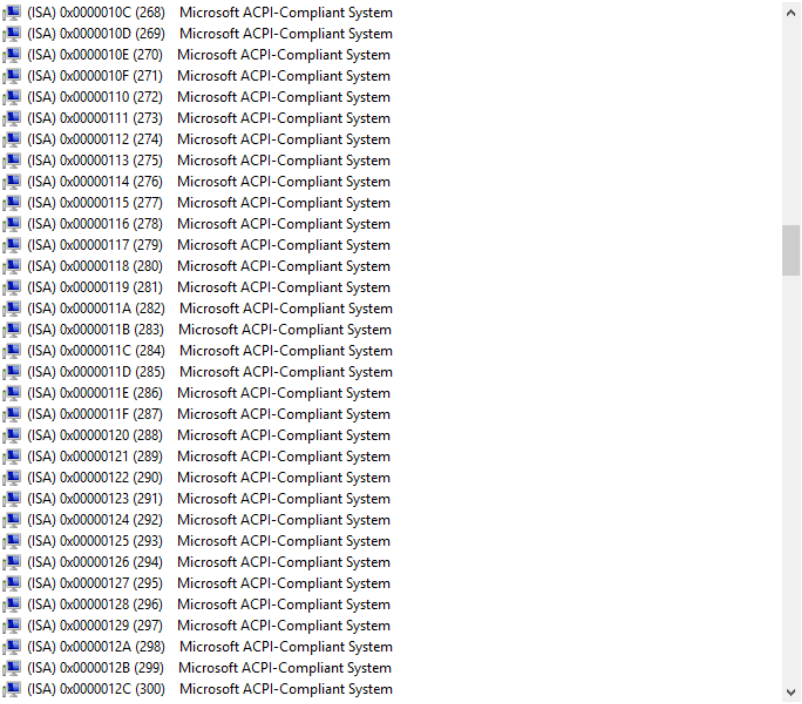
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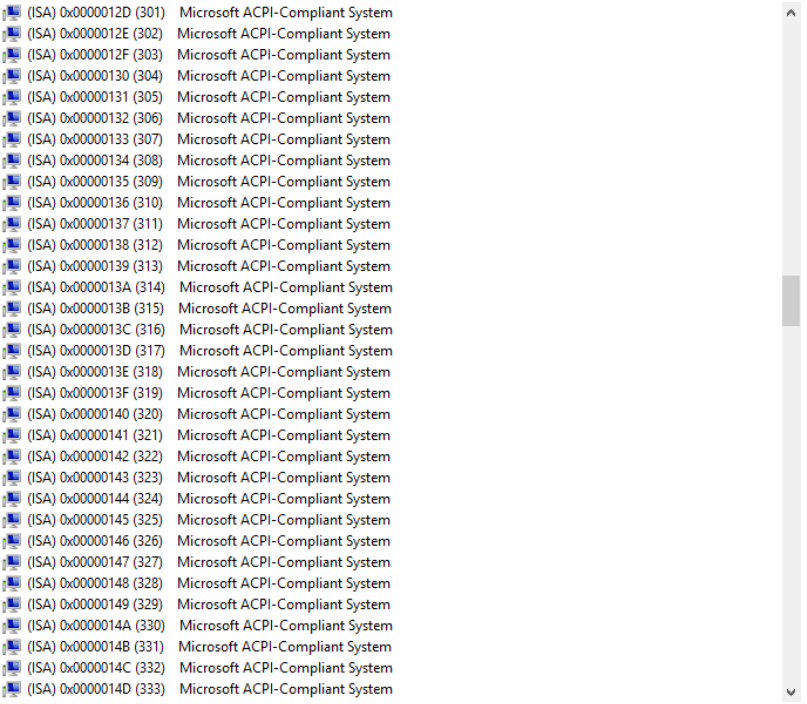
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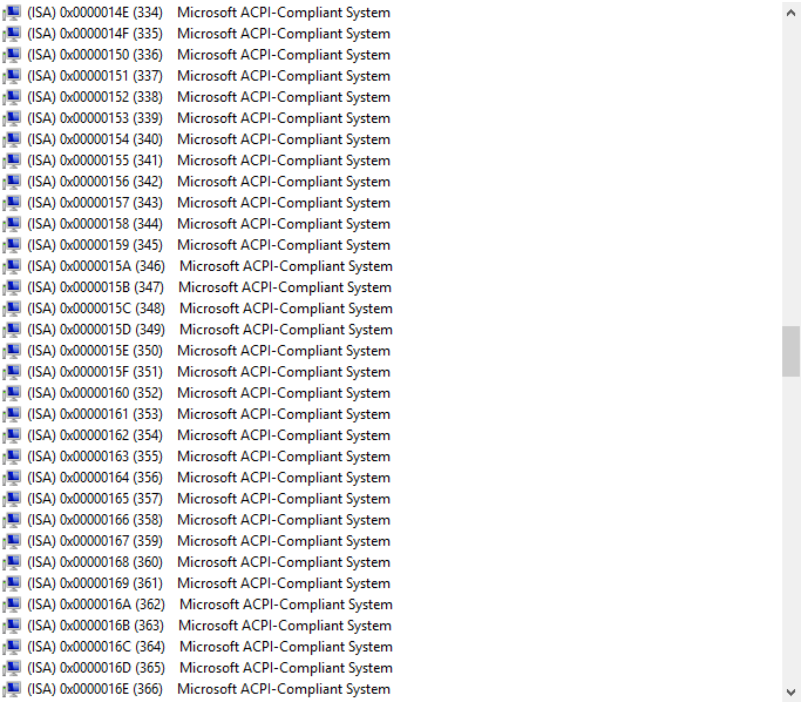
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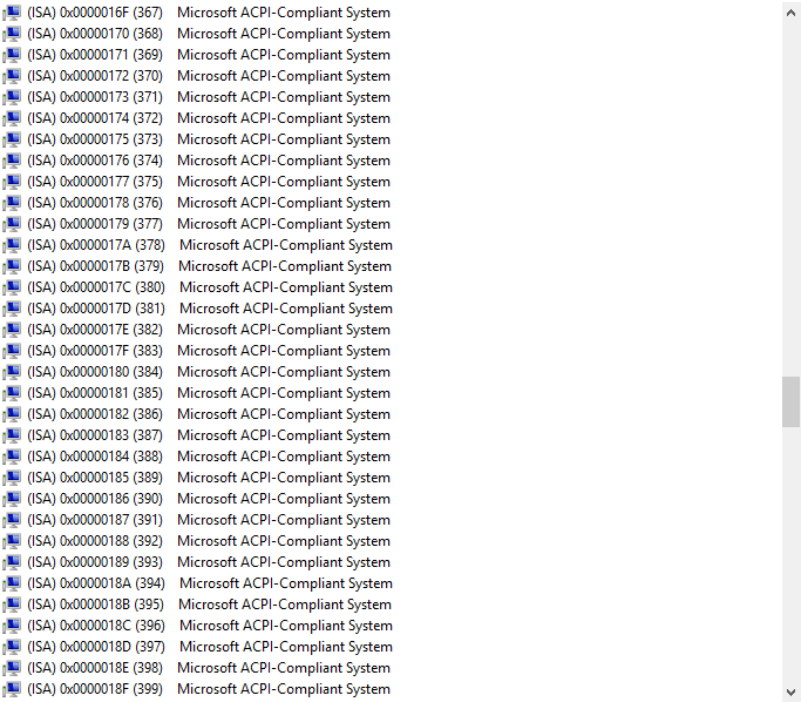
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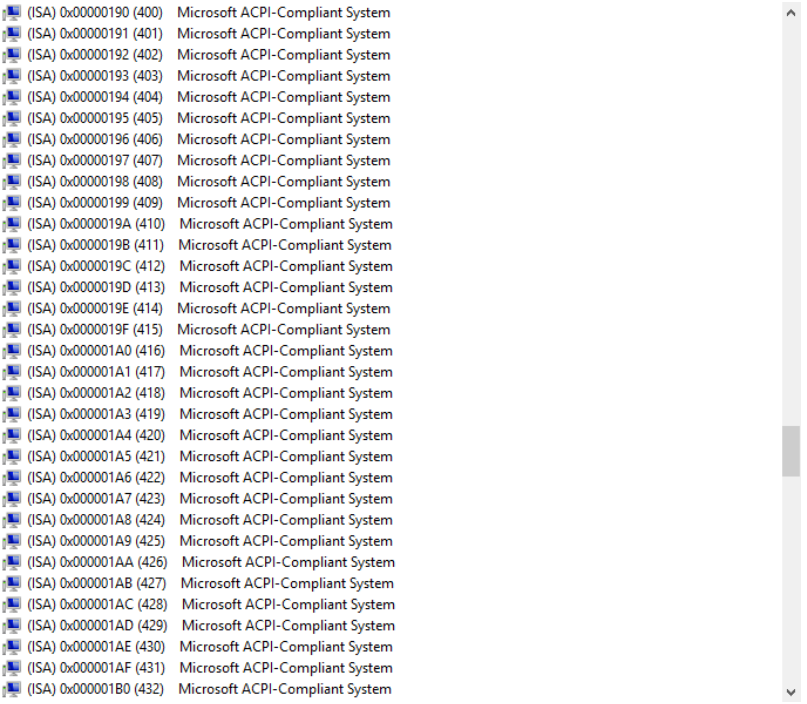
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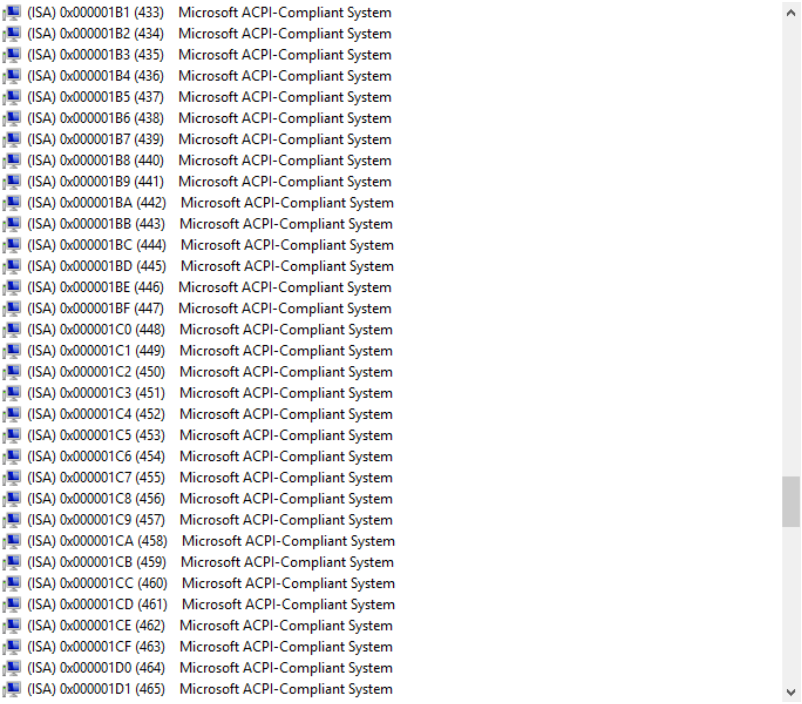
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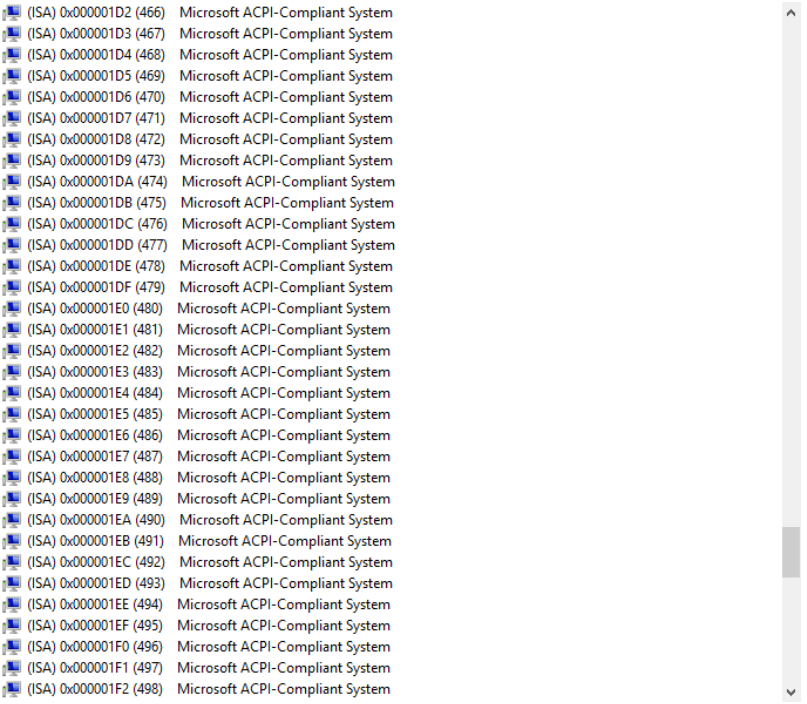
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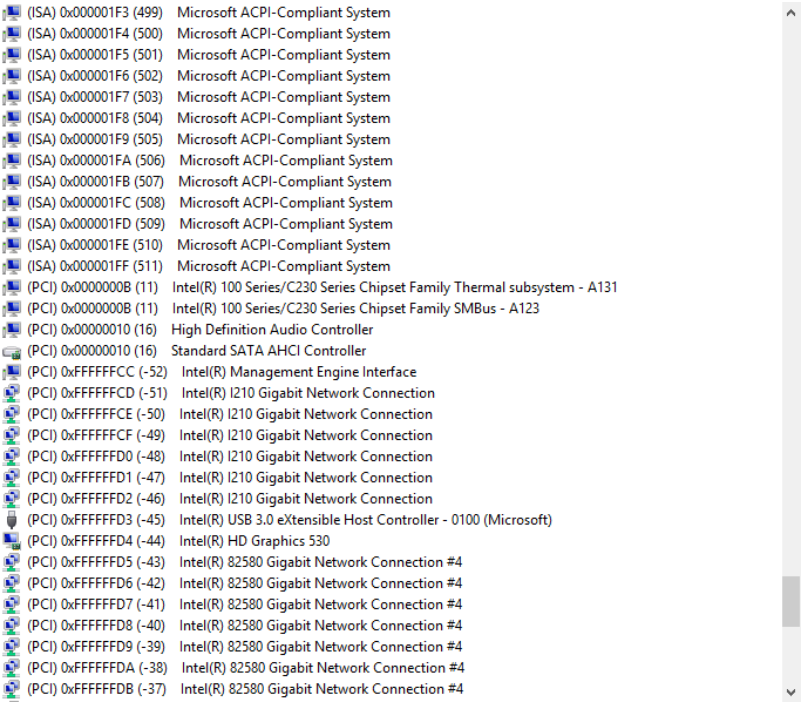
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(PCI) 0x00000010 (16) Standard SATA AHCI Controller
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(PCI) 0xFFFFFFCD (-51) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFCE (-50) Intel(R) I210 Gigabit Network Connection
(PCI) 0xFFFFFFCF (-49) Intel(R) I210 Gigabit Network Connection
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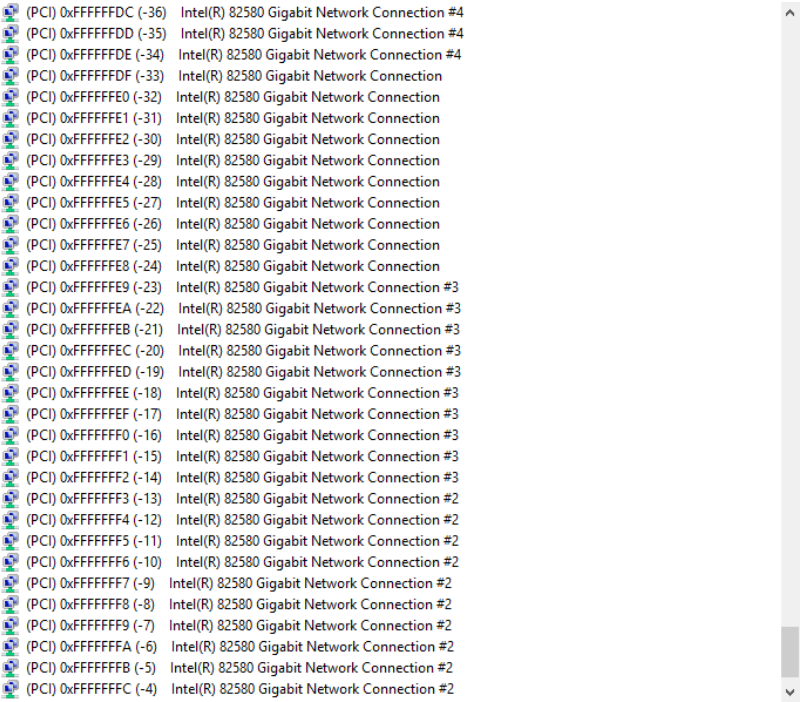
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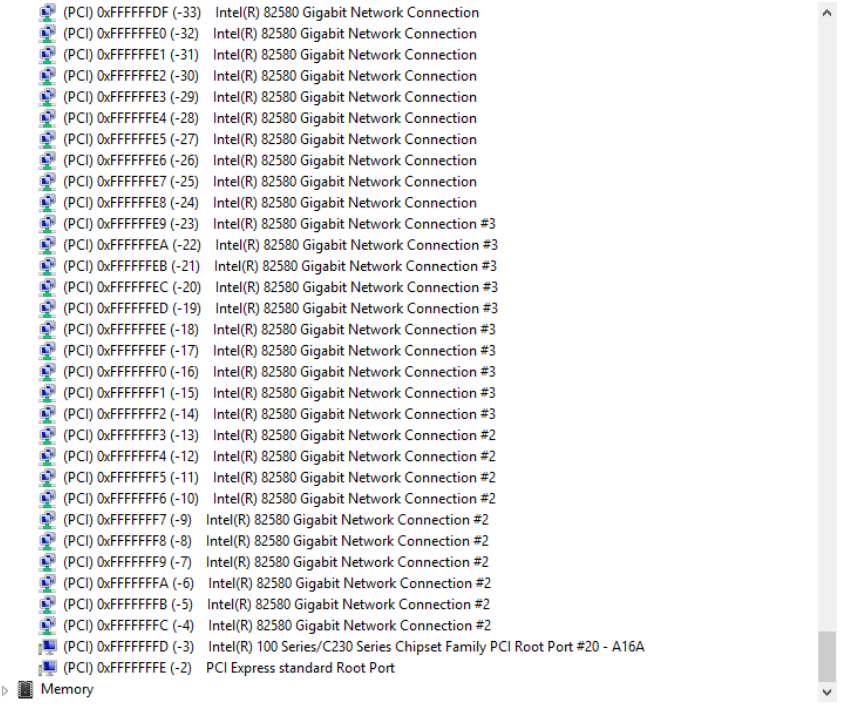
(PCI) 0xFFFFFFDD (-35) Intel(R) 82580 Gigabit Network Connection #4
(PCI) 0xFFFFFFDE (-34) Intel(R) 82580 Gigabit Network Connection #4
(PCI) 0xFFFFFFDF (-33) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE0 (-32) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE1 (-31) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE2 (-30) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE3 (-29) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE4 (-28) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE5 (-27) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE6 (-26) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE7 (-25) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE8 (-24) Intel(R) 82580 Gigabit Network Connection
(PCI) 0xFFFFFFE9 (-23) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFEA (-22) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFEB (-21) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFEC (-20) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFED (-19) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFEE (-18) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFEF (-17) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFF0 (-16) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFF1 (-15) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFF2 (-14) Intel(R) 82580 Gigabit Network Connection #3
(PCI) 0xFFFFFFF3 (-13) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF4 (-12) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF5 (-11) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF6 (-10) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF7 (-9) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF8 (-8) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFF9 (-7) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFA (-6) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFB (-5) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFC (-4) Intel(R) 82580 Gigabit Network Connection #2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(PCI) 0xFFFFFFFA (-6) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFB (-5) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFC (-4) Intel(R) 82580 Gigabit Network Connection #2
(PCI) 0xFFFFFFFD (-3) Intel(R) 100 Series/C230 Series Chipset Family PCI Root Port #20 - A16A
(PCI) 0xFFFFFFFE (-2) PCI Express standard Root Port
Memory

Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

Table1: LED Status

	STA_LED2	STA_LED1	STA_LED0
LED Off	0	0	0
Red LED On	0	0	1
Red LED Blink	0	1	0
Red LED Fast Blink	0	1	1
Reserved	1	0	0
Green LED Blink	1	0	1
Green LED Fast Blink	1	1	0
Green LED On	1	1	1

Table2: Status LED and register mapping table

	CPLD Slave Address 0x90 (Note1)			
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

Sample Code:

```
*********************************************************************************************
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*********************************************************************************************
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
```

```
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*********************************************************************************************
```

C.2 LAN Bypass

Table1: LAN Kit ID Select

LAN_ID3	LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	0	LAN Kit 1 Selected
0	0	0	1	LAN Kit 2 Selected
0	0	1	0	LAN Kit 3 Selected
0	0	1	1	LAN Kit 4 Selected
0	1	0	0	LAN Kit 5 Selected
0	1	0	1	LAN Kit 6 Selected
0	1	1	0	LAN Kit 7 Selected
0	1	1	1	LAN Kit 8 Selected
1	0	0	0	LAN Kit 9 Selected
1	0	0	1	LAN Kit 10 Selected

Table2: LAN Bypass register table

Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refert to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function

	behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

Sample Code

```
*********************************************************************************************
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*********************************************************************************************
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
```

```
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xBF;
else                                    // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
        bData = bData & 0xEF;
else                            // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*********************************************************************************
```

C.3 Software Reset Button (General Propose Input)

Table 1: Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

Table 2: LAN Bypass register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Sample Code:

```
*********************************************************************************
#define Word      BTN_STS      //This parameter is represented from Note1
#define Byte      BTN_STS_R    //This parameter is represented from Note2
*********************************************************************************
Byte   GET_Value (Word IoAddr, Byte BitNum,Byte Value){
       BYTE  TmpValue;

       TmpValue = inportb (IoAddr);
        return   (TmpValue & (1 << BitNum))
}
*********************************************************************************
VOID   Main(){
       Byte RstBtn;

       RstBtn = GET_Value (BTN_STS, BTN_STS_R);  // Active Low
}
*********************************************************************************
```