FWS-2360

Desktop Network Appliance

User's Manual 1st Ed

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2360	1
● SATA cable	1
● SATA power cable	1
● Power adapter	1
● HDD bracket kit	1
● Rubber foot	4

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O
外壳	O	O	O	O	O	O
中央处理器与内存	O	O	O	O	O	O
硬盘	O	O	O	O	O	O
电源	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	O	O	O	O	O	O
Hard Disk	O	O	O	O	O	O
PSU	O	O	O	O	O	O

O： The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
● Processor	Intel® Atom™ Processor Supports Dual and Quad core
● Chipset	Intel® C3000 SoC Processor
● System Memory	DDR4 SODIMM ECC DIMM (Dual core 1 slot Quad core 2 Slot) Up to 32GB
● Ethernet	Intel® X553 (Marvell 88E1543) RJ45 x 4 Intel® i211 RJ45 x 2 Or Intel® i210 SFP x 2 (Default Intel® i211 RJ45 x 2))
● Bypass	Supports up to 2 pairs bypass function
● Storage	2.5" HDD bay x 1 Onboard eMMC up to 16GB, SATA 6.0 Gb/s port x 1
● Expansion Interface	Mini-Card socket (full-size) x 2 (1 with SIM socket) USB 3.0 x 2
● Front Panel I/O	Power LED x 1 Status LED x 1 Storage Active LED x 1 Bypass LED x 2 LAN LED x 12
● Rear Panel I/O	USB3.0 Port x 2(Quad Core CPU) USB3.0 Port x 1(Dual Core CPU) RJ-45 Port x 4 SFP x 2

	RJ-45 Console x 1 12V DC Power Input x 1 Software Reset Button x 1 Power Button x 1 Antenna Hole x 4
RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
TPM	TPM v1.2 9660/TPM2.0 9665
GPIO	Reserve internal pin header 8-bit Digital I/O interface (4-in /4-out)
Fan	System Fan x 1
Color	Black
Power Requirement	12V DC Power in connector
Dimension (W x D x H)	8.66" x 4.13" x 1.73" (220mm x 105mm x 44mm)

Display

Graphic Engine	--
Output Interface	--

I/O

Serial Port	RJ-45 console x 1
Keyboard and Mouse	Reserved pin-header
USB	USB 3.0 x 2

Environmental

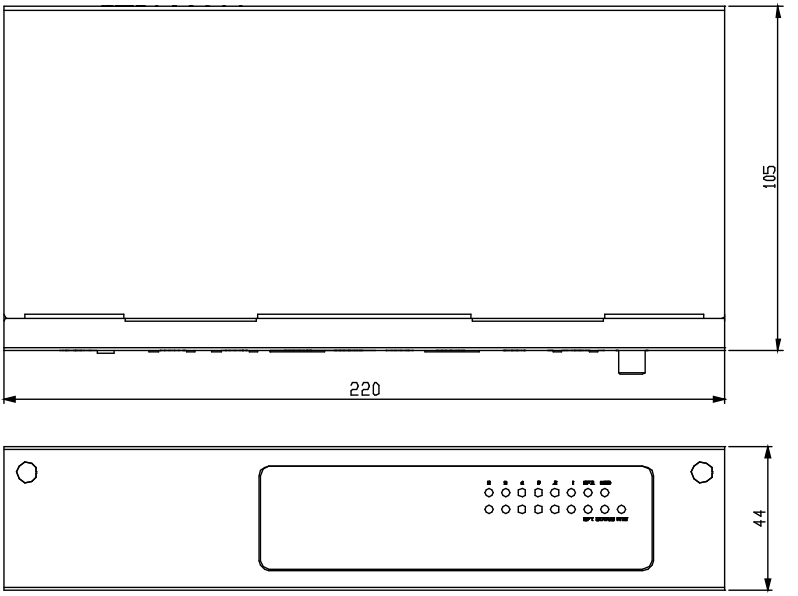
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing
Anti-Vibration	0.5 Grms/ 5 ~ 500Hz / operation (2.5" HDD) 1.5 Grms/ 5 ~ 500Hz / non operation
Anti-Shock	10 G peak acceleration (11 m sec. duration), operation 20 G peak acceleration (11 m sec. duration), non operation

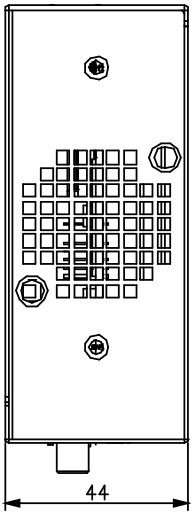
Chapter 2

Hardware Information

2.1 Dimensions

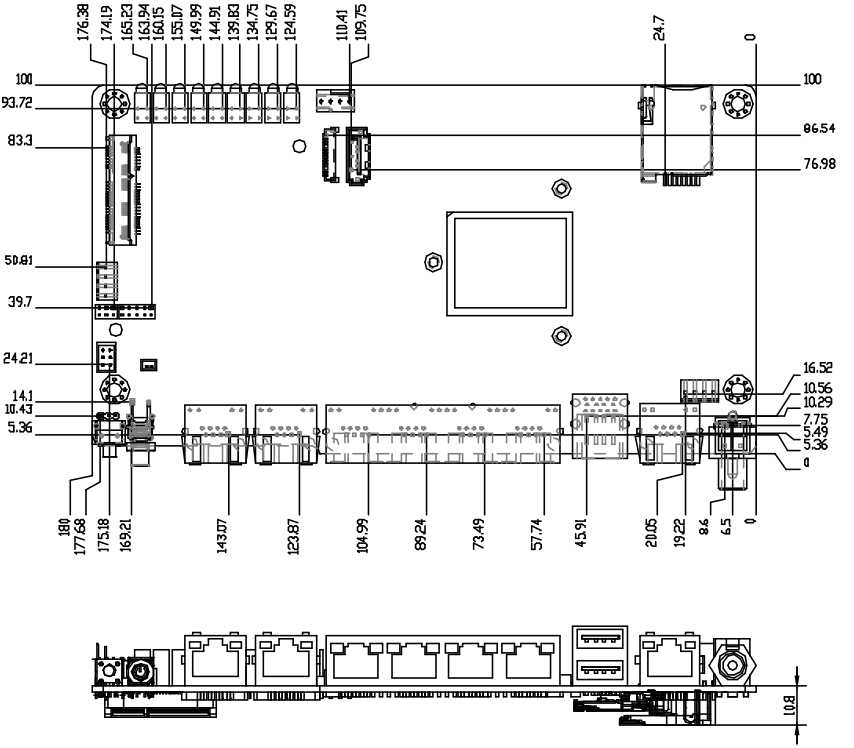
System



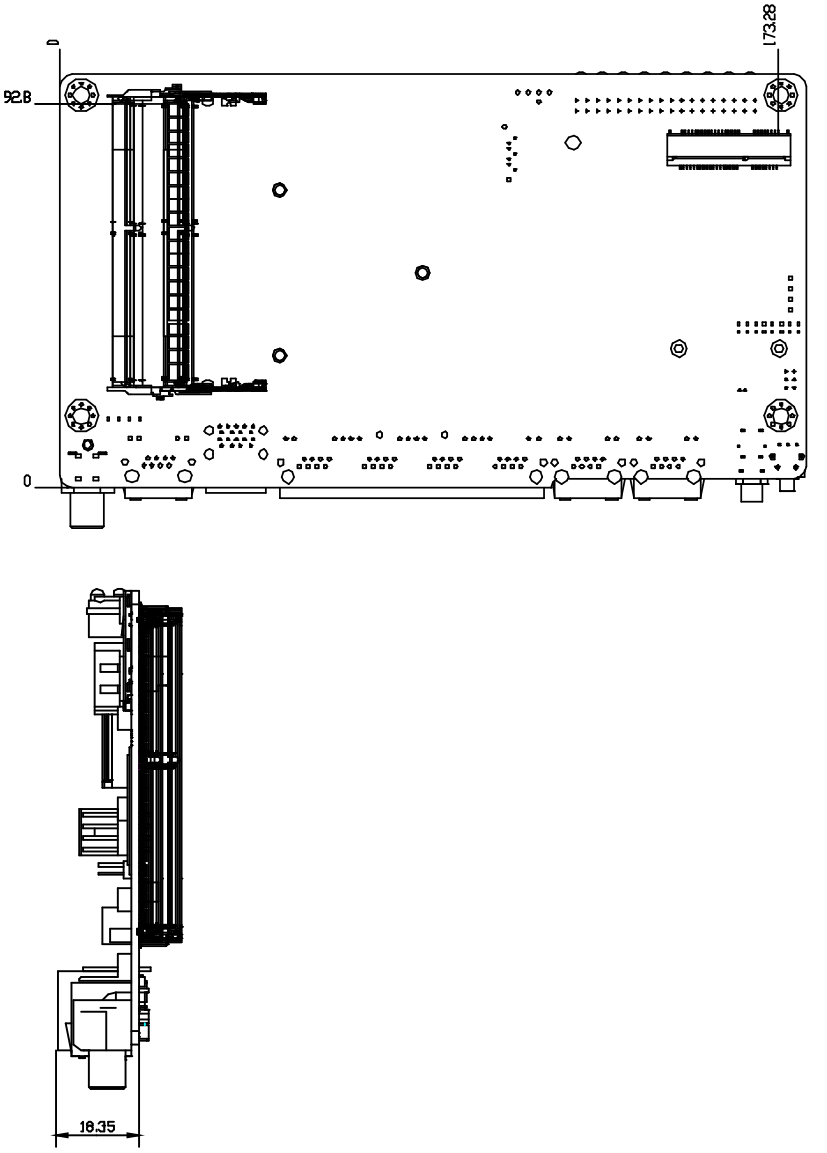


Board

Component Side

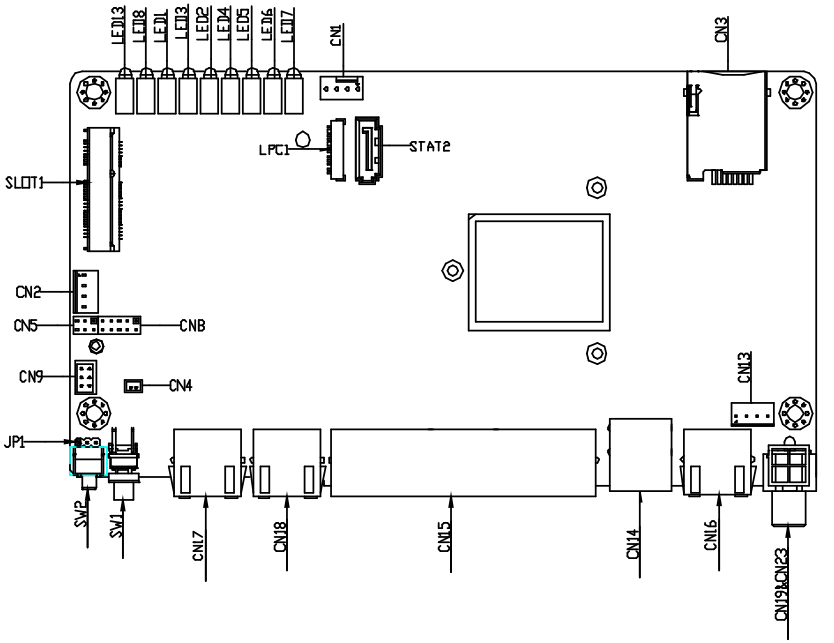


Solder Side

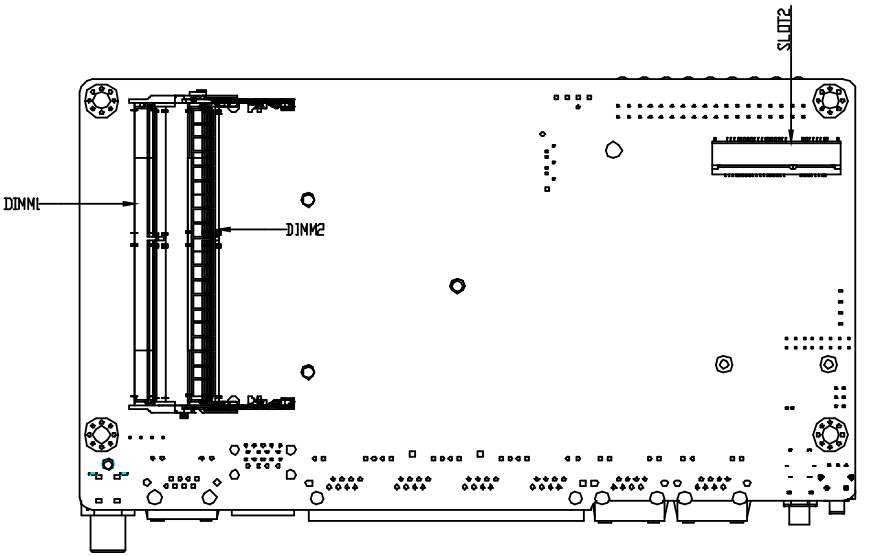


2.2 Jumpers and Connectors

Component Side



Solder Side



2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	Auto PWR Button
CN5	Clear CMOS

2.3.1 AUTO Power Button (JP1)

Normal	1-2
Auto power on	2-3

2.3.2 Clear CMOS (CN5)

Normal	1-3.2-4
Clear CMOS	3-5,4-6

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN19	DC-INPUT (Only 12V)
CN16	Console Port(Serial Port)
CN14	USB3.0 x2
CN15	LAN 3~6 RJ45 Port
CN18	LAN 2 RJ45 Port
CN17	LAN 1 RJ45 Port
SW1	Power Button
SW2	Software Button
CN10	Power Button Pin Header
CN11	System Reset Pin Header
CN12	CASEOPEN Pin Header
CN9	PS2 Pin Header
CN8	Digital IO Pin Header
CN4	BAT
SLOT1	PCIE Mini Card Full Function w/SIM CN3
LED8	Power/HDD/Status LED
LED1	2*BYPASS LED
LED2~7	LAN2~7 Link/Act LED
CN1	System FAN
CN2	SATA Power Con
CN3	SIM Card with SLOT1
SATA1.2	SATA Con
DIMM1.2	DDR4 SODIMM
SLOT2	Mini Card Full Function

2.4.1 Power Button Pin Header (CN10)

Pin	Signal	Pin	Signal
1	PWR_SW#	2	GND

2.4.2 System Reset Pin Header (CN11)

Pin	Signal	Pin	Signal
1	Reset#	2	GND

2.4.3 CASEOPEN Pin Header (CN12)

Pin	Signal	Pin	Signal
1	CASEOPEN	2	GND

2.4.4 PS2 Pin Header (CN9)

Pin	Signal	Pin	Signal
1	PS2_KDAT	2	PS2_KCLK
3	GND	4	+V5S
5	PS2_MDAT	6	PS2_MCLK

2.4.5 Digital IO Pin Header (CN8)

Pin	Signal	Pin	Signal
1	Input bit1	2	Output bit1
3	Input bit2	4	Output bit2
5	Input bit3	6	Output bit3
7	Input bit4	8	Output bit4
9	+5V	10	GND

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The FWS-2360 CMOS memory has an integral lithium battery backup for data retention. You have to replace the battery when it finally runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

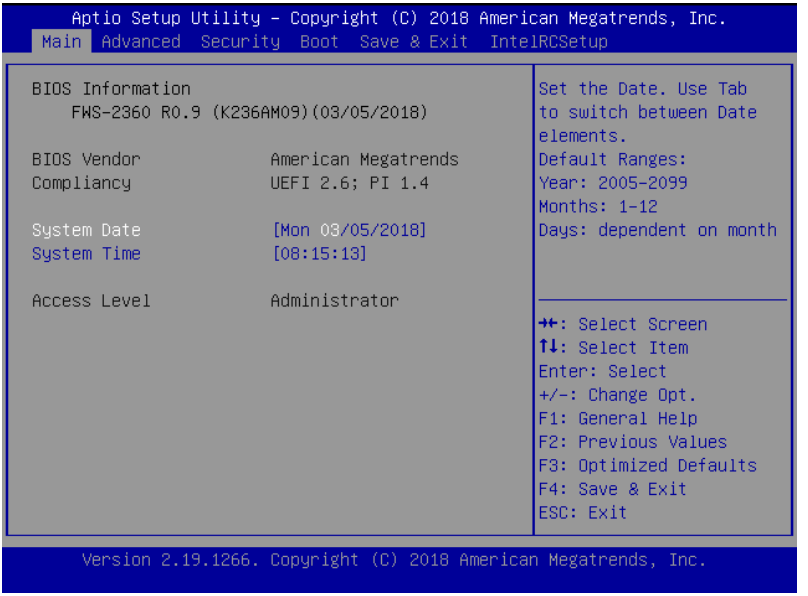
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

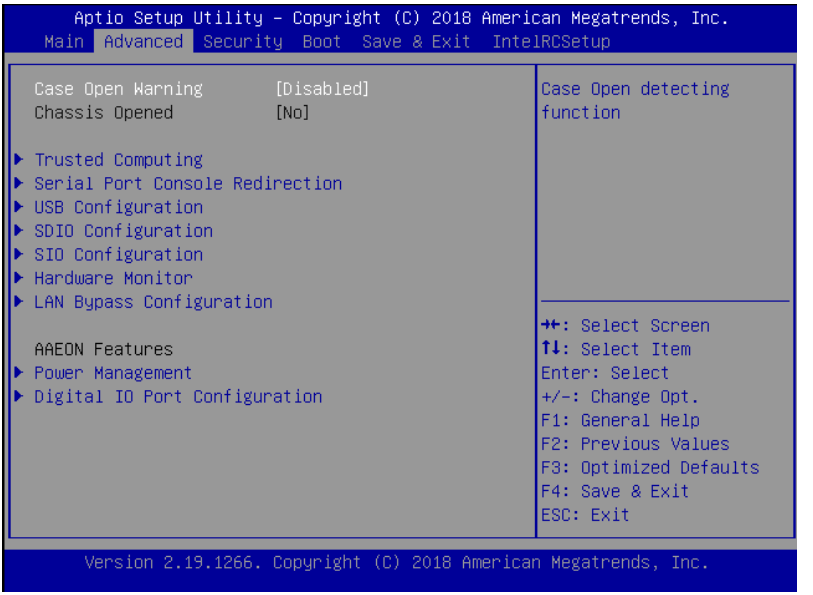
Boot – Enable/ Disable quiet Boot Option

Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main



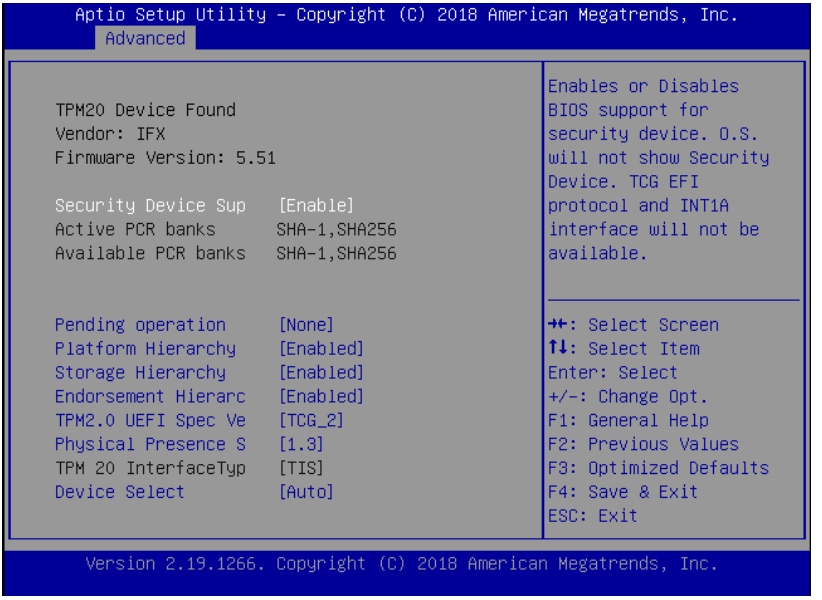
3.4 Setup Submenu: Advanced



Options summary:

Case Open Warning	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Clear	
Case Open detecting function		

3.4.1 Advanced: Trusted Computing

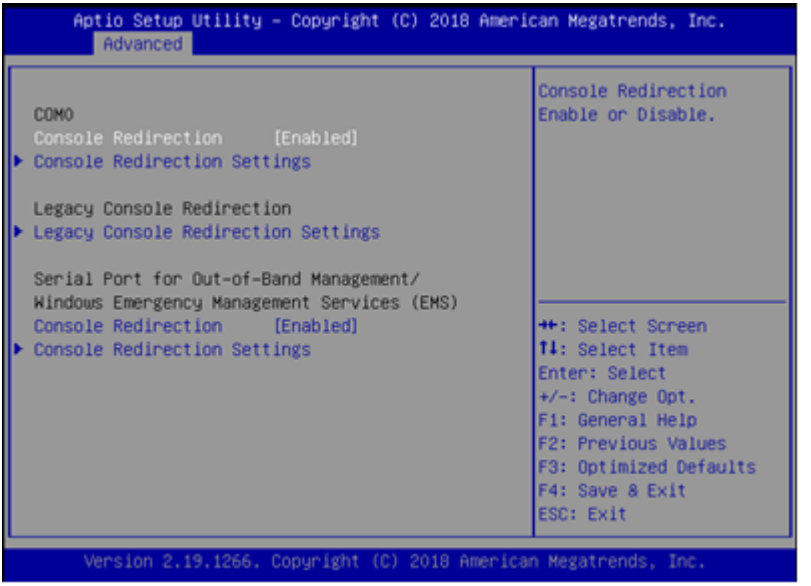


Options summary:

Security Device Sup	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Platform Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		

Storage Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support, TCG_1_2 : the Compatible mode for Win8/Win10 TCG_2 : Support new TCG2 protocol and event		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

3.4.2 Advanced: Serial Port Console Redirection

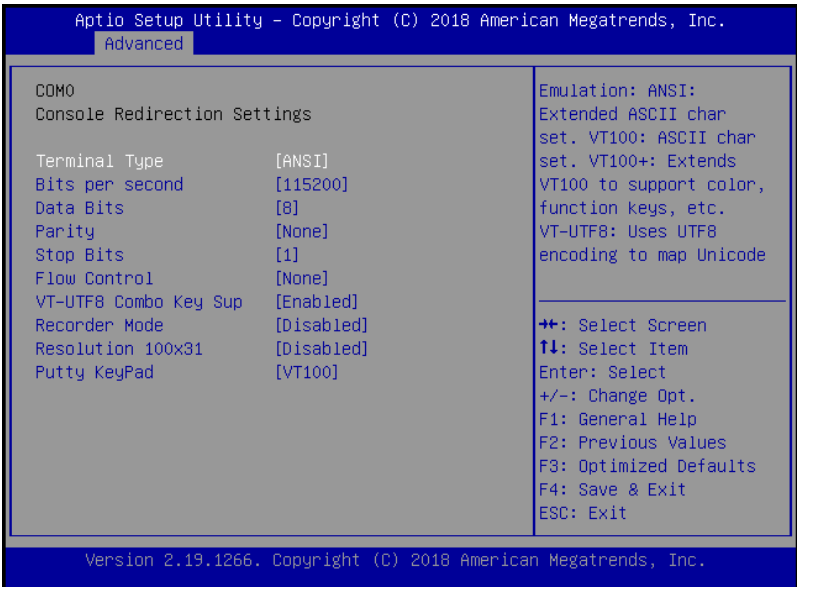


Options summary:

COM0		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		
Console Redirection Settings		
Legacy Console Redirection		
Legacy Console Redirection Settings		
Serial Port for Out-of-Band Management / Windows Emergency Management Services		
Console Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		

Console Redirection Settings

3.4.2.1 COM0 Console Redirection



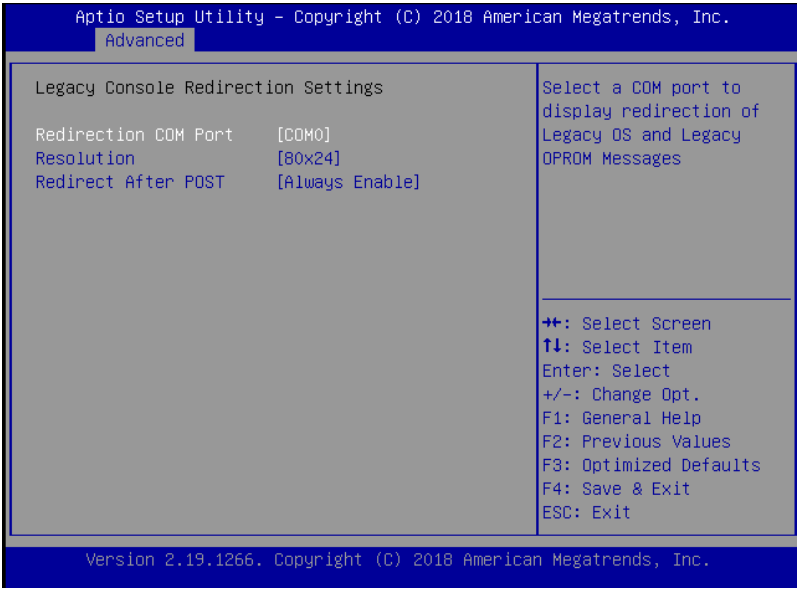
Options summary:

Terminal Type	VT100	
	VY100+	
	VT-UTF8	
	ANSI	Optimal Default, Failsafe Default
Emulation : ANSI : Extended ASCII char set. VT100 : ASCII char set. VT100+ : Extends VT100 to support color, function keys, etc. VT-UTF8 : Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	

	57600	
	11520	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		
Data bit	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default

	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		

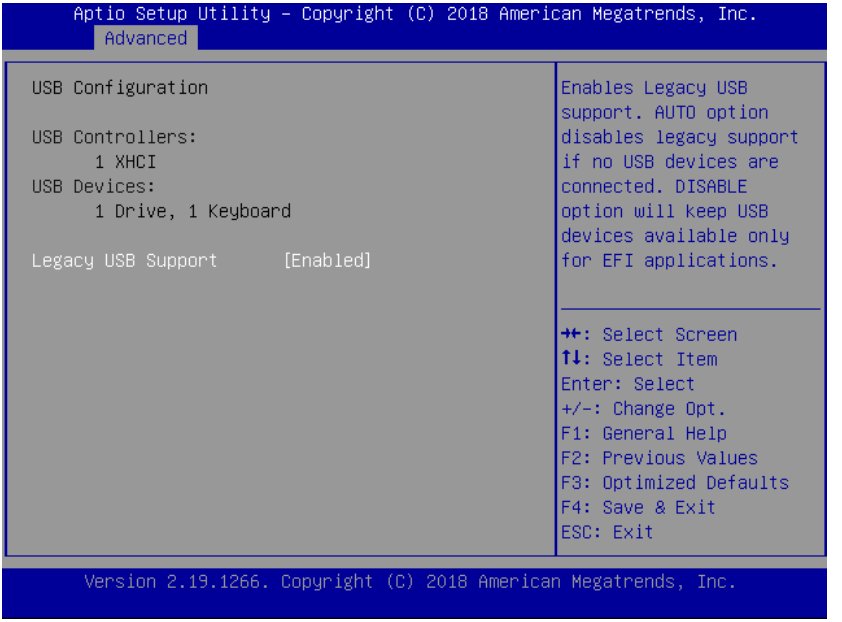
3.4.2.2 Legacy Console Redirection Settings



Options summary:

Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection.		
Redirection After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When BootLoader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is		

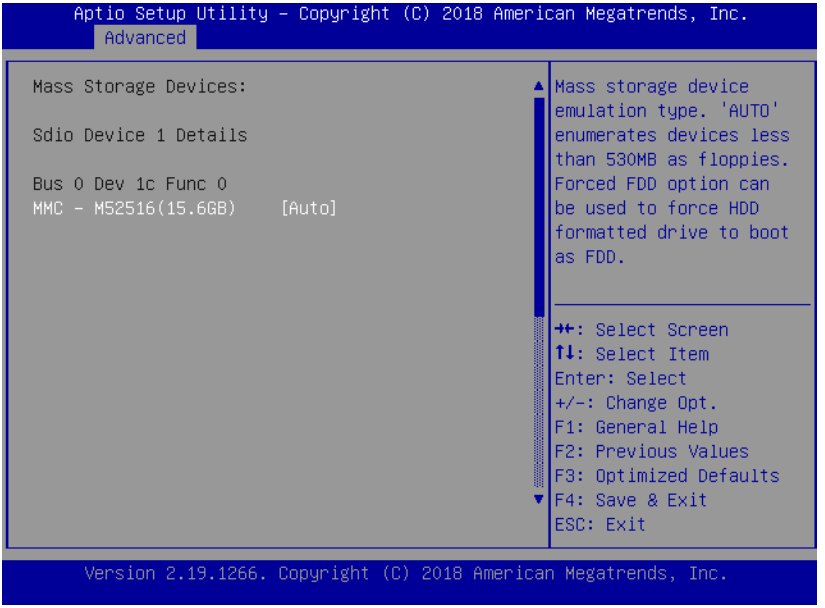
3.4.3 Advanced: USB Configuration



Options summary:

Legacy USB Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

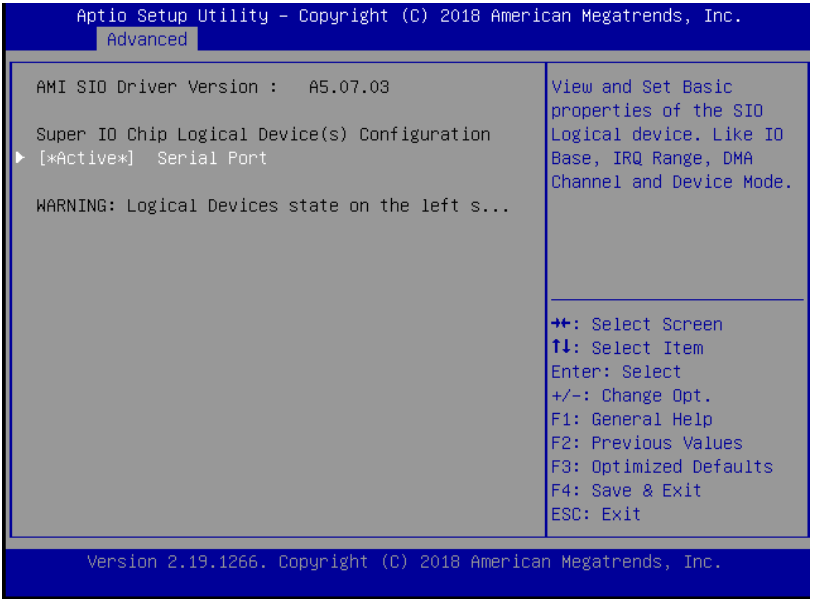
3.4.4 Advanced: SDIO Configuration



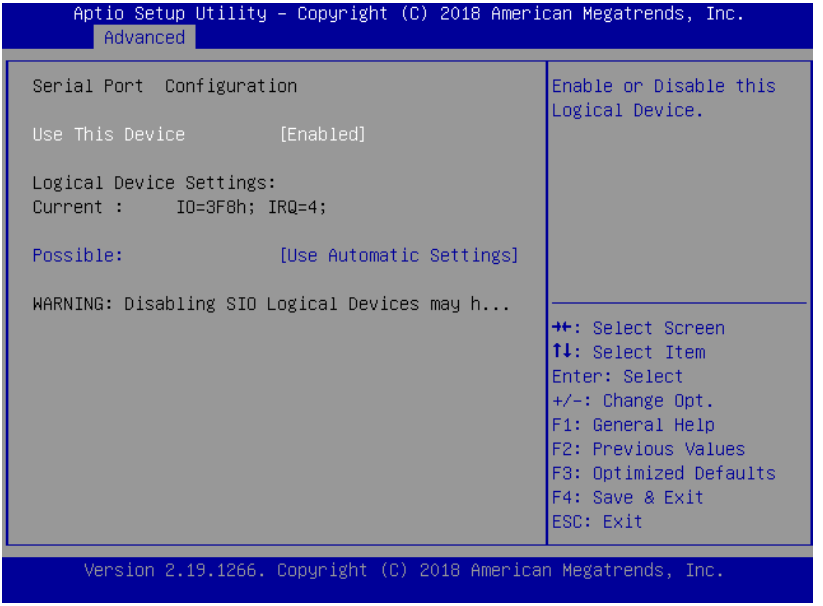
Options summary:

Mass storage device emulation type	Auto	Optimal Default, Failsafe Default
	Floppy	
	Forced FDD	
	Hard Disk	
Mass storage device emulation type. 'AUTO' enumerates devices less than 530MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.		

3.4.5 Advanced: SIO Configuration



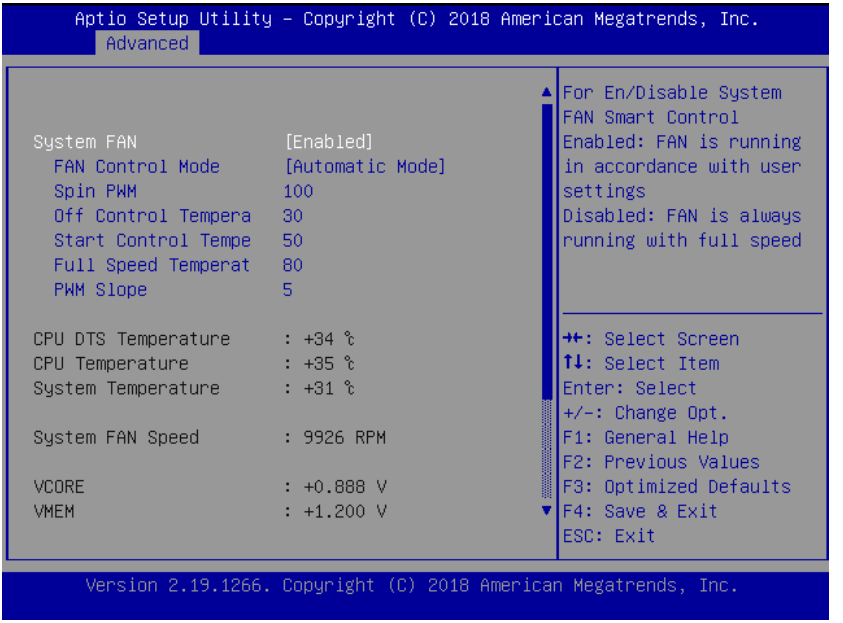
3.4.5.1 SIO Configuration: Serial Port Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.6 Advanced: Hardware Monitor



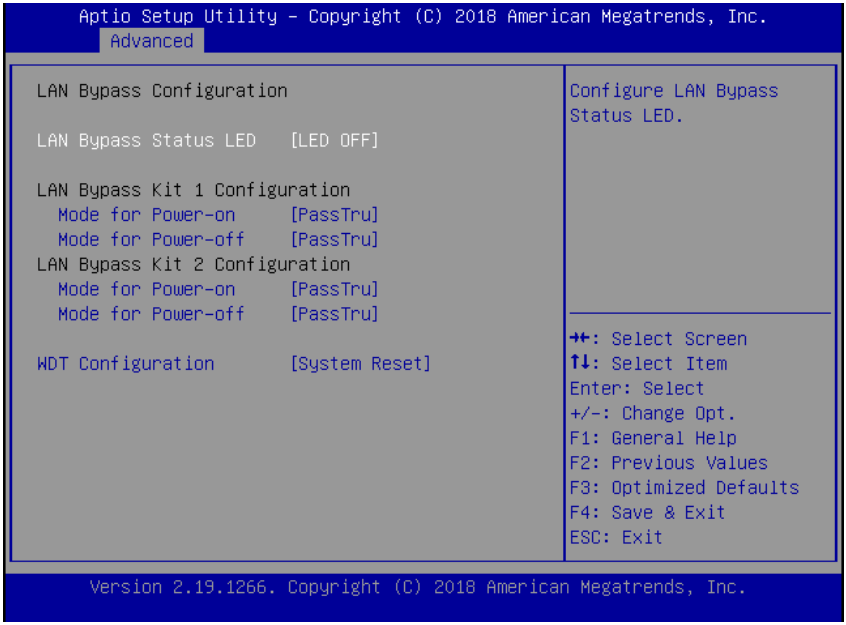
Options summary:

System Fan	Enabled	Optimal Default, Failsafe Default
	Disabled	
For En/Disable System FAN Smart Control\nEnabled: FAN is running in accordance with user settings\nDisabled: FAN is always running with full speed		
FAN Control Mode	Automatic Mode	Optimal Default, Failsafe Default
	Manual Mode	
Manual Mode: Depends on PWM Duty\nAutomatic Mode: FAN Speed is depends on CPU Temperature		
Spin PWM	100	Optimal Default, Failsafe Default
The PWM Duty of FAN Spin\nRange:[0 - 255]		
Off Control Temperature	30	Optimal Default, Failsafe Default

Temperature Limit Value of Fan Off\nNote: Some fans have the minimum speed even if the PWM value is 0		
Start Control Temperature	50	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Start Control		

Full Speed Temperature	80	Optimal Default, Failsafe Default
Temperature Limit Value of FAN Full Speed		
PWM Slope	5	Optimal Default, Failsafe Default
Slope PWM value/Degree C for FAN Speed Control\nRange:[1-15]		

3.4.7 Advanced: LAN Bypass Configuration



Options summary:

Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
LAN Bypass Status LED		
Mode for Power-on	ByPass	
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-on state. (Bypass/Pass Through)		
Mode for Power-off	ByPass	

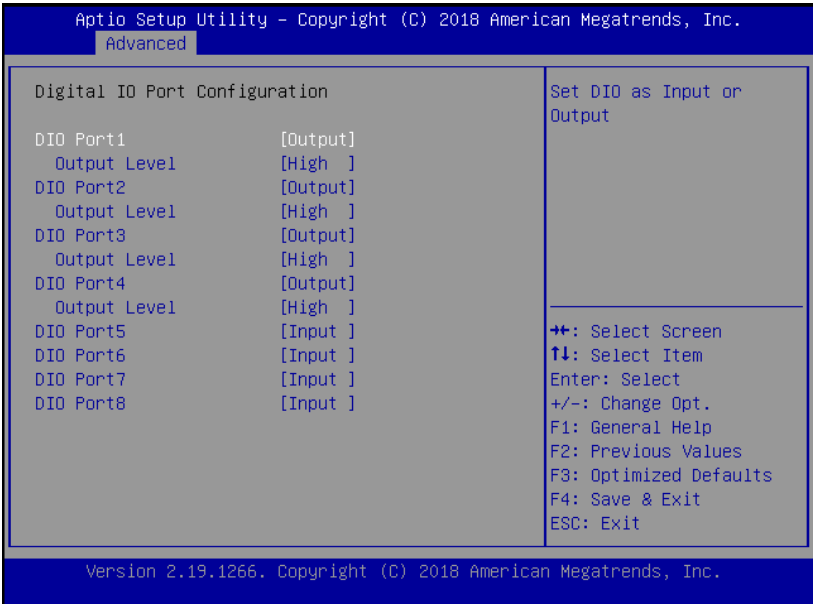
	PassTru	Optimal Default, Failsafe Default
Configure LAN kit behavior when system in power-off state. (Bypass/Pass Through)		
WDT Configuration	System Reset	Optimal Default, Failsafe Default
	Force ByPass	
Configure LAN kit behavior when WDT is triggered. (Bypass/Pass Through)		

3.4.8 Advanced: Power Management

Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time : System will wake on the hr :: min :: sec Specified Dynamic Time : System will wake on the current time + Increase minutes(s).		

3.4.9 Advanced: Digital IO Port Configuration



Options summary:

DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		

3.5 Setup submenu: Security

Change User/Supervisor Password

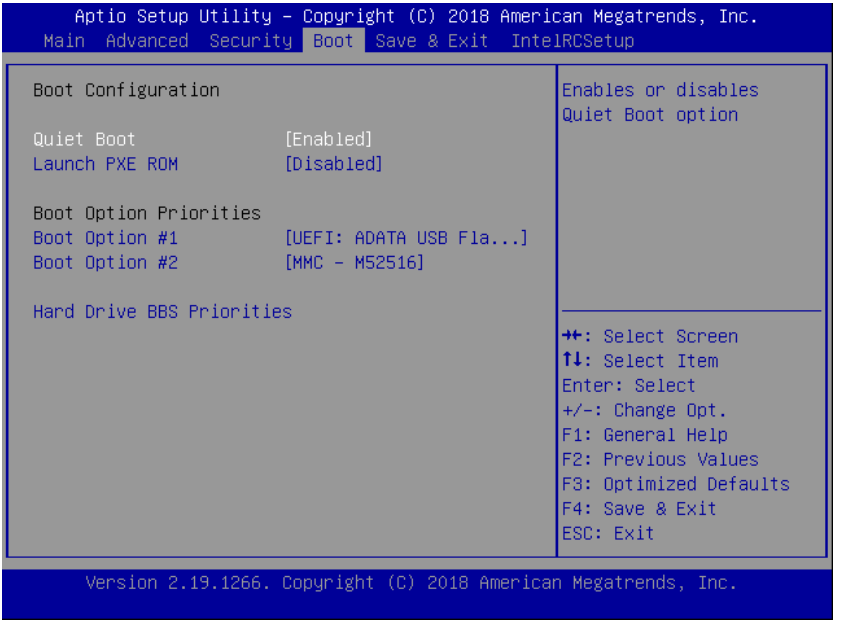
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

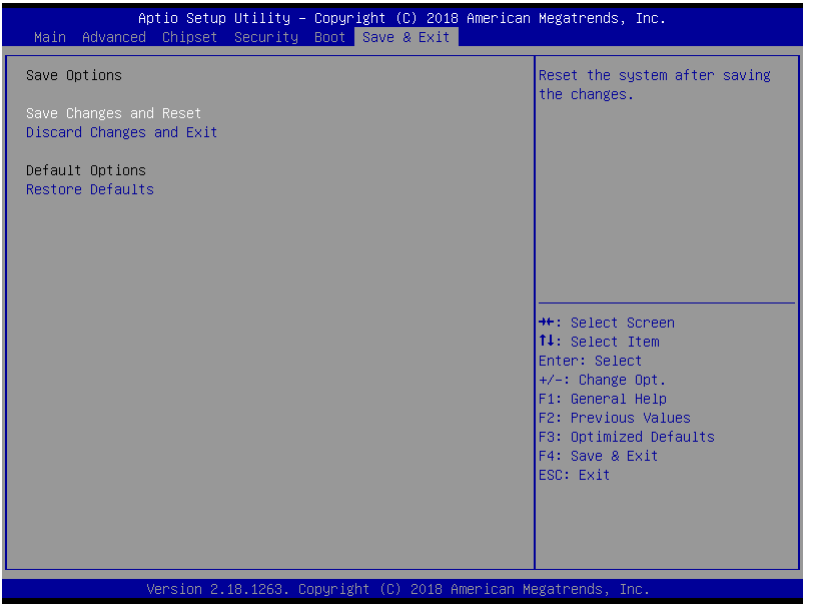
3.6 Setup submenu: Boot



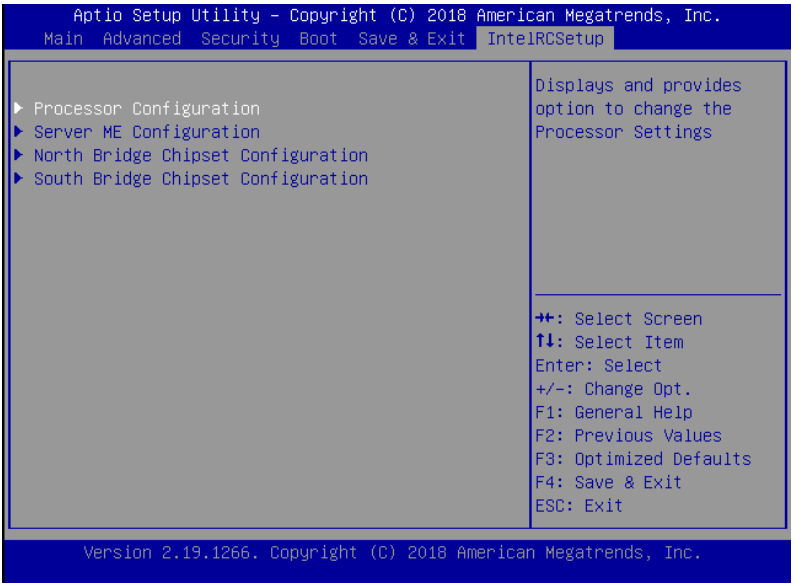
Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
Launch PXE Rom	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		
Boot Option #1	UFEI OS (Lilee System SSM 1GB 0910)	Optimal Default, Failsafe Default
	Disabled	
Sets the system boot order.		

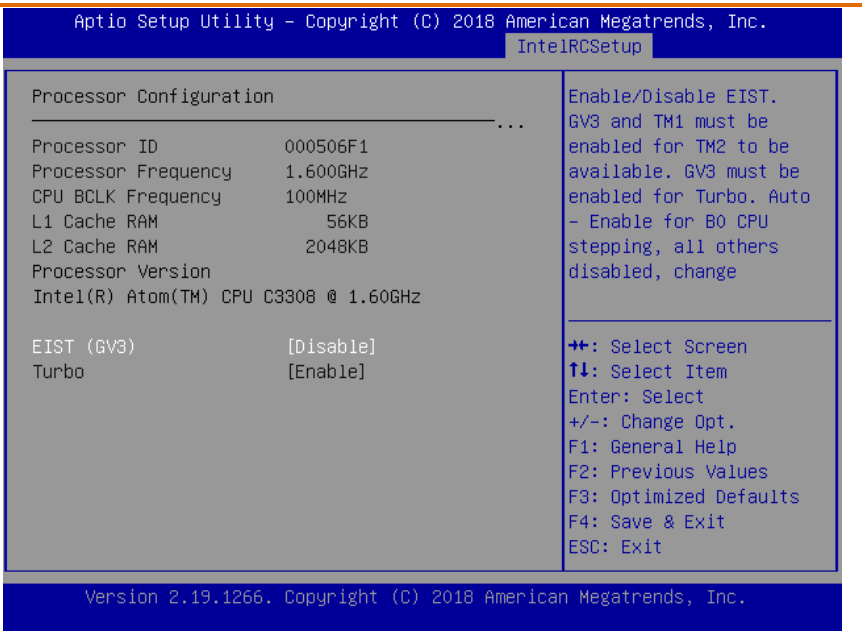
3.8 Setup submenu: Save & Exit



3.9 Setup submenu: IntelRCSetup



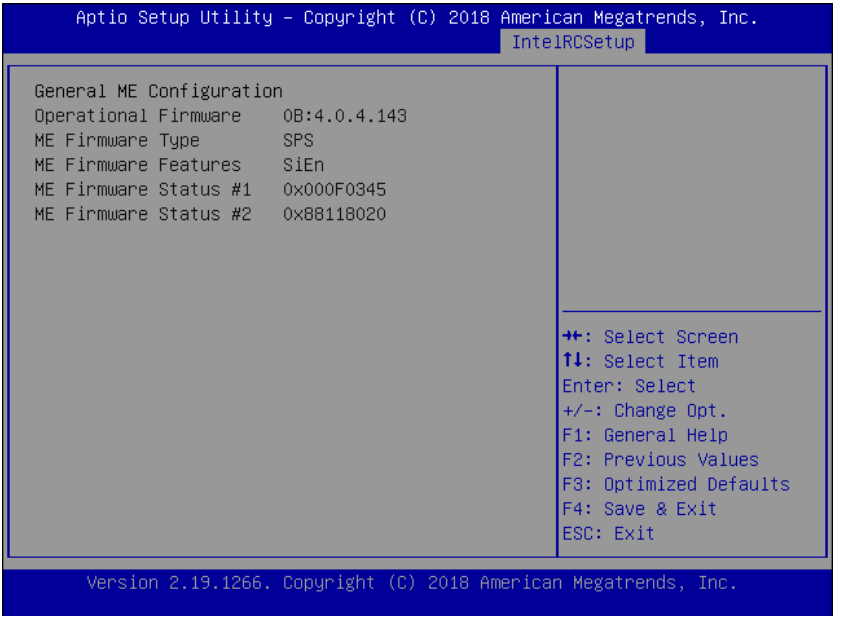
3.9.1 IntelRCSetup: Power Configuration



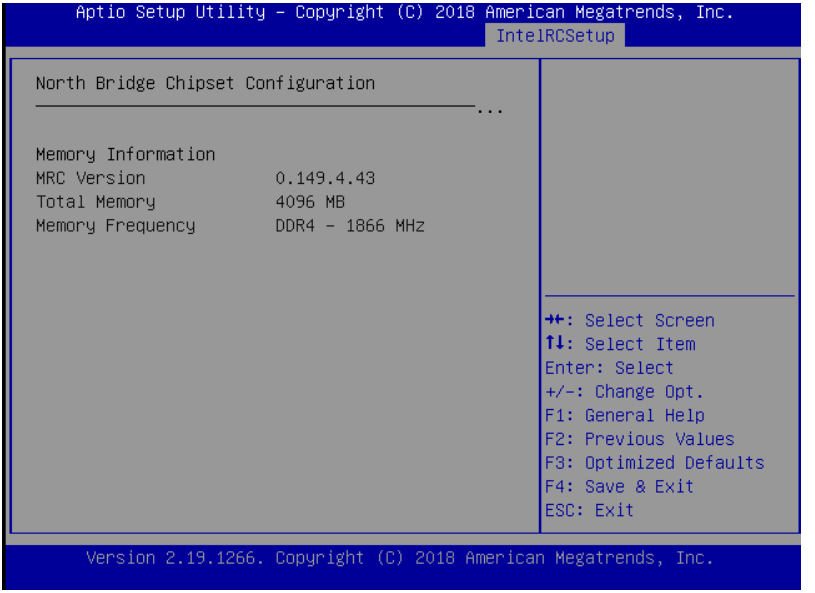
Options summary:

EIST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable EIST. GV3 and TM1 must be enabled for TM2 to be available. GV3 must be enabled for Turbo. Auto - Enable for B0 CPU stepping, all others disabled, change setting to override.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable CPU Turbo capability. This option only applies to ES2 and above.		

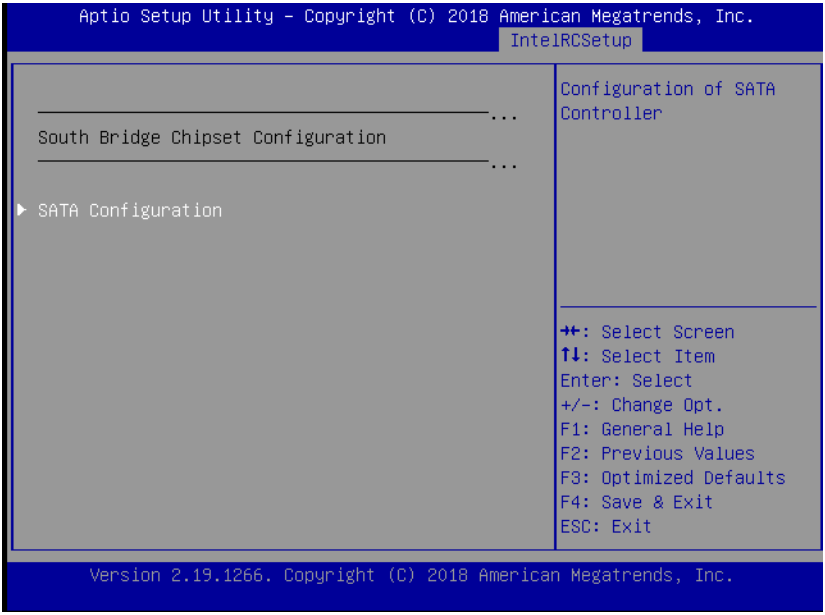
3.9.2 IntelRCSetup: Server ME Configuration



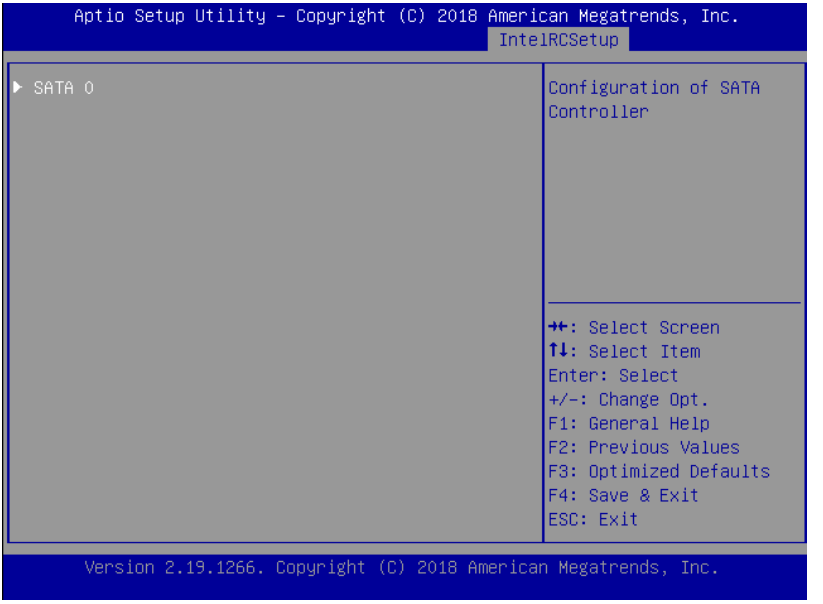
3.9.3 IntelRCSetup: North Bridge Chipset Configuration



3.9.4 IntelRCSetup: South Bridge Chipset Configuration



3.9.4.1 South Bridge Chipset Configuration: SATA Configuration

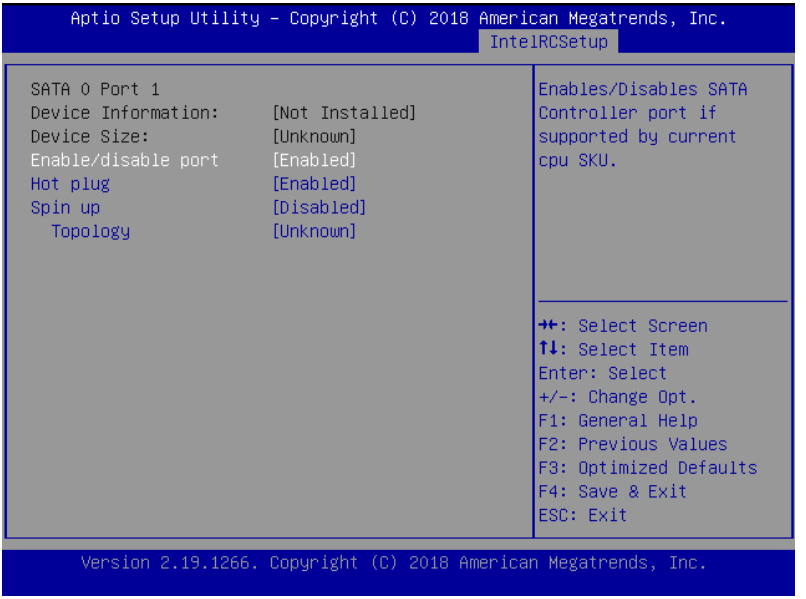


3.9.4.1.1 SATA Configuration: SATA 0

Options summary:

Enable controller	Enabled	Optimal Default, Failsafe Default	
	Disabled		
Enable or disable the Chipset SATA Controller. The Chipset SATA Controller support the 2 black internal SATA ports (up to 3Gb/s supported per port).			Enables/Disables SATA Controller if supported by current cpu SKU.

3.9.4.1.1.1 SATA 0: Port 1



Options summary:

Enable/disable port	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables/Disables SATA Controller port if supported by current cpu SKU.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Hot Plug		
Spin up	Disabled	Optimal Default, Failsafe Default
	Enabled	
Spin up		
Topology	Unknown	Optimal Default, Failsafe Default
	ISATA	
	Direct Connect	

	Flex	
	M2	
Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2.		

Chapter 4

Driver Installation

4.1 Driver Installation

Please download the driver from the AAEON website - http://www.aaeon.com/en/p/desktop-network-appliance-fws-2360. It contains all the drivers and utilities you need to set up your product. Follow the steps below to install the drivers.

For Windows:

Step 1 – Open the Step 1 – LAN\22_4_0_1_CD folder

Step 2 – Double click Autorun.exe

For Linux:

Step 1 – Open the Step 1 – LAN\22_4_0_1_CD\PROXGB\LINUX folder

Step 2 – Double click ixgbe-5.1.3.tar.gz

Step 3 – Follow the README instructions

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte    SIOIndex    //This parameter is represented from Note1
#define byte    SIOData    //This parameter is represented from Note2
#define    void    IOWriteByte(byte IOPort, byte Value);
#define    byte    IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte    TimerLDN    //This parameter is represented from Note3
#define byte    TimerReg    //This parameter is represented from Note4
#define byte    TimerVal    // This parameter is represented from Note24
#define byte    UnitLDN    //This parameter is represented from Note5
#define byte    UnitReg    //This parameter is represented from Note6
#define byte    UnitBit    //This parameter is represented from Note7
#define byte    UnitVal    //This parameter is represented from Note8
#define byte    EnableLDN    //This parameter is represented from Note9
#define byte    EnableReg    //This parameter is represented from Note10
#define byte    EnableBit    //This parameter is represented from Note11
#define byte    EnableVal    //This parameter is represented from Note12
#define byte    StatusLDN    // This parameter is represented from Note13
#define byte    StatusReg    // This parameter is represented from Note14
#define byte    StatusBit    // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ( ){
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig ( ){
// Disable WDT counting
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
// Clear Watchdog Timeout Status
WDTClearTimeoutStatus();
// WDT relative parameter setting
WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
// Watchdog Timer counter setting
SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID    WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************
```

```
*********************************************************************************
OID    SIOEnterMBPnPMode(){
        Switch(SIOIndex){
                Case 0x2E:
                        IOWriteByte(SIOIndex, 0x87);
                        IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0x55);
Break;
                Case 0x4E:
                        IOWriteByte(SIOIndex, 0x87);
                        IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0xAA);
                        Break;
        }
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0x02);
        IOWriteByte(SIOData, 0x02);
}

VOID    SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}
*********************************************************************************
```

```
*****************************************************************************
VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
IOWriteByte(SIOData, Value);
SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

Standard LAN Bypass Platform Setting

B.1 Status LED

B.1.1 Introduction

FWS-2360 provides a LED indicator which can change the LED status by AAEON SDK.

User is able to program the LED status to express different status.

B.1.2 Status LED Configuration

Table1: LED Status

STA_LED2	STA_LED1	STA_LED0	LED States
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table2: Status LED relative register mapping table

	CPLD Slave Address 0x90 (Note1)			
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

B.1.3 Sample Code

```
*****************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*****************************************************************************************
*****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
```

```
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*********************************************************************************************
*****
```

B.2 LAN Bypass

B.2.1 Introduction

FWS-2360 provides LAN Bypass kit and allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

B.2.1 LAN Bypass Configuration

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table2: LAN Bypass relative register table

Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass relative register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

B.2.3 Sample Code

```
*****************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*****************************************************************************************
*****
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;


BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
```

```
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xBF;
else                                    // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
        bData = bData & 0xEF;
else                            // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
```

```
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*********************************************************************************
```

B.3 Software Reset Button (General Propose Input)

B.3.1 Introduction

FWS-2360 provides a general propose input button which status get by AAEON SDK.

B.3.2 Soft Reset Button Configuration

Table 2: LAN Bypass relative register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low 1: Pin Level States High

Table 1 : Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

B.3.3 Sample Code

```
*****************************************************************************
#define Word        BTN_STS        //This parameter is represented from Note1
#define ByteBTN_STS_R              //This parameter is represented from Note2
*****************************************************************************
Byte    GET_Value (Word IoAddr, Byte BitNum,Byte Value){
        BYTE  TmpValue;

        TmpValue = inportb (IoAddr);
return    (TmpValue & (1 << BitNum))
}
*****************************************************************************
VOID    Main(){
        Byte RstBtn;

        RstBtn = GET_Value (BTN_STS, BTN_STS_R);  // Active Low
}
*****************************************************************************
```