FWS-2280

Desktop Network Appliance

User Manual 2nd Ed

Last Updated: August 27, 2021

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2280	1
● 2.5" SSD Bay	1
● SATA Cable	1
● SATA Power Cable	1
● Power Adapter	1
● System Rubber Foot	4

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

18. If any of the following situations arises, please the contact our service personnel:

    i. Damaged power cord or plug

    ii. Liquid intrusion to the device

    iii. Exposure to moisture

    iv. Device is not working as expected or in a manner as described in this manual

    v. The device is dropped or damaged

    vi. Any obvious signs of damage displayed on the device

19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚(PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注:

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

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Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Desktop Network Appliance
Processor	Intel Elkhart lake SoC Processor 2~4 cores
Chipset	SoC
System Memory	260-pin DDR4 SO-DIMM x 1 3200MHz

Network	
Ethernet	Intel® i211, Gigabit Ethernet x 4
	Intel® i210, SFP x 1
Bypass	—

Display	
Graphic Controller	Intel® UHD Graphics
Connector	HDMI x 1

Storage	
HDD	—
CF/CFast/mSATA	mSATA slot x 1
	SATA III port x 1

Internal/Expansion Interface

PCIe Slot	—
Mini-PCIe Slot	Mini Card Socket (PCIe + USB 2.0, full size) with SIM x 1 Mini Card Socket (PCIe, half size) x 1 M.2 B key 3052 (USB 3.0, full size) with SIM x 1 (Optional)
Keyboard and Mouse	—
USB	USB2.0 Type A x 2

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	GPIO Programmable push button x 1
TPM	(TPM SLB9670 VQ2.0 FW7.85 Optional)
GPIO	(4 bits input, 4bits output optional)
Fan	Fan-less
MTBF (Hours)	TBD
Color	Black

Physical & Environmental

Power Requirement	2 x 12V DC Power Input Connector Lockable, 40W power adapter
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz / operation (SSD)

Physical & Environmental

	1.5 Grms/ 5 ~ 500Hz / non-operation
Shock	10 G peak acceleration (11 m sec. duration), operation
	20 G peak acceleration (11 m sec. duration), non-operation
Dimension (W x D x H)	8.27" x 4.09" x 1.73" (210mm x 105mm x 44mm)

I/O

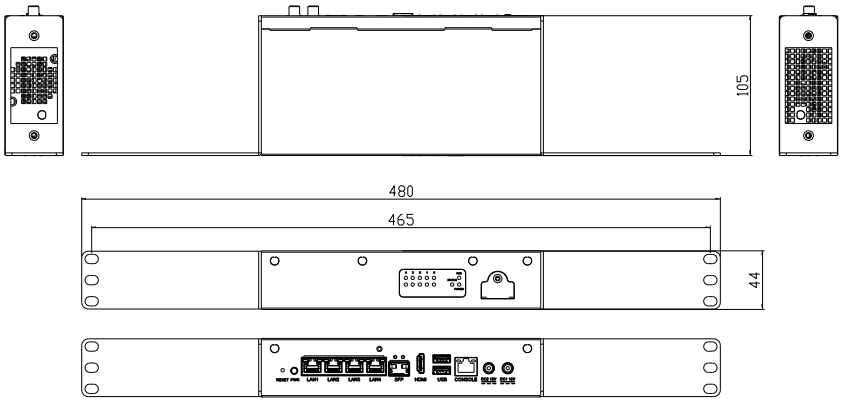
Front Panel	3 x LEDs (Power, Status, Storage)
	1 x Micro-SIM
	2 x Antenna Holes
Rear Panel	2 x DC Power Input Connector Lockable
	1 x Power Button
	2 x USB2.0 Ports
	4 x 1.0Gbps RJ45 Ports
	1 x SFP
	1 x RJ-45 Console
	1 x Reset Button
	3 x Antenna Holes

Chapter 2

Hardware Information

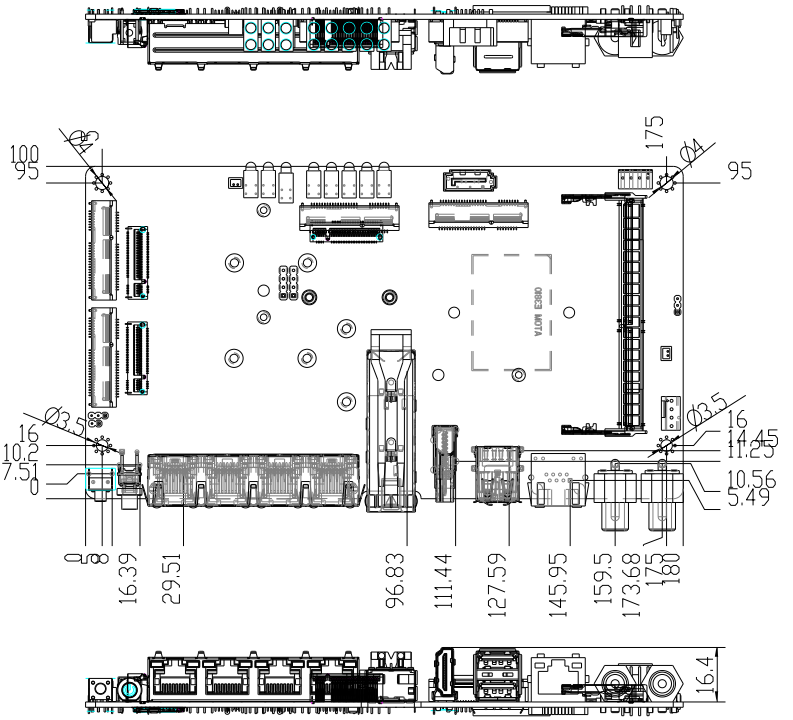
2.1 Dimensions

System

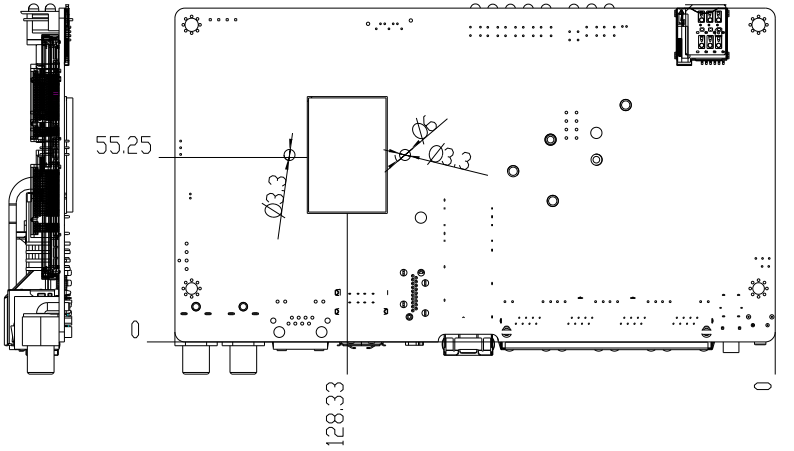


Board

Top and I/O View



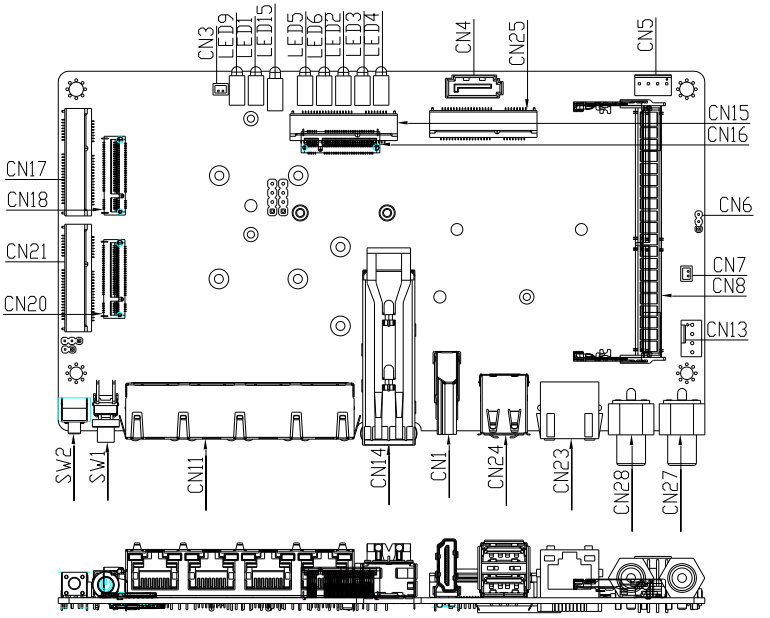
Bottom and Side View



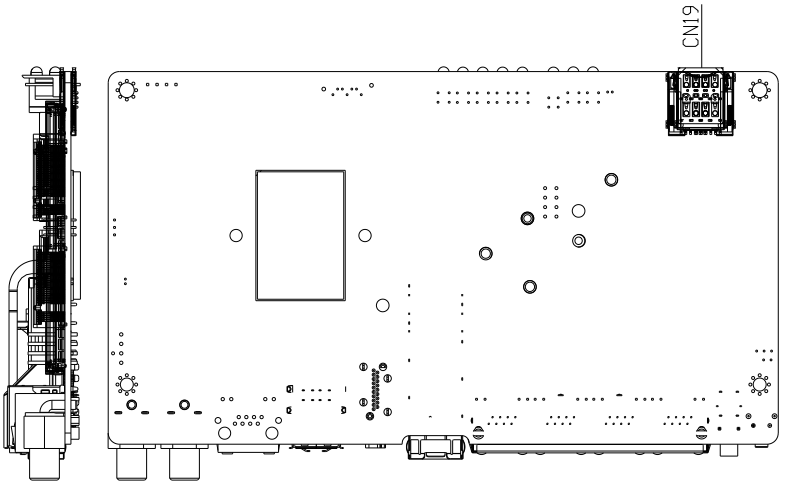
2.2 Jumpers and Connectors

Note: Components and their locations may vary depending upon which configuration was purchased. If you have questions about your FWS-2280, visit our website to contact an AAEON support representative.

Top and I/O View



Bottom and Side View

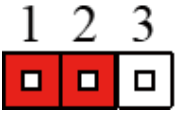


2.3 List of Jumpers

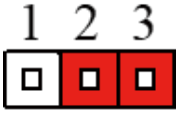
Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CN6	Clear CMOS
JP1	Auto Power Button Selection

2.3.1 Clear CMOS (CN6)

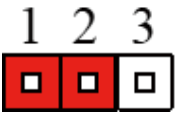


Normal **(Default)**

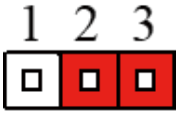


Clear CMOS

2.3.2 Auto Power Button Selection (JP1)



Don't use Auto Power Button **(Default)**



Use Auto Power Button

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application. (Optional) denotes a component that is not included on the standard configuration. Some optional components may replace standard components. Contact AAEON support if you have any questions about the configuration of your FWS-2280 system.

Label	Function
CN1	HDMI Connector
CN4	SATA Connector
CN5	SATA Power Connector (only +5V)
CN10	LAN Ports 1 thru 4 RJ45
CN14	LAN Port 5 SFP
CN13	Fan Connector
CN15/CN16	Mini PCIe / M.2 E-Key (co-lay option) only PCIe function
CN17/CN18	Mini PCIe / M.2 E-Key (co-lay option) only PCIe function
CN19	Micro SIM for CN17/CN18
CN20/CN21	Mini PCIe / M.2 B-Key (co-lay option) only USB3.0 function
CN22	Micro SIM for CN21/CN20
CN23	Serial Port1
CN24	Dual USB2.0 Connector
CN25	mSATA Slot
CN27	Redundant DC-INPUT1 (12V)
CN28	Redundant DC-INPUT2 (12V)
CN30	DIO Connector
SW1	Power Button
SW2	Software Reset

2.4.1 SATA Power Connector (CN5)

Pin	Signal	Pin	Signal
1	NC	2	GND
3	GND	4	+5V

2.4.2 Digital IO Connector (CN30)

Pin	Signal	Signal Type
1	DIO0	Input/ Output
2	DIO1	Input/ Output
3	DIO2	Input/ Output
4	DIO3	Input/ Output
5	DIO4	Input/ Output
6	DIO5	Input/ Output
7	DIO6	Input/ Output
8	DIO7	Input/ Output
9	+3.3V	PWR
10	GND	GND

2.4.3 Switch GPIO Mapping (SW2)

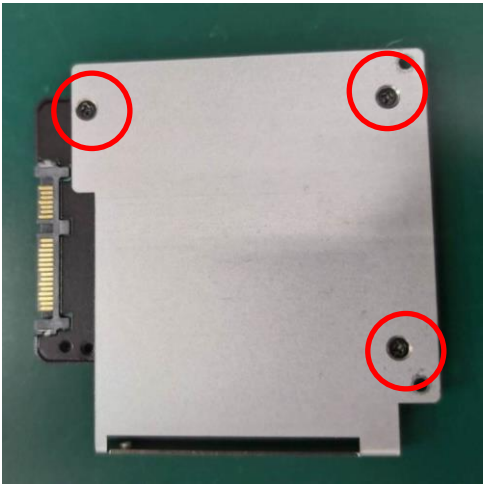
SW2 GPIO Mapping
Mapping SIO GP64

2.5 2.5″ SATA Drive Installation

This section details how to install a 2.5″ SATA Drive (SSD) for your FWS-2280. If you have any questions or are unsure about your system's specifications, refer to Chapter 1 or contact an AAEON representative be visiting the support page on our webite.

Step 1: Remove the top cover by first removing the two screws which secure it to the bottom chassis, then sliding the bottom chassis as shown.

Step 2: Mount the SATA drive to the drive bracket and secure with three screws.



Step 3: Insert the bracket into the system, being careful to line the bracket up with the post on the chassis as shown:

Step 4: Secure the drive bracket to the standoffs with two screws:

Step 5: Connect the SATA and SATA Power Cables to the SATA drive.

Step 6: Reattach the top panel, making sure to replace the screws removed in Step 1

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or display an error message. The system can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the system will load the default configuration and reboot automatically.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The system configuration was reset by the Clear CMOS jumper
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <Esc> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access hardware monitor and advanced board features and options

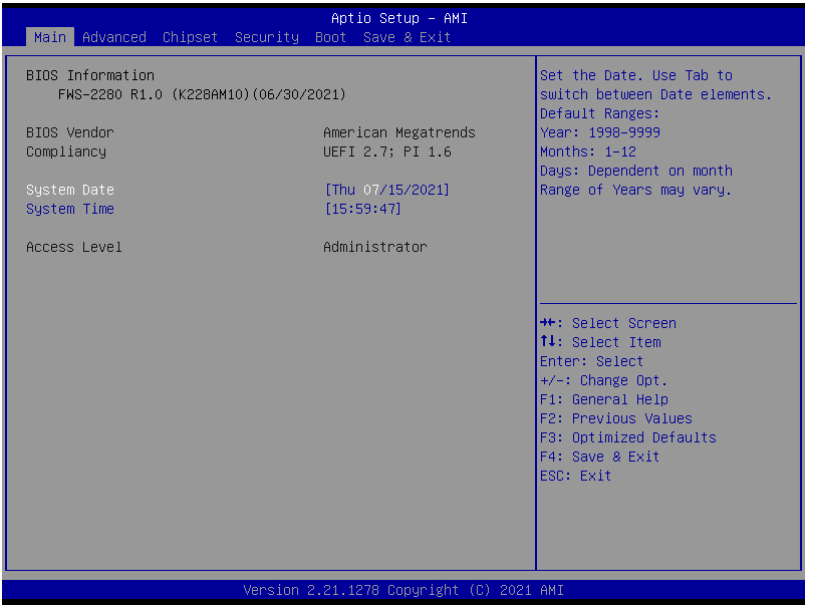
Chipset - Chipset settings and options

Security – The setup administrator password can be set here

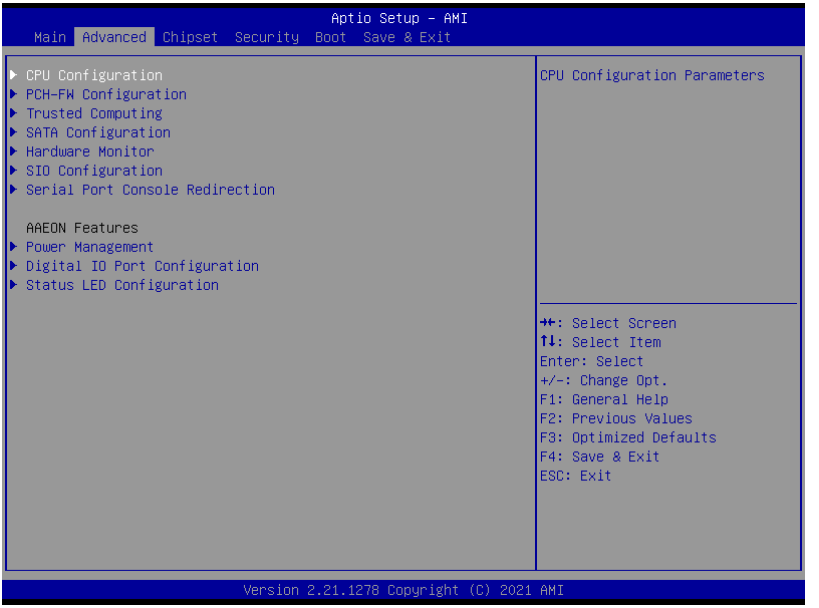
Boot – Set boot drive priority and quiet boot options

Save & Exit – Save changes and exit the program

3.3 Setup Submenu: Main



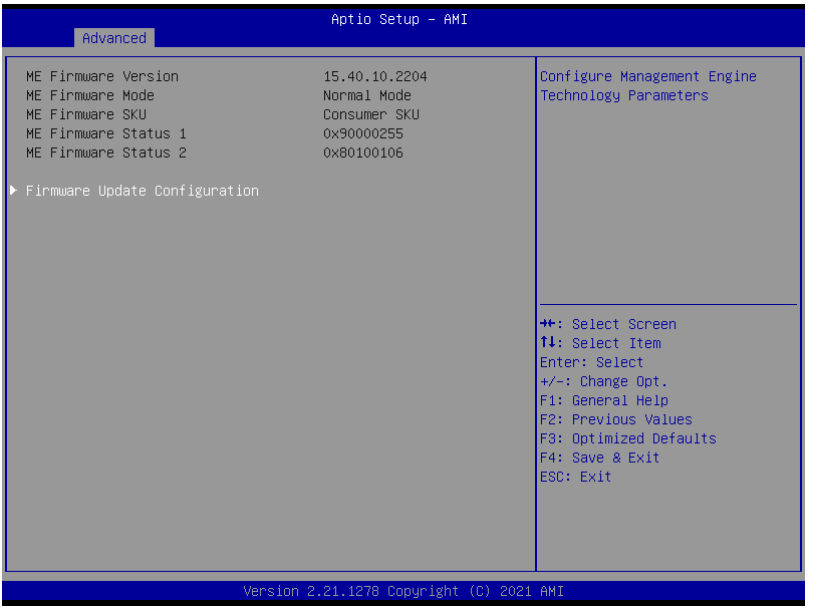
3.4 Setup Submenu: Advanced



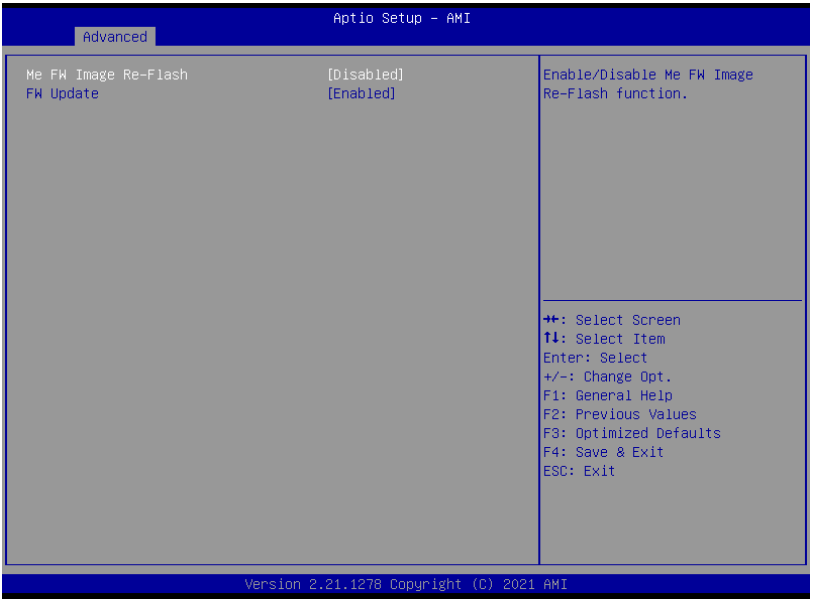
3.4.1 CPU Configuration

Options Summary		
Active Processor Cores	All	Optimal Default; Failsafe Default
	1~N	
Number of cores to enable in each processor package.		

3.4.2 PCH-FW Configuration



3.4.2.1 Firmware Update Configuration



Options Summary		
Me FW Image Re-Flash	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.3 Trusted Computing

Options Summary		
Security Deice Support	Enable	Optimal Default, Failsafe Default
	Disable	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA256 PCR Bank.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

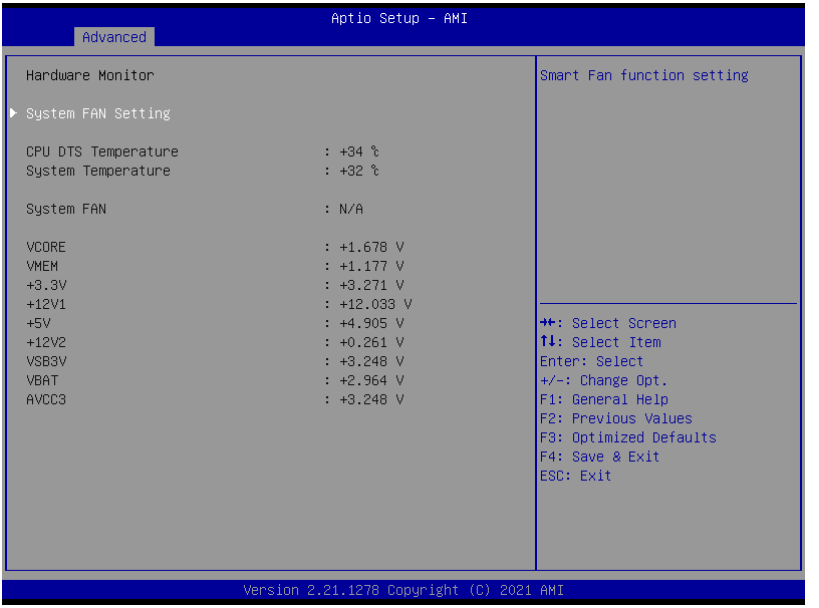
Table Continues on Next Page

Options Summary		
Platform Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Endorsement Hierarchy		
TPM 2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCH2 Spec Version Support. TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.3	Optimal Default, Failsafe Default
	1.2	
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3		
Device Select	Auto	Optimal Default, Failsafe Default
	TPM 1.2	
	TPM 2.0	
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.		

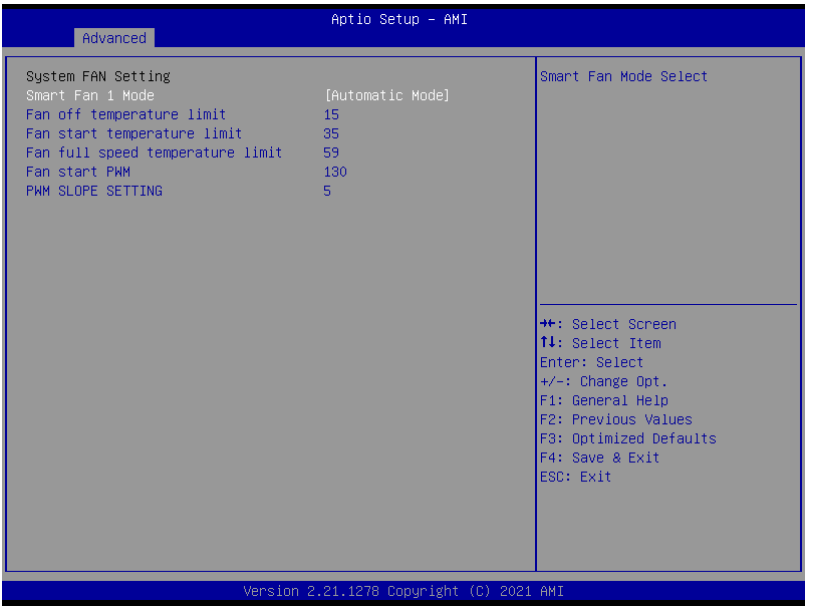
3.4.4 SATA Configuration

Options Summary		
SATA Controller(s)	Enabled	Optimal Default; Failsafe Default
	Disabled	
Enable/ Disable SATA Device		

3.4.5 Hardware Monitor



3.4.5.1 System FAN Setting

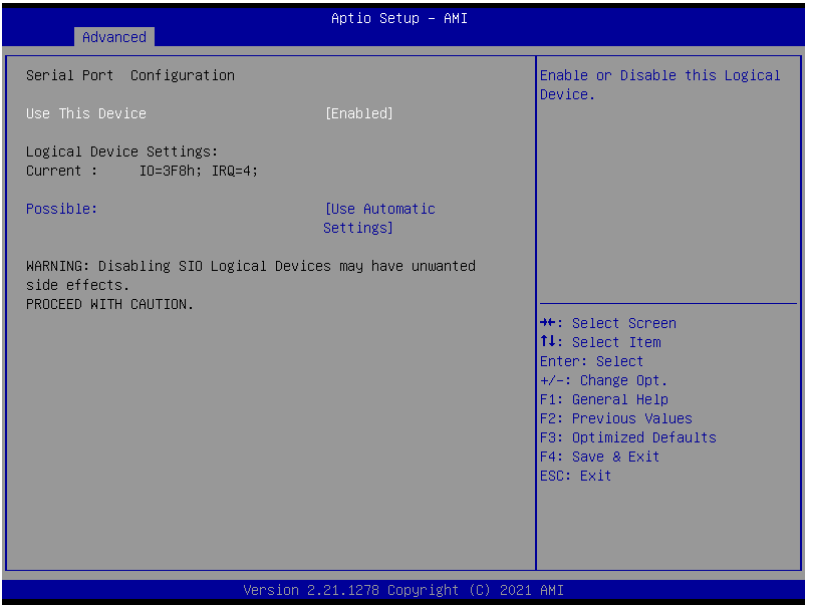


Options Summary		
Smart Fan 1 Mode	Software Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Manual PWM Setting	127	Optimal Default, Failsafe Default
	0~255	
Manual Mode: Fan will work with this Manual PWM Value		
Fan off temperature limit	15	Optimal Default, Failsafe Default
Fan will off when temperature lower than this limit		
Fan start temperature limit	35	Optimal Default, Failsafe Default
Fan will work when temperature higher than this limit		
Fan full Speed Temperature limit	59	Optimal Default, Failsafe Default
Fan will full speed when temperature higher than this limit		

Options Summary		
Fan start PWM	130	Optimal Default, Failsafe Default
Fan will start with this PWM value		
PWM SLOPE SETTING	5	Optimal Default, Failsafe Default
PWM SLOPE Selection Slope = PWM value/℃		

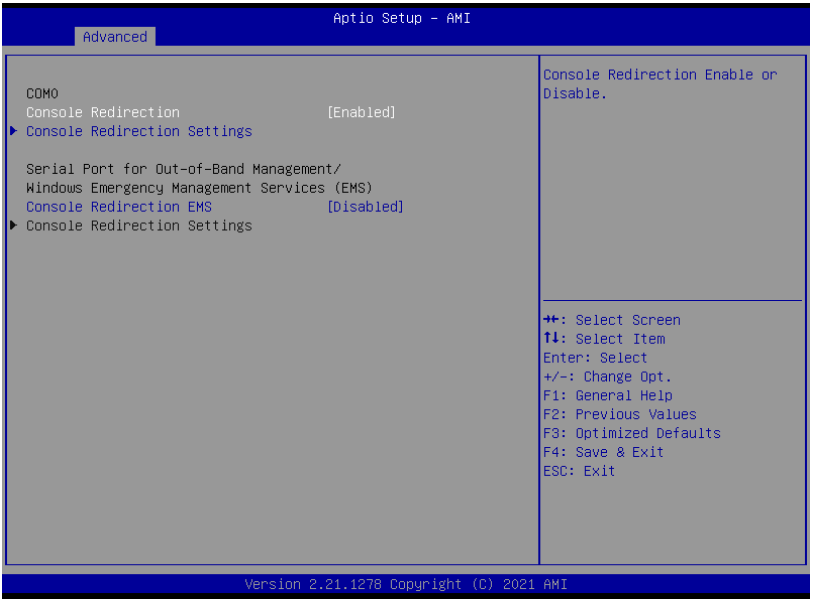
3.4.6 SIO Configuration

3.4.6.1 Serial Port Configuration



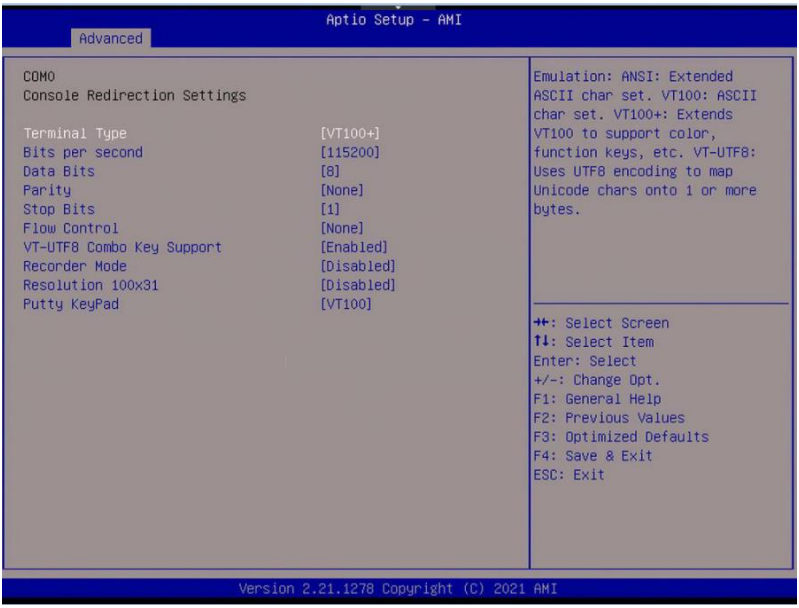
Options Summary		
Use This Device	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable this Logical Device.		
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.4.7 Serial Port Console Configuration



Options Summary		
Console Redirection	Enabled	Optimal Default, Failsafe Default
	Disabled	
Console Redirection Enable or Disable.		
Console Redirection Settings		
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.		
Console Redirection EMS	Enabled	
	Disabled	Optimal Default, Failsafe Default
Console Redirection Enable or Disable.		

3.4.7.1 COM0 Console Redirection Settings

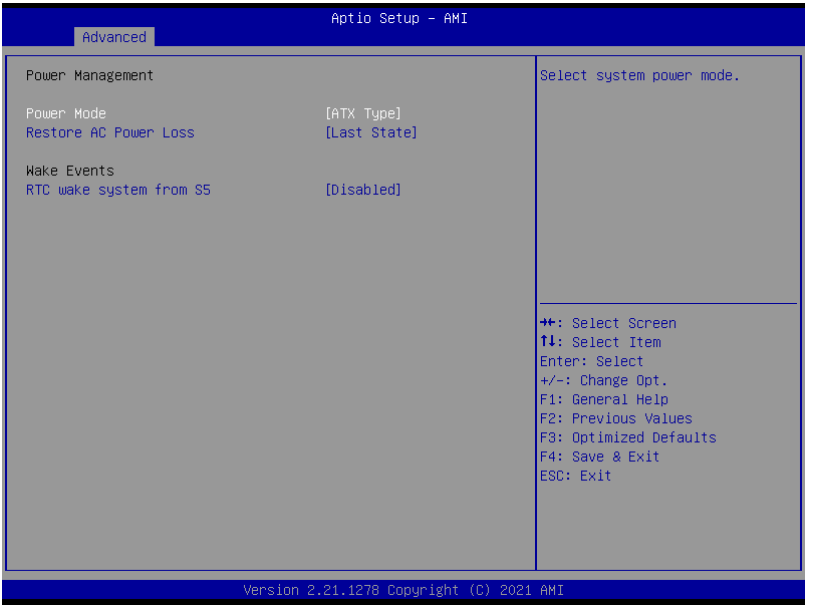


Options Summary		
Terminal Type	VT100	
	VT100+	Optimal Default, Failsafe Default
	VT-UTF8	
	ANSI	
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Options Summary		
Data bit	7	
	8	Optimal Default, Failsafe Default
Data Bits		
Parity	None	Optimal Default, Failsafe Default
	Even	
	Odd	
	Mark	
	Space	
A Parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.		
Stop Bits	1	Optimal Default, Failsafe Default
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may.		
Flow control	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.		
Recorder Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables extended terminal resolution.		
Putty KeyPad	VT100	Optimal Default, Failsafe Default
	LINUX	
	XTERMR6	
	SCO	
	ESCN	

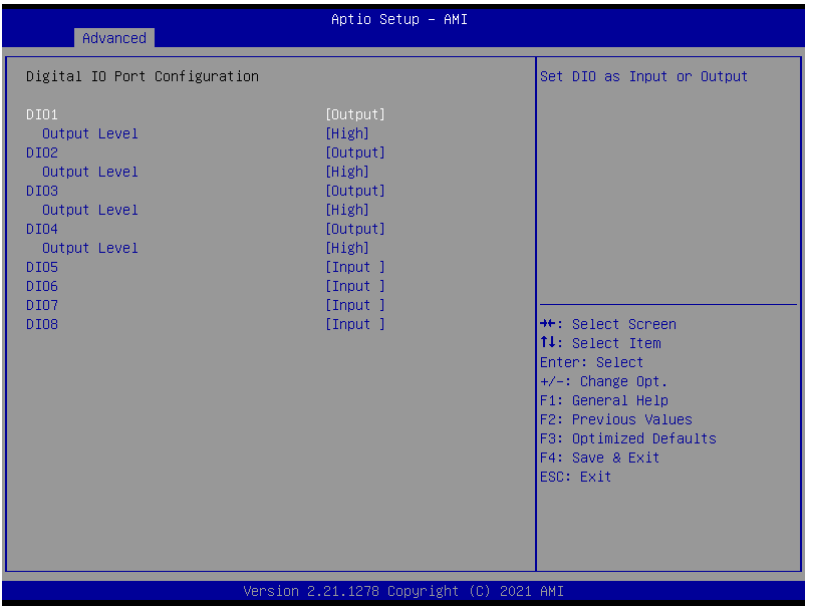
Options Summary		
	VT400	
Select FunctionKey and KeyPad on Putty.		

3.4.8 Power Management



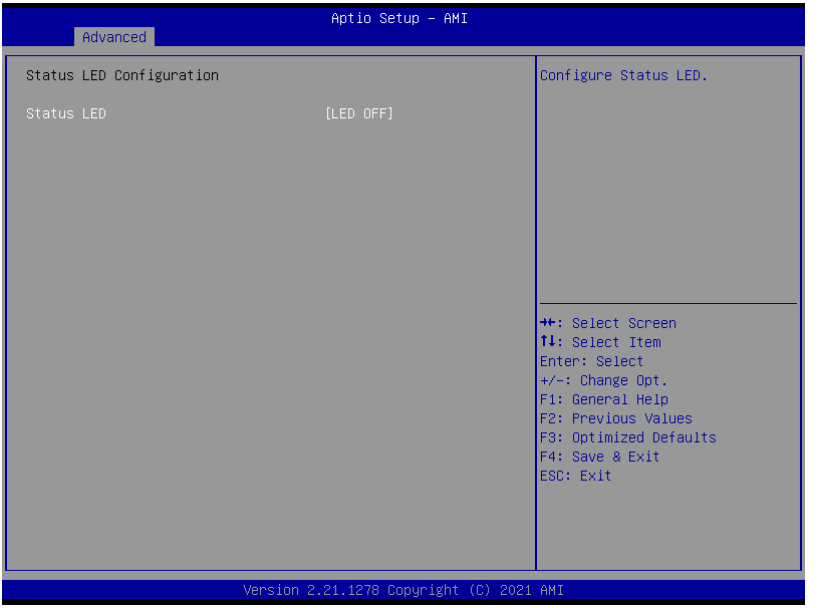
Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
	Bypass	
Fixed Time : System will wake on the hr :: min :: sec specified Dynamic Time : System will wake on the current time + Increase minutes(s). Bypass: BIOS will not control RTC wake function during system shutdown		

3.4.9 Digital IO Port Configuration



Options Summary		
DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input or Output		

3.4.10 Status LED Configuration



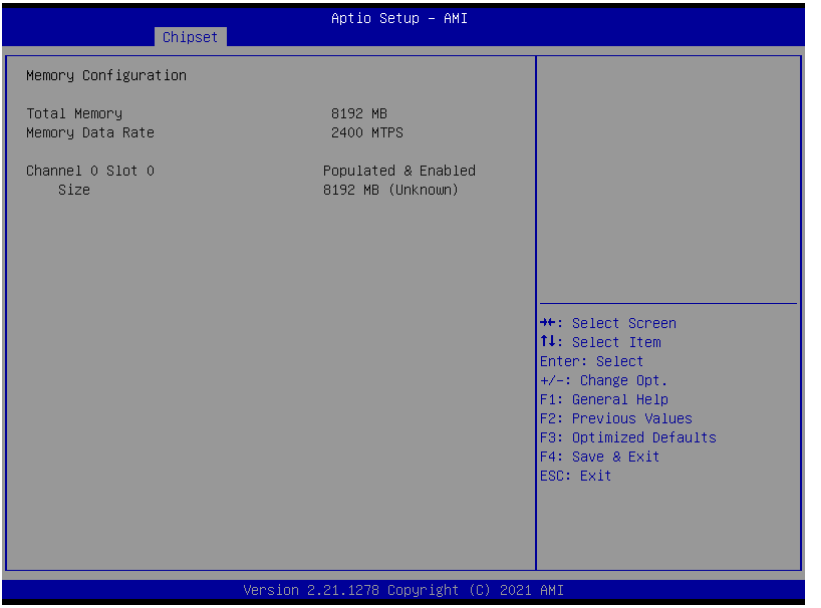
Options Summary		
Configure LAN Bypass Status LED	LED OFF	Optimal Default, Failsafe Default
	RED LED ON	
	RED LED BLINK	
	RED LED FAST BLINK	
	GREEN LED ON	
	GREEN LED BLINK	
	GREEN LED FAST BLINK	
Configure Status LED.		

3.5 Setup Submenu: Chipset

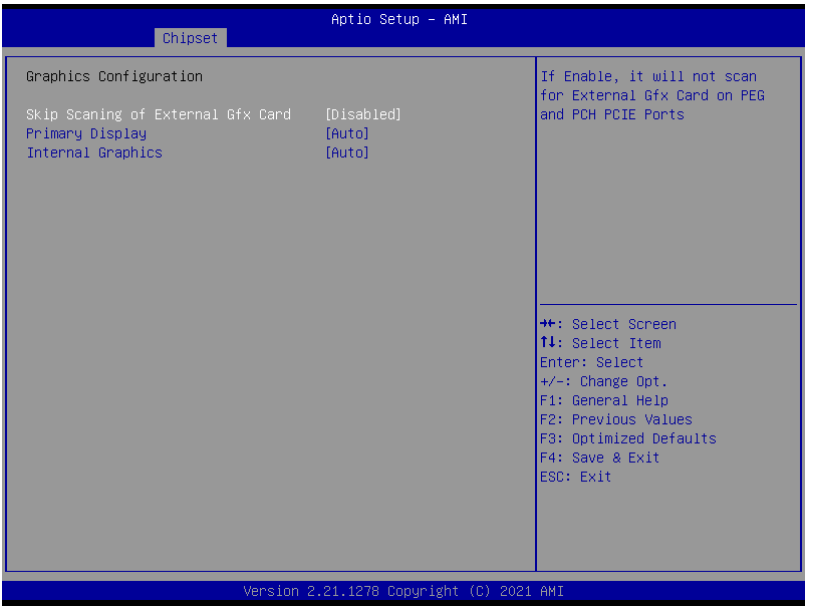
3.5.1 System Agent (SA) Configuration

Options Summary		
VT-d	Disabled	
	Enabled	Optimal Default; Failsafe Default
VT-d capability		

3.5.1.1 Memory Configuration

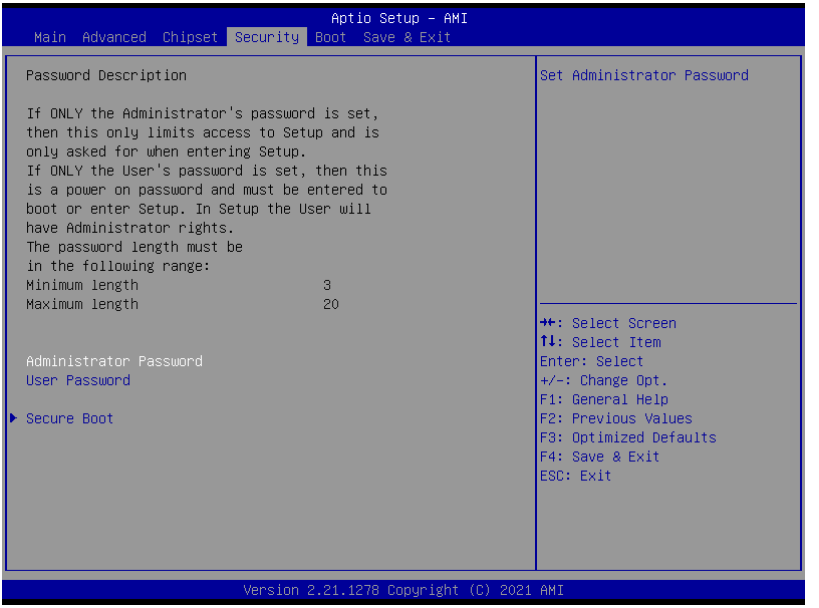


3.5.1.2 Graphics Configuration



Options Summary		
Skip Scaning of External Gfx Card	Disabled	Optimal Default, Failsafe Default
	Enabled	
If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCI	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select HG for Hybrid Gfx.		
Internal Graphics	Auto	Optimal Default, Failsafe Default
	Disabled	
	Enabled	
Keep IGFX enabled based on the setup options.		

3.6 Setup Submenu: Security



Change User/Administrator Password

You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

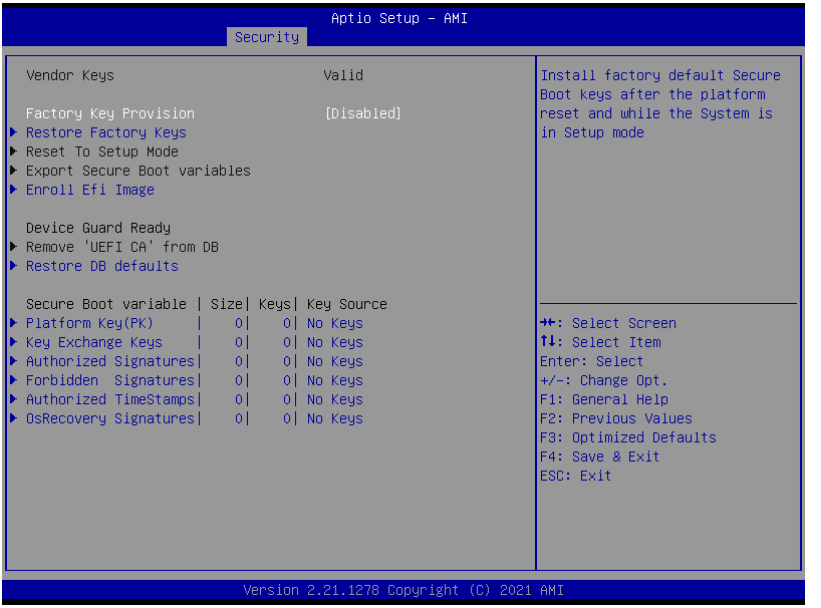
Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PLK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	Force System to User Mode. Install factory default Secure Boot key databases.	
Reset To Setup Mode	Delete all Secure Boot key databases from NVRAM	

3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode		
Restore Factory Keys	Force System to User Mode. Install factory default Secure Boot key databases.	
Reset To Setup Mode	Delete all Secure Boot key databases from NVRAM	
Export Secure Boot variables	Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device	
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)	
Remove 'UEFI CA' from DB	Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)	
Restore DB defaults	Restore DB variable to factory defaults	

Secure Boot Variables

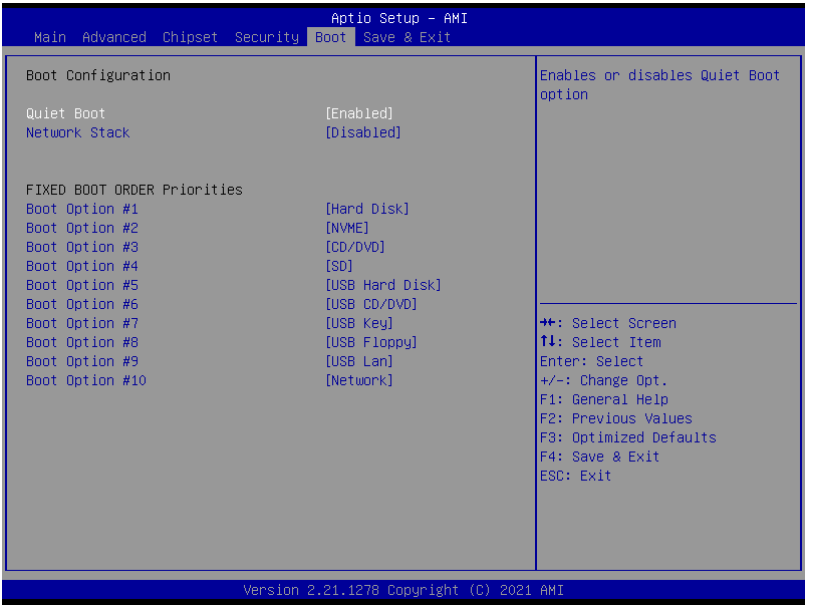
Enroll Factory Defaults or load certificates from a file:

1. Public Key Certificate in:
   a) EFI_SIGNATURE_LIST
   b) EFI_CERT_X509 (DER encoded)
   c) EFI_CERT_RSA2048 (bin)
   d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/COFF Image (SHA256)

Key Source:

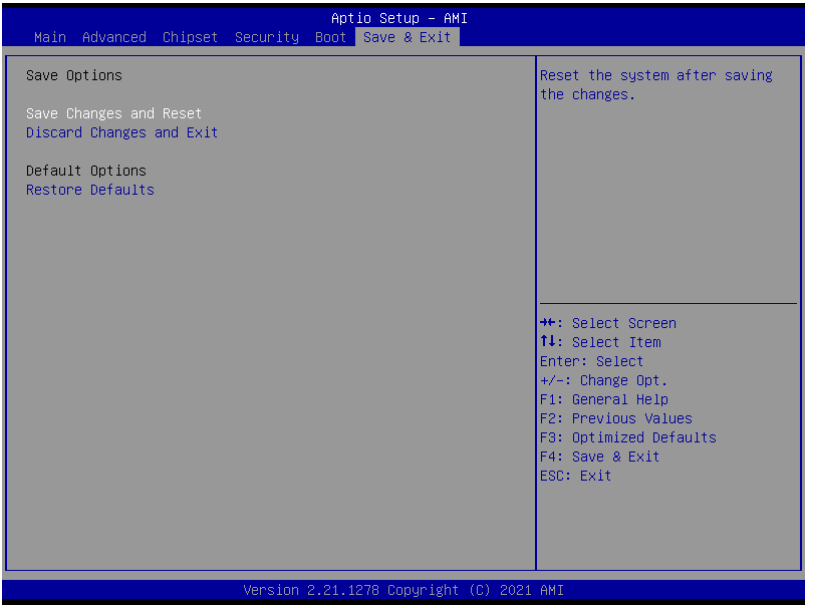
Default, External, Mixed

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		
FIXED BOOT ORDER Priorities	Sets the system boot order	

3.8 Setup Submenu: Save & Exit



Chapter 4

Driver Installation

4.1 Driver Download and Installation

Drivers for the FWS-2280 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/desktop-network-appliance-fws-2280

Download the driver(s) you need and follow the steps below to install them.

LAN Driver for Linux:

Download LAN.gz and install via the Linux GUI.

If you are not utilizing a GUI shell for your system, then install via terminal.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
// Disable WDT counting
WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
// Clear Watchdog Timeout Status
WDTClearTimeoutStatus();
// WDT relative parameter setting
WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
// Watchdog Timer counter setting
SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID    WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************
```

```
*****************************************************************************
OID   SIOEnterMBPnPMode(){
      Switch(SIOIndex){
            Case 0x2E:
                  IOWriteByte(SIOIndex, 0x87);
                  IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0x55);
Break;
            Case 0x4E:
                  IOWriteByte(SIOIndex, 0x87);
                  IOWriteByte(SIOIndex, 0x01);
IOWriteByte(SIOIndex, 0x55);
IOWriteByte(SIOIndex, 0xAA);
                  Break;
      }
}

VOID   SIOExitMBPnPMode(){
      IOWriteByte(SIOIndex, 0x02);
      IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
      IOWriteByte(SIOData, LDN);
}
*****************************************************************************
```

```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
IOWriteByte(SIOData, Value);
SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

Hardware and LAN Bypass Programming

B.1 Status LED

B.1.1 Introduction

The FWS-2280 features several LED indicators which can be programmed using the AAEON SDK. The user can program the LED indicators to display different status modes.

B.1.2 Status LED Configuration

Table1: LED Status

STA_LED2	STA_LED1	STA_LED0	LED Status
0	0	0	LED Off
0	0	1	Red
0	1	0	Red Blinking (Slowly)
0	1	1	Red Blinking (Quickly)
1	0	0	Reserved
1	0	1	Green Blinking (Slowly)
1	1	0	Green Blinking (Quickly)
1	1	1	Green

Table2: Status LED relative register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

B.1.3 Sample Code

```
************************************************************
#define Byte  CPLD_SLAVE_ADDRESS//This parameter is represented
from Note1
#define Byte  OFFSET            //This parameter is represented
from Note2
************************************************************
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
     //LED Off
     //BIT2=0, BIT1=0, BIT0=0
     bData = bData & 0xF8;
     break;
}
case 1:
{
     //Red LED On
     //BIT2=0, BIT1=0, BIT0=1
     bData = (bData & 0xF8) | 0x01;
     break;
}
case 2:
{
     //Red LED Blink
     //BIT2=0, BIT1=1, BIT0=0
     bData = (bData & 0xF8) | 0x02;
     break;
}
case 3:
{
     //Red LED Fast Blink
     //BIT2=0, BIT1=1, BIT0=1
     bData = (bData & 0xF8) | 0x03;
     break;
}
case 4:
```

```
{
     //Green LED On
     //BIT2=1, BIT1=1, BIT0=1
     bData = (bData & 0xF8) | 0x07;
     break;
}
case 5:
{
     //Green LED Blink
     //BIT2=1, BIT1=0, BIT0=1
     bData = (bData & 0xF8) | 0x05;
     break;
}
case 6:
{
     //Green LED Fast Blink
     //BIT2=1, BIT1=1, BIT0=0
     bData = (bData & 0xF8) | 0x06;
     break;
}
default:
     break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
************************************************************
```

B.2 LAN Bypass

B.2.1 Introduction

The FWS-2280 supports LAN Bypass to allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

B.2.1 LAN Bypass Configuration

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table2: LAN Bypass relative register table

Function	Description
LAN_ID3	Used to select which LAN Kit will be configured (see Table 1 of this section). These parameters should be set before ACT_EN
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior for selected LAN kit, when system power is on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior for selected LAN kit, when system power is off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior for selected LAN kit, when WDT is triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass relative register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

B.2.3 Sample Code

```
************************************************************
#define Byte  CPLD_SLAVE_ADDRESS//This parameter is represented
from Note1
#define Byte  OFFSET            //This parameter is represented
from Note2
************************************************************
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;


BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
     bData = bData | 0x08;
else
     bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
     bData = bData | 0x04;
else
     bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
     bData = bData | 0x02;
else
     bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
     bData = bData | 0x01;
```

```
else
     bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
     bData = bData & 0xBF;
else                   // Bypass
     bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
     bData = bData & 0xDF;
else                   // Bypass
     bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET) // Reset
     bData = bData & 0xEF;
else              // Bypass
     bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
```

```
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
**************************************************************
```

B.3 Software Reset Button (General Propose Input)

B.3.1 Introduction

The FWS-2280 features a general-purpose input button which can be programed with the AAEON SDK.

B.3.2 Soft Reset Button Configuration

Table 2: LAN Bypass relative register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low 1: Pin Level States High

Table 1 : Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

B.3.3 Sample Code

```
************************************************************
#define Word  BTN_STS   //This parameter is represented from
Note1
#define Byte  BTN_STS_R      //This parameter is represented
from Note2
************************************************************
Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
     BYTE TmpValue;

     TmpValue = inportb (IoAddr);
return  (TmpValue & (1 << BitNum))
}
************************************************************
VOID  Main(){
     Byte RstBtn;

     RstBtn = GET_Value (BTN_STS, BTN_STS_R); // Active Low
}
************************************************************
```

Appendix C

Glue Removal Procedure

C.1 Removing Glue from Your System

To protect components from damage and ensure proper operation out of the box, glue may have been applied to some cables or connectors to keep them in place during shipping. This glue must be removed before attempting to swap components or perform maintenance. This section details the steps needed to remove the glue.

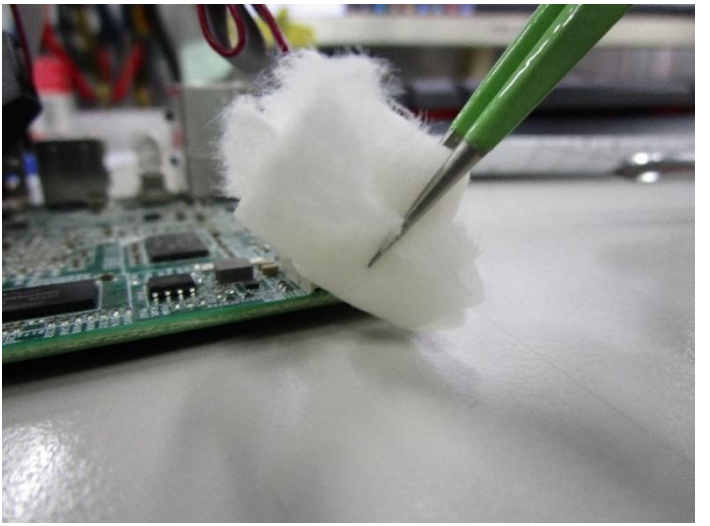
Before performing any kind of system maintenance, ensure the system is shut down (not in sleep or hibernate mode) and the power cable has been removed. Follow steps in Chapter 2 to access the components inside.

You will need the following items for this step:

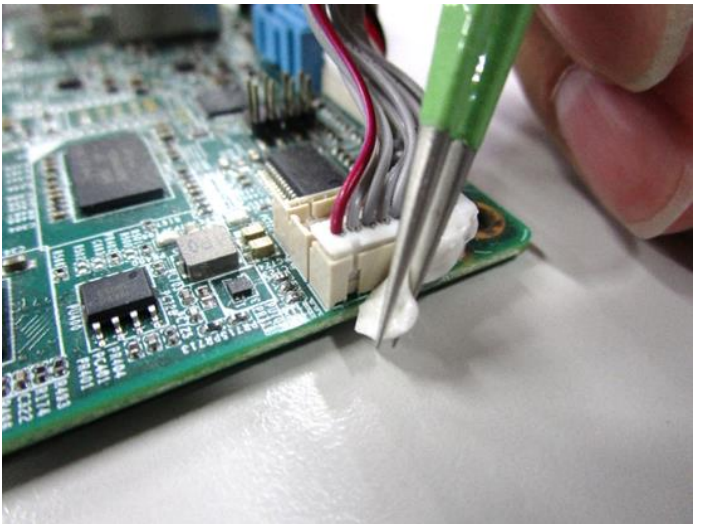
- Cotton or cotton swab
- Anti-static tweezers
- An alcohol solution that is at least 99.5% alcohol (ethanol solution or denatured alcohol). AAEON recommends using an eye dropper or a bottle with a nozzle as in the picture below:

Step 1: Using an eyedropper or bottle as shown above, apply a few drops of alcohol to the glue.

Step 2: Allow the alcohol to soak for 10 seconds, then use a cotton swab or cotton with anti-static tweezers to evenly rub the alcohol over the glue.



Step 3: Let soak for 10 more seconds, then use anti-static tweezers to remove the glue.



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