FWS-2275

Desktop Network Appliance

User's Manual 3rd Ed

Last Updated: May 29, 2025

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2275	1
● Antenna	2
● Power Adapter	1
● VESA mount	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○: 表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×: 表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period)) : 10 年

备注:

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON System QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	O	O	O	O	O
Connector and Cable	×	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU and Memory	×	O	O	O	O	O
Hard Disk	×	O	O	O	O	O
LCD Modules	×	O	O	O	O	O
CD-ROM/DVD-ROM	×	O	O	O	O	O
Touch Modules	×	O	O	O	O	O
Power	×	O	O	O	O	O
Battery	×	O	O	O	O	O

The table is prepared in accordance with the provisions of SJ/T 11364.

O：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years.

Notes：

1. This product defined period of use is under normal condition.
2. In above part, CPU/Memory/ Hard Disk/CD-ROM/DVD-ROM/ Power are optional.
3. In above part, LCD Modules/ Touch Modules are for all-in-one product model.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	Desktop Network Appliance
Processor	Intel® Celeron® Processor N3350 SoC
Chipset	SoC
System Memory	Onboard LPDDR4, 2GB

Network	
Ethernet	Intel® Ethernet Controller I210, GbE x 3 (co-lay with Mini PCIe)
Bypass	—

Display	
Graphic Controller	Intel® HD graphics integrated
Connector	HDMI Connector (Optional)

Storage	
HDD	—
CF/CFast/mSATA	Onboard eMMC 16GB (Optional up to 32GB)

Internal	
PCIe Slot	—
Mini-PCIe Slot	Full-size Mini Card Slot with SIM Socket x 1
Keyboard and Mouse	—
USB	USB 3.2 Gen 1 x 2

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
Software Button	—
TPM	TPM v1.2 9660/TPM2.0 9665 (Optional)
GPIO	4-bits Input, 4-bit Output
Fan	—
MTBF (Hours)	550,521
Color	Black

Environmental

Power Requirement	9V ~ 24V DC Power
Operating Temperature	32°F ~ 122°F (0°C ~ 50°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz / operation
	1.5 Grms/ 5 ~ 500Hz / non-operation
Shock	10 G peak acceleration (11 m sec. duration), operation
	20 G peak acceleration (11 m sec. duration), non-operation
Dimension (W X D X H)	45.3" x 45.3"x 17.3" (115mm x 115mm x 44mm)

I/O

Front Panel	USB 3.2 Gen 1 x 2
	LED x 6 (Top Row x 3, Bottom Row x 2)
	Power Button with LED Integrated x 1
	Micro-USB Console Port x 1

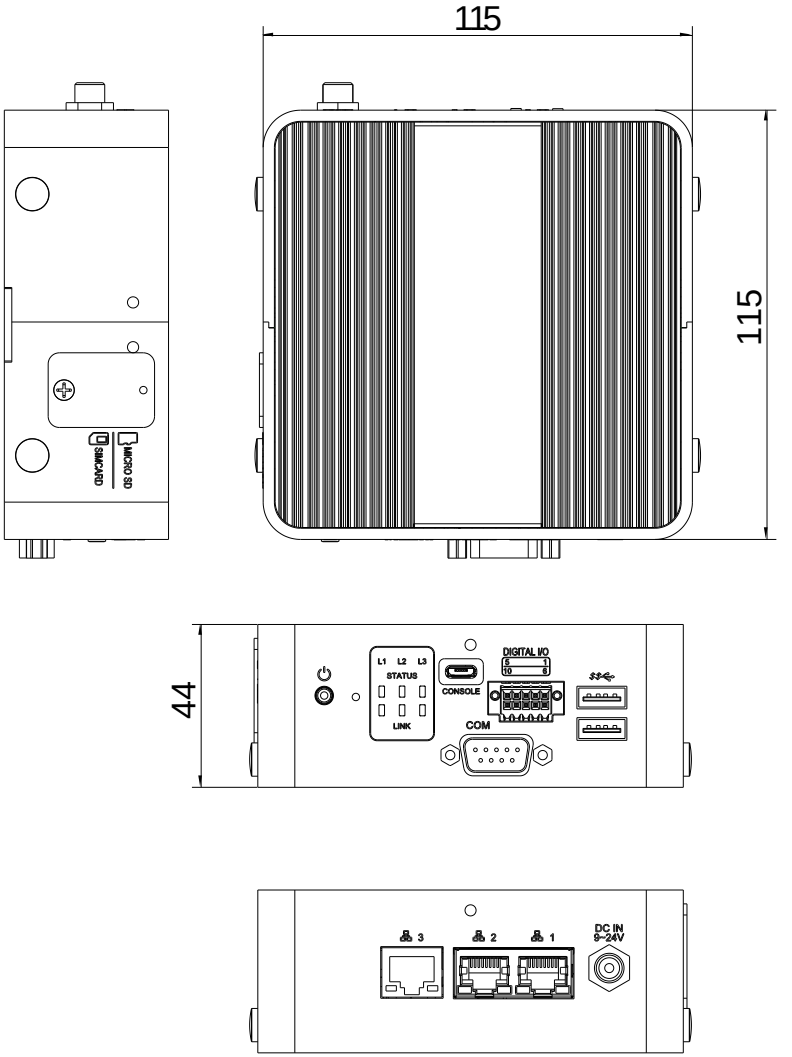
Front Panel (Cont.)	RS-232/422/485 x 1
	GPIO 8-bit, 4-bit Input, 4-bit Output
	Reset Button x 1
Rear Panel	1GbE RJ-45 Ports x 3
	Power Input Connector, Lockable x 1
Left I/O	SIM Slot x 1 + Micro-SD Slot with Cover x 1
	Wi-Fi Antenna Connector
	LTE Antenna Connector
Right I/O	Wi-Fi Antenna Connector
	LTE Antenna Connector

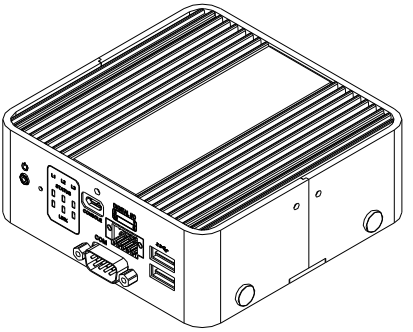
Chapter 2

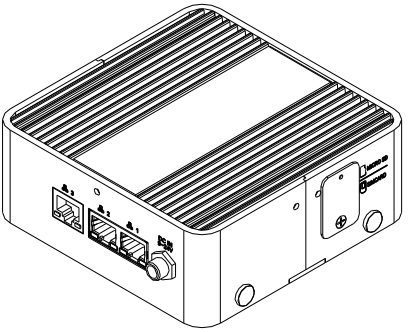
Hardware Information

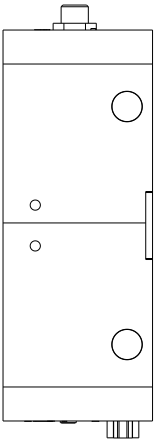
2.1 Dimensions

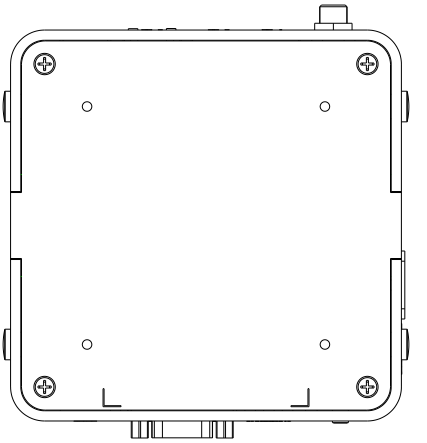
System



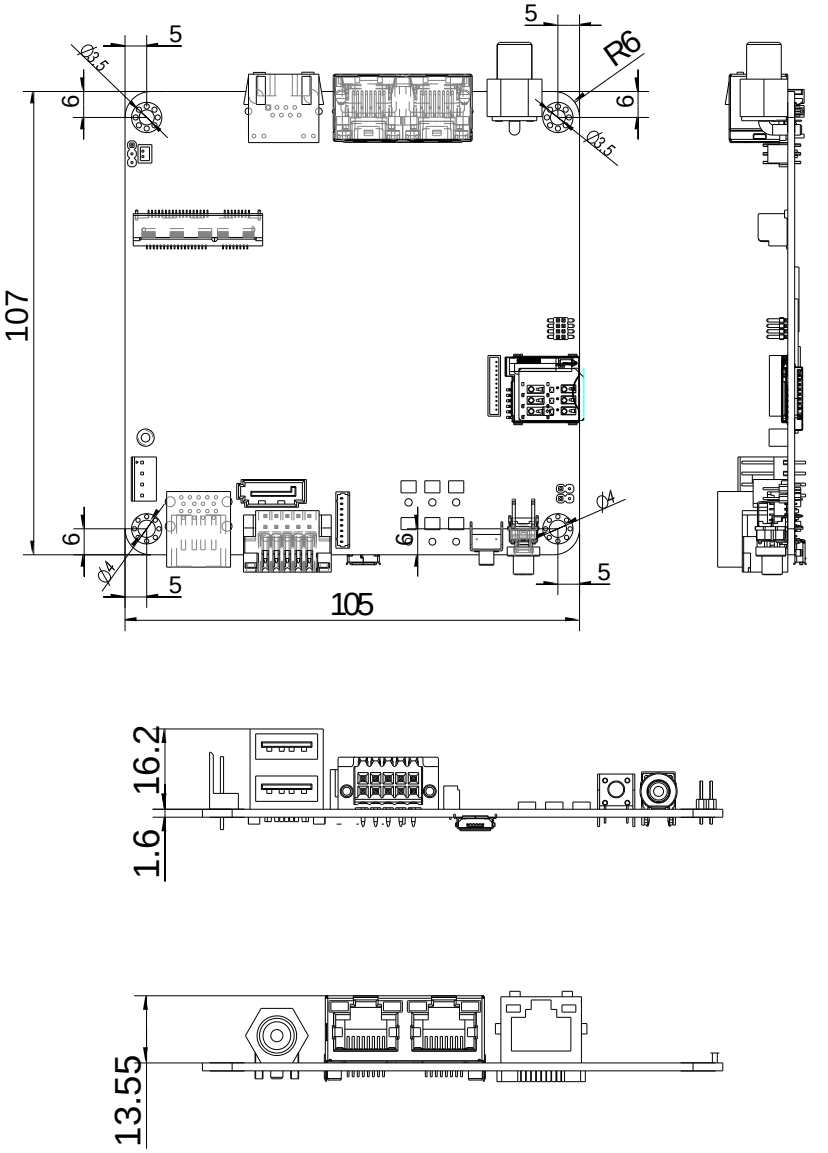


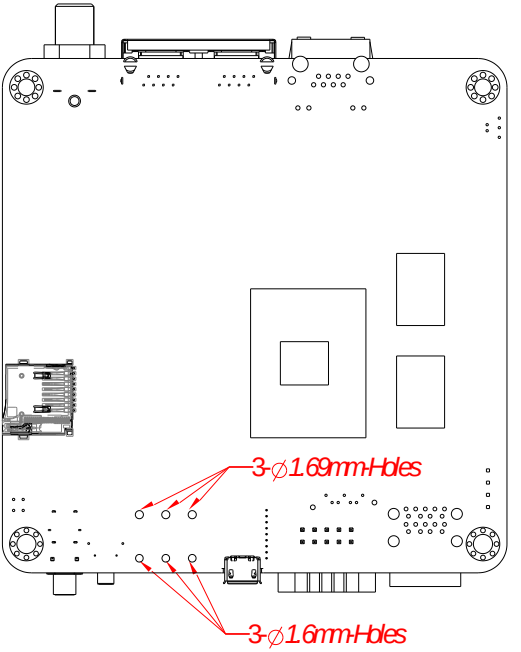






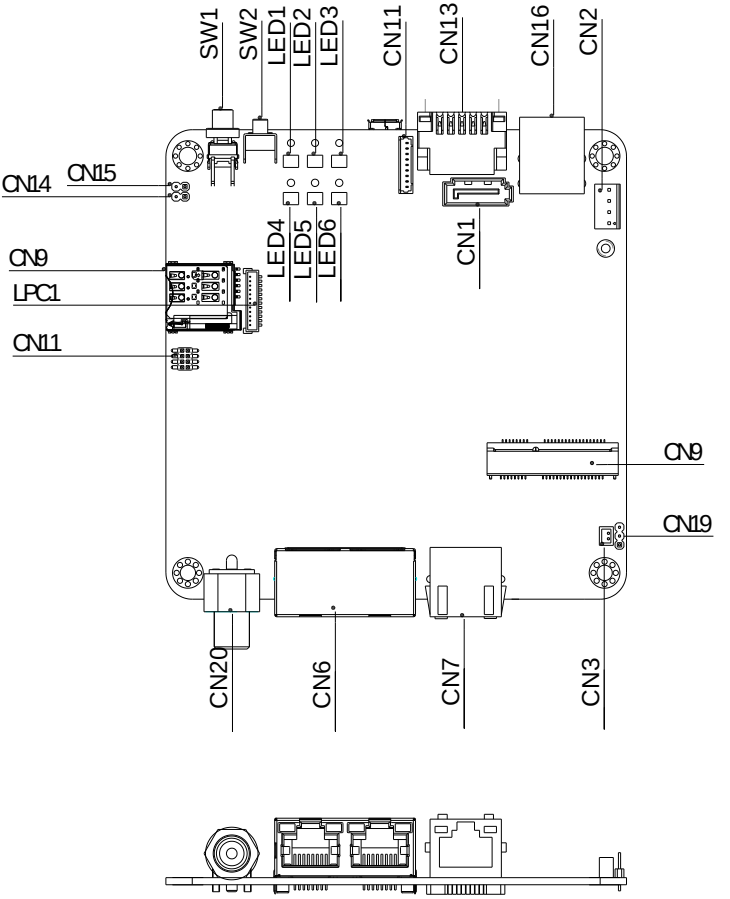
Board



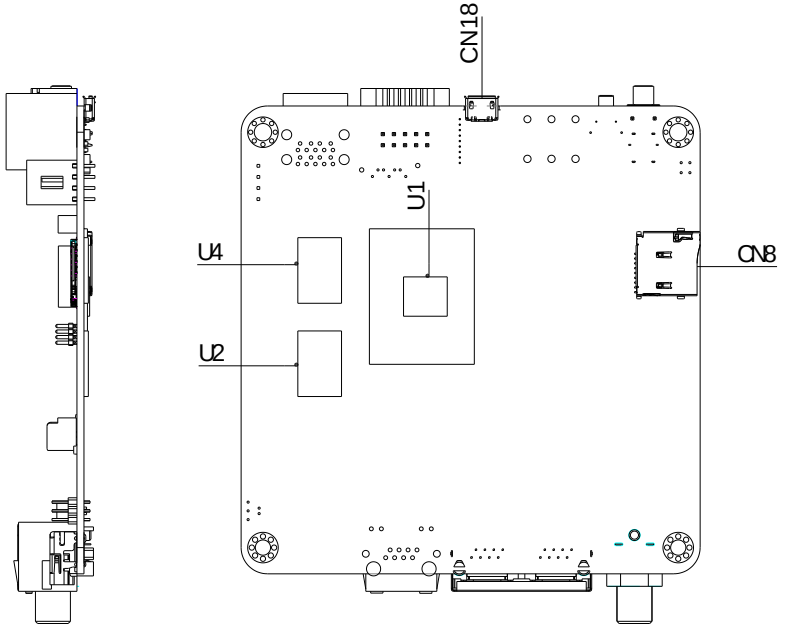

3-∅1.69mm Holes
3-∅1.6mm Holes

2.2 Jumpers and Connectors

Component Side



CPU Side

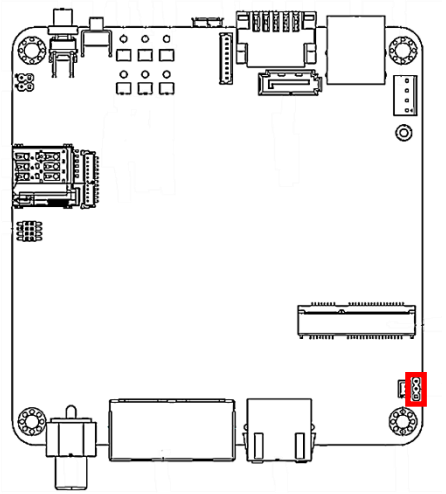


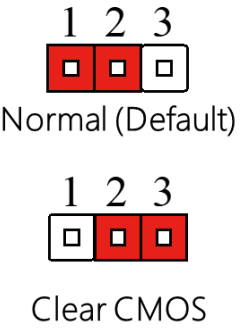
2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application.

Label	Function
CN19	CMOS Setting Selection

2.3.1 CMOS Setting Selection (CN19)



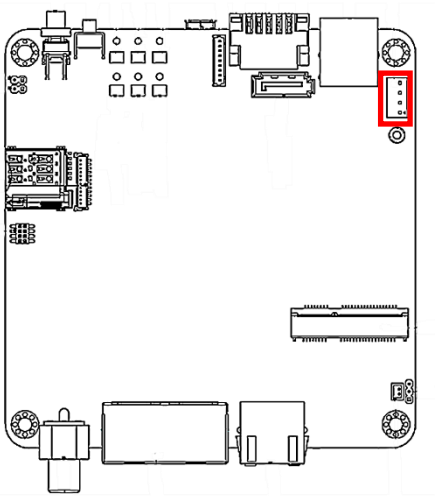


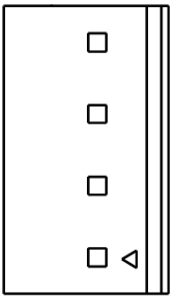
2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application.

Label	Function
CN1	SATA Connector
CN2	SATA Power Connector (+5V only)
CN3	Battery Connector
CN6	LAN Port 1 & 2 RJ45
CN7	LAN Port 3 RJ45
CN8	Micro-SD
CN9	Mini Card (option) with Micro-SIM
CN11	Serial Port 1
CN13	DIO Connector
CN16	Dual (2x) USB3.0 Port
CN18	Micro-USB Console (Serial Port 1)
CN20	DC Jack (9V~24V)
LED1	Status LED
LED2	Status LED
LED3	Status LED
LED4	LAN Port 1 Activity
LED5	LAN Port 2 Activity
LED6	LAN Port 3 Activity
SW1	Power Button
SW2	Software Reset

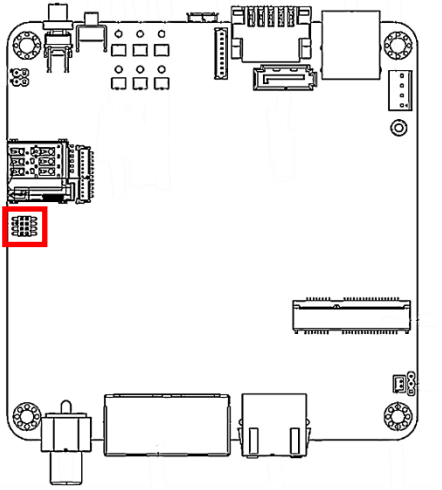
2.4.1 SATA Power Connector (CN2)

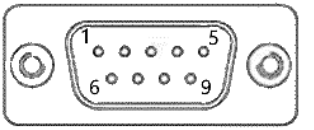




Pin	Signal	Pin	Signal
1	NA	3	GND
2	GND	4	+5V

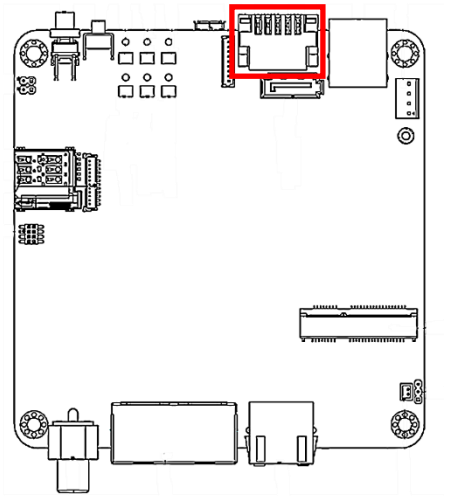
2.4.2 Serial Port 1 (RS-232/422/485) (CN11)





Pin	Signal	Pin	Signal
1	DCD (485DATA-/422TX-)	6	CTS
2	DSR	7	DTR (422RX-)
3	RXD (422RX+)	8	RI
4	RTS	9	GND
5	TXD (485DATA+/422TX+)		

2.4.3 DIO Connector (CN13)



Pin	Signal	Pin	Signal
1	GND	6	DC-INPUT (9V~24V)
2	Bit0	7	Bit4
3	Bit1	8	Bit5
4	Bit2	9	Bit6
5	Bit3	10	Bit7

2.5 GPIO Mapping

Please see Section 2.4 List of Connectors for connector reference table.

2.5.1 LED GPIO Mapping (LED1, LED2, LED3)

LED	On SIO81866	Color	Control	Power
LED1	GP10	Blue	Addr 0xA00h[bit0] "0"=on,"1"=off	VSB
	GP22	Red	Addr 0xA01h[bit2] "0"=on,"1"=off	VSB
	GP23	Green	Addr 0xA01h[bit3] "0"=on,"1"=off	VSB
LED2	GP56	Blue	Addr 0xA04h[bit6] "0"=on,"1"=off	VCC
	GP54	Red	Addr 0xA04h[bit4] "0"=on,"1"=off	VSB
	GP40	Green	Addr 0xA03h[bit0] "0"=on,"1"=off	VSB
LED3	GP61	Blue	Addr 0xA05h[bit1] "0"=on,"1"=off	VCC
	GP60	Red	Addr 0xA05h[bit0] "0"=on,"1"=off	VCC
	GP57	Green	Addr 0xA04h[bit7] "0"=on,"1"=off	VCC

2.5.2 DIO Controller (CN13) GPIO Mapping

Pin	Signal	GPIO Mapping	Pin	Signal	GPIO Mapping
2	Bit0	Mapping SIO GP80	7	Bit4	Mapping SIO GP84
3	Bit1	Mapping SIO GP81	8	Bit5	Mapping SIO GP85
4	Bit2	Mapping SIO GP82	9	Bit6	Mapping SIO GP86
5	Bit3	Mapping SIO GP83	10	Bit7	Mapping SIO GP87

2.5.3 Software Reset Switch (SW2) GPIO Mapping

SW2 GPIO Mapping
Mapping SIO GP64

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or an error is detected, the module will load the default configuration and reboot automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration was reset by the Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The system CMOS memory has an integrated lithium battery backup for data retention. The battery unit will need to be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, power on the computer and immediately press <Del> or <Esc>.

The function for each interface can be found below.

Main – Basic system information. Date and Time can be set here. Press <Tab> to switch between date elements

Advanced – Configuration for major system features (CPU, Super IO, Hardware Monitor, Digital I/O, etc.)

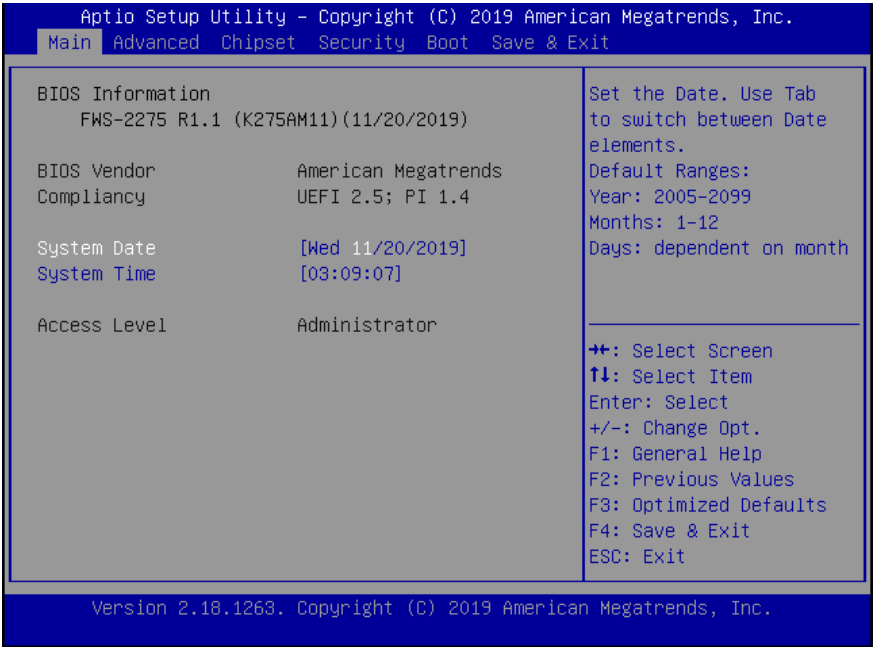
Chipset – Configuration for Chipset features.

Security – Set BIOS Administrator and User password.

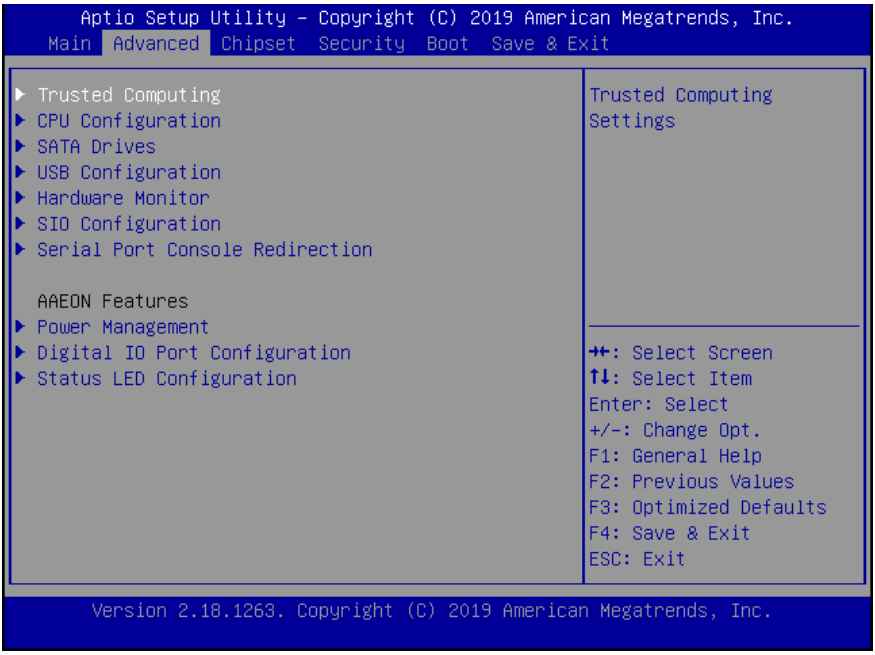
Boot – Adjust Boot configuration and priorities.

Save & Exit –Save changes or restore default settings, and exit system setup.

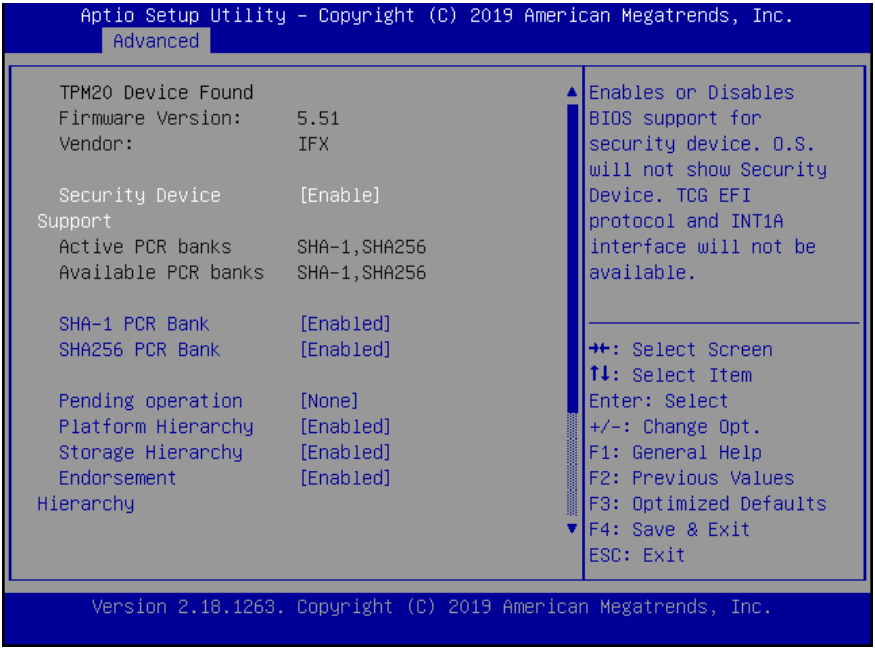
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



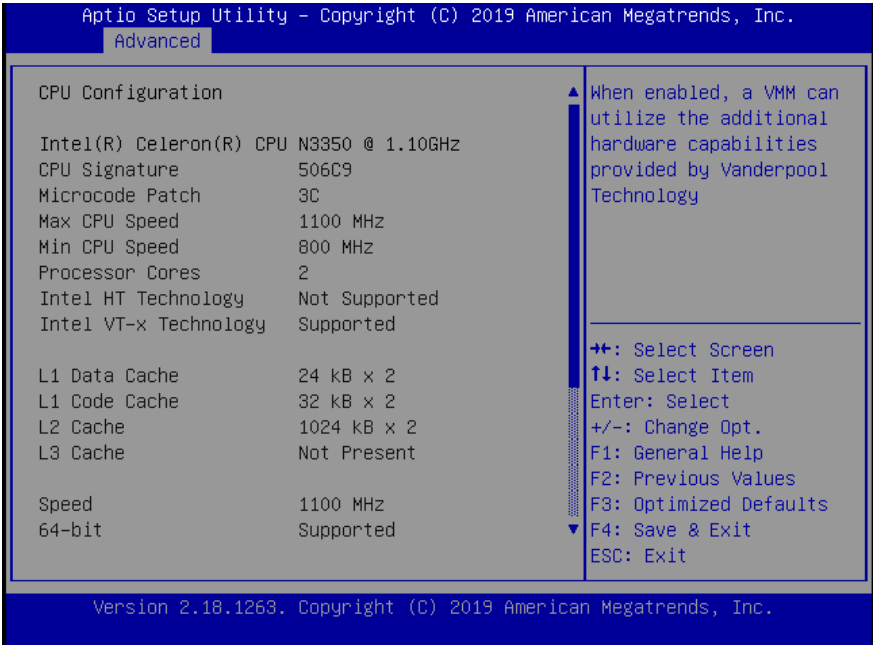
3.4.1 Advanced: Trusted Computing



Options Summary		
Security Device Support	Disabled	
	Enabled	Default Setting
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA-1 PCR Bank	Disabled	
	Enabled	Default Setting
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disabled	
	Enabled	Default Setting
Enable or Disable SHA256 PCR Bank		
Pending operation	None	Default Setting
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		
Platform Hierarchy	Disabled	
	Enabled	Default Setting

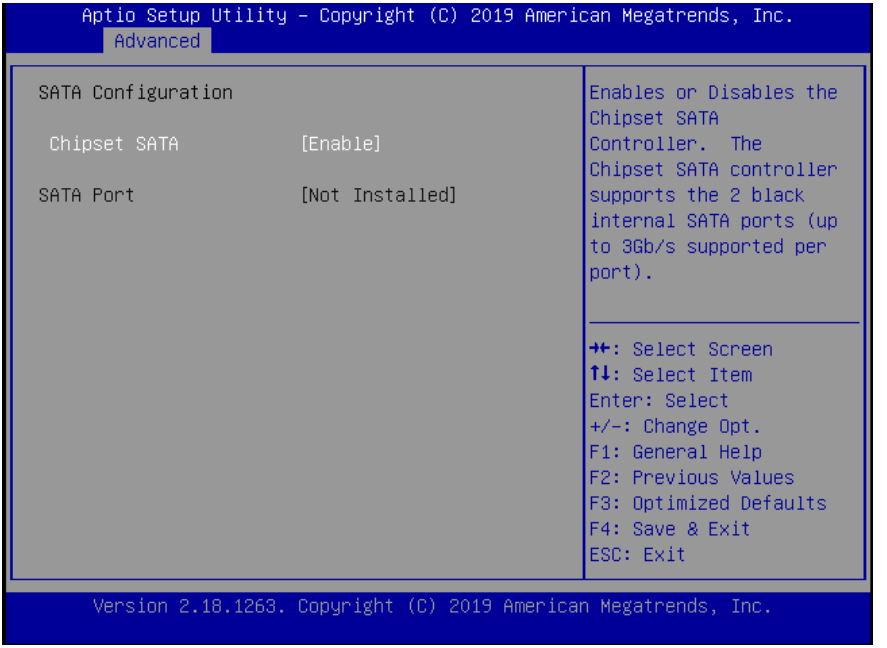
Options Summary		
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Disabled	
	Enabled	Default Setting
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Disabled	
	Enabled	Default Setting
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_1_2	
	TCG_2	Default Setting
Select the TCG2 Spec Version Support, TCG_1_2: Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.2	
	1.3	Default Setting
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Default Setting
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

3.4.2 Advanced: CPU Configuration



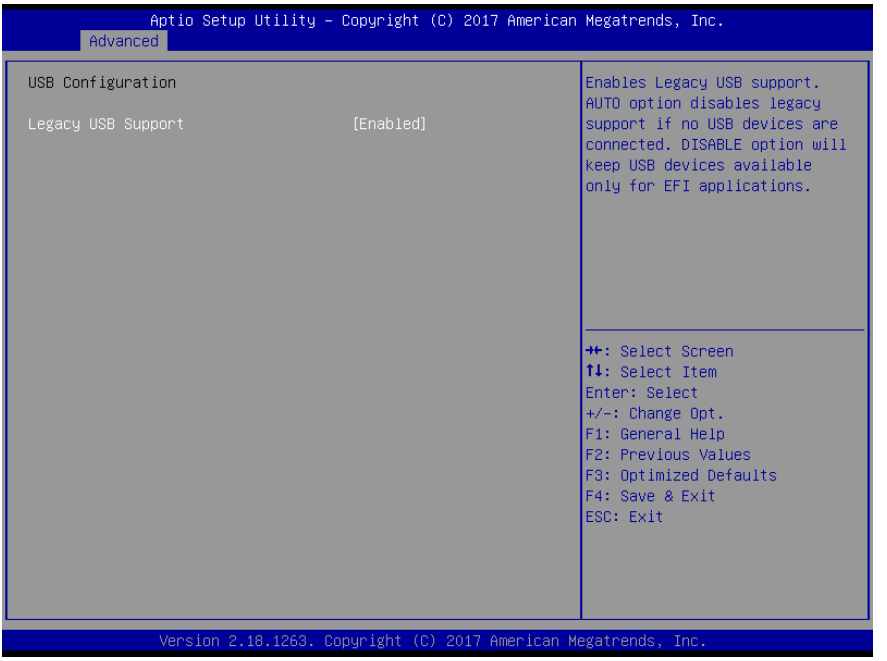
Options Summary		
Intel Virtualization Technology	Disabled	
	Enabled	Default Setting
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology		
VT-d	Disabled	
	Enabled	Default Setting
Enable/Disable CPU VT-d		
EIST	Disabled	Default Setting
	Enabled	
Enable/Disable Intel SpeedStep		
Power Limit 1 Enable	Disabled	Default Setting
	Enabled	
Enable/Disable Power Limit 1		

3.4.3 Advanced: SATA Drives



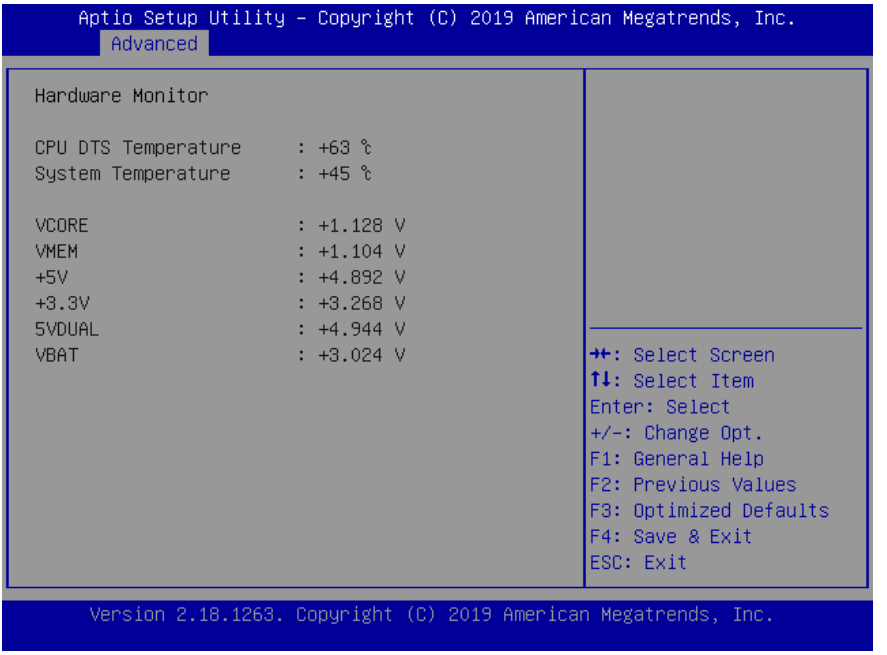
Options Summary		
Chipset SATA	Disabled	
	Enabled	Default Setting
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).		

3.4.4 Advanced: USB Configuration

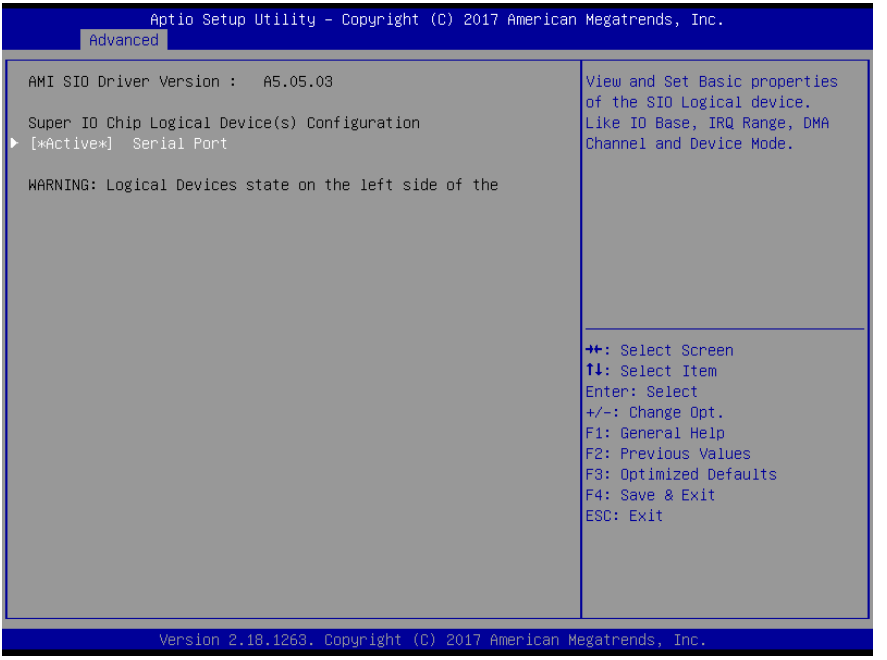


Options Summary		
Legacy USB Support	Disabled	
	Enabled	Default Setting
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.		

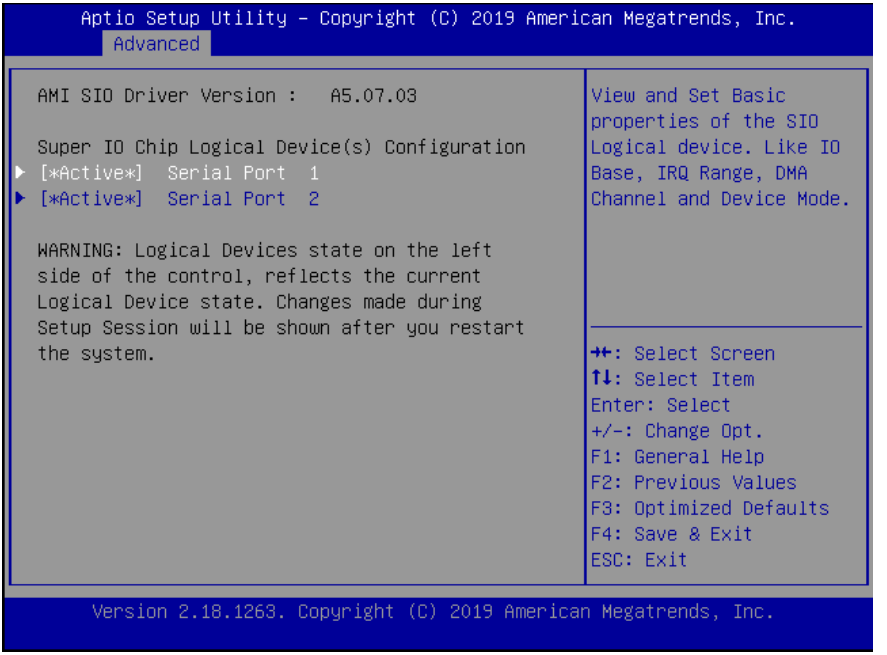
3.4.5 Advanced: Hardware Monitor



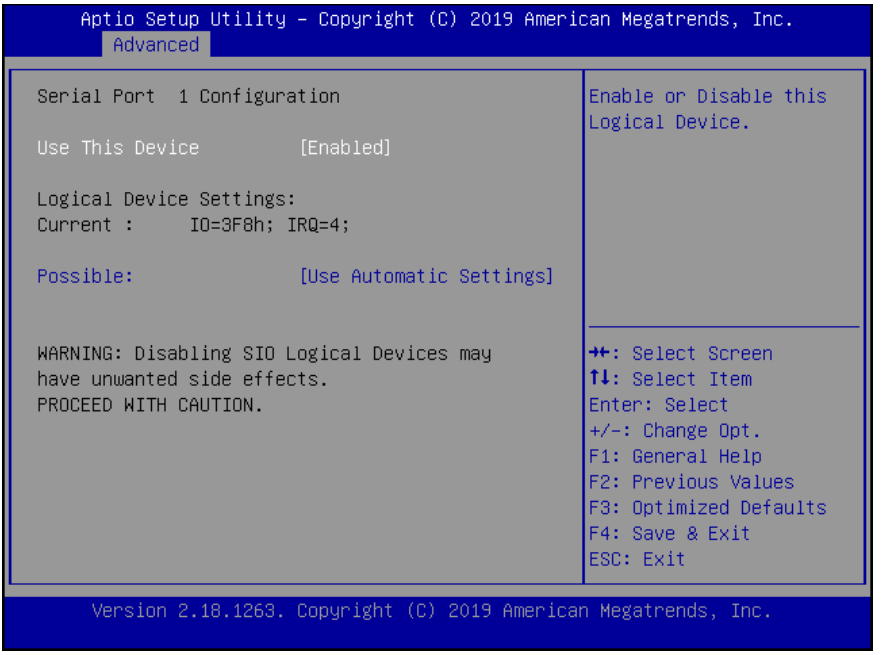
3.4.6 Advanced: SIO Configuration



3.4.6.1 Serial Port Configuration

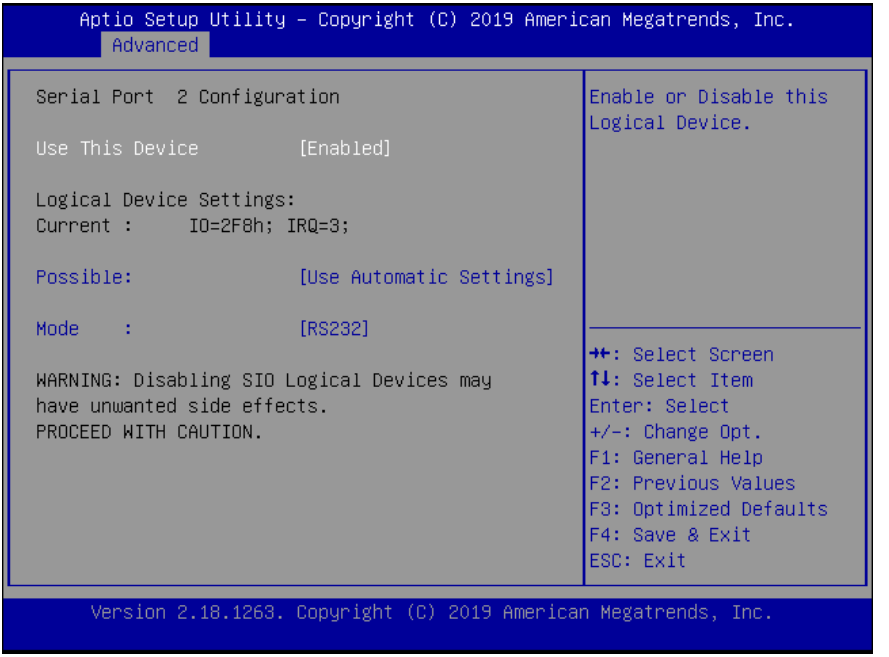


3.4.6.1.1 Serial Port 1 Configuration



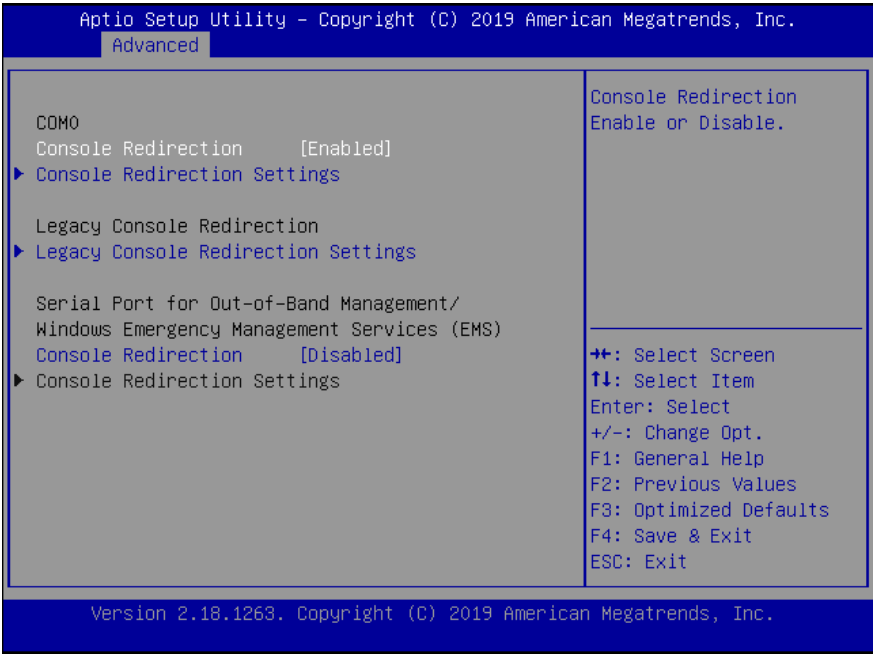
Options Summary		
Use This Device	Disabled	
	Enabled	Default Setting
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Default Setting
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.6.1.2 Serial Port 2 Configuration



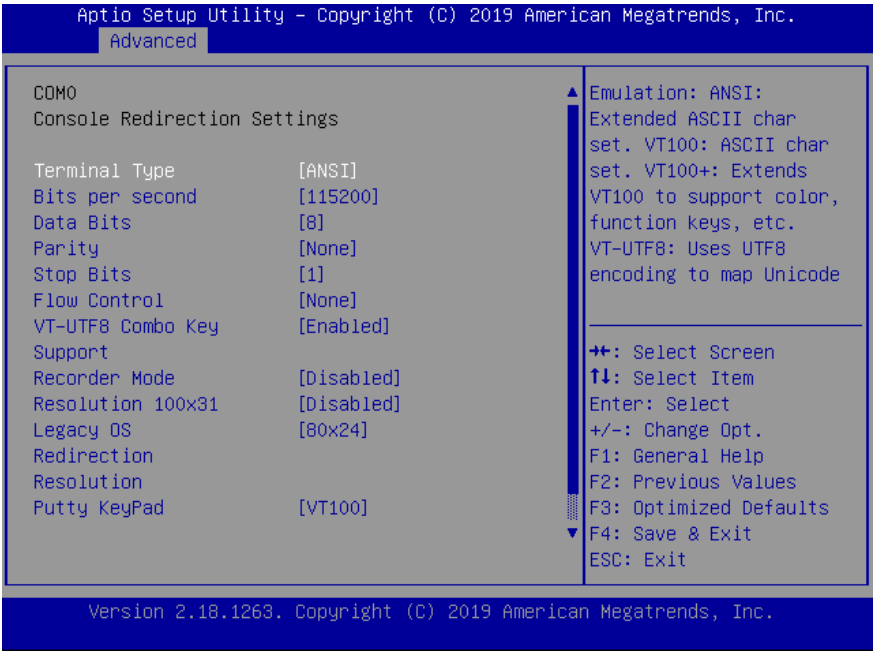
Options Summary		
Use This Device	Disabled	
	Enabled	Default Setting
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Default Setting
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=4;	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Default Setting
	RE422	
	RS485	
UART RS232, 422, 485 Selection.		

3.4.7 Advanced: Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	
	Enabled	Default Setting
Console Redirection Enabled or Disabled.		
Console Redirection	Disabled	Default Setting
	Enabled	
Console Redirection Enable or Disable.		

3.4.7.1 Console Redirection Settings

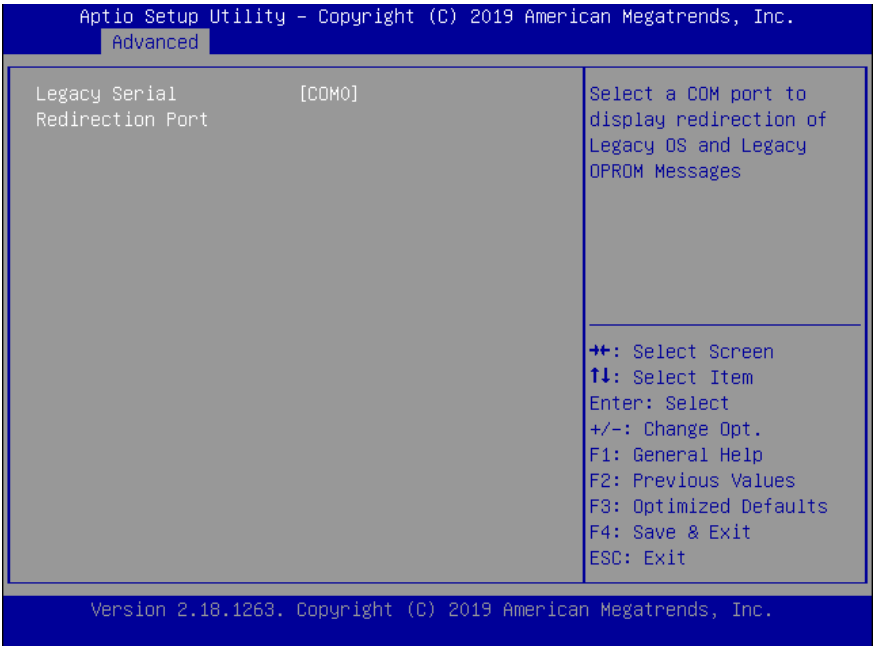


Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	
	ANSI	Default Setting
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.		
Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Default Setting
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

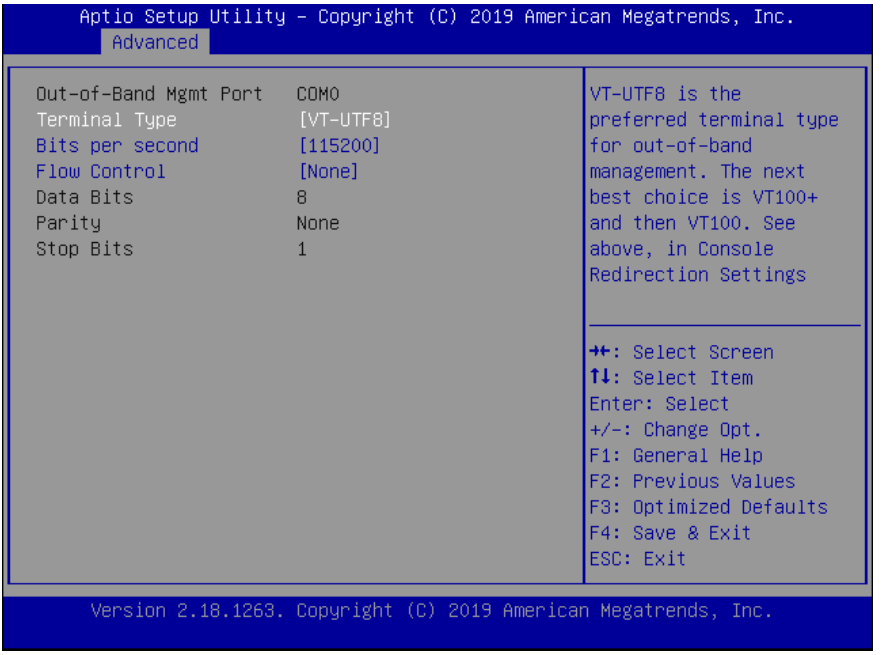
Options Summary		
Data Bits	7	
	8	Default Setting
Data Bits		
Parity	None	Default Setting
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.		
Stop Bits	1	Default Setting
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		
Flow Control	None	Default Setting
	Hardware RTS/CTS	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
VT-UTF8 Combo Key Support	Disabled	
	Enabled	Default Setting
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals		
Recorder Mode	Disabled	Default Setting
	Enabled	
On this mode enabled only text will be sent. This is to capture Terminal data.		
Resolution 100x31	Disabled	Default Setting
	Enabled	
Enables or disables extended terminal resolution		
Legacy OS Redirection Resolution	80x24	Default Setting
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection		

Options Summary		
Putty KeyPad	VT100	Default Setting
	LINUX	
	XTERMR6	
	SCO	
	ESCN	
	VT400	
Select FunctionKey and KeyPad on Putty.		
Redirection After BIOS POST	Always Enable	Default Setting
	BootLoader	
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.		

3.4.7.2 Legacy Console Redirection Settings



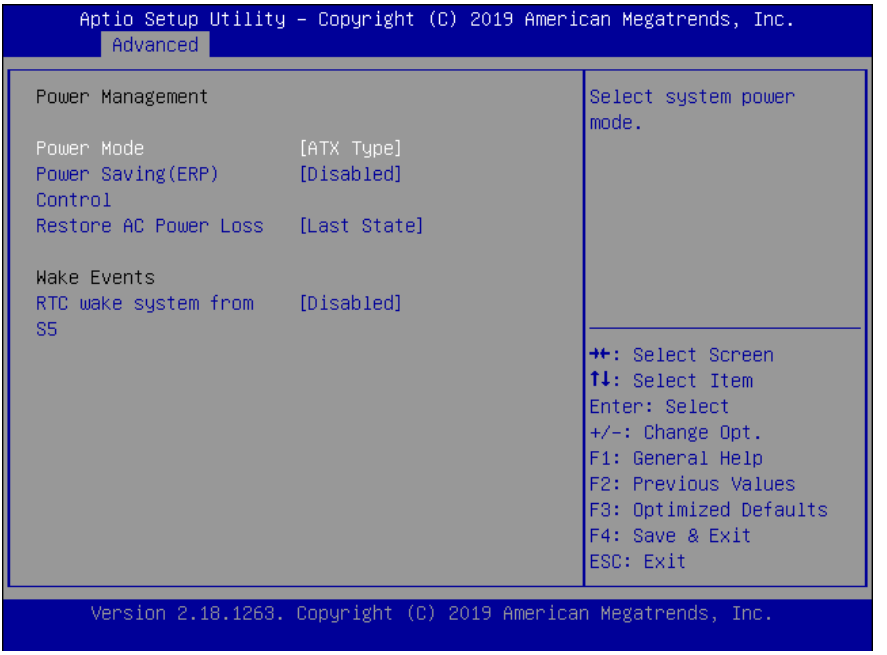
3.4.7.3 Serial Port for Out-of-Band Management/Windows EMS



Options Summary		
Terminal Type	VT100	
	VT100+	
	VT-UTF8	Default Setting
	ANSI	
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.		
Bits per second	9600	
	19200	
	57600	
	115200	Default Setting
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.		

Options Summary		
Flow Control	None	Default Setting
	Hardware RTS/CTS	
	Software Xon/Xoff	
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		
Data Bits	7	
	8	Default Setting
Data Bits		
Parity	None	Default Setting
	Even	
	Odd	
	Mark	
	Space	
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.		
Stop Bits	1	Default Setting
	2	
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.		

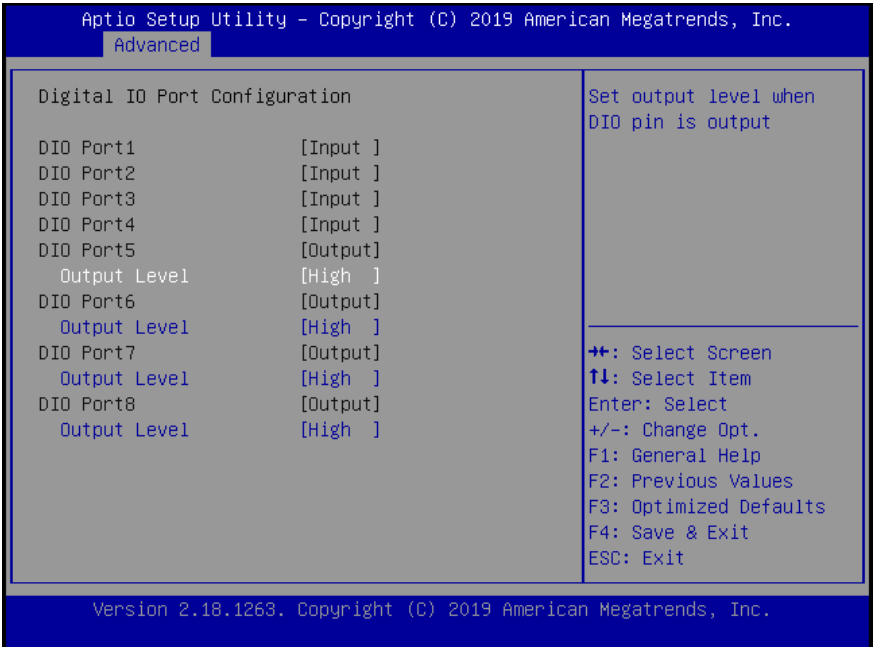
3.4.8 Advanced: Power Management



Options Summary		
Power Mode	ATX Type	Default Setting
	AT Type	
Select Power Supply Mode.		
Power Saving(ERP) Control	Disabled	Default Setting
	Enabled	
Configure power mode for power saving function.		
Restore AC Power Loss	Power Off	
	Power On	
	Last State	Default Setting
Select AC power state when power is re-applied after a power failure.		
RTC Wake system from S5	Disabled	Default Setting
	Fixed time	
	Dynamic time	
Fixed Time: System will wake on the hr::min::sec specified. Dynamic Time: System will wake on the current time + Increase minute(s)		

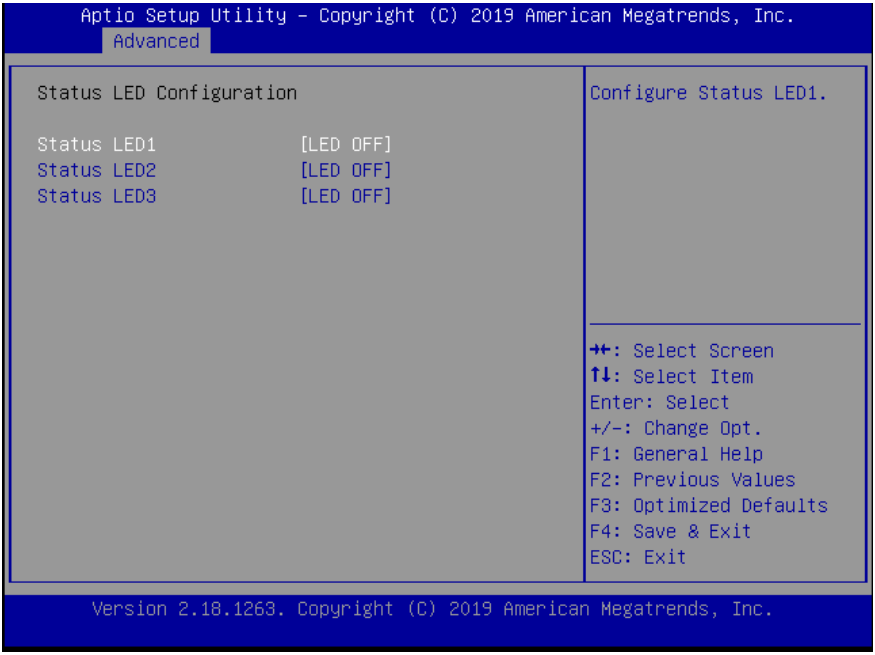
Options Summary		
Wake up day (Fixed time option)	0	Default Setting
Select 0 for daily system wake up, 1-31 for which day of month that you would like the system to wake up.		
Wake up hour (Fixed time option)	0	Default Setting
Select 0-23 For example enter 3 for 3am and 15 for 3pm.		
Wake up minute (Fixed time option)	0	Default Setting
0-59		
Wake up second (Fixed time option)	0	Default Setting
0-59		
Wake up minute increase (Dynamic time option)	1	Default Setting
1-5		

3.4.9 Advanced: Digital IO Port Configuration



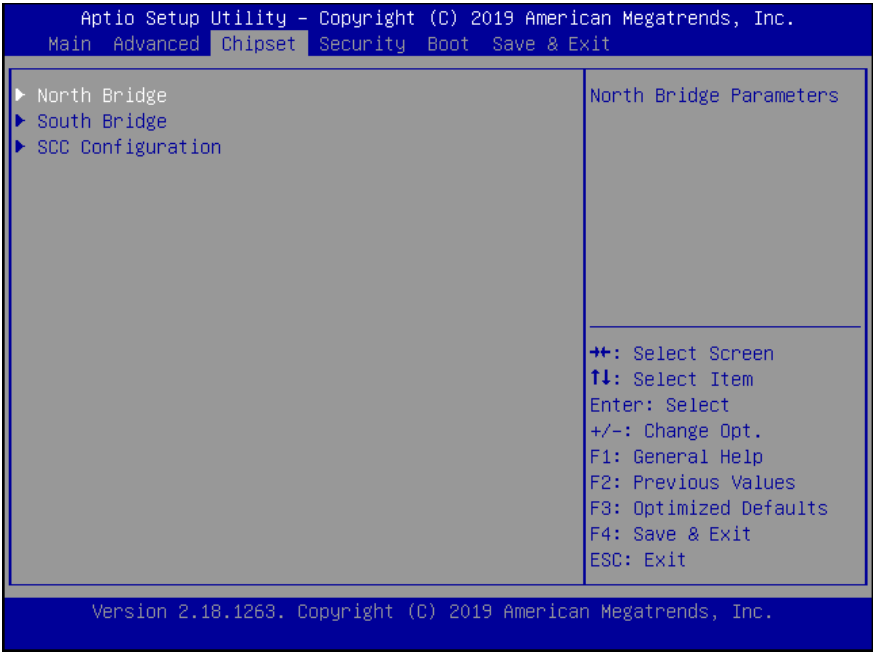
Options Summary		
DIO Port 1~4	Input	Default Setting
Set DIO as Input		
DIO Port 5~8	Output	Default Setting
Set DIO as Output		
DIO Port 5~8 Level	Low	
	High	Default Setting
Set output level when DIO pin is output		

3.4.10 Advanced: Status LED Configuration

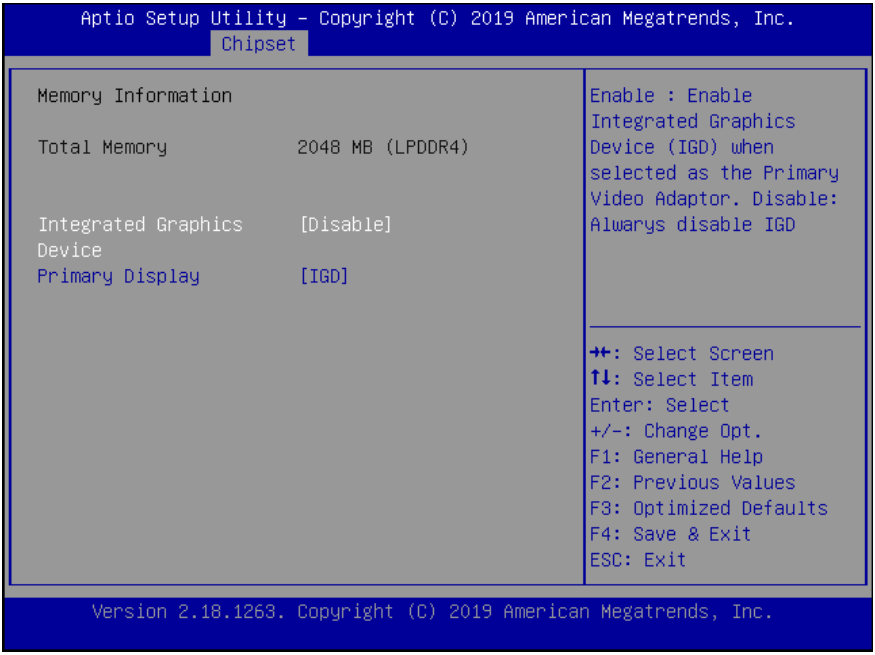


Options Summary		
Status LED 1	LED Off	Default Setting
	BLUE LED ON	
	RED LED ON	
	GREEN LED ON	
Configure Status LED1.		
Status LED 2	LED Off	Default Setting
	BLUE LED ON	
	RED LED ON	
	GREEN LED ON	
Configure Status LED2.		
Status LED 2	LED Off	Default Setting
	BLUE LED ON	
	RED LED ON	
	GREEN LED ON	
Configure Status LED3.		

3.5 Setup Submenu: Chipset

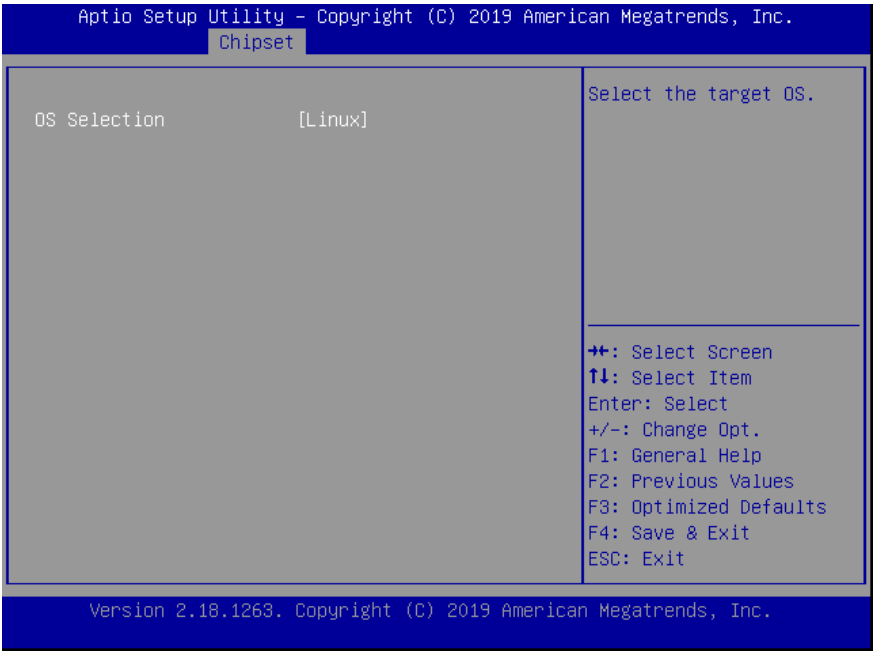


3.5.1 Chipset: North Bridge



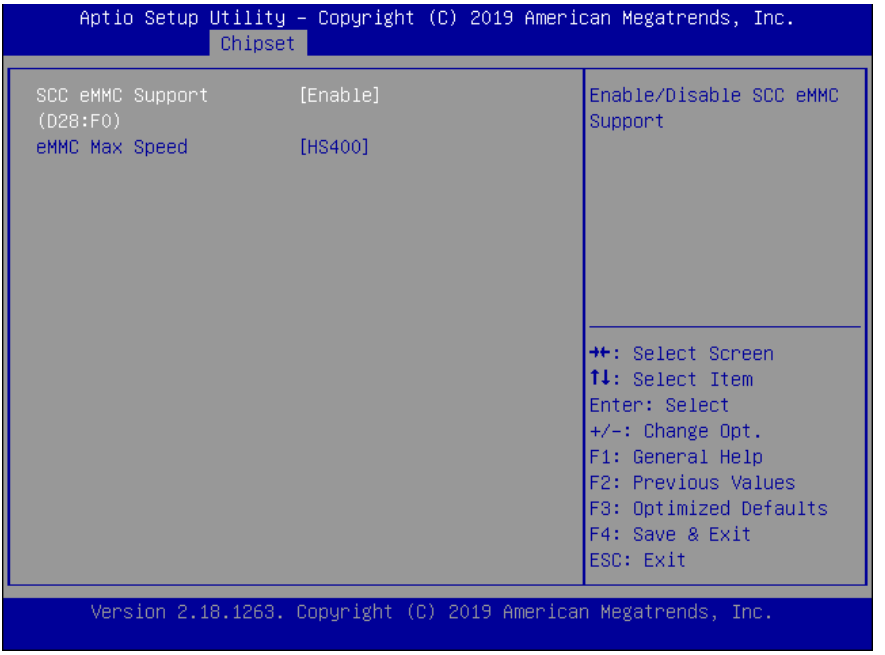
Options Summary		
Integrated Graphics Device	Disabled	Default Setting
	Enabled	
Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD		
Primary Display	IGD	Default Setting
	PCIe	
Select which of IGD/PCI Graphics device should be Primary Display		

3.5.2 Chipset: South Bridge



Options Summary		
OS Selection	Linux	Default Setting
	Windows	
Select the target OS.		

3.5.3 Chipset: SCC Configuration



Options Summary		
SCC eMMC Support (D28:F0)	Enabled	Default Setting
	Disabled	
Enable/Disable SCC eMMC Support		
eMMC Max Speed	HS400	Default Setting
	HS200	
	DDR50	
Select the eMMC max Speed allowed.		

3.6 Setup Submenu: Security

Change User/Supervisor Password

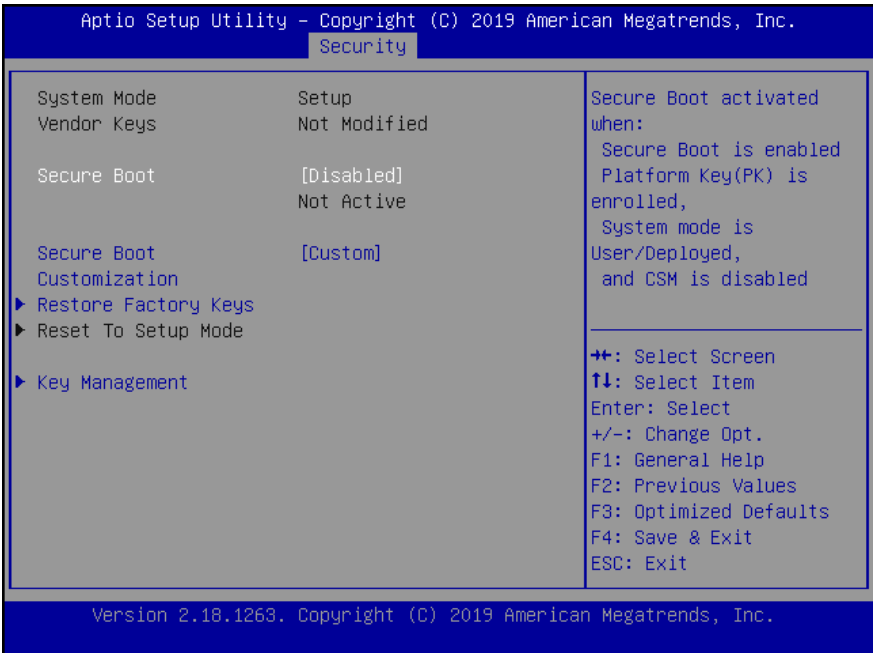
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

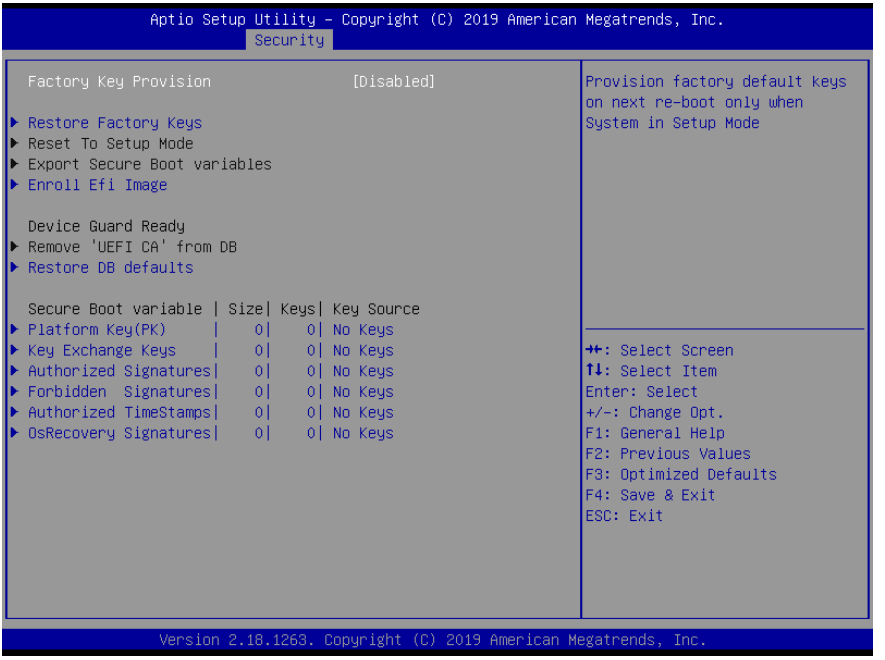
Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Secure Boot



Options Summary		
Secure Boot	Disabled	Default Setting
	Enabled	
Secure Boot activated when: Secure Boot is enabled Platform Key(PK) is enrolled, System mode is User/Deployed, and CSM is disabled		
Secure Boot Customization	Custom	Default Setting
	Standard	
Customizable Secure Boot mode: In Custom mode Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	Yes	Select 'Yes' to Restore Factory Keys
	No	
Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys		
Reset To Setup Mode	Yes	Select 'Yes' to Reset to Setup Mode
	No	
Delete NVRAM content of all UEFI Secure Boot key databases		

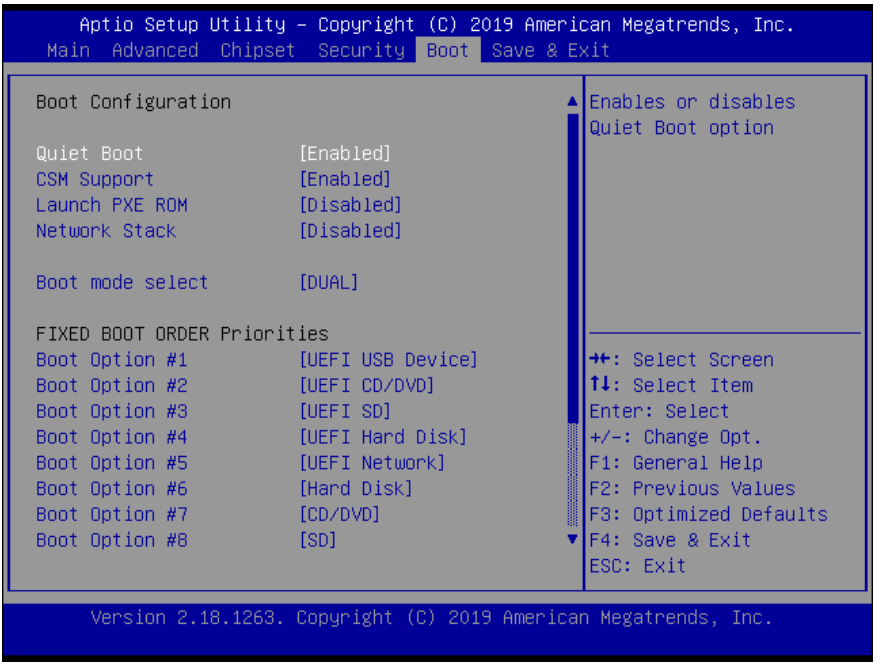
3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Default Setting
	Enabled	
Provision factory default keys on next re-boot only when System in Setup Mode		
Restore Factory Keys	Yes	Select 'Yes' to Restore Factory Keys
	No	
Force System to User Mode. Configure NVRAM to contain OEM-defined factory default Secure Boot keys		
Reset To Setup Mode	Yes	Select 'Yes' to Reset to Setup Mode
	No	
Delete NVRAM content of all UEFI Secure Boot key databases		
Export Secure Boot variables	OK	
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image	OK	
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		

Options Summary		
Remove 'UEFI CA' from DB	Yes No	Select 'Yes' to Remove UEFI-CA from DB
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		
Restore DB defaults	Yes No	Select 'Yes' to Restore DB defaults
Restore DB variable to factory defaults		
Secure Boot variable | Size| Keys| Key Source		
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

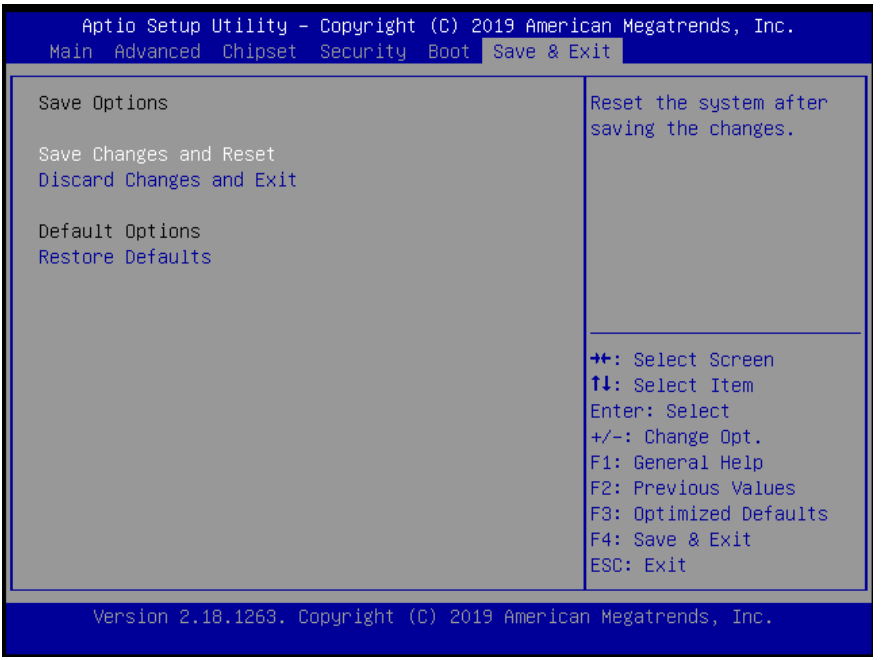
3.7 Setup submenu: Boot



Options Summary		
Quite Boot	Disabled	
	Enabled	Default Setting
Enables or disables Quiet Boot option.		
CSM Support	Enabled	Default Setting
	Disabled	
Enable/Disable CSM Support.		
Launch PXE ROM	Disabled	Default Setting
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		
Network Stack	Disabled	Default Setting
	Enabled	
Enable/Disable UEFI Network Stack		
Boot mode select	DUAL	Default Setting
	LEGACY	
	UEFI	

Options Summary
Select boot mode LEGACY/UEFI

3.8 Setup Submenu: Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and OS Support

Drivers for the FWS-2275 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/desktop-network-appliance-fws-2275

Drivers for the FWS-2275 are designed to work with specific operating systems, and may not work with every OS supported by the FWS-2275. The following chart details which drivers to install for each supported OS.

FWS-2275 OS/Driver Support			
Driver	Win10_X64	Win10_X86	Linux
Step 1 Chipset	Yes		
Step 2 Serial IO	Yes		
Step 3 Graphics	Yes		
Step 4 TXE	Yes		
Step 5 LAN	Yes		Yes
Step 6 WLAN	Yes	Yes	
Step 7 Console Driver	Yes	Yes	

If you have any questions or need assistance, contact your AAEON sales representative for support.

4.2 Drivers Installation

Follow the steps below to install the drivers for FWS-2275.

Step 1 – Install Chipset Driver

1. Open the **Step1 - Chipset** folder and select your OS
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Serial IO Driver

1. Open the **Step2 – Serial IO** folder and select your OS
2. Run the **SetupSerialIO.exe.** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install Graphics Driver

1. Open the **Step3 - Graphic** folder and select your OS
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – TXE Driver

1. Open the **Step4 - TXE** folder and select your OS
2. Run the **SetupTXE.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – LAN Driver

1. Open the **Step5 – LAN** folder and select your OS
2. For Windows, run the **PROWinx64.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. For Linux, use command line to install from **igb-5.3.5.10.tar.gz**

Step 6 – Install WLAN Driver

1. Open the **Step6 – WLAN** folder and select your OS
2. Right click on the **.inf** file and select 'Install'
3. Drivers will be installed automatically

Step 7 – Install Console Driver

1. Open the **Step7 – Console Driver** folder
2. Run the **2500_installer.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*********************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID   WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*********************************************************************************
```

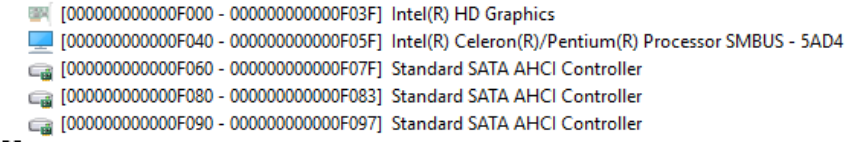
```
*******************************************************************************
VOID   SIOEnterMBPnPMode(){
       Switch(SIOIndex){
              Case 0x2E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0x55);
                        Break;
              Case 0x4E:
                     IOWriteByte(SIOIndex, 0x87);
                     IOWriteByte(SIOIndex, 0x01);
                        IOWriteByte(SIOIndex, 0x55);
                        IOWriteByte(SIOIndex, 0xAA);
                     Break;
       }
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0x02);
       IOWriteByte(SIOData, 0x02);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}
*******************************************************************************
```

```
*****************************************************************************
VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

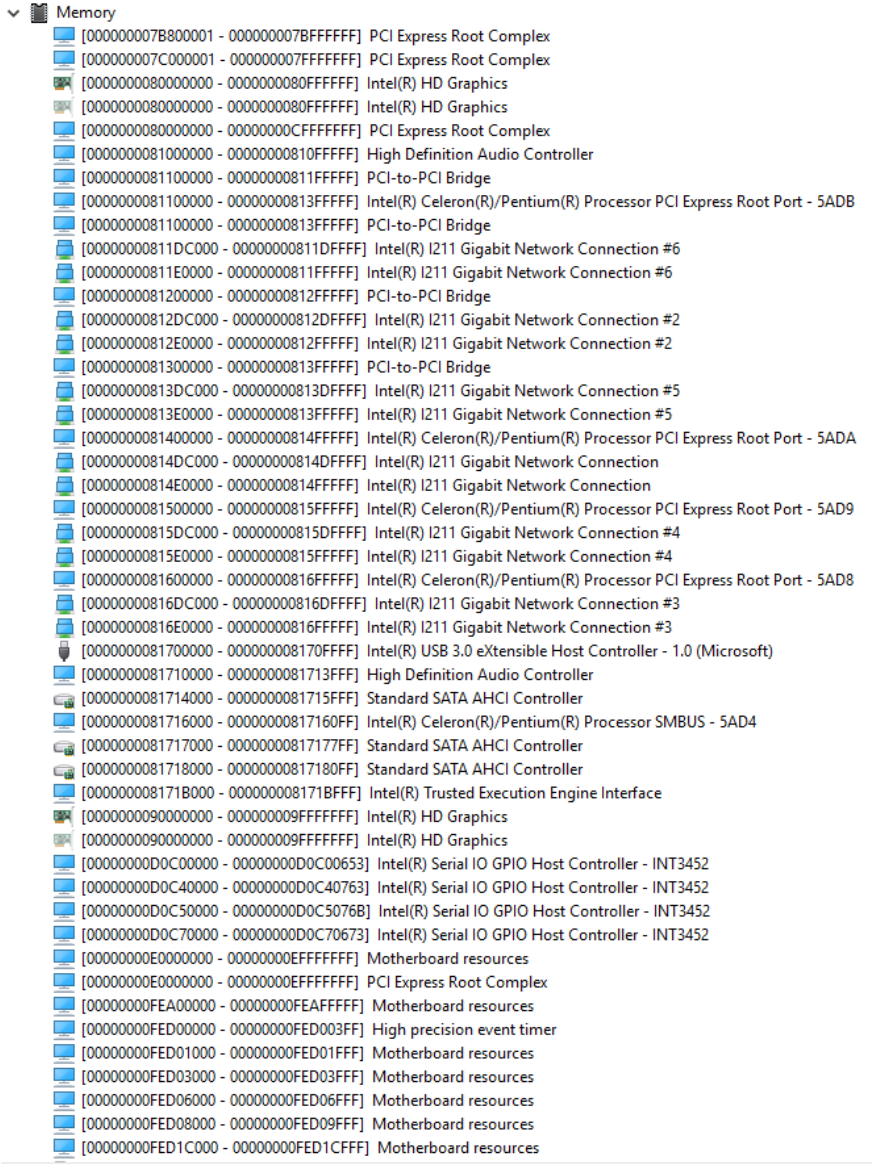
Appendix B

I/O Information

B.1 I/O Address Map

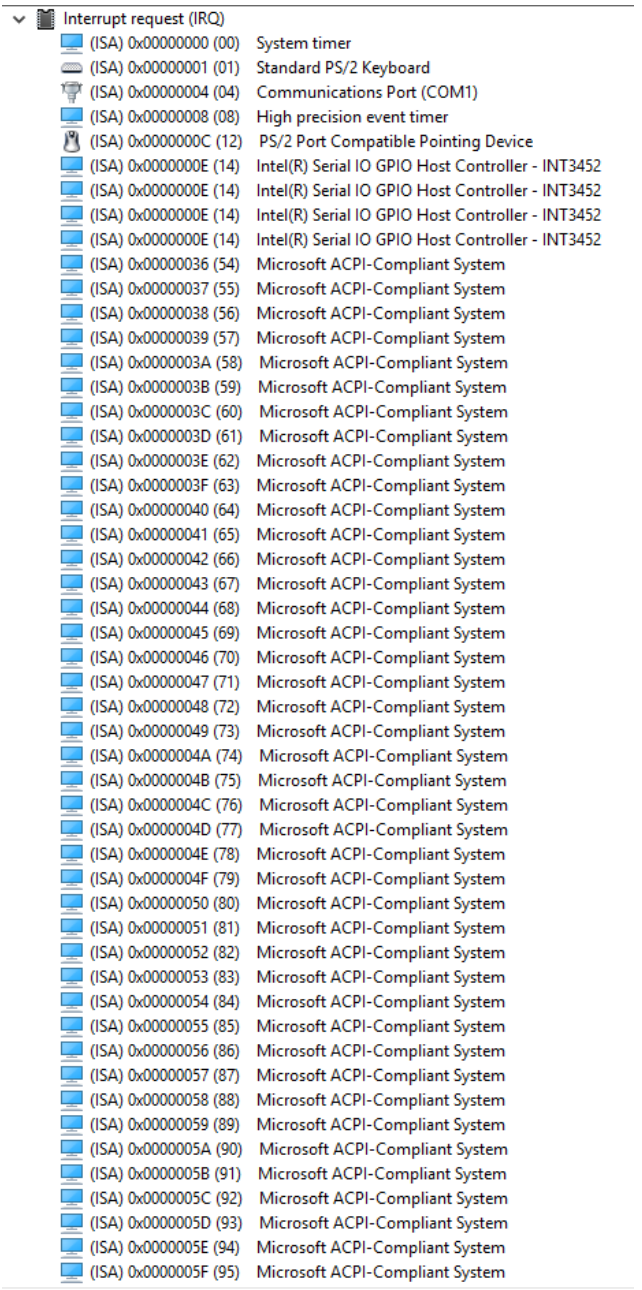

[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller

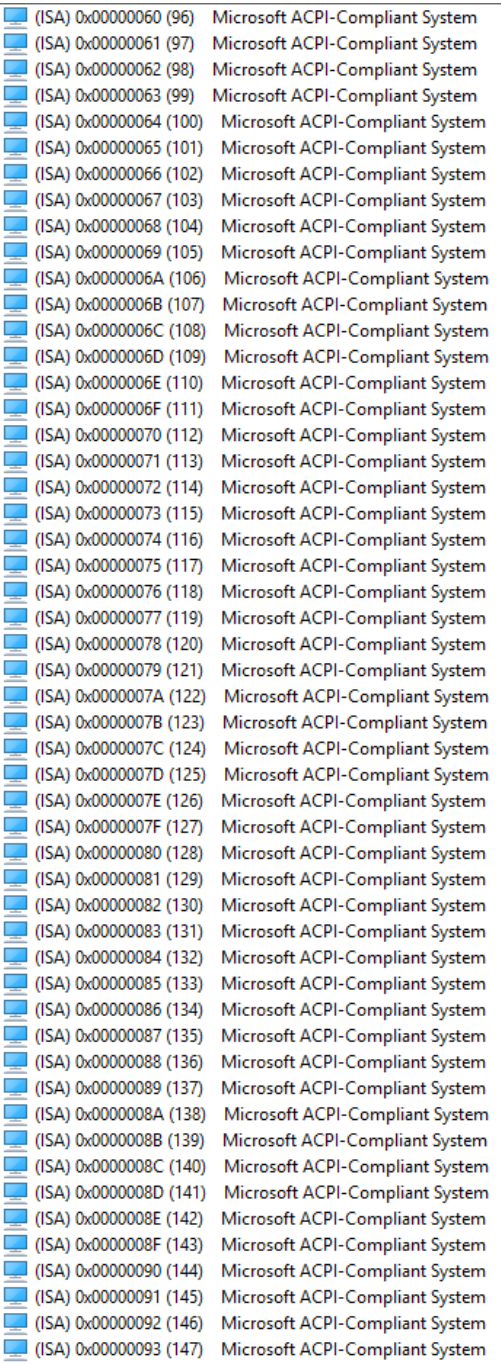
B.2 Memory Address Map



[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
[00000000FED80000 - 00000000FEDBFFFF] Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources

B.3 IRQ Mapping Chart

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(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
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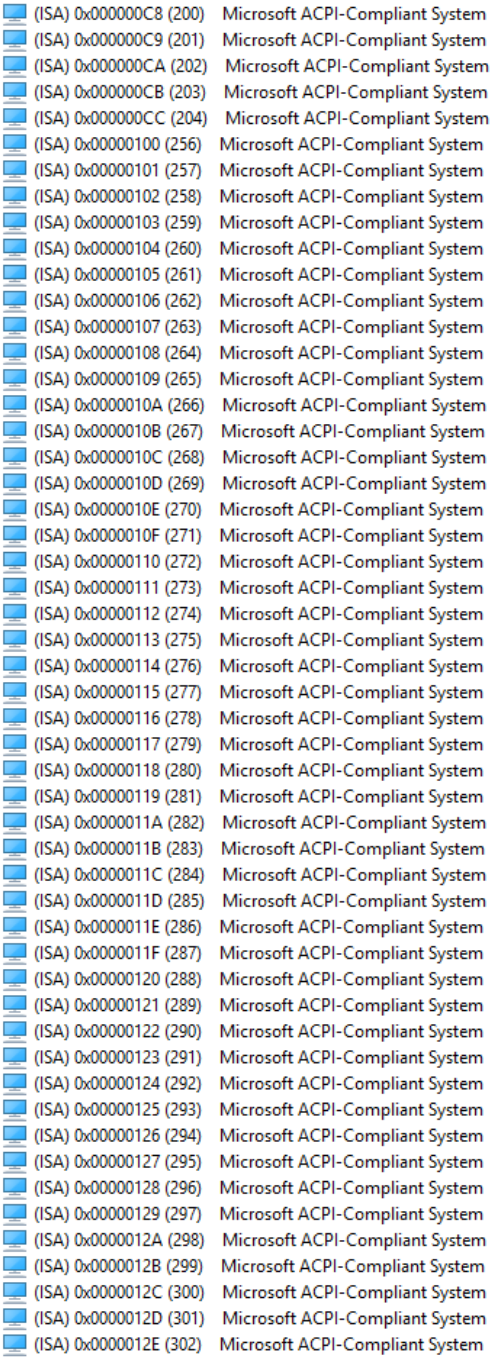
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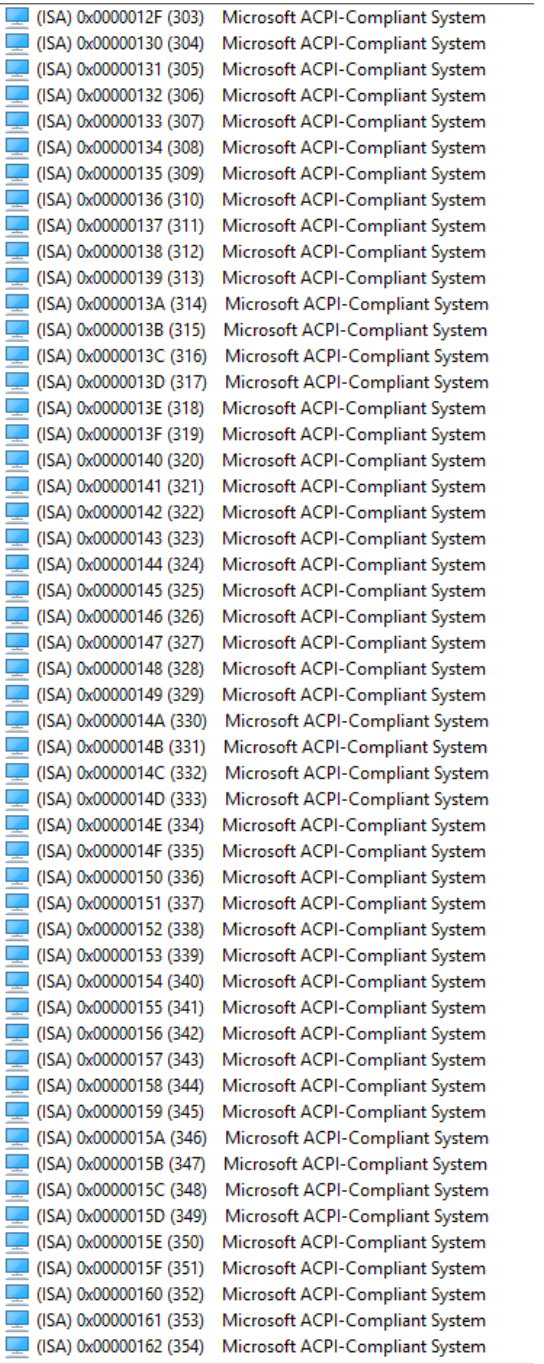
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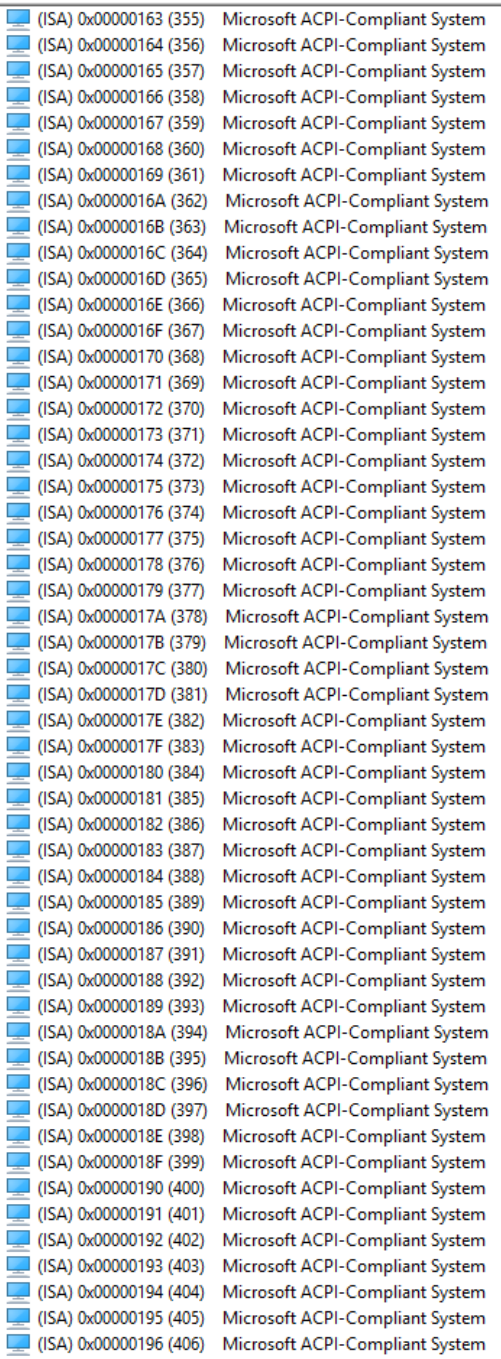

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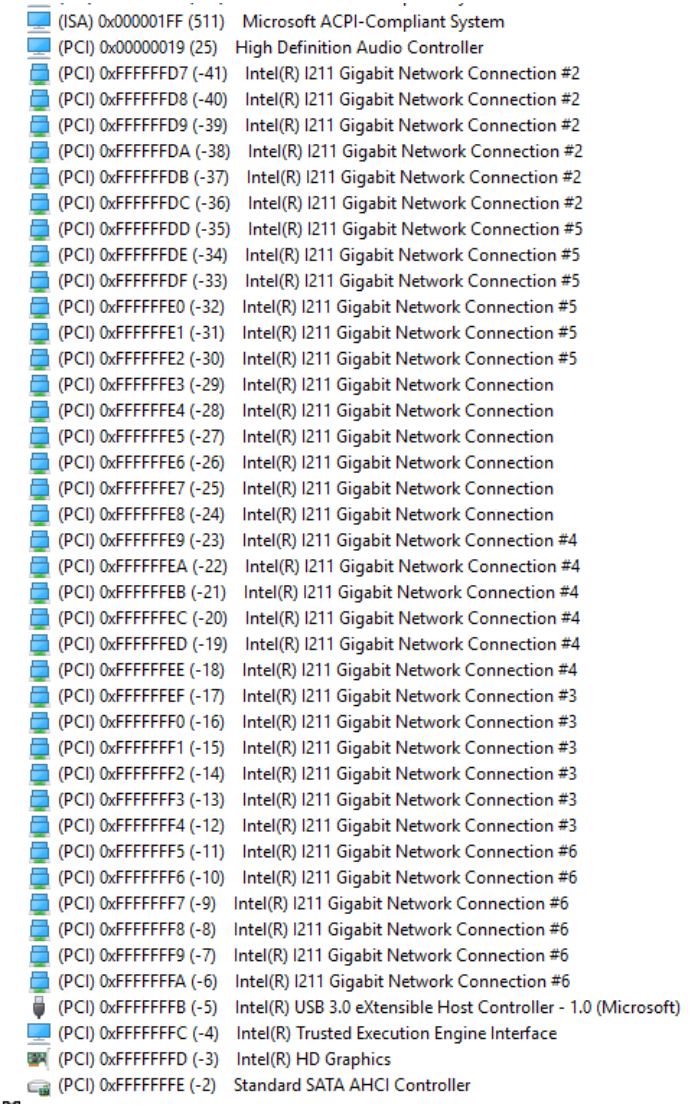
(ISA) 0x000001F1 (497) Microsoft ACPI-Compliant System
(ISA) 0x000001F2 (498) Microsoft ACPI-Compliant System
(ISA) 0x000001F3 (499) Microsoft ACPI-Compliant System
(ISA) 0x000001F4 (500) Microsoft ACPI-Compliant System
(ISA) 0x000001F5 (501) Microsoft ACPI-Compliant System
(ISA) 0x000001F6 (502) Microsoft ACPI-Compliant System
(ISA) 0x000001F7 (503) Microsoft ACPI-Compliant System
(ISA) 0x000001F8 (504) Microsoft ACPI-Compliant System
(ISA) 0x000001F9 (505) Microsoft ACPI-Compliant System
(ISA) 0x000001FA (506) Microsoft ACPI-Compliant System
(ISA) 0x000001FB (507) Microsoft ACPI-Compliant System
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System


(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000019 (25) High Definition Audio Controller
(PCI) 0xFFFFFFD7 (-41) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFD8 (-40) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFD9 (-39) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFDA (-38) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFDB (-37) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFDC (-36) Intel(R) I211 Gigabit Network Connection #2
(PCI) 0xFFFFFFDD (-35) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFDE (-34) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFDF (-33) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFE0 (-32) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFE1 (-31) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFE2 (-30) Intel(R) I211 Gigabit Network Connection #5
(PCI) 0xFFFFFFE3 (-29) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE4 (-28) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE5 (-27) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE6 (-26) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE7 (-25) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE8 (-24) Intel(R) I211 Gigabit Network Connection
(PCI) 0xFFFFFFE9 (-23) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFEA (-22) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFEB (-21) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFEC (-20) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFED (-19) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFEE (-18) Intel(R) I211 Gigabit Network Connection #4
(PCI) 0xFFFFFFEF (-17) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF0 (-16) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF1 (-15) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF2 (-14) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF3 (-13) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF4 (-12) Intel(R) I211 Gigabit Network Connection #3
(PCI) 0xFFFFFFF5 (-11) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFF6 (-10) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFF7 (-9) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFF8 (-8) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFF9 (-7) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFFA (-6) Intel(R) I211 Gigabit Network Connection #6
(PCI) 0xFFFFFFFB (-5) Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
(PCI) 0xFFFFFFFC (-4) Intel(R) Trusted Execution Engine Interface
(PCI) 0xFFFFFFFD (-3) Intel(R) HD Graphics
(PCI) 0xFFFFFFFE (-2) Standard SATA AHCI Controller

Appendix C

AAEON SDK Hardware Settings

C.1 Status LED

FWS-2275 provides a LED indicator which can change the LED status by AAEON SDK. User is able to program the LED status to express different status.

C.1.1 Status LED Configuration

The LED status indicator of FWS-2275 is programmable with AAEON SDK for your application.

Table1: LED Status

	STA_LED2	STA_LED1	STA_LED0
LED Off	0	0	0
Red	0	0	1
Red Blinking (Slowly)	0	1	0
Red Blinking (Quickly)	0	1	1
Reserved	1	0	0
Green Blinking (Slowly)	1	0	1
Green Blinking (Quickly)	1	1	0
Green	1	1	1

Table2: Status LED and register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

C.1.2 Sample Code

```
*************************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*************************************************************************************************
*****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
        //LED Off
        //BIT2=0, BIT1=0, BIT0=0
        bData = bData & 0xF8;
        break;
}
case 1:
{
        //Red LED On
        //BIT2=0, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x01;
        break;
}
case 2:
{
        //Red LED Blink
        //BIT2=0, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x02;
        break;
}
case 3:
{
        //Red LED Fast Blink
        //BIT2=0, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x03;
        break;
}
case 4:
```

```
{
        //Green LED On
        //BIT2=1, BIT1=1, BIT0=1
        bData = (bData & 0xF8) | 0x07;
        break;
}
case 5:
{
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
}
case 6:
{
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
}
default:
        break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*********************************************************************************************
*****
```

C.2 LAN Bypass

FWS-2275 provides LAN Bypass kit and allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

C.2.1 LAN Bypass

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table2: LAN Bypass register table

Function	Description
LAN_ID3	Use for selecting which LAN kit will be configured, refert to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID2	
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

C.2.2 Sample Code

```
*****************************************************************************************
*****
#define ByteCPLD_SLAVE_ADDRESS   //This parameter is represented from Note1
#define ByteOFFSET               //This parameter is represented from Note2
*****************************************************************************************
*****
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
        bData = bData | 0x08;
else
        bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
        bData = bData | 0x04;
else
        bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
        bData = bData | 0x02;
else
        bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
        bData = bData | 0x01;
else
        bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH)   // Pass Through
        bData = bData & 0xBF;
else                                    // Bypass
        bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH)   // Pass Through
```

```
        bData = bData & 0xDF;
else                                    // Bypass
        bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
        bData = bData & 0xEF;
else                                    // Bypass
        bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*********************************************************************************
```

C.3 Software Reset Button Configuration

FWS-2275 provides a general propose input button which status get by AAEON SDK.

C.3.1 Soft Reset Button Configuration

Table 2 : LAN Bypass relative register table	
Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1 : Soft Reset Button register mapping table					
	Attribute	Register(I/O)	BitNum	Value	Attribute
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)	BTN_STS

C.3.2 Sample Code

```
*****************************************************************************
#define Word        BTN_STS        //This parameter is represented from Note1
#define ByteBTN_STS_R              //This parameter is represented from Note2
*****************************************************************************
Byte    GET_Value (Word IoAddr, Byte BitNum,Byte Value){
        BYTE  TmpValue;

        TmpValue = inportb (IoAddr);
         return    (TmpValue & (1 << BitNum))
}
*****************************************************************************
VOID    Main(){
        Byte RstBtn;

        RstBtn = GET_Value (BTN_STS, BTN_STS_R);  // Active Low
}
*****************************************************************************
```