



FWS-2273

Desktop Network Appliance

User's Manual 5th Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2273	1
● SATA Cable	1
● SATA Power Cable	1
● Power Adapter	1
● Rubber Foot	4

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	○	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件仍符合欧盟指令 2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period))：10 年

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON System

QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯 醚(PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU and Memory	×	○	○	○	○	○
Hard Disk	×	○	○	○	○	○
LCD Modules	×	○	○	○	○	○
CD-ROM/DVD-ROM	×	○	○	○	○	○
Touch Modules	×	○	○	○	○	○
Power	×	○	○	○	○	○
Battery	×	○	○	○	○	○
The table is prepared in accordance with the provisions of SJ/T 11364. ○ : Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572. × : Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1). EFUP (Environment Friendly Use Period) value: 10 years. Notes: 1. This product defined period of use is under normal condition. 2. In above part, CPU/Memory/ Hard Disk/CD-ROM/DVD-ROM/ Power are optional. 3. In above part, LCD Modules/ Touch Modules are for all-in-one product model.						

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Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	Desktop Network Appliance
Processor	Intel® Celeron® N3350 Processor SoC
Chipset	Intel® Celeron® N3350 Processor SoC
System Memory	DDR3L 1866MHz Single-Channel SODIMM x 1 (Max. 8GB, up to 1600MHz)

Note: To avoid random non-booting issue caused by the incompatibility of Intel® Pentium® Processor N Series with certain unstable 1866MHz memories, memory with frequency greater than 1600MHz will automatically fix to 1600MHz, while memory that runs at a speed lower than 1600MHz will maintain its original speed.

Network

Ethernet	Intel® Ethernet Controller I210, GbE x 4 Intel® Ethernet Controller I210, SFP x 2
Bypass	Supports up to 2 pairs LAN bypass function

Display

Graphic Controller	Integrated Intel® HD Graphics 505
Connector	HDMI x 1

Storage

HDD	2.5" HDD Bay x 1
CF/CFast/mSATA	CompactFlash™ Socket x 1 (Colay for BOM, optional CFast™ Socket x 1) SATA 6Gb/s x 1

Expansion Interface

PCIe Slot	—
Mini-PCIe Slot	Full-size Mini Card with SIM Socket x 2
KB Mouse	Reserve Pin Header
USB	USB 3.0 x 2

Miscellaneous

RTC	Internal RTC
Watchdog Timer	1~255 steps by software programmable
TPM	(TPM v1.2 9660/TPM 2.0 9665 Optional)
GPIO	Reserve internal Pin Header 8-bit Digital I/O interface (4-in/4-out)
Fan	Fanless, Reserved Pin Header for System Fan
MTBF (Hours)	109,725
Color	Black

I/O

Front Panel	Power LED x 1
	Status LED x 1
	Storage Active LED x 1
	Bypass LED x 2
	LAN LED x 12
Rear Panel	USB 3.0 Port x 2
	RJ-45 x 4
	SFP x 2
	RJ-45 Console x 1
	12V DC Power Input x 1
	Software Reset Button x 1

I/O

Rear Panel (Cont.)	Power Button x 1,
	HDMI x 1
	Antenna Hole x 2

Environmental Parameters and Dimension

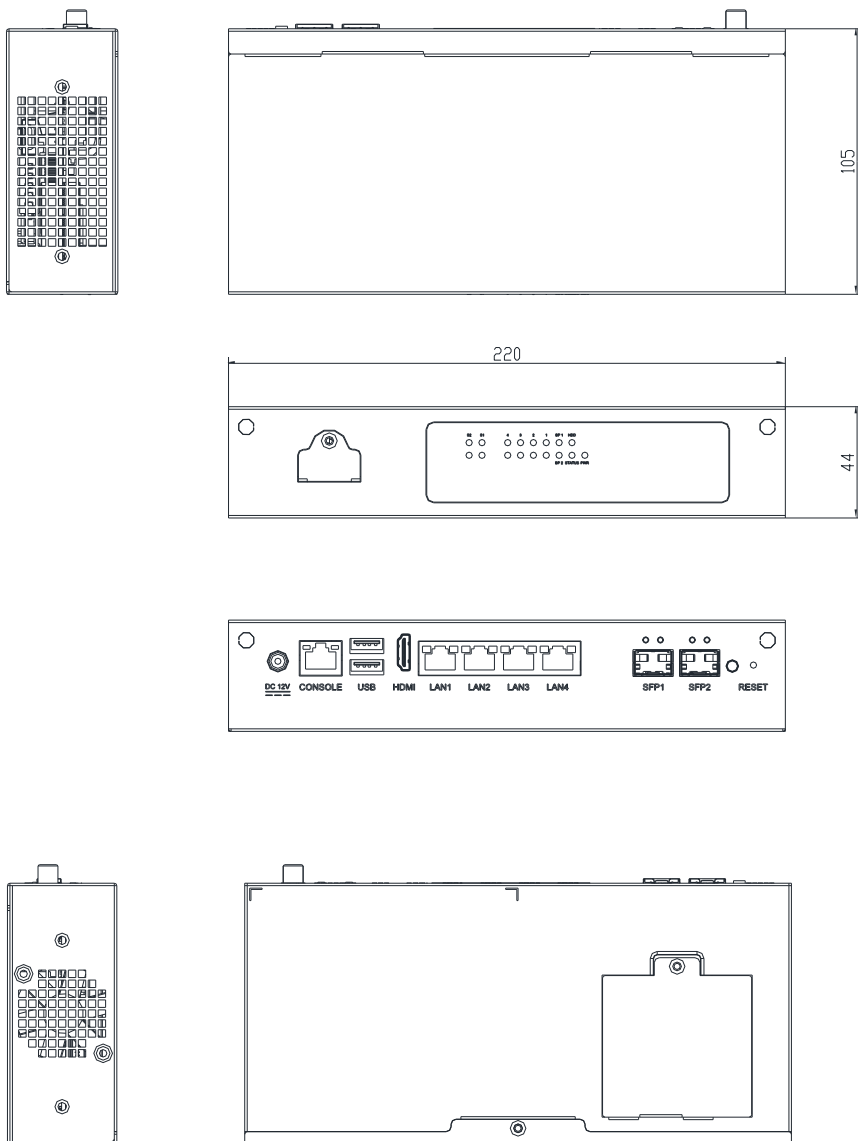
Power Requirement	12V DC-In
Operating Temperature	32°F ~ 104°F (0°C ~ 40°C)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10% ~ 80% relative humidity, non-condensing
Storage Humidity	10% ~ 80% @40°C; non-condensing
Vibration	0.5 Grms/ 5 ~ 500Hz/ operation (2.5" HDD)
	1.5 Grms/ 5 ~ 500Hz/ non-operation
Shock	10 G peak acceleration (11 m sec. duration), operation
	20 G peak acceleration (11 m sec. duration), non-operation
Dimension (W x D x H)	8.66" x 4.13" x 1.73" (220mm x 105mm x 44mm)

Chapter 2

Hardware Information

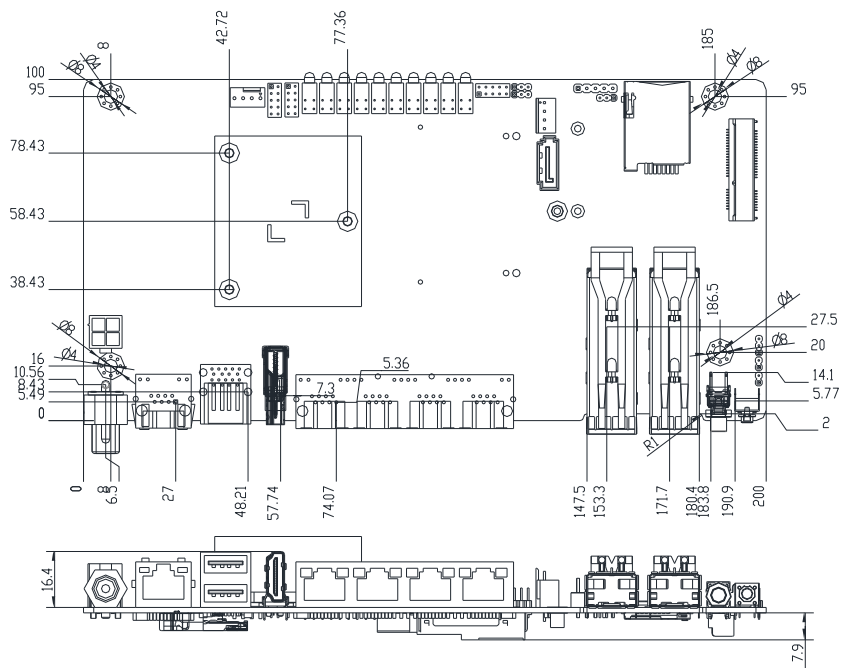
2.1 Dimensions

System

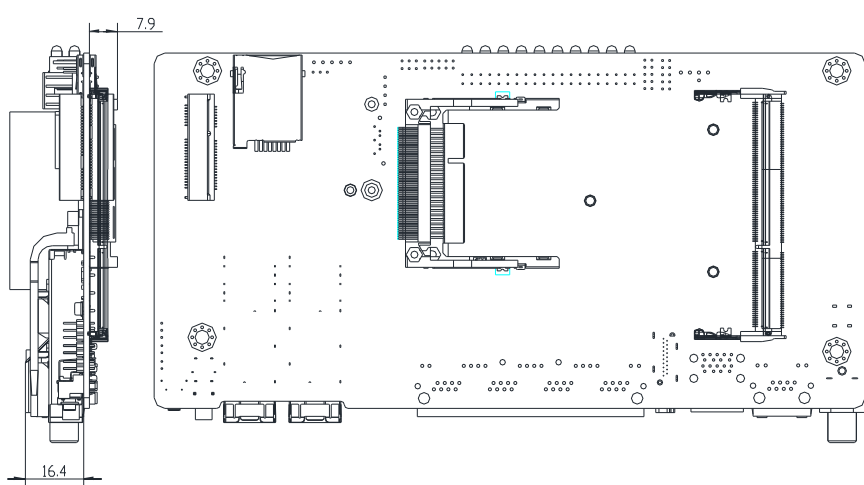


Board

Component Side

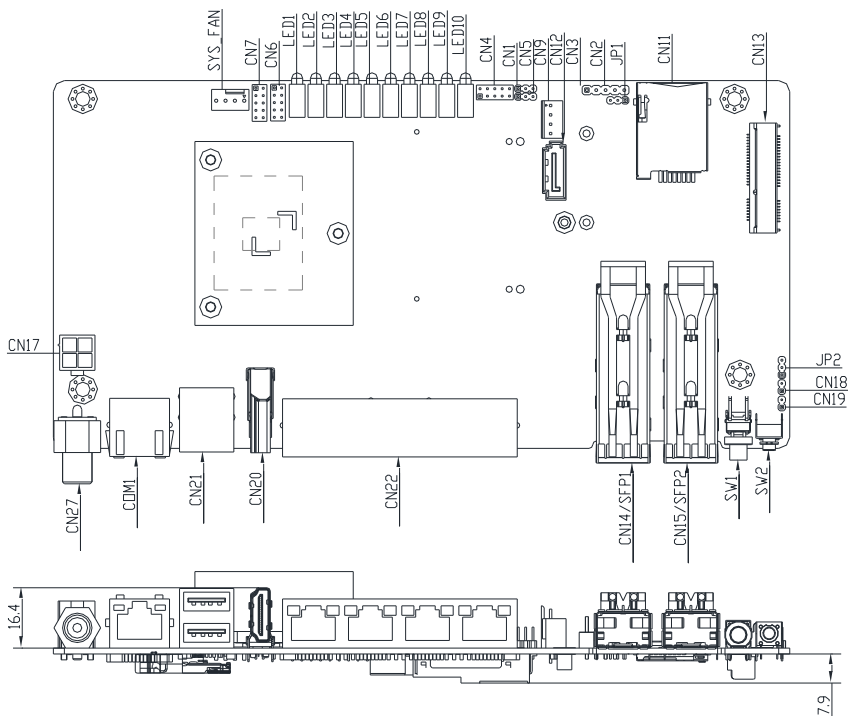


Solder Side

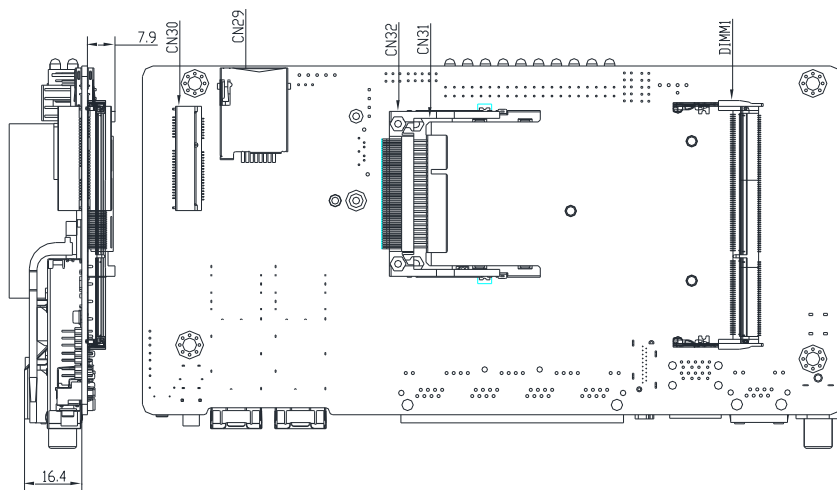


2.2 Jumpers and Connectors

Component Side



Solder Side

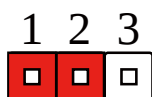
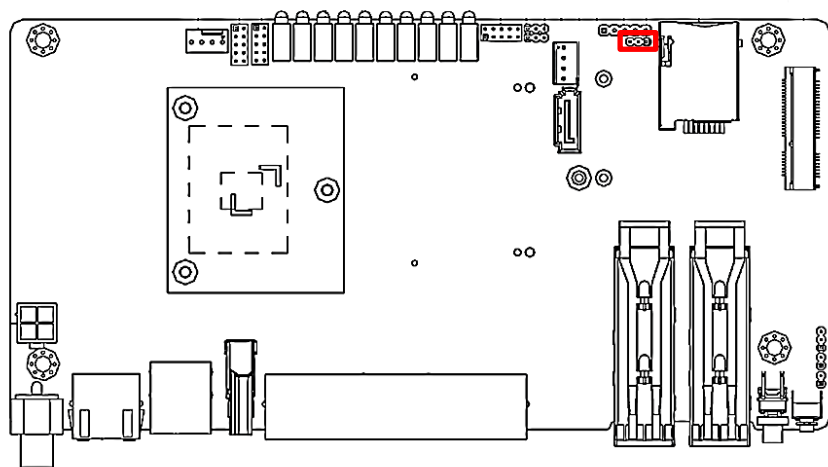


2.3 List of Jumpers

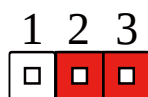
Please refer to the table below for all of the board’s jumpers that you can configure for your application

Label	Function
JP1	CF Power Selection
JP2	Auto PWRBTN Selection
CN1	CMOS Setting Selection

2.3.1 CFD Voltage 3.3V/5V Selection (JP1)

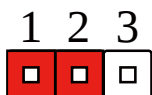
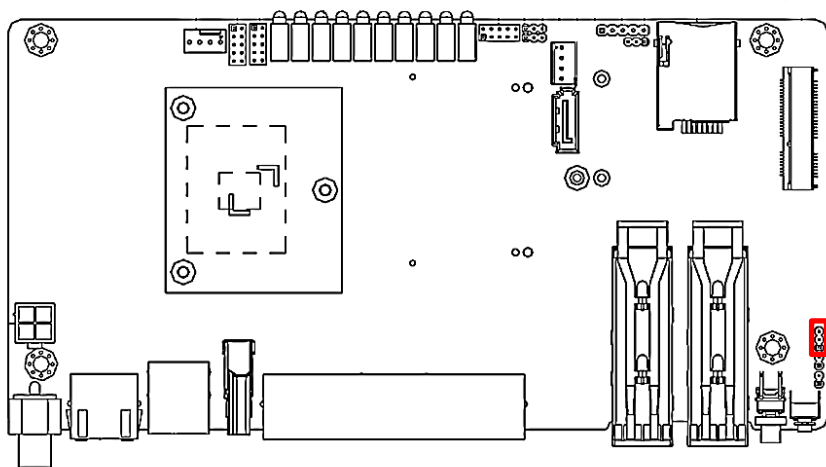


5V

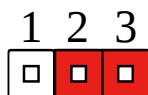


3.3V (Default)

2.3.2 Auto PWRBTN Selection (JP2)

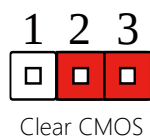
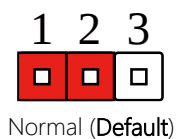
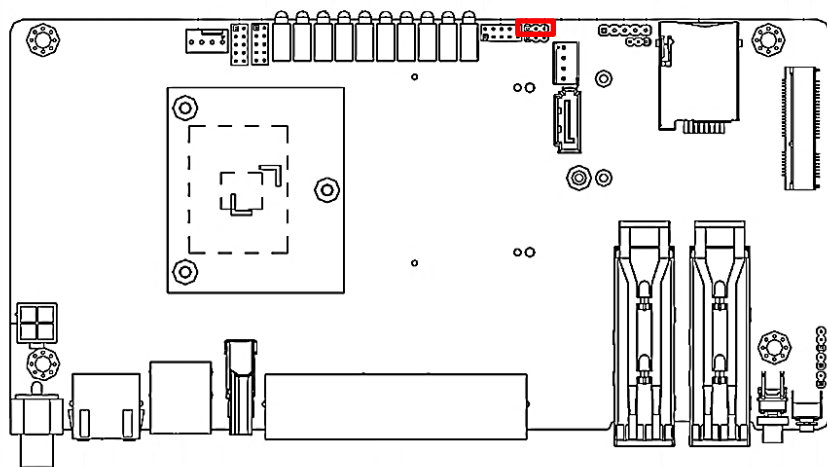


Don't use Auto PWRBTN (Default)



Use Auto PWRBTN

2.3.3 CMOS Setting Selection (CN1)

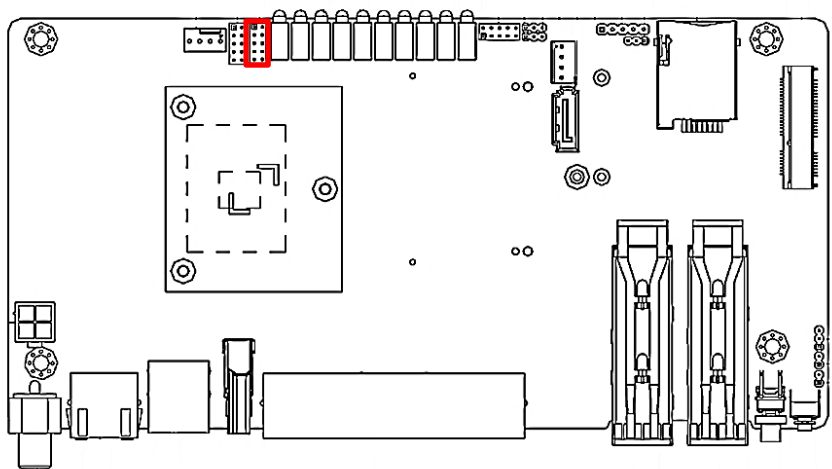


2.4 List of Connectors

Please refer to the table below for all of the board’s connectors that you can configure for your application

Label	Function
DIMM1	DDR3L SODIMM Socket
CPU_FAN1	4P Smart Fan
CON1	COM Port
CN12	SATA Interface
CN9	SATA Power
CN13	Mini PCIe Socket (USB 2.0 Only)
CN30	Mini PCIe Socket
CN31	CF Card Socket
CN11/ CN29	SIM Card Socket
CN18	Reset Button
CN19/SW1	Power Button
CN21	Dual USB 3.0 Port
CN6	Digital I/O
CN22	RJ-45 LAN 1-4
SFP1	SFP LAN 5
SFP2	SFP LAN 6
CN7	Dual USB 2.0 Port Pin Header
SW2	Software Reset
CN3	Battery Socket
CN4	Front Panel Pin Header
LED1	Power LED
LED2	HDD/Stats LED
LED3	Bypass LED
LED4-LED7	RJ-45 LAN Link Stats LED
LED9-LED10	SFP LAN Link Stats LED

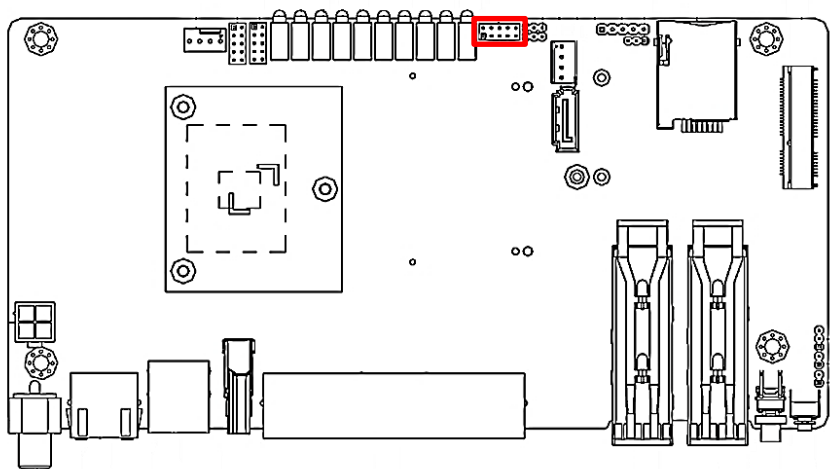
2.4.1 Digital I/O (CN6)



This connector offers 4-pair of digital I/O functions and address is 801H. The pin definitions are illustrated below:

Pin	Signal	Pin	Signal
1	Digital- IN/OUT(Port1 Bit 1)	2	Digital- IN/OUT (Port1 Bit 2)
3	Digital- IN/OUT (Port1 Bit 4)	4	Digital- IN/OUT (Port1 Bit 5)
5	Digital- IN/OUT (Port3 Bit 4)	6	Digital- IN/OUT (Port3 Bit 5)
7	Digital- IN/OUT (Port6 Bit 3)	8	Digital- IN/OUT (Port4 Bit 7)
9	+5V	10	GND

2.4.2 Front Panel Pin Header (CN4)



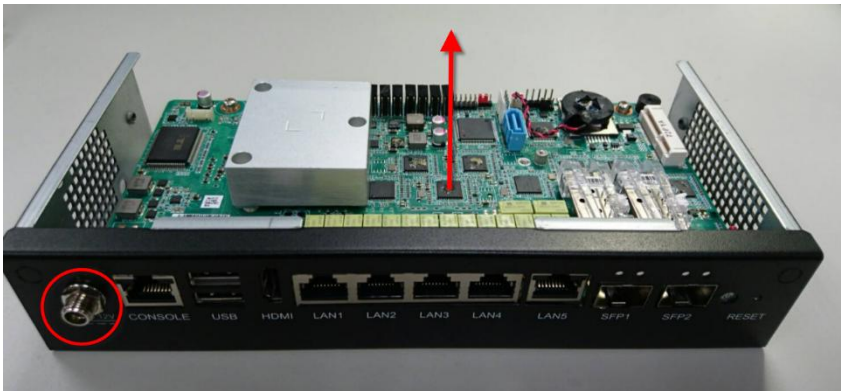
Pin	Signal	Pin	Signal
1	GND	2	POWER LED
3	HDD LED(-)	4	HDD LED(+)
5	BPLED1(-)	6	BPLED1(+)
7	BPLED2(-)	8	BPLED2(+)
9	Stats Led Red	10	Stats Led Green

2.5 2.5" Hard Disk Drive Installation

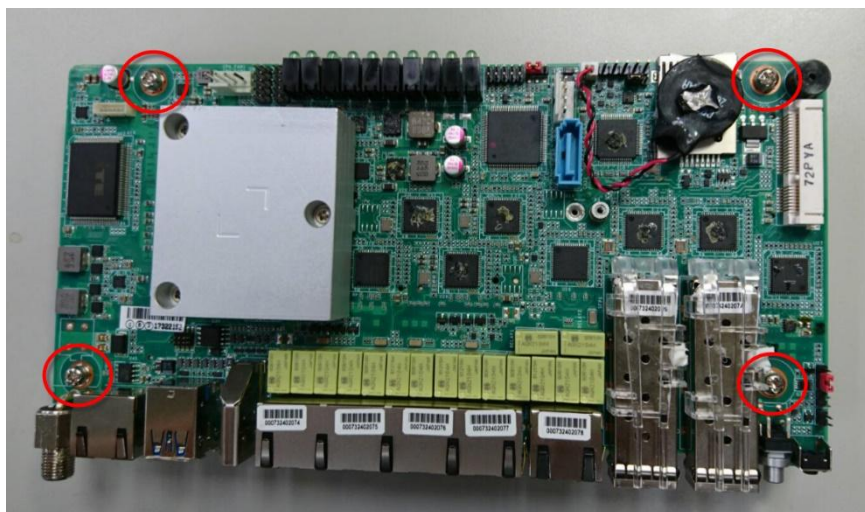
1. Loosen the screw and remove the top case from the lower side.



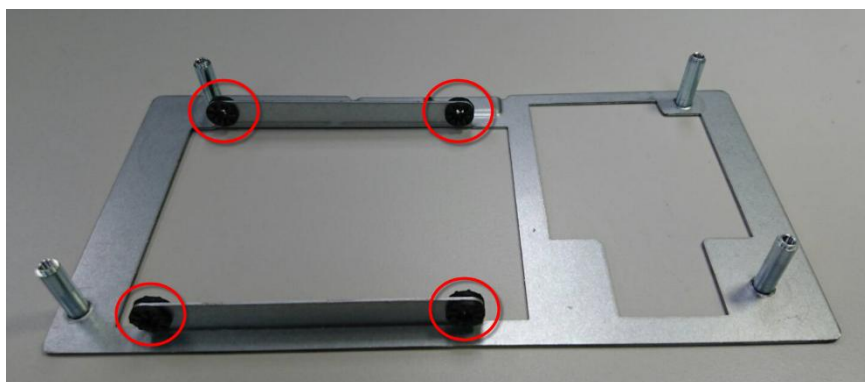
2. Loosen the screw and remove the motherboard module.



3. Loosen the four (4) screws and remove the motherboard.



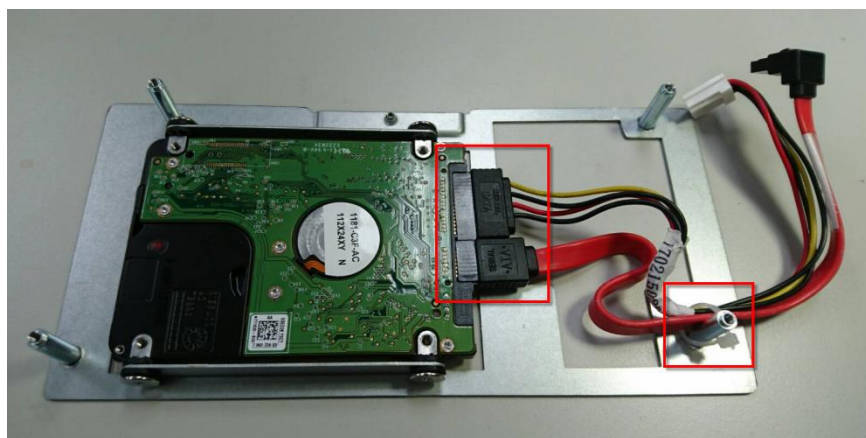
4. Put the assembled cushions on the hard disk driver bracket.



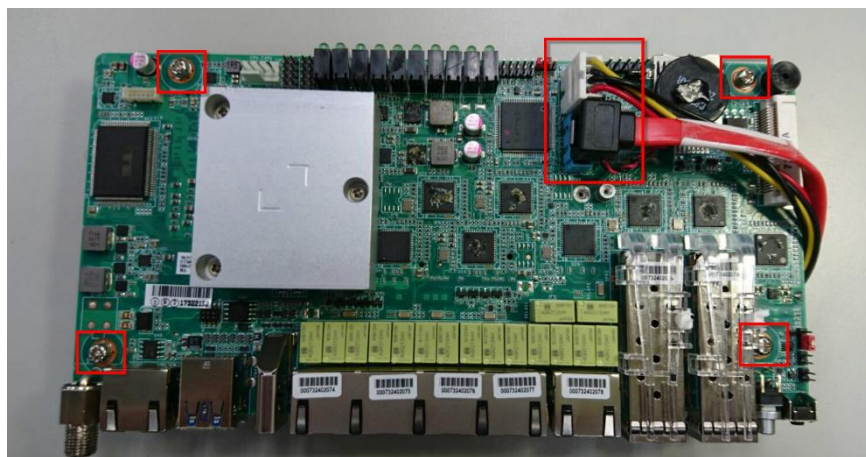
5. Lock the HDD onto the cushions with the four screws.



6. Connect the SATA cable and power cable into the Hard Disk, and lock in the cable with the cable ties.



7. Connect the SATA cable and the power cable onto the motherboard, and lock in the motherboard with the four (4) screws.



8. Put the assembled motherboard module onto the bottom case, and lock the screw.



9. Put the assembled top case onto the bottom case.



10. Lock the screw.



2.6 Mini PCIe Card Installation

1. Unscrew the Mini PCIe card cover lid.



2. Push the Mini PCIe card into the slot



3. Lock down the Mini PCIe card with the screw.



4. Lock down the Mini PCIe card cover with the screw.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The FWS-2273 CMOS memory has an integral lithium battery backup for data retention. You have to replace the battery when it finally runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

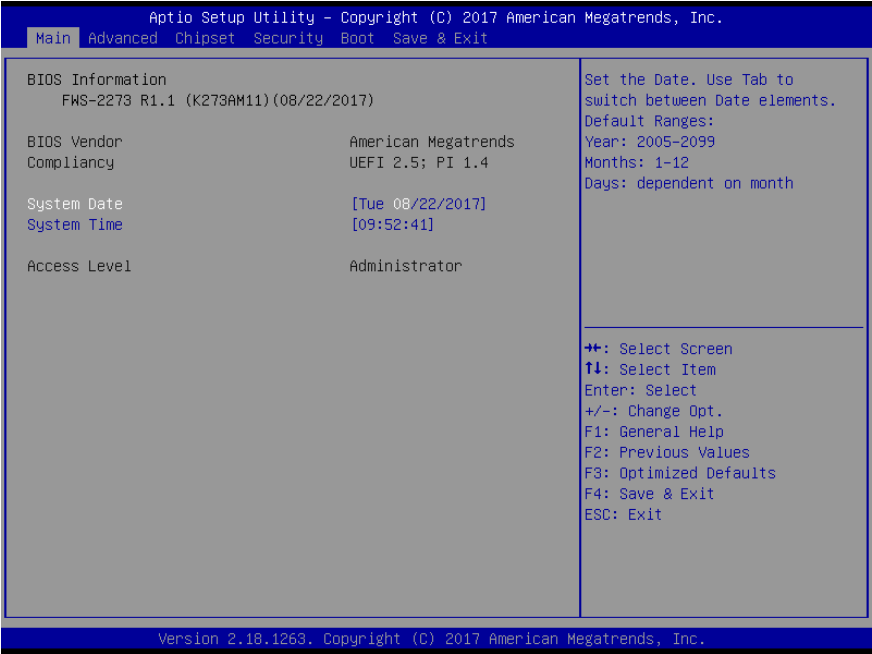
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

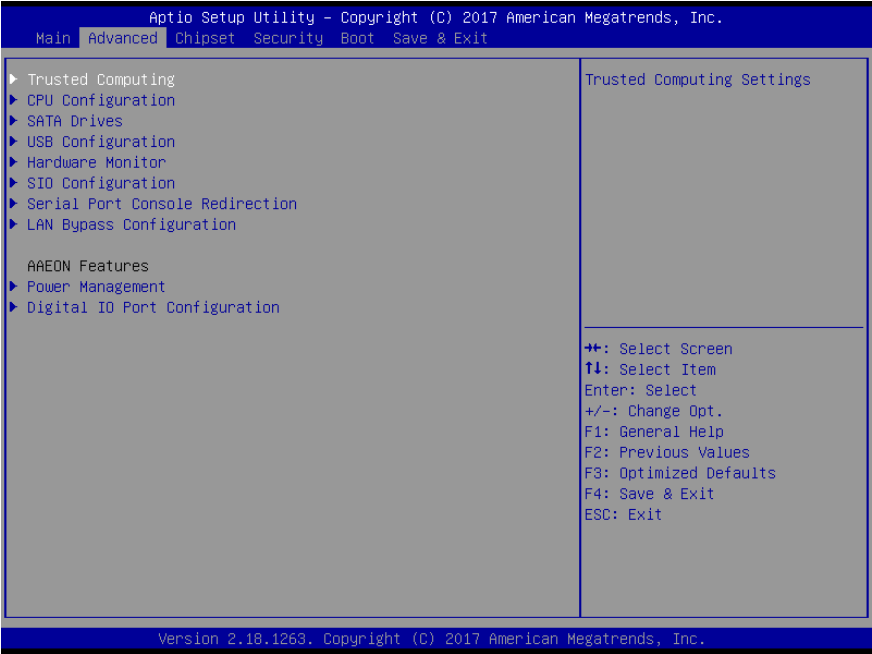
Boot – Enable/ Disable quiet Boot Option

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



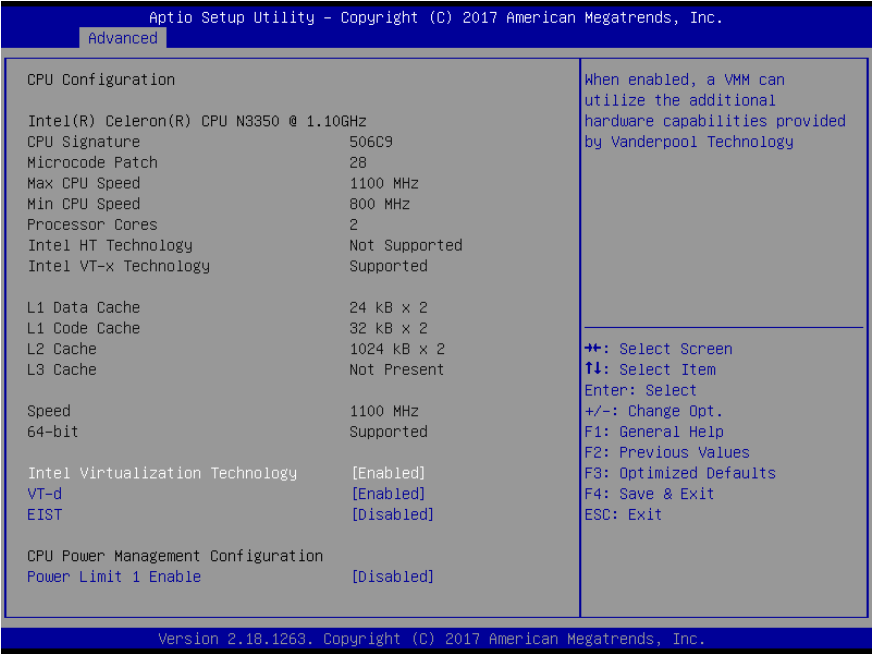
3.4.1 Trusted Computing



Options Summary	
Security Device Support	Disabled
	Enabled
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.	
SHA-1 PCR Bank	Disabled
	Enabled
Enable or Disable SHA-1 PCR Bank.	
SHA256 PCR Bank	Disabled
	Enabled
Enable or Disable SHA256 PCR Bank.	
Pending operation	None
	TPM Clear
Schedule an Operation for the Security Device.	
NOTE: Your Computer will reboot during restart in order to change State of Security Device.	

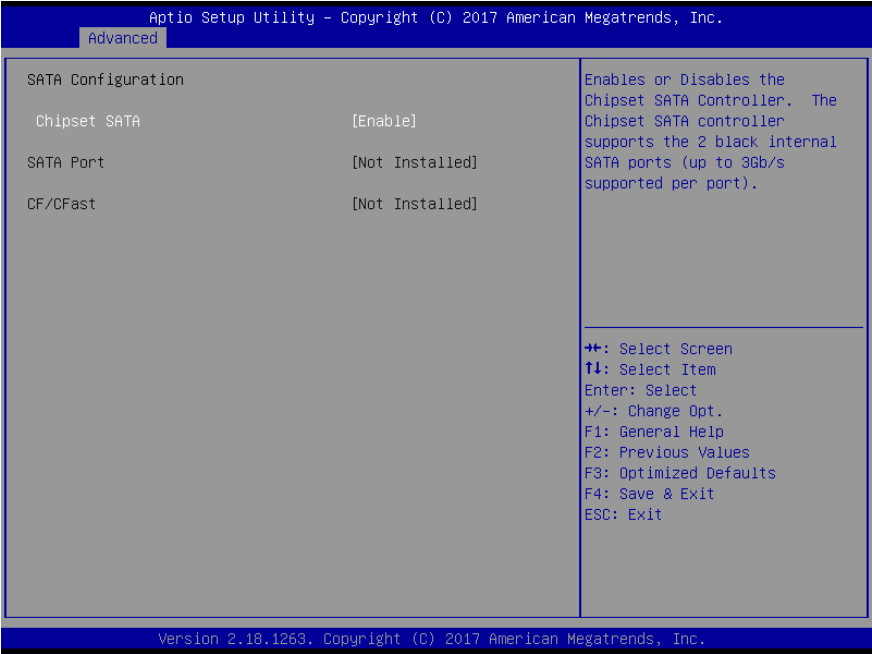
Options Summary	
Platform Hierarchy	Disabled
	Enabled
Enable or Disable Platform Hierarchy.	
Storage Hierarchy	Disabled
	Enabled
Enable or Disable Storage Hierarchy.	
Endorsement Hierarchy	Disabled
	Enabled
Enable or Disable Endorsement Hierarchy.	
TPM2.0 UEFI Spec Version	TCG_1_2
	TCG_2
Select the TCG2 Spec Version Support. TCG_1_2: The Compatible mode for Win8/Win10. TCG_2: Support new TCG2 protocol and event format for Win10 or later.	
Physical Presence Spec Version	1.2
	1.3
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	
Device Select	TPM 1.2
	TPM 2.0
	Auto
TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices if not found. TPM 1.2 devices will be enumerated.	

3.4.2 CPU Configuration



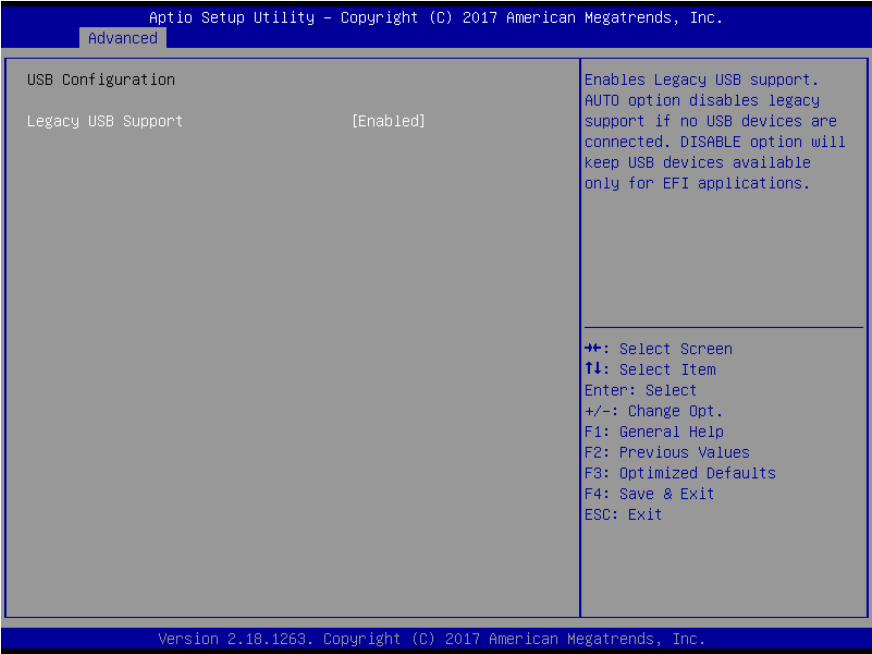
Options Summary	
Intel Virtualization Technology	Disabled
	Enabled
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.	
VT-d	Disabled
	Enabled
Enable/Disable CPU VT-d.	
EIST	Disabled
	Enabled
Enable/Disable Intel SpeedStep.	
Power Limit 1 Enable	Disabled
	Enabled
Enable/Disable Power Limit 1.	

3.4.3 SATA Drives



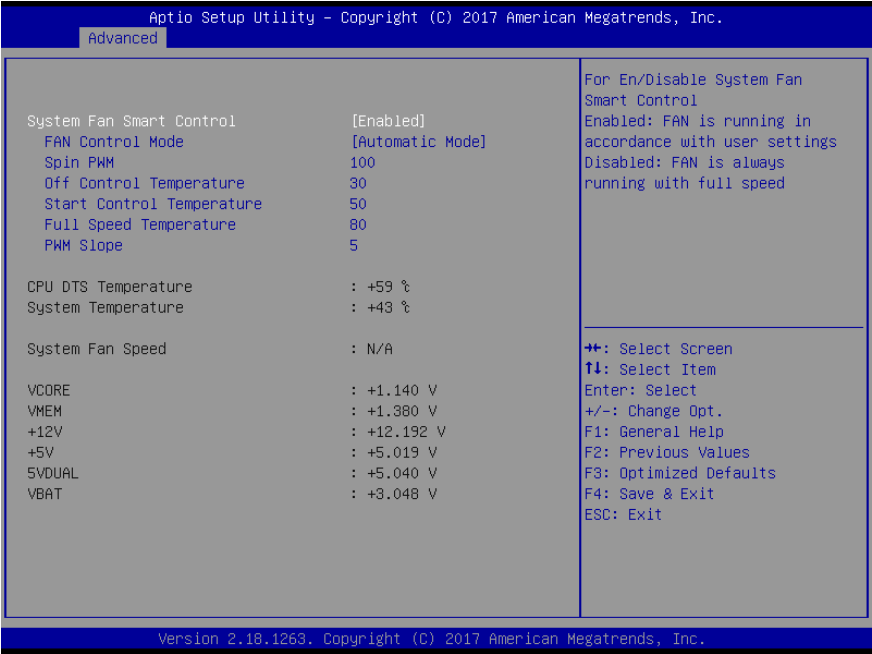
Options Summary	
Chipset SATA	Disabled
	Enabled
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).	

3.4.4 USB Configuration



Options Summary	
Legacy USB Support	Disabled
	Enabled
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	

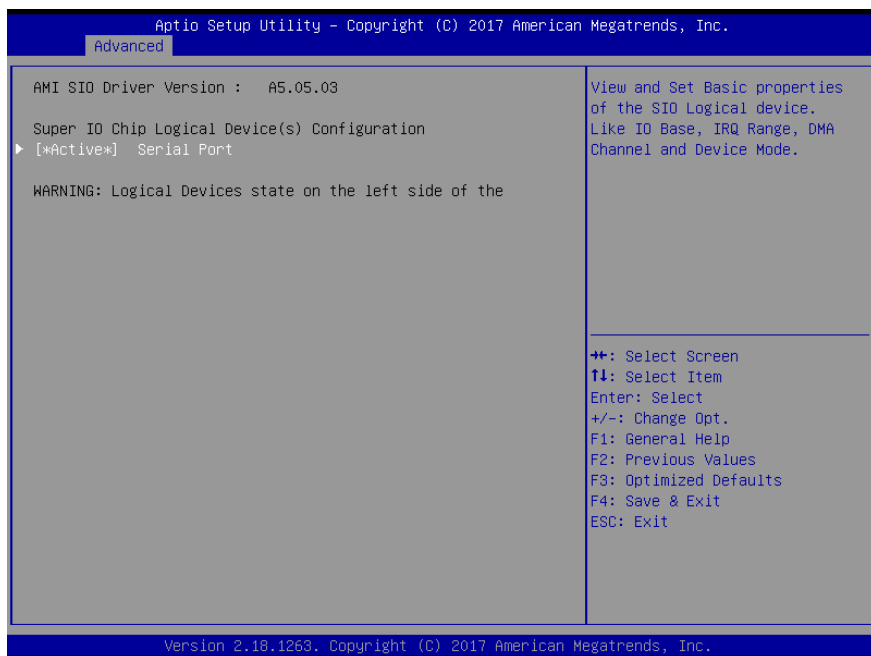
3.4.5 Hardware Monitor



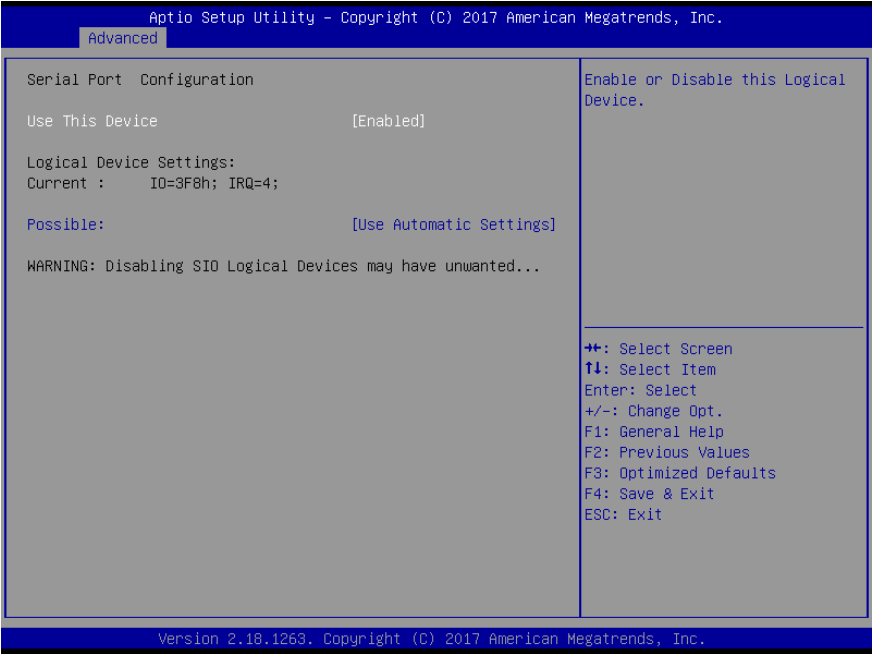
Options Summary	
System Fan Smart Control	Disabled
	Enabled
For Enable/Disable Fan 1 Smart Control. Enabled: FAN is running in accordance with user settings. Disabled: FAN is always running with full speed.	
Fan Control Mode	Automatic Mode
	Manual Mode
Manual Mode: Depends on PWM Duty. Automatic Mode: FAN Speed depends on System Temperature.	
Spin PWM	100 (0-255)
The PWM Duty of FAN Spin. Range:[0 - 255].	
Off Control Temperature	30 (0-127)
Temperature Limit Value of Fan Off. Note: Some fans have the minimum speed even if the PWM value is 0.	

Options Summary	
Start Control Temperature	50 (0-127)
Temperature Limit Value of FAN Start Control.	
Full Speed Temperature	80
Temperature Limit Value of FAN Full Speed.	
PWM Slope	5 (1-15)
Slope PWM value/Degree C for FAN Speed Control. Range: [1-15].	

3.4.6 SIO Configuration

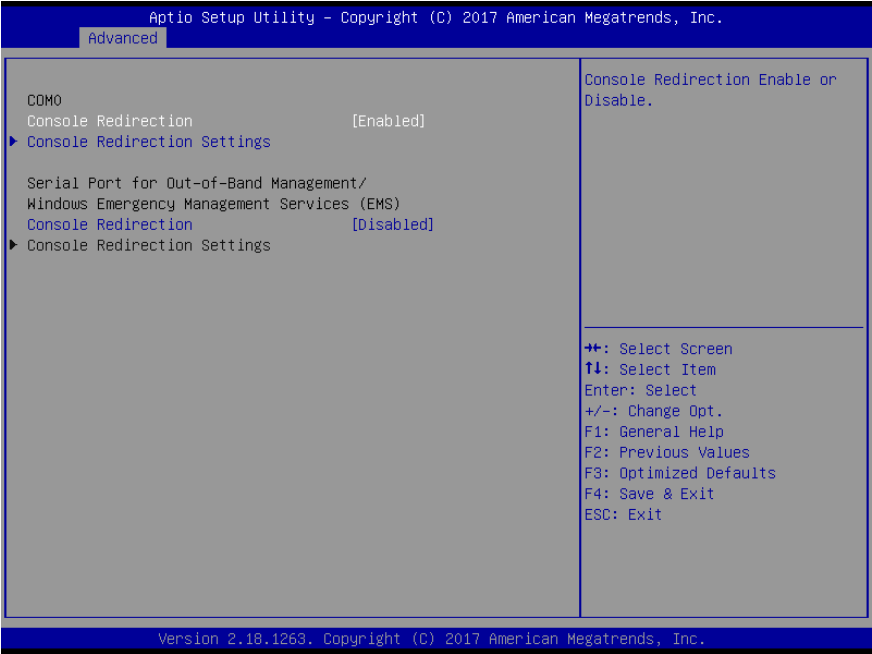


3.4.6.1 Serial Port Configuration



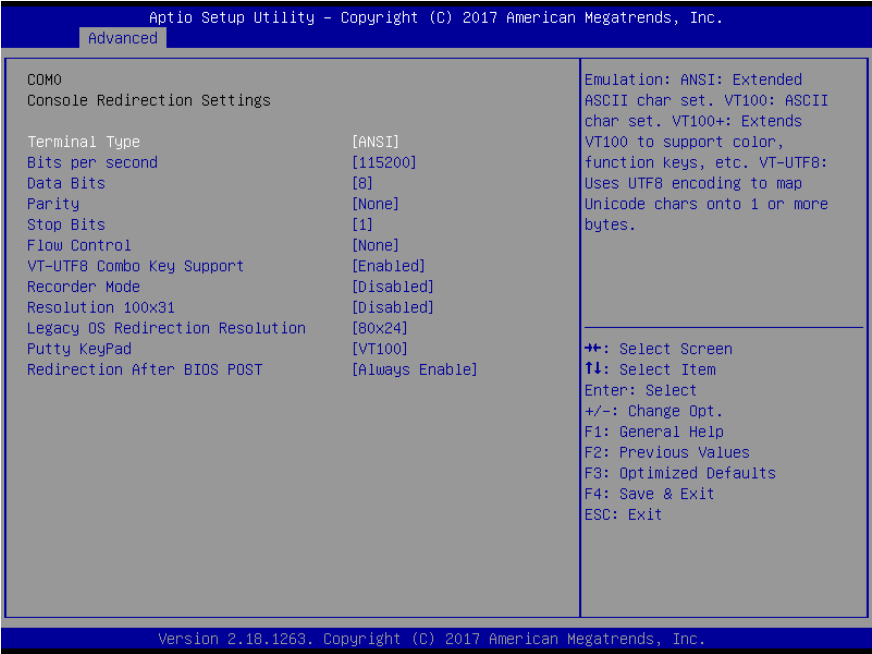
Options Summary	
Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

3.4.6.1.1 Serial Port Console Redirection



Options Summary	
Console Redirection	Disabled
	Enabled
Console Redirection Enabled or Disabled.	

3.4.6.1.2 Console Redirection Settings

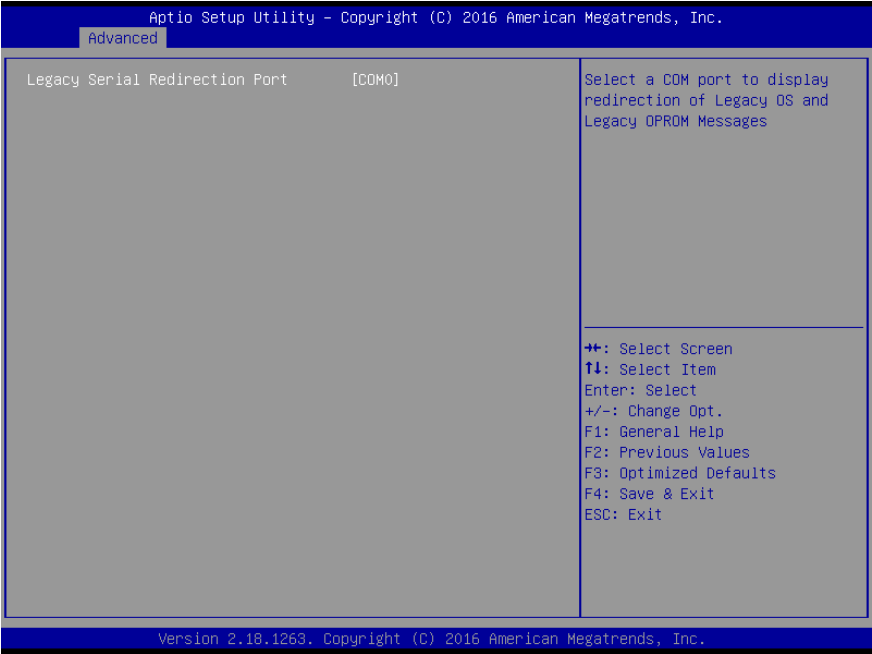


Options Summary	
Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	
Bits per second	9600
	19200
	38400
	57600
	115200

Options Summary	
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Data Bits	7
	8
Data Bits.	
Parity	None
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	1
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	
Flow Control	None
	Hardware RTS/CTS
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
VT-UTF8 Combo Key Support	Disabled
	Enabled
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.	
Recorder Mode	Disabled
	Enabled
On this mode enabled only text will be send. This is to capture Terminal data.	
Resolution 100x31	Disabled
	Enabled
Enables or disables extended terminal resolution.	
Legacy OS Redirection Resolution	80x24
	80x25
On Legacy OS, the Number of Rows and Columns supported redirection.	

Options Summary	
Putty KeyPad	VT100
	LINUX
	XTERMR6
	SCO
	ESCN
	VT400
Select FunctionKey and KeyPad on Putty.	
Redirection After BIOS POST	Always Enable
	BootLoader
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.	

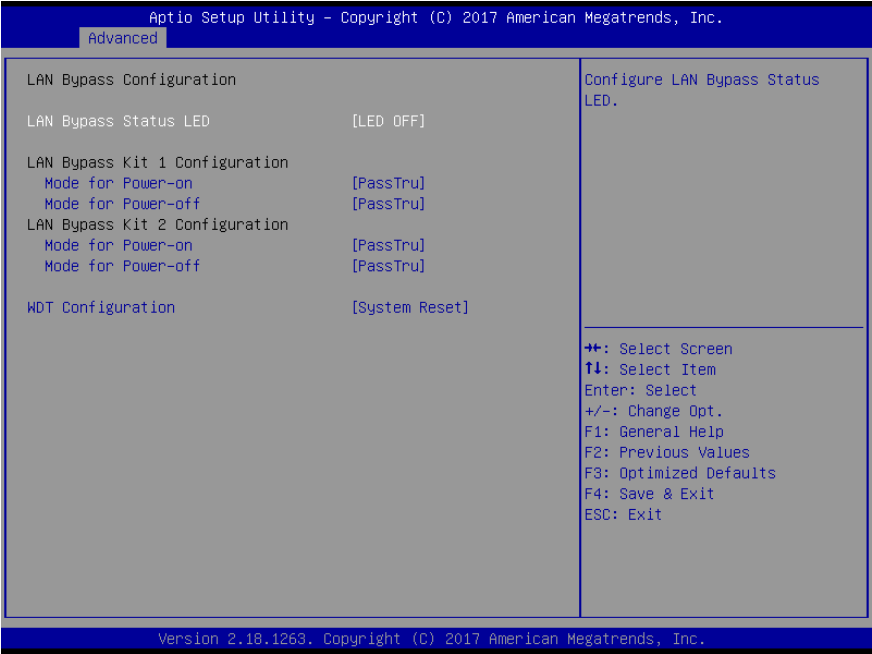
3.4.6.1.3 Serial Port for OOB Mgmt/Windows EMS



Options Summary	
Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.	
Bits per second	9600
	19200
	57600
	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	

Options Summary	
Flow Control	None
	Hardware RTS/CTS
	Software Xon/Xoff
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
Data Bits	7
	8
Data Bits.	
Parity	None
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	1
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	

3.4.6.1.4 LAN Bypass Configuration



Options Summary	
STATUS LED CTRL	LED OFF
	RED LED ON
	RED LED BLINK
	RED LED FAST BLINK
	GREEN LED ON
	GREEN LED BLINK
	GREEN LED FAST BLINK
Configure LAN Bypass Status LED.	
LAN kit Power ON	Bypass
	PassTru
Setting LAN kit function behavior when power on.(Bypass/Pass Through)	
LAN kit Power Off	Bypass
	PassTru
Setting LAN kit function behavior when power off.(Bypass/Pass Through)	

Options Summary	
WDT configuration	Force Bypass
	SystemReset
Configure WDT behavior. System Reset. Force Bypass.	

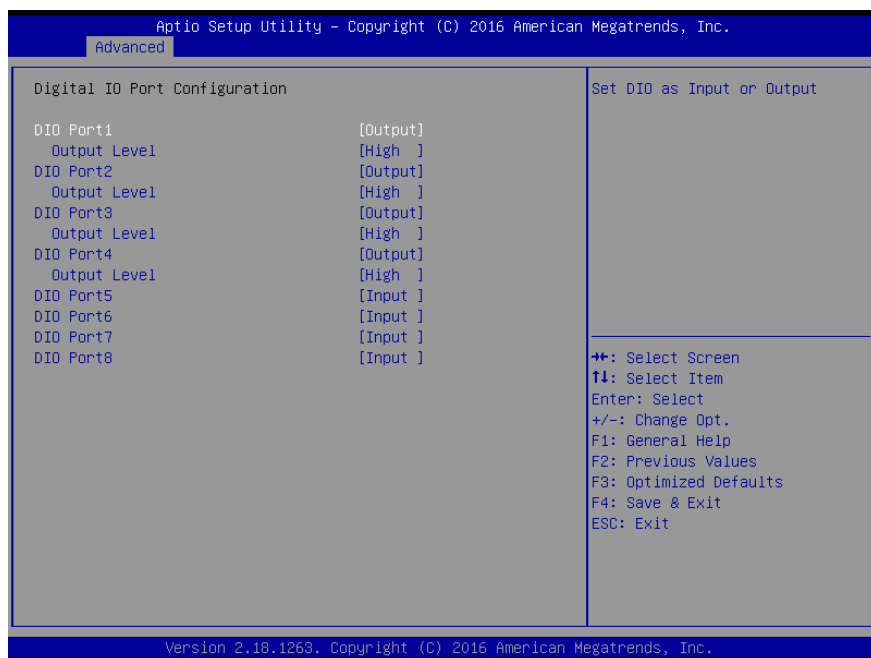
3.4.7 Advanced: Power Management



Options Summary	
Power Mode	ATX Type
	AT Type
Select Power Supply Mode.	
Restore AC Power Loss	Power Off
	Power On
	Last State
Select AC power state when power is re-applied after a power failure.	

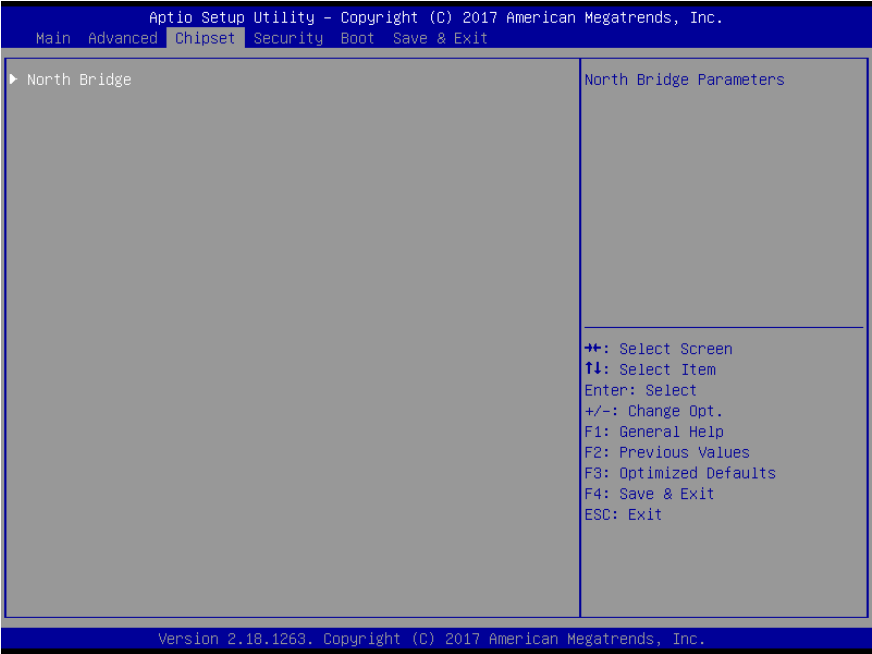
Options Summary	
RTC Wake system from S5	Disabled
	Fixed time
	Dynamic time
Fixed Time: System will wake on the hr::min::sec specified.	
Dynamic Time: System will wake on the current time + Increase minute(s).	
Wake up day (Fixed time option)	0
Select 0 for daily system wake up, 1-31 for which day of month that you would like the system to wake up.	
Wake up hour (Fixed time option)	0
Select 0-23 For example enter 3 for 3am and 15 for 3pm.	
Wake up minute (Fixed time option)	0
0-59.	
Wake up second (Fixed time option)	0
0-59.	
Wake up minute increase (Dynamic time option)	1
1-5.	

3.4.8 Digital IO Port Configuration

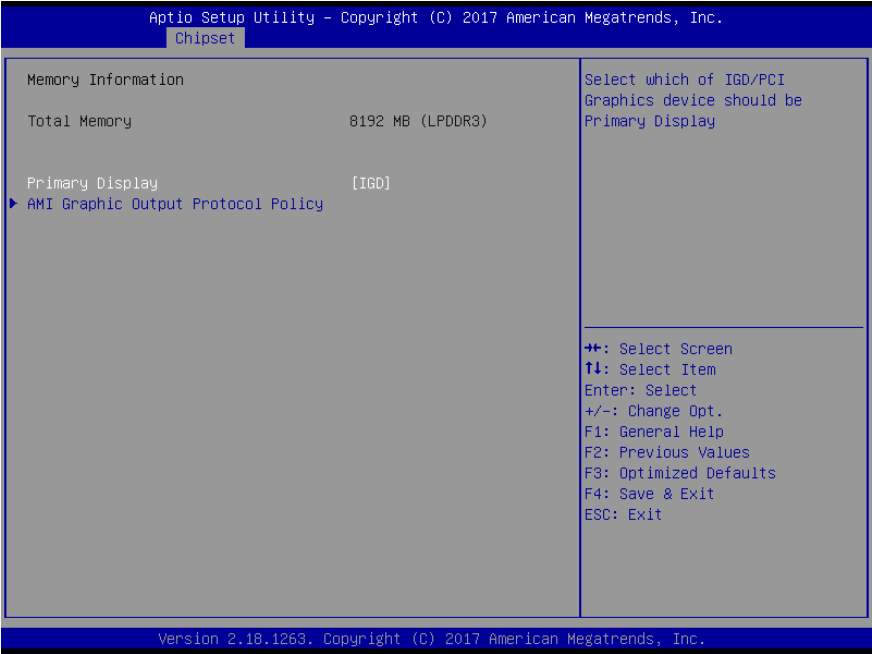


Options Summary	
DIO_P#1~4	Input
	Output
Set DIO as Input or Output.	
DIO_P#5~8	Input
	Output
Set DIO as Input or Output.	
DIO_P#1~4 Direction	Low
	High
Set output level when DIO pin is output.	

3.5 Setup Submenu: Chipset



3.5.1 Chipset: North Bridge



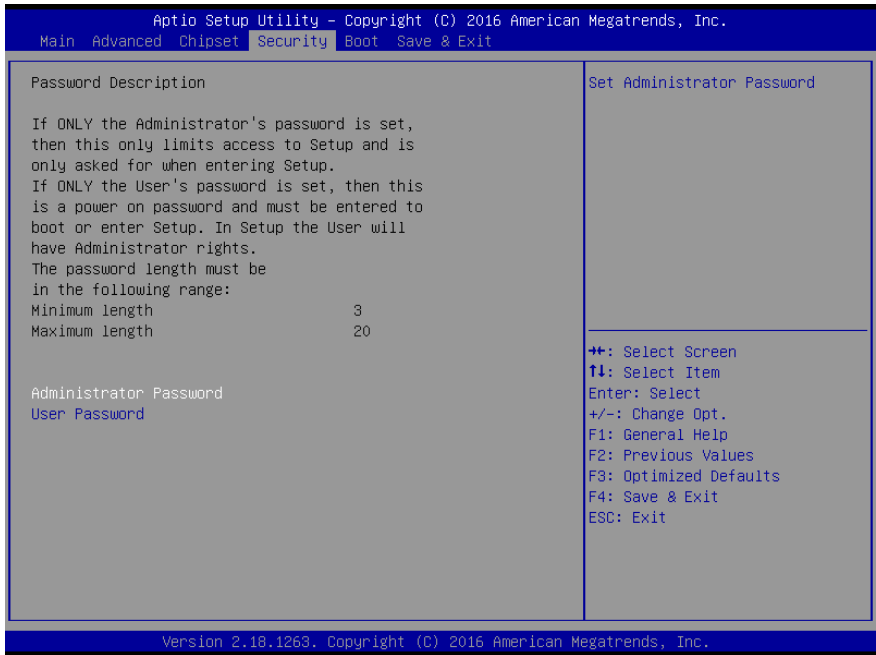
Options Summary	
Primary Display	IGD
	PCIe
Select which of IGD/PCI Graphics device should be Primary Display.	

3.5.1.1 North Bridge: AMI Graphic Output Protocol Policy



Options Summary	
Output Select	HDMI1
Output Interface.	

3.6 Setup Submenu: Security



Change User/Supervisor Password

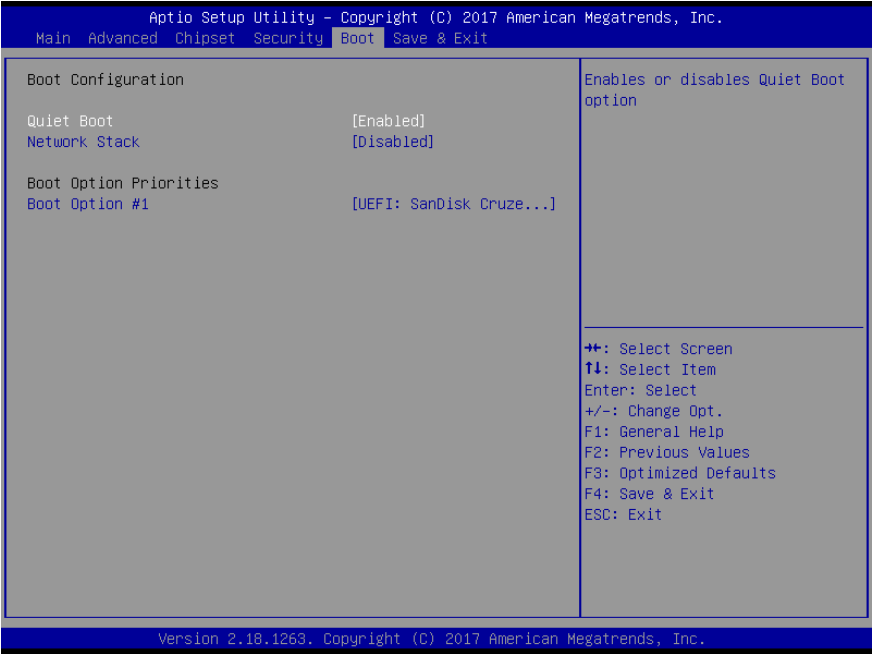
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup Submenu: Boot



Options Summary	
Quiet Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Network Stack	Disabled
	Enabled
Enable/Disable UEFI Network Stack.	

3.8 Setup Submenu: Exit



Chapter 4

Driver Installation

4.1 Driver Installation

Please download the driver from AAEON website. It contains all the drivers and utilities you need to setup your product. Follow the steps below to install the drivers.

<http://www.aaeon.com/en/p/desktop-network-appliance-fws-2273>

Step 1 – Open the **Step 1 - LAN** folder and select the OS folder your system is.

Step 2 – Double click on **igb-5.3.5.4.tar** file and follow the **README** instructions

Step 3 – Drivers can then be installed.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: Super I/O Relative Register Table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2: Watchdog Relative Register Table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN  //This parameter is represented from Note9
#define byte   EnableReg  //This parameter is represented from Note10
#define byte   EnableBit  //This parameter is represented from Note11
#define byte   EnableVal  //This parameter is represented from Note12
#define byte   StatusLDN  // This parameter is represented from Note13
#define byte   StatusReg  // This parameter is represented from Note14
#define byte   StatusBit  // This parameter is represented from Note15
*****

```

```
*****
VOID  Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID  SIOEnterMBPnPMode0{
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****

```

```

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

```

```

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}

```

Appendix B

I/O Information

B.1 I/O Address Map

Input/output (I/O)	
[0000000000000000 - 000000000000006F]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000060 - 0000000000000060]	Standard PS/2 Keyboard
[0000000000000061 - 0000000000000061]	Motherboard resources
[0000000000000063 - 0000000000000063]	Motherboard resources
[0000000000000064 - 0000000000000064]	Standard PS/2 Keyboard
[0000000000000065 - 0000000000000065]	Motherboard resources
[0000000000000067 - 0000000000000067]	Motherboard resources
[0000000000000070 - 0000000000000070]	Motherboard resources
[0000000000000070 - 0000000000000077]	System CMOS/real time clock
[0000000000000078 - 00000000000000CF7]	PCI Express Root Complex
[0000000000000080 - 000000000000008F]	Motherboard resources
[0000000000000092 - 0000000000000092]	Motherboard resources
[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[00000000000000B2 - 00000000000000B3]	Motherboard resources
[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
[000000000000003F8 - 000000000000003FF]	Communications Port (COM1)
[00000000000000400 - 0000000000000047F]	Motherboard resources
[000000000000004D0 - 000000000000004D1]	Programmable interrupt controller
[00000000000000500 - 000000000000005FE]	Motherboard resources
[00000000000000680 - 0000000000000069F]	Motherboard resources
[00000000000000A00 - 00000000000000A2F]	Motherboard resources
[00000000000000A30 - 00000000000000A3F]	Motherboard resources
[00000000000000A40 - 00000000000000A4F]	Motherboard resources
[00000000000000D00 - 00000000000000FFF]	PCI Express Root Complex
[000000000000009000 - 000000000000009FFF]	PCI-to-PCI Bridge
[000000000000009000 - 00000000000000BFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
[000000000000009000 - 00000000000000BFFF]	PCI-to-PCI Bridge
[00000000000000A000 - 00000000000000AFF]	PCI-to-PCI Bridge
[00000000000000B000 - 00000000000000BFFF]	PCI-to-PCI Bridge
[00000000000000C000 - 00000000000000CFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
[00000000000000D000 - 00000000000000DFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[00000000000000E000 - 00000000000000EFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[00000000000000F000 - 00000000000000F03F]	Intel(R) HD Graphics

 [000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
 [000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
 [000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
 [000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
 [000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
--

B.2 Memory Address Map

Memory	
[000000007B800001 - 000000007BFFFFFF]	PCI Express Root Complex
[000000007C000001 - 000000007CFFFFFF]	PCI Express Root Complex
[0000000080000000 - 0000000080FFFFFF]	Intel(R) HD Graphics
[0000000080000000 - 0000000080FFFFFF]	Intel(R) HD Graphics
[0000000080000000 - 00000000CFFFFFFF]	PCI Express Root Complex
[0000000081000000 - 00000000810FFFFF]	High Definition Audio Controller
[0000000081100000 - 00000000811FFFFF]	PCI-to-PCI Bridge
[0000000081100000 - 00000000813FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
[0000000081100000 - 00000000813FFFFF]	PCI-to-PCI Bridge
[00000000811DC000 - 00000000811DFFFF]	Intel(R) I211 Gigabit Network Connection #6
[00000000811E0000 - 00000000811FFFFF]	Intel(R) I211 Gigabit Network Connection #6
[0000000081200000 - 00000000812FFFFF]	PCI-to-PCI Bridge
[00000000812DC000 - 00000000812DFFFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000812E0000 - 00000000812FFFFF]	Intel(R) I211 Gigabit Network Connection #2
[0000000081300000 - 00000000813FFFFF]	PCI-to-PCI Bridge
[00000000813DC000 - 00000000813DFFFF]	Intel(R) I211 Gigabit Network Connection #5
[00000000813E0000 - 00000000813FFFFF]	Intel(R) I211 Gigabit Network Connection #5
[0000000081400000 - 00000000814FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
[00000000814DC000 - 00000000814DFFFF]	Intel(R) I211 Gigabit Network Connection
[00000000814E0000 - 00000000814FFFFF]	Intel(R) I211 Gigabit Network Connection
[0000000081500000 - 00000000815DFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[00000000815DC000 - 00000000815DFFFF]	Intel(R) I211 Gigabit Network Connection #4
[00000000815E0000 - 00000000815FFFFF]	Intel(R) I211 Gigabit Network Connection #4
[0000000081600000 - 00000000816FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[00000000816DC000 - 00000000816DFFFF]	Intel(R) I211 Gigabit Network Connection #3
[00000000816E0000 - 00000000816FFFFF]	Intel(R) I211 Gigabit Network Connection #3
[0000000081700000 - 000000008170FFFF]	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
[0000000081710000 - 0000000081713FFF]	High Definition Audio Controller
[0000000081714000 - 0000000081715FFF]	Standard SATA AHCI Controller
[0000000081716000 - 00000000817160FF]	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5ADA
[0000000081717000 - 00000000817177FF]	Standard SATA AHCI Controller
[0000000081718000 - 00000000817180FF]	Standard SATA AHCI Controller
[0000000081718000 - 000000008171BFFF]	Intel(R) Trusted Execution Engine Interface
[0000000090000000 - 000000009FFFFFFF]	Intel(R) HD Graphics
[0000000090000000 - 000000009FFFFFFF]	Intel(R) HD Graphics
[00000000D0C00000 - 00000000D0C00653]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C40000 - 00000000D0C40763]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C50000 - 00000000D0C5076B]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C70000 - 00000000D0C70673]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF]	PCI Express Root Complex
[00000000FEA00000 - 00000000FEAFFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED01000 - 00000000FED01FFF]	Motherboard resources
[00000000FED03000 - 00000000FED03FFF]	Motherboard resources
[00000000FED06000 - 00000000FED06FFF]	Motherboard resources
[00000000FED08000 - 00000000FED09FFF]	Motherboard resources
[00000000FED1C000 - 00000000FED1CFFF]	Motherboard resources



[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0



[00000000FED80000 - 00000000FEDBFFFF] Motherboard resources



[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources

B.3 IRQ Mapping Chart

Interrupt request (IRQ)		
	(ISA) 0x00000000 (00)	System timer
	(ISA) 0x00000001 (01)	Standard PS/2 Keyboard
	(ISA) 0x00000004 (04)	Communications Port (COM1)
	(ISA) 0x00000008 (08)	High precision event timer
	(ISA) 0x0000000C (12)	PS/2 Port Compatible Pointing Device
	(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
	(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
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	(ISA) 0x000001DF (479)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E0 (480)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E1 (481)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E2 (482)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E3 (483)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E4 (484)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E5 (485)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E6 (486)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E7 (487)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E8 (488)	Microsoft ACPI-Compliant System
	(ISA) 0x000001E9 (489)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EA (490)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EB (491)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EC (492)	Microsoft ACPI-Compliant System
	(ISA) 0x000001ED (493)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EE (494)	Microsoft ACPI-Compliant System
	(ISA) 0x000001EF (495)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F0 (496)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F1 (497)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F2 (498)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F3 (499)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F4 (500)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F5 (501)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F6 (502)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F7 (503)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F8 (504)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F9 (505)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FA (506)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FB (507)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FC (508)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FD (509)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FE (510)	Microsoft ACPI-Compliant System

	(ISA) 0x000001FF (-511)	Microsoft ACPI-Compliant System
	(PCI) 0x00000019 (25)	High Definition Audio Controller
	(PCI) 0xFFFFFDD7 (-41)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDD8 (-40)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDD9 (-39)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDDA (-38)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDDB (-37)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDDC (-36)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDDD (-35)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE (-34)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDEF (-33)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE0 (-32)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE1 (-31)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE2 (-30)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE3 (-29)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE4 (-28)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE5 (-27)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE6 (-26)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE7 (-25)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE8 (-24)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFDE9 (-23)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDEA (-22)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDEB (-21)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDEC (-20)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDED (-19)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDEE (-18)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFDEF (-17)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE0 (-16)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE1 (-15)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE2 (-14)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE3 (-13)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE4 (-12)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFDE5 (-11)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDE6 (-10)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDE7 (-9)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDE8 (-8)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDE9 (-7)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDEA (-6)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFDEB (-5)	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
	(PCI) 0xFFFFFDEC (-4)	Intel(R) Trusted Execution Engine Interface
	(PCI) 0xFFFFFDED (-3)	Intel(R) HD Graphics
	(PCI) 0xFFFFFDEE (-2)	Standard SATA AHCI Controller

Appendix C

Standard LAN Bypass Platform Setting

C.1 Introduction to LED

FWS-2273 provides a LED indicator which can change the LED status by AAEON SDK. User is able to program the LED status to express different status.

C.1.1 Status LED Configuration

The LED status indicator of FWS-2273 is programmable with AAEON SDK for your application.

Table 1: LED Status

	STA_LED2	STA_LED1	STA_LED0
LED Off	0	0	0
Red	0	0	1
Red Blinking (Slowly)	0	1	0
Red Blinking (Quickly)	0	1	1
Reserved	1	0	0
Green Blinking (Slowly)	1	0	1
Green Blinking (Quickly)	1	1	0
Green	1	1	1

Table 2: Status LED and Register Mapping Table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset (SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

C.1.2 Sample Code

```

*****
****
#define ByteCPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define ByteOFFSET //This parameter is represented from Note2
*****
****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
//LED Off
//BIT2=0, BIT1=0, BIT0=0
bData = bData & 0xF8;
break;
}
case 1:
{
//Red LED On
//BIT2=0, BIT1=0, BIT0=1
bData = (bData & 0xF8) | 0x01;
break;
}
case 2:
{
//Red LED Blink
//BIT2=0, BIT1=1, BIT0=0
bData = (bData & 0xF8) | 0x02;
break;
}
case 3:
{
//Red LED Fast Blink
//BIT2=0, BIT1=1, BIT0=1
bData = (bData & 0xF8) | 0x03;
break;
}
case 4:

```

```
{
    //Green LED On
    //BIT2=1, BIT1=1, BIT0=1
    bData = (bData & 0xF8) | 0x07;
    break;
}
case 5:
{
    //Green LED Blink
    //BIT2=1, BIT1=0, BIT0=1
    bData = (bData & 0xF8) | 0x05;
    break;
}
case 6:
{
    //Green LED Fast Blink
    //BIT2=1, BIT1=1, BIT0=0
    bData = (bData & 0xF8) | 0x06;
    break;
}
default:
    break;
}
SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
*****
*****
```

C.2 Introduction to LAN Bypass

FWS-2273 provides LAN Bypass kit and allow uninterrupted network traffic even if a single in-line appliance is shut down or hangs.

C.2.1 LAN Bypass

Table 1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table 2: LAN Bypass Register Table

Function	Description
LAN_ID3	
LAN_ID2	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table 3: LAN Bypass Register Mapping Table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

C.2.2 Sample Code

```

*****
****
#define ByteCPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define ByteOFFSET //This parameter is represented from Note2
*****
****
// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
    bData = bData | 0x08;
else
    bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
    bData = bData | 0x04;
else
    bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
    bData = bData | 0x02;
else
    bData = bData & 0xFD;
// Set Reg01h bit0
if(bLanSel & 0x01)
    bData = bData | 0x01;
else
    bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH) // Pass Through
    bData = bData & 0xBF;
else // Bypass
    bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH) // Pass Through

```

```
        bData = bData & 0xDF;
else // Bypass
    bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
    bData = bData & 0xEF;
else // Bypass
    bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);

*****
```

C.3 Introduction to Software Reset Button Configuration

FWS-2273 provides a general propose input button which status get by AAEON SDK.

C.3.1 Soft Reset Button Configuration

Table 2: LAN Bypass Relative Register Table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Table 1: Soft Reset Button Register Mapping Table

Attribute	Register(I/O)	BitNum	Value	Attribute
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3) BTN_STS

C.3.2 Sample Code

```
*****
#define Word      BTN_STS      //This parameter is represented from Note1
#define ByteBTN_STS_R      //This parameter is represented from Note2
*****
Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
    BYTE  TmpValue;

    TmpValue = inportb (IoAddr);
    return  (TmpValue & (1 << BitNum))
}
*****
VOID  Main(){
    Byte RstBtn;

    RstBtn = GET_Value (BTN_STS, BTN_STS_R); // Active Low
}
*****
```