

FWS-2271

Network Appliance

User's Manual 1st Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● FWS-2271	1
● SATA cable	1
● SATA power cable	1
● Power adapter	1
● HDD bracket kit	1
● Rubber foot	4

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○
<p>O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注:</p> <p>一、此产品所标示之环保使用期限，系指在一般正常使用状况下。</p> <p>二、上述部件物质中央处理器、内存、硬盘、光驱、触控模块为选购品。</p>						

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products
AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1 - Product Specifications	1
1.1 Specifications	2
Chapter 2 – Hardware Information	5
2.1 Dimensions	6
2.2 Jumpers and Connectors.....	8
2.3 List of Jumpers	10
2.3.1 CF Power Selection (JP1).....	11
2.3.2 Auto PWRBTN Selection (JP2)	11
2.3.3 CMOS Setting Selection (CN12)	11
2.4 List of Connectors.....	12
2.4.1 Digital I/O (CN1).....	13
2.6 Hard Disk Drive Installation.....	14
Chapter 3 - AMI BIOS Setup	24
3.1 System Test and Initialization	25
3.2 AMI BIOS Setup	26
3.3 Setup Submenu: Main.....	27
3.4 Setup Submenu: Advanced.....	28
3.4.1 Advanced: Trusted Computing	29
3.4.2 Advanced: CPU Configuration	31
3.4.3 Advanced: SATA Drives	33
3.4.4 Advanced: USB Configuration	34
3.4.5 Advanced: Hardware Monitor	35
3.4.6 Advanced: SIO Configuration.....	37
3.4.6.1 SIO Configuration: Serial Port Configuration.....	38
3.4.6.1.2 Console Redirection Settings	40
3.4.7 Advanced: LAN Bypass Configuration.....	46

3.4.8	Advanced: Power Management.....	48
3.4.9	Advanced: Digital I/O Port Configuration.....	50
3.5	Setup submenu: Chipset.....	51
3.5.1	Chipset: North Bridge.....	52
3.5.1.1	North Bridge: AMI Graphic Output Protocol Policy	53
3.6	Setup submenu: Security	54
3.7	Setup submenu: Boot.....	56
3.8	Setup submenu: Exit	57
Chapter 4 – Drivers Installation.....		58
4.1	Driver Installation.....	59
Appendix A - Watchdog Timer Programming.....		60
A.1	Watchdog Timer Initial Program	61
Appendix B - I/O Information		67
B.1	I/O Address Map	68
B.2	Memory Address Map	70
B.3	IRQ Mapping Chart.....	72
Appendix C - Standard LAN Bypass Platform Setting		81
C.1	Status LED	82
C.2	LAN Bypass.....	85
C.3	Software Reset Button Configuration.....	88

Chapter 1

Product Specifications

1.1 Specifications

System

- **Processor** Intel® Pentium® N4200/N3350 processor
SoC
- **System Memory** 204-pin DDR3L 1867MHz SODIMM slot x 1, up to 8GB
- **Chipset** -
- **Ethernet** Intel® i211 (Co-lay with Intel® i210)
Gigabit Ethernet x 6 (BOM Optional 4 Ports)
- **Bypass** Supports up to 2 pairs bypass function
- **Storage** 2.5" HDD bay x 1
CFast™ socket x 1 (Co-lay for BOM Optional CompactFlash™ socket x 1)
- **Expansion Interface** Mini-Card socket (full-size) with SIM socket x 2
USB 3.0 Type A on I/O side x 2
- **OS Support** **Windows 10 (64 bit)**
VGA
Chipset
LAN
Yocto* Tool based Embedded Linux 4.1 or above
VGA
Chipset
LAN

- **Front Panel I/O**
 - Power LED x 1
 - Status LED x 1
 - HDD Active LED x 1
 - Bypass LED x 2
 - LAN LED x 12
- **Rear Panel I/O**
 - USB 3.0 Port x 2
 - RJ-45 Port x 6 (BOM Optional RJ-45 Port x 4)
 - RJ-45 Console x 1
 - 12V DC Power Input x 1
 - Software Programmable button x1
 - HDMI x 1
 - Power Button x 1
- **RTC**
 - Internal RTC
- **Watchdog Timer**
 - 1~255 steps by software programming
- **Software Button**
 - GPIO Programmable push button x 1
- **TPM**
 - Optional TPM v1.2 9660/TPM2.0 9665
- **GPIO**
 - Reserve internal pin header 8-bit Digital I/O interface (4-in /4-out)
- **Fan**
 - System Fan x 1
- **Color**
 - White
- **Power Supply**
 - DC 40W power input
- **Power Requirement**
 - DC 12V power jack
- **Dimension (W x D x H)**
 - 200 x 105 x 44mm (7.87 x 4.13 x 1.73")
- **Certification**
 - CE/FCC Class A

Display

- **Graphic Engine** Intel® HD Graphics
- **Output Interface** HDMI

I/O

- **Serial Port** RJ-45 console x 1
- **Keyboard and Mouse** Reserved box header
- **USB** USB 3.0 Type A on I/O side x 2

Environmental

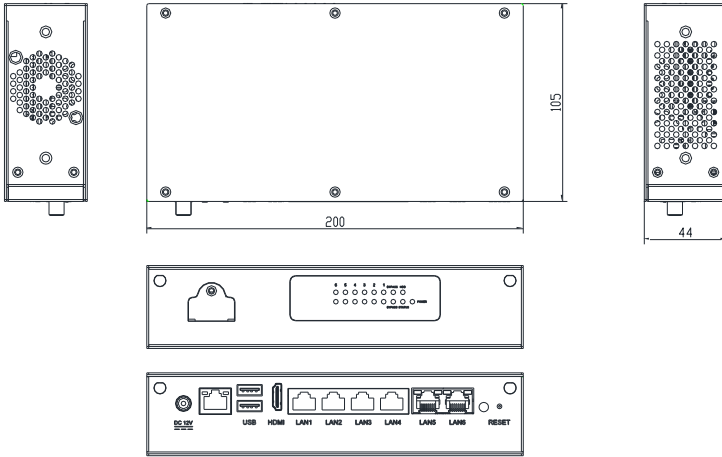
- **Operating Temperature** 0 ~ 40°C (32 ~ 104°F)
- **Storage Temperature** -20 ~ 60°C (4 ~ 104°F)
- **Operating Humidity** 10 ~ 80% relative humidity, non-condensing
- **Storage Humidity** 10 ~ 80% @ 40°C, non-condensing
- **Anti-Vibration** 0.5 Grms/5~500Hz/ operation (2.5" HDD)
1.5 Grms /5~500Hz/ non-operation
- **Anti-Shock** 10 G peak acceleration (11m sec. duration),
operation
20 G peak acceleration (11m sec. duration),
non operation

Chapter 2

Hardware Information

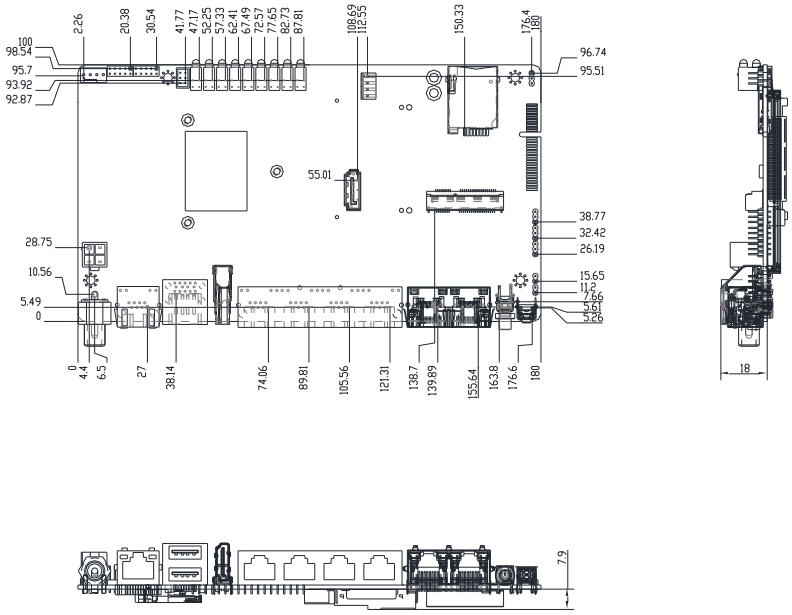
2.1 Dimensions

System

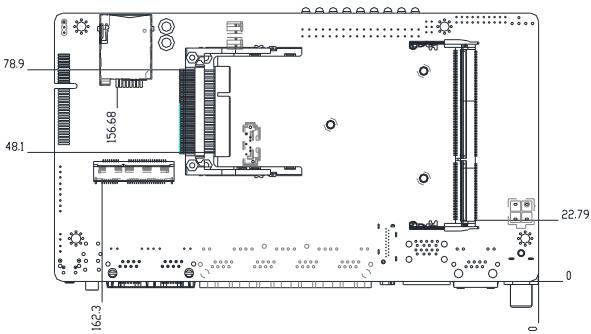


Board

Component Side

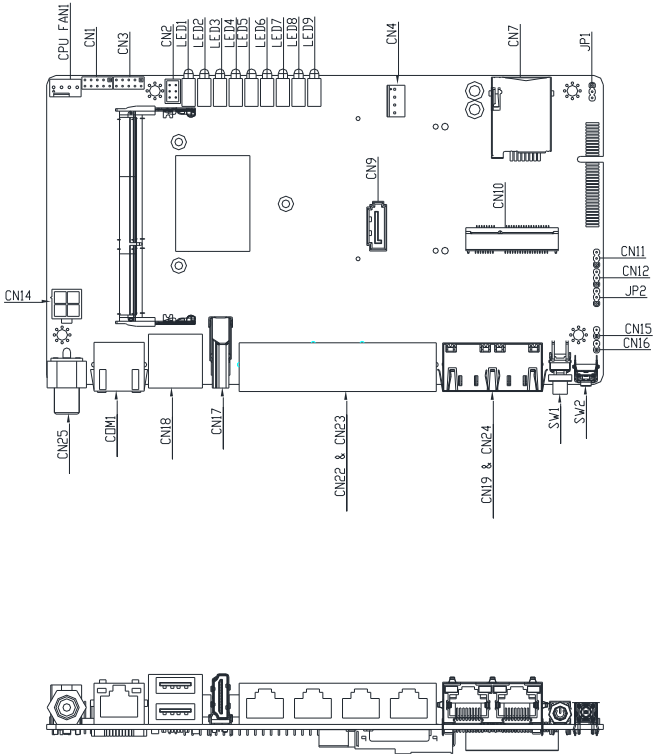


Solder Side

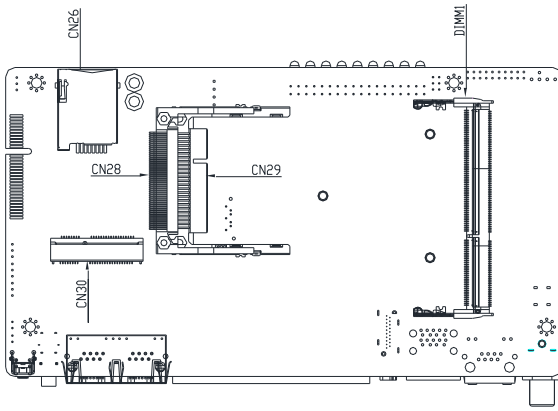


2.2 Jumpers and Connectors

Component Side



Solder Side



2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
JP1	CF POWER Selection
JP2	Auto PWRBTN Selection
CN12	CMOS Setting Selection

2.3.1 CF Power Selection (JP1)



5V



3.3V (Default)

2.3.2 Auto PWRBTN Selection (JP2)



Don't use Auto PWRBTN (Default)



Use Auto PWRBTN

2.3.3 CMOS Setting Selection (CN12)



Normal (Default)



Clear CMOS

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
DIMM1	DDR3L SODIMM SOCKET
CPU_FAN1	4P SMART FAN
CN2	KB/MS
CON1	COM PORT
CN9	SATA6G INTERFACE
CN4	SATA POWER
CN10/CN30	Mini Pci-E socket
CN28	CF CARD SOCKET
CN7/CN26	SIM CARD SOCKET
CN15	RESET
CN16	POWER BUTTON
CN18	USB3.0 DUAL Port
CN1	Digital I/O
CN19	LAN1-4
CN20	LAN5-6

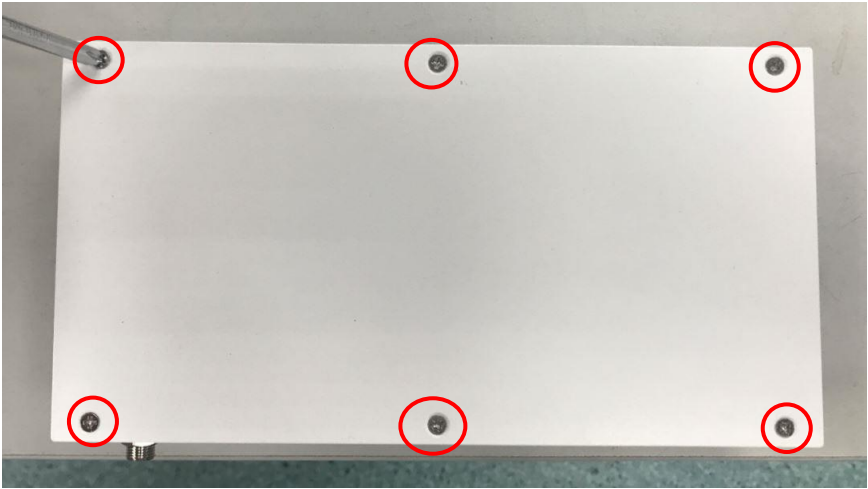
2.4.1 Digital I/O (CN1)

This connector offers 4-pair of digital I/O functions and address is 801H. The pin definitions are illustrated below:

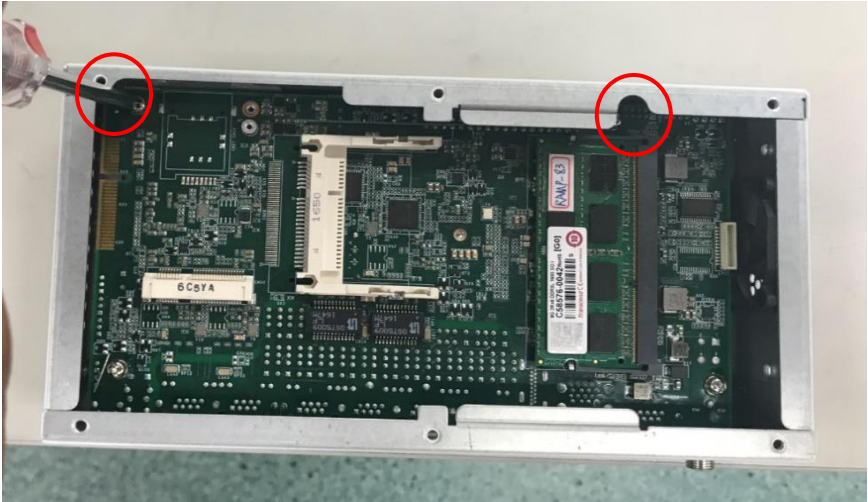
Pin	Signal	Pin	Signal
1	Digital- IN/OUT(Port1 Bit 1)	2	Digital- IN/OUT (Port1 Bit 2)
3	Digital- IN/OUT (Port1 Bit 4)	4	Digital- IN/OUT (Port1 Bit 5)
5	Digital- IN/OUT (Port3 Bit 4)	6	Digital- IN/OUT (Port3 Bit 5)
7	Digital- IN/OUT (Port6 Bit 3)	8	Digital- IN/OUT (Port4 Bit 7)
9	+5V	10	GND

2.6 Hard Disk Drive Installation

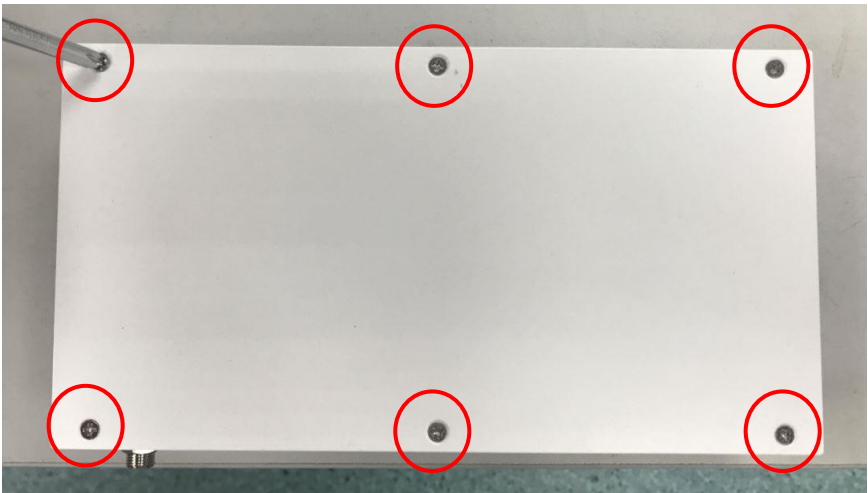
1. Remove the screws, then the back cover.



2. Remove the screws on the PCB-Bracket.



3. Remove the screws, and take off the upper casing.



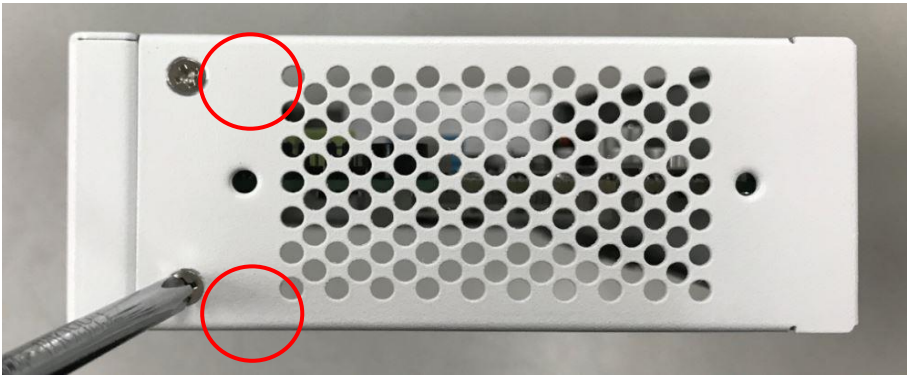
4. Remove the screws for the PCB Bracket, and then remove the PCB Bracket itself.



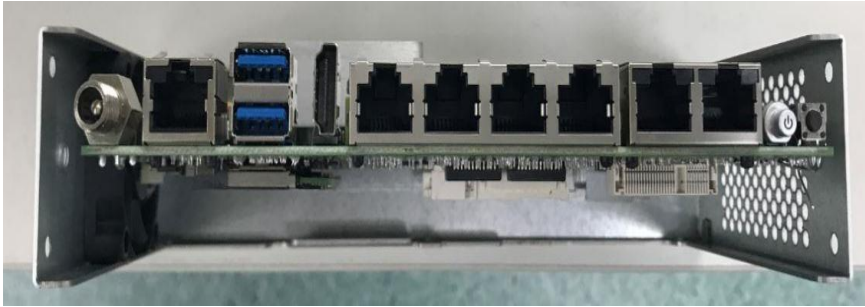
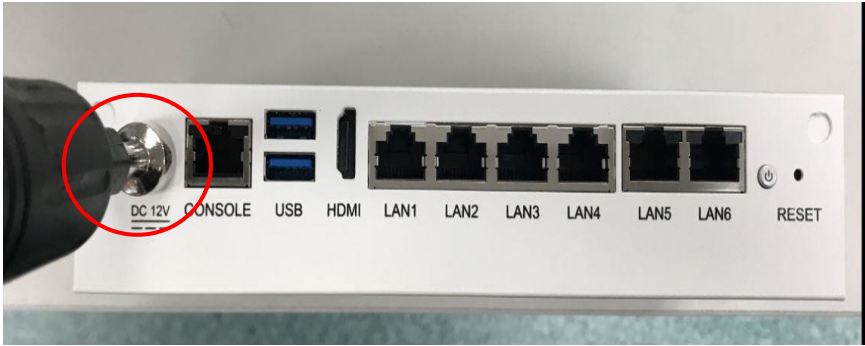
5. Remove both screws on the left hand side.



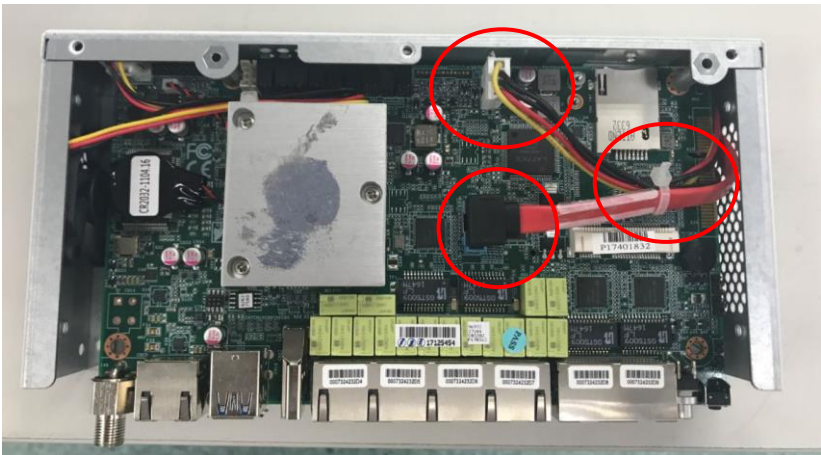
6. Remove both screws on the right hand side.



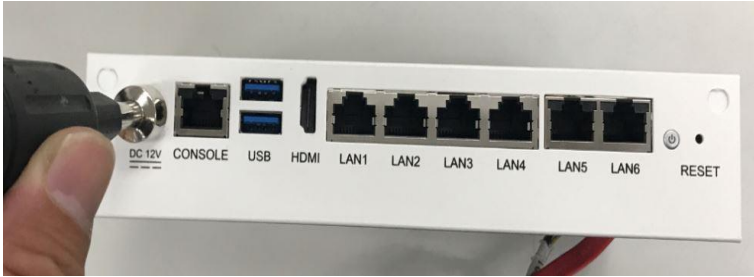
7. Remove the screws for the DC Power, then take out the back cover.



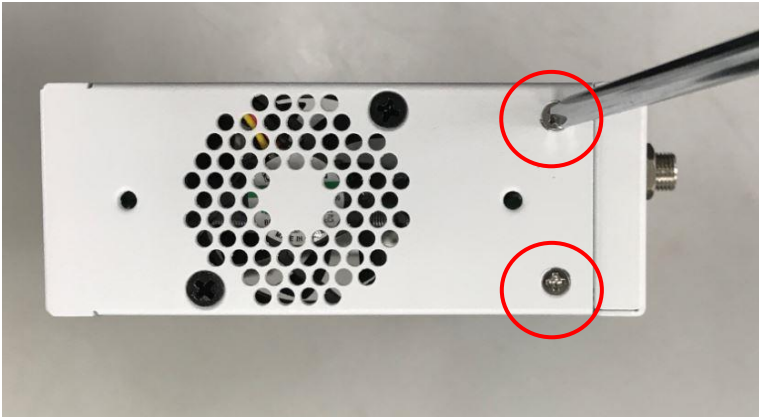
8. Slot the SATA Cable and the POWER cable together, and secure them with a fastener.



- After assembling the parts, close the cover and secure the DC Power screws and bolts.



- Secure both screws on the left hand side.



- Secure both screws on the right hand side.



- Secure the screws on the PCB Bracket.



- Assemble the anti-vibration pad and put it onto the HDD Bracket.



- Secure the screws onto the anti-vibration pad.



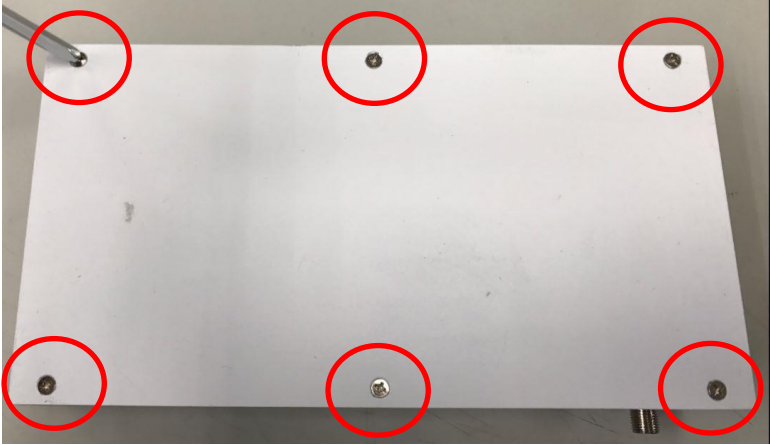
- Secure the HDD Bracket onto the HDD.



- Secure the SATA Cable and the Power Cable onto the HDD, and assemble the HDD within the apparatus.



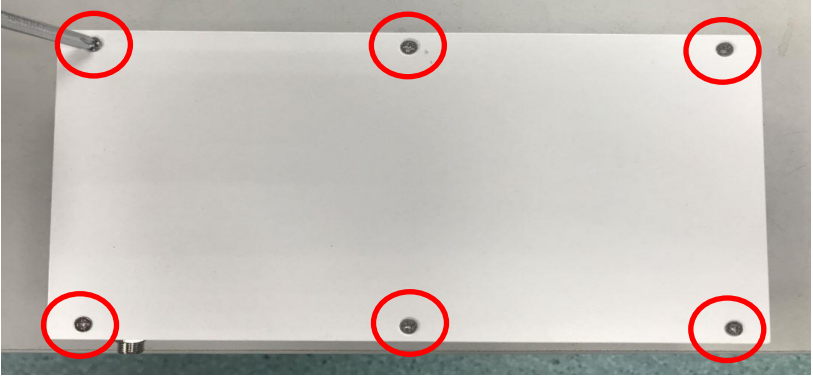
17. Assemble the lower cover and secure the screws.



18. Secure the PCB Bracket screws.



19. Secure the screws.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

Note: The Intel Apollo Lake platform only supports UEFI boot mode.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

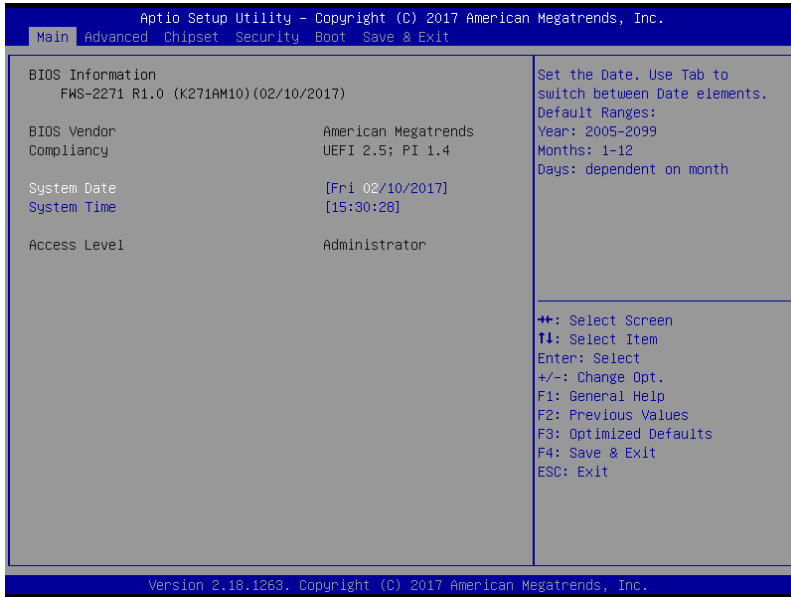
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

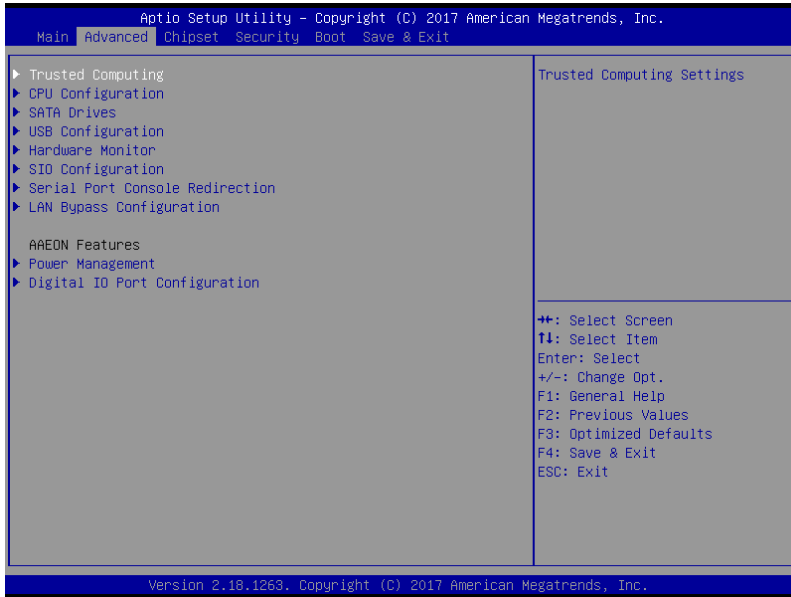
Boot – Enable/ Disable quiet Boot Option

Save & Exit – Save your changes and exit the program

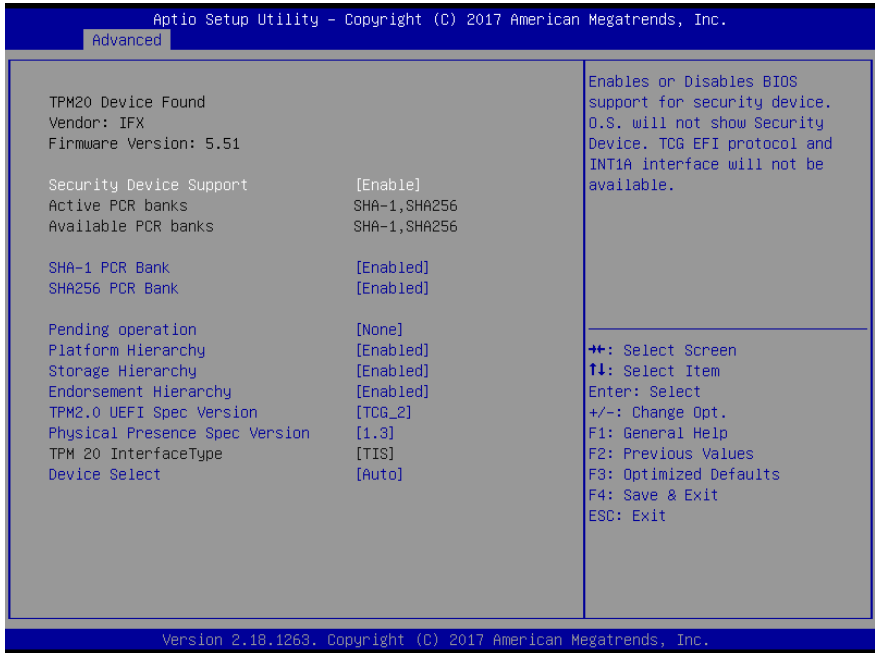
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



3.4.1 Advanced: Trusted Computing



Options summary:

Security Device Support	Disabled
	Enabled
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.	
SHA-1 PCR Bank	Disabled
	Enabled
Enable or Disable SHA-1 PCR Bank	
SHA256 PCR Bank	Disabled
	Enabled
Enable or Disable SHA256 PCR Bank	

Pending operation	None
	TPM Clear
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.	
Platform Hierarchy	Disabled
	Enabled
Enable or Disable Platform Hierarchy	
Storage Hierarchy	Disabled
	Enabled
Enable or Disable Storage Hierarchy	
Endorsement Hierarchy	Disabled
	Enabled
Enable or Disable Endorsement Hierarchy	
TPM2.0 UEFI Spec Version	TCG_1_2
	TCG_2
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later	
Physical Presence Spec Version	1.2
	1.3
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.	
Device Select	TPM 1.2
	TPM 2.0
	Auto

TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

3.4.2 Advanced: CPU Configuration

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

Advanced

CPU Configuration		When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
Intel(R) Pentium(R) CPU N4200 @ 1.10GHz		
CPU Signature	506C9	
Microcode Patch	24	
Max CPU Speed	1100 MHz	
Min CPU Speed	800 MHz	
Processor Cores	4	
Intel HT Technology	Not Supported	
Intel VT-x Technology	Supported	
L1 Data Cache	24 kB x 4	
L1 Code Cache	32 kB x 4	
L2 Cache	1024 kB x 2	
L3 Cache	Not Present	
Speed	1100 MHz	
64-bit	Supported	
Intel Virtualization Technology	[Enabled]	
VT-d	[Enabled]	
EIST	[Disabled]	
CPU Power Management Configuration		
Power Limit 1 Enable	[Disabled]	

++: Select Screen
 ↑: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 ESC: Exit

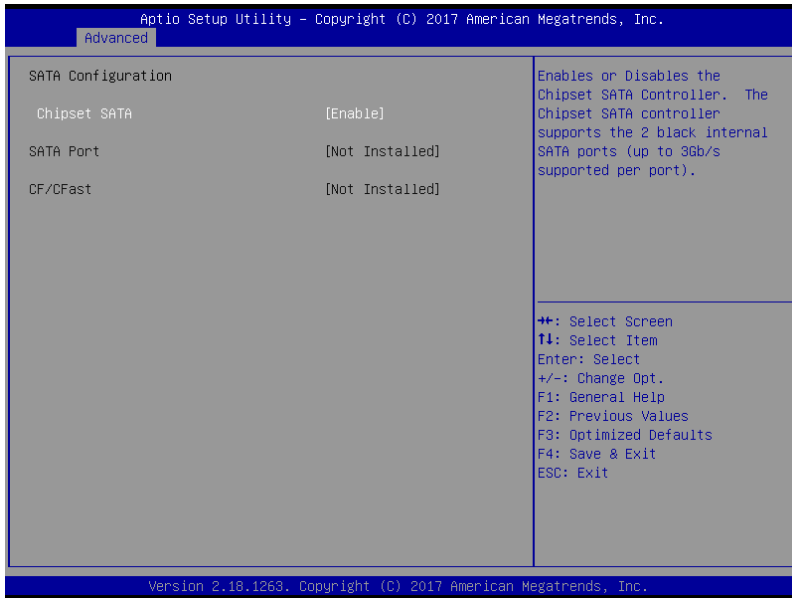
Version 2.18.1263. Copyright (C) 2017 American Megatrends, Inc.

Options summary:

Intel Virtualization Technology	Disabled
	Enabled
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology	
VT-d	Disabled
	Enabled
Enable/Disable CPU VT-d	
EIST	Disabled

	Enabled
Enable/Disable Intel SpeedStep	
Power Limit 1 Enable	Disabled
	Enabled
Enable/Disable Power Limit 1	

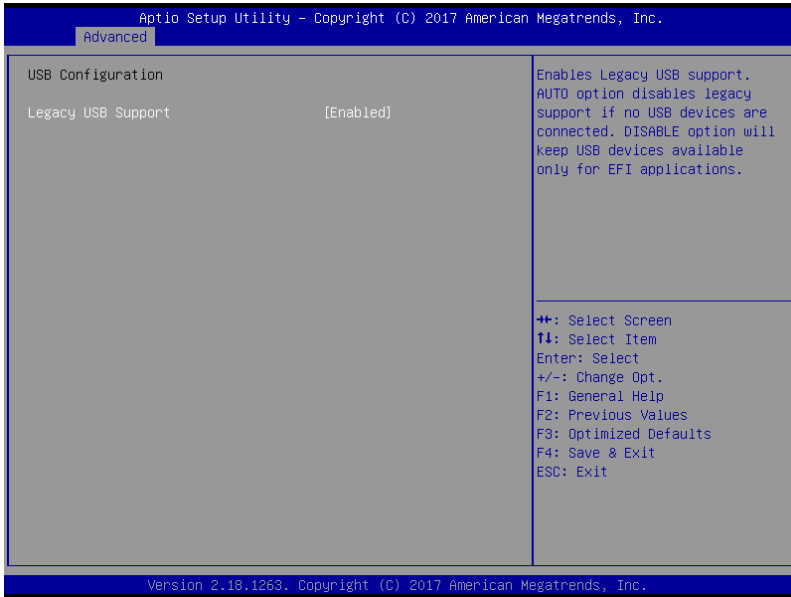
3.4.3 Advanced: SATA Drives



Options summary:

Chipset SATA	Disabled
	Enabled
Enables or Disables the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).	

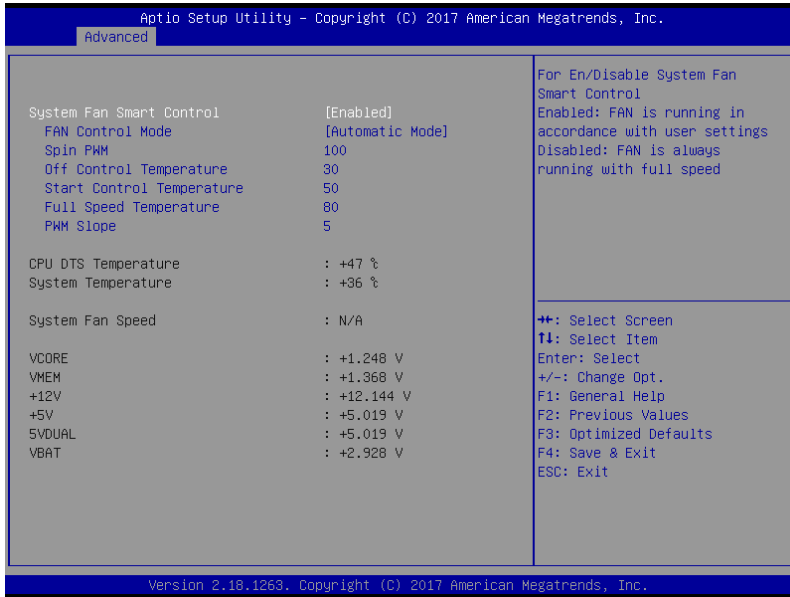
3.4.4 Advanced: USB Configuration



Options summary:

Legacy USB Support	Disabled
	Enabled
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.	

3.4.5 Advanced: Hardware Monitor

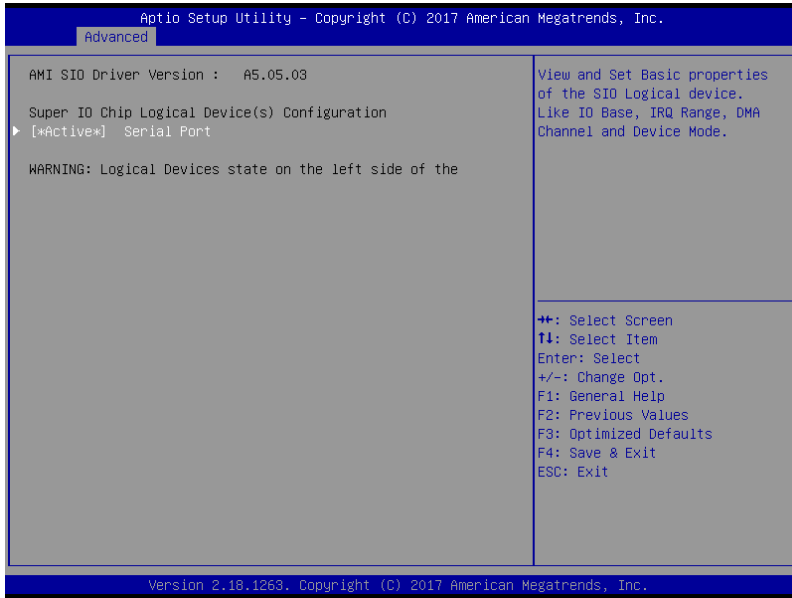


Options summary:

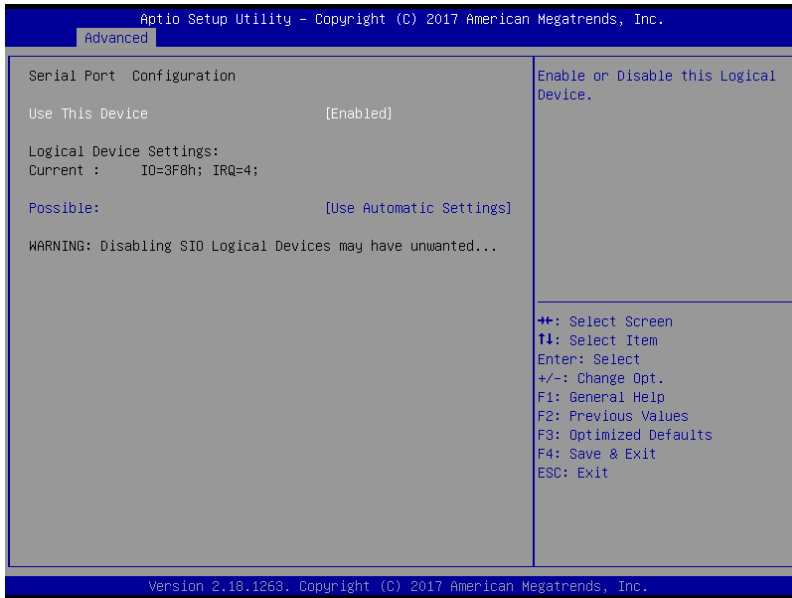
System Fan Smart Control	Disabled
	Enabled
For En/Disable Fan 1 Smart Control. Enabled: FAN is running in accordance with user settings. Disabled: FAN is always running with full speed	
Fan Control Mode	Automatic Mode
	Manual Mode
Manual Mode: Depends on PWM Duty. Automatic Mode: FAN Speed is depends on System Temperature	
Spin PWM	100 (0-255)

The PWM Duty of FAN Spin	
Range:[0 - 255]	
Off Control Temperature	30 (0-127)
Temperature Limit Value of Fan Off.	
Note: Some fans have the minimum speed even if the PWM value is 0	
Start Control Temperature	50 (0-127)
Temperature Limit Value of FAN Start Control	
Full Speed Temperature	80
Temperature Limit Value of FAN Full Speed	
PWM Slope	5 (1-15)
Slope PWM value/Degree C for FAN Speed Control	
Range:[1-15]	

3.4.6 Advanced: SIO Configuration



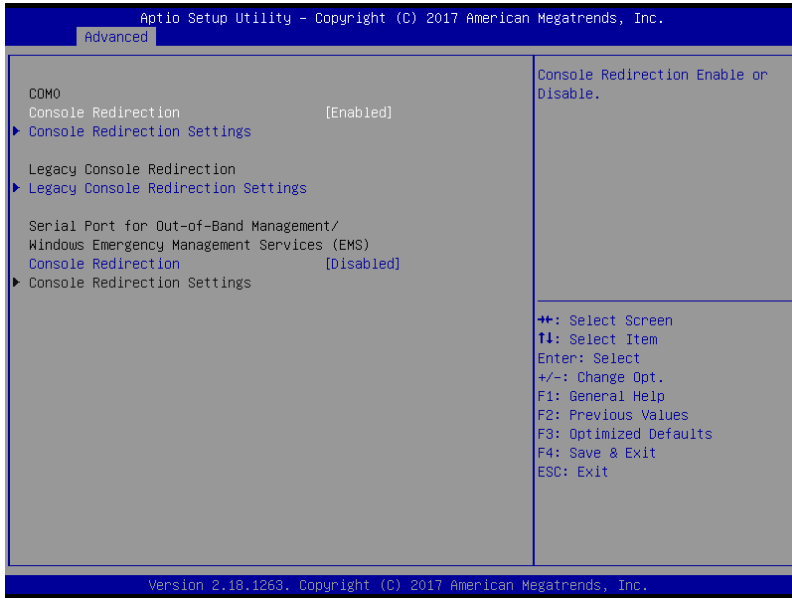
3.4.6.1 SIO Configuration: Serial Port Configuration



Options summary:

Use This Device	Disabled
	Enabled
Enable or Disable this Logical Device.	
Possible:	Use Automatic Settings
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=4;
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.	

3.4.6.1.1 Serial Port Configuration: Serial Port Console Redirection



Options summary:

Console Redirection	Disabled
	Enabled
Console Redirection Enabled or Disabled.	

3.4.6.1.2 Console Redirection Settings



Options summary:

Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	
Bits per second	9600
	19200
	38400
	57600

	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Data Bits	7
	8
Data Bits	
Parity	None
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	1
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	
Flow Control	None
	Hardware RTS/CTS
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
VT-UTF8 Combo Key Support	Disabled

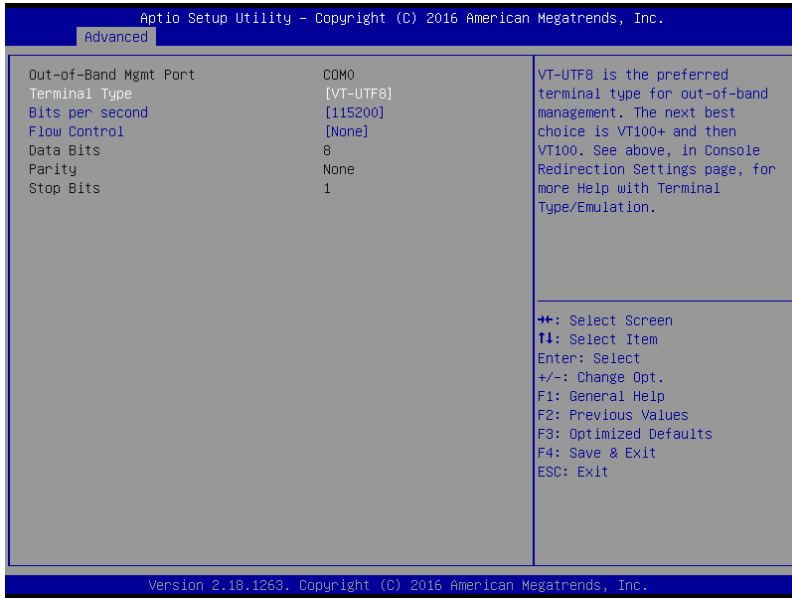
	Enabled
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	
Recorder Mode	Disabled
	Enabled
On this mode enabled only text will be send. This is to capture Terminal data.	
Resolution 100x31	Disabled
	Enabled
Enables or disables extended terminal resolution	
Legacy OS Redirection Resolution	80x24
	80x25
On Legacy OS, the Number of Rows and Columns supported redirection	
Putty KeyPad	VT100
	LINUX
	XTERMR6
	SCO
	ESCN
	VT400
Select FunctionKey and KeyPad on Putty.	
Redirection After BIOS POST	Always Enable
	BootLoader
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.	

3.4.6.1.3 Legacy Console Redirection Settings



Legacy Serial Redirection Port	COM0
Select a COM port to display redirection of Legacy OS and Legacy OPRM Messages	

3.4.6.1.4 Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)

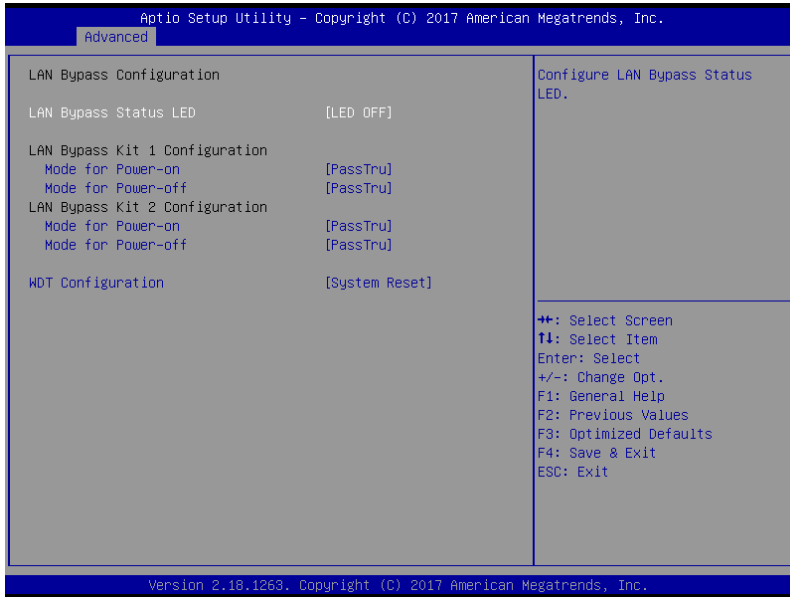


Options summary:

Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.	
Bits per second	9600
	19200
	57600

	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Flow Control	None
	Hardware RTS/CTS
	Software Xon/Xoff
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	
Data Bits	7
	8
Data Bits	
Parity	None
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	1
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	

3.4.7 Advanced: LAN Bypass Configuration

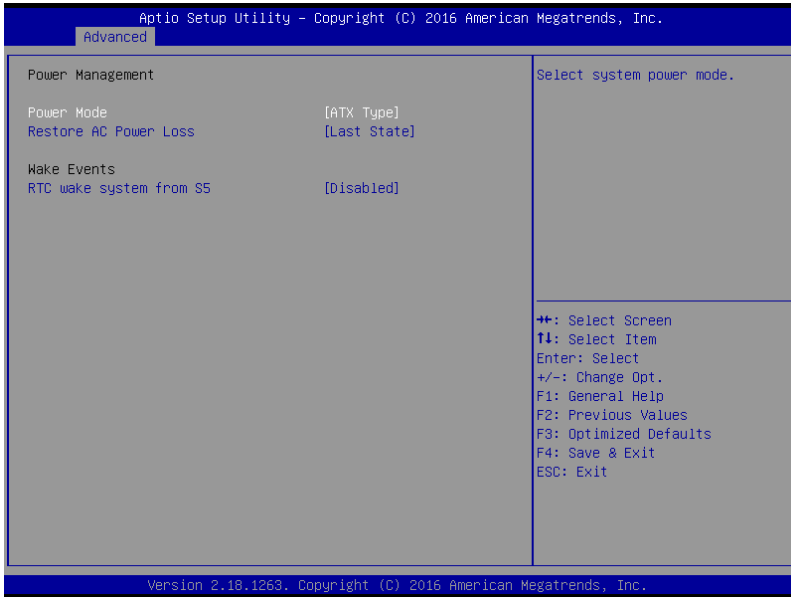


Options summary:

STATUS LED CTRL	LED OFF
	RED LED ON
	RED LED BLINK
	RED LED FAST BLINK
	GREEN LED ON
	GREEN LED BLINK
	GREEN LED FAST BLINK
Configure LAN Bypass Status LED.	
LAN kit Power ON	Bypass
	PassTru
Setting LAN kit function behavior when power on.(Bypass/Pass Through)	

LAN kit Power Off	Bypass
	PassTru
Setting LAN kit function behavior when power off.(Bypass/Pass Through)	
WDT configuration	Force Bypass
	SystemReset
Configure WDT behavior , System Reset Force Bypass	

3.4.8 Advanced: Power Management

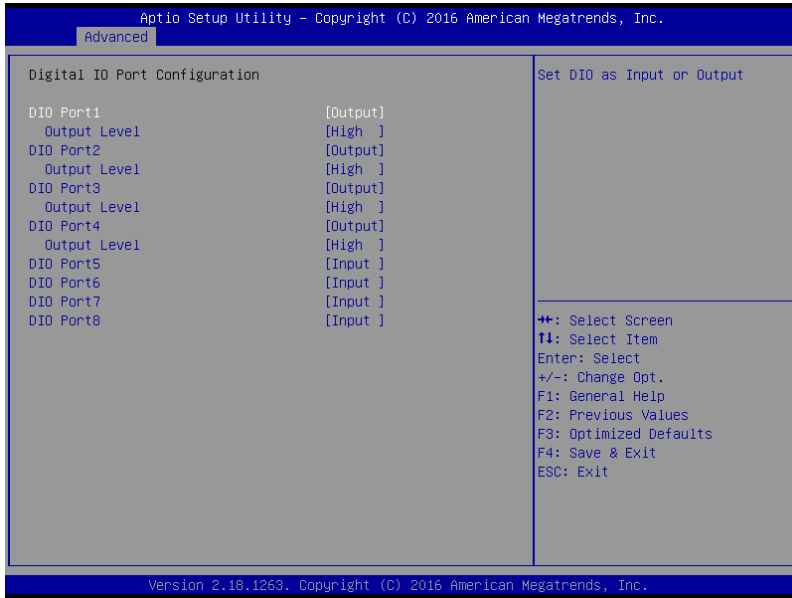


Options summary:

Power Mode	ATX Type
	AT Type
Select Power Supply Mode.	
Restore AC Power Loss	Power Off
	Power On
	Last State
Select AC power state when power is re-applied after a power failure.	
RTC Wake system from S5	Disabled
	Fixed time
	Dynamic time

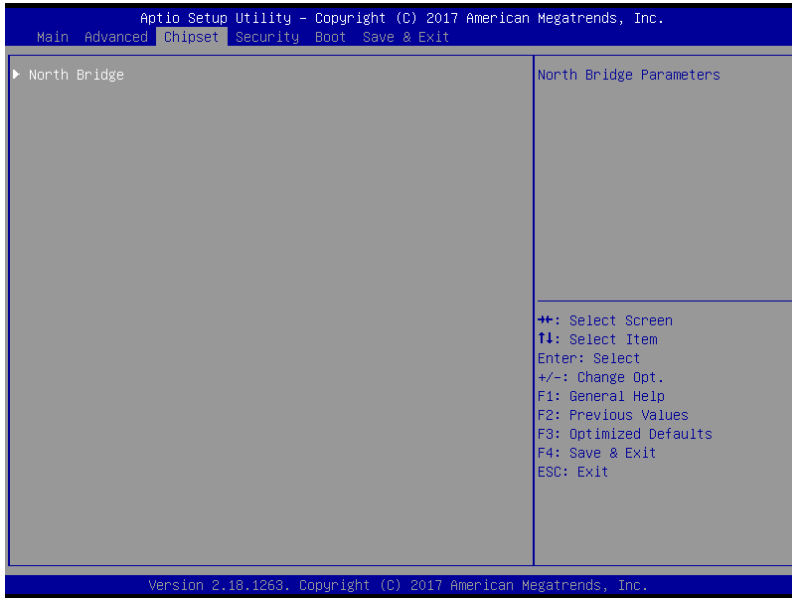
Fixed Time: System will wake on the hr::min::sec specified.	
Dynamic Time: System will wake on the current time + Increase minute(s)	
Wake up day (Fixed time option)	0
Select 0 for daily system wake up, 1-31 for which day of month that you would like the system to wake up.	
Wake up hour (Fixed time option)	0
Select 0-23 For example enter 3 for 3am and 15 for 3pm.	
Wake up minute (Fixed time option)	0
0-59	
Wake up second (Fixed time option)	0
0-59	
Wake up minute increase (Dynamic time option)	1
1-5	

3.4.9 Advanced: Digital I/O Port Configuration



DIO_P#1~4	Input
	Output
Set DIO as Input or Output	
DIO_P#5~8	Input
	Output
Set DIO as Input or Output	
DIO_P#1~4 Direction	Low
	High
Set output level when DIO pin is output	

3.5 Setup submenu: Chipset



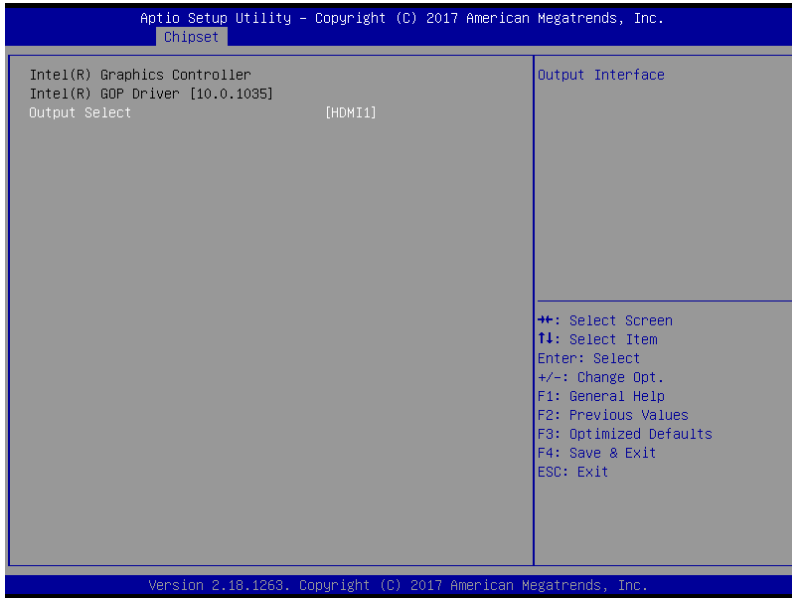
3.5.1 Chipset: North Bridge



Options summary:

Primary Display	IGD
	PCIe
Select which of IGD/PCI Graphics device should be Primary Display	

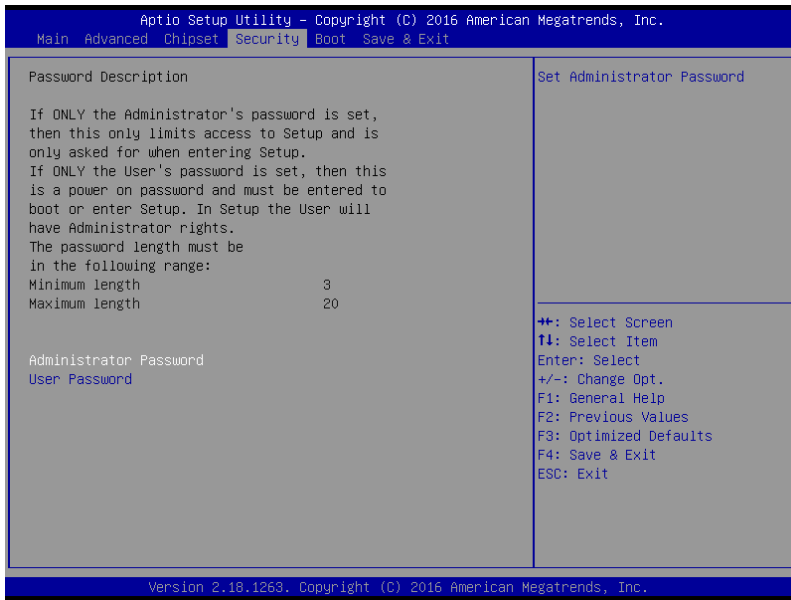
3.5.1.1 North Bridge: AMI Graphic Output Protocol Policy



Options summary :

Output Select	HDMI1
Output Interface	

3.6 Setup submenu: Security



Change User/Administrator Password

You can set password for limit BIOS access -

If ONLY the Administrator's password is set, a password window will be prompted when user can enter Setup utility. User can (Note#1) enter Setup utility with limited access (Note#2), if user presses "Enter Key" directly. User can have full access to Setup utility if password is given.

If ONLY the User's password is set, a password window will always be prompted during POST. User can have system boot only if password is given. In the meanwhile, User have full access to Setup utility.

If BOTH "User" and "Administrator" passwords are set, a password window will always be prompted during POST. User can have system boot only if password is given. In the

meanwhile, user access level in Setup utility depends on password given.

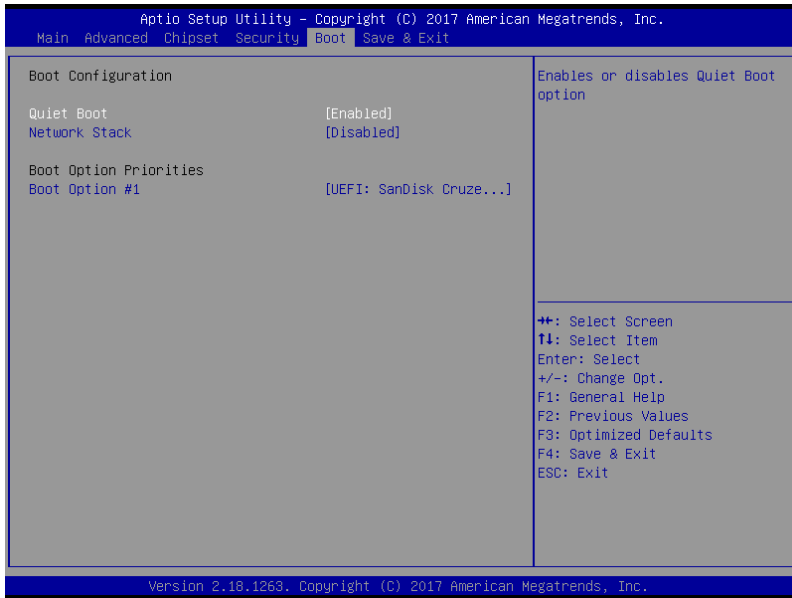
Note:

1. BIOS can be customized to disallow user enter setup in such situation.
2. How user is limited" will need to be customized according customer's actual application.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter directly to disable password protection.

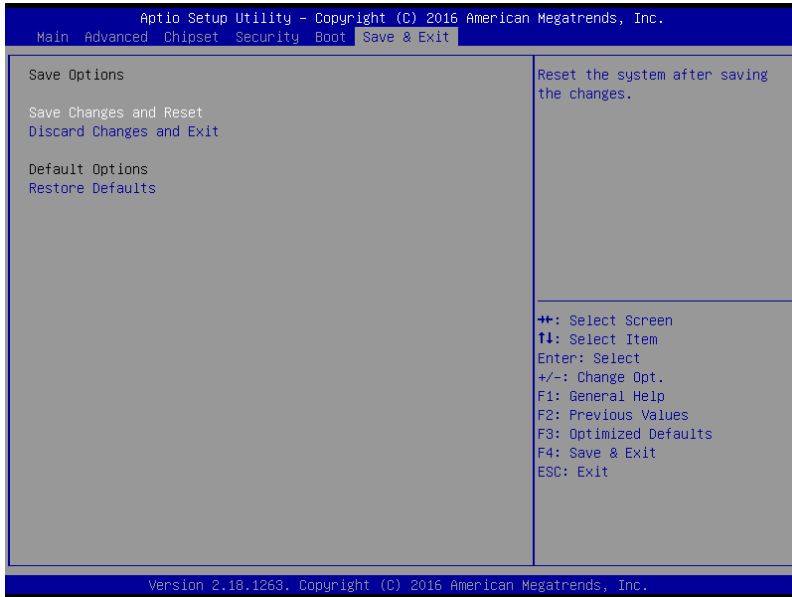
3.7 Setup submenu: Boot



Options summary :

Quiet Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Network Stack	Disabled
	Enabled
Enable/Disable UEFI Network Stack	

3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Driver Installation

Please download the driver from AAEON website. It contains all the drivers and utilities you need to setup your product. Follow the steps below to install the drivers.

<http://www.aaeon.com/en/p/desktop-network-appliance-fws-2271>

Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphics** folder followed by **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 3 – Install TXE Driver

1. Open the **Step 4 - TXE** folder, followed by the **SetupTXE.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install Network Driver

1. Open the **Step 3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
- 5.

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0x73(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0x72(Note6)	7(Note7)	1(Note8)	Select time unit. 1: second 0: minute
Watchdog Enable (KRST)	0x07(Note9)	0x72(Note10)	6(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0x71(Note14)	0(Note15)	1	1: Clear timeout status

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex //This parameter is represented from Note1
#define byte   SIOData //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN //This parameter is represented from Note3
#define byte   TimerReg //This parameter is represented from Note4
#define byte   TimerVal // This parameter is represented from Note24
#define byte   UnitLDN //This parameter is represented from Note5
#define byte   UnitReg //This parameter is represented from Note6
#define byte   UnitBit //This parameter is represented from Note7
#define byte   UnitVal //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
*****
```

```
*****  
VOID Main(){  
    // Procedure : AaeonWDTConfig  
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)  
    // (boolean)Unit : Select time unit(0: second, 1: minute).  
    AaeonWDTConfig();  
  
    // Procedure : AaeonWDTEnable  
    // This procedure will enable the WDT counting.  
    AaeonWDTEnable();  
}  
*****
```

```
*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****
```

```
*****
VOID  SIOEnterMBPnPMode0{
    Switch(SIOIndex){
        Case 0x2E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0x55);
            Break;
        Case 0x4E:
            IOWriteByte(SIOIndex, 0x87);
            IOWriteByte(SIOIndex, 0x01);
            IOWriteByte(SIOIndex, 0x55);
            IOWriteByte(SIOIndex, 0xAA);
            Break;
    }
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0x02);
    IOWriteByte(SIOData, 0x02);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}
*****
```

```
*****
VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

Appendix B

I/O Information

B.1 I/O Address Map




Network Appliance
FWS-2271

Input/output (IO)	
[0000000000000000]	PCI Express Root Complex
[0000000000000020]	Programmable interrupt controller
[0000000000000024]	Programmable interrupt controller
[0000000000000028]	Programmable interrupt controller
[000000000000002C]	Programmable interrupt controller
[000000000000002E]	Motherboard resources
[0000000000000030]	Programmable interrupt controller
[0000000000000034]	Programmable interrupt controller
[0000000000000038]	Programmable interrupt controller
[000000000000003C]	Programmable interrupt controller
[0000000000000040]	System timer
[000000000000004E]	Motherboard resources
[0000000000000050]	System timer
[0000000000000060]	Standard PS/2 Keyboard
[0000000000000061]	Motherboard resources
[0000000000000063]	Motherboard resources
[0000000000000064]	Standard PS/2 Keyboard
[0000000000000065]	Motherboard resources
[0000000000000067]	Motherboard resources
[0000000000000070]	Motherboard resources
[0000000000000070]	System CMOS/real time clock
[0000000000000078]	PCI Express Root Complex
[0000000000000080]	Motherboard resources
[0000000000000092]	Motherboard resources
[00000000000000A0]	Programmable interrupt controller
[00000000000000A4]	Programmable interrupt controller
[00000000000000A8]	Programmable interrupt controller
[00000000000000AC]	Programmable interrupt controller
[00000000000000B0]	Programmable interrupt controller
[00000000000000B2]	Motherboard resources
[00000000000000B4]	Programmable interrupt controller
[00000000000000B8]	Programmable interrupt controller
[00000000000000BC]	Programmable interrupt controller
[00000000000003F8]	Communications Port (COM1)
[0000000000000400]	Motherboard resources
[00000000000004D0]	Programmable interrupt controller
[0000000000000500]	Motherboard resources
[0000000000000680]	Motherboard resources
[0000000000000A00]	Motherboard resources
[0000000000000A30]	Motherboard resources
[0000000000000A40]	Motherboard resources
[0000000000000D00]	PCI Express Root Complex
[00000000000009000]	PCI-to-PCI Bridge
[00000000000009000]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
[00000000000009000]	PCI-to-PCI Bridge
[0000000000000A000]	PCI-to-PCI Bridge
[0000000000000B000]	PCI-to-PCI Bridge
[0000000000000C000]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
[0000000000000D000]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[0000000000000E000]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[0000000000000F000]	Intel(R) HD Graphics




















































 [000000000000F000 - 000000000000F03F] Intel(R) HD Graphics
 [000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
 [000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
 [000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
 [000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
--





















































B.2 Memory Address Map





















































Memory Address Range	Device Name
[000000007B800001 - 000000007BFFFFFF]	PCI Express Root Complex
[000000007C000001 - 000000007CFFFFFF]	PCI Express Root Complex
[0000000080000000 - 0000000080FFFFFF]	Intel(R) HD Graphics
[0000000080000000 - 0000000080FFFFFF]	Intel(R) HD Graphics
[0000000080000000 - 00000000CFFFFFFF]	PCI Express Root Complex
[0000000081000000 - 00000000810FFFFF]	High Definition Audio Controller
[0000000081100000 - 00000000811FFFFF]	PCI-to-PCI Bridge
[0000000081100000 - 00000000813FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB
[0000000081100000 - 00000000813FFFFF]	PCI-to-PCI Bridge
[00000000811DC000 - 00000000811DFFFF]	Intel(R) I211 Gigabit Network Connection #6
[00000000811E0000 - 00000000811FFFFF]	Intel(R) I211 Gigabit Network Connection #6
[0000000081200000 - 00000000812FFFFF]	PCI-to-PCI Bridge
[00000000812DC000 - 00000000812DFFFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000812E0000 - 00000000812FFFFF]	Intel(R) I211 Gigabit Network Connection #2
[0000000081300000 - 00000000813FFFFF]	PCI-to-PCI Bridge
[00000000813DC000 - 00000000813DFFFF]	Intel(R) I211 Gigabit Network Connection #5
[00000000813E0000 - 00000000813FFFFF]	Intel(R) I211 Gigabit Network Connection #5
[0000000081400000 - 00000000814FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADA
[00000000814DC000 - 00000000814DFFFF]	Intel(R) I211 Gigabit Network Connection
[00000000814E0000 - 00000000814FFFFF]	Intel(R) I211 Gigabit Network Connection
[0000000081500000 - 00000000815DFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[00000000815DC000 - 00000000815DFFFF]	Intel(R) I211 Gigabit Network Connection #4
[00000000815E0000 - 00000000815FFFFF]	Intel(R) I211 Gigabit Network Connection #4
[0000000081600000 - 00000000816FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[00000000816DC000 - 00000000816DFFFF]	Intel(R) I211 Gigabit Network Connection #3
[00000000816E0000 - 00000000816FFFFF]	Intel(R) I211 Gigabit Network Connection #3
[0000000081700000 - 000000008170FFFF]	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
[0000000081710000 - 0000000081713FFF]	High Definition Audio Controller
[0000000081714000 - 0000000081715FFF]	Standard SATA AHCI Controller
[0000000081716000 - 00000000817160FF]	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
[0000000081717000 - 00000000817177FF]	Standard SATA AHCI Controller
[0000000081718000 - 00000000817180FF]	Standard SATA AHCI Controller
[000000008171B000 - 000000008171BFFF]	Intel(R) Trusted Execution Engine Interface
[0000000090000000 - 000000009FFFFFFF]	Intel(R) HD Graphics
[0000000090000000 - 000000009FFFFFFF]	Intel(R) HD Graphics
[00000000D0C00000 - 00000000D0C00653]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C40000 - 00000000D0C40763]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C50000 - 00000000D0C5076B]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C70000 - 00000000D0C70673]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF]	PCI Express Root Complex
[00000000FEA00000 - 00000000FEAFFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED01000 - 00000000FED01FFF]	Motherboard resources
[00000000FED03000 - 00000000FED03FFF]	Motherboard resources
[00000000FED06000 - 00000000FED06FFF]	Motherboard resources
[00000000FED08000 - 00000000FED09FFF]	Motherboard resources
[00000000FED1C000 - 00000000FED1CFFF]	Motherboard resources
















































	[00000000FED40000 - 00000000FED44FFF] Trusted Platform Module 2.0
	[00000000FED80000 - 00000000FEDBFFFF] Motherboard resources
	[00000000FEE00000 - 00000000FEEFFFFF] Motherboard resources





















































B.3 IRQ Mapping Chart





















































Interrupt request (IRQ)	
 (ISA) 0x00000000 (00)	System timer
 (ISA) 0x00000001 (01)	Standard PS/2 Keyboard
 (ISA) 0x00000004 (04)	Communications Port (COM1)
 (ISA) 0x00000008 (08)	High precision event timer
 (ISA) 0x0000000C (12)	PS/2 Port Compatible Pointing Device
 (ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
 (ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
 (ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
 (ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
 (ISA) 0x00000036 (54)	Microsoft ACPI-Compliant System
 (ISA) 0x00000037 (55)	Microsoft ACPI-Compliant System
 (ISA) 0x00000038 (56)	Microsoft ACPI-Compliant System
 (ISA) 0x00000039 (57)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003A (58)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003B (59)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003C (60)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003D (61)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003E (62)	Microsoft ACPI-Compliant System
 (ISA) 0x0000003F (63)	Microsoft ACPI-Compliant System
 (ISA) 0x00000040 (64)	Microsoft ACPI-Compliant System
 (ISA) 0x00000041 (65)	Microsoft ACPI-Compliant System
 (ISA) 0x00000042 (66)	Microsoft ACPI-Compliant System
 (ISA) 0x00000043 (67)	Microsoft ACPI-Compliant System
 (ISA) 0x00000044 (68)	Microsoft ACPI-Compliant System
 (ISA) 0x00000045 (69)	Microsoft ACPI-Compliant System
 (ISA) 0x00000046 (70)	Microsoft ACPI-Compliant System
 (ISA) 0x00000047 (71)	Microsoft ACPI-Compliant System
 (ISA) 0x00000048 (72)	Microsoft ACPI-Compliant System
 (ISA) 0x00000049 (73)	Microsoft ACPI-Compliant System
 (ISA) 0x0000004A (74)	Microsoft ACPI-Compliant System
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
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


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	(ISA) 0x000001F1 (497)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F2 (498)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F3 (499)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F4 (500)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F5 (501)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F6 (502)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F7 (503)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F8 (504)	Microsoft ACPI-Compliant System
	(ISA) 0x000001F9 (505)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FA (506)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FB (507)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FC (508)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FD (509)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FE (510)	Microsoft ACPI-Compliant System

	(ISA) 0x000001FF (511)	Microsoft ACPI-Compliant System
	(PCI) 0x00000019 (25)	High Definition Audio Controller
	(PCI) 0xFFFFFD7 (-41)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFD8 (-40)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFD9 (-39)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDA (-38)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDB (-37)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDC (-36)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFFDD (-35)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDE (-34)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFDF (-33)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFE0 (-32)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFE1 (-31)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFE2 (-30)	Intel(R) I211 Gigabit Network Connection #5
	(PCI) 0xFFFFFE3 (-29)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE4 (-28)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE5 (-27)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE6 (-26)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE7 (-25)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE8 (-24)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFFE9 (-23)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFEA (-22)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFEB (-21)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFEC (-20)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFED (-19)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFEE (-18)	Intel(R) I211 Gigabit Network Connection #4
	(PCI) 0xFFFFFEF (-17)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF0 (-16)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF1 (-15)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF2 (-14)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF3 (-13)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF4 (-12)	Intel(R) I211 Gigabit Network Connection #3
	(PCI) 0xFFFFFFF5 (-11)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFF6 (-10)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFF7 (-9)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFF8 (-8)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFF9 (-7)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFFA (-6)	Intel(R) I211 Gigabit Network Connection #6
	(PCI) 0xFFFFFFFB (-5)	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
	(PCI) 0xFFFFFFFC (-4)	Intel(R) Trusted Execution Engine Interface
	(PCI) 0xFFFFFFFD (-3)	Intel(R) HD Graphics
	(PCI) 0xFFFFFFFE (-2)	Standard SATA AHCI Controller

Appendix C

Standard LAN Bypass Platform Setting

C.1 Status LED

The LED status indicator of FWS-2271 is programmable with AAEON SDK for your application.

Table1: LED Status

	STA_LED2	STA_LED1	STA_LED0
LED Off	0	0	0
Red LED On	0	0	1
Red LED Blink	0	1	0
Red LED Fast Blink	0	1	1
Reserved	1	0	0
Green LED Blink	1	0	1
Green LED Fast Blink	1	1	0
Green LED On	1	1	1

Table2: Status LED and register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
STA_LED2	R/W	0x00 (Note2)	2	(Table 1)
STA_LED1	R/W	0x00 (Note2)	1	(Table 1)
STA_LED0	R/W	0x00 (Note2)	0	(Table 1)

Sample Code:

```
*****
#define ByteCPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define ByteOFFSET //This parameter is represented from Note2
*****
bData = aaeonSmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);

switch( LED_FLAG)
{
case 0:
{
//LED Off
//BIT2=0, BIT1=0, BIT0=0
bData = bData & 0xF8;
break;
}
case 1:
{
//Red LED On
//BIT2=0, BIT1=0, BIT0=1
bData = (bData & 0xF8) | 0x01;
break;
}
case 2:
{
//Red LED Blink
//BIT2=0, BIT1=1, BIT0=0
bData = (bData & 0xF8) | 0x02;
break;
}
case 3:
{
//Red LED Fast Blink
//BIT2=0, BIT1=1, BIT0=1
bData = (bData & 0xF8) | 0x03;
break;
}
case 4:
{
//Green LED On
//BIT2=1, BIT1=1, BIT0=1
```

```
        bData = (bData & 0xF8) | 0x07;
        break;
    }
    case 5:
    {
        //Green LED Blink
        //BIT2=1, BIT1=0, BIT0=1
        bData = (bData & 0xF8) | 0x05;
        break;
    }
    case 6:
    {
        //Green LED Fast Blink
        //BIT2=1, BIT1=1, BIT0=0
        bData = (bData & 0xF8) | 0x06;
        break;
    }
    default:
        break;
    }
    SmbusWriteByte(CPLD_SLAVE_ADDRESS, 0x00, bData);
    *****
```


C.2 LAN Bypass

Table1: LAN Kit ID Select

LAN_ID2	LAN_ID1	LAN_ID0	LAN kit selected
0	0	0	LAN Kit 1 Selected
0	0	1	LAN Kit 2 Selected

Table2: LAN Bypass register table

Function	Description
LAN_ID3	
LAN_ID2	Use for selecting which LAN kit will be configured, refer to Table 1 of ID Select table of LAN kit. They should be set before ACT_EN.
LAN_ID1	
LAN_ID0	
PWR_ON	Use for configuring LAN Bypass function behavior to LAN kit, when system power on. 1: Bypass 0: Pass Through
PWR_OFF	Use for configuring LAN Bypass function behavior to LAN kit, when system power off. 1: Bypass 0: Pass Through
WDT_EN	Use for configuring WDT function behavior to LAN kit, when WDT triggered. 0: Normal WDT reset (Default) 1: Force Bypass
ACT_EN	Use for activating programming of LAN kit. It is edge triggering (falling edge 1 to 0) and should be set to high(1) as its normal state.

Table3: LAN Bypass register mapping table

CPLD Slave Address 0x90 (Note1)				
	Attribute	Offset(SMBUS)	BitNum	Value
LAN_ID3	R/W	0x01(Note2)	3	(Table 1)
LAN_ID2	R/W	0x01(Note2)	2	(Table 1)
LAN_ID1	R/W	0x01(Note2)	1	(Table 1)
LAN_ID0	R/W	0x01(Note2)	0	(Table 1)
PWR_ON	R/W	0x01(Note2)	6	(Table 2)
PWR_OFF	R/W	0x01(Note2)	5	(Table 2)
WDT_EN	R/W	0x01(Note2)	4	(Table 2)
ACT_EN	R/W	0x01(Note2)	7	(Table 2)

Sample Code

```

*****
#define ByteCPLD_SLAVE_ADDRESS //This parameter is represented from Note1
#define ByteOFFSET //This parameter is represented from Note2
*****

// Select Lan Pair
BYTE bLanSel = LAN_PAIR;

BYTE bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
// Set Reg01h bit3
if(bLanSel & 0x08)
    bData = bData | 0x08;
else
    bData = bData & 0xF7;
// Set Reg01h bit2
if(bLanSel & 0x04)
    bData = bData | 0x04;
else
    bData = bData & 0xFB;
// Set Reg01h bit1
if(bLanSel & 0x02)
    bData = bData | 0x02;
else
    bData = bData & 0xFD;

```

```
// Set Reg01h bit0
if(bLanSel & 0x01)
    bData = bData | 0x01;
else
    bData = bData & 0xFE;

// Power On Action (Reg01h bit6)
if(SET_PASS_THROUGH) // Pass Through
    bData = bData & 0xBF;
else // Bypass
    bData = bData | 0x40;

// Power Off Action (Reg01h bit5)
if(SET_PASS_THROUGH) // Pass Through
    bData = bData & 0xDF;
else // Bypass
    bData = bData | 0x20;

// WDT Action (Reg01h bit4)
if(SET_WDT_RESET)// Reset
    bData = bData & 0xEF;
else // Bypass
    bData = bData | 0x10;

SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData);

// Apply Settings (Reg01h bit7)
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData & 0x7F);
Sleep(500);
bData = SmbusReadByte(CPLD_SLAVE_ADDRESS, OFFSET);
SmbusWriteByte(CPLD_SLAVE_ADDRESS, OFFSET, bData | 0x80);
*****
```

C.3 Software Reset Button Configuration

Table 1: Soft Reset Button register mapping table

	Attribute	Register(I/O)	BitNum	Value
BTN_STS	R	0xA05(Note1)	4(Note2)	(Note3)

Table 2: LAN Bypass register table

Function	Description
BTN_STS	Reading this register returns the pin level status which is normal high active low. 0: Pin Level States Low. 1: Pin Level States High.

Sample Code:

```

*****
#define Word    BTN_STS    //This parameter is represented from Note1
#define ByteBTN_STS_R    //This parameter is represented from Note2
*****
Byte  GET_Value (Word IoAddr, Byte BitNum,Byte Value){
    BYTE  TmpValue;

    TmpValue = inportb (IoAddr);
    return  (TmpValue & (1 << BitNum))
}
*****
VOID  Main(){
    Byte RstBtn;

    RstBtn = GET_Value (BTN_STS, BTN_STS_R); // Active Low
}
*****

```