EPIC-PTH9

EPIC Board

User's Manual 1st Ed

Last Updated: June 23, 2026

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● EPIC-PTH9	1
● Screw Kit	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page on AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON **主板/子板/背板** QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period)) : 10年

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON Main Board/Daughter Board/Backplane QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○

The table is prepared in accordance with the provisions of SJ/T 11364.

○：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years

Notes: This product defined period of use is under normal condition.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	4" EPIC Board
CPU	Intel® Core™ Ultra Series 3 processors: Intel® Core™ Ultra X7 Processor 358H (16C/16T, up to 4.8 GHz, 25W) Intel® Core™ Ultra 7 Processor 356H (16C/16T, up to 4.7 GHz, 25W)
Chipset	Integrated with Intel® SoC
Memory Type	DDR5 7200, Dual-Channel SODIMM x 2, up to 128GB (Non ECC)
BIOS	UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Security	TPM 2.0
RTC Battery	Lithium Battery 3V/240mAh
Dimension	4.53" x 6.50" (115mm x 165mm)
OS Support	Windows 11 (64-bit) Ubuntu 26.04 kernel 7.0.0-14 generic

Power

Power Requirement	9V – 24V DC or 12V only
Power Supply Type	AT/ATX (Default: AT)
Connector	4-pin ATX Connector
Power Consumption	Intel® Core™ Ultra X7 Processor 358H, DDR5 32GB, 8.23A @+12V (Typical) Intel® Core™ Ultra X7 Processor 358H, DDR5 32GB, 9.32A @+12V (Max)

Display

Controller	Intel® Graphics (Intel® Core™ Ultra 9 Processor 386H / Intel® Core™ Ultra 7 Processor 356H) Intel® Arc™ B390 GPU (Intel® Core™ Ultra X9 Processor 388H / Intel® Core™ Ultra X7 Processor 358H)
LVDS	LVDS x 1, Dual-Channel 18/24-bit, up to 1920 x 1080
eDP	eDP x 1, up to 3840 x 2160 (optional)
Display Interface	HDMI 2.1 x 1, up to 3840 x 2160 @60Hz DP 2.1 x 1, up to 3840 x 2160 @60Hz
Multiple Display	Up to 3 Simultaneous Displays

Audio

Codec	Realtek ALC897
Audio Interface	Line-in / Line-out / Mic (Audio function not available for WiTAS SKU)
Speaker	-

External I/O

Ethernet	Intel® Ethernet Connection I219, 1GbE RJ-45 x 1
	(PXE support x 1)
	Intel® Ethernet Controller I226, 2.5GbE RJ-45 x 3
	(PXE support x 1)
USB	USB 2.0 x 2
	USB 3.2 Gen 2 x 2
Serial Port	-
Video	DP 2.1 x 1
	HDMI 2.1 x 1

Internal I/O

USB	USB 2.0 x 4
Serial Port	COM 1, COM 2 (RS-232/422/485, support 5V/12V/RI)
	COM 3, COM 4 (RS-232 only, support RI only)
Audio	Audio Header x 1
DIO/GPIO	GPIO 8-bit
SMBus/I2C	SMBus / I2C /Timed GPIO (Default: SMBus, change by BOM)
Touch	-
Fan	4-pin Smart Fan
SIM	Nano SIM x 1
Front Panel	Power Button, Reset Button, Power LED, Buzzer
Others	-

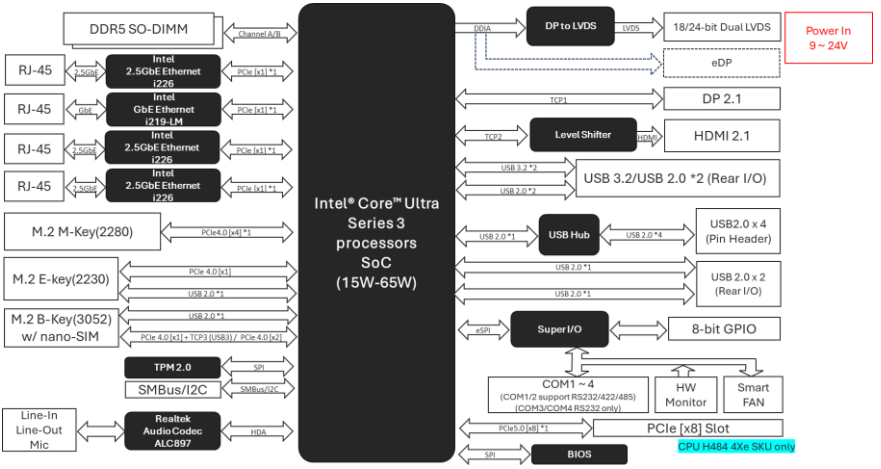
Expansion

M.2	M.2 3052 B-Key x 1 (PCIe 4.0 [x1] + USB 3.0 / PCIe 4.0 [x2] x 1) Default: PCIe 4.0 [x2], change by BOM M.2 2280 M-Key x 1 (PCIe 4.0 [x4]) M.2 2230 E-Key x 1 (PCIe 4.0 [x1] + USB 2.0)
Others	PCIe 5.0 [x8] Slot x 1 (support by Intel® Core™ Ultra 7 Processor 356H CPU only)

Environmental

Operating Temperature	-4°F – 158°F (-20°C – 70°C)
Storage Temperature	-40°F – 185°F (-40°C – 85°C)
Operating Humidity	0% – 90% relative humidity, non-condensing
MTBF (Hours)	860,096
Certification	CE/FCC Class A

1.2 Block Diagram

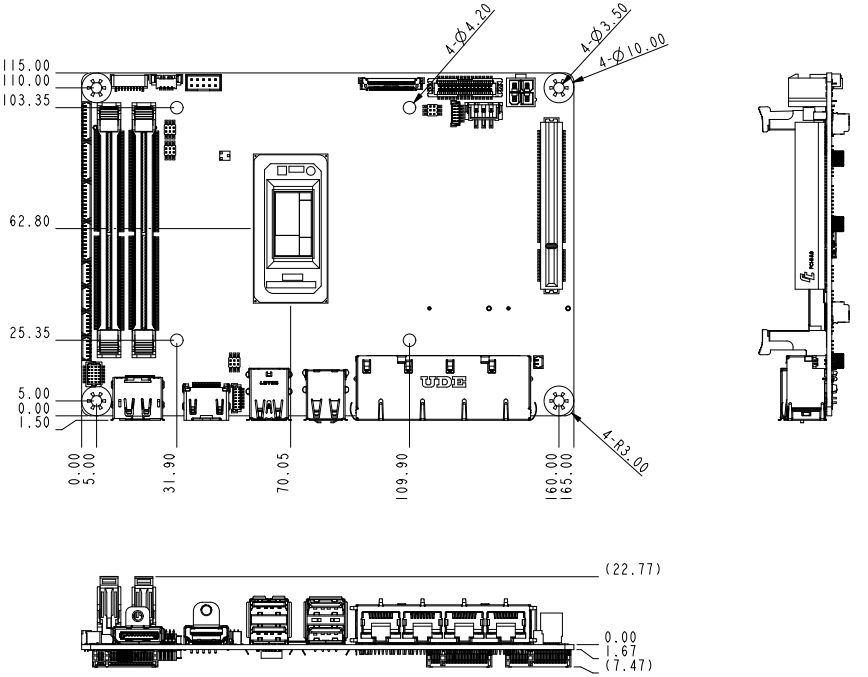


Chapter 2

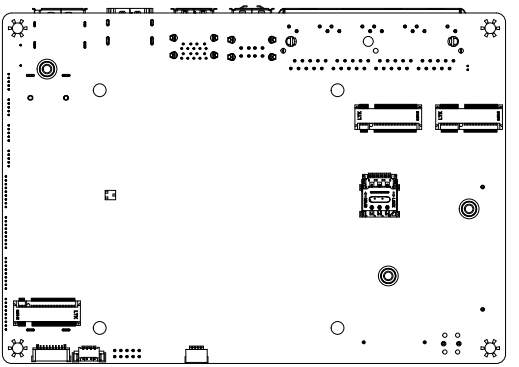
Hardware Information

2.1 Dimensions

Top View

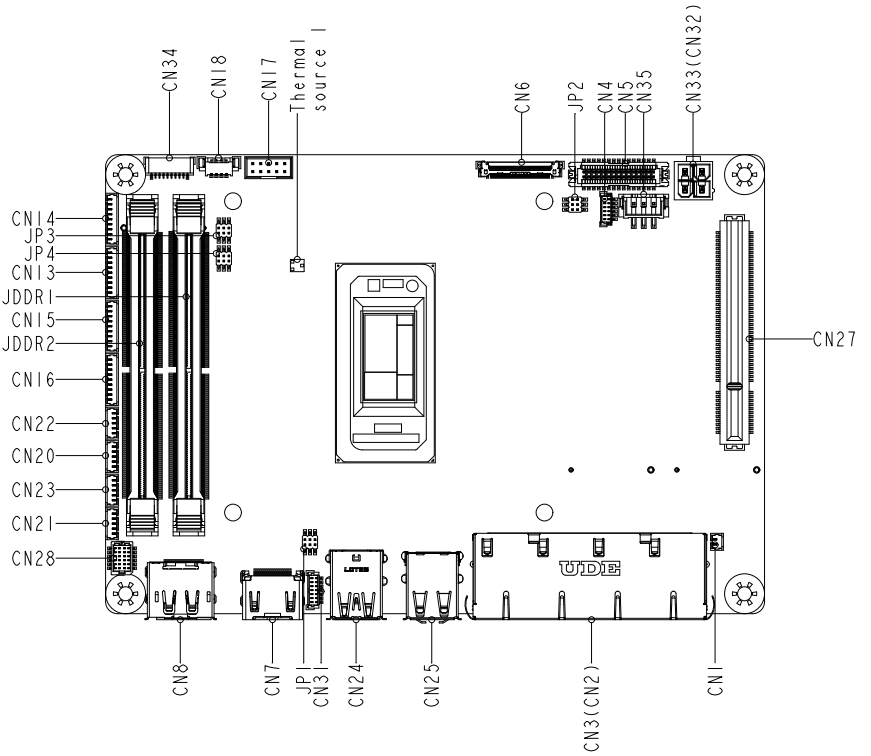


Bottom View

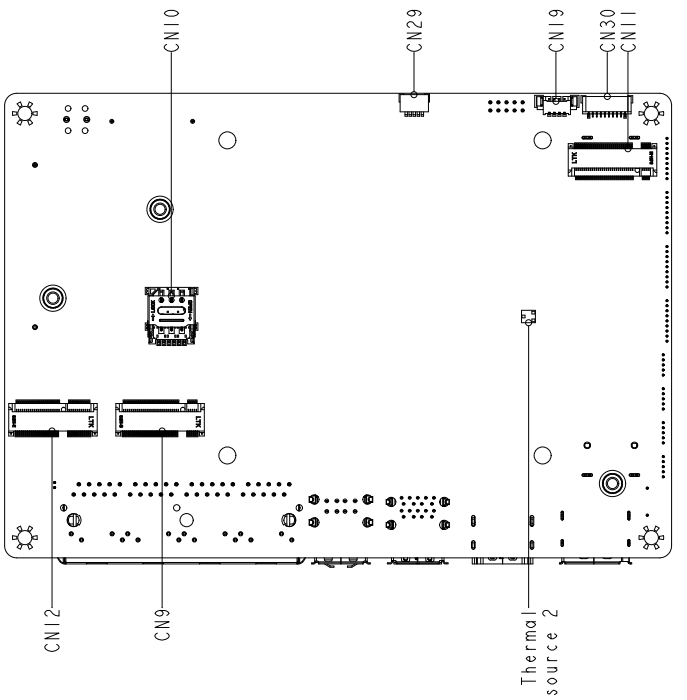


2.2 Jumpers and Connectors

Top View



Bottom View

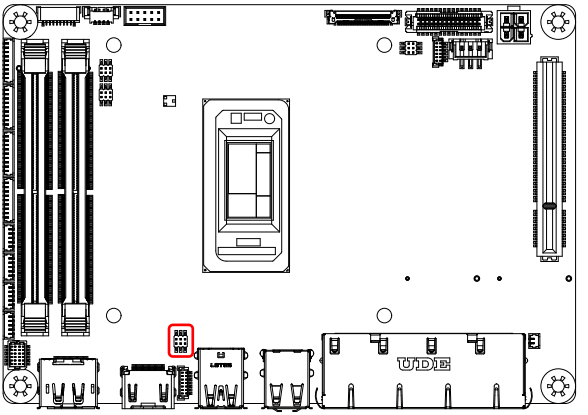


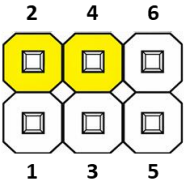
2.3 List of Jumpers

The board features a number of jumpers which can be configured for your application. Please refer to the table below and following sections for all jumpers which can be configured.

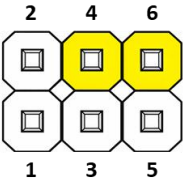
Label	Function
JP1 (2-4-6)	Clear CMOS Jumper
JP1 (1-3-5)	Auto Power Button Enable/Disable Selection
JP2 (2-4-6)	LVDS/eDP Operating Voltage Selection
JP2 (1-3-5)	LVDS Backlight Inverter Voltage Selection
JP3	COM 1 Pin 9 Function Selection
JP4	COM 2 Pin 9 Function Selection

2.3.1 Clear CMOS Jumper (JP1)





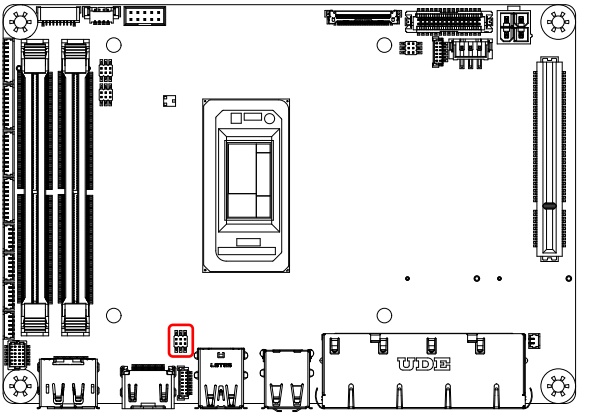
Normal (Default)

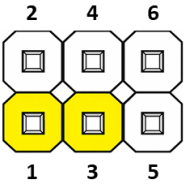


Enable CMOS

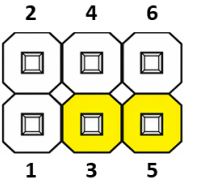
Clear CMOS Jumper		
2-4	Save CMOS	Default
4-6	Clear CMOS	

2.3.2 Auto Power Button Enable/Disable (JP1)





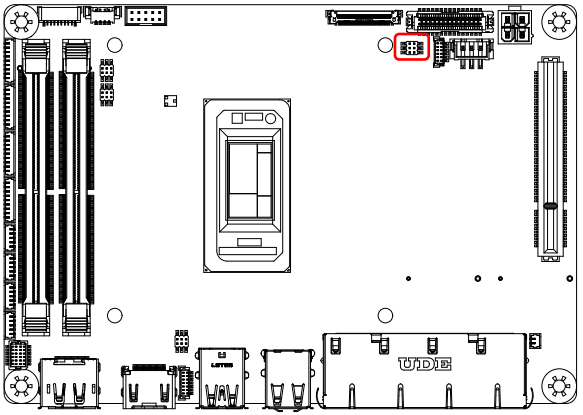
Disable Auto Power Button

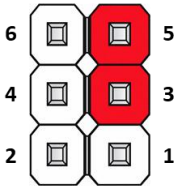


Enable Auto Power Button (Default)

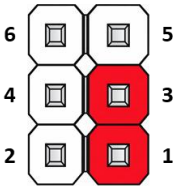
Auto Power Button Enable/Disable Selection		
1-3	Disable	
3-5	Enable	Default

2.3.3 LVDS Backlight Inverter Voltage Selection (JP2)





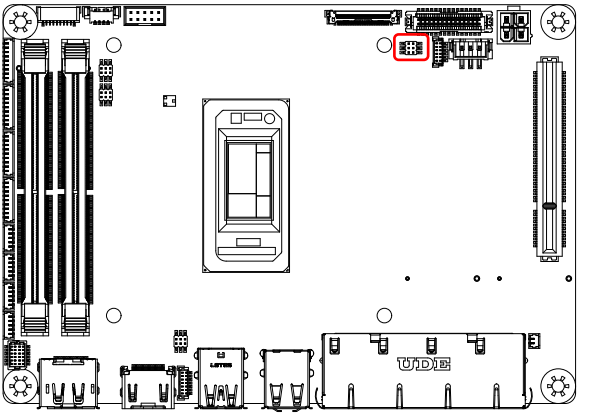
5V (Default)

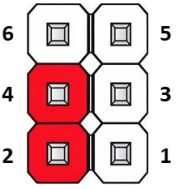


+12V

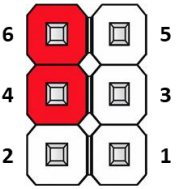
LVDS Backlight Inverter Voltage Selection		
1-3	+12V	
3-5	+5V	Default

2.3.4 LVDS/eDP Operating Voltage Selection (JP2)





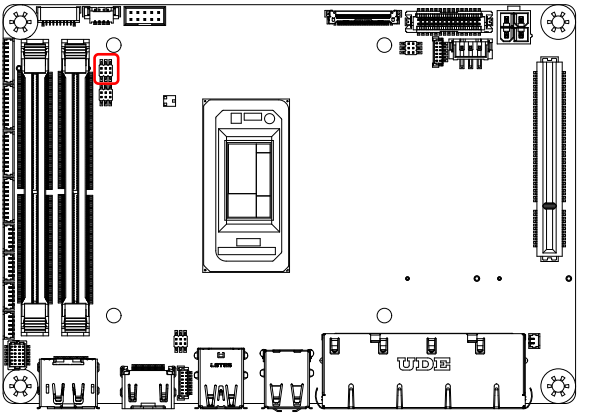
3.3V (Default)

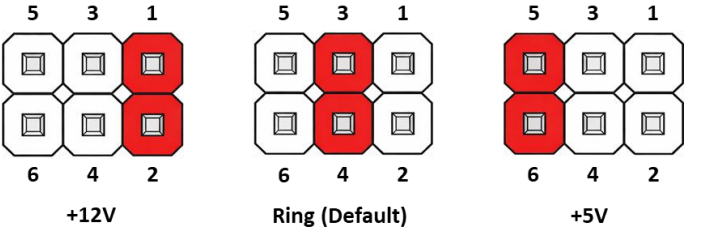


+5V

LVDS/eDP Operating Voltage Selection		
2-4	+3.3V	Default
4-6	+5V	

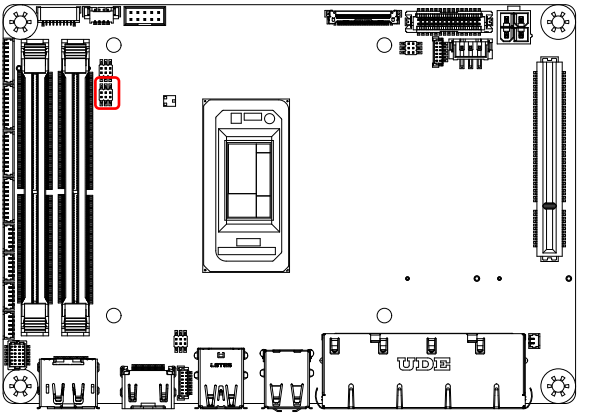
2.3.5 COM 1 Pin 9 Function Selection (JP3)

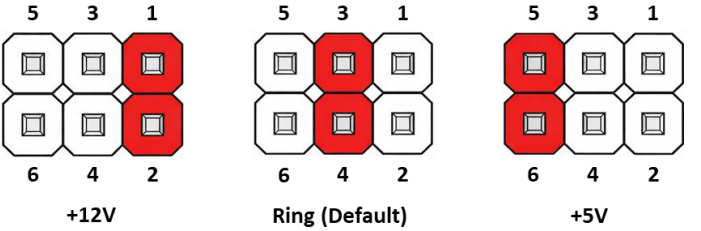




COM 1 Port Power/RI Selection (JP3)		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

2.3.6 COM 2 Pin 9 Function Selection (JP4)





COM 2 Port Power/RI Selection (JP4)		
1-2	+12V	
3-4	Ring	Default
5-6	+5V	

2.4 List of Connectors

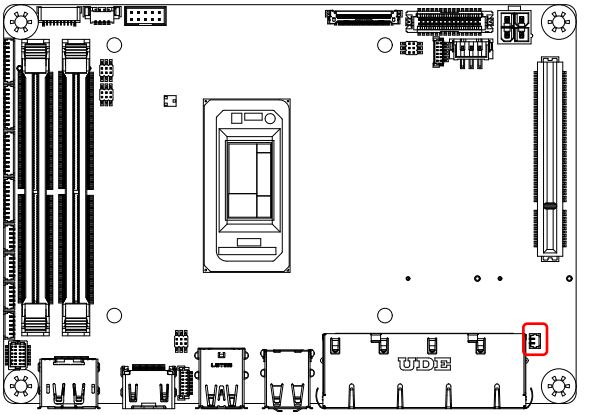
This section details the connectors featured on the board, which can be configured for your application.

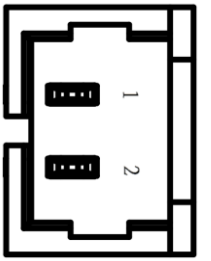
Please refer to the table below for a list of all connectors on this board which can be configured.

Label	Function
CN1	RTC Battery Connector
CN3	RJ-45 LAN Port 1/Port 2/Port 3/Port 4
CN4	LVDS Inverter/Backlight Connector
CN5	LVDS Connector
CN6	eDP Connector
CN7	HDMI Port
CN8	Display Port
CN9	M.2 3052 B-Key Slot
CN10	Nano SIM Card Socket
CN11	M.2 2280 M-Key Slot
CN12	M.2 2230 E-Key
CN13	COM Port 1 Header
CN14	COM Port 2 Header
CN15	COM Port 3 Header
CN16	COM Port 4 Header
CN17	8-bit GPIO Header
CN18	4-pin Fan 1 Connector
CN19	4-pin Fan 2 Connector
CN20	USB 2.0 Port 5 Header
CN21	USB 2.0 Port 6 Header
CN22	USB 2.0 Port 7 Header
CN23	USB 2.0 Port 8 Header
CN24	USB 3.2/USB 2.0 Port 1/Port 2
CN25	USB 2.0 Port 3/Port 4
CN27	PCIe [x8] Slot
CN28	Audio I/O Port
CN29	I2C/SMBus Connector
CN30	Port 80 Debug Port Connector
CN31	SPI Flash Programming Port
CN33	External Power Input
CN34	Front Panel

Label	Function
CN35	External +5VSB Input
JDDR1	DDR5 SODIMM Channel 1
JDDR2	DDR5 SODIMM Channel 2

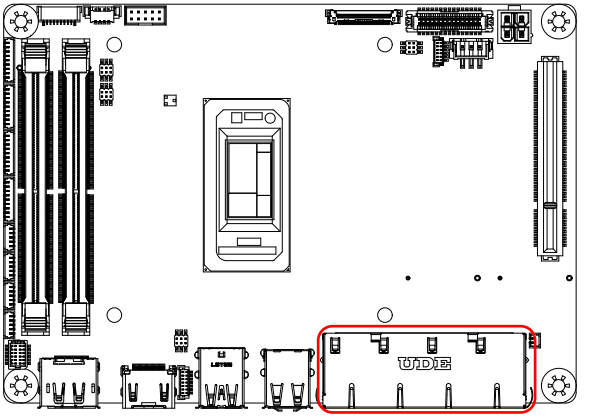
2.4.1 RTC Battery Connector (CN1)

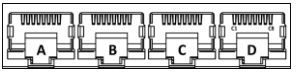




Pin	Pin Name	Signal Type	Signal Level
1	+3.3V	PWR	+3.3V
2	GND	GND	GND

2.4.2 RJ-45 LAN Port 1/Port 2/Port 3/Port 4 (CN3)





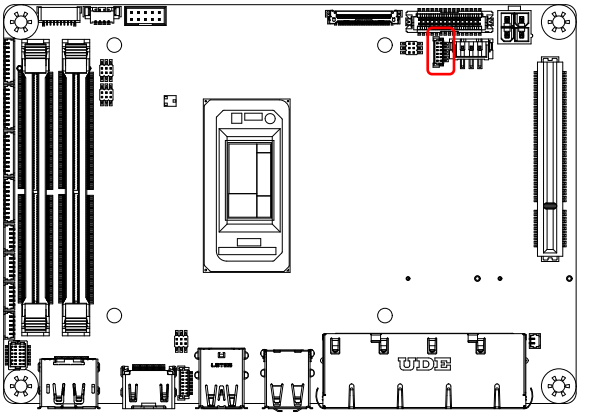
Pin	Pin Name	Signal Type	Signal Level
A_1	LAN2_MDI0_P	DIFF	-
A_2	LAN2_MDI0_N	DIFF	-
A_3	LAN2_MDI1_P	DIFF	-
A_4	LAN2_MDI1_N	DIFF	-

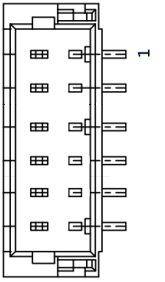
Pin	Pin Name	Signal Type	Signal Level
A_5	LAN2_MDI2_P	DIFF	-
A_6	LAN2_MDI2_N	DIFF	-
A_7	LAN2_MDI3_P	DIFF	-
A_8	LAN2_MDI3_N	DIFF	-
B_1	LAN1_MDI0_P	DIFF	-
B_2	LAN1_MDI0_N	DIFF	-
B_3	LAN1_MDI1_P	DIFF	-
B_4	LAN1_MDI1_N	DIFF	-
B_5	LAN1_MDI2_P	DIFF	-
B_6	LAN1_MDI2_N	DIFF	-
B_7	LAN1_MDI3_P	DIFF	-
B_8	LAN1_MDI3_N	DIFF	-
C_1	LAN3_MDI0_P	DIFF	-
C_2	LAN3_MDI0_N	DIFF	-
C_3	LAN3_MDI1_P	DIFF	-
C_4	LAN3_MDI1_N	DIFF	-
C_5	LAN3_MDI2_P	DIFF	-
C_6	LAN3_MDI2_N	DIFF	-
C_7	LAN3_MDI3_P	DIFF	-
C_8	LAN3_MDI3_N	DIFF	-
D_1	LAN4_MDI0_P	DIFF	-
D_2	LAN4_MDI0_N	DIFF	-
D_3	LAN4_MDI1_P	DIFF	-
D_4	LAN4_MDI1_N	DIFF	-
D_5	LAN4_MDI2_P	DIFF	-
D_6	LAN4_MDI2_N	DIFF	-
D_7	LAN4_MDI3_P	DIFF	-
D_8	LAN4_MDI3_N	DIFF	-

Note: The chip used for LAN port 1 is Intel® Ethernet Connection I219.

Note: The chip used for LAN ports 2, 3, and 4 is Intel® Ethernet Controller I226.

2.4.3 LVDS Inverter/Backlight Connector (CN4)

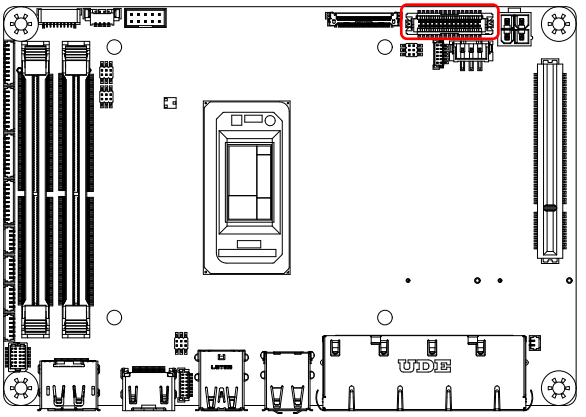


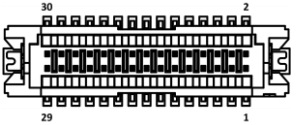


Pin	Pin Name	Signal Type	Signal Level
1	BKL_PWR	PWR	+5V(Default)/+12V
2	BKL_PWR	PWR	+5V(Default)/+12V
3	BKL_CONTROL	OUT	-
4	GND	GND	GND
5	GND	GND	GND
6	BKL_ENABLE	OUT	+3.3V

Note: BKL_PWR can be set to +5V or +12V by JP3.
Note: The driving current of BKL_PWR supports up to 2.5A.

2.4.4 LVDS Connector (CN5)



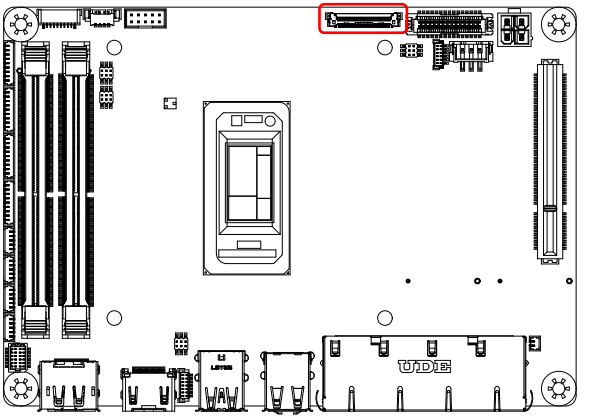


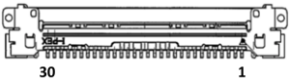
Pin	Pin Name	Signal Type	Signal Level
1	BKL_ENABLE	OUT	-
2	BKL_CONTROL	OUT	-
3	LCD_PWR	PWR	+3.3V/+5V
4	GND	GND	GND
5	LVDS_A_CLK-	DIFF	-
6	LVDS_A_CLK+	DIFF	-
7	LCD_PWR	PWR	+3.3V/+5V
8	GND	GND	GND
9	LVDS_DA0-	DIFF	-
10	LVDS_DA0+	DIFF	-
11	LVDS_DA1-	DIFF	-
12	LVDS_DA1+	DIFF	-
13	LVDS_DA2-	DIFF	-
14	LVDS_DA2+	DIFF	-
15	LVDS_DA3-	DIFF	-
16	LVDS_DA3+	DIFF	-
17	DDC_DATA	IN/OUT	+3.3V
18	DDC_CLK	IN/OUT	+3.3V
19	LVDS_DB0-	DIFF	-
20	LVDS_DB0+	DIFF	-
21	LVDS_DB1-	DIFF	-
22	LVDS_DB1+	DIFF	-
23	LVDS_DB2-	DIFF	-
24	LVDS_DB2+	DIFF	-

Pin	Pin Name	Signal Type	Signal Level
25	LVDS_DB3-	DIFF	-
26	LVDS_DB3+	DIFF	-
27	LCD_PWR	PWR	+3.3V/+5V
28	GND	GND	GND
29	LVDS_B_CLK-	DIFF	-
30	LVDS_B_CLK+	DIFF	-

Note: +VDD can be set to +3.3V or +5V by JP2.
Note: The driving current of +VDD supports up to 1.5A.
Note: LVDS and eDP can be set by BOM. Default is LVDS.
Note: For Single Channel LVDS, connect the LVDS_DA signals.
Note: For Dual Channel LVDS, connect the LVDS_DA signals to the odd-numbered channels, and the LVDS_DB signals to the even-numbered channels.

2.4.5 eDP Connector (CN6)



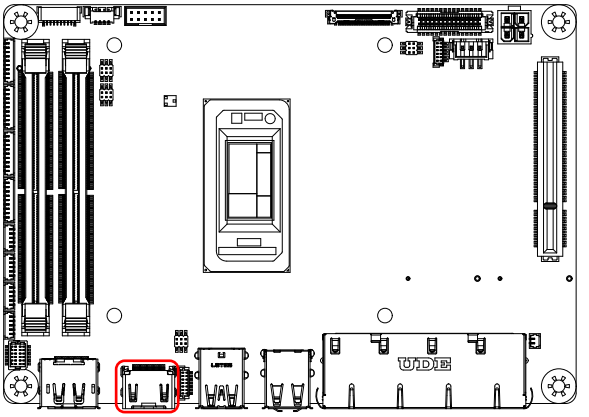


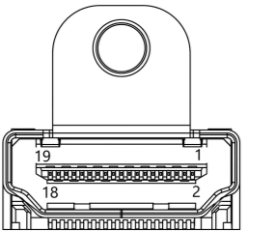
Pin	Pin Name	Signal Type	Signal Level
1	+VCC_EDP_BKLT	PWR	+12V
2	+VCC_EDP_BKLT	PWR	+12V
3	+VCC_EDP_BKLT	PWR	+12V
4	+VCC_EDP_BKLT	PWR	+12V
5	GND	GND	GND
6	GND	GND	GND
7	GND	GND	GND
8	EDP_HPD	-	-
9	EDP_BKLT_EN	-	-

Pin	Pin Name	Signal Type	Signal Level
10	NC		
11	EDP_BKLTCTL	-	-
12	GND	GND	GND
13	EDP_ AUX _DP	DIFF	-
14	EDP_ AUX _DN	DIFF	-
15	GND	GND	GND
16	EDP_LANE3_DP	DIFF	-
17	EDP_LANE3_DN	DIFF	-
18	GND	GND	GND
19	EDP_LANE0_DP	DIFF	-
20	EDP_LANE0_DN	DIFF	-
21	GND	GND	GND
22	EDP_LANE1_DP	DIFF	-
23	EDP_LANE1_DN	DIFF	-
24	GND	GND	GND
25	EDP_LANE2_DP	DIFF	-
26	EDP_LANE2_DN	DIFF	-
27	GND	GND	GND
28	+VDD	PWR	+3.3V
29	+VDD	PWR	+3.3V
30	+VDD	PWR	+3.3V

Note: +VDD can be set to +3.3V or +5V by JP2.
Note: The driving current of +VDD supports up to 1.5A.
Note: LVDS and eDP can be set by BOM. Default is LVDS.
Note: The driving current of +VCC_EDP_BKLT supports up to 1.2A

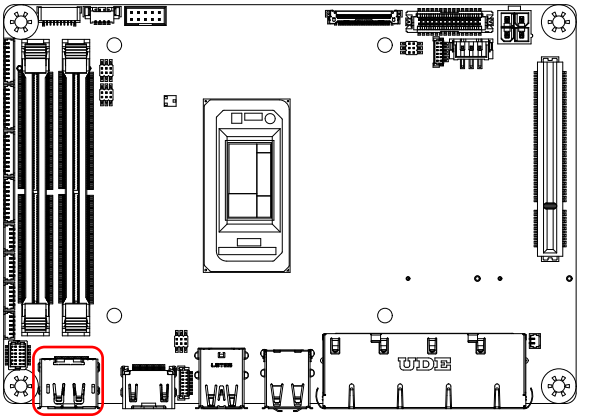
2.4.6 HDMI Port (CN7)

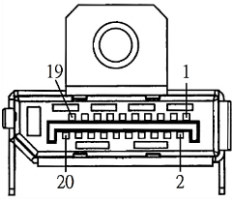




Pin	Pin Name	Signal Type	Signal Level
1	HDMI_TX2+	DIFF	-
2	GND	GND	GND
3	HDMI_TX2-	DIFF	-
4	HDMI_TX1+	DIFF	-
5	GND	GND	GND
6	HDMI_TX1-	DIFF	-
7	HDMI_TX0+	DIFF	-
8	GND	GND	GND
9	HDMI_TX0-	DIFF	-
10	HDMI_CLK+	DIFF	-
11	GND	GND	GND
12	HDMI_CLK-	DIFF	-
13	N/A	N/A	N/A
14	N/A	N/A	N/A
15	DDC_CLK	IN/OUT	-
16	DDC_DATA	IN/OUT	-
17	GND	GND	GND
18	+V5S	PWR	+5V
19	HDMI_HPD	IN	-

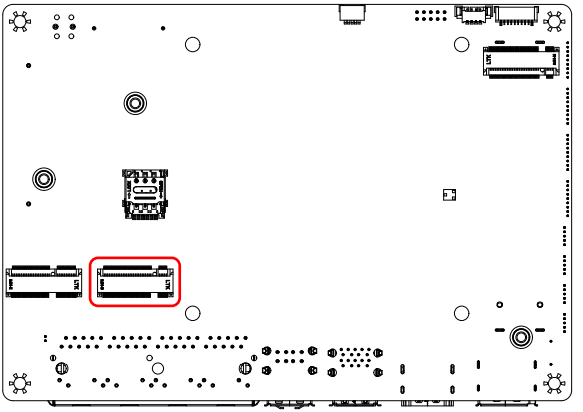
2.4.7 Display Port (CN8)

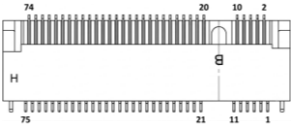




Pin	Pin Name	Signal Type	Signal Level
1	DP_TX0_DP	DIFF	-
2	GND	GND	GND
3	DP_TX0_DN	DIFF	-
4	DP_TX1_DP	DIFF	-
5	GND	GND	GND
6	DP_TX1_DN	DIFF	-
7	DP_TX2_DP	DIFF	-
8	GND	GND	GND
9	DP_TX2_DN	DIFF	-
10	DP_TX3_DP	DIFF	-
11	GND	GND	GND
12	DP_TX3_DN	DIFF	-
13	DP_OB_AUX_EN	IN	-
14	GND	GND	GND
15	DP_AUX_DP	IN/OUT	-
16	GND	GND	GND
17	DP_AUX_DN	IN/OUT	-
18	DP_HPD	IN/OUT	-
19	GND	GND	GND
20	+3.3V	PWR	+3.3V

2.4.8 M.2 3052 B-Key Slot (CN9)



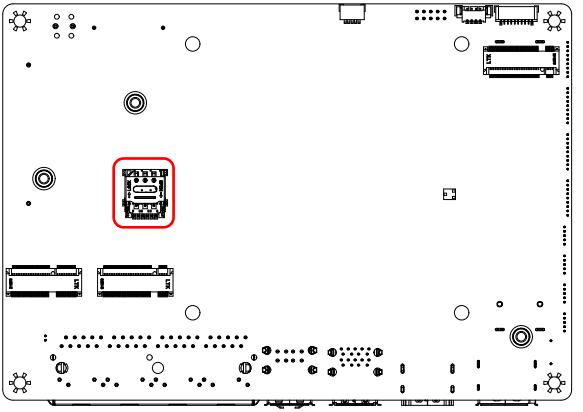


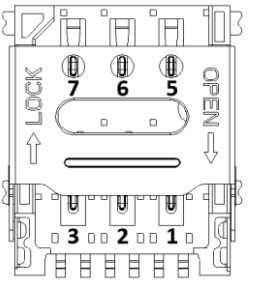
Pin	Pin Name	Signal Type	Signal Level
1	NC		
2	+V3P3S	PWR	+3.3V
3	GND	GND	GND
4	+V3P3S	PWR	+3.3V
5	GND	GND	GND
6	NC		
7	USB2_DP	DIFF	-
8	KEYB_DISABLE_N	IN	
9	USB2_DN	DIFF	-
10	PCH_SATA_LED_N	OUT	+3.3V
11	GND	GND	GND
20	NC	-	-
21	NC	-	-
22	NC	-	-
23	NC	-	-
24	NC	-	-
25	NC	-	-
26	NC	-	-
27	GND	GND	GND
28	NC	-	-
29	PCIE_B2_RXN/ USB3_2 _RXN	DIFF	-
30	UIM_RST_M2B	OUT	-

Pin	Pin Name	Signal Type	Signal Level
31	PCIE_B2_RXP/ USB3_2_ RXP	DIFF	-
32	UIM_CLK_M2B	-	-
33	GND	GND	GND
34	UIM_DAT_M2B	IN/OUT	-
35	PCIE_B2_TXN/ USB3_2_ TXN	DIFF	-
36	UIM_PWR	PWR	-
37	PCIE_B2_TXP/ USB3_2_T XP	DIFF	-
38	NC	-	-
39	GND	GND	GND
40	NC	-	-
41	PCIE_B1_RXN	DIFF	-
42	NC	-	-
43	PCIE_B1_RXP	DIFF	-
44	NC	-	-
45	GND	GND	GND
46	NC	-	-
47	PCIE_B1_TXN	DIFF	-
48	NC	-	-
49	PCIE_B1_TXP	DIFF	-
50	BUF_PLT_RST#	OUT	
51	GND	GND	GND
52	M2B_CLKREQ#	IN	-
53	PCIE_4_CLK_DN	DIFF	-
54	KEYB_WAKE_N	IN	-
55	PCIE_4_CLK_DP	DIFF	-
56	NC	-	-
57	GND	GND	GND
58	NC	-	-
59	NC	-	-
60	NC	-	-
61	NC	-	-
62	NC	-	-
63	NC	-	-
64	NC	-	-
65	NC	-	-
66	SIM_Detect	IN	-

Pin	Pin Name	Signal Type	Signal Level
67	KEYB_WWAN_RST_N	OUT	-
68	PCH_SUS_CLK	IN	-
69	NC	-	-
70	+V3P3A	PWR	+3.3V
71	GND	GND	GND
72	+V3P3A	PWR	+3.3V
73	GND	GND	GND
74	+V3P3A	PWR	+3.3V
75	NC	-	-

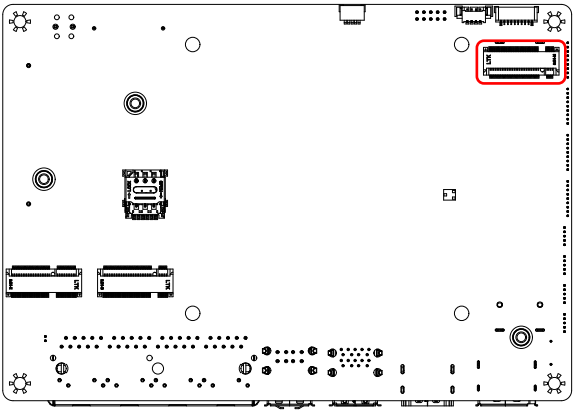
2.4.9 Nano SIM Card Socket (CN10)

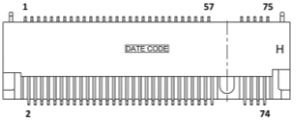




Pin	Pin Name	Signal Type	Signal Level
1	UIM_PWR	PWR	-
2	UIM_RST	IN	-
3	UIM_CLK	IN	-
5	GND	GND	GND
6	UIM_VPP	PWR	-
7	UIM_DATA	IN/OUT	-

2.4.10 M.2 2280 M-Key Slot (CN11)



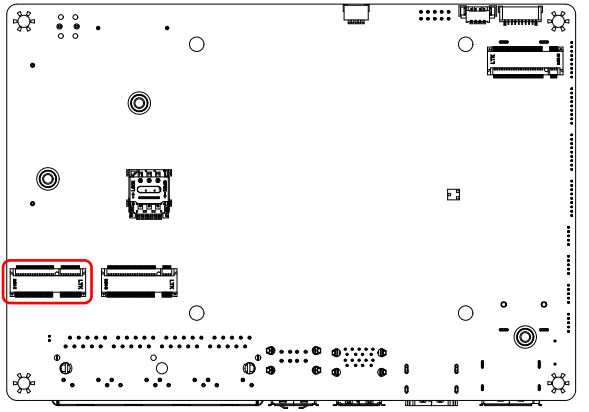


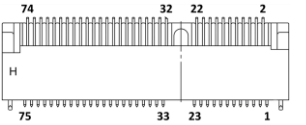
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V3P3S	PWR	+3.3V
3	GND	GND	GND
4	+V3P3S	PWR	+3.3V
5	PCIE_C4_RXN	DIFF	-
6	CARD_PWR_OFF_N	IN	-
7	PCIE_C4_RXP	DIFF	-
8	NC	-	-
9	GND	GND	GND
10	PCH_SATA_LED_N	OUT	+3.3V
11	PCIE_C4_TXN	DIFF	-
12	+V3P3S	PWR	+3.3V
13	PCIE_C4_TXP	DIFF	-
14	+V3P3S	PWR	+3.3V
15	GND	GND	GND
16	+V3P3S	PWR	+3.3V
17	PCIE_C3_RXN	DIFF	-
18	+V3P3S	PWR	+3.3V
19	PCIE_C3_RXP	DIFF	-
20	NC	-	-
21	GND	GND	GND
22	NC	-	-
23	PCIE_C3_TXN	DIFF	-
24	NC	-	-

Pin	Pin Name	Signal Type	Signal Level
25	PCIE_C3_TXP	DIFF	-
26	NC	-	-
27	GND	GND	GND
28	NC	-	-
29	PCIE_C2_RXN	DIFF	-
30	NC	-	-
31	PCIE_C2_RXP	DIFF	-
32	NC	-	-
33	GND	GND	GND
34	NC	-	-
35	PCIE_C2_TXN	DIFF	-
36	NC	-	-
37	PCIE_C2_TXP	DIFF	-
38	NC	-	-
39	GND	GND	GND
40	NC	-	-
41	PCIE_C1_RXN	DIFF	-
42	NC	-	-
43	PCIE_C1_RXP	DIFF	-
44	NC	-	-
45	GND	GND	GND
46	NC	-	-
47	PCIE_C1_TXN	DIFF	-
48	NC	-	-
49	PCIE_C1_TXP	DIFF	-
50	BUF_PLT_RST#	IN	-
51	GND	GND	GND
52	M2M_CLKREQ#	OUT	-
53	PCIE_6_CLK_DN	DIFF	-
54	PCIE_WAKE#	OUT	-
55	PCIE_6_CLK_DP	DIFF	-
56	NC	-	-
57	GND	GND	GND
58	NC	-	-
67	NC	-	-
68	SUS_CLK	IN	-
69	NC	-	-
70	+V3P3S	PWR	+3.3V
71	GND	GND	GND

Pin	Pin Name	Signal Type	Signal Level
72	+V3P3S	PWR	+3.3V
73	GND	GND	GND
74	+V3P3S	PWR	+3.3V
75	GND	GND	GND

2.4.11 M.2 2230 E-Key (CN12)



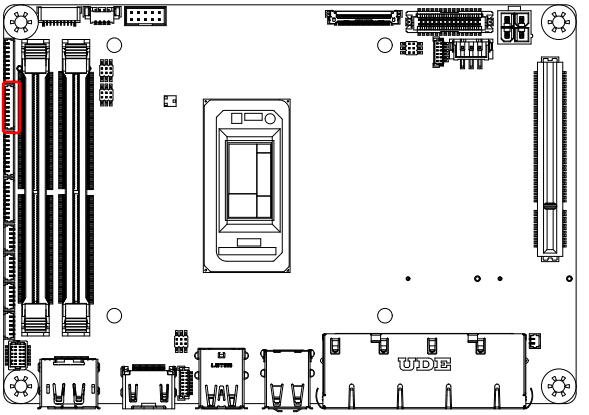


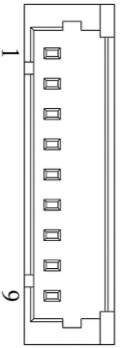
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	+V3P3A	PWR	+3.3V
3	USB2_DP	DIFF	-
4	+V3P3A	PWR	+3.3V
5	USB2_DN	DIFF	-
6	NC	-	-
7	GND	GND	GND
8	I2SCLK	OUT	-
9	NC	-	-
10	I2S_SYNC	OUT	-
11	NC	-	-
12	I2S_IN	IN	-
13	NC	-	-
14	I2S_OUT	OUT	-
15	NC	-	-
16	NC	-	-
17	NC	-	-

Pin	Pin Name	Signal Type	Signal Level
18	GND	GND	GND
19	NC	-	-
20	NC	-	-
21	NC	-	-
22	NC	-	-
23	NC	-	-
32	NC	-	-
33	GND	GND	GND
34	NC	-	-
35	PCIE_B3_TXP	DIFF	-
36	NC	-	-
37	PCIE_B3_TXN	DIFF	-
38	NC	-	-
39	GND	GND	GND
40	NC	-	-
41	PCIE_B3_RXP	DIFF	-
42	NC	-	-
43	PCIE_B3_RXN	DIFF	-
44	NC	-	-
45	GND	GND	GND
46	NC	-	-
47	PCIE_CLK_DP	DIFF	-
48	NC	-	-
49	PCIE_CLK_DN	DIFF	-
50	SUS_CLK	OUT	-
51	GND	GND	GND
52	BUF_PLT_RST#	OUT	-
53	PCIE_CLKREQ	IN	-
54	NC	-	-
55	PCIE_WAKE#	IN/OUT	-
56	NC	-	-
57	GND	GND	GND
58	NC	-	-
59	NC	DIFF	-
60	NC	-	-
61	NC	DIFF	-
62	NC	-	-
63	GND	GND	GND
64	NC	-	-

Pin	Pin Name	Signal Type	Signal Level
65	NC	-	-
66	NC	-	-
67	NC	-	-
68	NC	-	-
69	GND	GND	GND
70	NC	-	-
71	NC	-	-
72	+V3P3A	PWR	+3.3V
73	NC	-	-
74	+V3P3A	PWR	+3.3V
75	GND	GND	GND

2.4.12 COM Port 1 Header (CN13)





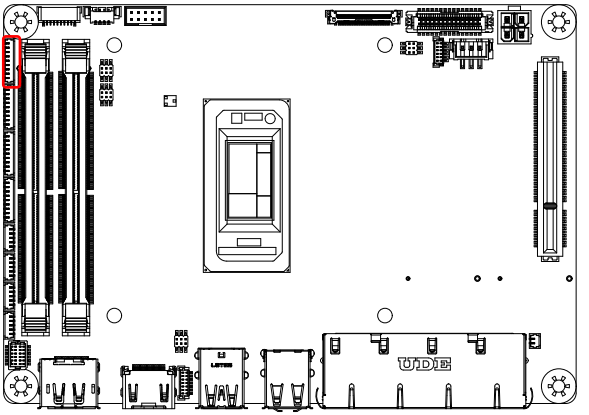
RS-232 (Default)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD1	IN	-
2	DSR1	IN	-
3	RX1	IN	-
4	RTS1	OUT	±9V
5	TX1	OUT	±9V
6	CTS1	IN	-
7	DTR1	OUT	±9V
8	RI1/ +5V/ +12V	IN/ PWR	+5V/+12V
9	GND	GND	GND

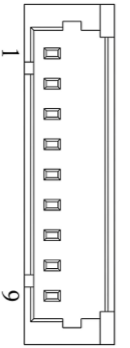
RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	-
6	NC		
7	RS422_RX-	IN	-
8	NC		
9	GND	GND	GND

RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	IN/OUT	±5V
2	NC		
3	RS485_D+	IN/OUT	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	GND	GND	GND

Note: COM Port RS-232/422/485 can be set by BIOS setting. Default is RS-232.
Note: Pin 8 function can be set by JP3. Default is RING.

2.4.13 COM Port 2 Header (CN14)





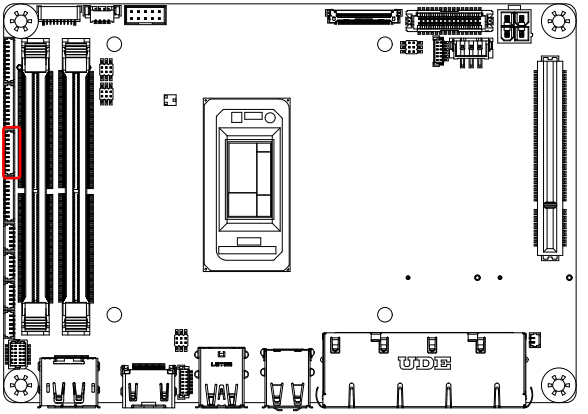
RS-232 (Default)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD2	IN	-
2	DSR2	IN	-
3	RX2	IN	-
4	RTS2	OUT	±9V
5	TX2	OUT	±9V
6	CTS2	IN	-
7	DTR2	OUT	±9V
8	RI2/ +5V/ +12V	IN/ PWR	+5V/+12V
9	GND	GND	GND

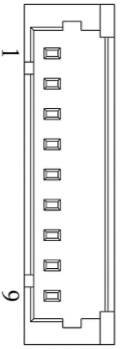
RS-422			
Pin	Pin Name	Signal Type	Signal Level
1	RS422_TX-	OUT	±5V
2	NC		
3	RS422_TX+	OUT	±5V
4	NC		
5	RS422_RX+	IN	-
6	NC		
7	RS422_RX-	IN	-
8	NC		
9	GND	GND	GND

RS-485			
Pin	Pin Name	Signal Type	Signal Level
1	RS485_D-	IN/OUT	±5V
2	NC		
3	RS485_D+	IN/OUT	±5V
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	GND	GND	GND

Note: COM Port RS-232/422/485 can be set by BIOS setting. Default is RS-232.
Note: Pin 8 function can be set by JP4. Default is RING.

2.4.14 COM Port 3 Header (CN15)

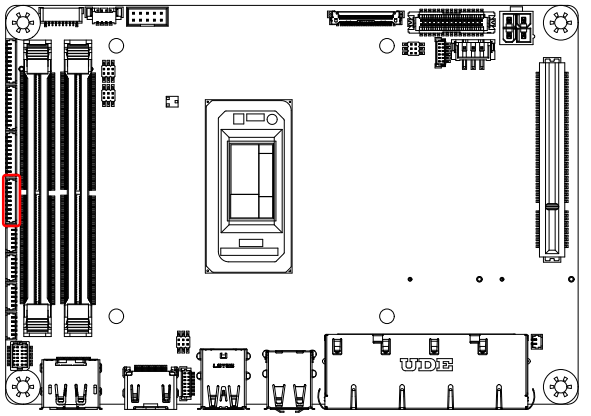


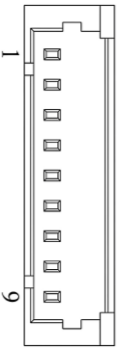


RS-232 (Default)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD3	IN	-
2	DSR3	IN	-
3	RX3	IN	-
4	RTS3	OUT	±9V
5	TX3	OUT	±9V
6	CTS3	IN	-
7	DTR3	OUT	±9V
8	RI3	IN	-

RS-232 (Default)			
Pin	Pin Name	Signal Type	Signal Level
9	GND	GND	GND

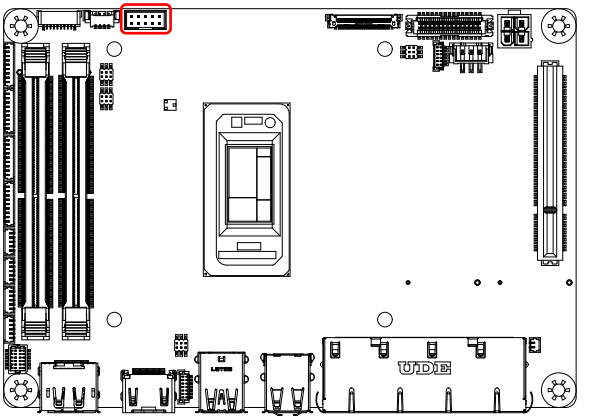
2.4.15 COM Port 4 Header (CN16)

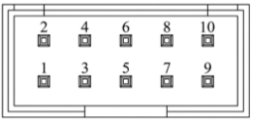




RS-232 (Default)			
Pin	Pin Name	Signal Type	Signal Level
1	DCD4	IN	-
2	DSR4	IN	-
3	RX4	IN	-
4	RTS4	OUT	±9V
5	TX4	OUT	±9V
6	CTS4	IN	-
7	DTR4	OUT	±9V
8	RI4	IN	-
9	GND	GND	GND

2.4.16 8-bit GPIO Header (CN17)

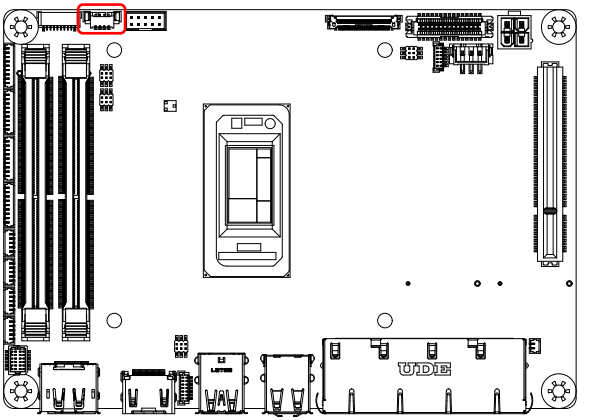


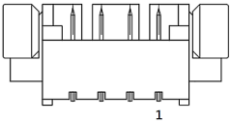


Pin	Pin Name	Signal Type	Signal Level
1	GPIO_0	IN/OUT	-
2	GPIO_1	IN/OUT	-
3	GPIO_2	IN/OUT	-
4	GPIO_3	IN/OUT	-
5	GPIO_4	IN/OUT	-
6	GPIO_5	IN/OUT	-
7	GPIO_6	IN/OUT	-
8	GPIO_7	IN/OUT	-
9	+V5S	PWR	+5V
10	GND	GND	GND

Note: The driving current of +V5S supports up to 0.5A.

2.4.17 4-pin Fan 1 Connector (CN18)

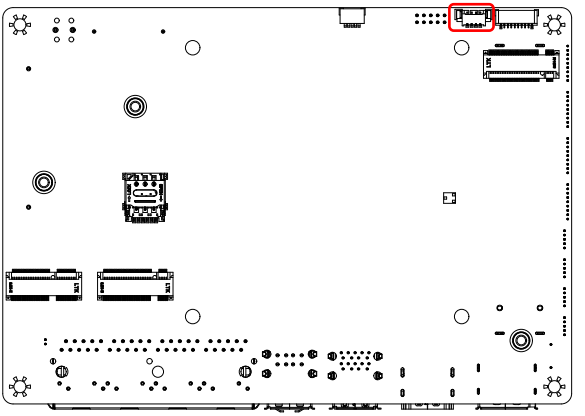


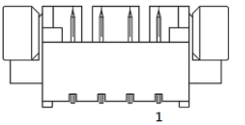


Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	-
4	FAN_CTL	OUT	-

Note: The driving current of FAN_POWER supports up to 1A.

2.4.18 4-pin Fan 2 Connector (CN19)

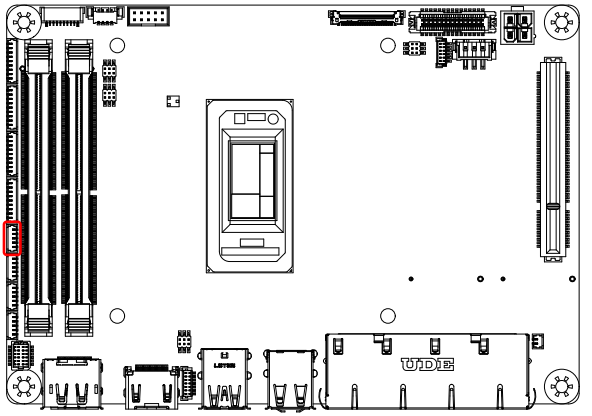


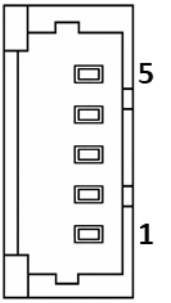


Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	FAN_POWER	PWR	+12V
3	FAN_TAC	IN	-
4	FAN_CTL	OUT	-

Note: The driving current of FAN_POWER supports up to 1A.

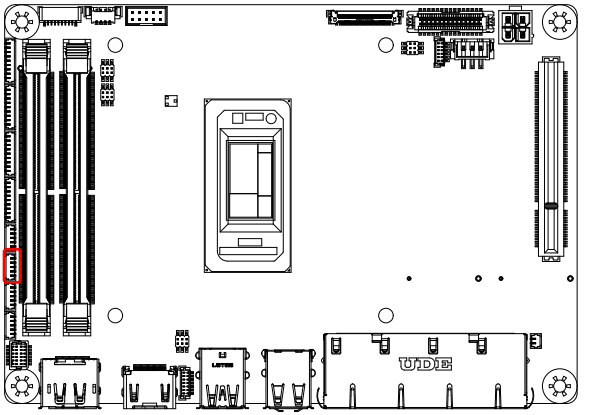
2.4.19 USB 2.0 Port 5 Header (CN20)

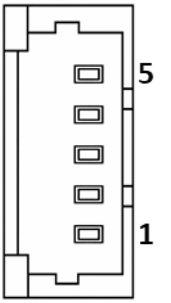




Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_5_DN	DIFF	-
3	USB2_5_DP	DIFF	-
4	GND	GND	GND
5	GND	GND	GND

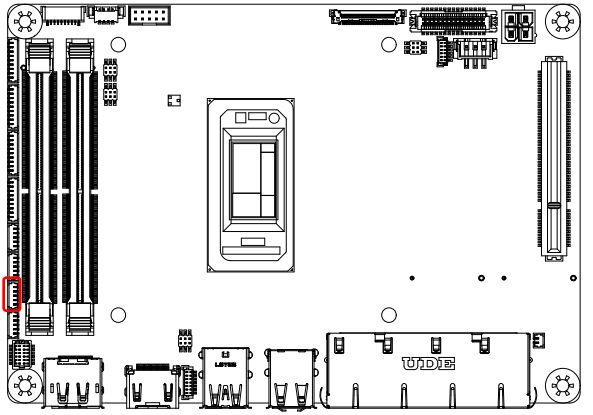
2.4.20 USB 2.0 Port 6 Header (CN21)

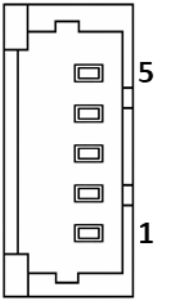




Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_6_DN	DIFF	-
3	USB2_6_DP	DIFF	-
4	GND	GND	GND
5	GND	GND	GND

2.4.21 USB 2.0 Port 7 Header (CN22)

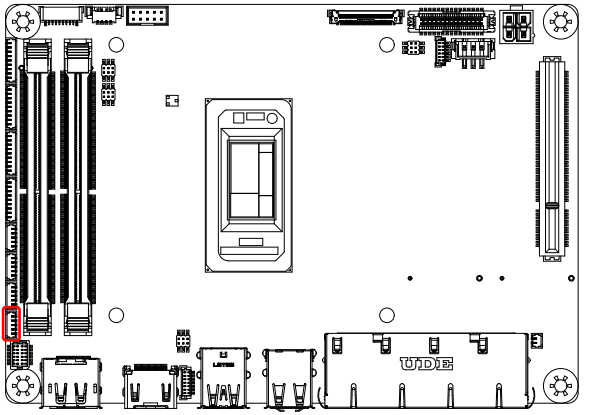


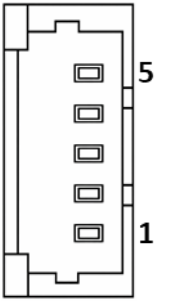


Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V

Pin	Pin Name	Signal Type	Signal Level
2	USB2_7_DN	DIFF	-
3	USB2_7_DP	DIFF	-
4	GND	GND	GND
5	GND	GND	GND

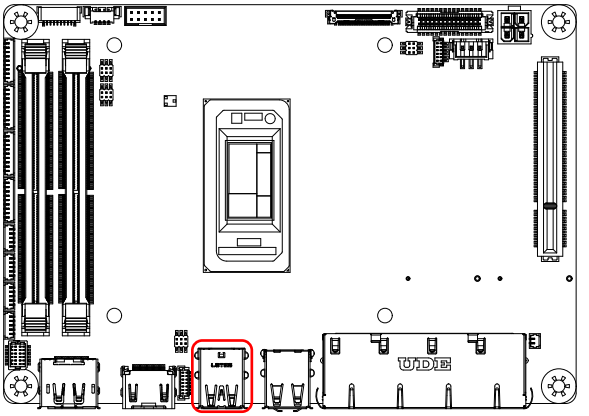
2.4.22 USB 2.0 Port 8 Header (CN23)

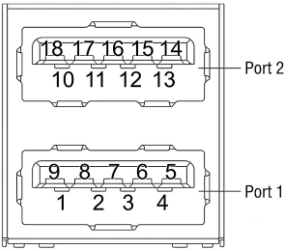




Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_8_DN	DIFF	-
3	USB2_8_DP	DIFF	-
4	GND	GND	GND
5	GND	GND	GND

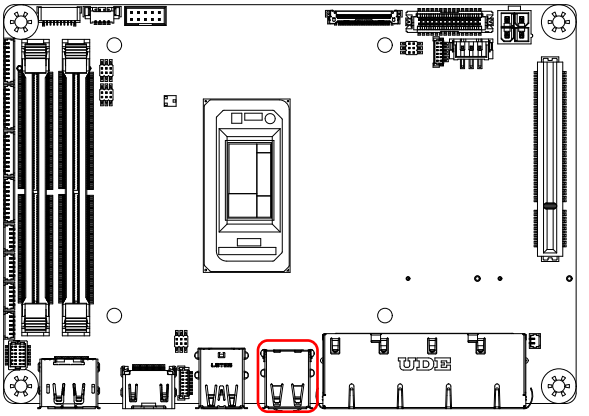
2.4.23 USB 3.2/USB 2.0 Port 1/Port 2 (CN24)

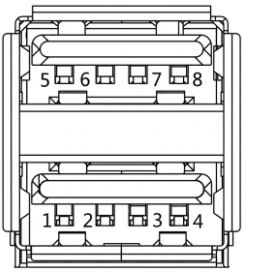




Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_1_DN	DIFF	-
3	USB2_1_DP	DIFF	-
4	GND	GND	GND
5	USB3_1_RXN	DIFF	-
6	USB3_1_RXP	DIFF	-
7	GND	GND	GND
8	USB3_1_TXN	DIFF	-
9	USB3_1_TXP	DIFF	-
10	+5VSB	PWR	+5V
11	USB2_2_DN	DIFF	-
12	USB2_2_DP	DIFF	-
13	GND	GND	GND
14	USB3_2_RXN	DIFF	-
15	USB3_2_RXP	DIFF	-
16	GND	GND	GND
17	USB3_2_TXN	DIFF	-
18	USB3_2_TXP	DIFF	-

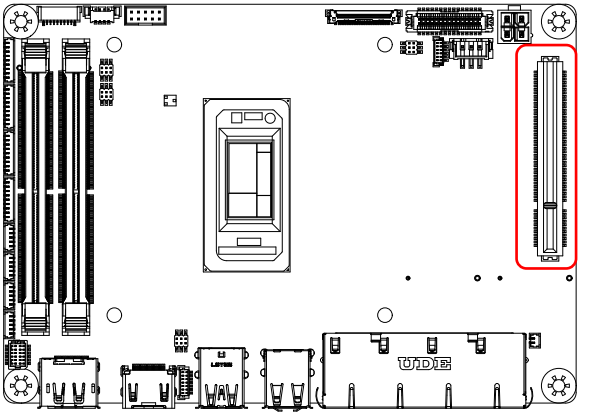
2.4.24 USB 2.0 Port 3/Port 4 (CN25)

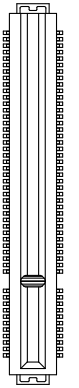




Pin	Pin Name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB2_3_DN	DIFF	-
3	USB2_3_DP	DIFF	-
4	GND	GND	GND
5	+5VSB	PWR	+5V
6	USB2_4_DN	DIFF	-
7	USB2_4_DP	DIFF	-
8	GND	GND	GND

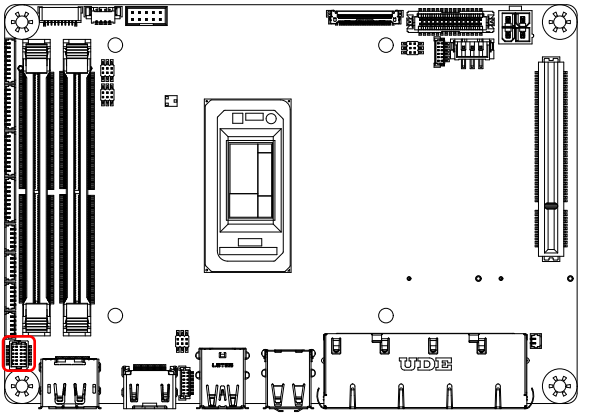
2.4.25 PCIe [x8] Slot (CN27)

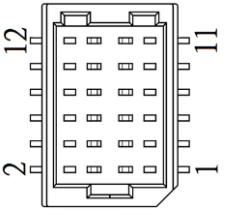




Note: Standard configuration. PCIe 5.0 [x8] Slot supported by Intel® Core™ Ultra 9 Processor 386H / Intel® Core™ Ultra 7 Processor 356H CPU SKUs only).

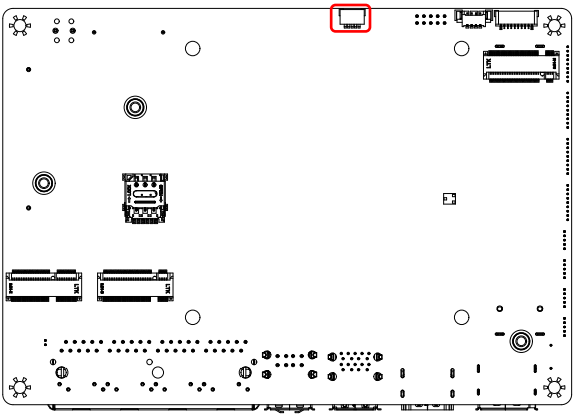
2.4.26 Audio I/O Port (CN28)

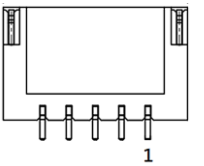




Pin	Pin Name	Signal Type	Signal Level
1	RIGHT_OUT	OUT	-
2	MIC_R	IN	-
3	LEFT_OUT	OUT	-
4	MIC_L	IN	-
5	JD_LOUT	IN	-
6	JD_MIC	IN	-
7	GND_AUDIO	GND	GND
8	GND_AUDIO	GND	GND
9	JD_LIN	IN	-
10	LINE_R_IN	IN	-
11	+VDD_AUDIO	PWR	+5V
12	LINE_L_IN	IN	-

2.4.27 I2C/SMBus Connector (CN29)

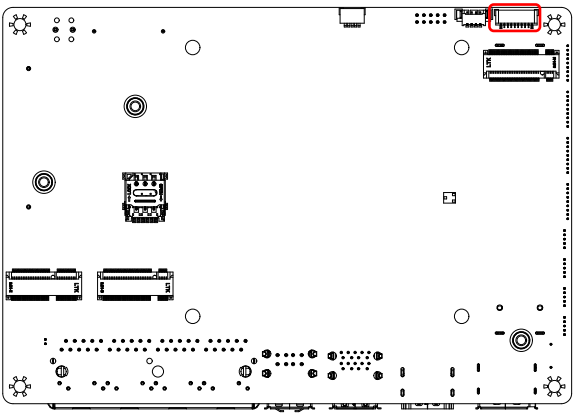


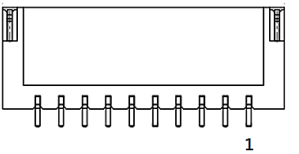


Pin	Pin Name	Signal Type	Signal Level
1	+V3P3A/+V3P3S	PWR	+3.3V
2	SMB_CLK/ I2C_CLK/TIME_SYNC0	OUT	+3.3V
3	SMB_DAT/ I2C_DAT/TIME_SYNC1	IN/OUT	+3.3V
4	SMB_ALERT/ INT_SERIRQ/LAN_SDP	IN	+3.3V
5	GND	GND	GND

Note: Default function is I2C.

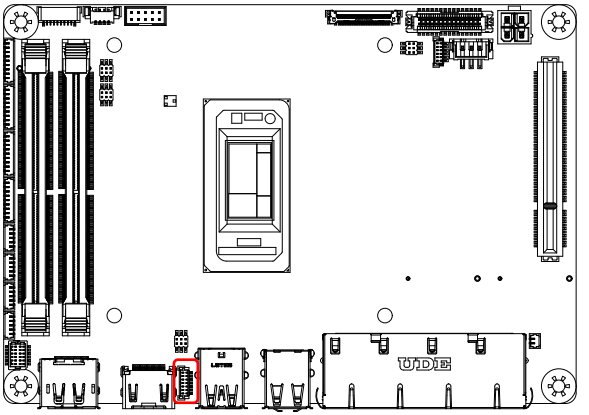
2.4.28 eSPI Debug Header (CN30)

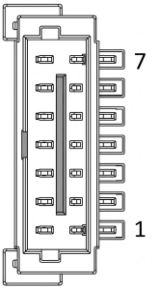




Pin	Pin Name	Signal Type	Signal Level
1	ESPI_IO0	Signal	+1.8V
2	ESPI_IO1	Signal	+1.8V
3	ESPI_IO2	Signal	+1.8V
4	ESPI_IO3	Signal	+1.8V
5	+V3P3S	PWR	+3.3V
6	ESPI_CS	Signal	
7	ESPI_RESET#	Signal	+1.8V
8	GND	GND	
9	ESPI_CLK	Signal	+1.8V
10	+V3P3A	PWR	+3.3V

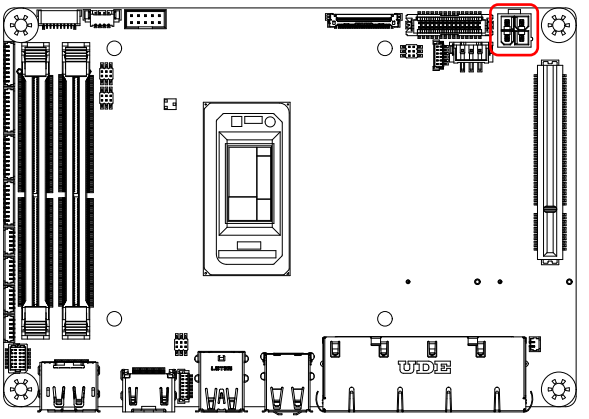
2.4.29 SPI Flash Programming Port (CN31)

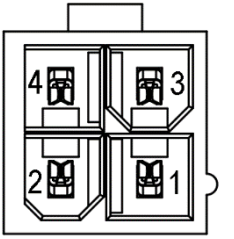




Pin	Pin Name	Signal Type	Signal Level
1	SPI_MISO	OUT	-
2	GND	GND	GND
3	SPI_CLK	IN	-
4	+V1P8A_SPI	PWR	+1.8V
5	SPI_MOSI	IN	-
6	SPI_CS	IN	-
7	NC	-	-

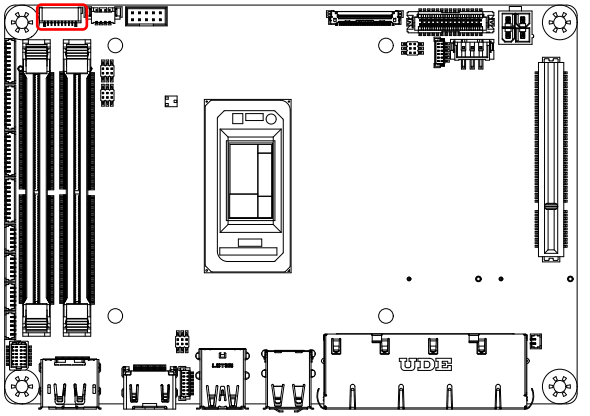
2.4.30 External Power Input (CN33)

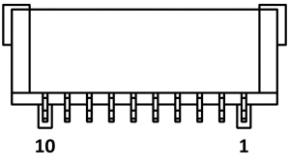




Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	GND	GND	
3	+VIN	PWR	+12V or +9~+24V
4	+VIN	PWR	+12V or +9~+24V

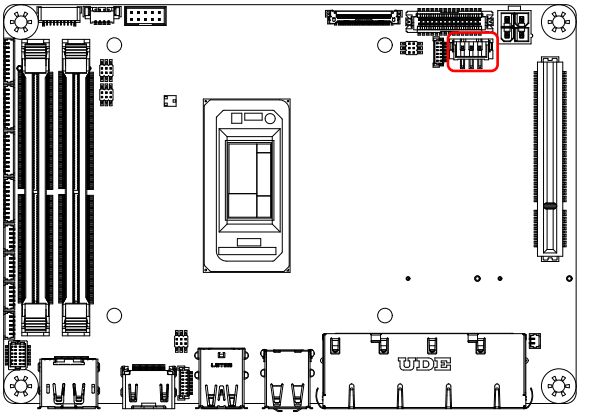
2.4.31 Front Panel (CN34)

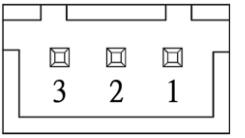




Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	GND
2	EXT_PWRBTN#	IN	-
3	SSD_LED-	OUT	-
4	SSD_LED+	OUT	-
5	BUZZER-	OUT	-
6	BUZZER+	OUT	-
7	GND	GND	GND
8	PWR_LED+	OUT	-
9	GND	GND	GND
10	HWRST#	IN	-

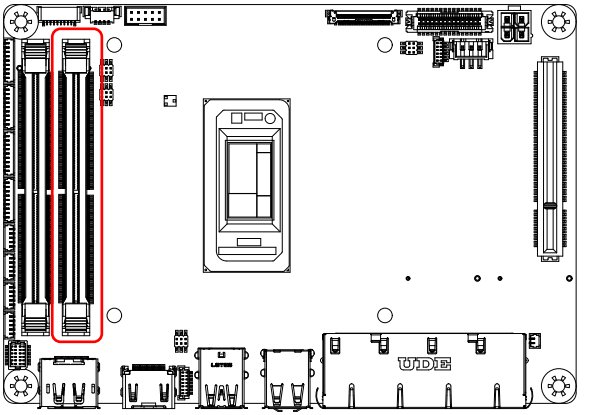
2.4.32 External +5VSB Input (CN35)





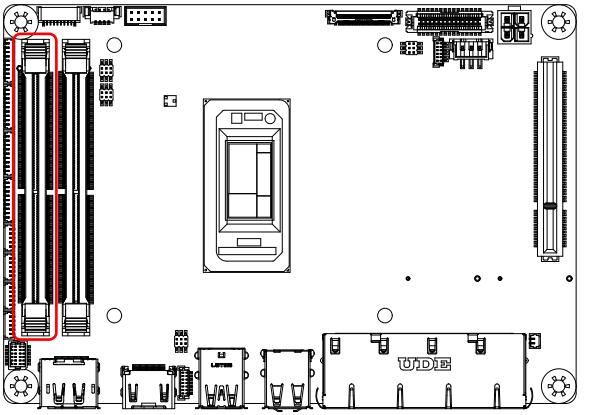
Pin	Pin Name	Signal Type	Signal Level
1	PS_ON#	OUT	+5V
2	GND	GND	GND
3	+5VSB	PWR	+5V

2.4.33 DDR5 SODIMM Channel 1 (JDDR1)



Standard specifications.

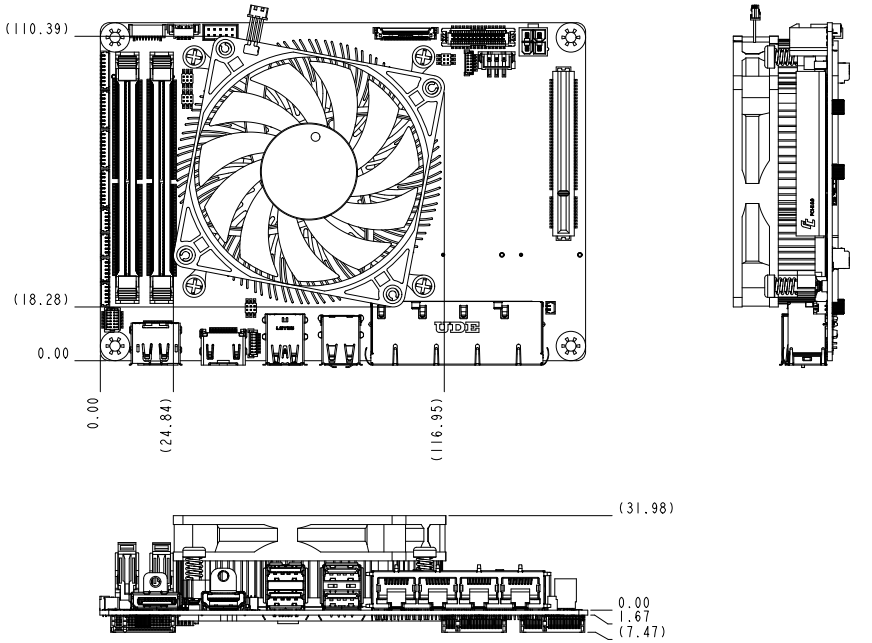
2.4.34 DDR5 SODIMM Channel 2 (JDDR2)



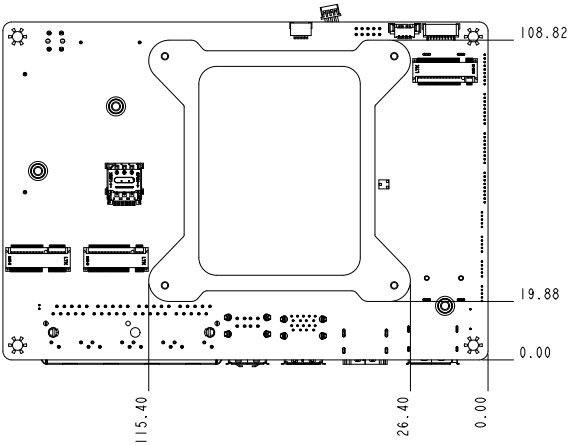
Standard specifications.

2.5 Thermal Solution Assembly

Top View

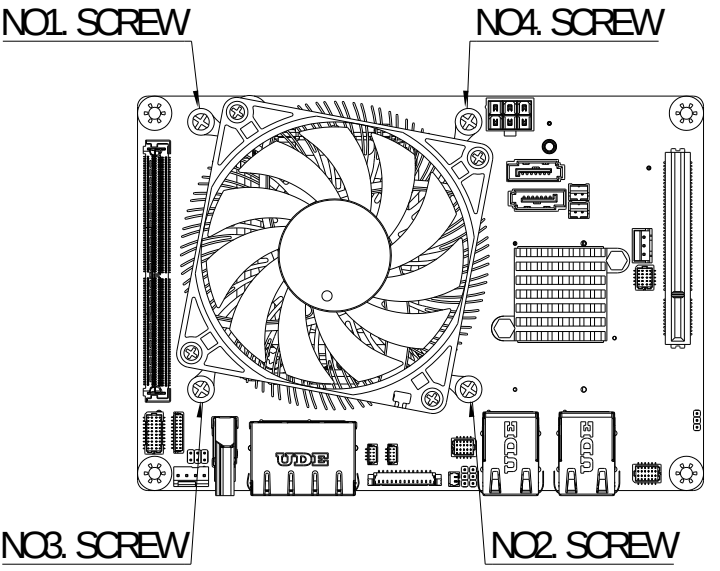


Bottom View

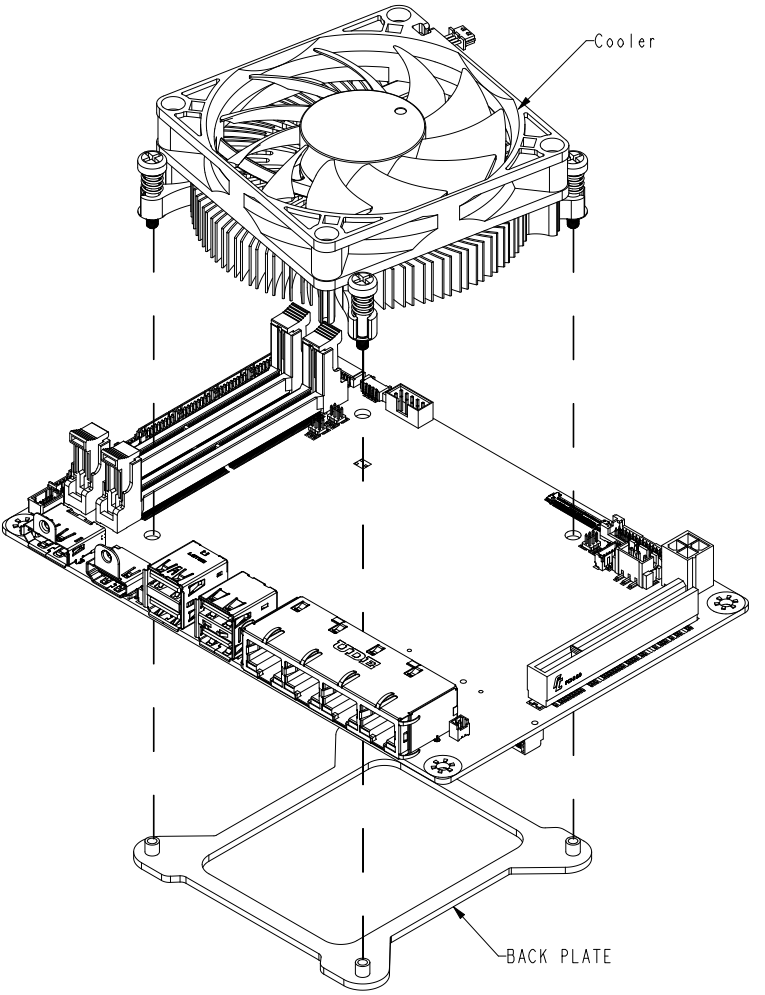


Installation Instructions

1. Do not apply any thermal grease to the cooler - the required amount has already been applied.
2. The back plate should be pre-attached to the underside of the motherboard. Remember to peel off the insulation slice liner prior to installation.
3. Place the cooler directly on top of the CPU so that the cooler screws are aligned with the mounting holes on the back plate.
4. Make sure screwdriver torque setting is no more than 5.0 kgf-cm (4.3 lbf-in) and keep heatsink screws direction vertical.
5. Screw in two diagonal screws (i.e. the #1 and #2 screws) until they are just snug (do not fully tighten), then do the same with the remaining two diagonal screws.
6. Finish by fully tightening all four screws.
7. Connect the fan cable to the CPU fan connector on the motherboard.



Part No: EPIC-PTH9-FAN01



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The EPIC-PTH9 CMOS memory has an integral lithium battery backup for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Access and configure advanced processor options and features

System I/O – Host bridge parameters

Security – The setup administrator password can be set here

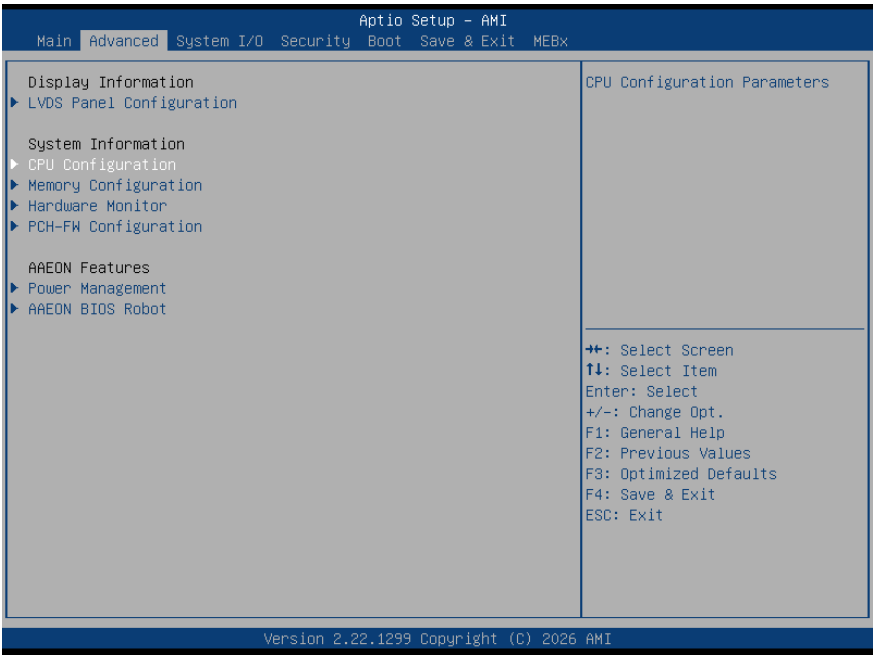
Boot – Set boot options including boot priority and Quiet Boot option

Save & Exit – Save your changes and exit the program

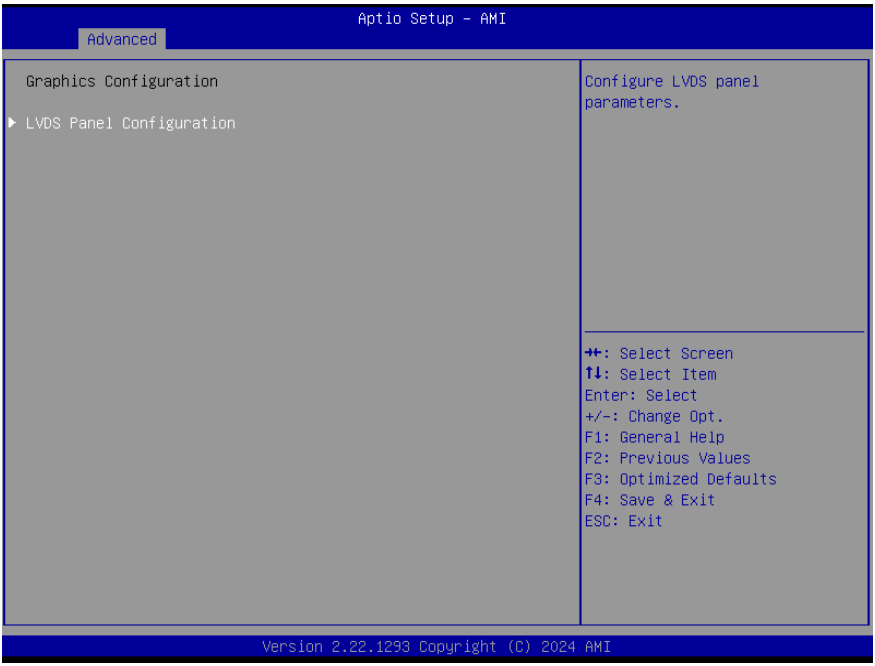
MEBx – Enables/disable MEBx option

3.3 Setup Submenu: Main

3.4 Setup Submenu: Advanced



3.4.1 Graphics Configuration

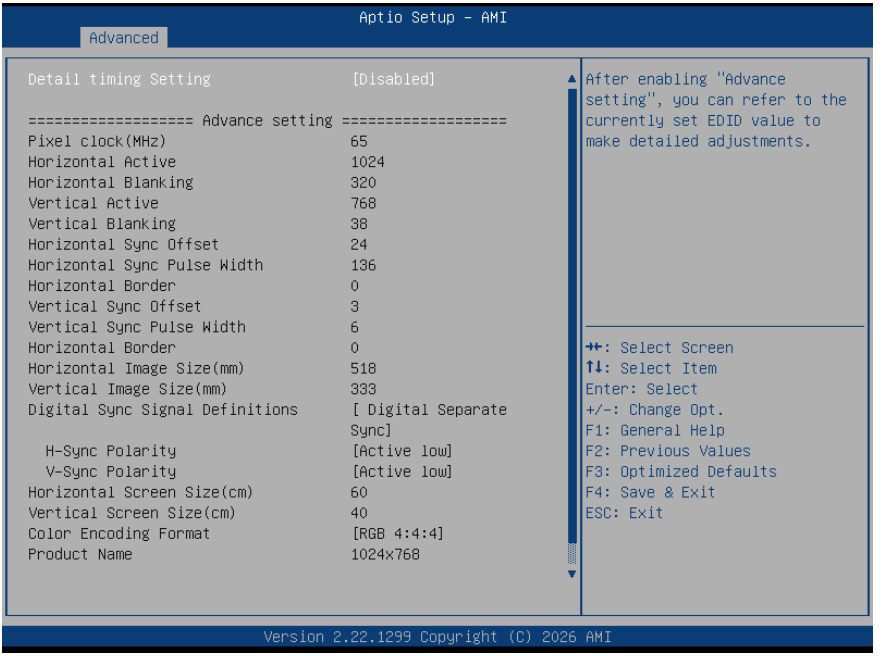


3.4.1.1 LVDS_0 Configuration

Options Summary		
LVDS	Disabled	
	Enabled	Optimal Default, Failsafe Default
Disabled – PTN3460 chip is not processed. Enabled – PTN3460 chip is processed.		
LVDS Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	

Options Summary		
Select Panel Type.		
Color Depth and data format	VESA 24bit	
	JEIDA 24bit	
	VESA/JEIDA 18bit	Optimal Default, Failsafe Default
Select the color depth and data packing format. Note: To use 36-bit or 48-bit mode, set LVDS Mode to Dual Mode.		
LVDS Mode	Signal Mode	Optimal Default, Failsafe Default
	Dual Mode	
Single / Dual Mode selection.		
Backlight Mode	External	Optimal Default, Failsafe Default
	Internal	
Select the backlight control method. Internal – Controlled by the driver; supports Windows brightness adjustment. External – Controlled through EAPI.		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type.		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control signal type.		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select backlight control level.		

3.4.1.2 Detail Timing Setting

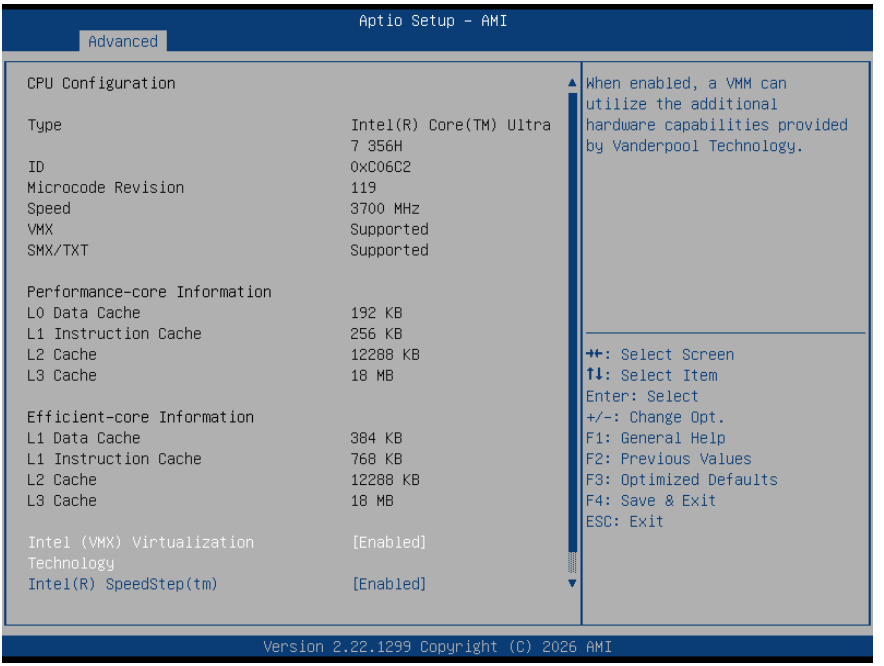


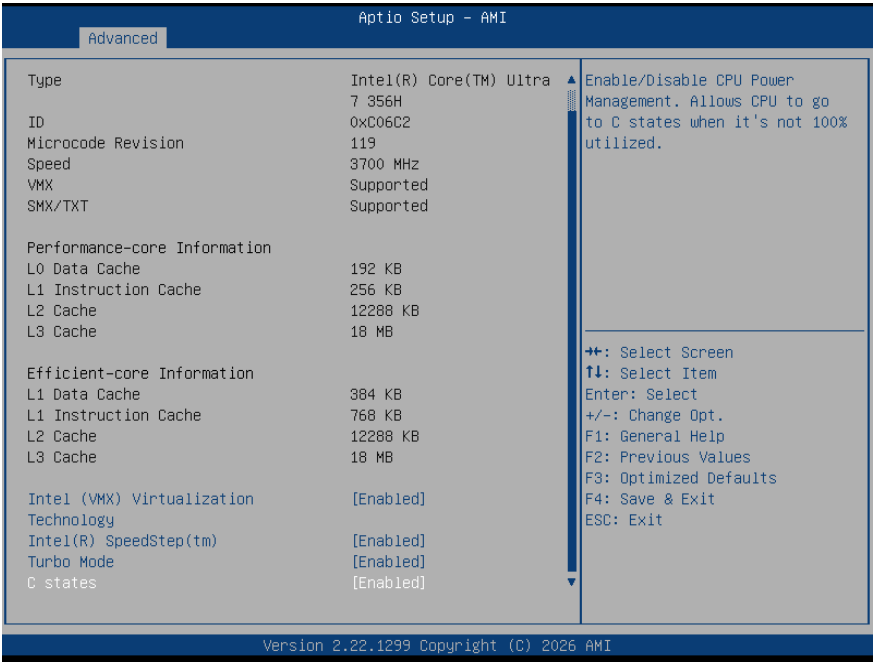
Options Summary		
Detail Timing Setting	Disabled	Optimal Default, Failsafe Default
	Enabled	
After enabling Advanced Settings, you can refer to the current EDID values to make detailed timing adjustments.		

3.4.1.3 PTN3460 Advance Setting

Options Summary		
PTN3460 Advance Setting	Disabled	Optimal Default, Failsafe Default
	Enabled	
Detailed settings for PTN3460.		

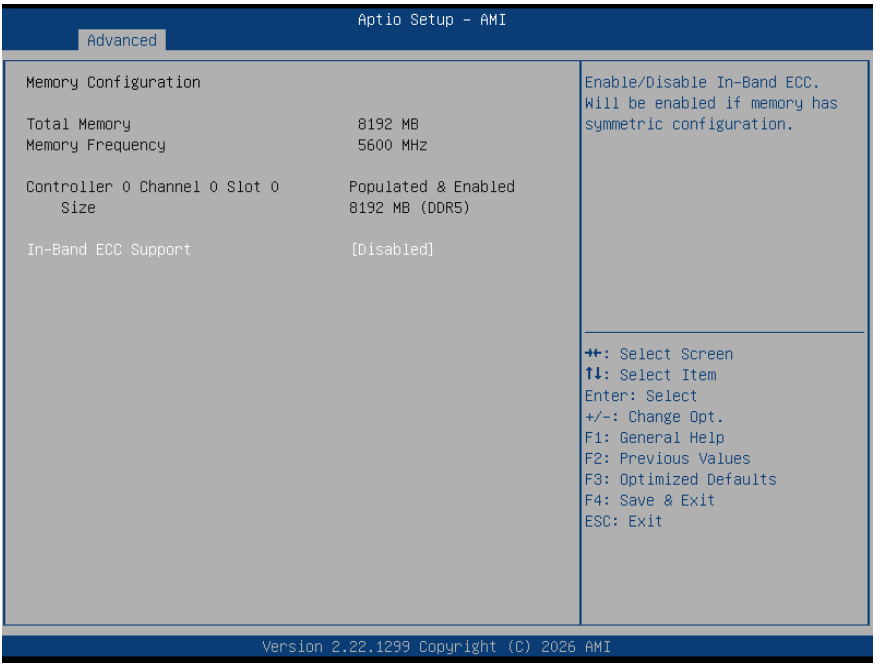
3.4.2 CPU Configuration





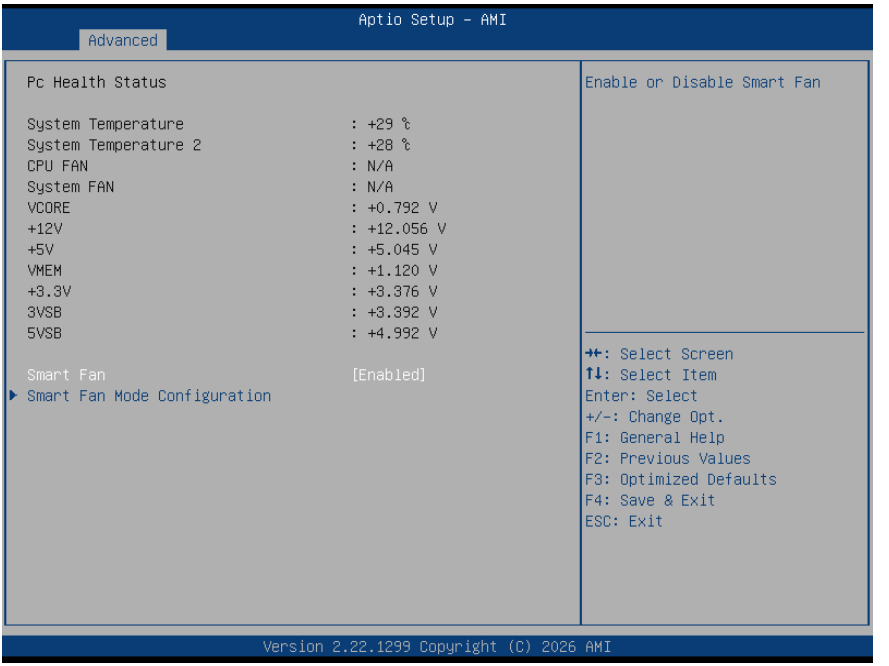
Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel® SpeedStep™	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable processor Turbo Mode (this also requires EMTTM to be enabled). AUTO means enabled.		
C states	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.		

3.4.3 Memory Configuration



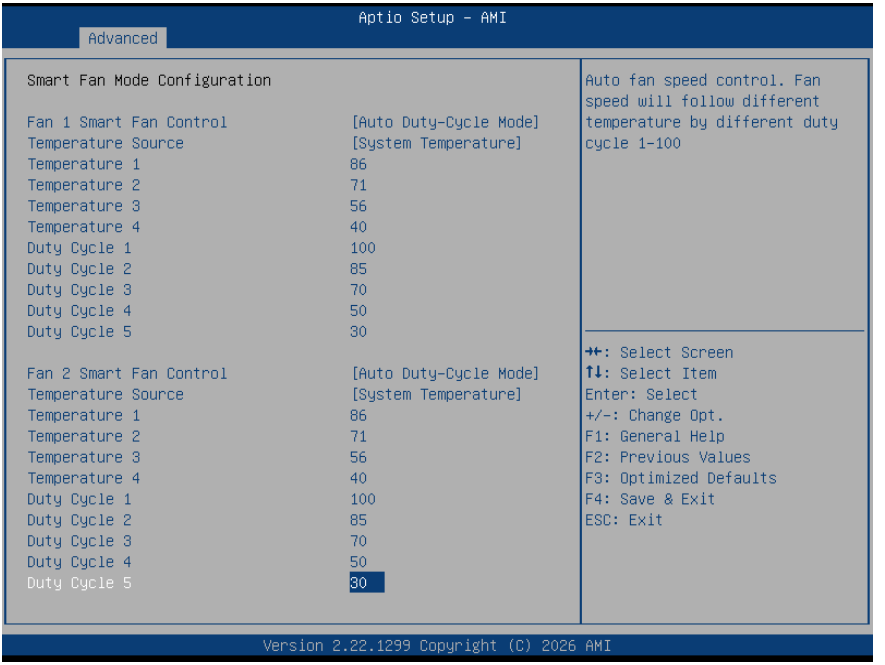
Options Summary		
In-Band ECC Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable In-Band ECC. Will be enabled if memory has symmetric configuration.		

3.4.4 Hardware Monitor



Options Summary		
Smart Fan	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables Smart Fan.		

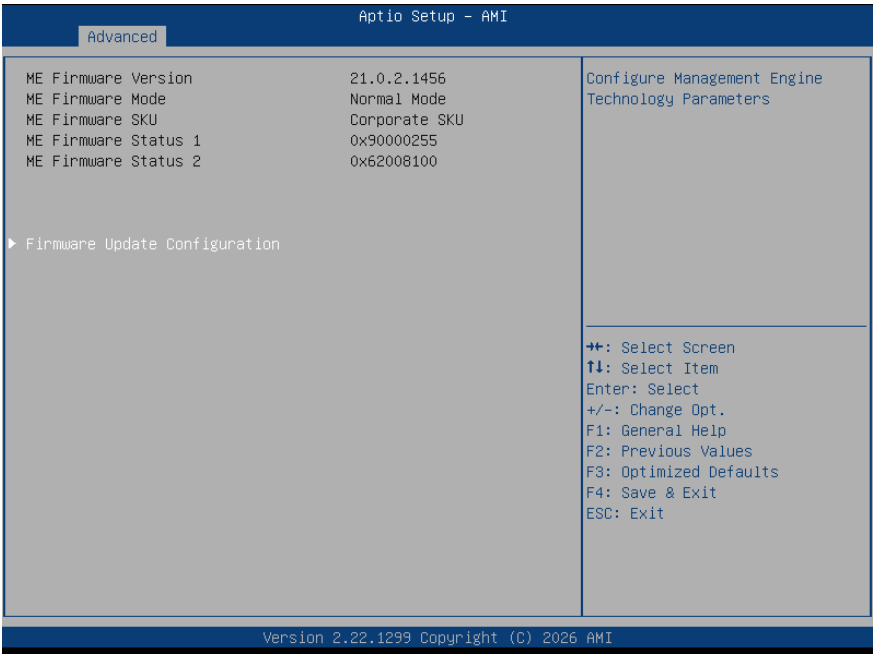
3.4.4.1 Smart Fan Mode Configuration



Options Summary		
Fan 1 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select.		
Temperature Source	System Temperature 2	
	System Temperature	Optimal Default, Failsafe Default
Select the monitored temperature source for this fan.		
Temperature 1	86	
Duty Cycle 1	100	
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.		
Fan 2 Smart Fan Control	Manual Duty Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select.		
Temperature Source	System Temperature 2	
	System Temperature	Optimal Default, Failsafe Default
Select the monitored temperature source for this fan.		

Options Summary		
Temperature 1	86	
Duty Cycle 1	100	
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100.		

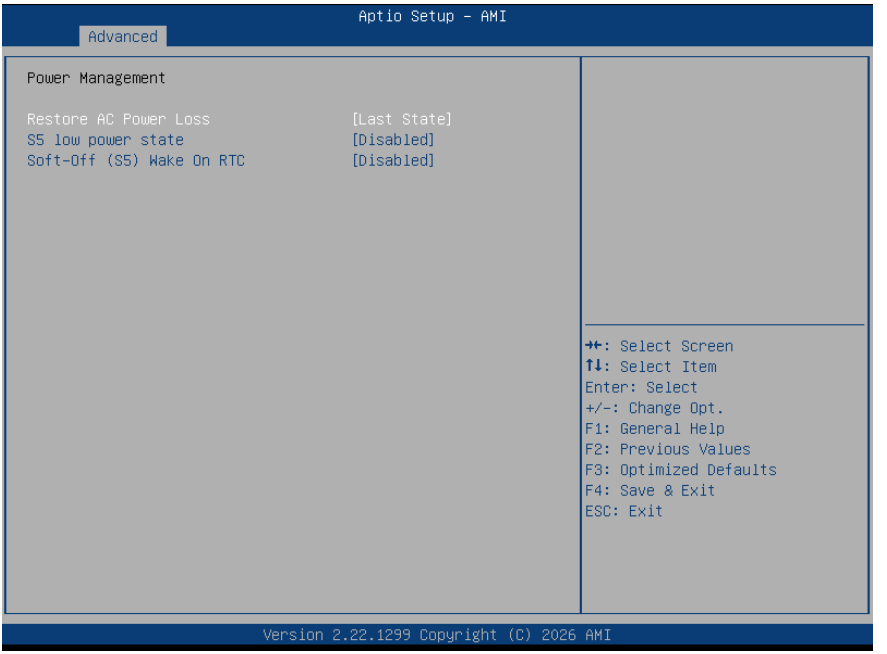
3.4.5 PCH-FW Configuration



3.4.6 Firmware Update Configuration

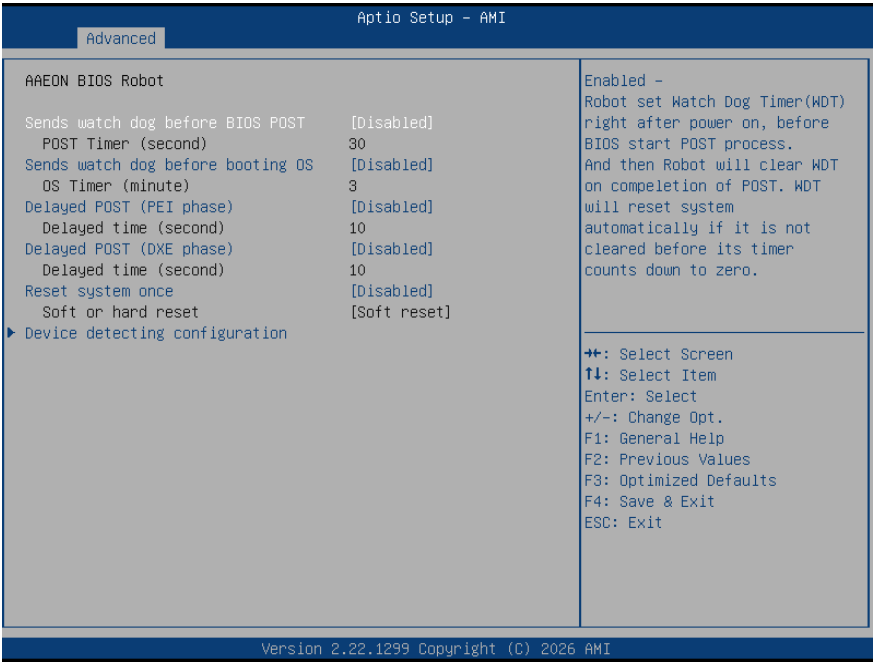
Options Summary		
Me FW Image Re-Flash	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable/Disable Me FW Image Re-Flash function.		
FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable ME FW Update function.		

3.4.7 Power Management



Options Summary		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
Select power state when power is re-applied after a power failure.		
S5 low power state	Disabled	Optimal Default, Failsafe Default
	Enabled	
Configure power mode for power saving function.		
Soft-Off (S5) Wake On RTC	Disable	Optimal Default, Failsafe Default
	By Date	
	By Weekday	
	Bypass	
By Date: System will wake on the with hr::min::sec specified. By Weekday: System will wake on the enabled weekday with hr::min::sec specified. Bypass: BIOS will not control RTC wake function.		

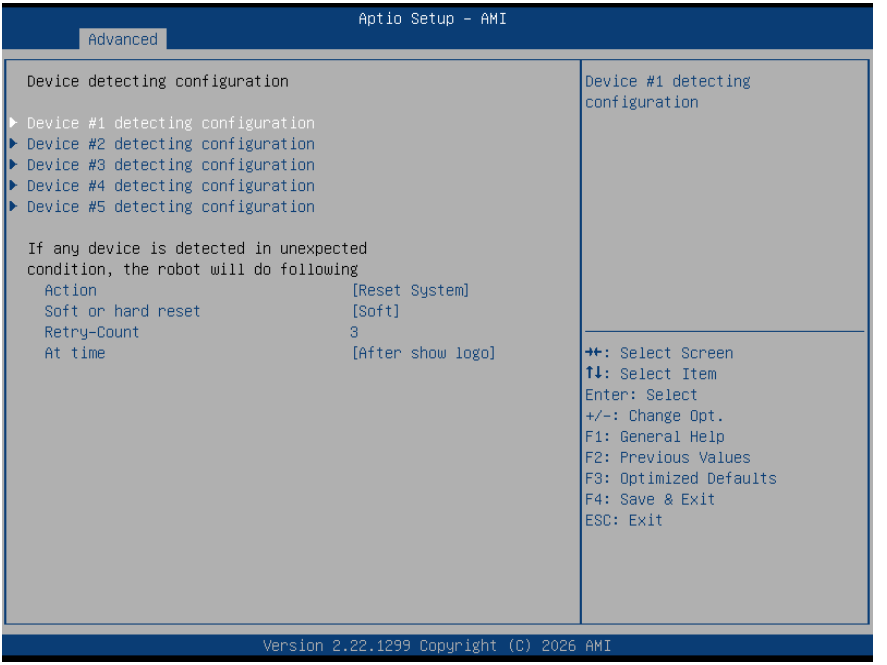
3.4.8 AAEON BIOS Robot



Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled – Robot sets the Watchdog Timer (WDT) immediately after power-on, before BIOS starts the POST process, and clears it upon POST completion. If the WDT is not cleared before the timer expires, the system will automatically reset.		
POST Timer (second)	30	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for POST. **WARNING**: Do not set to a value equal or shorter than normal POST time, otherwise system may never complete POST unless clearing BIOS settings. More than 2x normal POST time is suggested.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot set Watch Dog Timer (WDT) after POST completion, before BIOS transfer control to OS. **WARNING**: Before enabling this function, a program in OS must be in responsible for clearing WDT. Also, this function should be disabled if OS is going to update itself.		
OS Timer (minute)	3	Optimal Default, Failsafe Default
Timer count set to Watch Dog Timer for OS loading.		

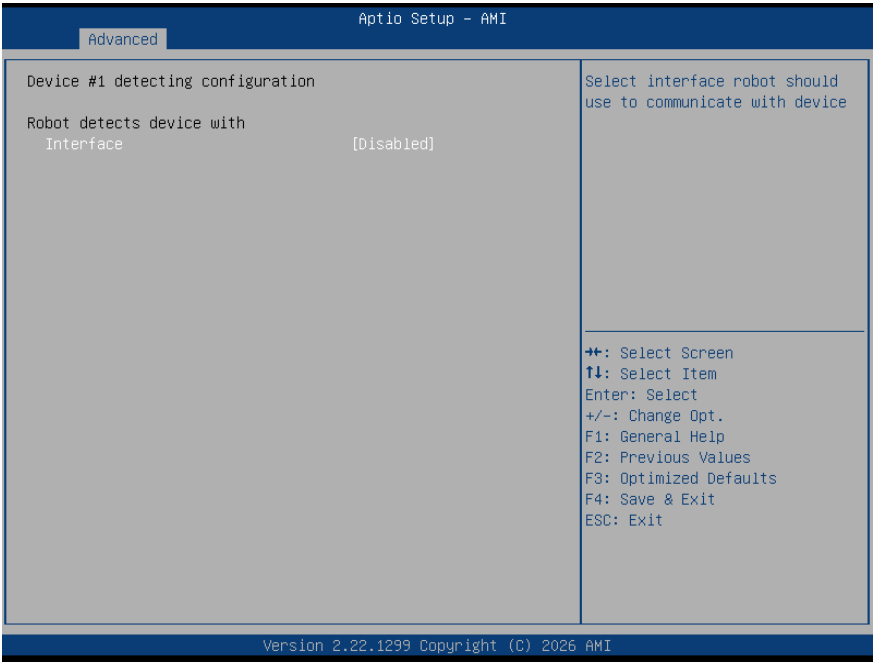
Options Summary		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS from starting POST, right after power on. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this before 'Sends watch dog'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot holds BIOS before POST completion. This allows BIOS POST to start with stable power or start after system is physically warmed-up. Note: Robot does this after 'Sends watch dog before BIOS POST'.		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enabled - Robot resets system for one time on each boot. This will send a soft or hard reset to onboard devices, thus puts devices to more stable state.		
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset	
Select reset type robot should send on each boot.		

3.4.9 Device Detecting Configuration



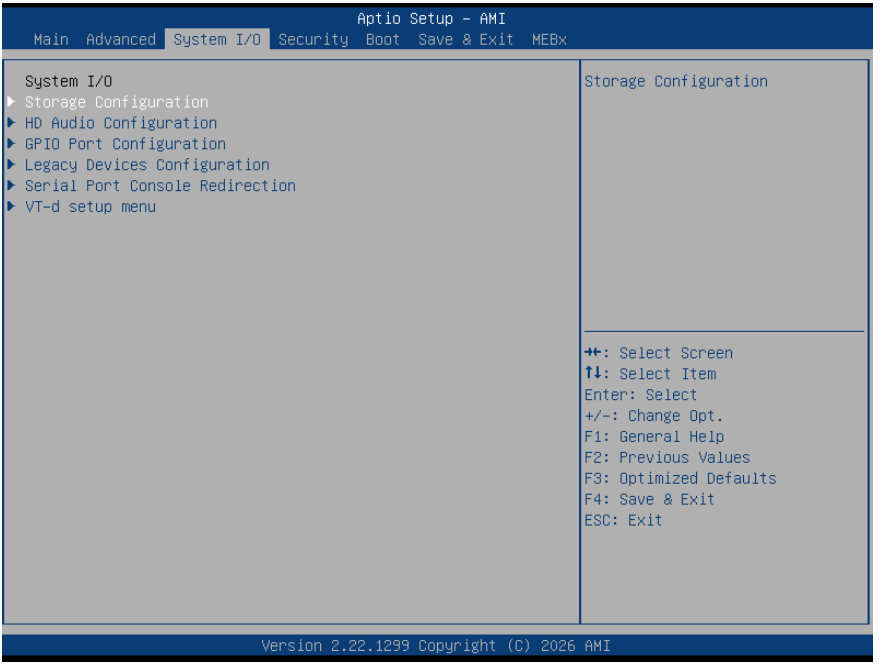
Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should perform.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	30	Optimal Default, Failsafe Default
Fill in the retry counter. Robot will reset the system up to the specified number of times, then allow the system to continue POST.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select the robot action time: After Show Logo – Robot performs the action after the logo is displayed. System devices are mostly initialized and ready. Before Show Logo – Robot performs the action before the logo is displayed, but some devices may not be ready.		

3.4.9.1 Device # Detecting Configuration

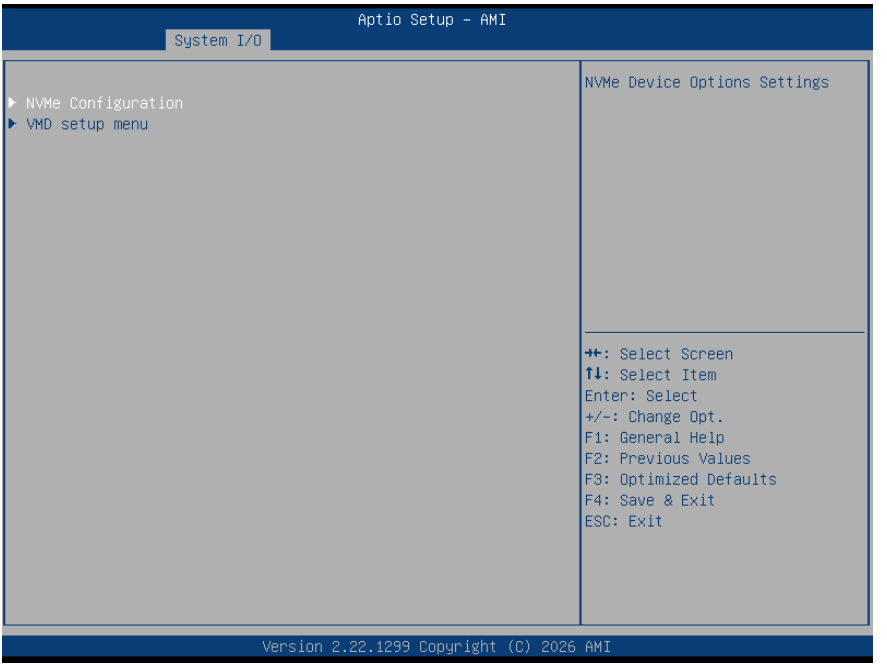


Options Summary		
Interface	Disable	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

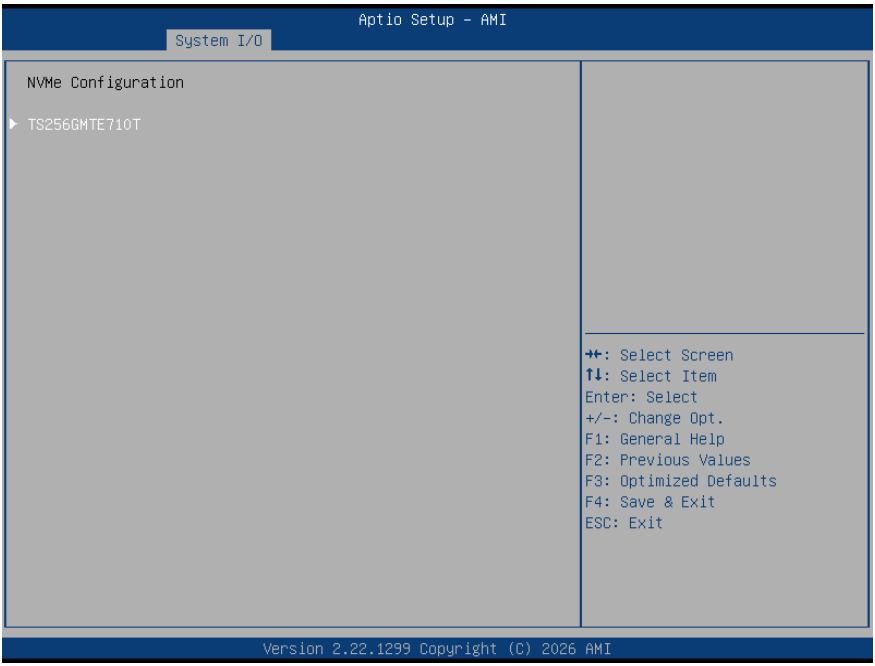
3.5 Setup Submenu: System I/O

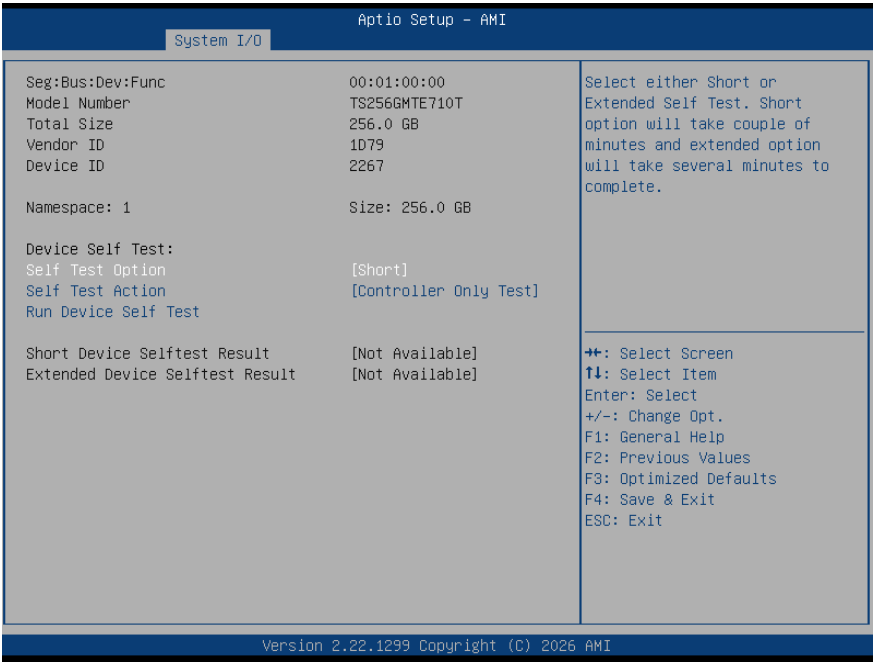


3.5.1 Storage Configuration



3.5.2 NVMe Configuration



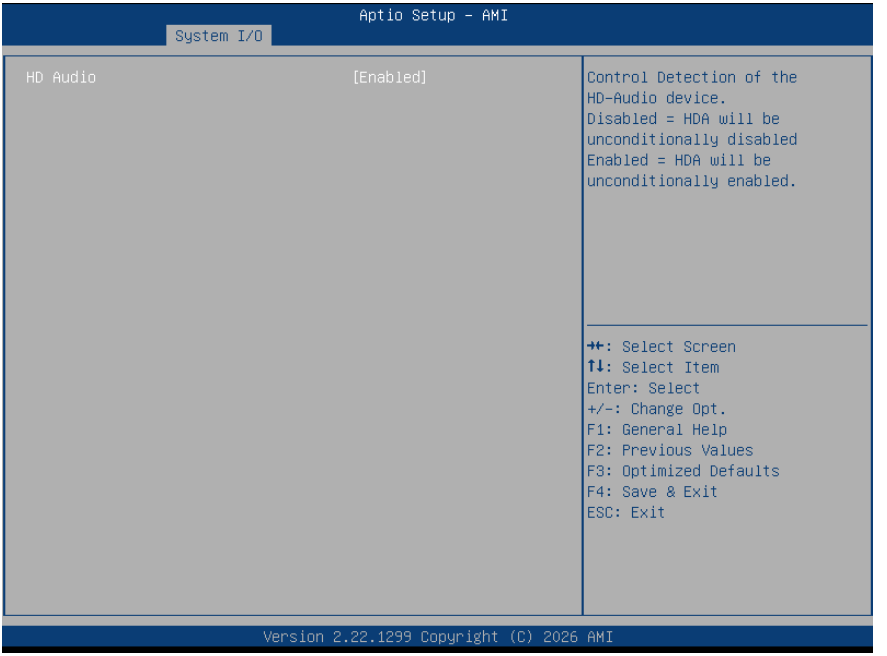


Options Summary		
Self Test Option	Short	Optimal Default, Failsafe Default
	Extended	
Select either Short or Extended Self Test. Short option will take couple of minutes and extended option will take several minutes to complete.		
Self Test Action	Controller Only Test	Optimal Default, Failsafe Default
	Controller and NameSpace Test	
Select either to test Controller alone or Controller and NameSpace. Selecting Controller and NameSpace option will take lot longer to complete the test.		
Run Device Self Test	N/A	N/A
Perform device self test for the corresponding option and action selected by user. Pressing 'Esc' key will abort the test. Result shown below is the recent result logged in the device.		

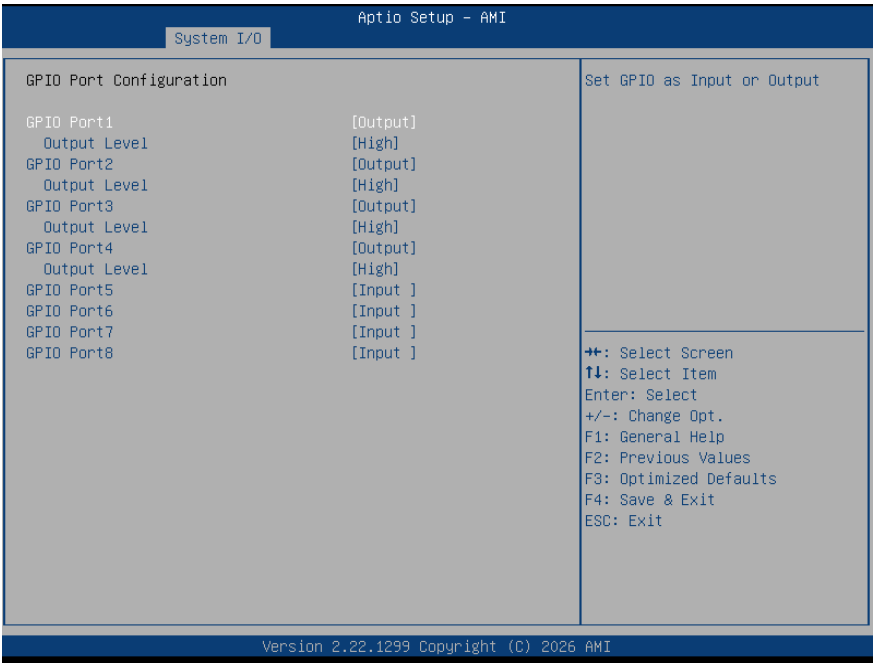
3.5.3 VMD Setup Menu

Options Summary		
Enable VMD Controller	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable VMD Controller.		

3.5.4 HD Audio Configuration

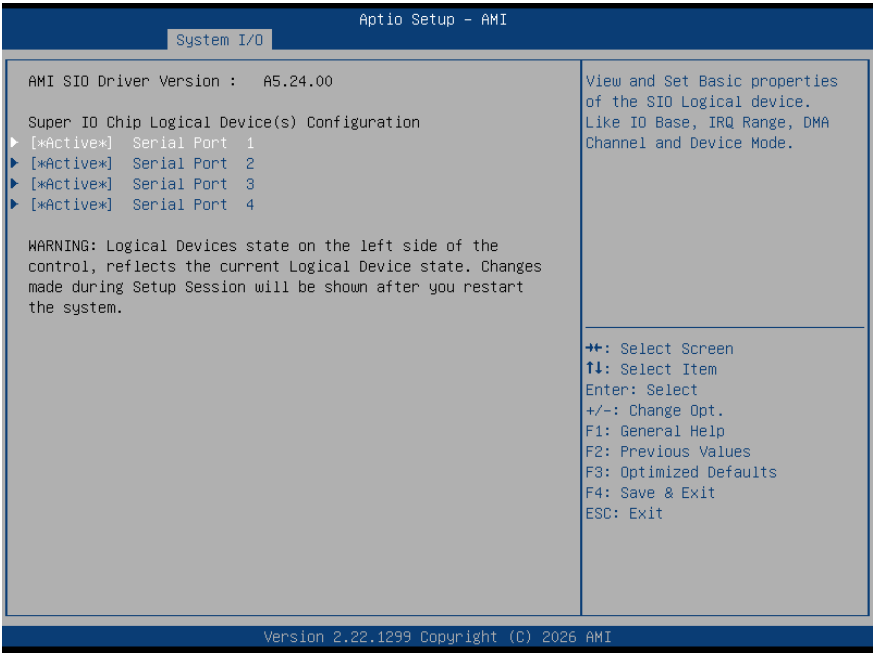


3.5.5 GPIO Port Configuration

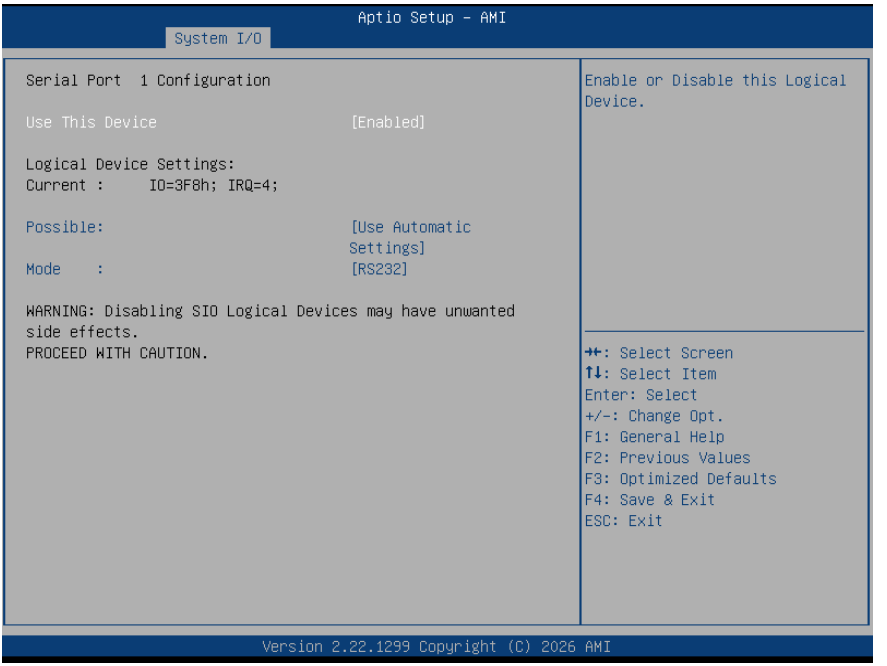


Options Summary		
GPIO Port*	Output	
	Input	
Set GPIO as Input or Output.		
Output Level	High	
	Low	
Set output level when GPIO pin is output.		

3.5.6 Legacy Devices Configuration

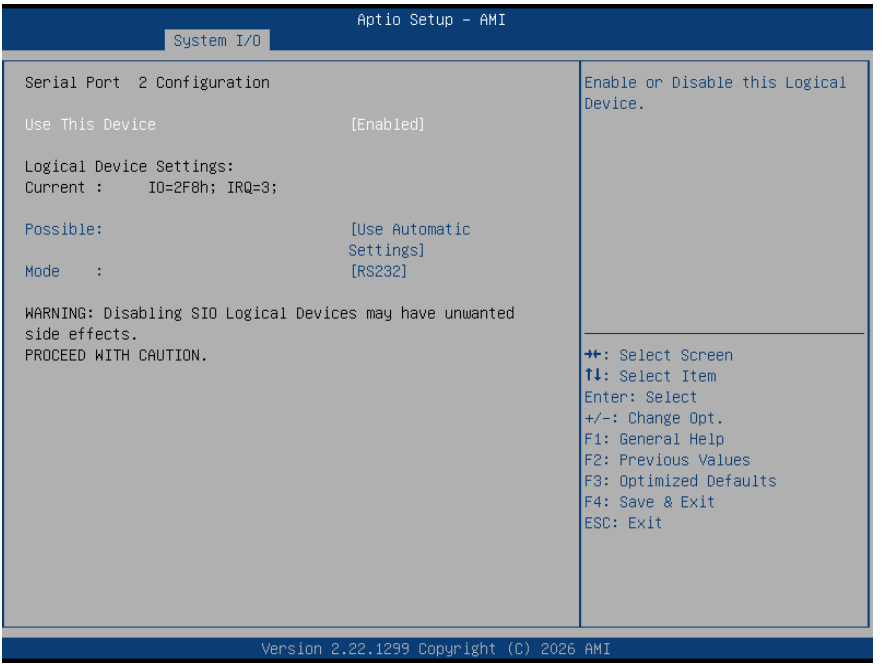


3.5.6.1 Serial Port 1 Configuration



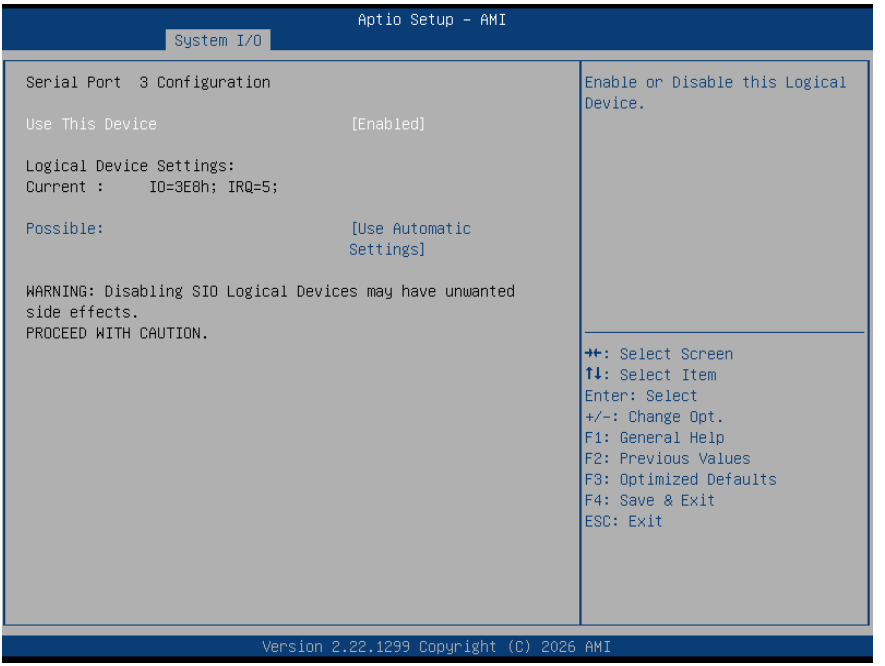
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.5.6.2 Serial Port 2 Configuration



Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection.		

3.5.6.3 Serial Port 3 Configuration

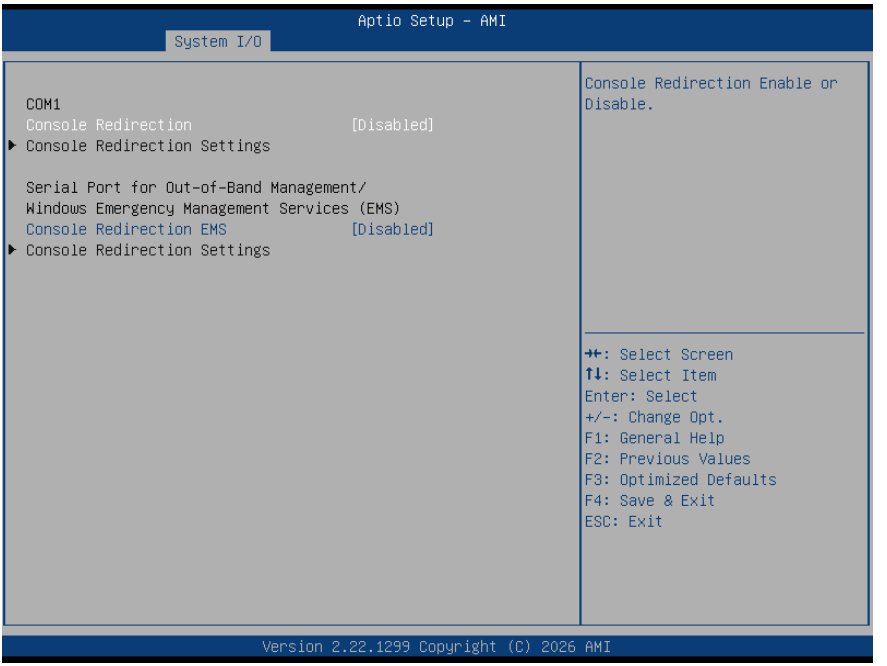


Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8h; IRQ=5	
	IO=2E8h; IRQ=7	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.5.6.4 Serial Port 4 Configuration

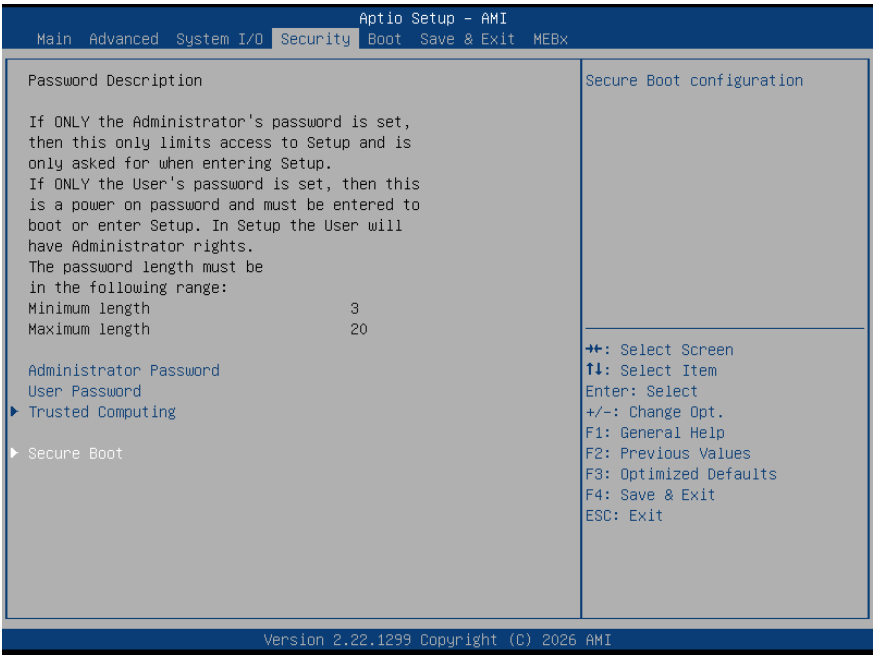
Options Summary		
Use This Device	Disable	
	Enable	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8h; IRQ=7	
	IO=3E8h; IRQ=5	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.5.7 Serial Port Console Redirection



Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Console Redirection EMS.		

3.6 Setup Submenu: Security



Change User/Administrator Password

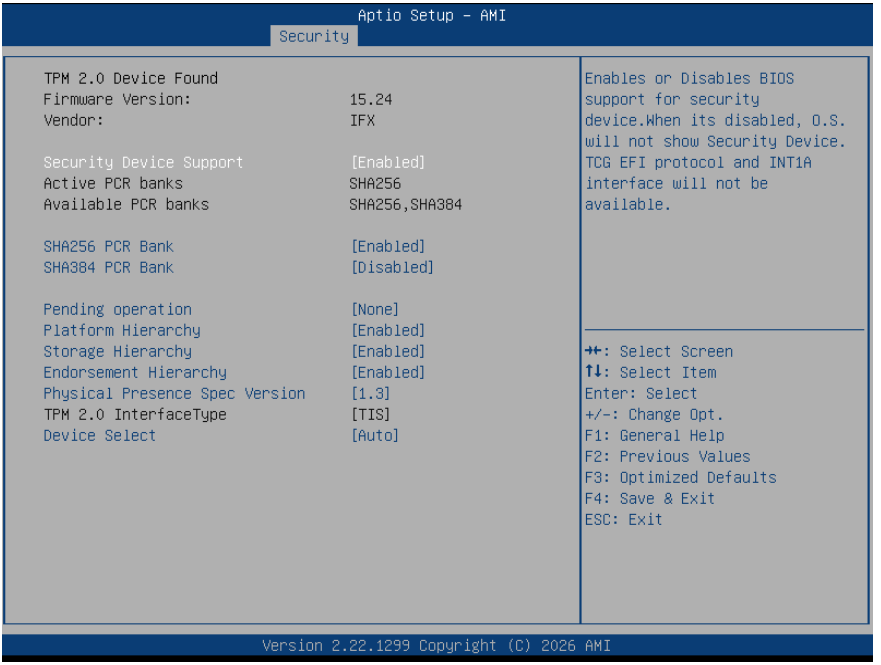
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Trusted Computing



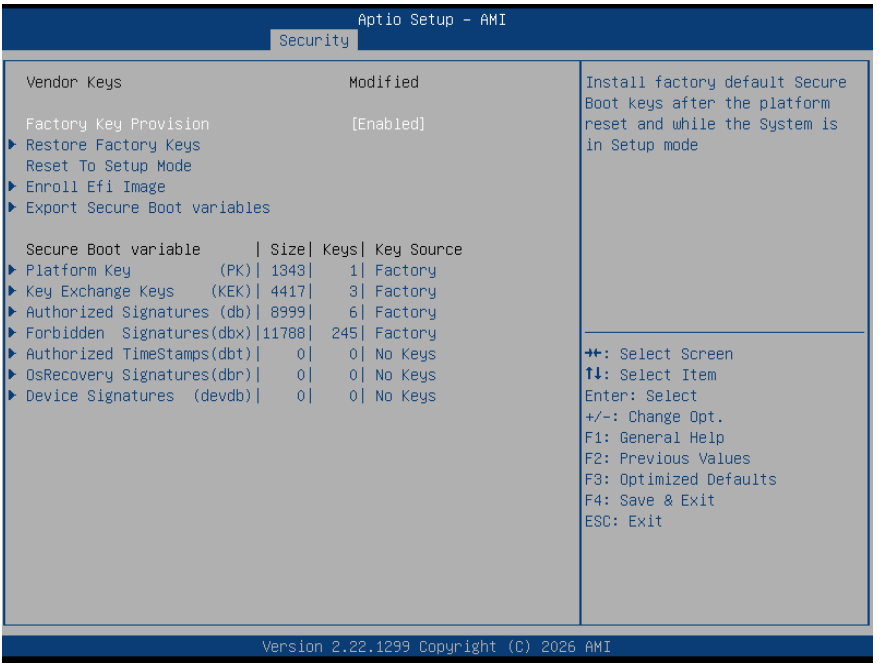
Options Summary		
Security Device Support	Enable	Optimal Default, Failsafe Default
	Disable	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
SHA256 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA256 PCR Bank.		
SHA384 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA384 PCR Bank.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. **NOTE**: Your Computer will reboot during restart in order to change State of Security Device.		
Platform Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	

Options Summary		
Enable or Disable Platform Hierarchy.		
Storage Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Storage Hierarchy.		
Endorsement Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Endorsement Hierarchy.		
Physical Presence Spec Version	1.3	Optimal Default, Failsafe Default
	1.2	
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
Device Select	Auto	
	TPM 1.2	
	TPM 2.0	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices if not found. TPM 1.2 devices will be enumerated.		

3.6.2 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Reset to Setup Mode		
Delete all Secure Boot key databases from NVRAM.		

3.6.3 Expert Key Management



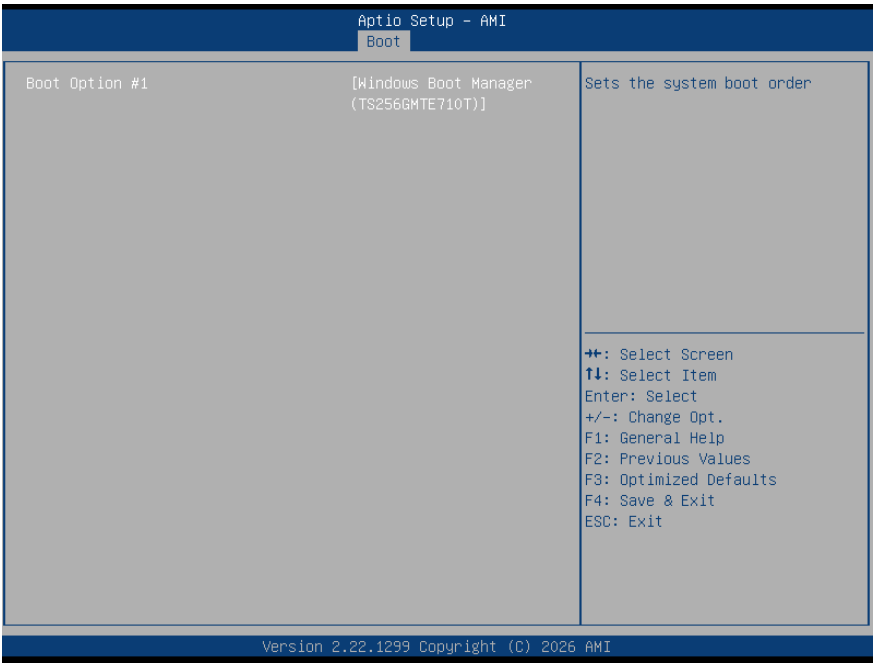
Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		
Reset to Setup Mode		
Delete all Secure Boot key databases from NVRAM.		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db).		

Options Summary	
Restore DB defaults	
Restore DB variable to factory defaults.	
Platform Key (PK)	Details
	Export
	Update
	Delete
Key Exchange Keys	Details
	Export
	Update
	Append
	Delete
Authorized Signatures	Details
	Export
	Update
	Append
	Delete
Forbidden Signatures	Details
	Export
	Update
	Append
	Delete
Authorized TimeStamps	Update
	Append
OsRecovery Signatures	Update
	Append
Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate: a) EFI_SIGNATURE_LIST. b) EFI_CERT_X509 (DER). c) EFI_CERT_RSA2048 (bin). d) EFI_CERT_SHAXXX. 2. Authenticated UEFI Variable. 3. EFI PE/COFF Image (SHA256). Key Source: Factory, External, Mixed.	

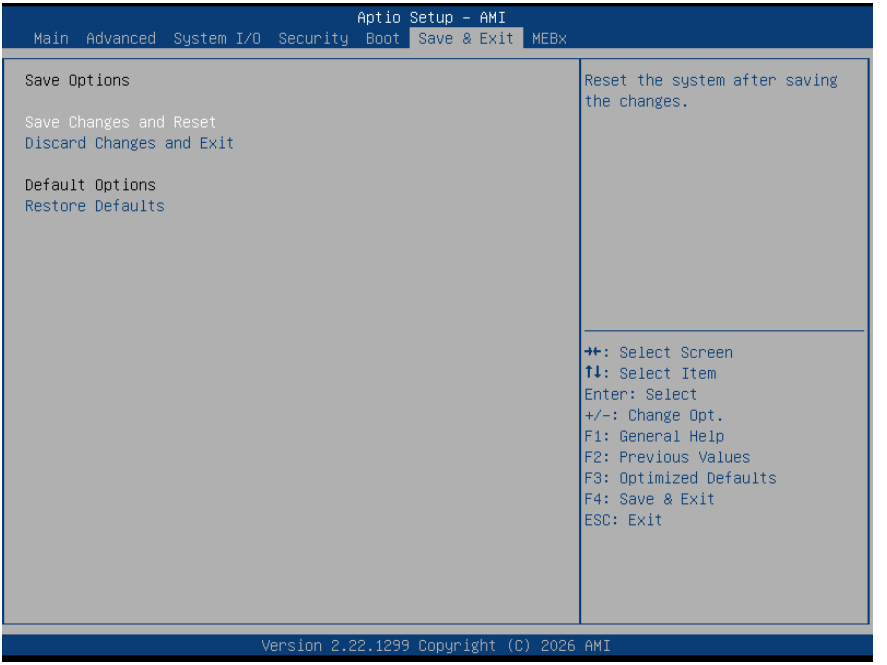
3.7 Setup Submenu: Boot

Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		
BOOT Option Priorities		
Sets the system boot order.		

3.7.1 BBS Priorities

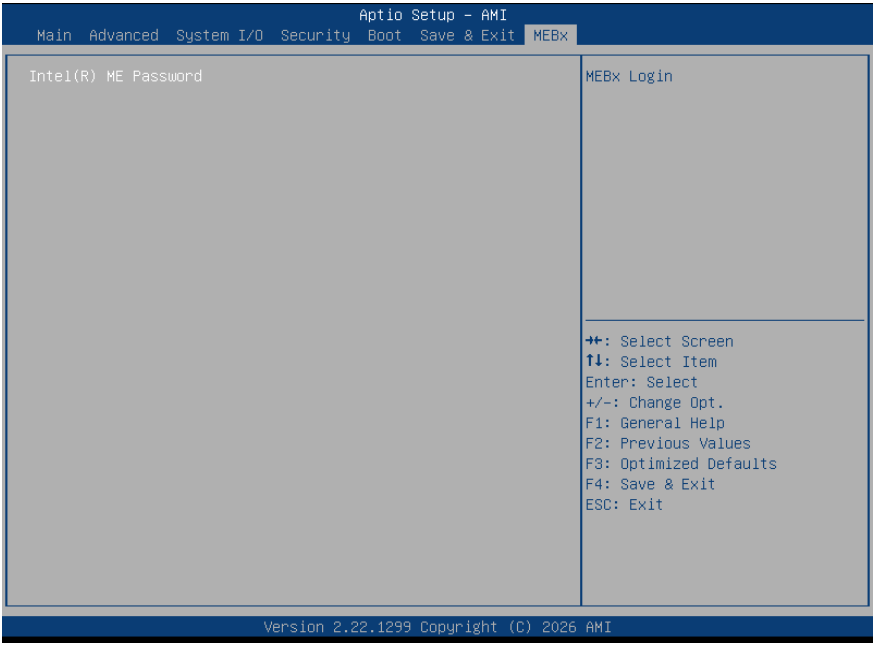


3.8 Setup Submenu: Save & Exit



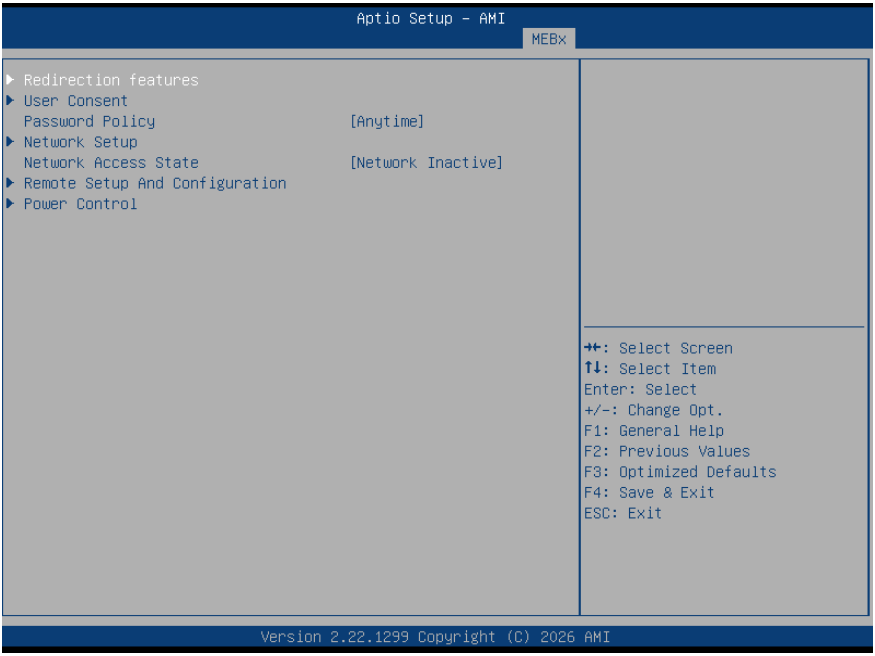
Options Summary	
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Restore Defaults	Restore/Load Default values for all the setup options.

3.9 Setup Submenu: MEBx



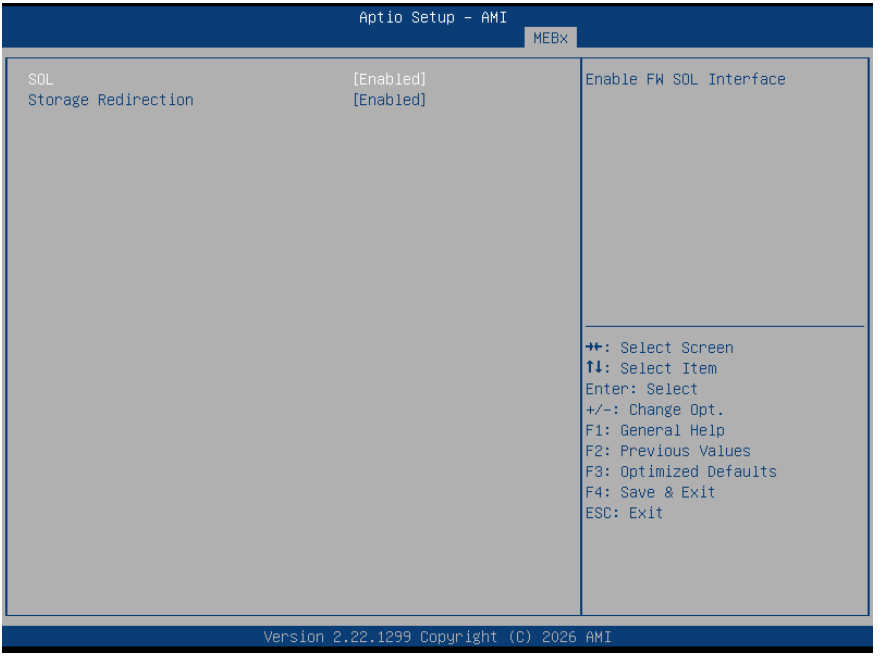
Options Summary		
Intel® Standard Manageability	Disabled	
	Partially Disable	
	Enabled	Optimal Default, Failsafe Default

3.9.1 Intel(R) Standard Manageability Configuration



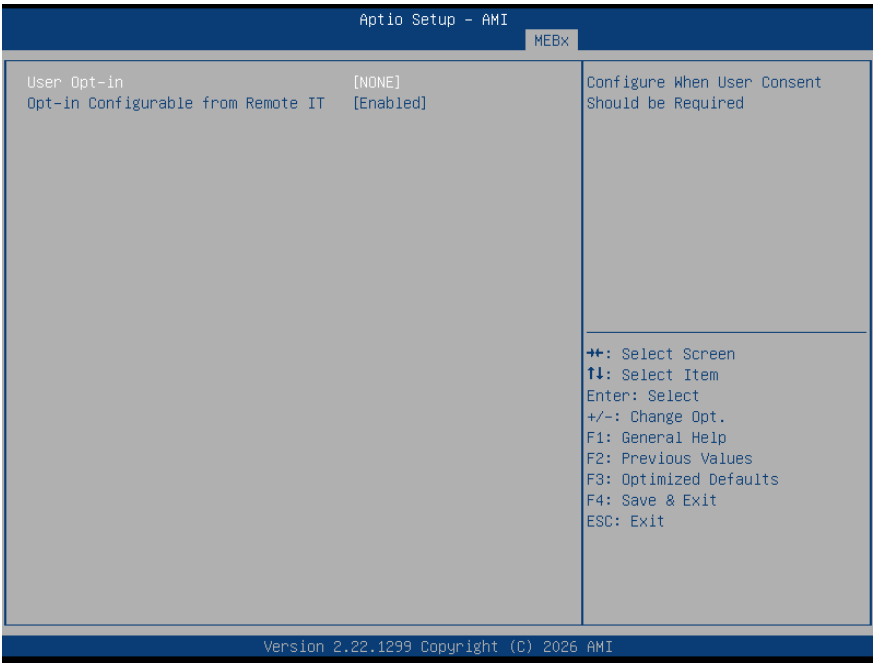
Options Summary		
Password Policy	Default Password Only	
	During Setup and Configuration	
	Anytime	Optimal Default, Failsafe Default
Network Access State	Network Active	
	Network Inactive	Optimal Default, Failsafe Default
	Full Unprovision	
Changes network state of ME. When disabling, it will also clear some other settings.		

3.9.2 Redirection Features



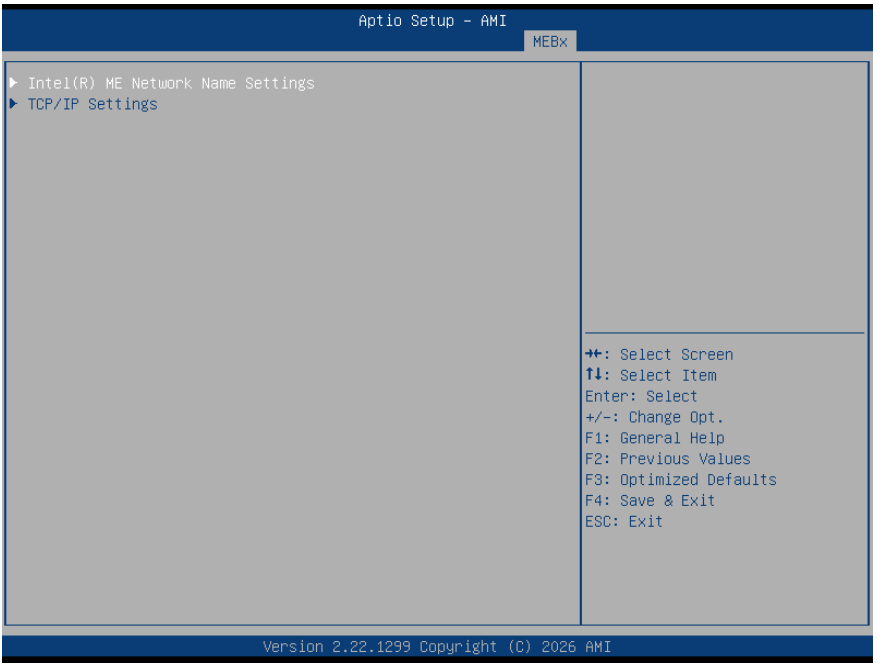
Options Summary		
SOL	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable FW SOL Interface.		
Storage Redirection	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable FW Remote – Storage Redirection.		

3.9.3 User Consent

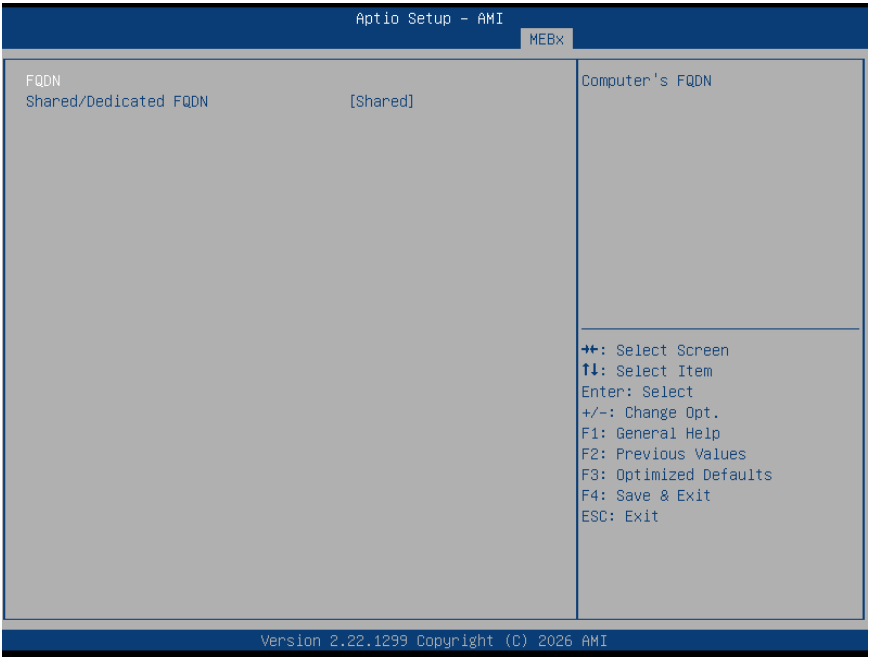


Options Summary		
User Opt-in	None	Optimal Default, Failsafe Default
	KVM	
	ALL	
Configure when User Consent Should be Required.		
Opt-in Configurable from Remote IT	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Remote Change Capability of User Consent Feature.		

3.9.4 Network Setup

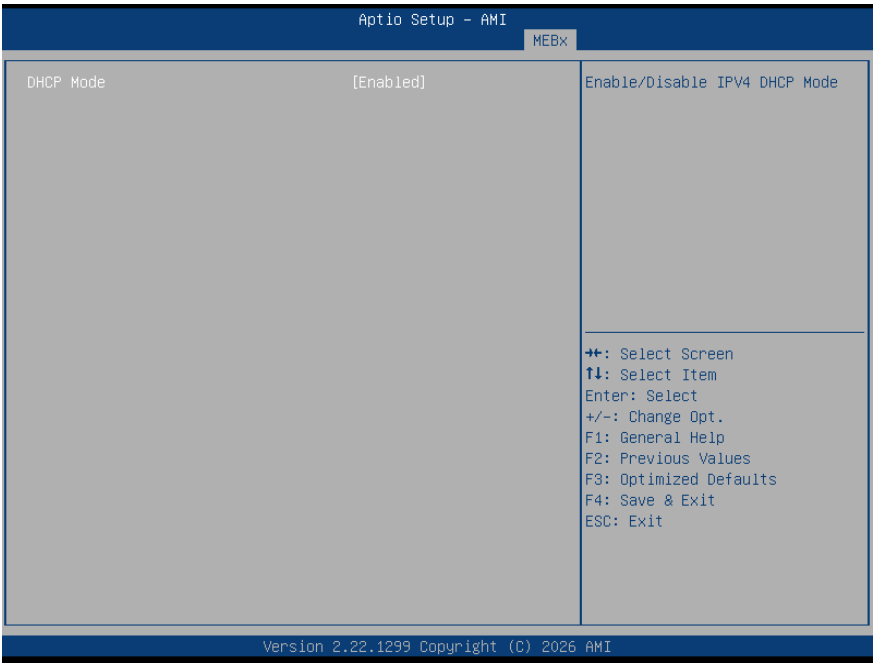


3.9.5 Intel® ME Network Name Settings



Options Summary		
FQDN		
Computer's FQDN.		
Shared/Dedicated FQDN	Dedicated	
	Shared	Optimal Default, Failsafe Default

3.9.6 TCP/IP Settings

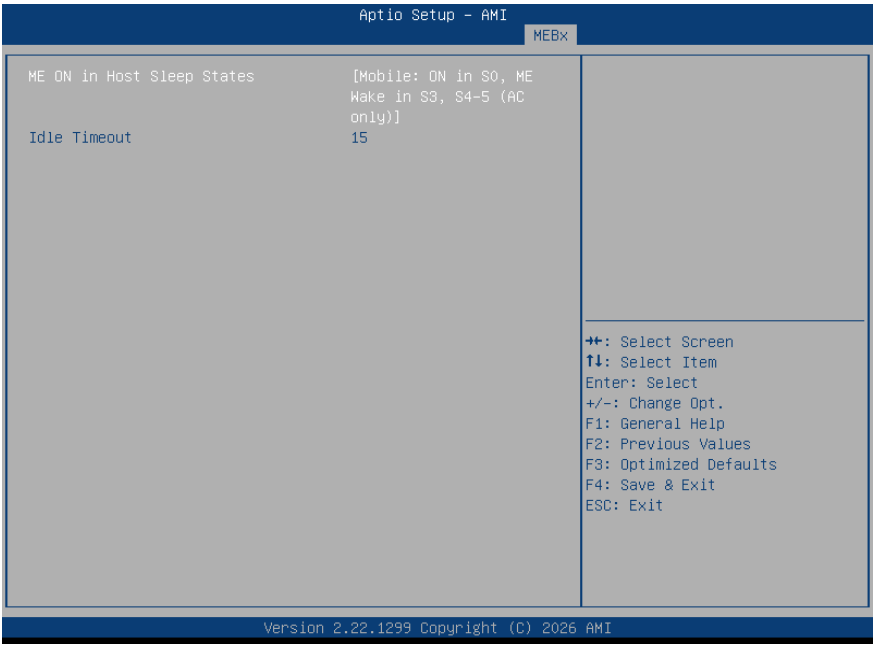


Options Summary		
DHCP Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable IPV4 DHCP Mode.		

3.9.7 Remote Setup and Configuration

Options Summary		
Provisioning Server Address		
Provisioning server address. Either host name or IPv4 or IPv6 address.		
Provisioning Server Port number		
Provisioning server port number (0-65535).		
Remote Configuration **	Enabled	Optimal Default, Failsafe Default
	Disabled	

3.9.8 Power Control



Options Summary		
ME ON in Host Sleep States	Mobile: ON in S0	
	Mobile: ON in S0, ME Wake in S3, S4-5 (AC only)	Optimal Default, Failsafe Default
Idle Timeout	15	Optimal Default, Failsafe Default
Timeout Value (1-65535).		

Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the EPIC-PTH9 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/product/detail/epic_boards_epic-pth9/download

Download the driver(s) you need and follow the steps below to install them.

Install Chipset Drivers

1. Open the **Chipset** folder and select your OS
2. Open the **SetupChipset.exe** file
3. Follow the instructions
4. Drivers will be installed automatically

Install Graphics Driver

1. Open the **Graphics** folder and select your OS
2. Open the **Installer.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Install LAN Drivers

Intel® Ethernet Controller I226

1. Open the folder
2. Right-click **e2fn.inf**
3. Select **Install** or **Show more options → Install**
4. Driver will be installed

Intel® Ethernet Connection I219

1. Open the folder
2. Right-click **e1dn.inf**
3. Select **Install** or **Show more options → Install**
4. Driver will be installed

Install Intel CSME Driver

1. Open the **Intel CSME** folder and select your OS
2. Open the **SetupME.exe** file
3. Follow the instructions
4. Drivers will be installed automatically

Install Peripheral Drivers

Serial IO Driver

1. Open the **Peripheral Driver** folder
2. Navigate to the **LPSS_PTL_30.100.2534.18_MUP3.0** ZIP file
3. Open the **SetupSerialIO.exe** file
4. Follow the instructions
5. Drivers will be installed automatically

Intel® Platform Monitoring Technology Driver

1. Open the **Peripheral Driver** folder
2. Navigate to the **intcpmt-7.3.11.3** ZIP file
3. Right-click **intcpmt.inf**
4. Select **Install** or **Show more options → Install**
5. Driver will be installed

NPU Driver

1. Open the **Peripheral Driver** folder
2. Navigate to the **npudriver-32.0.100.4621** ZIP file
3. Right-click **npu.inf**
4. Select **Install** or **Show more options → Install**
5. Driver will be installed

RAID Driver

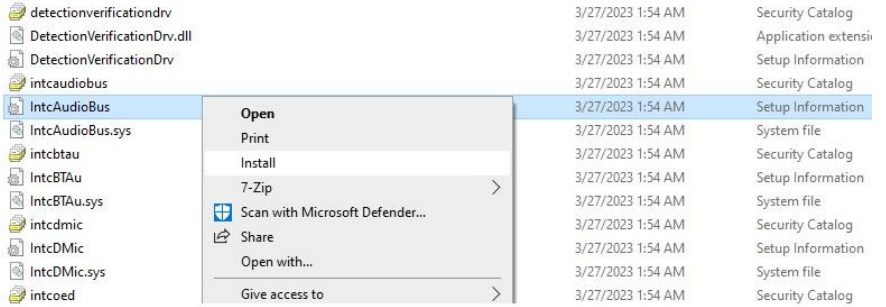
1. Open the **RAID Driver** folder and select your OS
2. Open the **SetupRST.exe** file
3. Follow the instructions
4. Drivers will be installed automatically

Install Intel Smart Sound Technology Driver

1. Open the **Intel Smart Sound Technology Driver** folder
2. Navigate the folder as follows: **Production** > **Drivers**, then follow the below instructions to install the BUS Driver (**IntcAudioBus.inf**) and OED Driver (**IntcOED.inf**).

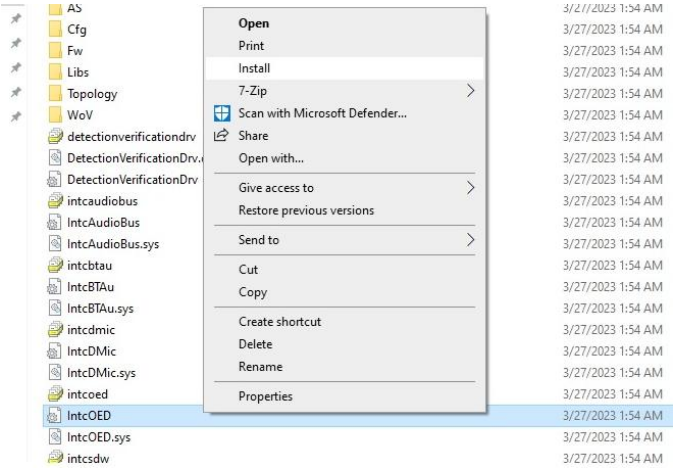
BUS driver (IntcAudioBus.inf)

a. Right click -> Install



OED driver (IntcOED.inf)

b. Right click -> Install



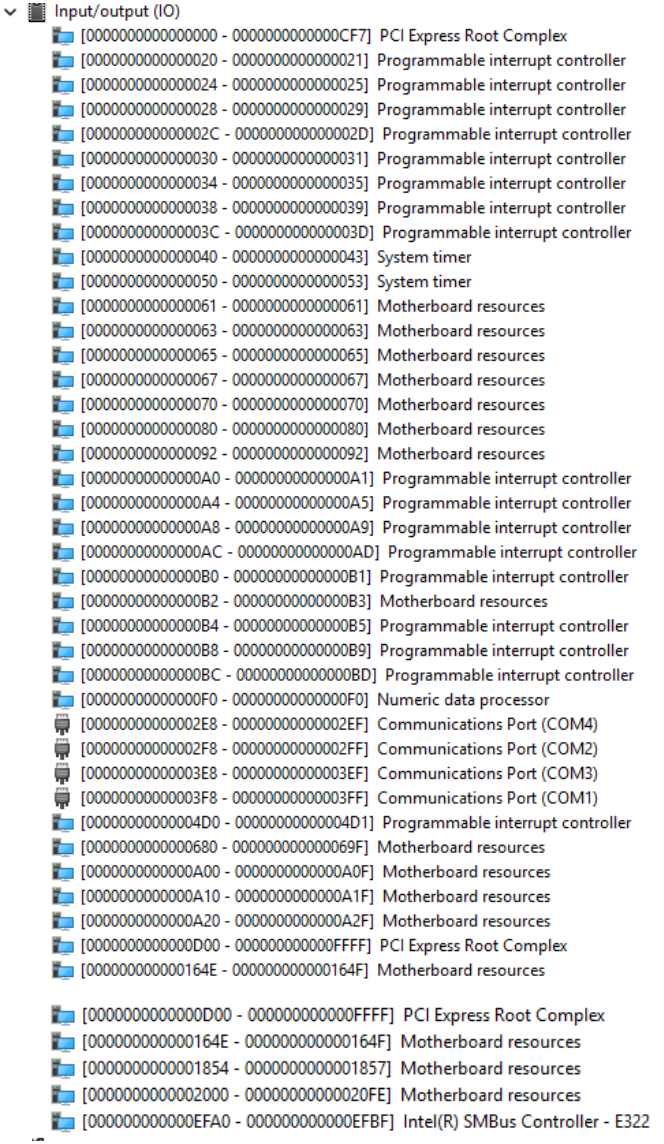
Install Realtek Audio Driver

1. Open the **Realtek Audio Driver** folder
2. Open the **Setup.exe** file
3. Follow the instructions
4. Drivers will be installed automatically

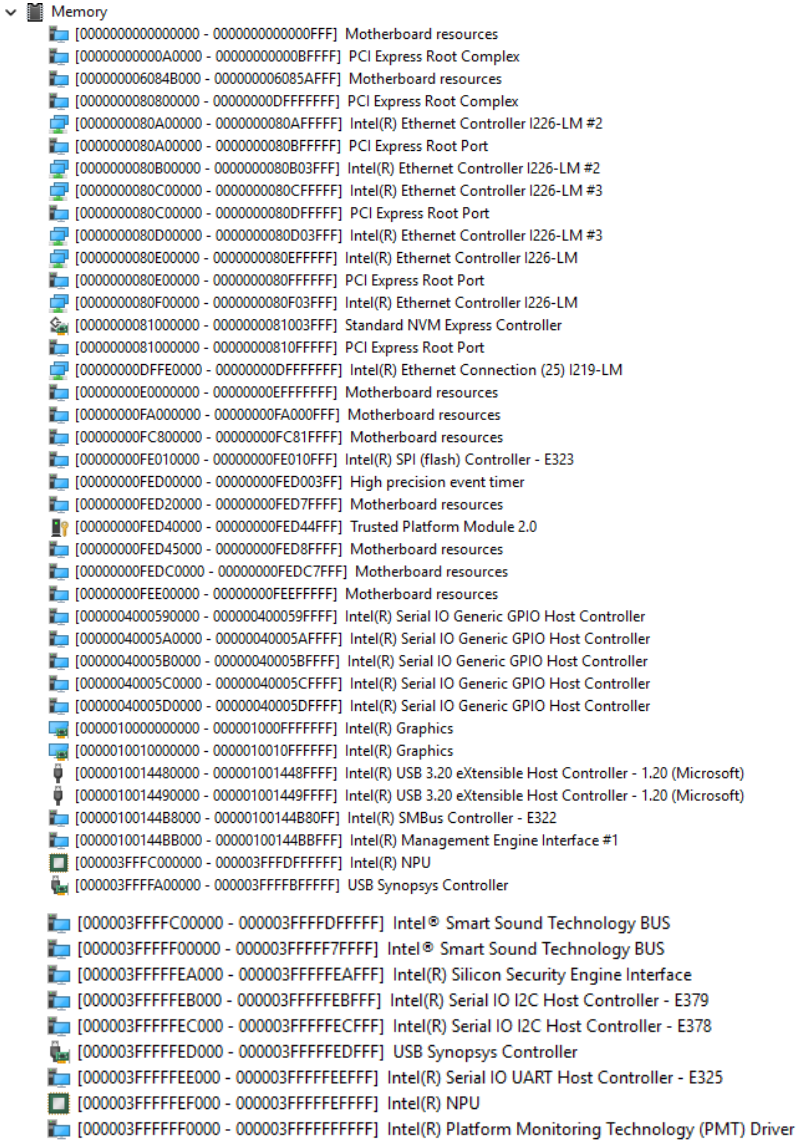
Appendix A

I/O Information

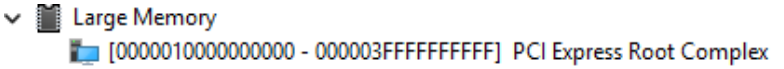
A.1 I/O Address Map



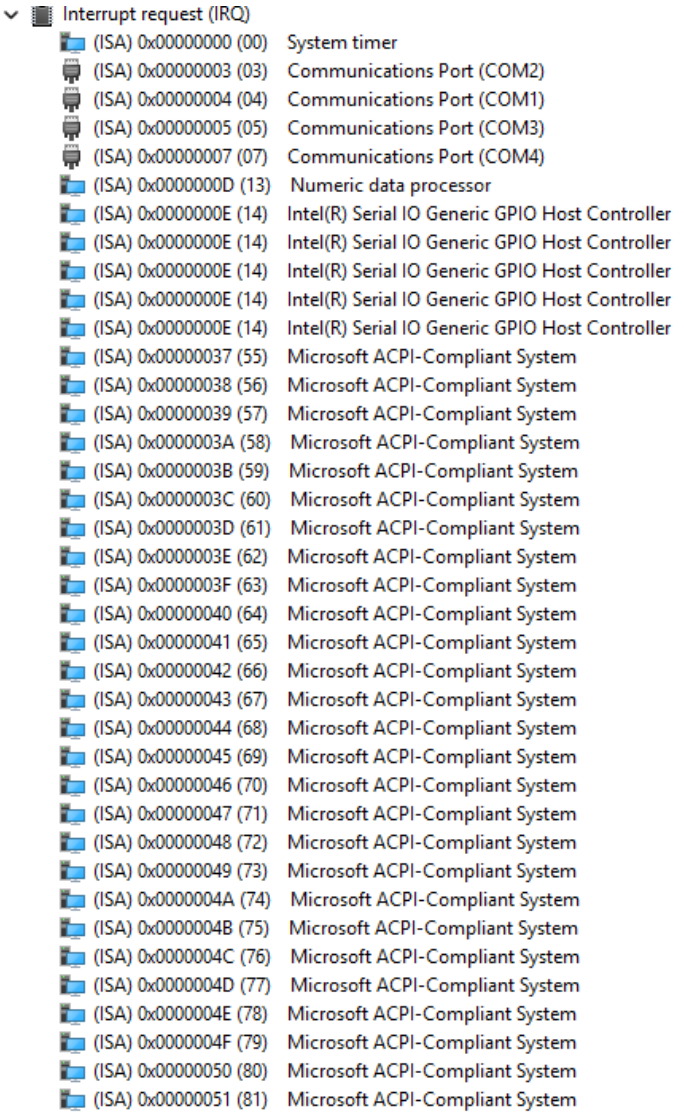
A.2 Memory Address Map



A.3 Large Memory Address



A.4 IRQ Mapping Chart



(ISA) 0x00000050 (80) Microsoft ACPI-Compliant System
(ISA) 0x00000051 (81) Microsoft ACPI-Compliant System
(ISA) 0x00000052 (82) Microsoft ACPI-Compliant System
(ISA) 0x00000053 (83) Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84) Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85) Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86) Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87) Microsoft ACPI-Compliant System
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(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System

(ISA) 0x000001D9 (473) Microsoft ACPI-Compliant System
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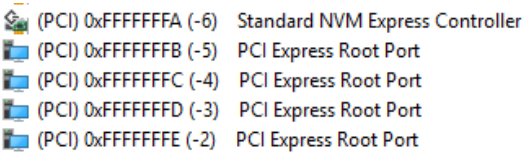
(PCI) 0x00000010 (16) Intel(R) Serial IO UART Host Controller - E325
(PCI) 0x00000011 (17) USB Synopsys Controller

(PCI) 0x0000001C (28) Intel(R) Serial IO I2C Host Controller - E379
(PCI) 0xFFFFFFD3 (-45) Intel(R) Silicon Security Engine Interface
(PCI) 0xFFFFFFD4 (-44) Intel® Smart Sound Technology BUS
(PCI) 0xFFFFFFD5 (-43) Intel(R) Ethernet Connection (25) I219-LM
(PCI) 0xFFFFFFD6 (-42) Intel(R) NPU
(PCI) 0xFFFFFFD7 (-41) Intel(R) Ethernet Controller I226-LM
(PCI) 0xFFFFFFD8 (-40) Intel(R) Ethernet Controller I226-LM
(PCI) 0xFFFFFFD9 (-39) Intel(R) Ethernet Controller I226-LM
(PCI) 0xFFFFFFDA (-38) Intel(R) Ethernet Controller I226-LM
(PCI) 0xFFFFFFDB (-37) Intel(R) Ethernet Controller I226-LM
(PCI) 0xFFFFFFDC (-36) Intel(R) Ethernet Controller I226-LM #3
(PCI) 0xFFFFFFDD (-35) Intel(R) Ethernet Controller I226-LM #3
(PCI) 0xFFFFFFDE (-34) Intel(R) Ethernet Controller I226-LM #3
(PCI) 0xFFFFFFDF (-33) Intel(R) Ethernet Controller I226-LM #3
(PCI) 0xFFFFFFE0 (-32) Intel(R) Ethernet Controller I226-LM #3
(PCI) 0xFFFFFFE1 (-31) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFE2 (-30) Intel(R) Ethernet Controller I226-LM #2
(PCI) 0xFFFFFFE3 (-29) Intel(R) Ethernet Controller I226-LM #2
(PCI) 0xFFFFFFE4 (-28) Intel(R) Ethernet Controller I226-LM #2
(PCI) 0xFFFFFFE5 (-27) Intel(R) Ethernet Controller I226-LM #2
(PCI) 0xFFFFFFE6 (-26) Intel(R) Ethernet Controller I226-LM #2
(PCI) 0xFFFFFFE7 (-25) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE8 (-24) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE9 (-23) Intel(R) Graphics
(PCI) 0xFFFFFFEA (-22) Intel(R) Platform Monitoring Technology (PMT) Driver
(PCI) 0xFFFFFFEB (-21) Standard NVM Express Controller
(PCI) 0xFFFFFFEC (-20) Standard NVM Express Controller
(PCI) 0xFFFFFFED (-19) Standard NVM Express Controller
(PCI) 0xFFFFFFEE (-18) Standard NVM Express Controller
(PCI) 0xFFFFFFEF (-17) Standard NVM Express Controller
(PCI) 0xFFFFFFF0 (-16) Standard NVM Express Controller
(PCI) 0xFFFFFFF1 (-15) Standard NVM Express Controller
(PCI) 0xFFFFFFF2 (-14) Standard NVM Express Controller
(PCI) 0xFFFFFFF3 (-13) Standard NVM Express Controller
(PCI) 0xFFFFFFF4 (-12) Standard NVM Express Controller
(PCI) 0xFFFFFFF5 (-11) Standard NVM Express Controller
(PCI) 0xFFFFFFF6 (-10) Standard NVM Express Controller
(PCI) 0xFFFFFFF7 (-9) Standard NVM Express Controller
(PCI) 0xFFFFFFF8 (-8) Standard NVM Express Controller
(PCI) 0xFFFFFFF9 (-7) Standard NVM Express Controller
(PCI) 0xFFFFFFFA (-6) Standard NVM Express Controller


(PCI) 0xFFFFFFFA (-6) Standard NVM Express Controller
(PCI) 0xFFFFFFFB (-5) PCI Express Root Port
(PCI) 0xFFFFFFFC (-4) PCI Express Root Port
(PCI) 0xFFFFFFFD (-3) PCI Express Root Port
(PCI) 0xFFFFFFFE (-2) PCI Express Root Port

Appendix B

Mating Connectors

B.1 List of Mating Connectors and Cables

Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model no		
CN1	External RTC	Molex	51021-0200	Battery Cable	175011901C
CN4	LVDS Inverter	Aces	50233-006h	N/A	N/A
CN5	LVDS Conn	HIROSE	DF13-30DS-1. 25C	N/A	N/A
CN6	eDP Conn	I-PEX	20453-030T-01S	N/A	N/A
CN13	COM Port 1	Molex	21021-0900	UART Wafer Cable	1701090150
CN14	COM Port 2	Molex	21021-0900	UART Wafer Cable	1701090150
CN15	COM Port 3	Molex	21021-0900	UART Wafer Cable	1701090150
CN16	COM Port 4	Molex	21021-0900	UART Wafer Cable	1701090150
CN17	GPIO	Molex	51110-1050	N/A	N/A
CN20	USB 2.0 Conn	Molex	51021-0500	USB Wafer Cable	1700050207
CN21	USB 2.0 Conn	Molex	51021-0500	USB Wafer Cable	1700050207
CN22	USB 2.0 Conn	Molex	51021-0500	USB Wafer Cable	1700050207
CN23	USB 2.0 Conn	Molex	51021-0500	USB Wafer Cable	1700050207
CN28	Audio with detect	Aces	50247-012H0H0-001	Audio Cable 25cm	170X000156
CN29	I2C/SMBus	JST	SHR-05V-S-B	I2C/SMBUS cable	170X000743
CN30	Port 80 Debug Card	JST	SHR-10V-S-B	Debug Card Cable	1703100133
CN32	Power	N/A	N/A	Power cable	170204010R
CN34	Front Panel Conn	JST	SHR-10V-S-B	Front Panel Cable 10cm	170X000603
CN35	External +5VSB Power Input and PS_ON#	JST	XHP-3	External +5VSB Power Input and PS_ON#	170220020B