

# EPIC-CFS7-PUC

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EPIC Board

User's Manual 1<sup>st</sup> Ed

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## Packing List

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Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● EPIC-CFS7-PUC	1
● Jumper Cap	1
● Back plate for cooler	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

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This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

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Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
18. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## 产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯 醚(PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

- 一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
- 二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。
- 三、上述部件物质液晶模块、触控模块仅一体机产品适用。

## China RoHS Requirement (EN)

### Hazardous and Toxic Materials List

AAEON System

QQ4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBs)	Polybrominated ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

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# Chapter 1

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Product Specifications

## 1.1 Specifications

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### System

Form Factor	4" EPIC Board
CPU	8th Generation Intel® Core™ Processor family
CPU Frequency	Up to 4.6GHz
Chipset	Intel® H310/Q370 (TDP: 6W)
Memory Type	DDR4 2666 MHz SODIMM x 2 (Dual Channel, Non-ECC)
Max. Memory Capacity	Up to 32GB
BIOS	AMI UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	+12V
Power Supply Type	AT/ATX
Power Consumption (Typical)	95.04W (system)
Dimensions	<b>System (L x W x H):</b> 8.50" x 7.09" x 2.56" (216mm x 180mm x 65mm) <b>Board (L x W):</b> 4.53" x 6.5" (115mm x 165mm)
Operating Temperature	32°F ~ 122°F (0°C ~ 50°C)
Storage Temperature	-4°F ~ 176°F (-20°C ~ 80°C)
Operating Humidity	0 ~ 90% @ 40°C, non-condensing
MTBF (Hours)	TBD
Certification	CE/FCC Class A

## Display

VGA/LCD Controller	8th Generation Intel® Core™ Processor family
Video Output	HDMI x 2
Backlight Inverter Supply	—

## I/O

Ethernet	Intel® I211, 10/100/1000Base, RJ45 x 4 (Supports PoE 802.3af); two ports on main board, two ports on daughter board
Audio	—
USB Port	USB3.2 Gen 2/ USB2.0 x 4 (Rear I/O) USB2.0 x 2 (Internal header)
Serial Port	RS-232/422/485 x 2 (Internal header)
Parallel Port (printer port)	—
HDD Interface	SATA III (6.0 Gbps) x 1
SSD	—
Expansion Slot	PCIe[x4] FPC slot (For PoE card) Full Size mSATA/mPCIe slot x 1 LPC Bus SMBus (default) / I2C (option)
DIO	Isolated DIO 32 bits (16 bits in/16 bits out) *system function from daughter board
TPM	—
Touch	—
SIM	—



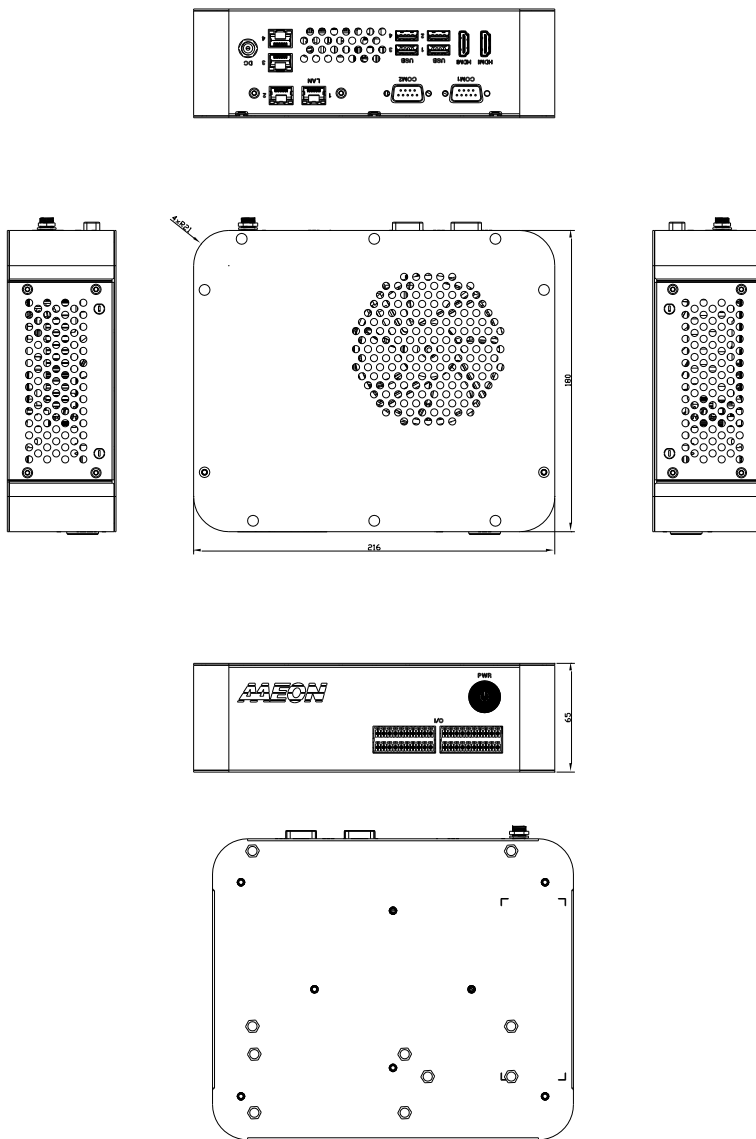
# Chapter 2

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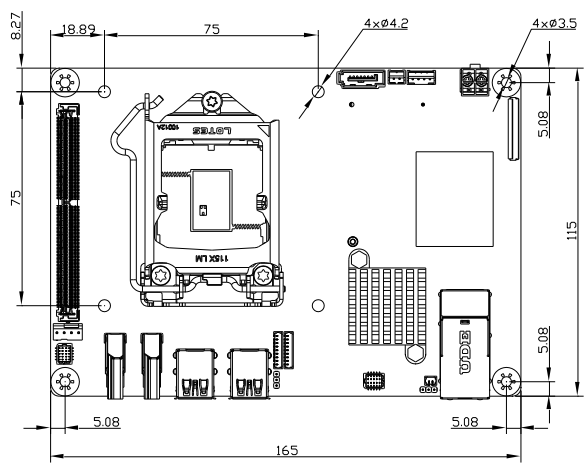
Hardware Information

## 2.1 Dimensions

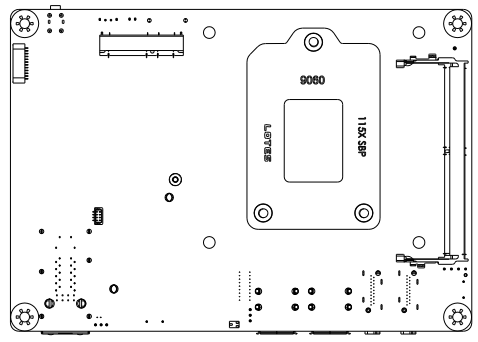
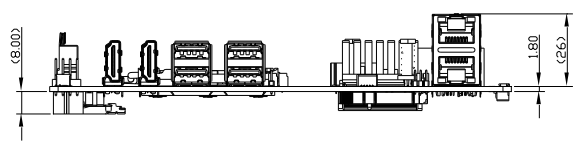
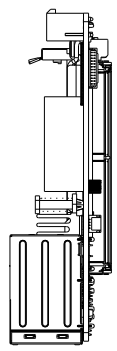
### System



### Board

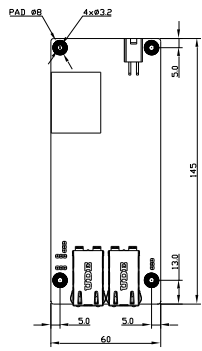


Component Side

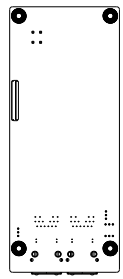


Solder Side

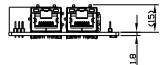
### POE Carrier Board



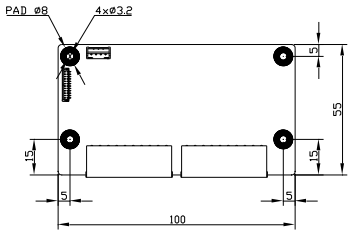
Component Side



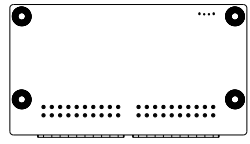
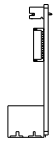
Solder Side



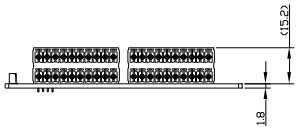
### DIO Carrier Board



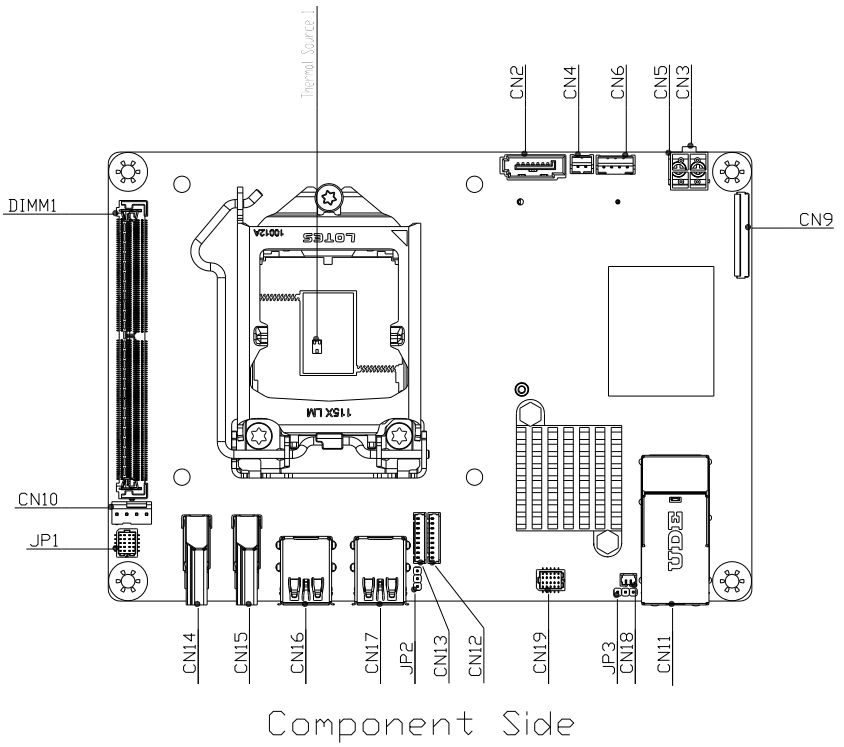
Component Side

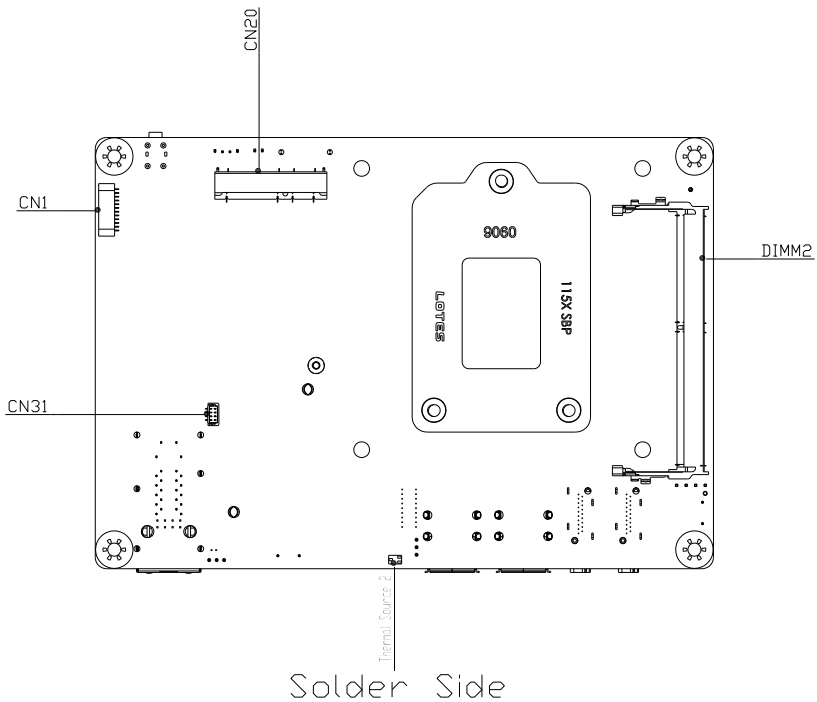


Solder Side

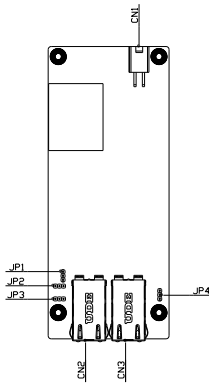


## 2.2 Jumpers and Connectors

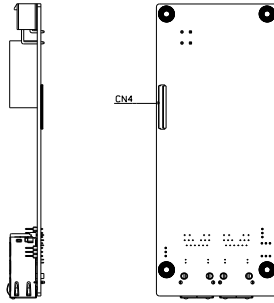




### POE Carrier Board



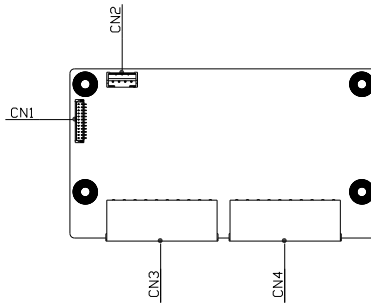
Component Side



Solder Side



### DIO Carrier Board



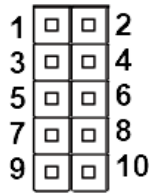
Component Side

## 2.3 List of Jumpers (Main Board)

Please refer to the table below for all of the board's jumpers that you can configure for your application.

Label	Function
JP1	Front Panel PIN Header
JP2	AT/ATX Mode Selection
JP3	Clear C-MOS PIN Header

### 2.3.1 Front Panel PIN Header (JP1)



Pin	Signal Description	Pin	Signal Description
1	GND	2	EXT_PWRBTN#
3	FP_HDLED-	4	FP_HDLED+
5	FP_SPKR-	6	+V5S
7	GND	8	PWRLED+
9	GND	10	HWRST#

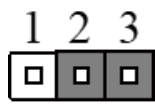


### 2.3.2 AT/ATX mode Selection (JP2)

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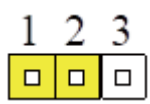
ATX Mode



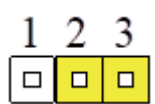
AT mode (Default)

### 2.3.3 Clear CMOS Jumper (JP3)

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Normal (Default)



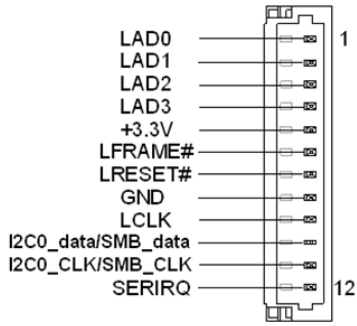
Clear CMOS

## 2.4 List of Connectors (Main Board)

The table below lists all of the board's connectors, configurable for your application.

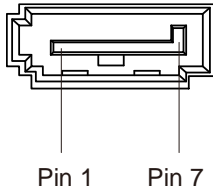
Label	Function
CN1	LPC Connector for Debug
CN2	SATA Connector
CN4	SATA Power Connector
CN5	2-Pin DC IN Connector
CN6	DIO Power Connector
CN9	PCIe [x4] FPC Connector
CN10	CPU Fan Connector
CN11	POE LAN RJ45 Connector
CN12	RS232/422/485 COM2 Connector
CN13	RS232/422/485 COM1 Connector
CN14	HDMI Connector
CN15	HDMI Connector
CN16	USB 3.2 Gen 2 (10 Gbps) Connector
CN17	USB 3.2 Gen 2 (10 Gbps) Connector
CN18	RTC Connector
CN19	USB 2.0 Connector
CN20	Mini Card Connector
CPU1	CPU Socket
DIMM1	DDR4 SO-DIMM RAM Socket 1
DIMM2	DDR4 SO-DIMM RAM Socket 2

## 2.4.1 LPC Port (CN1)



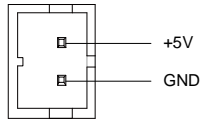
Pin	Signal Description	Pin	Signal Description
1	LPC_AD0	7	RST#
2	LPC_AD1	8	GND
3	LPC_AD2	9	CLK
4	LPC_AD3	10	I2C0_data/SMB_data
5	P3V3	11	I2C0_CLK/SMB_CLK
6	FRAME#	12	INT_SERIRQ

### 2.4.2 SATA Connector (CN2)



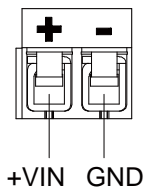
Pin	Signal Description	Pin	Signal Description
1	GND	5	SATA_RXN0
2	SATA_TXP0	6	SATA_RXP0
3	SATA_TXN0	7	GND
4	GND		

### 2.4.3 SATA Power (CN4)



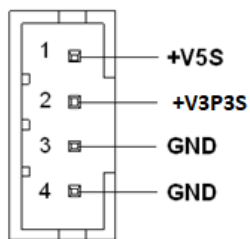
Pin	Signal Description
1	+5V max 1A
2	GND

### 2.4.4 2 Pin DC IN Connector (CN5)



Pin	Signal Description
1	+12V
2	GND

### 2.4.5 DIO Power Connector (CN6)

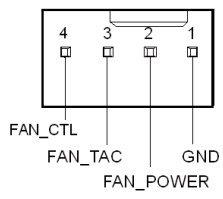


Pin	Signal Description
1	+V5S max 0.5A
2	+V3P3S max 1A
3	GND
4	GND

## 2.4.6 PCIe [x4] FPC Connector (CN9)

Pin	Signal Description	Pin	Signal Description
1	+V3P3S	21	PCIE_12_TXN
2	+V3P3S	22	PCIE_12_TXP
3	+V3P3S	23	GND
4	SMB_DATA	24	PCIE_11_TXN
5	SMB_CLK	25	PCIE_11_TXP
6	BUF_PLT_RST#	26	GND
7	+V3P3A	27	PCIE_10_TXN
8	GND	28	PCIE_10_TXP
9	PCIE_10_RXP	29	GND
10	PCIE_10_RXN	30	PCIE_3_CLK_DN
11	GND	31	PCIE_3_CLK_DP
12	PCIE_12_RXP	32	GND
13	PCIE_12_RXN	33	PCIE_9_TXN
14	GND	34	PCIE_9_TXP
15	PCIE_11_RXP	35	GND
16	PCIE_11_RXN	36	+V12V
17	GND	37	+V12V
18	PCIE_9_RXP	38	+V12V
19	PCIE_9_RXN	39	+V12V
20	GND	40	+V12V

### 2.4.7 CPU FAN Connector (CN10)



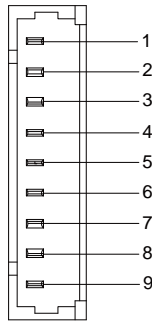
Pin	Signal Description	Current
1	GND	
2	FAN_POWER	1 Amp
3	FAN_TAC	
4	FAN_CTL	

### 2.4.8 POE LAN (RJ-45) Connector (CN11)

Pin	Signal Description	Pin	Signal Description
R1A	LAN2_MDI0_N	L1A	LAN2_LED_100#
R2A	LAN2_MDI0_P	L2A	LAN2_LED_1000#
R3A	LAN2_MDI1_N	L3A	AGND
R4A	LAN2_MDI1_P	L4A	OUT2_LED
R5A	LAN2_MDI2_N		
R6A	LAN2_MDI2_P		
R7A	LAN2_MDI2_N		
R8A	LAN2_MDI3_P		
R9A	CAP	R11A	OUT2
R10A	GND	R12A	AGND
R1B	LAN1_MDI0_N	L1B	LAN1_LED_100#
R2B	LAN1_MDI0_P	L2B	LAN1_LED_1000#

Pin	Signal Description	Pin	Signal Description
R3B	LAN1_MDI1_N	L3B	AGND
R4B	LAN1_MDI1_P	L4B	OUT1_LED
R5B	LAN1_MDI2_N		
R6B	LAN1_MDI2_P		
R7B	LAN1_MDI3_N		
R8B	LAN1_MDI3_P		
R9B	CAP	R11B	OUT1
R10B	GND	R12B	AGND

## 2.4.9 RS232/422/485 connector COM1, COM2 (CN12/13)



RS232

Pin	Signal Description	Pin	Signal Description
1	DCD2	6	CTS2
2	DSR2	7	DTR2
3	RX2	8	R1
4	RTS2	9	GND
5	TX2		



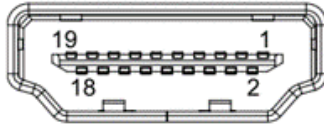
## RS422

Pin	Signal Description	Pin	Signal Description
1	RS422_TX2-	6	NC
2	NC	7	RS422_RX2-
3	RS422_TX2+	8	NC/+5V/+12V max 0.5A
4	NC	9	GND
5	RS422_RX2+		

## RS485

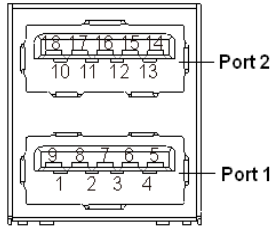
Pin	Signal Description	Pin	Signal Description
1	RS485_D2-	6	NC
2	NC	7	NC
3	RS485_D2+	8	NC/+5V/+12V max 0.5A
4	NC	9	GND
5	NC		

## 2.4.10 HDMI Connector (CN14/15)



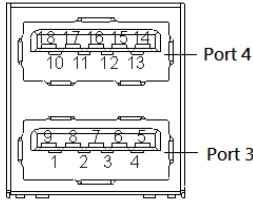
Pin	Signal Description	Pin	Signal Description
1	HDMI_TX2+	11	GND
2	GND	12	HDMI_CLK-
3	HDMI_TX2-	13	NC
4	HDMI_TX1+	14	NC
5	GND	15	DDC_CLK
6	HDMI_TX1-	16	DDC_DATA
7	HDMI_TX0+	17	GND
8	GND	18	+5V
9	HDMI_TX0-	19	HDMI_HPD
10	HDMI_CLK+		

## 2.4.11 USB 3.2 Gen 2 Connector (CN16)



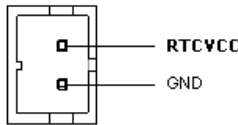
Pin	Signal Description	Pin	Signal Description
1	+5VSB	10	+5VSB
2	USB1_D-	11	USB2_D-
3	USB1_D+	12	USB2_D+
4	GND	13	GND
5	USB1_SSRX-	14	USB2_SSRX-
6	USB1_SSRX+	15	USB2_SSRX+
7	GND	16	GND
8	USB1_SSTX-	17	USB2_SSTX-
9	USB1_SSTX+	18	USB2_SSTX+

### 2.4.12 USB 3.2 Gen 2 Connector (CN17)



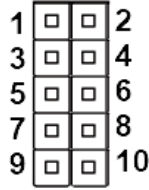
Pin	Signal Description	Pin	Signal Description
1	+5VSB	10	+5VSB
2	USB3_D-	11	USB4_D-
3	USB3_D+	12	USB4_D+
4	GND	13	GND
5	USB3_SSRX-	14	USB4_SSRX-
6	USB3_SSRX+	15	USB4_SSRX+
7	GND	16	GND
8	USB3_SSTX-	17	USB4_SSTX-
9	USB3_SSTX+	18	USB4_SSTX+

### 2.4.13 RTC Connector (CN18)



Pin	Signal Description
1	RTCVCC
2	GND

## 2.4.14 USB 2.0 Connector (CN19)



Pin	Signal Description	Pin	Signal Description
1	VCC	2	VCC
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	GND	10	GND

## 2.4.15 Mini Card Connector (CN20)

Pin	Signal Description	Pin	Signal Description
1	PCIE_WAKE#	27	GND
2	+3.3VSB	28	+1.5V
3	NC	29	GND
4	GND	30	SMB_CLK
5	NC	31	PCIE_TX-
6	+1.5V	32	SMB_DATA
7	IN	33	PCIE_TX+
8	UIM_PWR	34	GND
9	GND	35	GND
10	UIM_DATA	36	USB_D-
11	PCIE_REF_CLK-	37	GND

Pin	Signal Description	Pin	Signal Description
12	UIM_CLK	38	USB_D+
13	PCIE_REF_CLK+	39	+3.3VSB
14	UIM_RST	40	GND
15	GND	41	+3.3VSB
16	UIM_VPP	42	NC
17	NC	43	GND
18	GND	44	NC
19	NC	45	NC
20	W_DISABLE#	46	NC
21	GND	47	NC
22	PCIE_RST#	48	+1.5V
23	PCIE_RX-	49	NC
24	+3.3VSB	50	GND
25	PCIE_RX+	51	NC
26	GND	52	+3.3VSB

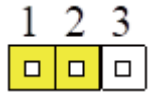
## 2.4.16 DDR4 SO-DIMM Slot (DIMM1 & DIMM2)

Standard specification

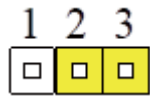
## 2.5 List of Jumpers (POE Board)

Label	Function
JP1	OUT2 Select
JP2	AGND2 Select
JP3	AGND1 Select
JP4	OUT1 Select

### 2.5.1 OUT2 Select (JP1)

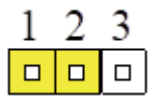


OUT2\_1236 (Default)

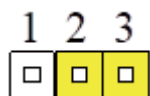


OUT2\_4578

### 2.5.2 AGND2 Select (JP2)

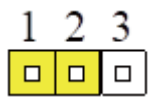


AGND2\_1236 (Default)

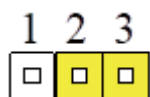


AGND2\_4578

### 2.5.3 AGND1 Select (JP3)



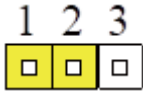
AGND1\_1236 (Default)



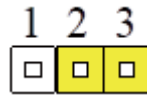
AGND1\_4578

## 2.5.4 OUT1 Select (JP4)

---



OUT1\_1236 (Default)



OUT1\_4578



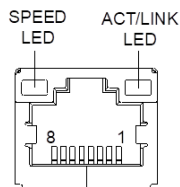
## 2.6 List of Connectors (POE Board)

Label	Function
CN1	12V DC IN
CN2	LAN2 RJ-45 Port
CN3	LAN1 RJ-45 Port
CN4	FPC Cable Port (Connect to EPIC-CFS7)

### 2.6.1 12V DC In (CN1)

Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	GND	GND	
3	+V_IN	PWR	12V
4	+V_IN	PWR	12V

### 2.6.2 LAN RJ-45 Port (CN2/CN3)



Pin	Pin Name	Signal Type	Signal Level
1	TRP1+	DIFF	
2	TRP1-	DIFF	
3	TRP2+	DIFF	
4	TRP3+	DIFF	

Pin	Pin Name	Signal Type	Signal Level
5	TRP3-	DIFF	
6	TRP2-	DIFF	
7	TRP4+	DIFF	
8	TRP4-	DIFF	

### 2.6.3 FPC Cable Port (CN4)



Pin	Pin Name	Signal Type	Signal Level
1	+V12S	PWR	+12V
2	+V12S	PWR	+12V
3	+V12S	PWR	+12V
4	+V12S	PWR	+12V
5	+V12S	PWR	+12V
6	GND	GND	
7	PCIE_9_TXP	DIFF	
8	PCIE_9_TXN	DIFF	
9	GND	GND	

Pin	Pin Name	Signal Type	Signal Level
10	PCIE_3_CLK_DP	DIFF	
11	PCIE_3_CLK_DN	DIFF	
12	GND	GND	
13	PCIE_10_TXP	DIFF	
14	PCIE_10_TXN	DIFF	
15	GND	GND	
16	PCIE_11_TXP	DIFF	
17	PCIE_11_TXN	DIFF	
18	GND	GND	
19	PCIE_12_TXP	DIFF	
20	PCIE_12_TXN	DIFF	
21	GND	GND	
22	PCIE_9_RXN	DIFF	
23	PCIE_9_RXP	DIFF	
24	GND	GND	
25	PCIE_11_RXN	DIFF	
26	PCIE_11_RXP	DIFF	
27	GND	GND	
28	PCIE_12_RXN	DIFF	
29	PCIE_12_RXP	DIFF	
30	GND	GND	
31	PCIE_10_RXN	DIFF	
32	PCIE_10_RXP	DIFF	
33	GND	GND	
34	+V3P3A	DIFF	+3.3V
35	BUF_PLT_RST#	I/O	+3.3V

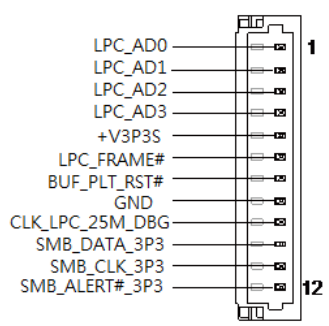
Pin	Pin Name	Signal Type	Signal Level
36	SMB_CLK	I/O	+3.3V
37	SMB_DATA	I/O	+3.3V
38	+V3P3S		+3.3V
39	+V3P3S		+3.3V
40	+V3P3S		+3.3V

## 2.7 List of Connectors (DIO Board)

Note: There are no jumpers on DIO Board.

Label	Function
CN1	LPC Port
CN2	Power In (from EPIC-CFS7)
CN3	GPI Port
CN4	GPO Port

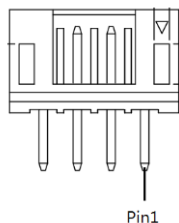
### 2.7.1 LPC Port (CN1)



Pin	Pin Name	Signal Type	Signal Level
1	LPC_AD0	I/O	+3.3V
2	LPC_AD1	I/O	+3.3V
3	LPC_AD2	I/O	+3.3V
4	LPC_AD3	I/O	+3.3V
5	+V3P3S	PWR	+3.3V
6	LPC_FRAME#	IN	

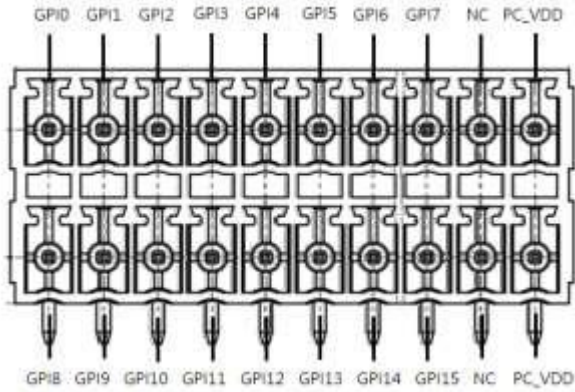
Pin	Pin Name	Signal Type	Signal Level
7	BUF_PLT_RST#	IN	+3.3V
8	GND	GND	
9	CLK_LPC_25M_DBG	OUT	
10	SMB_DATA_3P3	I/O	+3.3V
11	SMB_CLK_3P3	IN	+3.3V
12	SMB_ALERT#_3P#	I/O	+3.3V

## 2.7.2 Power In (CN2)



Pin	Pin Name	Signal Type	Signal Level
1	+V5S	PWR	+5V
2	+V3P3S	PWR	+3.3V
3	GND	GND	
4	GND	GND	

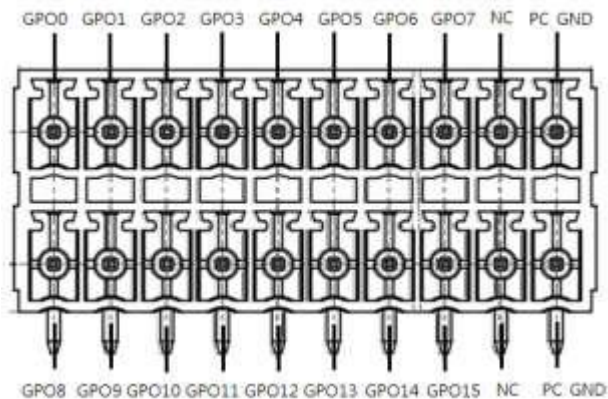
### 2.7.3 GPI Port (CN3)



Pin	Pin Name	Signal Type	Signal Level
1	GPI0	IN	+12V/+24V
2	GPI1	IN	+12V/+24V
3	GPI2	IN	+12V/+24V
4	GPI3	IN	+12V/+24V
5	GPI4	IN	+12V/+24V
6	GPI5	IN	+12V/+24V
7	GPI6	IN	+12V/+24V
8	GPI7	IN	+12V/+24V
9	NC	NC	
10	PC_VDD	PWR	+12V/+24V
11	GPI8	IN	+12V/+24V
12	GPI9	IN	+12V/+24V
13	GPI10	IN	+12V/+24V
14	GPI11	IN	+12V/+24V

Pin	Pin Name	Signal Type	Signal Level
15	GP112	IN	+12V/+24V
16	GP113	IN	+12V/+24V
17	GP114	IN	+12V/+24V
18	GP115	IN	+12V/+24V
19	NC	NC	
20	PC_VDD	PWR	+12V/+24V

## 2.7.4 GPO Port (CN4)



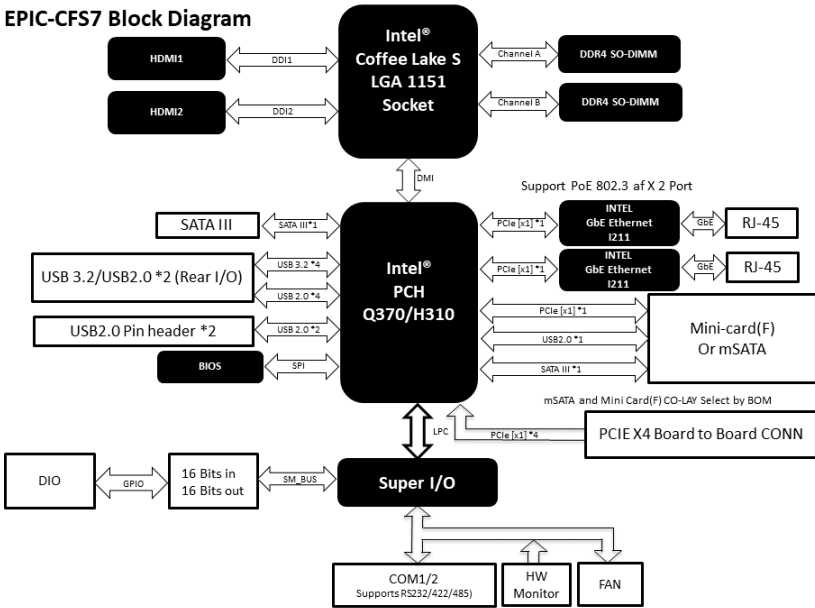
Pin	Pin Name	Signal Type	Signal Level
1	GPO0	OUT	+12V/+24V
2	GPO1	OUT	+12V/+24V
3	GPO2	OUT	+12V/+24V
4	GPO3	OUT	+12V/+24V
5	GPO4	OUT	+12V/+24V
6	GPO5	OUT	+12V/+24V



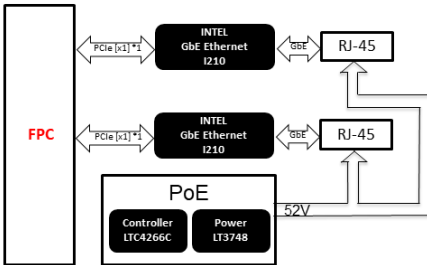
Pin	Pin Name	Signal Type	Signal Level
7	GPO6	OUT	+12V/+24V
8	GPO7	OUT	+12V/+24V
9	NC	NC	
10	PC_GND	GND	
11	GPO8	OUT	+12V/+24V
12	GPO9	OUT	+12V/+24V
13	GPO10	OUT	+12V/+24V
14	GPO11	OUT	+12V/+24V
15	GPO12	OUT	+12V/+24V
16	GPO13	OUT	+12V/+24V
17	GPO14	OUT	+12V/+24V
18	GPO15	OUT	+12V/+24V
19	NC	NC	
20	PC_GND	GND	

## 2.8 Block Diagrams

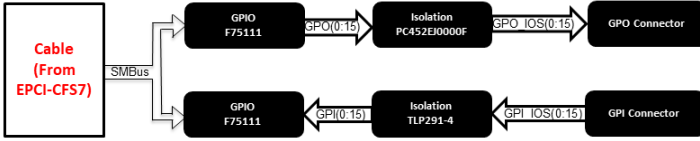
### EPIC-CFS7 Block Diagram



### CFS7\_POE A0.1 Block Diagram



### EPIC-CFS7-DIO A0.2 Block Diagram



# Chapter 3

---

BIOS Setup

## 3.1 System Test and Initialization

---

The EPIC-CFS7-PUC board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System Configuration Verification routines check the current system configuration stored on the CMOS memory and BIOS NVRAM. If the system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup System Configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The EPIC-CFS7-PUC CMOS memory has an integral lithium battery backup for data retention. You will need to replace the complete unit when it runs down.

## 3.2 AMI BIOS Setup

---

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in a battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

To enter setup, power on the computer and press <Del> or <ESC> immediately. The following are short descriptions of each submenu:

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Enable/ Disable boot options for legacy network devices

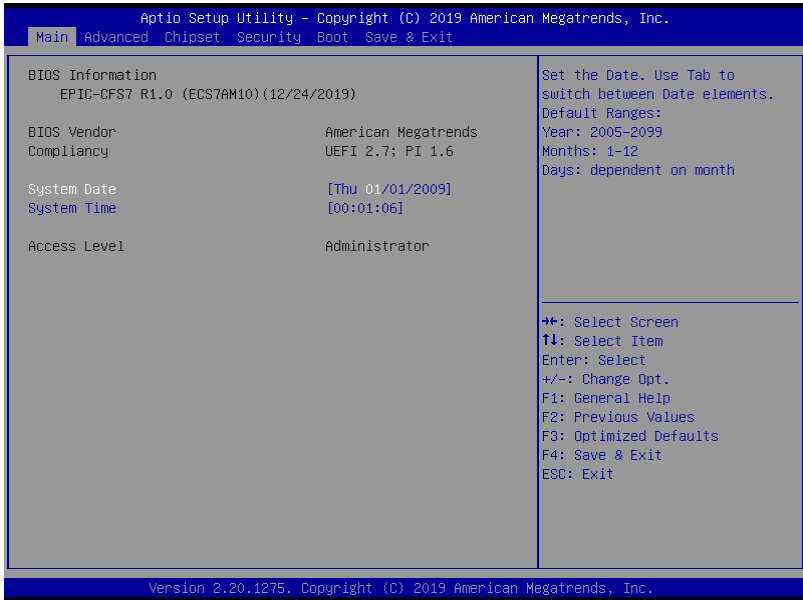
**Chipset** – Host bridge parameters

**Security** – The setup administrator password can be set here

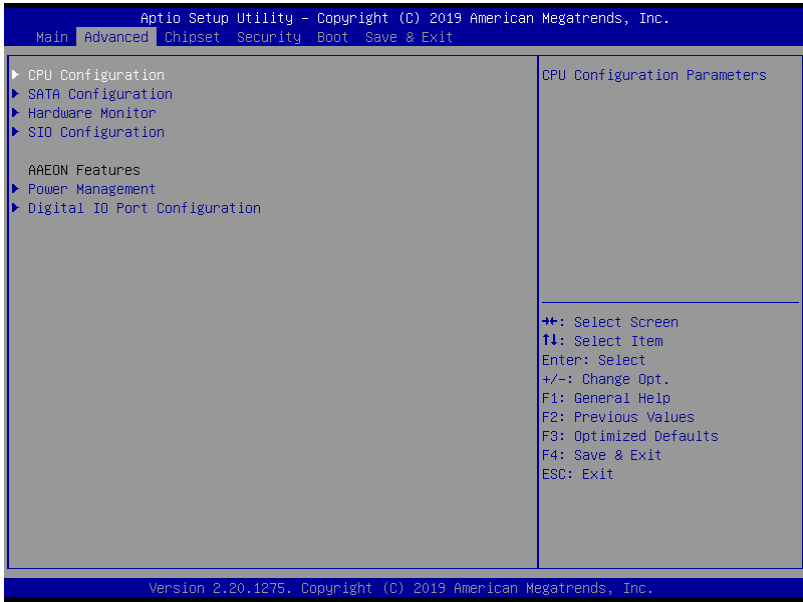
**Boot** – Enable/ Disable Quiet Boot option

**Save & Exit** – Save your changes and exit system setup

### 3.3 Setup Submenu: Main

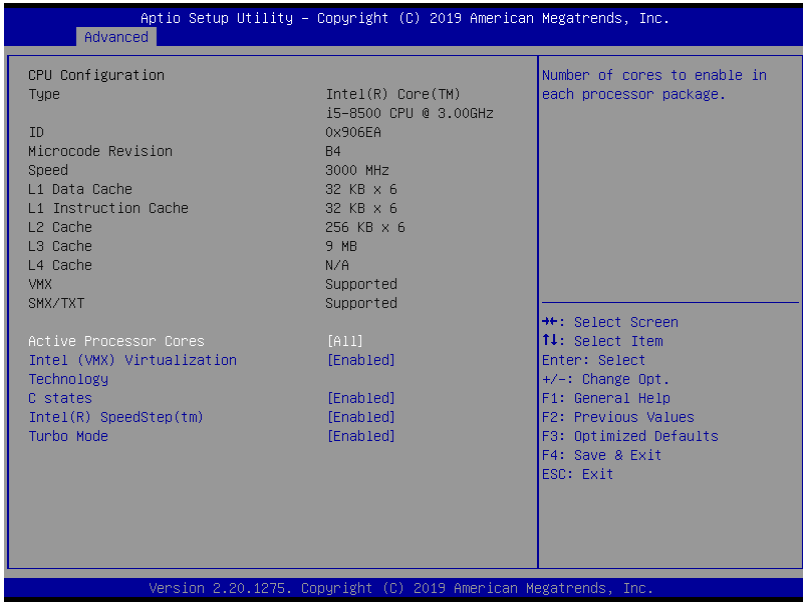


### 3.4 Setup Submenu: Advanced



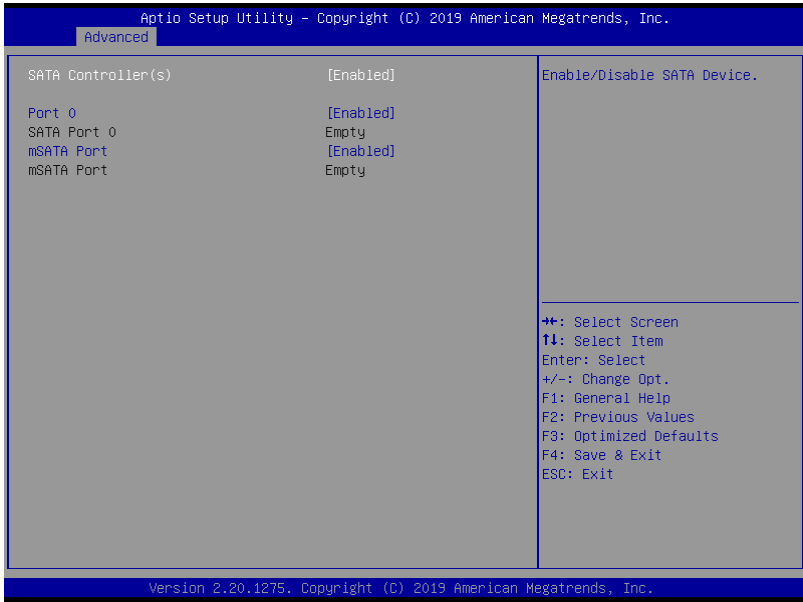


### 3.4.1 CPU Configuration



Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
Number of cores to enable in each processor package.		
Intel (VMX) Virtualization Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
C-States	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable C States.		
Intel(R) SpeedStep(tm)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).		

### 3.4.2 SATA Configuration



Options Summary		
SATA Controller(s)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable SATA Device.		
Port 0	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SATA Port		
mSATA port	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SATA Port		

### 3.4.3 Hardware Monitor

Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

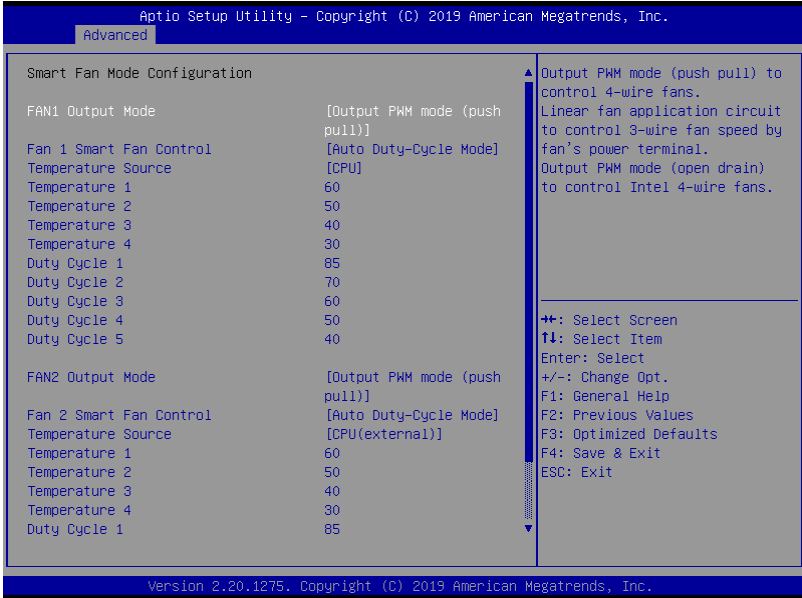
Advanced

<p>Pc Health Status</p> <p>CPU(external) Temperature : +38 % System Temperature : +30 % CPU Temperature : +61 % Fan1 Speed : N/A Fan2 Speed : 2487 RPM VDDRE : +0.960 V +12V : +11.704 V +5V : +5.045 V VMEM : +1.224 V +3.3V : +3.312 V VSB3V : +3.328 V +5VSB : +4.896 V VBAT : +2.752 V</p> <p>Smart Fan [Enabled] ▶ Smart Fan Mode Configuration</p>	<p>Enable or Disable Smart Fan</p> <p>←+: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save &amp; Exit ESC: Exit</p>
--	--

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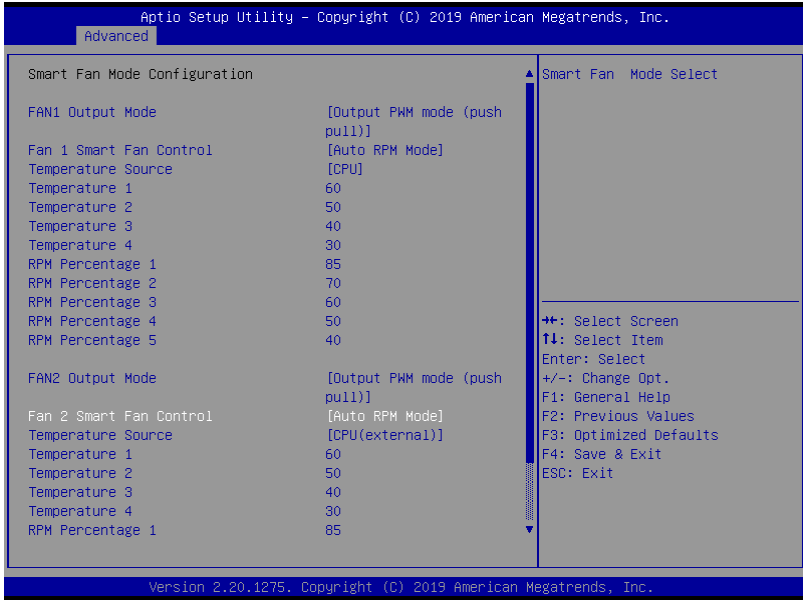
### 3.4.3.1 Smart Fan Mode Configuration

#### Auto Duty-Cycle Mode



Options Summary		
<b>FAN1 Output Mode</b>	Output PWM mode (open drain)	Optimal Default, Failsafe Default
	Linear Fan Application	
	Output PWM mode (push pull)	
Output PWM mode (push pull) to control 4-wire fans. Linear fan application circuit to control 3-wire fan speed by fan's power terminal. Output PWM mode (open drain) to control Intel 4-wire fans.		
<b>Fan Mode</b>	Auto RPM Mode	Optimal Default, Failsafe Default
	Auto Duty-Cycle Mode	
Smart Fan Mode Select		
<b>Temperature Source</b>	CPU	Optimal Default, Failsafe Default
	CPU (external)	
	System	
Select the monitored temperature source for this fan.		
<b>Duty Cycle</b>	Auto fan speed control. Fan speed will follow different temperature	
<b>Temperature</b>	by different duty cycle 1-100	

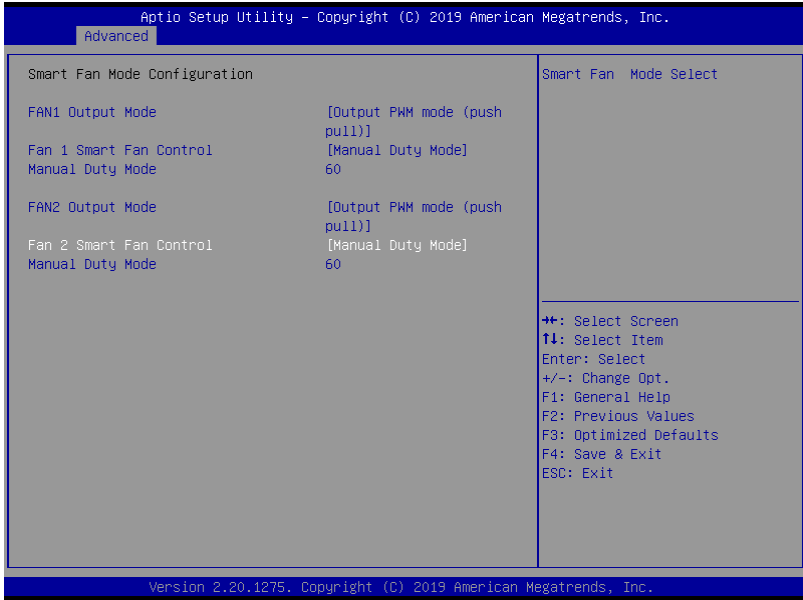
## Auto RPM Mode



### Options Summary

RPM Percentage	Auto fan speed control. Fan speed will follow different temperature by different RPM 1-100
Temperature	

## Manual Duty Mode

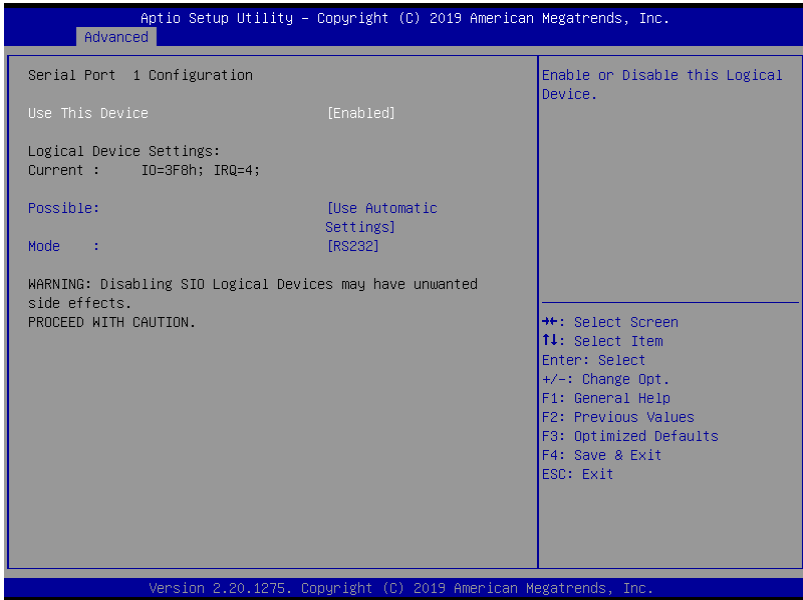


Options Summary		
Manual Duty Mode	60	Optimal Default, Failsafe Default
Manual mode fan control, user can write expected duty cycle (PWM fan type) 1-100		

### 3.4.4 SIO Configuration



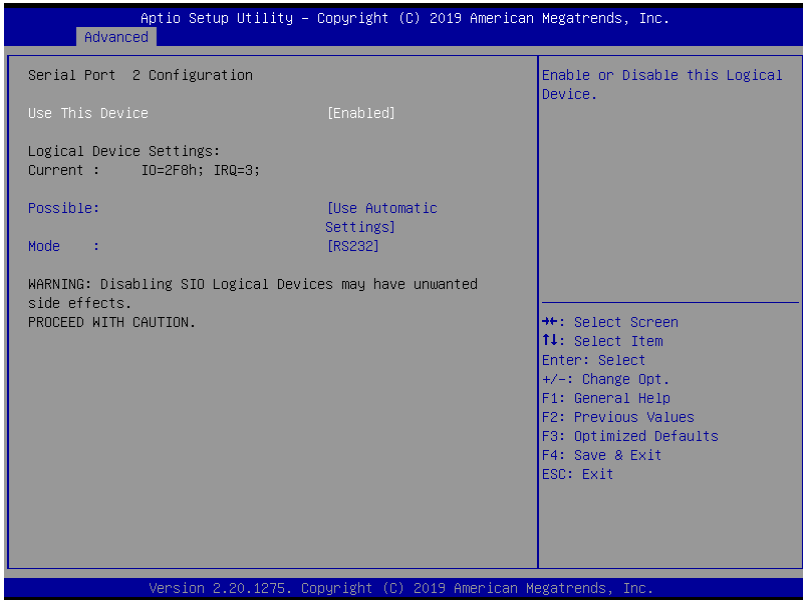
### 3.4.4.1 Serial Port 1 Configuration



Options Summary		
Use This Device	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4	
	IO=2F8h; IRQ=3	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

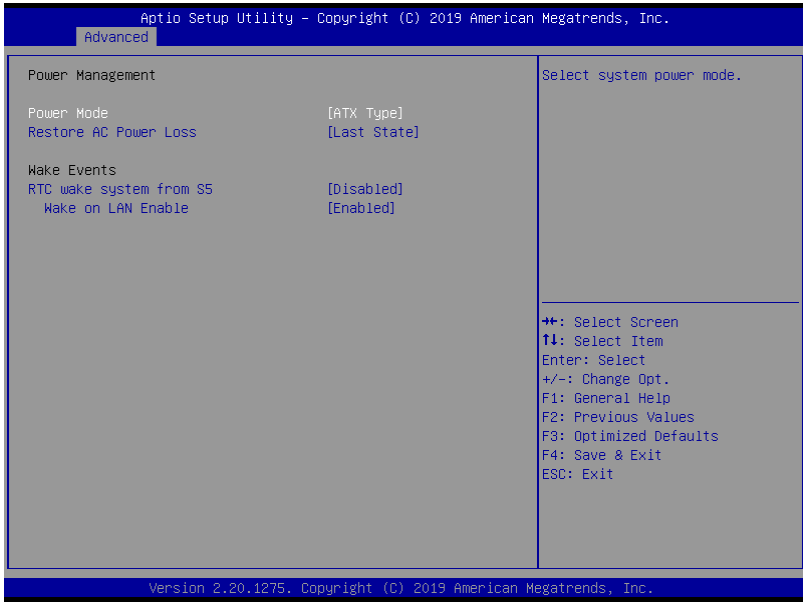


### 3.4.4.2 Serial Port 2 Configuration



Options Summary		
Use This Device	Disable	Optimal Default, Failsafe Default
	Enable	
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3	
	IO=3F8h; IRQ=4	
Allows user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		
Mode	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

### 3.4.5 Power Management



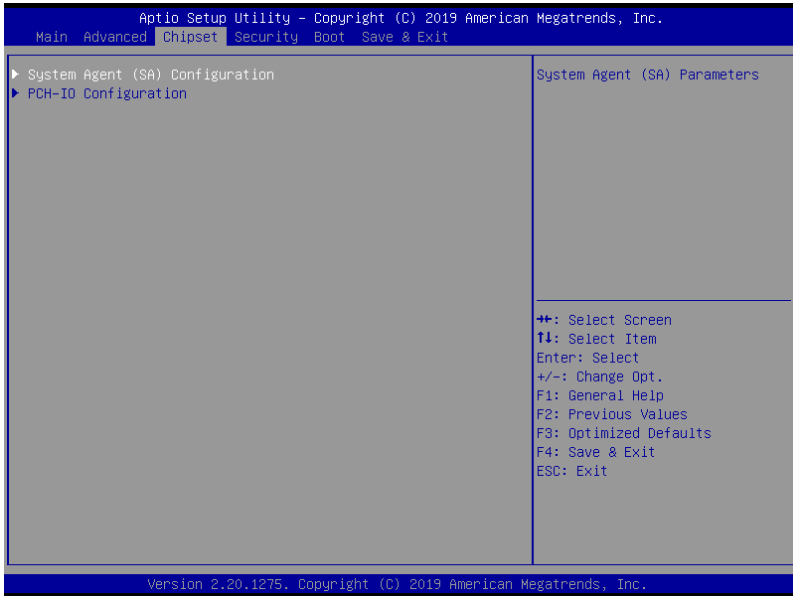
Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Always On	
	Always Off	
IO Restore AC power Loss		
RTC wake system from S5	Disable	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Fixed Time: System will wake on the hr::min::sec specified./n Dynamic Time: System will wake on the current time + Increase minute(s)		
Wake on LAN Enable	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable integrated LAN to wake the system.		

### 3.4.6 Digital IO Port Configuration



Options Summary		
DIO Port*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output		

### 3.5 Setup Submenu: Chipset



### 3.5.1 System Agent (SA) Configuration

The screenshot displays the Aptio Setup Utility interface for the Chipset section. The title bar reads "Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc." and the sub-header is "Chipset".

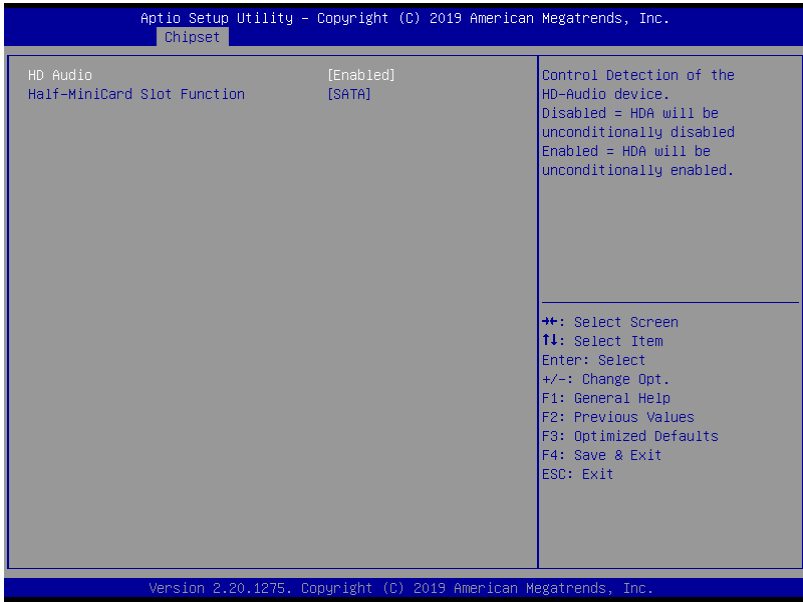
Memory Configuration	
Memory Frequency	2133 MHz
Channel 0 Slot 0	Populated & Enabled
Size	16384 MB (DDR4)
Number of Ranks	2
Manufacturer	Transcend
Channel 1 Slot 0	Not Populated / Disabled

Legend:

- +/: Select Screen
- ↑↓: Select Item
- Enter: Select
- +/-: Change Opt.
- F1: General Help
- F2: Previous Values
- F3: Optimized Defaults
- F4: Save & Exit
- ESC: Exit

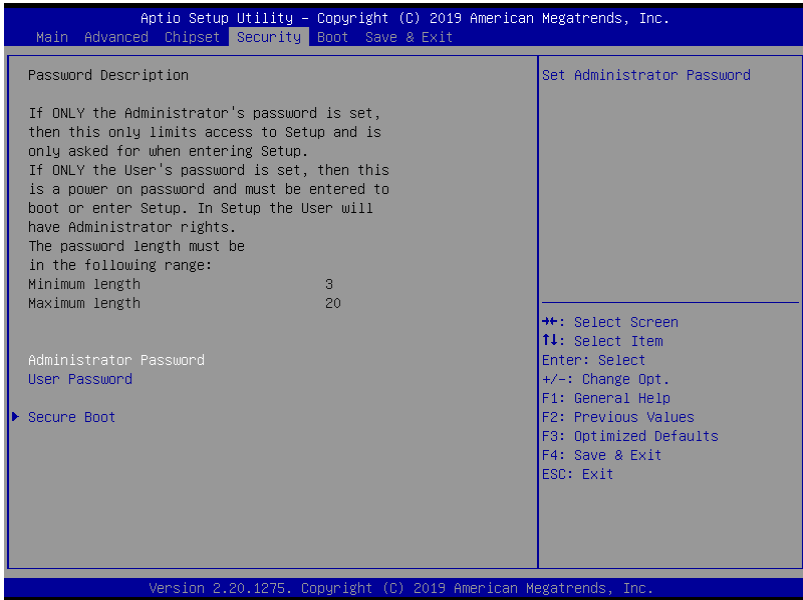
Version 2.20.1275. Copyright (C) 2019 American Megatrends, Inc.

### 3.5.2 PCH-IO Configuration



Options Summary		
HD Audio	Disabled	Optimal Default, Failsafe Default
	Enabled	
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		
MiniCard Slot Function	SATA	Optimal Default, Failsafe Default
	PCIe	
Select function enabled for Half-MiniCard (CN20) slot		

## 3.6 Setup Submenu: Security



### Change User/Administrator Password

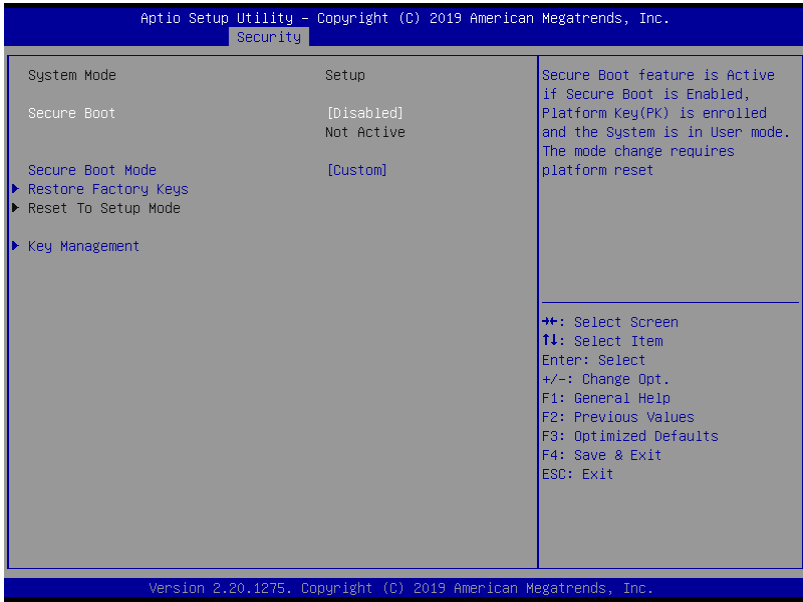
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

### Removing the Password

Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

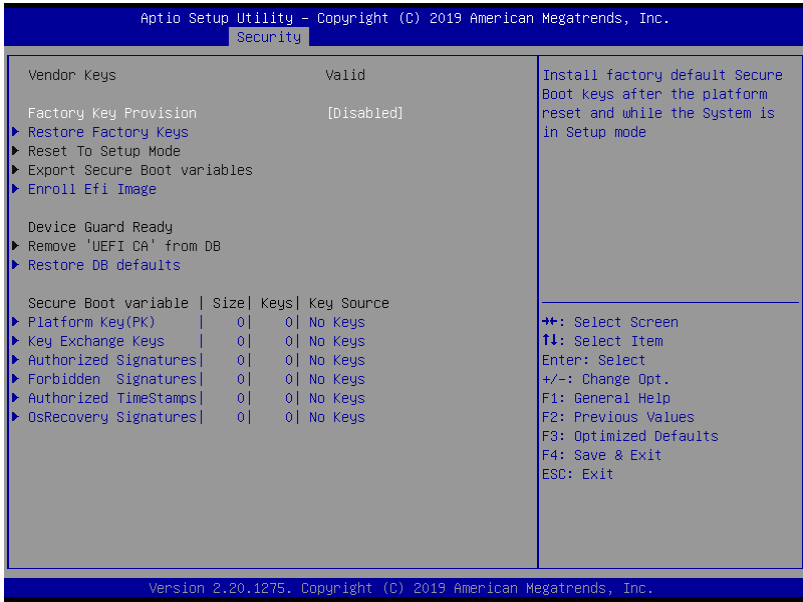
### 3.6.1 Secure Boot



Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		



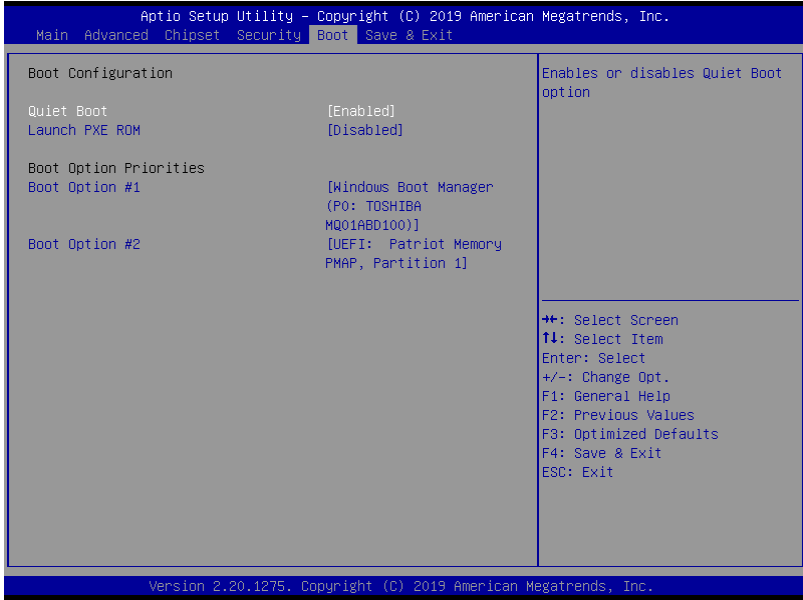
### 3.6.1.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases		
Reset To Setup Mode		
Delete all Secure Boot key databases from NVRAM		
Export Secure Boot variables		
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device		
Enroll Efi Image		
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		
Remove 'UEFI CA' from DB		
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)		

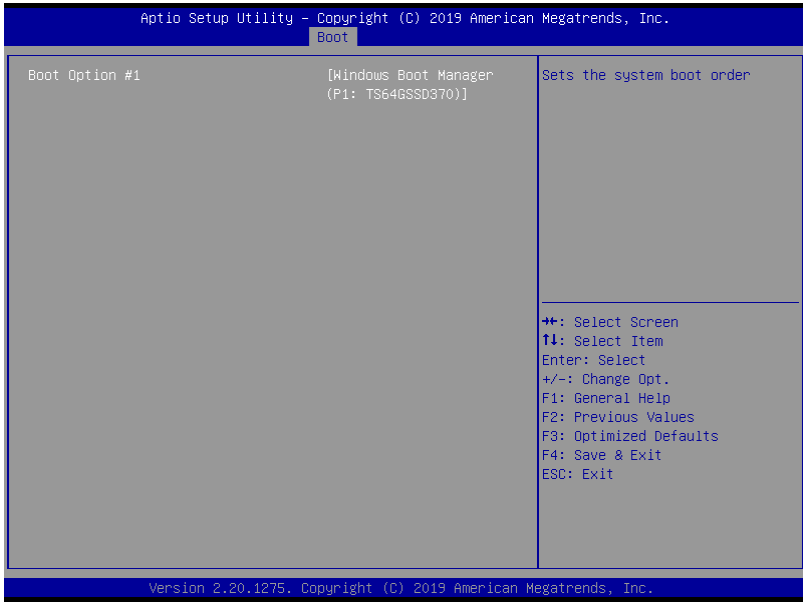
Options Summary	
Restore DB defaults	
Restore DB variable to factory defaults	
Platform Key(PK)	Details
	Export
	Update
	Delete
Key Exchange Keys	Details
	Export
	Update
	Append
Authorized Signatures	Delete
	Details
	Export
	Update
Forbidden Signatures	Append
	Delete
	Details
	Export
Authorized TimeStamps	Update
	Append
	Update
	Append
OsRecovery Signatures	Update
	Append
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed	

### 3.7 Setup Submenu: Boot

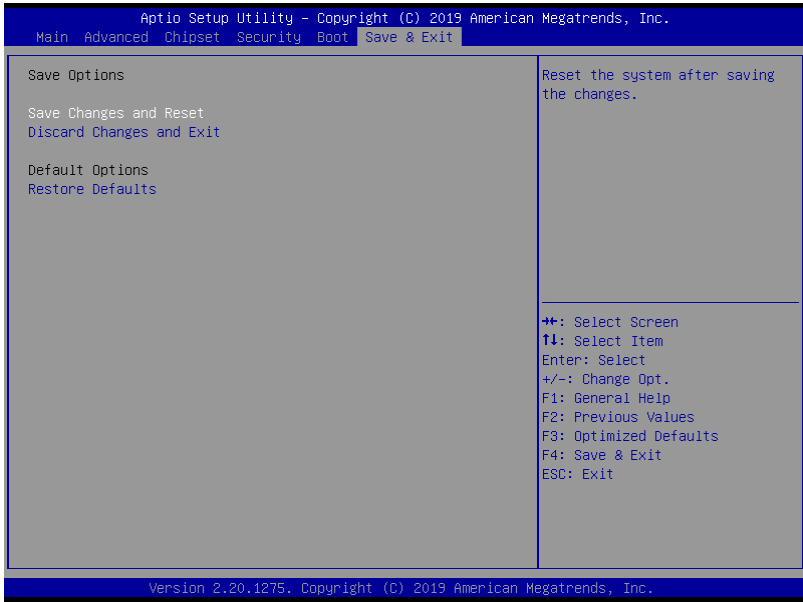


Options Summary		
Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or disable showing boot logo.		
Lunch PXE ROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy Network OpROM		

### 3.7.1 BBS Priorities



### 3.8 Setup Submenu: Save & Exit



# Chapter 4

---

Driver Installation

## 4.1 Driver Installation

Drivers for the EPIC-CFS7-PUC can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/p/epic-boards-epic-CFS7-PUC>

Download the driver(s) you need and follow the steps below to install them.

Before beginning installation, use the following chart to determine if your operating system (OS) is compatible with the drivers AAEON provides for the EPIC-CFS7-PUC. Some drivers are limited in their compatibility and will only work with certain operating systems. If you have any questions, contact your AAEON sales representative for assistance.

OS Compatibility Table		
Driver	Windows 10 64 bit	Linux
Step 1 – Chipset	Yes	No
Step 2 – Graphics	Yes	No
Step 3 – Network	Yes	No
Step 4 – ME	Yes	No

### Step 1 – Install Chipset Drivers

1. Open the **Step 1 – Chipset** folder
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

## Step 2 – Install Graphics Drivers

1. Open the **Step 2 - Graphic** folder
2. Open the **win64\_25.20.100.6373.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

## Step 3 – Install Network Drivers

1. Open the **Step 3 – Network** folder
2. Open the **ProWinx64.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

## Step 4 – Install ME Drivers

1. Open the **Step 4 – ME** folder
2. Open the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically




























# Appendix A






















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I/O Information

## A.1 I/O Address Map

Input/output (IO)	
[0000000000000000 - 000000000000CF7]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000050 - 0000000000000053]	System timer
[0000000000000061 - 0000000000000061]	Motherboard resources
























	[0000000000000063 - 0000000000000063]	Motherboard resources
	[0000000000000065 - 0000000000000065]	Motherboard resources
	[0000000000000067 - 0000000000000067]	Motherboard resources
	[0000000000000070 - 0000000000000070]	Motherboard resources
	[0000000000000080 - 0000000000000080]	Motherboard resources
	[0000000000000092 - 0000000000000092]	Motherboard resources
	[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
	[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
	[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
	[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
	[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
	[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
	[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
	[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
	[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
	[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
	[00000000000000B2 - 00000000000000B3]	Motherboard resources
	[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
	[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
	[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
	[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
	[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
	[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
	[00000000000000F0 - 00000000000000F0]	Numeric data processor
	[00000000000000F0 - 00000000000000F0]	Numeric data processor


























	[00000000000002F8 - 00000000000002FF]	Communications Port (COM2)
	[00000000000003F8 - 00000000000003FF]	Communications Port (COM1)
	[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
	[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
	[0000000000000680 - 000000000000069F]	Motherboard resources
	[0000000000000A00 - 0000000000000A0F]	Motherboard resources
	[0000000000000A10 - 0000000000000A1F]	Motherboard resources
	[0000000000000A20 - 0000000000000A2F]	Motherboard resources
	[0000000000000D00 - 000000000000FFFF]	PCI Express Root Complex
	[000000000000164E - 000000000000164F]	Motherboard resources
	[0000000000001800 - 00000000000018FE]	Motherboard resources
	[0000000000001854 - 0000000000001857]	Motherboard resources
	[0000000000001854 - 0000000000001857]	Motherboard resources
	[0000000000002000 - 00000000000020FE]	Motherboard resources
	[0000000000003000 - 0000000000003FFF]	Intel(R) PCI Express Root Port #7 - A33E
	[0000000000004000 - 0000000000004FFF]	Intel(R) PCI Express Root Port #6 - A33D
	[0000000000005000 - 000000000000503F]	Intel(R) UHD Graphics 630
	[0000000000005060 - 000000000000507F]	Standard SATA AHCI Controller
	[0000000000005080 - 0000000000005083]	Standard SATA AHCI Controller
	[0000000000005090 - 0000000000005097]	Standard SATA AHCI Controller
	[000000000000EFA0 - 000000000000EFBF]	Intel(R) SMBus - A323

## A.2 Memory Address Map

Memory	
[0000000000A0000 - 0000000000BFFFF]	PCI Express Root Complex
[0000000040000000 - 00000000403FFFFF]	Motherboard resources
[0000000090000000 - 000000009FFFFFFF]	Intel(R) UHD Graphics 630
[0000000090000000 - 00000000DFFFFFFF]	PCI Express Root Complex
[00000000A0000000 - 00000000A0FFFFFFF]	Intel(R) UHD Graphics 630
[00000000A1100000 - 00000000A11FFFFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000A1100000 - 00000000A11FFFFF]	Intel(R) PCI Express Root Port #7 - A33E
[00000000A1120000 - 00000000A1123FFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000A1200000 - 00000000A121FFFFF]	Intel(R) I211 Gigabit Network Connection
[00000000A1200000 - 00000000A12FFFFF]	Intel(R) PCI Express Root Port #6 - A33D
[00000000A1220000 - 00000000A1223FFF]	Intel(R) I211 Gigabit Network Connection
[00000000A1300000 - 00000000A130FFFFF]	Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
[00000000A1314000 - 00000000A1315FFF]	Standard SATA AHCI Controller
[00000000A1318000 - 00000000A13180FF]	Intel(R) SMBus - A323
[00000000A1319000 - 00000000A13197FF]	Standard SATA AHCI Controller
[00000000A131A000 - 00000000A131A0FF]	Standard SATA AHCI Controller
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000FC800000 - 00000000FE7FFFFF]	PCI Express Root Complex
[00000000FD000000 - 00000000FD69FFFFF]	Motherboard resources
[00000000FD6A0000 - 00000000FD6AFFFFF]	Intel(R) Serial IO GPIO Host Controller - INT3450
[00000000FD6B0000 - 00000000FD6BFFFFF]	Intel(R) Serial IO GPIO Host Controller - INT3450
[00000000FD6C0000 - 00000000FD6CFFFFF]	Motherboard resources
[00000000FD6D0000 - 00000000FD6DFFFFF]	Intel(R) Serial IO GPIO Host Controller - INT3450
[00000000FD6E0000 - 00000000FD6EFFFFF]	Intel(R) Serial IO GPIO Host Controller - INT3450
[00000000FD6F0000 - 00000000FD6FFFFF]	Motherboard resources
[00000000FE000000 - 00000000FE01FFFFF]	Motherboard resources
[00000000FE010000 - 00000000FE010FFF]	Intel(R) SPI (flash) Controller - A324
[00000000FE0FB000 - 00000000FE0FBFFF]	Intel(R) Management Engine Interface
[00000000FE0FC000 - 00000000FE0FFFFF]	High Definition Audio Controller
[00000000FE100000 - 00000000FE11FFFFF]	High Definition Audio Controller
[00000000FE200000 - 00000000FE77FFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED10000 - 00000000FED17FFF]	Motherboard resources
[00000000FED18000 - 00000000FED18FFF]	Motherboard resources
[00000000FED19000 - 00000000FED19FFF]	Motherboard resources
[00000000FED20000 - 00000000FED33FFF]	Motherboard resources
[00000000FED45000 - 00000000FED8FFFFF]	Motherboard resources
[00000000FED90000 - 00000000FED93FFF]	Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFF]	Motherboard resources
[00000000FF000000 - 00000000FFFFFFFFF]	Motherboard resources

## A.3 IRQ Mapping Chart

▼		Interrupt request (IRQ)
		(ISA) 0x00000000 (00) System timer
		(ISA) 0x00000000 (00) System timer
		(ISA) 0x00000003 (03) Communications Port (COM2)
		(ISA) 0x00000004 (04) Communications Port (COM1)
		(ISA) 0x0000000D (13) Numeric data processor
		(ISA) 0x0000000D (13) Numeric data processor
		(ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3450
		(ISA) 0x00000037 (55) Microsoft ACPI-Compliant System
		(ISA) 0x00000038 (56) Microsoft ACPI-Compliant System
		(ISA) 0x00000039 (57) Microsoft ACPI-Compliant System
		(ISA) 0x0000003A (58) Microsoft ACPI-Compliant System
		(ISA) 0x0000003B (59) Microsoft ACPI-Compliant System
		(ISA) 0x0000003C (60) Microsoft ACPI-Compliant System
		(ISA) 0x0000003D (61) Microsoft ACPI-Compliant System
		(ISA) 0x0000003E (62) Microsoft ACPI-Compliant System
		(ISA) 0x0000003F (63) Microsoft ACPI-Compliant System
		(ISA) 0x00000040 (64) Microsoft ACPI-Compliant System
		(ISA) 0x00000041 (65) Microsoft ACPI-Compliant System
		(ISA) 0x00000042 (66) Microsoft ACPI-Compliant System
		(ISA) 0x00000043 (67) Microsoft ACPI-Compliant System
		(ISA) 0x00000044 (68) Microsoft ACPI-Compliant System
		(ISA) 0x00000045 (69) Microsoft ACPI-Compliant System

	(ISA) 0x000001FE (510)	Microsoft ACPI-Compliant System
	(ISA) 0x000001FF (511)	Microsoft ACPI-Compliant System
	(PCI) 0x00000010 (16)	High Definition Audio Controller
	(PCI) 0xFFFFF9E9 (-23)	Intel(R) Management Engine Interface
	(PCI) 0xFFFFF9EA (-22)	Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
	(PCI) 0xFFFFF9EB (-21)	Intel(R) UHD Graphics 630
	(PCI) 0xFFFFF9EC (-20)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9ED (-19)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9EE (-18)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9EF (-17)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9F0 (-16)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9F1 (-15)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9F2 (-14)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9F3 (-13)	Intel(R) I211 Gigabit Network Connection
	(PCI) 0xFFFFF9F4 (-12)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9F5 (-11)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9F6 (-10)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9F7 (-9)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9F8 (-8)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9F9 (-7)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9FA (-6)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9FB (-5)	Intel(R) I211 Gigabit Network Connection #2
	(PCI) 0xFFFFF9FC (-4)	Standard SATA AHCI Controller
	(PCI) 0xFFFFF9FD (-3)	Intel(R) PCI Express Root Port #7 - A33E
	(PCI) 0xFFFFF9FE (-2)	Intel(R) PCI Express Root Port #6 - A33D

# Appendix B

---

## Watchdog Timer Programming



## B.1 Watchdog Timer Registers

Table 1 : Watch dog relative IO address

	Default Value	Note
I/O Base Address	0x2E	I/O Base address for Watchdog operation. This address is assigned by SIO LDN7

Table 2 : Watchdog relative register table

Register	Offset	BitNum	Value	Note
Watchdog WDRST# Enable	0x00	7	1	Enable/Disable time out output via WDRST# 0: Disable 1: Enable
Pulse Width	0x05	0:1	01	Width of Pulse signal 00: 1ms (do not use) 01: 25ms 10: 125ms 11: 5s <b><i>Pulse width is must longer then 16ms.</i></b>
Signal Polarity	0x05	2	0	0: low active 1: high active <b><i>Must set this bit to 0</i></b>
Counting Unit	0x05	3	0	Select time unit. 0: second 1: minute
Output Signal Type	0x05	4	1	0: Level 1: Pulse <b><i>Must set this bit to 1</i></b>
Watchdog Timer Enable	0x05	5	1	0: Disable 1: Enable
Timeout Status	0x05	6	1	1: timeout occurred. Write a 1 to clear timeout status
Timer Counter	0x06			Time of watchdog timer (0~255)

## B.2 Watchdog Sample Program

```
*****
// WDT I/O operation relative definition (Please reference to Table 1)
#define WDTAddr 0x510 // WDT I/O base address
Void WDTWriteByte(byte Register, byte Value);
byte WDTReadByte(byte Register);
Void WDTSetReg(byte Register, byte Bit, byte Val);
// Watch Dog relative definition (Please reference to Table 2)
#define DevReg 0x00 // Device configuration register
    #define WDRstBit 0x80 // Watchdog WDTRST# (Bit7)
    #define WDRstVal 0x80 // Enabled WDTRST#
#define TimerReg 0x05 // Timer register
    #define PSWidthBit 0x00 // WDTRST# Pulse width (Bit0:1)
    #define PSWidthVal 0x01 // 25ms for WDTRST# pulse
    #define PolarityBit 0x02 // WDTRST# Signal polarity (Bit2)
    #define PolarityVal 0x00 // Low active for WDTRST#
    #define UnitBit 0x03 // Unit for timer (Bit3)
    #define ModeBit 0x04 // WDTRST# mode (Bit4)
    #define ModeVal 0x01 // 0:level 1: pulse
    #define EnableBit 0x05 // WDT timer enable (Bit5)
    #define EnableVal 0x01 // 1: enable
    #define StatusBit 0x06 // WDT timer status (Bit6)
#define CounterReg 0x06 // Timer counter register
*****

*****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Counter of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    EnterSIOconfig();
    SetWDT();
    AaeonWDTConfig(Counter, Unit);
    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
    ExitSIOconfig();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID EnterSIOconfig 0{
    IOWriteByte (IoConfAddr,0x87);
    IOWriteByte (IoConfAddr,0x87);
}

VOID ExitSIOconfig 0{
    IOWriteByte (IoConfAddr,0xAA);
}

VOID SetWDT 0
    IOWriteByte (IoConfAddr,0x2B);
    IOWriteByte(IoConfAddr+1, (IOReadByte(IoConfAddr+1)&0xFC));
}

// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable 0{
    WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (byte Counter, BOOLEAN Unit){
    // Disable WDT counting
    WDTEnableDisable(0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting(Timer, Unit);
}

VOID WDTEnableDisable(byte Value){
    If (Value == 1)
        WDTSetBit(TimerReg, EnableBit, 1);
    else
        WDTSetBit(TimerReg, EnableBit, 0);
}

VOID WDTParameterSetting(byte Counter, BOOLEAN Unit){
    // Watchdog Timer counter setting
    WDTWriteByte(CounterReg, Counter);
    // WDT counting unit setting

```

```

    WDTSetBit(TimerReg, UnitBit, Unit);
    // WDT output mode set to pulse
    WDTSetBit(TimerReg, ModeBit, ModeVal);
    // WDT output mode set to active low
    WDTSetBit(TimerReg, PolarityBit, PolarityVal);
    // WDT output pulse width is 25ms
    WDTSetBit(TimerReg, PSWidthBit, PSWidthVal);
    // Watchdog WDRST# Enable
    WDTSetBit(DevReg, WDRstBit, WDRstVal);
}

VOID WDTClearTimeoutStatus(){
    WDTSetBit(TimerReg, StatusBit, 1);
}
*****

*****

VOID WDTWriteByte(byte Register, byte Value){
    IOWriteByte(WDTAddr+Register, Value);
}

byte WDTReadByte(byte Register){
    return IOReadByte(WDTAddr+Register);
}

VOID WDTSetBit(byte Register, byte Bit, byte Val){
    byte TmpValue;

    TmpValue = WDTReadByte(Register);
    TmpValue &= ~(1 << Bit);
    TmpValue |= Val << Bit;
    WDTWriteByte(Register, TmpValue);
}

*****

```