

# **EMB-H61B**

Manual 1<sup>st</sup> Ed.

December 2012



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## Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 Industrial Motherboard
- 1 SATA Cable
- 1 SATA Power Cable
- 1 Metal I/O Bracket
- 1 DVD-ROM for Manual (in PDF Format) and Drivers

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

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Chapter

1

**General  
Information**

## 1.1 Features

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- Intel® Socket 1155 for 3<sup>rd</sup> /2<sup>nd</sup> Generation Core™ i7/ i5/ i3/ Pentium® / Celeron® Processors  
(Supports Intel® 22/32 nm CPU up to 65W)
- 2 x 204-pin Dual-Channel DDR3 1333/1066MHz SO-DIMM  
Up to 16GB
- Intel® integrated Graphics Engine Supports Dual View by VGA, HDMI x 2, LVDS
- Realtek PCI-Express Gigabit Ethernet x 2
- SATA 3.0Gb/s x 2 & CF Socket x 1 (Supports Both CF-SATA Card and CF Type 1)
- USB 2.0 x 8 & COM x 6
- PCI-Express 2.0 [x4] x 1 & Full-size Mini Card(PCle +USB) + SIM Card x 1
- EuP/ErP Compliance
- 12V DC-in Support
- TPM Module Support



## 1.2 Specifications

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### System

- Processor Intel® 2<sup>nd</sup>/3<sup>rd</sup> generation Core™ i7/i5/i3 Processor, up to 65W
- System Memory 204-pin dual-channel DDR3 1333/1066 SODIMM x 2, Max. 16 GB
- Chipset Intel® H61 (B3)
- I/O Chipset Fintek F81866D-I
- Ethernet Realtek 8111F for 10/100/1000Base-T, RJ-45 x 2
- BIOS AMI BIOS, 64Mb ROM
- Wake On LAN Yes
- Watchdog Timer System reset: 1~255 steps programmable
- TPM Infineon SLB9635 TT 1.2
- H/W Status Monitoring Monitoring System Temperature, Voltage, and Cooling Fan status
- Expansion Interface PCI-Express 2.0 [x4] x 1, Full-size Mini Card(PCIe +USB) + SIM Card x1
- Battery Lithium battery
- Power Requirement 4-pin connector for DC12V input x 1; CPU fan x 1, System fan with 4-pin wafer x 1; SATA power with 4-pin wafer x 1
- Power Compliance Compliant with EuP/ErP
- Board Size 6.7”(L) x 6.7”(W) (170 mm x 170 mm)

- Gross Weight 1.1 lb (0.5 Kg)
- Operating Temperature 32°F ~ 131°F (0°C ~ 55°C)
- Storage Temperature -40°F ~ 185°F (-40°C ~ 85°C)
- Operating Humidity 0% ~ 90% relative humidity, non-condensing
- EMI CE/FCC Class A

### Display

- Chipset Intel® Graphics Media Accelerator
- Resolution Up to 2048x1536 @ 75Hz for VGA;  
Up to 1920x1200 @ 60Hz for HDMI;
- LCD Interface Dual 24-bit for LVDS  
Up to 1920 x 1200 @ 60 Hz
- Output Interface Multi-VGA output support:  
HDMI/ VGA/ LCD

### I/O

- Storage SATA 3.0 Gb/s x 2,  
CF Socket x 1 (Supports Both  
CF-SATA Card and CF Type 1)
- Serial Port RS-232 x 5 (COM2~COM6),  
RS-232/422/485 x 1 (COM1)  
supports 5V/12V/RI option
- USB USB2.0 x 8 (2 ports at mid-board,  
6 ports at back panel)
- Digital I/O Supports 8-bit (4-in/ 4-out)
- PS/2 Port Keyboard/ Mouse x 1
- Audio Audio jack with BTX type x 3  
(Mic-in, Line-out, Line-in)

Chapter

2

**Quick  
Installation  
Guide**

## 2.1 Safety Precautions

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**Warning!**

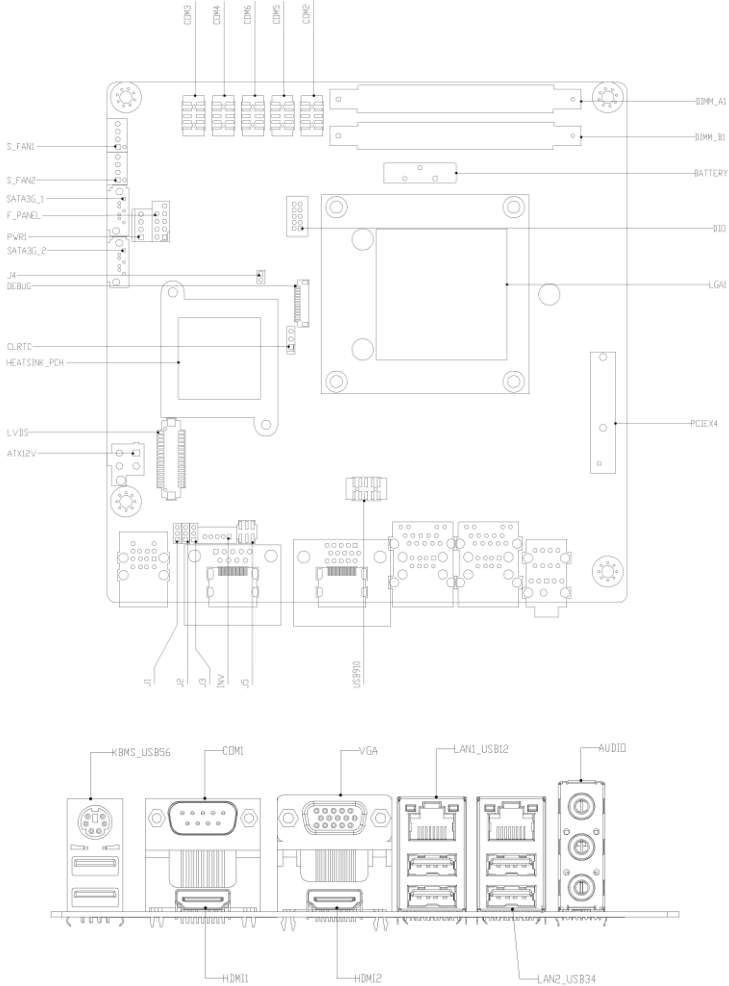
*Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.*

**Caution!**

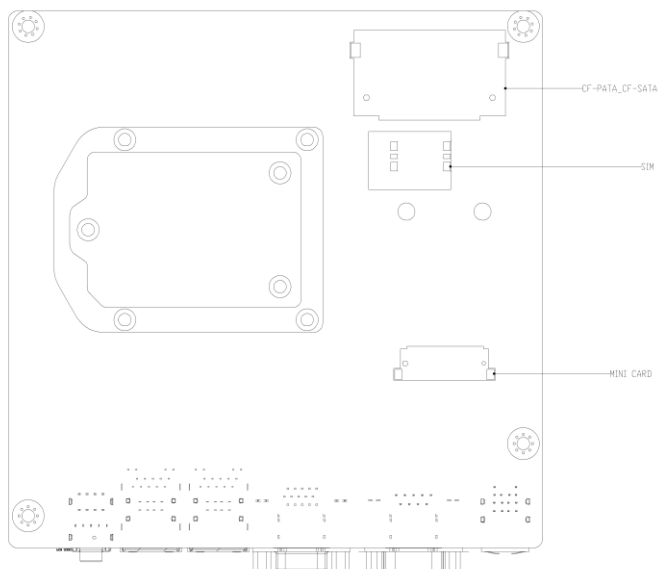
*Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis*

## 2.2 Location of Connectors and Jumpers

### Component Side

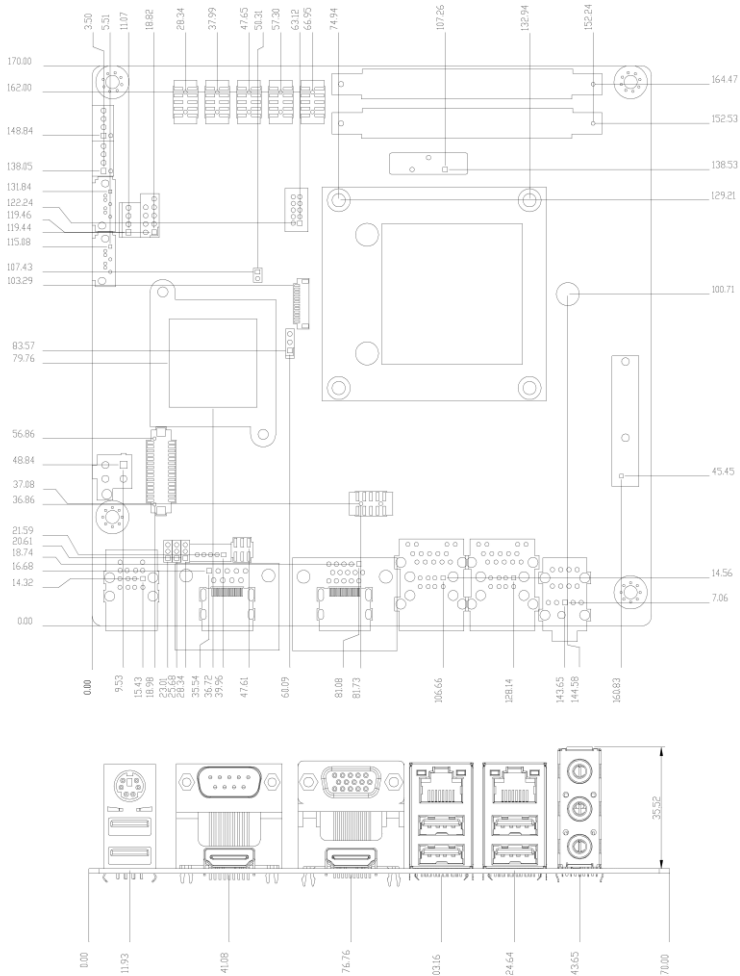


Solder Side

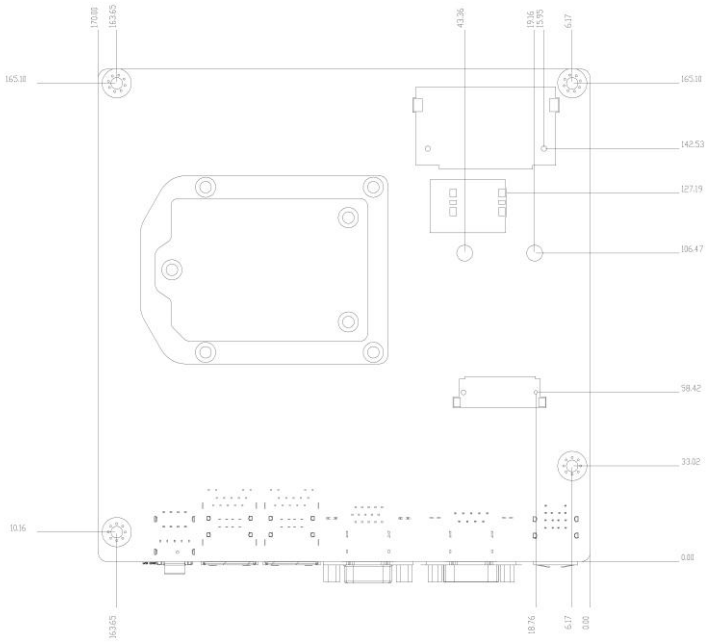


### 2.3 Mechanical Drawing

#### Component Side



Solder Side





## 2.4 List of Jumpers

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The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

<b>Label</b>	<b>Function</b>
CLRTC	Clear CMOS
J1	LVDS Panel Voltage Selection
J2	Inverter Voltage Selection
J3	Mode Selection for Back Light Control of Inverter
J4	AT/ATX mode Selection
J5	COM1 Ring/+5V/+12V Selection

## 2.5 List of Connectors

---

The board has a number of connectors that allow you to configure your system to suit your application.

The table below shows the function of each of the board's connectors:

<b>Label</b>	<b>Function</b>
ATX12V	ATX 4P Power Connector
AUDIO	Audio jack Connector
BATTERY	RTC - Coin Battery Holder
CF-PATA_CF-SATA	CF Socket (Supports Both CF-SATA Card and CF Type 1)
COM1	COM1 Connector
COM2	COM2 Connector
COM3	COM3 Connector
COM4	COM4 Connector

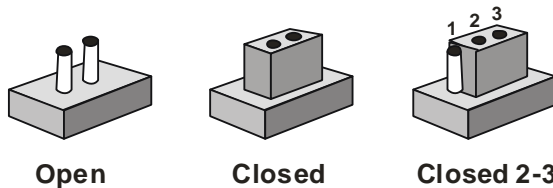
COM5	COM5 Connector
COM6	COM6 Connector
DEBUG	Debug Connector
DIMM_A1	DIMM1 Slot
DIMM_B1	DIMM2 Slot
DIO	Digital I/O Connector
F_PANEL	Front Panel Connector
HDMI1	HDMI Connector
HDMI2	HDMI Connector
INV	Inverter Connector
KBMS_USB56	PS/2 KB&MS and USB5/6 Connector
LAN1_USB12	LAN1 & USB1/2 Connector
LAN2_USB34	LAN2 & USB3/4 Connector
LGA1	CPU Socket - LGA-1155P
LVDS	LVDS Panel Signal Connector
MINICARD	Mini Card socket
PCIEX4	PCI Express x4 Slot
PWR1	SATA Power Connector
S_FAN1	System FAN Connector
S_FAN2	System FAN Connector
SATA3G_1	SATA II Connector
SATA3G_2	SATA II Connector
SIM	SIM Card Socket
USB910	Int. USB 2.0 Connector
VGA	D-Sub15_VGA Connector

## 2.6 Setting Jumpers

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You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

## 2.7 Clear CMOS (CLRTC)

CLRTC	Function
1-2	RTC Batt.
2-3	Clear CMOS

## 2.8 LVDS Panel Voltage Selection (J1)

J1	Function
1-2	+5V
2-3	+3.3V (Default)

## 2.9 Inverter Voltage Selection (J2)

J2	Function
1-2	+12V
2-3	+5V (Default)

## 2.10 Mode Selection for Back Light Control of Inverter (J3)

J3	Function
1-2	DC Voltage Control (Default)
2-3	PWM Control

## 2.11 AT/ATX Mode Selection (J4)

J4	Function
1-2	AT Mode (Default)
Empty	ATX Mode

## 2.12 COM1 Ring/+5V/+12V Selection (J5)

J5	Function
1-2	+12V
3-4	+5V
5-6	Ring (Default)

## 2.13 Internal COM Serial Port Connector (COM2 ~ COM6)

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	(NC)

## 2.14 PS/2 Keyboard/Mouse Connector with Dock USB 2.0 Connector (KBMS\_USB56)

Pin	Signal	Pin	Signal
1	GND	2	USB2_DP1
3	USB2_DN1	4	+5V
5	GND	6	USB2_DP2
7	USB2_DN2	8	+5V
9	GND	10	KB_DATA
11	MS_DATA	12	+5V
13	KB_CLK	14	MS_CLK

15	GND	16	GND
17	GND	18	GND

### 2.15 1000Base-T Ethernet Connector with Dock USB 2.0 Connector (LAN1\_ USB12 / LAN2\_ USB34)

Pin	Signal	Pin	Signal
1	+5V	2	USB2_DN2
3	USB2_DP2	4	GND
5	+5V	6	USB2_DN1
7	USB2_DP1	8	GND
9	LAN_CTR	10	LAN_MDI_DP0
11	LAN_MDI_DN0	12	LAN_MDI_DP1
13	LAN_MDI_DN1	14	LAN_MDI_DP2
15	LAN_MDI_DN2	16	LAN_MDI_DP3
17	LAN_MDI_DN3	18	GND
19	LAN_LED_LINK100#	20	LAN_LED_LINK1000#
21	LAN_LED_ACT#	22	LAN_LED_ACT
23	GND	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

### 2.16 Digital I/O Connector (DIO)

Pin	Signal	Pin	Signal
1	DIO_I#1 (DIO_P#1)	2	DIO_I#2 (DIO_P#2)

3	DIO_I#3 (DIO_P#3)	4	DIO_I#4 (DIO_P#4)
5	DIO_O#1 (DIO_P#5)	6	DIO_O#2 (DIO_P#6)
7	DIO_O#3 (DIO_P#7)	8	DIO_O#4 (DIO_P#8)
9	+5V	10	GND

### 2.17 Front Panel Connector (F\_PANEL)

Pin	Signal	Pin	Signal
1	HDLED+	2	PLED+
3	HDLED-	4	PLED-
5	GND	6	PANSWH#
7	HWRST#	8	GND
9	(NC)	10	(kill pin)

### 2.18 Inverter Connector (INV)

Pin	Signal
1	Inverter VCC
3	Back Light Control
5	GND
7	GND
9	Back Light Enable

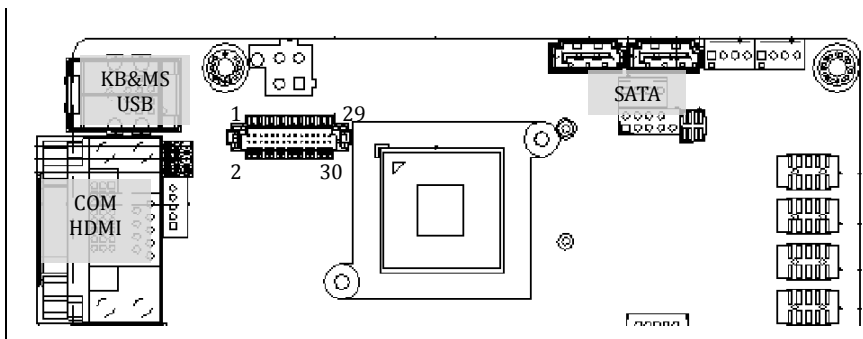
### 2.19 LVDS Panel Signal Connector (LVDS)

Pin	Signal	Pin	Signal
29	LVDS1_CLK-	30	LVDS1_CLK+
27	LVDS VCC	28	GND

25	LVDS1_D3-	26	LVDS1_D3+
23	LVDS1_D2-	24	LVDS1_D2+
21	LVDS1_D1-	22	LVDS1_D1+
19	LVDS1_D0-	20	LVDS1_D0+
17	EDID_Data	18	EDID_Clk
15	LVDS0_D3-	16	LVDS0_D3+
13	LVDS0_D2-	14	LVDS0_D2+
11	LVDS0_D1-	12	LVDS0_D1+
9	LVDS0_D0-	10	LVDS0_D0+
7	LVDS VCC	8	GND
5	LVDS0_CLK-	6	LVDS0_CLK+
3	LVDS VCC	4	GND
1	LVDS Panel Enable	2	Backlight Control for DC mode



**NOTE:** LVDS connector Vendor: PINREX; Model: 712-76-30GWR8. Please refer the drawing below, notice the location of PIN1, PIN2, PIN29 and PIN30.





**2.20 SATA Power Connector (PWR1)**

Pin	Signal
1	+5V
2	GND
3	GND
4	+12V

**2.21 FAN Connector (S\_FAN1 / S\_FAN2)**

Pin	Signal
1	PWM
2	SENSE
3	VCC
4	GND

**2.22 Internal USB 2.0 Connector (USB910)**

Pin	Signal	Pin	Signal
1	+5V	2	GND
3	USB2_DN1	4	GND
5	USB2_DP1	6	USB2_DP2
7	GND	8	USB2_DN2
9	GND	10	+5V

Chapter

3

**AMI  
BIOS Setup**

### 3.1 System Test and Initialization

---

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

#### **System configuration verification**

These routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the program outputs an error message. You will then need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The CMOS memory has lost power and the configuration information has been erased.

The EMB-H61B CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it runs down.

## 3.2 AMI BIOS Setup

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AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM so that it retains the Setup information when the power is turned off.

### Entering Setup

Power on the computer and press <Del> or <F2> immediately. This will allow you to enter Setup.

### Main

Set the date, use tab to switch between date elements.

### Advanced

Advanced BIOS Features Setup including TPM, ACPI, etc.

### Chipset

Host bridge parameters.

### Boot

Enables / disable quiet boot option.

### Security

Set setup administrator password.

### Save & Exit

Exit system setup after saving the changes.

## Setup Menu

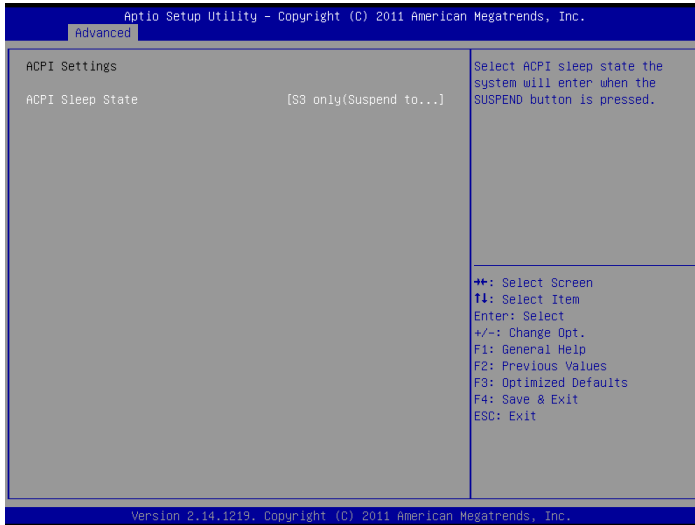
### Setup submenu: Main

Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.	
Main   Advanced   Chipset   Boot   Security   Save & Exit	
BIDS Information R1.2 (H61BAM12) (05/30/2012)	Set the Date. Use Tab to switch between Date elements.
BIDS Vendor Core Version Compliance	American Megatrends 4.6.5.3 x64 UEFI 2.3; PI 1.2
System Date System Time	[Fri 05/01/2012] [11:43:28]
Access Level	Administrator
++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.	

### Setup submenu: Advanced

Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.	
Main   Advanced   Chipset   Boot   Security   Save & Exit	
▶ ACPI Settings ▶ Trusted Computing ▶ S5 RTC Wake Settings ▶ CPU Configuration ▶ Digital ID ▶ SATA Configuration ▶ USB Configuration ▶ F81866 Super IO Configuration ▶ F81866 H/W Monitor	System ACPI Parameters.
++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.14.1219. Copyright (C) 2011 American Megatrends, Inc.	

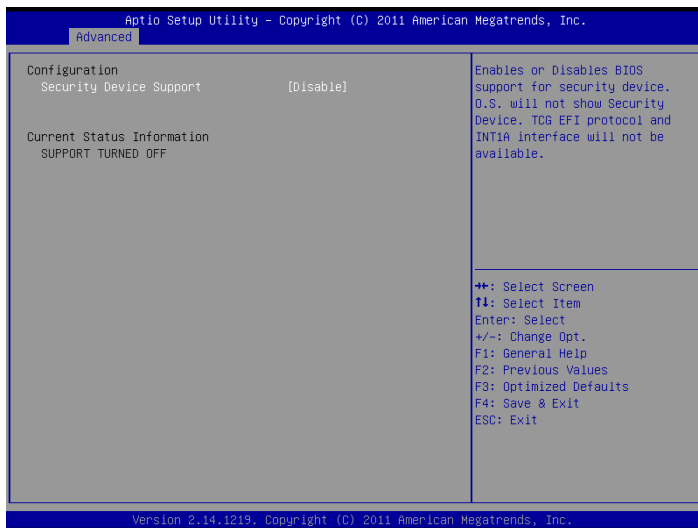
## ACPI Settings



### Options summary :

Suspend mode	S1 (CPU Stop Clock)	Optimal Default, Failsafe Default
	S3 (Suspend to RAM)	
Select the ACPI state used for System Suspend		

## Trusted Computing



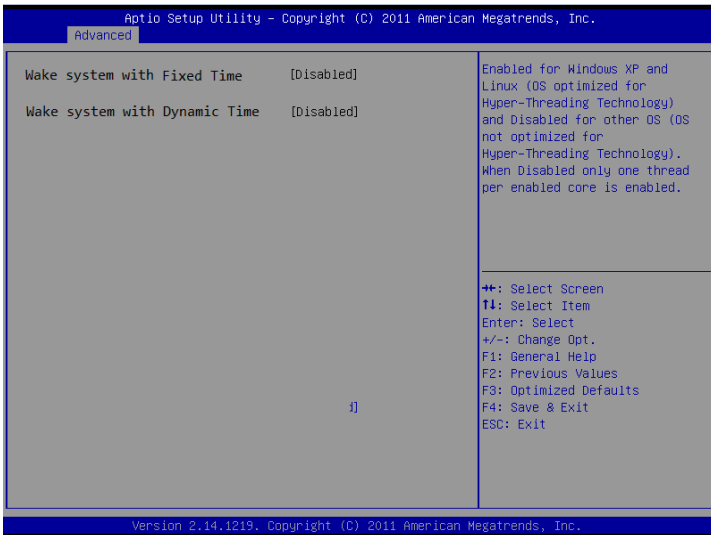
### Options summary:

Security Device Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable TPM support.		
TPM State	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable TPM State.		
Pending Operation	None	Optimal Default, Failsafe Default

	Enable Take Ownership	
	Disable Take Ownership	
	TPM Clear	

Select one-time TPM operation. Item value returns to 'None' after next POST.

### S5 RTC Wake Settings





## CPU Configuration

Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.

Advanced

CPU Configuration		Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only one thread per enabled core is enabled.
Intel(R) Core(TM) i3-3220 CPU @ 3.30GHz		
CPU Signature	306a9	
Microcode Patch	12	
Max CPU Speed	3300 MHz	
Min CPU Speed	1600 MHz	
CPU Speed	3300 MHz	
Processor Cores	2	
Intel HT Technology	Supported	
Intel VT-x Technology	Supported	
Intel SMX Technology	Not Supported	
64-bit	Supported	
L1 Data Cache	32 kB x 2	
L1 Code Cache	32 kB x 2	
L2 Cache	256 kB x 2	
L3 Cache	3072 kB	
Hyper-threading	[Enabled]	
Intel Virtualization Technology	[Disabled]	
		++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Aptio Setup Utility - Copyright (C) 2011 American Megatrends, Inc.

Advanced

CPU Configuration		Turbo Mode should be disabled when using 55W or 65W CPU
Intel(R) Core(TM) i7-3770K CPU @ 3.50GHz		
CPU Signature	306a8	
Microcode Patch	10	
Max CPU Speed	3500 MHz	
Min CPU Speed	1600 MHz	
CPU Speed	3500 MHz	
Processor Cores	4	
Intel HT Technology	Supported	
Intel VT-x Technology	Supported	
Intel SMX Technology	Not Supported	
64-bit	Supported	
L1 Data Cache	32 kB x 4	
L1 Code Cache	32 kB x 4	
L2 Cache	256 kB x 4	
L3 Cache	8192 kB	
Hyper-threading	[Enabled]	
Intel Virtualization Technology	[Disabled]	
Turbo Mode	[Enabled]	
		++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Options summary :

Hyper-Threading	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable CPU Hyper-Threading function		
Intel Virtualization Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Turbo Mode (Turbo mode should be disabled when using 55W or 65W CPU)		
Turbo Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Intel VT-x function		

## Digital IO Configuration

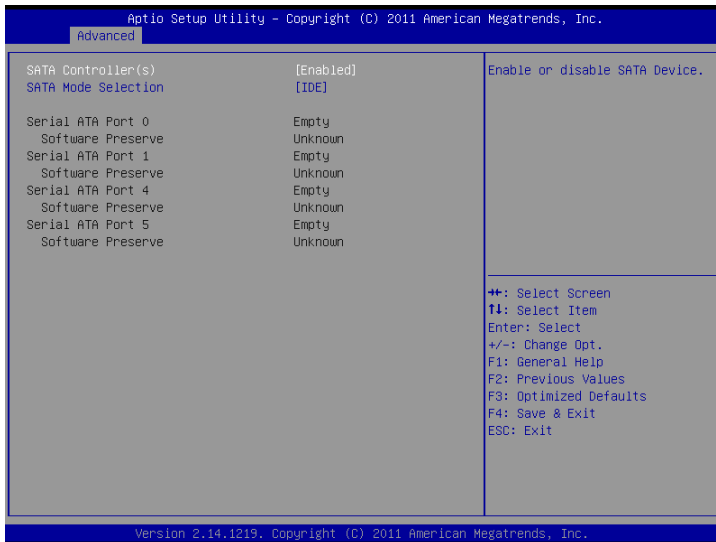


### Options summary :

DIO_P# 1-4	Input	Optimal Default, Failsafe Default
	Output	
Set GPIO as Input or Output		
DIO_P# 5-8	Input	Optimal Default, Failsafe Default
	Output	
Set GPIO as Input or Output		

DIO_P# 1-8	Low	Optimal Default, Failsafe Default
Direction	High	
Set GPIO Output as Hi or Low.		

**SATA Controller(s)**

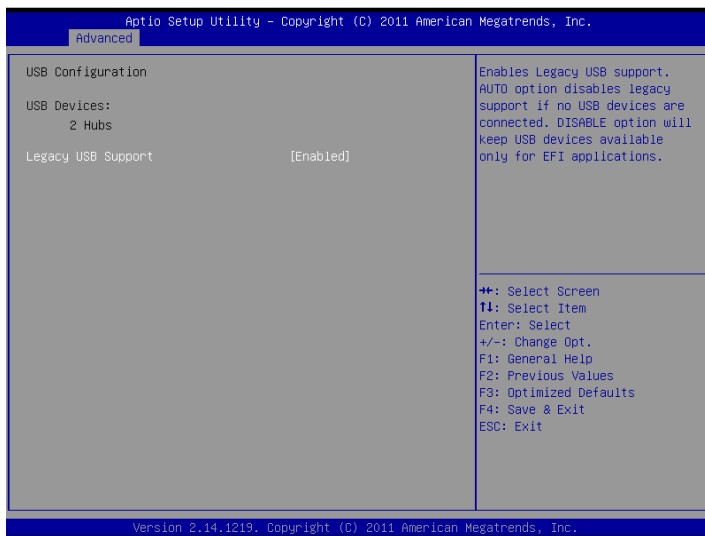


**Options summary :**

SATA Controller(s)	Disabled	Default
	Enabled	
SATA Controller(s)		
SATA Configuration	IDE	Default

	AHCI	
IDE: Configure SATA controllers as legacy IDE		
AHCI: Configure SATA controllers to operate in AHCI mode		
SATA Controller Speed	Gen1	Default
	Gen2	
Select serial ATA Controller Speed		
Port 0, 1, 4, 5	Disabled	Default
	Enabled	
Hot Plug	Disabled	Default
	Enabled	
En/Disable Hot Plug feature.		

## USB Configuration

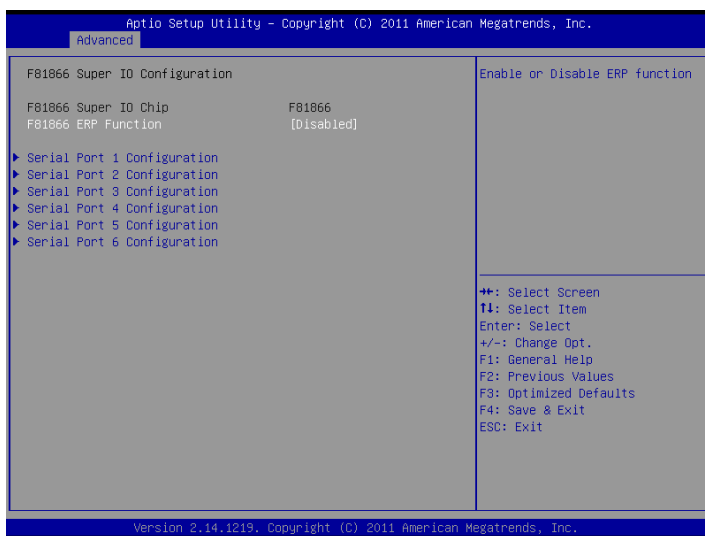


### Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		
Device Name (Emulation Type)	Auto	Optimal Default, Failsafe Default
	Floppy	

	Forced FDD	
	Hard Disk	
	CDROM	
<p>If Auto. USB devices less than 530MB will be emulated as Floppy and remaining as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD(Ex. ZIP drive)</p>		

## F81866 Super IO Configuration



## Serial Port Configuration

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Advanced

Serial Port 1 Configuration		Enable or Disable Serial Port (COM)
Serial Port	[Enabled]	
Device Settings	ID=3F8h; IRQ=4;	
Device Mode	[RS232]	
Change Settings	[Auto]	
		++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Advanced

Serial Port 2 Configuration		Enable or Disable Serial Port (COM)
Serial Port	[Enabled]	
Device Settings	ID=2F8h; IRQ=3;	
Change Settings	[Auto]	
		++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Options summary :

F81866 ERP Function	Disabled	Default
	Enabled	
Enable or Disable ERP function.		
Serial Port	Disabled	Default
	Enabled	
Allows BIOS to En/Disable correspond serial port.		
Device Mode	RS232	Default
	RS422	
	RS485	
Select working model.		
Change Settings (Serial Port 1)	Auto	Default
	IO=3F8h; IRQ=4;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=10,11;	
	IO=2E8h; IRQ=10,11	
Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 2)	Auto	Default
	IO=2F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4;	
	IO=2F8h; IRQ=3,4;	
	IO=3E8h; IRQ=10,11;	

	IO=2E8h; IRQ=10,11	
Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 3)	Auto	Default
	IO=3E8h; IRQ=10,11;	
	IO=2E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11	
Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 4)	Auto	Default
	IO=2E8h; IRQ=10,11;	
	IO=3E8h; IRQ=10,11;	
	IO=2D0h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11;	
Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 5)	Auto	Default
	IO=2D0h; IRQ=10,11;	
	IO=3E8h; IRQ=10,11;	
	IO=2E8h; IRQ=10,11;	
	IO=2D8h; IRQ=10,11	
Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 6)	Auto	Default
	IO=2D8h; IRQ=10,11	
	IO=3E8h; IRQ=10,11;	
	IO=2E8h; IRQ=10,11;	

	IO=2D8h; IRQ=10,11	
Allows BIOS to Select Serial Port resource.		
Device Mode	Disable IR1 function	Default
	Enable IR1 function, active pulse 1.6us	
	Enable IR1 function, active pulse 3/16 bit time	
Select Device Mode.		

### F81866 H/W Monitor

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Advanced

<p>Pc Health Status</p> <p>▶ Smart Fan Mode Configuration</p> <p>CPU Temperature : +23 ℃</p> <p>PCH temperature : +43 ℃</p> <p>Fan1 Speed : 2018 RPM</p> <p>Fan2 Speed : N/A</p> <p>VCore : +1.056 V</p> <p>5V Dual : +5.129 V</p> <p>5V : +5.129 V</p> <p>12V : +12.144 V</p> <p>VSBSV : +5.064 V</p> <p>VCC3V : +3.360 V</p> <p>VSBB3V : +3.360 V</p> <p>VBAT : +3.312 V</p>	<p>Smart Fan Mode Select</p> <hr/> <p>←+: Select Screen</p> <p>↑↓: Select Item</p> <p>Enter: Select</p> <p>+/-: Change Opt.</p> <p>F1: General Help</p> <p>F2: Previous Values</p> <p>F3: Optimized Defaults</p> <p>F4: Save &amp; Exit</p> <p>ESC: Exit</p>
--	--

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## Smart Fan Mode Configuration

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Advanced

Smart Fan Mode Configuration ▶ FAN 1 Configuration ▶ FAN 2 Configuration	Smart FAN Configuration  ++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
--	---

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Advanced

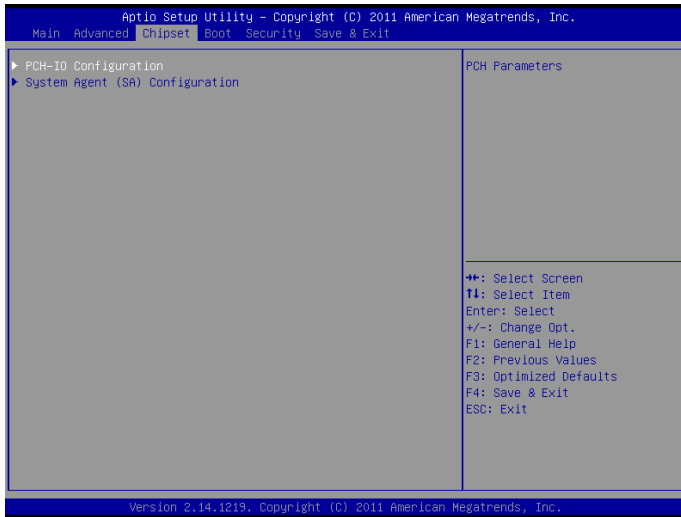
PC Health Status CPU Smart Fan control [Auto by Duty-Cycle] Target Temp. Sensor [CPU Temperature] Temperature Bound 1 75 Temperature Bound 2 65 Temperature Bound 3 55 Temperature Bound 4 45 Segment 1 Speed (%) 100 Segment 2 Speed (%) 80 Segment 3 Speed (%) 60 Segment 4 Speed (%) 40 Segment 5 Speed (%) 20 Full Speed Count 3000	++: Select Screen T1: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
---	--

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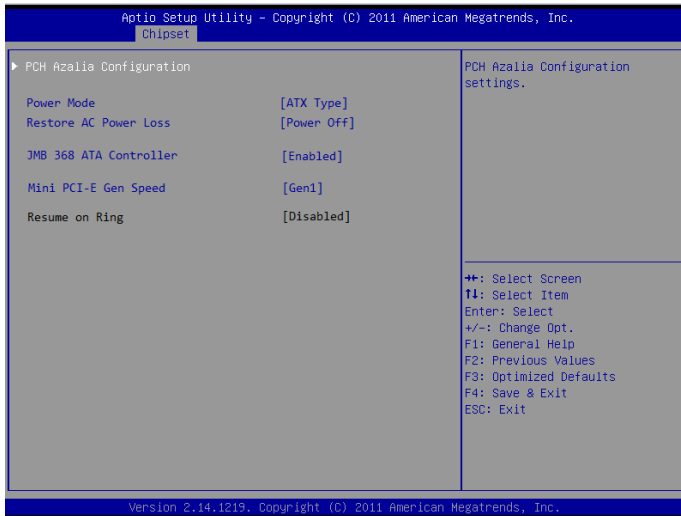
## Options summary :

SYS/CPU Smart Fan Control	Auto by RPM	Default
	Auto by Duty-Cycle	
	Manual by RPM	
	Manual by Duty-Cycle	
<p>Select CPU Smart FAN mode</p> <p>Auto by RPM: Automatically controlling the fan to maintain target Fan Speed.</p> <p>Auto by Duty-Cycle: Automatically controlling the fan to maintain target temperature.</p> <p>Manual by RPM: Manually controlling the fan with a given Fan Speed.</p> <p>Manual by Duty-Cycle: Manually controlling the fan with a given control PWM.</p>		
Target Temp. Sensor	CPU Temperature	Default
	Chassis Temperature	
	PCH Temperature	
Select target temperature source.		

## Setup submenu: Chipset



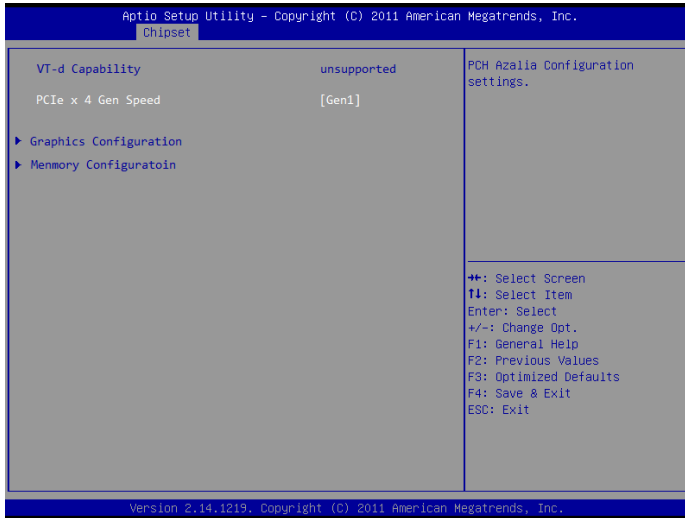
## PCH-IO Configuration



## Options summary :

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select Power Mode.		
Restore on AC Power Loss	Power Off	Default
	Power On	
	Last State	
Select the action system to take when restoring from power loss. ATX Type: Default Power Off AT Type: Default Power On		
JMB 386 ATA Controller	Disabled	Optimal Default, Failsafe Default (support CF-PATA)
	Enabled	
Enabling/Disabling PCI-E to CF-PATA controller.		
Mini PCI-E Gen Speed	Gen1	Optimal Default, Failsafe Default
	Gen2	
Select PCI Express Gen speed.		
Resume on Ring	Disabled	Default
	Enabled	
Enabling/Disabling Resume on Ring. Only show when F81866 Super IO Configuration switch to [Disable]		

### System Agent (SA) Configuration



Options summary :

PCIe x 4 Gen Speed	Gen1	Optimal Default, Failsafe Default
	Gen2	
Select PCI Express Gen speed.		



## Graphics Configuration

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Chipset

Graphics Configuration		Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.
Primary Display	[Auto]	**: Select Screen <b>T</b> : Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Internal Graphics	[Auto]	
GTT Size	[2MB]	
Aperture Size	[256MB]	
DWMT Pre-Allocated	[64M]	
DWMT Total Gfx Mem	[MAX]	
Primary IGFX Boot Display	[AUTO]	
CH7511B Panel Type	[1024x768 18 Bit]	
CH7511B Backlight Control Mode	[DC Mode]	
Brightness Setting	[100%]	
Brightness Control	[INVERT]	

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### Options summary :

Primary Display	Auto	Default
	IGFX	
	PEG	
Select which of IGFX/PEG Graphics device should be Primary Display.		
Internal Graphics	Auto	Default
	Disable	
	Enable	
Keep IGD enabled based on the setup options.		
GTT Size	1MB	Default
	2MB	

Select the GTT Size.

Aperture Size	128MB	Default
	256MB	
	512MB	

Select the Aperture Size.

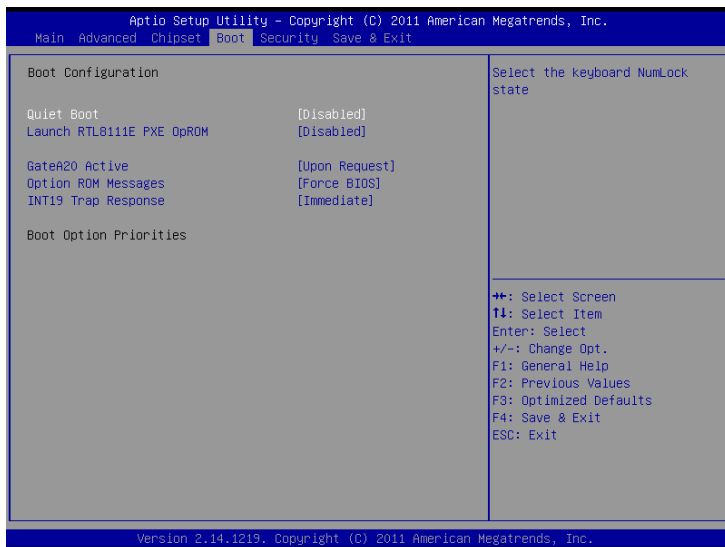
DVMT Pre-Allocated	32M	Default
	64M	
	96M	
	128M	
	160M	
	192M	
	224M	
	256M	
	288M	
	320M	
	352M	
	384M	
	416M	
	448M	
	480M	
512M		
1024M		

Select DVMT 5.0 Pre-Allocated(Fixed) Graphics Memory size used by the Internal Graphics Device.

DVMT Total Gfx Mem	128M		
	256M		
	MAX	Default	
Select DVMT Total Graphics Memory			
Primary IGFX Boot Display	AUTO	Default	
	CRT		
	HDMI-1		
	HDMI-2		
	DVI		
Select the Video Device which will be activated during POST. For dual-display, select "Auto". Note: The platform only supports single display in legacy environment (DOS).			
CH7511B Panel Type	640x480	18Bit	Default
	800x600	18Bit	
	1024x768	18Bit	
	640x480	24Bit	
	800x600	24Bit	
	1024x768	24Bit	
	1280x1024	48Bit	
	1600x1200	48Bit	
	800x480	18Bit	
	1280x768	18Bit	

	1280x768	24Bit
	1366x768	24Bit
	1440x900	48Bit
	1920x1080	48Bit
	1280x1024	18Bit
	1280x1024	24Bit
Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.		
CH7511B Baclight Control Mode	DC Mode	Default
	PWM Mode	
Select Ch7511B Backlight Control by DC or PWM Mode.		
Brightness setting	100%	Default
	75%	
	50%	
	25%	
	0%	
CH7511B Brightness Setting.		
Backlight Control	NORMAL	Default
	INVERT	
Select Ch7511B Backlight Control way.		

## Setup submenu: Boot

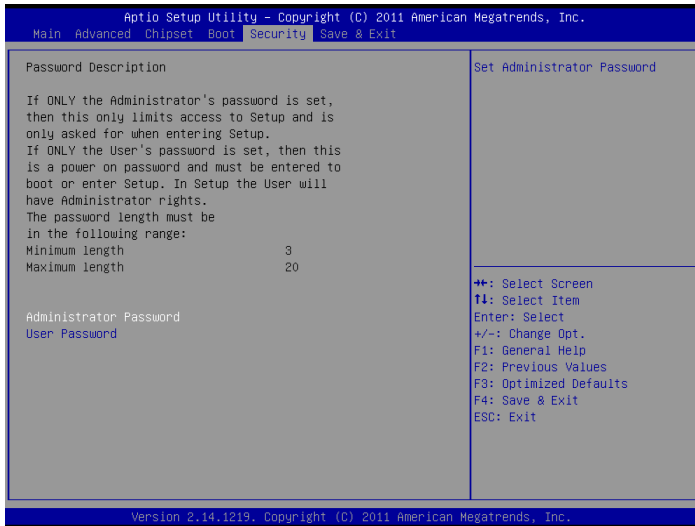


## Options summary :

Bootup NumLock State	On	Default
	Off	
Select the keyboard NumLock state.		
Quiet Boot	Disabled	Default
	Enabled	
En/Disable showing boot logo.		
Launch RTL8111F PXE OpROM	Disabled	Default
	Enabled	
Enable or Disable Legacy Boot Option for RTL811E.		

GateA20 Active	Upon Request	Default
	Always	
<p>UPON REQUEST – GA20 can be disabled using BIOS services.          ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.</p>		
Option ROM Messages	Force BIOS	Default
	Keep Current	
Set display mode for Option ROM.		
INT19 Trap Response	Immediate	Default
	Postponed	
<p>BIOS reaction on INT19 trapping by Option ROM:          IMMEDIATE – execute the trap right away;          POSTPONED – execute the trap during legacy boot.</p>		

## Setup submenu: Security



### Change User/Supervisor Password

You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

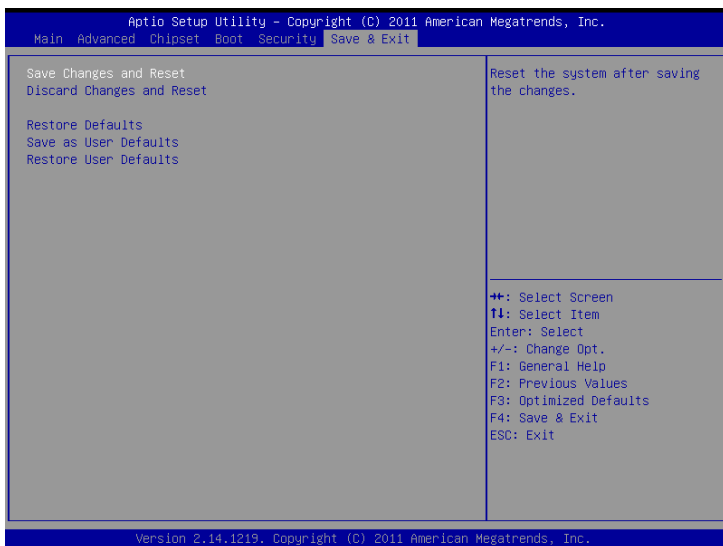
If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

### Removing the Password

Highlight this item and type in the current password. At the next dialog

box press Enter to disable password protection.

## Setup submenu: Exit





Chapter

4

**Driver  
Installation**

***Follow the sequence below to install the drivers:***

- Step 1 – Install Chipset Driver
- Step 2 – Install VGA Driver
- Step 3 – Install LAN Driver
- Step 4 – Install AUDIO Driver
- Step 5 – Install AHCI Driver
- Step 6 – Install ME Driver
- Step 7 – Install TPM Driver
- Step 8 – Install Serial Port Driver (Optional)

Please read following instructions for detailed installations.

## 4.1 Installation:

---

Insert DVD-ROM into the DVD-ROM Drive. And install the drivers from Step 1 to Step 8 in order.

### Step 1 – Install Chipset Driver

1. Click on the **Step1 - Chipset** folder and then double click on the **Setup.exe**
2. Follow the instructions that the window shows
3. The system will help you to install the driver automatically

### Step 2 – Install VGA Driver

1. Click on the **Step 2 - VGA** folder and select the OS your system is
2. Double click on **Setup.exe** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you to install the driver automatically

### Step 3 – Install LAN Driver

1. Click on the **Step 3 - LAN** folder and select the OS your system is
2. Double click on **setup.exe** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you to install the driver automatically

### Step 4 – Install AUDIO Driver

1. Click on the **Step 4 - Audio** folder and double click on **AsusSetup.exe**

2. Follow the instructions that the window shows
3. The system will help you to install the driver automatically

### Step 5 – Install AHCI Driver

1. Click on the **Step 5 - AHCI** folder
2. For XP, please copy the files to **Floppy** folder and press **F6** to install ; for other OS, system will install the driver automatically.

### Step 6 – Install ME Driver

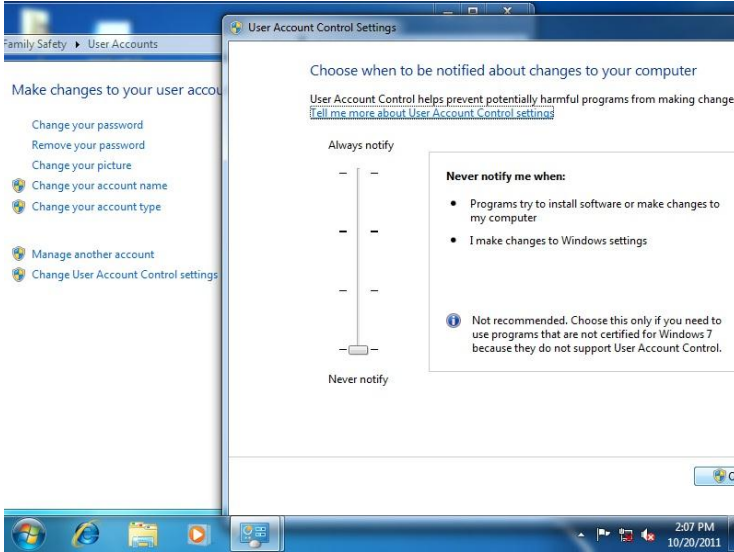
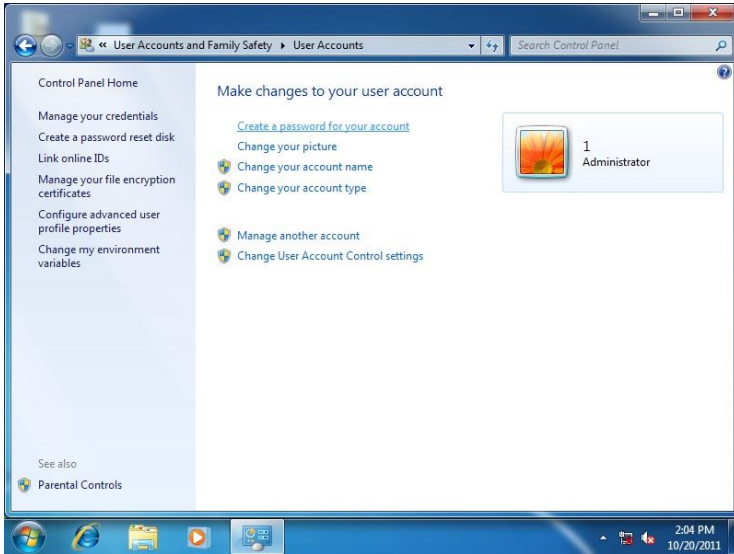
1. Click on the **Step 6 - ME** folder and select the OS your system is
2. Double click on **setup.exe** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you to install the driver automatically

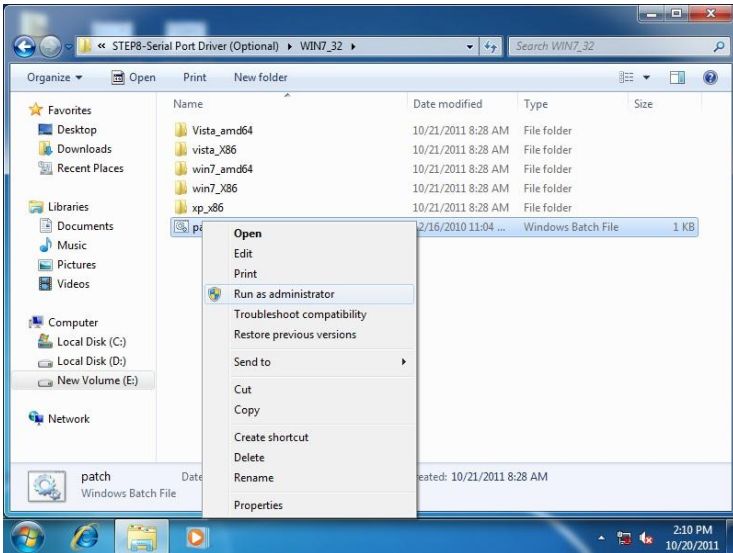
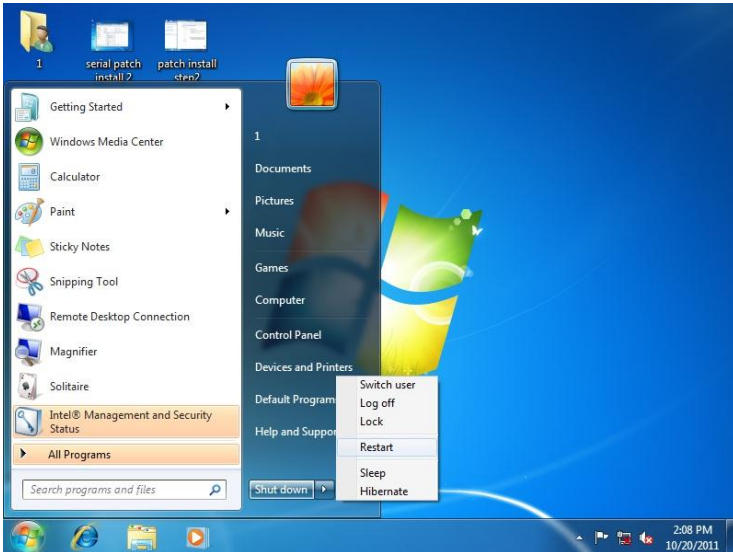
### Step 7 – Install TPM Driver

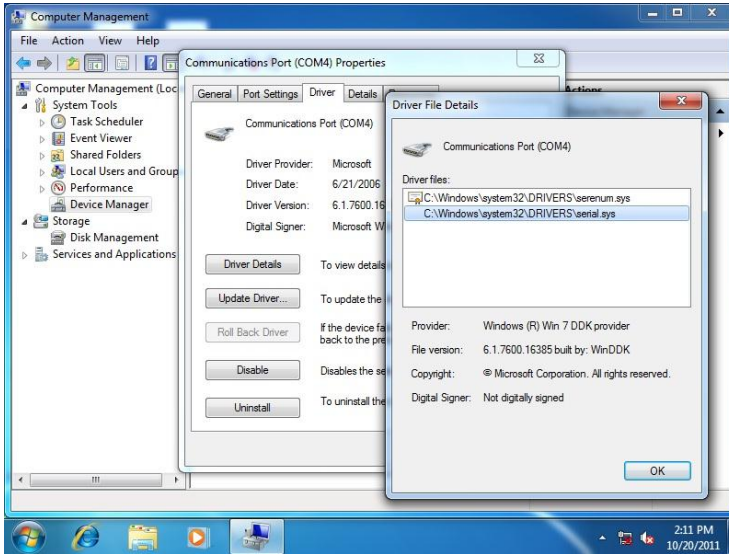
1. Click on the **Step 7 - TPM** folder and double click on **Setup.exe** file
2. Follow the instructions that the window shows
3. The system will help you to install the driver automatically

### Step 8 –Install Serial Port Driver (Optional)

1. Click on the **Step 8 - Install Serial Port Driver** folder.
2. Follow the below 5 step to install driver.







Appendix

**A**

# Programming the Watchdog Timer



## A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E <sup>(Note1)</sup>	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F <sup>(Note2)</sup>	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07 <sup>(Note3)</sup>	0xF6 <sup>(Note4)</sup>		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07 <sup>(Note5)</sup>	0xF5 <sup>(Note6)</sup>	3 <sup>(Note7)</sup>	0 <sup>(Note8)</sup>	Select time unit. 0: second 1: minute
Watchdog Enable	0x07 <sup>(Note9)</sup>	0xF5 <sup>(Note10)</sup>	5 <sup>(Note11)</sup>	1 <sup>(Note12)</sup>	0: Disable 1: Enable
Timeout Status	0x07 <sup>(Note13)</sup>	0xF5 <sup>(Note14)</sup>	6 <sup>(Note15)</sup>	1	1: Clear timeout status
Output Mode	0x07 <sup>(Note16)</sup>	0xF5 <sup>(Note17)</sup>	4 <sup>(Note18)</sup>	1 <sup>(Note19)</sup>	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07 <sup>(Note20)</sup>	0xFA <sup>(Note21)</sup>	0 <sup>(Note22)</sup>	1 <sup>(Note23)</sup>	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

\*\*\*\*\*

// SuperIO relative definition (Please reference to Table 1)

**#define byte** SIOIndex //This parameter is represented from **Note1**

**#define byte** SIOData //This parameter is represented from **Note2**

**#define void** IOWriteByte(**byte** IOPort, **byte** Value);

**#define byte** IOReadByte(**byte** IOPort);

// Watch Dog relative definition (Please reference to Table 2)

**#define byte** TimerLDN //This parameter is represented from **Note3**

**#define byte** TimerReg //This parameter is represented from **Note4**

**#define byte** TimerVal // This parameter is represented from **Note24**

**#define byte** UnitLDN //This parameter is represented from **Note5**

**#define byte** UnitReg //This parameter is represented from **Note6**

**#define byte** UnitBit //This parameter is represented from **Note7**

**#define byte** UnitVal //This parameter is represented from **Note8**

**#define byte** EnableLDN //This parameter is represented from **Note9**

**#define byte** EnableReg //This parameter is represented from **Note10**

**#define byte** EnableBit //This parameter is represented from **Note11**

**#define byte** EnableVal //This parameter is represented from **Note12**

**#define byte** StatusLDN // This parameter is represented from **Note13**

**#define byte** StatusReg // This parameter is represented from **Note14**

**#define byte** StatusBit // This parameter is represented from **Note15**

**#define byte** ModeLDN // This parameter is represented from **Note16**

**#define byte** ModeReg // This parameter is represented from **Note17**

**#define byte** ModeBit // This parameter is represented from **Note18**

**#define byte** ModeVal // This parameter is represented from **Note19**

**#define byte** WDTRstLDN // This parameter is represented from **Note20**

**#define byte** WDTRstReg // This parameter is represented from **Note21**

**#define byte** WDTRstBit // This parameter is represented from **Note22**

**#define byte** WDTRstVal // This parameter is represented from **Note23**

\*\*\*\*\*

```
*****
VOID Main() {
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AeonWDTEnable
VOID AeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AeonWDTConfig
VOID AeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte
Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```
*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

Appendix

**B**

# Mating Connector

## BSupport up to 65W.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector	
		Vendor	Model no
ATX12V	ATX 4P Power Connector	PINREX	740-41-04TWC0
AUDIO	Audio jack Connector	FOXCONN	JA33331-2119-4F
BATTERY	RTC - Coin Battery Holder	LOTES	KB7566BP5L
CF-PATA_ CF-SATA	CF CONN 50P,0.635mm,REVERS,S MT	PROCONN	CFH050-A0-53G6
COM1	D-SUB 9P,M,R/A,G/F,HIGH RISE	FOXCONN	DM10151-25W3-4F
COM2	Int. COM2 RS-232 Serial Port Connector	PINREX	52M-90-10GBE0
COM3	Int. COM2 RS-232 Serial Port Connector	PINREX	52M-90-10GBE0
COM4	Int. COM2 RS-232 Serial Port Connector	PINREX	52M-90-10GBE0
COM5	Int. COM2 RS-232 Serial Port Connector	PINREX	52M-90-10GBE0
COM6	Int. COM2 RS-232 Serial Port Connector	PINREX	52M-90-10GBE0
DEBUG	WtoB CON 12P,1.0mm,S/T,SMT	ACES	87212-12G0
DIMM_A1	DIMM1 Slot	FOXCONN	ATNA291-AED-4F
DIMM_B1	DIMM2 Slot	FOXCONN	ATNA291-AED-4F
DIO	Digital I/O Connector	PINREX	52S-90-10GB00
F_PANEL	Front Panel Connector	PINREX	210-92-05GB02

HDMI1	HDMI CON 19P,0.5MM,A TYPE,R/A	SINBON	1165-92104-24D
HDMI2	HDMI CON 19P,0.5MM,A TYPE,R/A	SINBON	1165-92104-24D
INV	Inverter Connector	PINREX	721-81-05TW00
KBMS_US B56	PS/2 Keyboard/Mouse Connector with Dock USB 2.0 Connector	FOXCONN	UB11121-HSDB-4F
LAN1_USB12	1000 Base-T Ethernet Connector with Dock USB 2.0 Connector	FOXCONN	JFM38U1M-21GS-4F
LAN2_USB34	1000 Base-T Ethernet Connector with Dock USB 2.0 Connector	FOXCONN	JFM38U1M-21GS-4F
LGA1	CPU Socket - LGA-1155P	LOTES	ACA-ZIF-096-P07
LVDS	LVDS Panel Signal Connector	PINREX	712-76-30GWR8
MINICARD	MINI PCI-E 52P,0.8mm,6.7H,SMT	LOTES	AAA-PCI-073-K02
PCIEX4	PCI Express x4 Slot	LOTES	AAA-PCI-022-K15
PWR1	SATA Power Connector	HR	A2540WV-4P
S_FAN1	System FAN Connector	PINREX	744-81-04TG20
S_FAN2	System FAN Connector	PINREX	744-81-04TG20
SATA3G_1	SATA II Connector	PINREX	770-83-07SV29
SATA3G_2	SATA II Connector	PINREX	770-83-07SV29
SIM	SIM Card Socket	HAMBURG	ICA-509
USB910	Int. USB 2.0 Connector	PINREX	222-97-05GBE1
VGA	D-SUB 15P,R/A F,HIGH RISE,DIP	HIGH TOP	1DS01511-31125



Appendix

C

# Electrical Specifications for I/O Ports

## C.1 DIO Programming

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EMB-H61B utilizes FINTEK 81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application. There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally. (These three steps are the same as programming WDT)

## C.2 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E <sup>(Note1)</sup>	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F <sup>(Note2)</sup>	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06 <sup>(Note3)</sup>	0x8A <sup>(Note4)</sup>	0 <sup>(Note5)</sup>		GPIO80
DIO-2 Pin Status	0x06 <sup>(Note6)</sup>	0x8A <sup>(Note7)</sup>	1 <sup>(Note8)</sup>		GPIO81
DIO-3 Pin Status	0x06 <sup>(Note9)</sup>	0x8A <sup>(Note10)</sup>	2 <sup>(Note11)</sup>		GPIO82
DIO-4 Pin Status	0x06 <sup>(Note12)</sup>	0x8A <sup>(Note13)</sup>	3 <sup>(Note14)</sup>		GPIO83
DIO-5 Pin Status	0x06 <sup>(Note15)</sup>	0x8A <sup>(Note16)</sup>	4 <sup>(Note17)</sup>		GPIO84
DIO-6 Pin Status	0x06 <sup>(Note18)</sup>	0x8A <sup>(Note19)</sup>	5 <sup>(Note20)</sup>		GPIO85
DIO-7 Pin Status	0x06 <sup>(Note21)</sup>	0x8A <sup>(Note22)</sup>	6 <sup>(Note23)</sup>		GPIO86
DIO-8 Pin Status	0x06 <sup>(Note24)</sup>	0x8A <sup>(Note25)</sup>	7 <sup>(Note26)</sup>		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06 <sup>(Note27)</sup>	0x89 <sup>(Note28)</sup>	0 <sup>(Note29)</sup>	<sup>(Note30)</sup>	GPIO80
DIO-2 Output Data	0x06 <sup>(Note31)</sup>	0x89 <sup>(Note32)</sup>	1 <sup>(Note33)</sup>	<sup>(Note34)</sup>	GPIO81
DIO-3 Output Data	0x06 <sup>(Note35)</sup>	0x89 <sup>(Note36)</sup>	2 <sup>(Note37)</sup>	<sup>(Note38)</sup>	GPIO82
DIO-4 Output Data	0x06 <sup>(Note39)</sup>	0x89 <sup>(Note40)</sup>	3 <sup>(Note41)</sup>	<sup>(Note42)</sup>	GPIO83
DIO-5 Output Data	0x06 <sup>(Note43)</sup>	0x89 <sup>(Note44)</sup>	4 <sup>(Note45)</sup>	<sup>(Note46)</sup>	GPIO84
DIO-6 Output Data	0x06 <sup>(Note47)</sup>	0x89 <sup>(Note48)</sup>	5 <sup>(Note49)</sup>	<sup>(Note50)</sup>	GPIO85
DIO-7 Output Data	0x06 <sup>(Note51)</sup>	0x89 <sup>(Note52)</sup>	6 <sup>(Note53)</sup>	<sup>(Note54)</sup>	GPIO86
DIO-8 Output Data	0x06 <sup>(Note55)</sup>	0x89 <sup>(Note56)</sup>	7 <sup>(Note57)</sup>	<sup>(Note58)</sup>	GPIO87

### C.3 Digital I/O Sample Program

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```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****

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// Digital Output control relative definition (Please reference to Table 3)

```

#define byte   DOutput1LDN // This parameter is represented from Note27
#define byte   DOutput1Reg // This parameter is represented from Note28
#define byte   DOutput1Bit // This parameter is represented from Note29
#define byte   DOutput1Val // This parameter is represented from Note30
#define byte   DOutput2LDN // This parameter is represented from Note31
#define byte   DOutput2Reg // This parameter is represented from Note32
#define byte   DOutput2Bit // This parameter is represented from Note33
#define byte   DOutput2Val // This parameter is represented from Note34
#define byte   DOutput3LDN // This parameter is represented from Note35
#define byte   DOutput3Reg // This parameter is represented from Note36
#define byte   DOutput3Bit // This parameter is represented from Note37
#define byte   DOutput3Val // This parameter is represented from Note38
#define byte   DOutput4LDN // This parameter is represented from Note39
#define byte   DOutput4Reg // This parameter is represented from Note40
#define byte   DOutput4Bit // This parameter is represented from Note41
#define byte   DOutput4Val // This parameter is represented from Note42
#define byte   DOutput5LDN // This parameter is represented from Note43
#define byte   DOutput5Reg // This parameter is represented from Note44
#define byte   DOutput5Bit // This parameter is represented from Note45
#define byte   DOutput5Val // This parameter is represented from Note46
#define byte   DOutput6LDN // This parameter is represented from Note47
#define byte   DOutput6Reg // This parameter is represented from Note48
#define byte   DOutput6Bit // This parameter is represented from Note49
#define byte   DOutput6Val // This parameter is represented from Note50
#define byte   DOutput7LDN // This parameter is represented from Note51
#define byte   DOutput7Reg // This parameter is represented from Note52
#define byte   DOutput7Bit // This parameter is represented from Note53
#define byte   DOutput7Val // This parameter is represented from Note54
#define byte   DOutput8LDN // This parameter is represented from Note55
#define byte   DOutput8Reg // This parameter is represented from Note56
#define byte   DOutput8Bit // This parameter is represented from Note57
#define byte   DOutput8Val // This parameter is represented from Note58

```

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```
*****
VOID Main() {
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum,
byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```
*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```



```

*****
Boolean SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****

```