COM-WHUC6

COM Express Module

User's Manual 2nd Ed

Last Updated: May 18, 2022

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● COM-WHUC6	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	COM Express Compact size, 95mm x 95mm
CPU	8th Generation Intel® Core™ ULT Series Processor
CPU Frequency	-
Chipset	Onboard 8th Generation Intel® Core™ SoC
Memory Type	SO-DIMM DDR4 2400 Socket x2
Max. Memory Capacity	Up to 32GB
BIOS	AMI BIOS, Legacy free BIOS
Wake on LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	Normal: +12V
Power Supply Type	AT/ ATX Mode
Power Consumption (Typical)	i7-8665UE, DDR4 32GB with 64GB eMMC, 12V @ 2.61A during 100% full loading test.
Dimension (L x W)	95mm x 95mm
Operating Temperature	32°F~ 140°F (0°C ~ 60°C)
Storage Temperature	-4°F ~ 158°F (-20°C ~ 70°C)
Operating Humidity	0% ~ 90% relative humidity, non-condensing
MTBF (Hours)	TBD
Certification	CE/FCC Class A

Display

VGA/LCD Controller	Intel® UHD Graphics 620 / 610
Video Output	DDI0: LVDS, (eDP by BOM change)
	DDI1: Display Port
	DDI2: Default VGA, (DP by SW1)
LVDS Interface	Support 18-bit and 24-bit dual channel

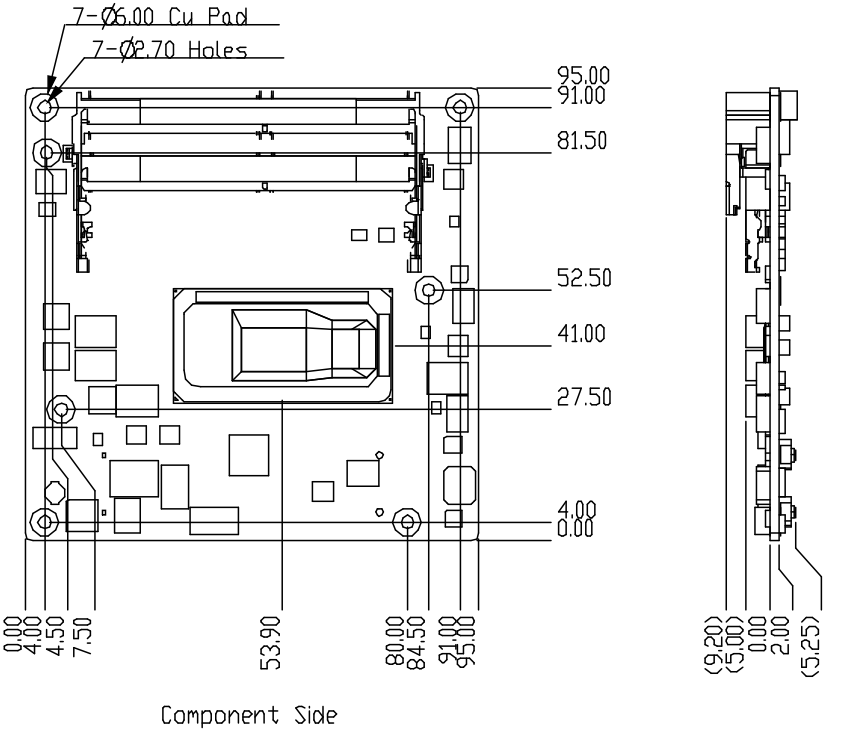
I/O

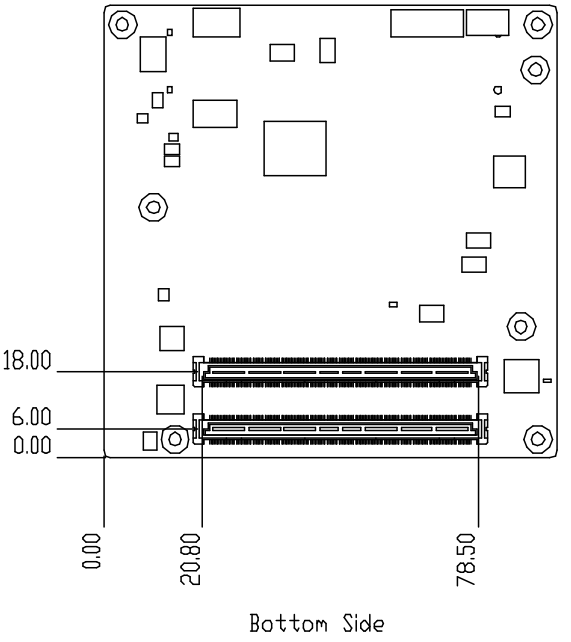
Ethernet	Intel® I219 GbE x 1
Audio	HD Audio x 1
USB Port	USB 2.0 x 8
	USB 3.2 Gen 2 x 4
Serial Port	2-wire UART x 2 (TX/RX)
HDD Interface	SATA3 x 2 as default (up to 3)
Onboard Storage	eMMC x 1 (up to 64GB)
Expansion Slot	PCIe[x1] x 4 + PCIe[x4] x 1 (default),
	I2C
	LPC
	SMBus
GPIO	8-bit
TPM	TPM 2.0 Optional

Chapter 2

Hardware Information

2.1 Dimensions

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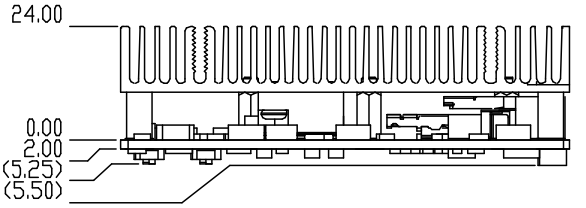
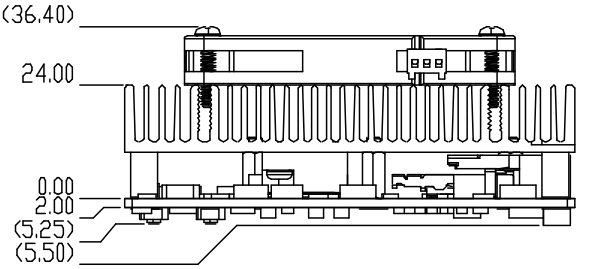
78.50
Bottom Side

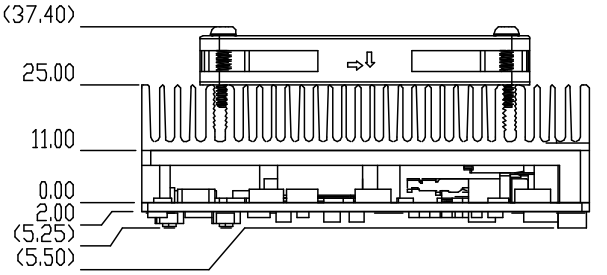
With Heat Sink (Part No: COM-WHUC6-HSK01)



With Active Cooling (Part No: COM-WHUC6-FAN01)

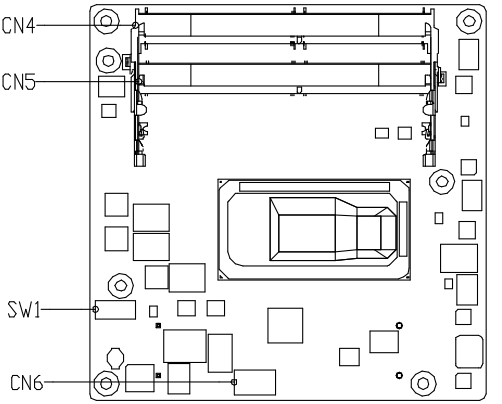


With Heat Spreader and Active Cooling (Part No: COM-WHUC6-HSP01 and COM-FAN02)

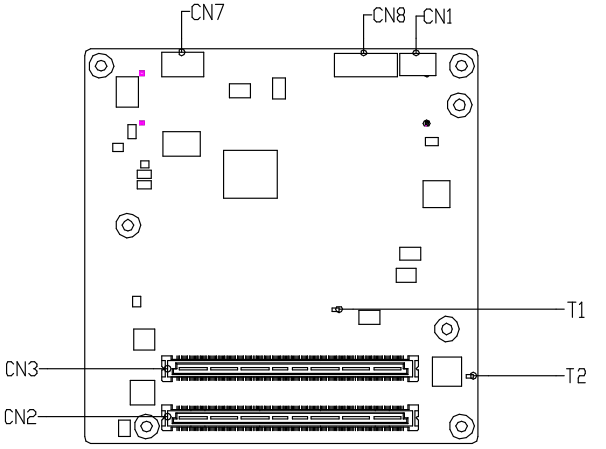


2.2 Jumpers and Connectors

Top Side



Bottom Side



2.3 List of Jumpers and Switches

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
SW1	AT/ATX switch & DDI/VGA switch

2.3.1 AT/ATX Switch & DDI/VGA Switch (SW1)

	ON	OFF
1	AT Mode	ATX Mode (Default)
2	VGA (Default)	DDI2

2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	RTC Battery Connector
CN2	Express ROW A/B Connector
CN3	Express ROW C/D Connector
CN4	DDR4 SO-DIMM Connector
CN5	DDR4 SO-DIMM Connector
CN6	EC Flash Programming Connector
CN7	SPI Flash Programming Connector
CN8	LPC debug card Connector

2.4.1 COM Express ROW A/B Connector (CN2)

Row A		Row B	
Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK	B8	LPC_DRQ0#(NC)
A9	GBE0_MDI1-	B9	LPC_DRQ1#(NC)

Row A		Row B	
Pin	Signal	Pin	Signal
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF(NC)	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+(NC)
A23	SATA2_TX-	B23	SATA3_TX-(NC)
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+(NC)
A26	SATA2_RX-	B26	SATA3_RX-(NC)
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	AC_SDIN2(NC)
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT

Row A		Row B	
Pin	Signal	Pin	Signal
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE# (NC)
A49	EXCD0_CPPE# (NC)	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+
A53	PCIE_TX5-	B53	PCIE_RX5-
A54	GPI0	B54	GPO1
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-

Row A		Row B	
Pin	Signal	Pin	Signal
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+
A72	LVDS_A0-	B72	LVDS_B0-
A73	LVDS_A1+	B73	LVDS_B1+
A74	LVDS_A1-	B74	LVDS_B1-
A75	LVDS_A2+	B75	LVDS_B2+
A76	LVDS_A2-	B76	LVDS_B2-
A77	LVDS_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+
A82	LVDS_A_CK-	B82	LVDS_B_CK-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY

Row A		Row B	
Pin	Signal	Pin	Signal
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	RSVD	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI _POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	TYPE10#(NC)	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWNOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V

Row A		Row B	
Pin	Signal	Pin	Signal
A110	GND (FIXED)	B110	GND (FIXED)

2.4.2 COM Express ROW C/D Connector (CN3)

Row C		Row D	
Pin	Signal	Pin	Signal
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND (FIXED)	D2	GND (FIXED)
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND (FIXED)	D5	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND (FIXED)	D8	GND (FIXED)
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	GND (FIXED)	D14	GND (FIXED)
C15	DDI1_PAIR6+(NC)	D15	DDI1_CTRLCLK_AUX+
C16	DDI1_PAIR6-(NC)	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+

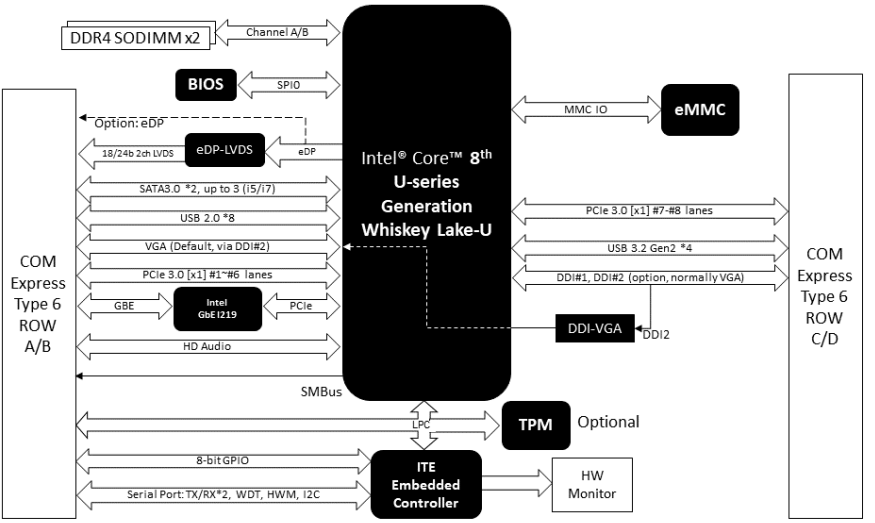
Row C		Row D	
Pin	Signal	Pin	Signal
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	GND (FIXED)	D21	GND (FIXED)
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	DDI1_PAIR4+(NC)	D25	RSVD
C26	DDI1_PAIR4-(NC)	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	DDI1_PAIR5+(NC)	D29	DDI1_PAIR1+
C30	DDI1_PAIR5-(NC)	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	DDI3_CTRLCLK_AUX+(NC)	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-(NC)	D37	DDI1_PAIR3-
C38	DDI3_DDC_AUX_SEL(NC)	D38	RSVD
C39	DDI3_PAIR0+(NC)	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-(NC)	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+(NC)	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-(NC)	D43	DDI2_PAIR1-
C44	DDI3_HPD(NC)	D44	DDI2_HPD

Row C		Row D	
Pin	Signal	Pin	Signal
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+(NC)	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-(NC)	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	DDI3_PAIR3+(NC)	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-(NC)	D50	DDI2_PAIR3-
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+(NC)	D52	PEG_TX0+(NC)
C53	PEG_RX0-(NC)	D53	PEG_TX0-(NC)
C54	TYPE0#(NC)	D54	PEG_LAN_RV#(NC)
C55	PEG_RX1+(NC)	D55	PEG_TX1+(NC)
C56	PEG_RX1-(NC)	D56	PEG_TX1-(NC)
C57	TYPE1#(NC)	D57	TYPE2#
C58	PEG_RX2+(NC)	D58	PEG_TX2+(NC)
C59	PEG_RX2-(NC)	D59	PEG_TX2-(NC)
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+(NC)	D61	PEG_TX3+(NC)
C62	PEG_RX3-(NC)	D62	PEG_TX3-(NC)
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+(NC)	D65	PEG_TX4+(NC)
C66	PEG_RX4-(NC)	D66	PEG_TX4-(NC)
C67	RSVD	D67	GND (FIXED)
C68	PEG_RX5+(NC)	D68	PEG_TX5+(NC)
C69	PEG_RX5-(NC)	D69	PEG_TX5-(NC)

Row C		Row D	
Pin	Signal	Pin	Signal
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+(NC)	D71	PEG_TX6+(NC)
C72	PEG_RX6-(NC)	D72	PEG_TX6-(NC)
C73	GND (FIXED)	D73	GND (FIXED)
C74	PEG_RX7+(NC)	D74	PEG_TX7+(NC)
C75	PEG_RX7-(NC)	D75	PEG_TX7-(NC)
C76	GND (FIXED)	D76	GND (FIXED)
C77	RSVD	D77	RSVD
C78	PEG_RX8+(NC)	D78	PEG_TX8+(NC)
C79	PEG_RX8-(NC)	D79	PEG_TX8-(NC)
C80	GND (FIXED)	D80	GND (FIXED)
C81	PEG_RX9+(NC)	D81	PEG_TX9+(NC)
C82	PEG_RX9-(NC)	D82	PEG_TX9-(NC)
C83	RSVD	D83	RSVD
C84	GND (FIXED)	D84	GND (FIXED)
C85	PEG_RX10+(NC)	D85	PEG_TX10+(NC)
C86	PEG_RX10-(NC)	D86	PEG_TX10-(NC)
C87	GND (FIXED)	D87	GND (FIXED)
C88	PEG_RX11+(NC)	D88	PEG_TX11+(NC)
C89	PEG_RX11-(NC)	D89	PEG_TX11-(NC)
C90	GND (FIXED)	D90	GND (FIXED)
C91	PEG_RX12+(NC)	D91	PEG_TX12+(NC)
C92	PEG_RX12-(NC)	D92	PEG_TX12-(NC)
C93	GND	D93	GND
C94	PEG_RX13+(NC)	D94	PEG_TX13+(NC)

Row C		Row D	
Pin	Signal	Pin	Signal
C95	PEG_RX13-(NC)	D95	PEG_TX13-(NC)
C96	GND (FIXED)	D96	GND (FIXED)
C97	RSVD	D97	RSVD
C98	PEG_RX14+(NC)	D98	PEG_TX14+(NC)
C99	PEG_RX14-(NC)	D99	PEG_TX14-(NC)
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+(NC)	D101	PEG_TX15+(NC)
C102	PEG_RX15-(NC)	D102	PEG_TX15-(NC)
C103	GND (FIXED)	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

2.5 Function Block Diagram



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

- You are starting your system for the first time.
- You have changed the hardware attached to your system.
- The CMOS memory has lost power and the configuration information has been erased.

The COM-WHUC6 CMOS memory uses a backup battery for data retention. The battery must be replaced if it runs out of power.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off.

To enter Setup, power on the computer and press <Del> immediately.

The function of each menu is as follows:

Main – Date and time can be set here. Use <Tab> to switch between date elements.

Advanced – Enable/disable boot option for legacy network devices.

System I/O – System I/O information and configuration.

Security – Password for setup administrator can be set here.

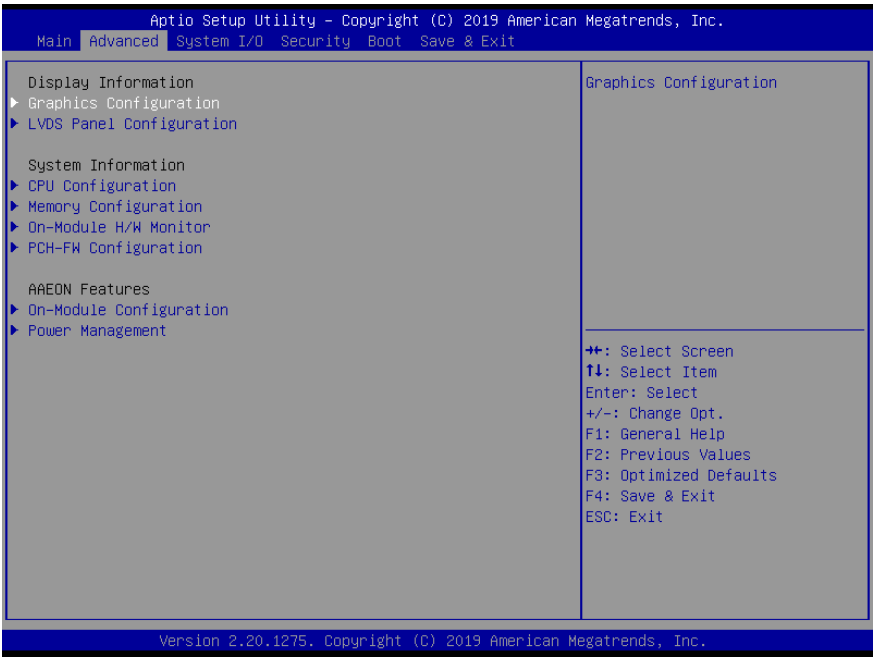
Boot – Enable/disable Quiet Boot option.

Save & Exit – Save changes and exit Setup.

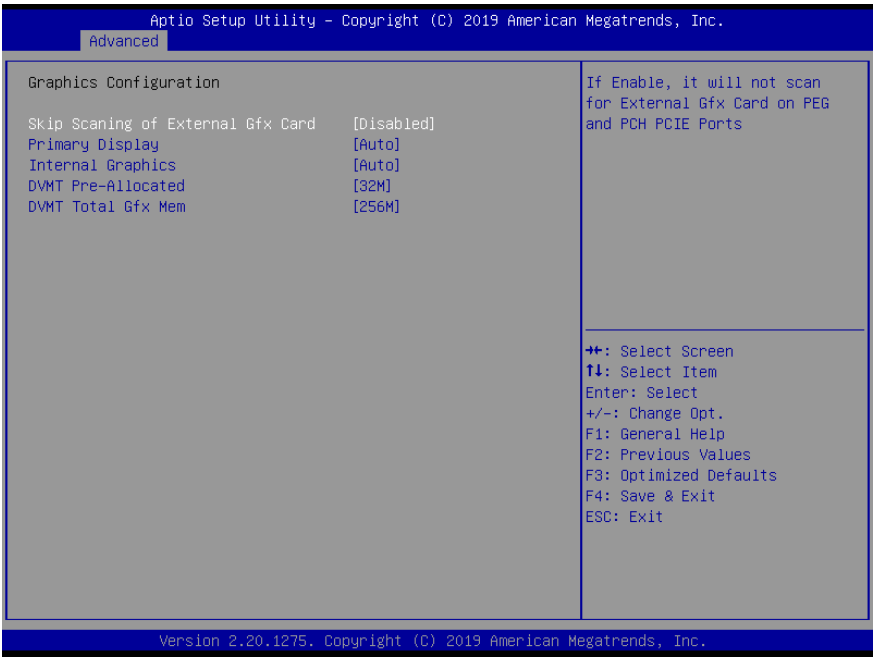
3.3 Main


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced System I/O Security Boot Save & Exit
== BIOS Information ==
COM-WHUC6 R1.1 (CWHUAM11)(11/06/2019)
== EC Information ==
(ECoM_016)(10/15/2019)
== CPU Information ==
Intel(R) Core(TM) i7-8665UE CPU @ 1.70GHz
== MEM Information ==
Total Memory 8192 MB
Memory Frequency 2133 MHz
== SATA Information ==
SATA Port 0 Empty
SATA Port 1 Empty
System Date [Tue 01/01/2019]
System Time [00:00:46]
Access Level Administrator
Set the Date. Use Tab to switch between Date elements.
Default Ranges:
Year: 1998-2199
Months: 1-12
Days: dependent on month
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.20.1275. Copyright (C) 2019 American Megatrends, Inc.

3.4 Advanced


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced System I/O Security Boot Save & Exit
Display Information
Graphics Configuration
LVDS Panel Configuration
System Information
CPU Configuration
Memory Configuration
On-Module H/W Monitor
PCH-FW Configuration
AAEON Features
On-Module Configuration
Power Management
Graphics Configuration
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.20.1275. Copyright (C) 2019 American Megatrends, Inc.

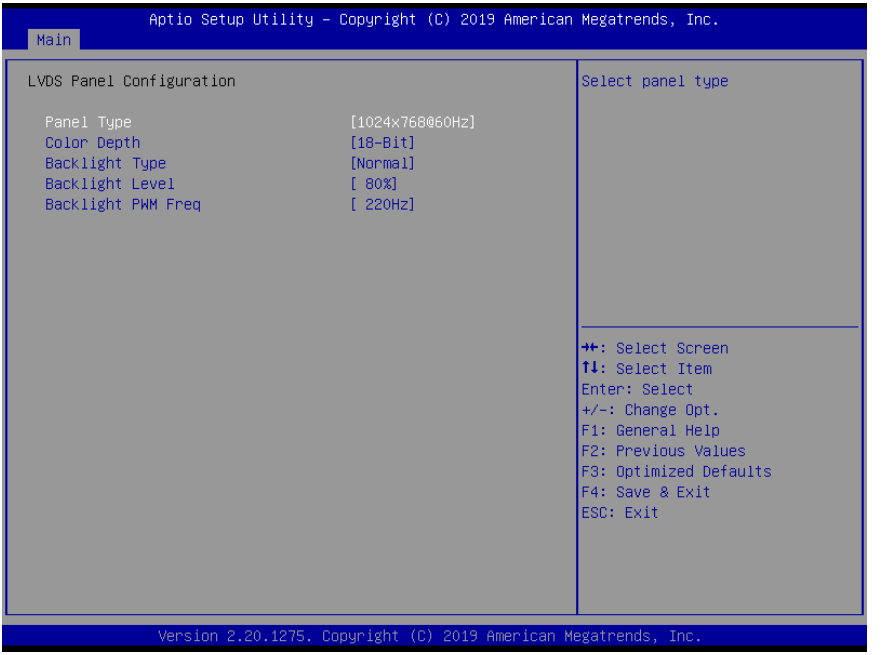
3.4.1 Graphics Configuration



Options Summary		
Skip Scaning of External Gfx Card	Disabled	Optimal Default, Failsafe Default
	Enabled	
If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PCI	
Select which of TGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Internal Graphics	Auto	Optimal Default, Failsafe Default
	Disabled	
	Enabled	
Keep IGFX enabled based on the setup options.		
DVMT Pre-Allocated	0M	Optimal Default, Failsafe Default
	32M	
	64M	

Options Summary		
DVMT Pre-Allocated	4M	
	12M	
	16M	
	20M	
	24M	
	28M	
	32M/F7	
	36M	
	40M	
	44M	
	48M	
	52M	
	56M	
	60M	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Drvice.		
DVMT Total Gfx Mem	128M	Optimal Default, Failsafe Default
	256M	
	MAX	
Select DVMT5.0 Total Graphic Memory Size used by the Internal Graphics Device.		

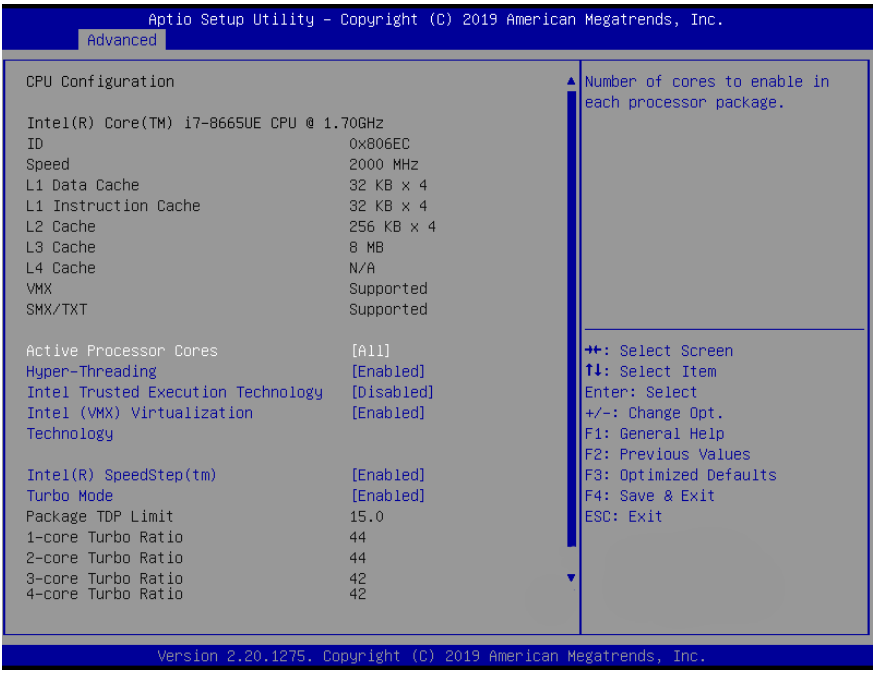
3.4.2 LVDS Panel Configuration



Options Summary		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x800@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	
Select panel type		

Options Summary		
Color Depth	18-Bit	Optimal Default, Failsafe Default
	24-Bit	
	36-Bit	
	48-Bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	Optimal Default, Failsafe Default
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	Optimal Default, Failsafe Default
	200Hz	
	220Hz	
	500Hz	
	1KHz	
	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.4.3 CPU Configuration

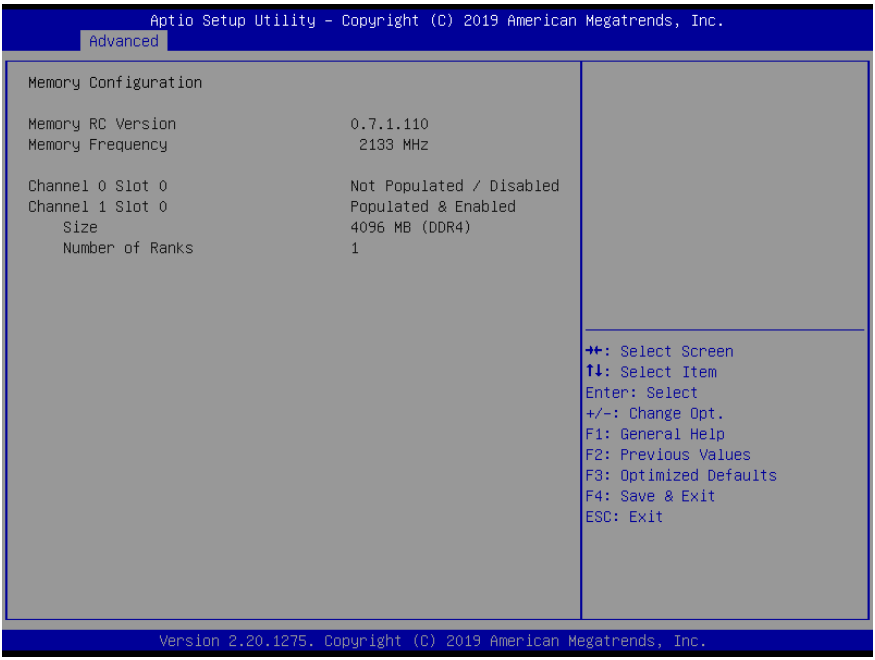


Options Summary		
Active Processor Cores	All	Optimal Default, Failsafe Default
	1	
	2	
	3	
Number of cores to enable in each processor package.		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled or Disabled Hyper-Threading Technology.		
Intel Trusted Execution Technology	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables utilization of additional hardware capabilities provided by Intel (R) Trusted Execution Technology. Changes require a full power cycle to take effect.		

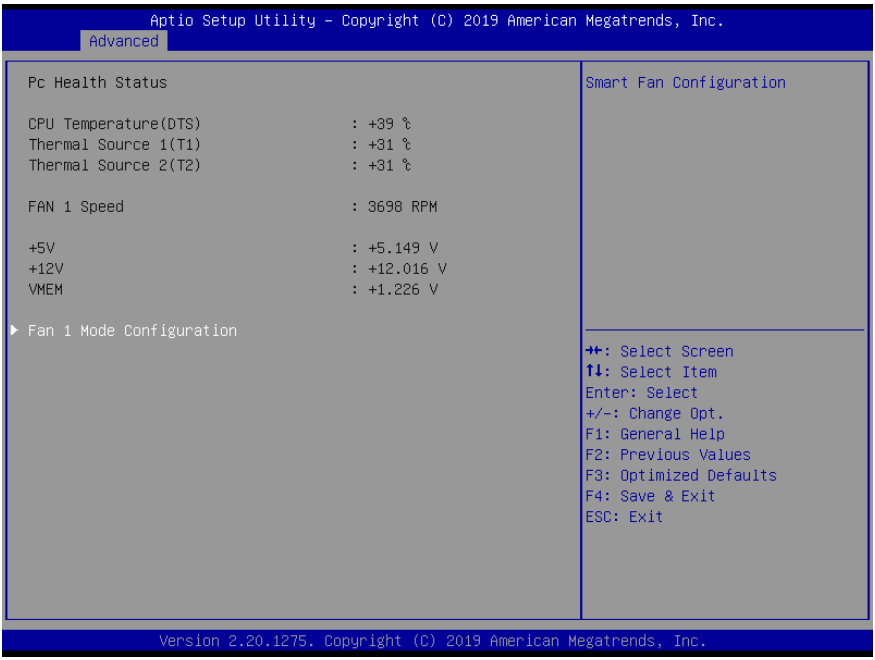
Table Continues on Next Page

Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/ Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).		

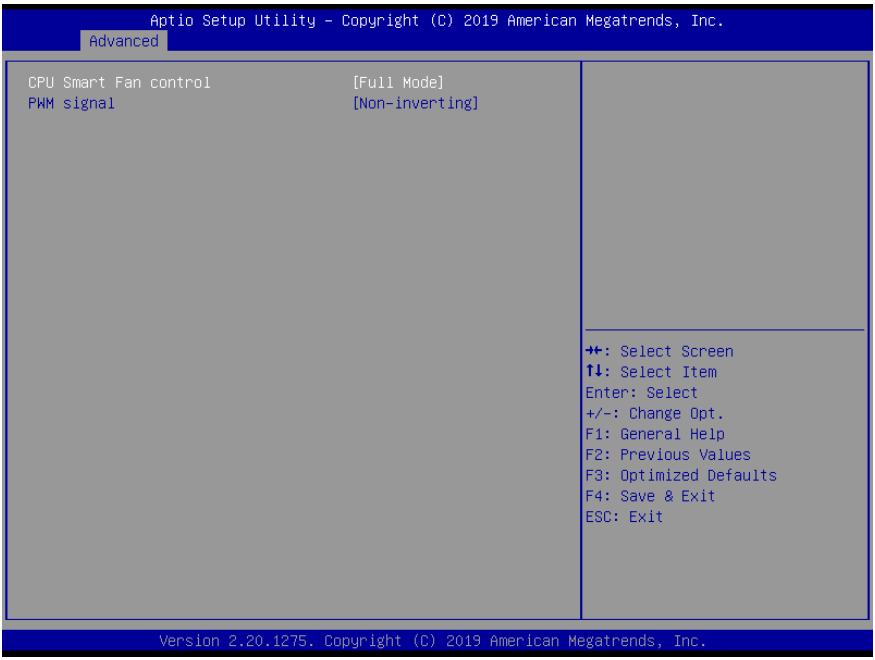
3.4.4 Memory Configuration



3.4.5 On-Module H/W Monitor

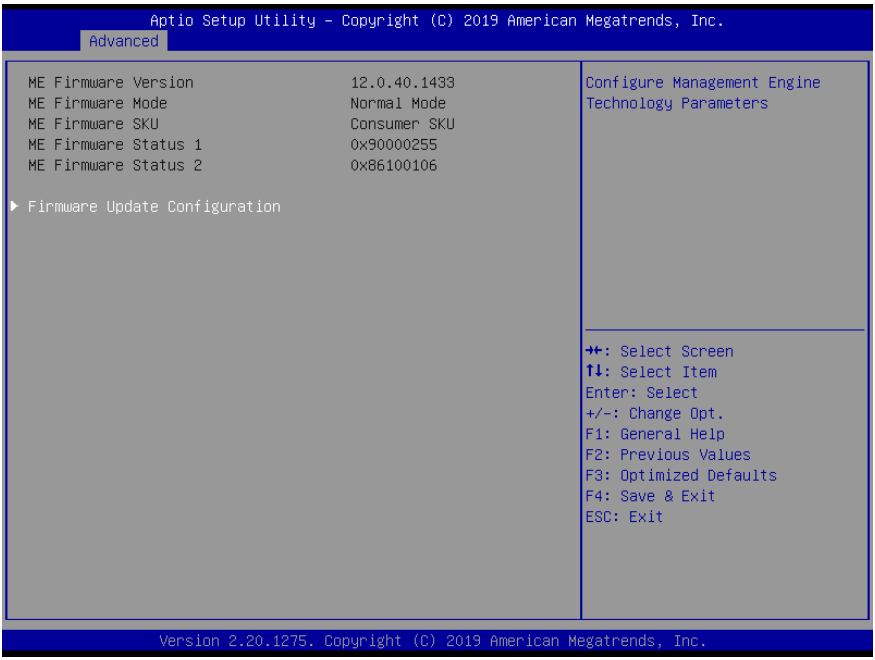


3.4.5.1 Fan 1 Mode Configuration

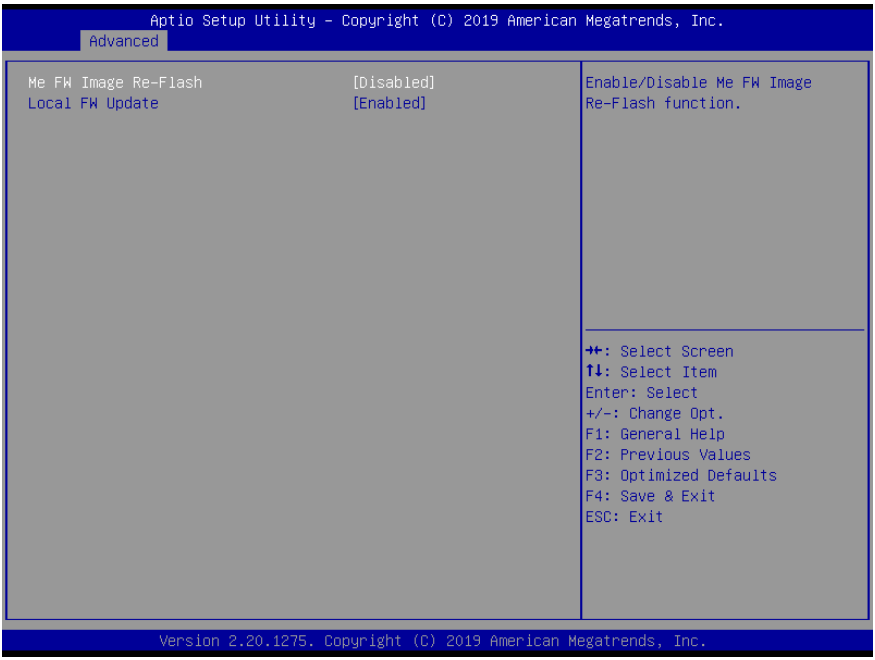


Options Summary		
CPU Smart Fan control	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
PWM signa	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		

3.4.6 PCH-FW Configuration

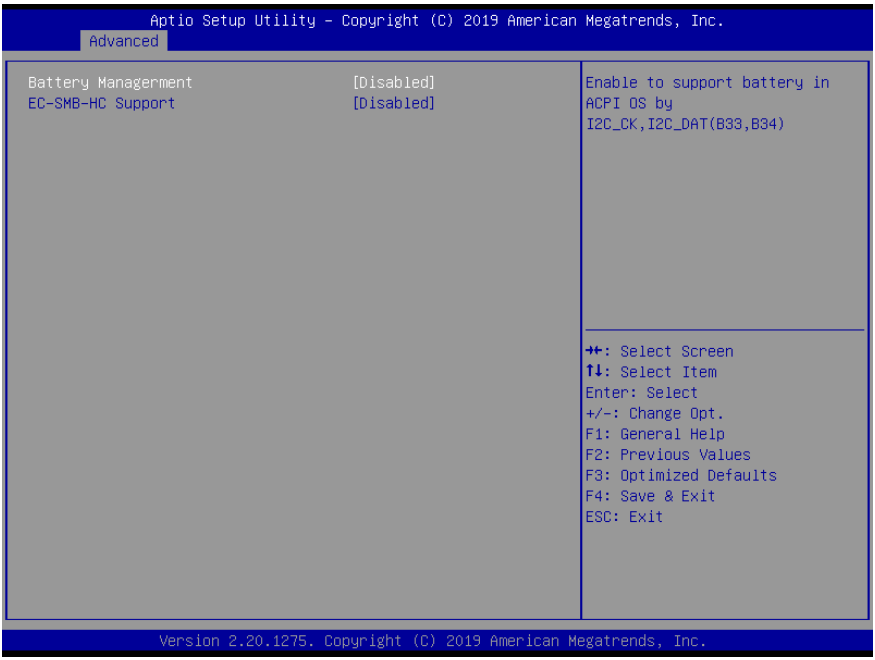


3.4.6.1 Firmware Update Configuration



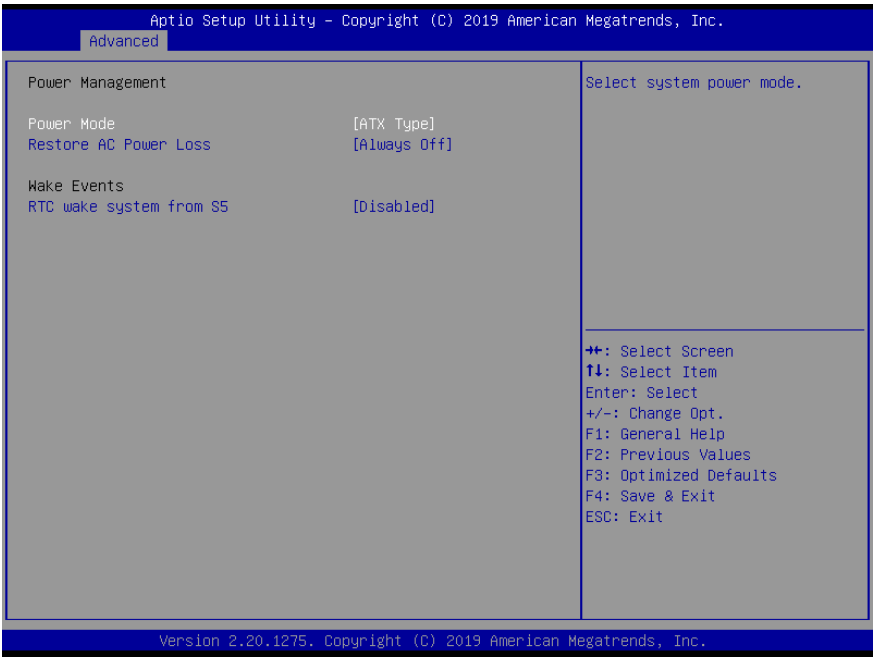
Options Summary		
Me FW Image Re-Flash	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/ Disable Me FW Image Re-Flash Function.		
Local FW Update	Disabled	
	Enabled	Optimal Default, Failsafe Default
Options for Local FW Update function		

3.4.7 On-Module Configuration



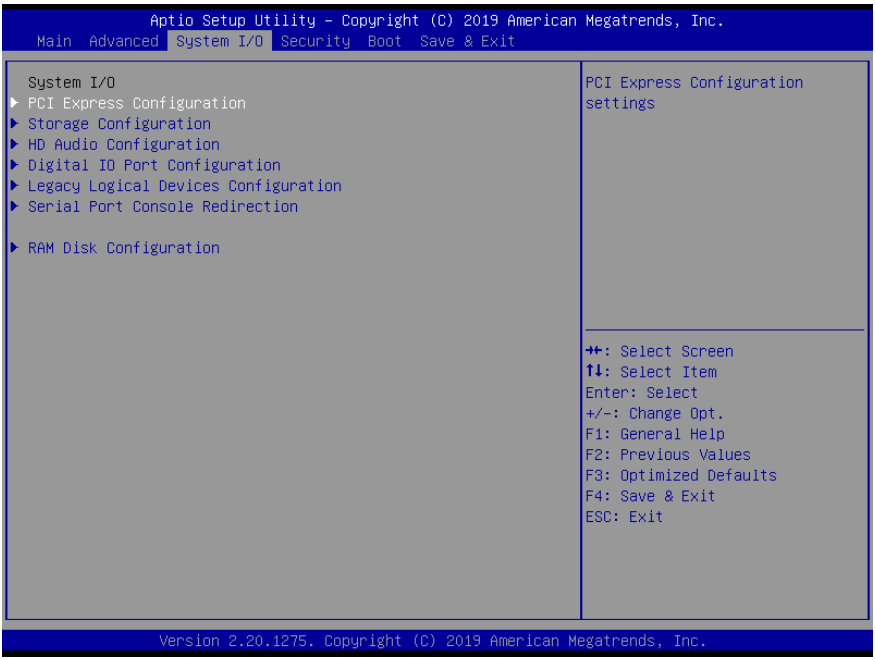
Options Summary		
Battery Managerment	Disabled	Optimal Default, Failsafe Default
	One Battery	
Enable to support battery in ACPI OS by I2C_CK, I2C_DAT(B33,B34)		
EC-SMB-HC Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
SMBus Host Controller Interface via Embedded Controller.		

3.4.8 Power Management

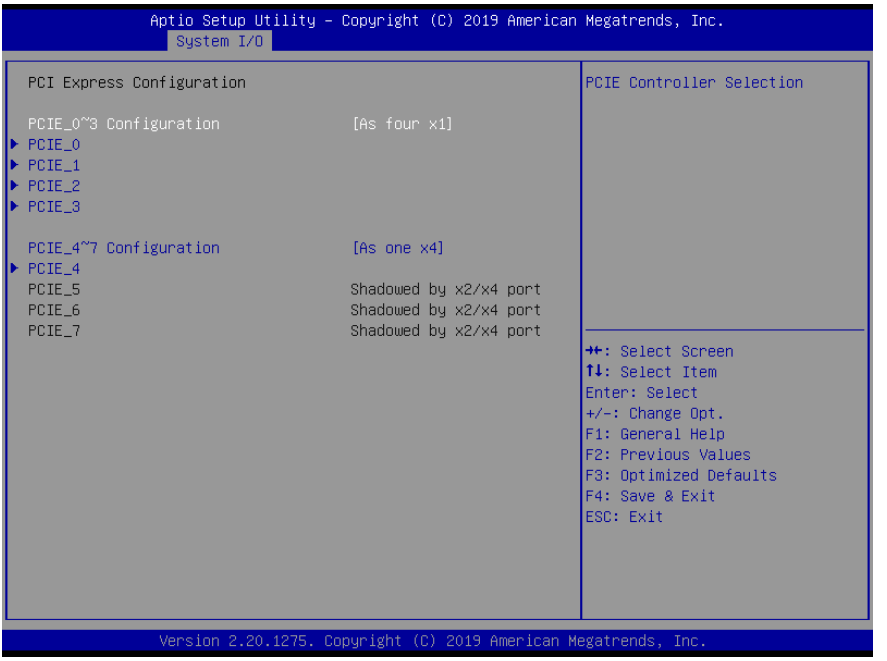


Options Summary		
Power Mode	ATX Type	
	AT Type	Optimal Default, Failsafe Default
Select system power mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
IO Restore AC Power Loss		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
Fixed Time: System will wake on the hr::mn::sec Specified. Dynamic Time: System will wake on the current time + Increase minute(s)		

3.5 System I/O

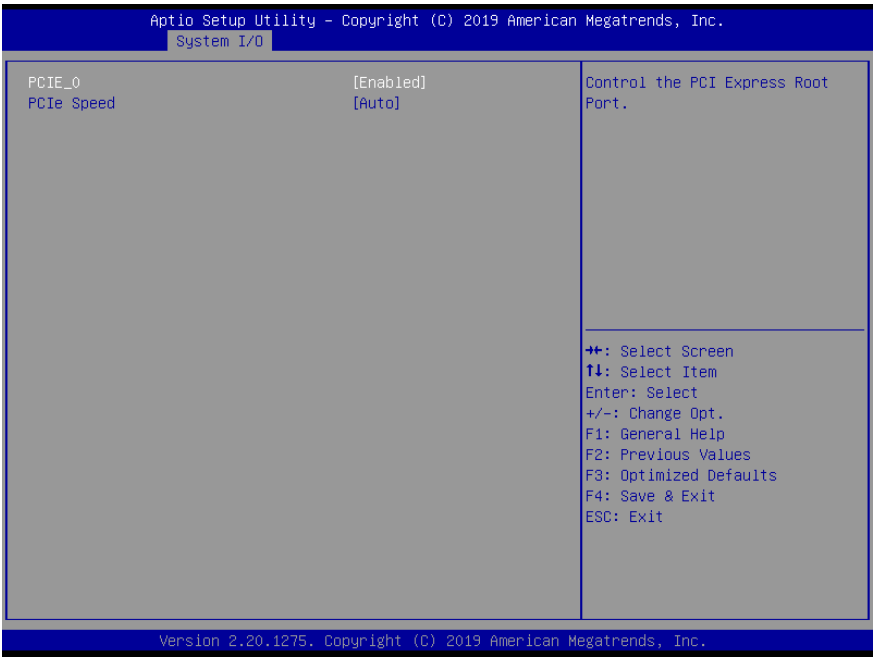

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Main Advanced System I/O Security Boot Save & Exit
System I/O
PCI Express Configuration
Storage Configuration
HD Audio Configuration
Digital IO Port Configuration
Legacy Logical Devices Configuration
Serial Port Console Redirection
RAM Disk Configuration
PCI Express Configuration settings
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.20.1275. Copyright (C) 2019 American Megatrends, Inc.

3.5.1 PCI Express Configuration



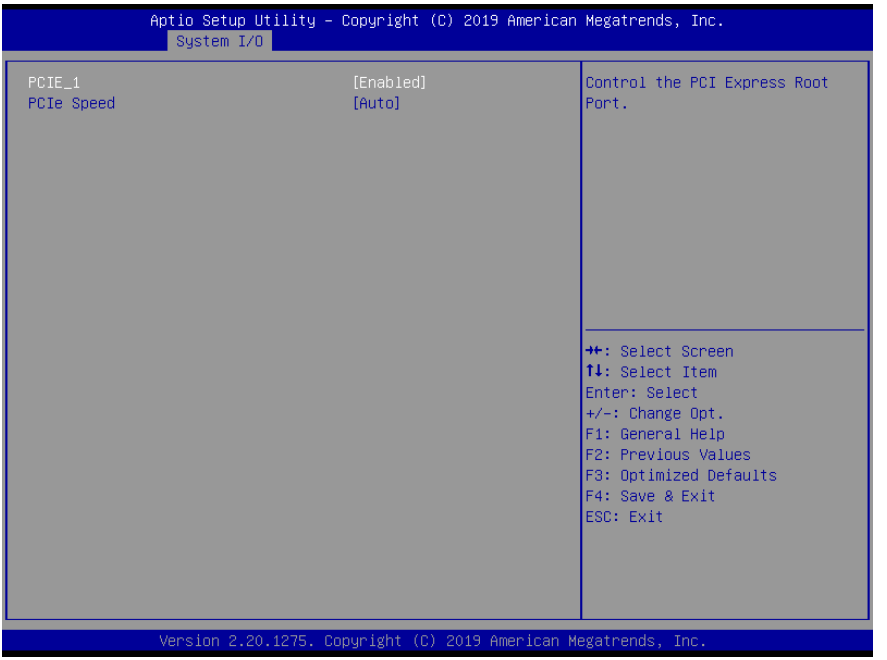
Options Summary		
PCIE_0~3 Configuration	As four x1	Optimal Default, Failsafe Default
	As one x2 and two x1	
	As two x2	
	As one x4	
PCIE Controller Selection		
PCIE_4~7 Configuration	As four x1	
	As one x2 and two x1	
	As two x2	
	As one x4	Optimal Default, Failsafe Default
PCI Express Root Port Settings.		

3.5.1.1 PCI Express Configuration: PCIE_0



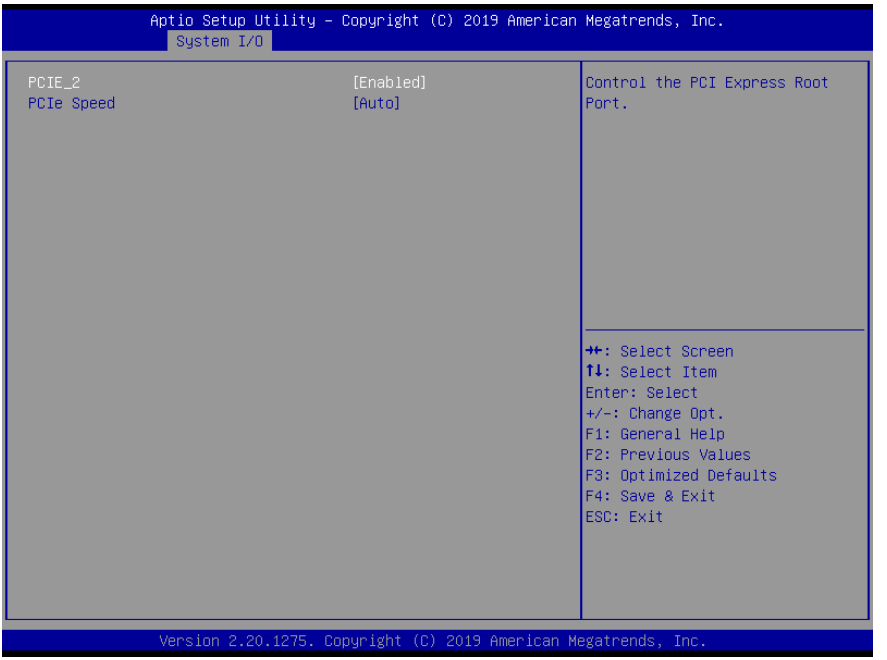
Options Summary		
PCIE_0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.5.1.2 PCI Express Configuration: PCIE_1



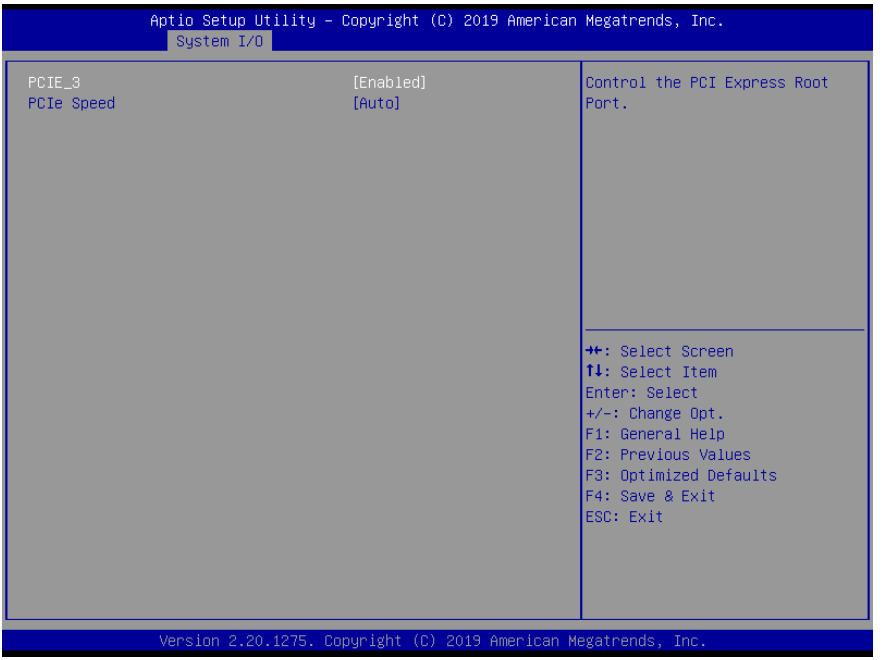
Options Summary		
PCIE_1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.5.1.3 PCI Express Configuration: PCIE_2



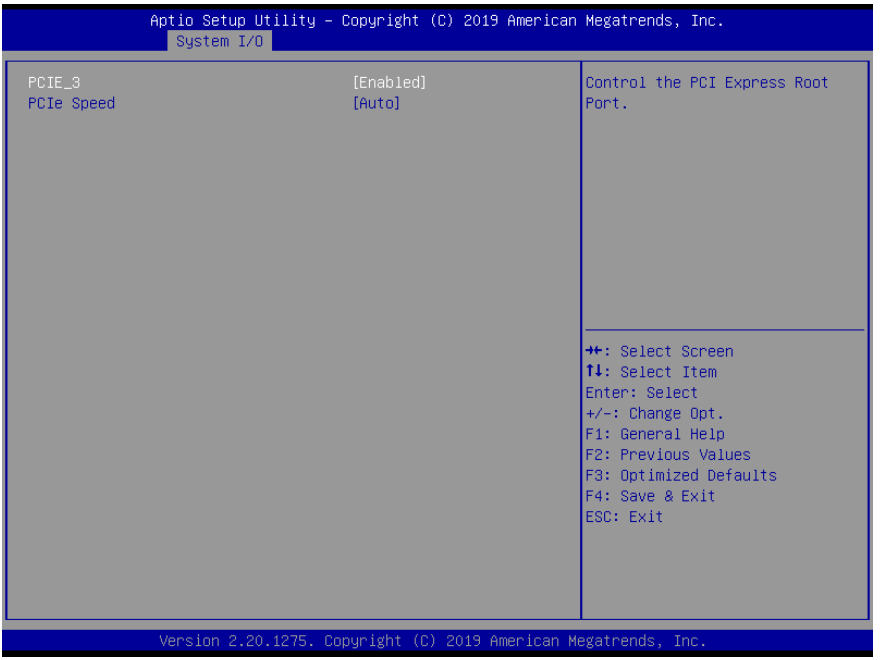
Options Summary		
PCIE_2	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.5.1.4 PCI Express Configuration: PCIE_3



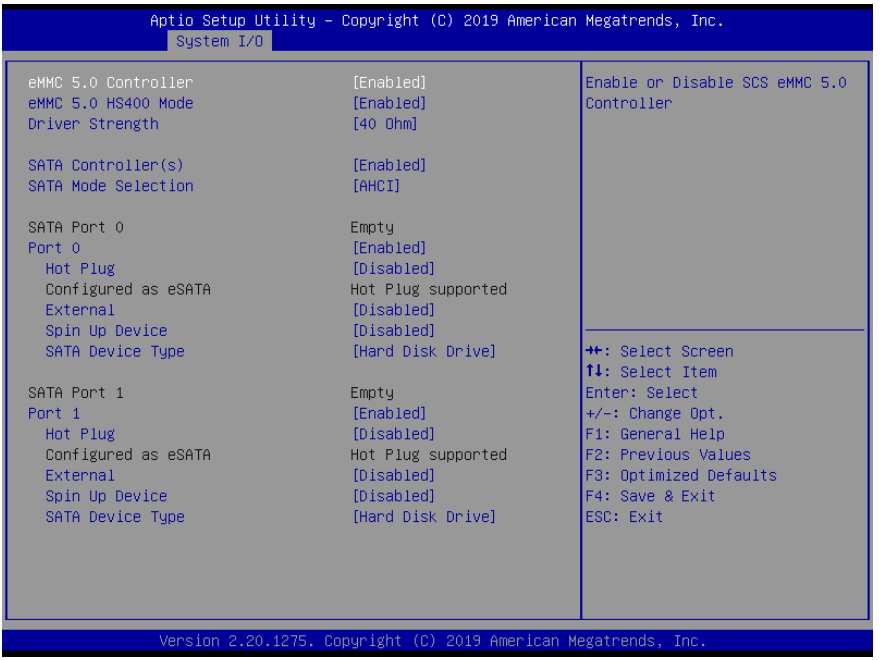
Options Summary		
PCIE_3	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.5.1.5 PCI Express Configuration: PCIE_4



Options Summary		
PCIE_4	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.5.2 Storage Configuration

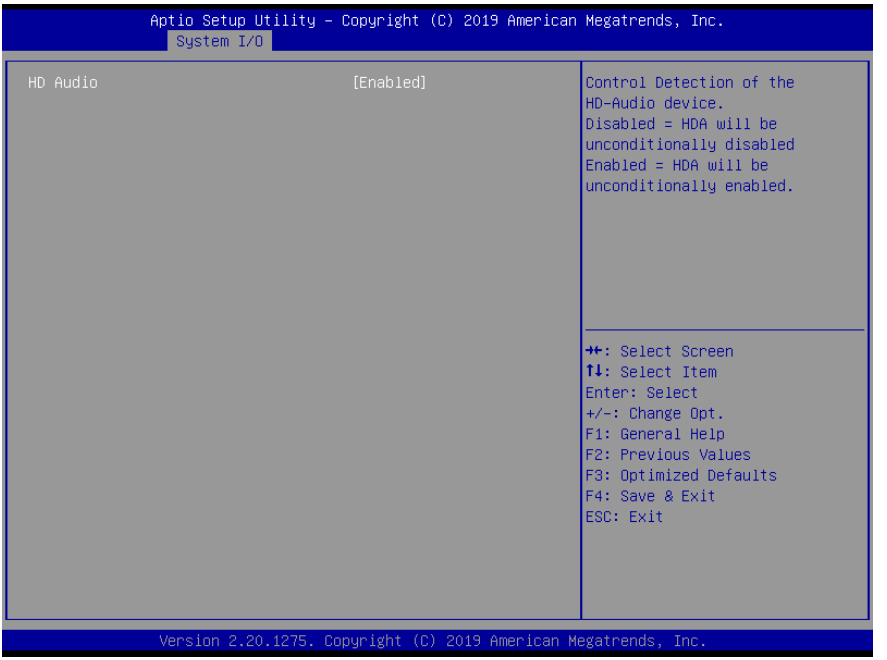


Options Summary		
eMMC 5.0 Controller	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SCS eMMC 5.0 Controller		
eMMC 5.0 HS400 Mode	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SCS eMMC 5.0 HS400 Mode		
Driver Strength	33 Ohm	Optimal Default, Failsafe Default
	40 Ohm	
	50 Ohm	
Sets I/O driver strength		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable SATA Device.		

Table Continues on Next Page

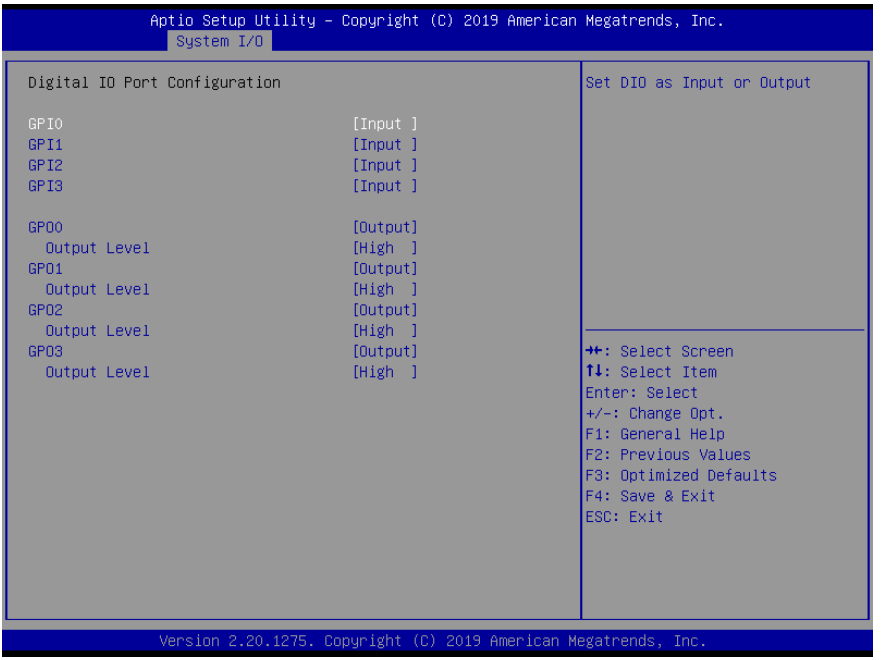
Options Summary		
SATA Mode Selection	AHCI Intel RST Premium with Intel Optane System Acceleration	Optimal Default, Failsafe Default
Determines how SATA controller(s) operate.		
Port 0	Disabled Enabled	Optimal Default, Failsafe Default
Enabled or Disabled SATA Port		
Hot Plug	Disabled Enabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		
External	Disabled Enabled	Optimal Default, Failsafe Default
Marks this port as external.		
Spin Up Device	Disabled Enabled	Optimal Default, Failsafe Default
If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.		
SATA Device Type	Hard Disk Drive Solid State Drive	Optimal Default, Failsafe Default
Identify the SATA port is connected to solid state Drive or Hard Disk Drive		
Port 1	Disabled Enabled	Optimal Default, Failsafe Default
Enabled or Disabled SATA Port		
Hot Plug	Disabled Enabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		
External	Disabled Enabled	Optimal Default, Failsafe Default
Marks this port as external.		
Spin Up Device	Disabled Enabled	Optimal Default, Failsafe Default
If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.		
SATA Device Type	Hard Disk Drive Solid State Drive	Optimal Default, Failsafe Default
Identify the SATA port is connected to solid state Drive or Hard Disk Drive		

3.5.3 HD Audio Configuration



Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled = HDA will be unconditionally disabled Enabled = HDA will be unconditionally enabled.		

3.5.4 Digital IO Port Configuration

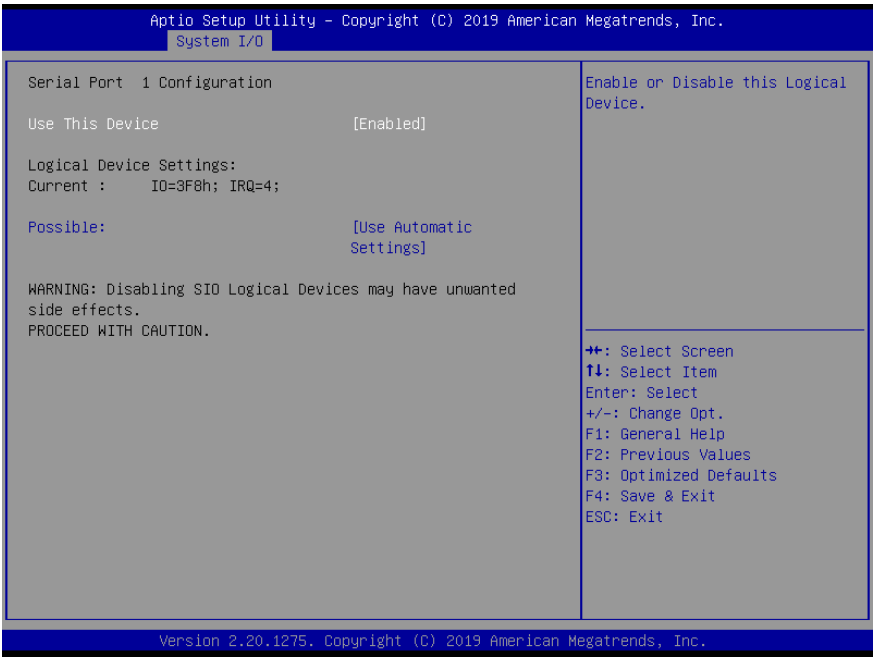


Options Summary		
GPI0	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
GPI1	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
GPI2	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
GPI3	Input	Optimal Default, Failsafe Default
	Output	
Set DIO as Input or Output		
GPO0	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		

Options Summary		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
GPO1	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
GPO2	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		
GPO3	Input	
	Output	Optimal Default, Failsafe Default
Set DIO as Input or Output		
Output Level	Low	
	High	Optimal Default, Failsafe Default
Set output level when DIO pin is output		

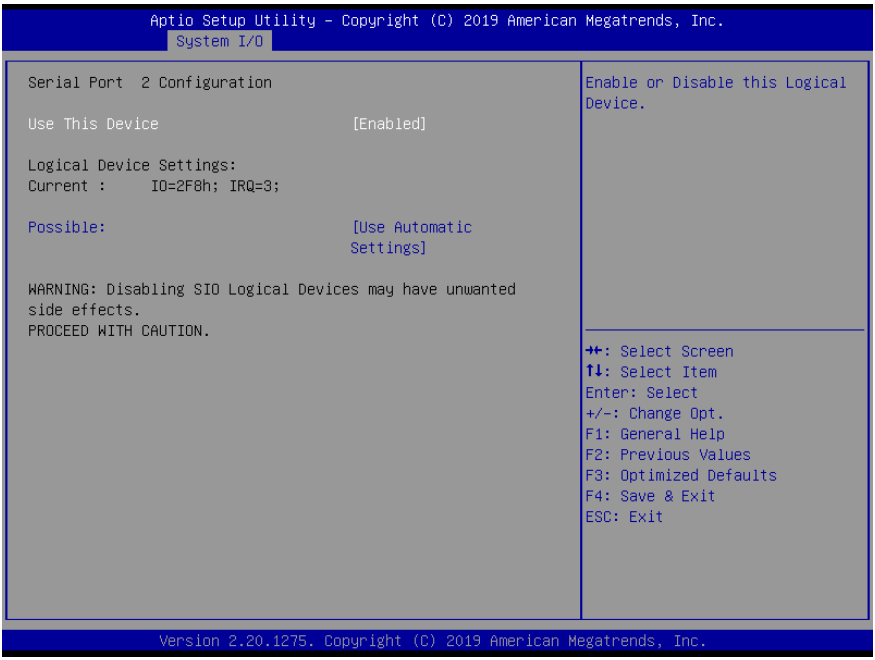
3.5.5 SIO Configuration

3.5.5.1 Serial Port 1 Configuration



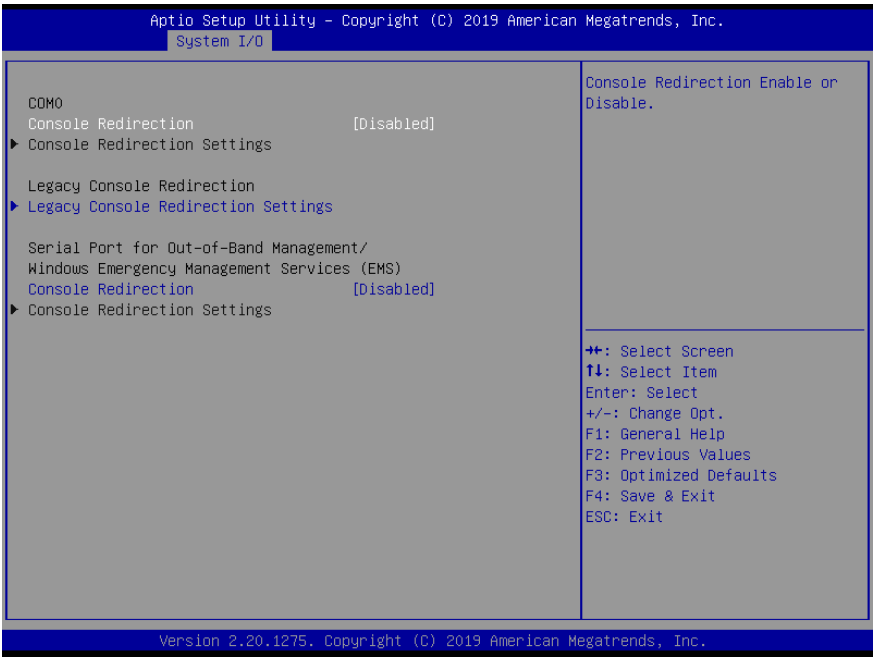
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4; DMA;	
	IO=2C8h; IRQ=11; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.5.2 Serial Port 2 Configuration



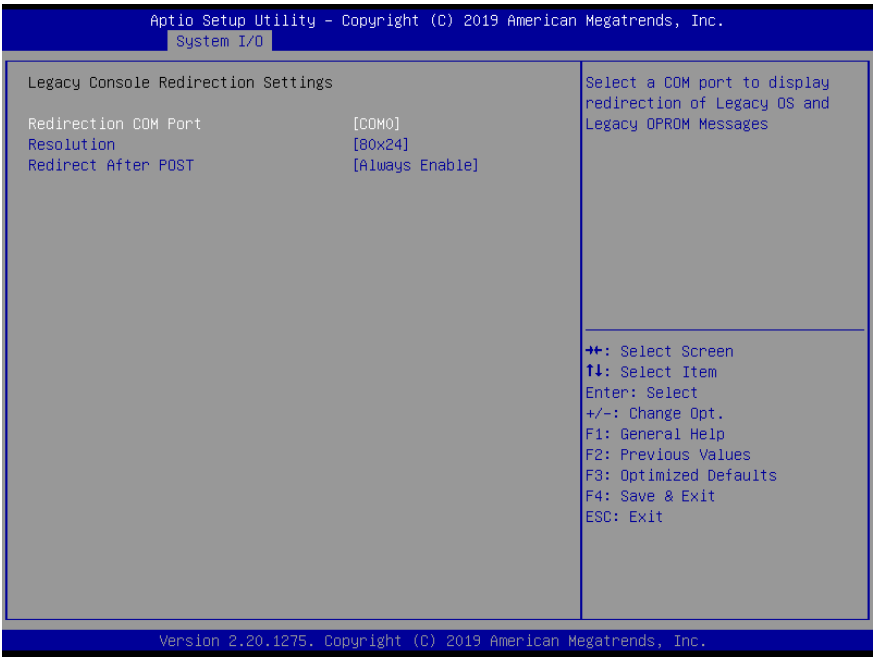
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3 DMA;	
	IO=2D8h; IRQ=10; DMA;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		

3.5.6 Serial Port Console Redirection



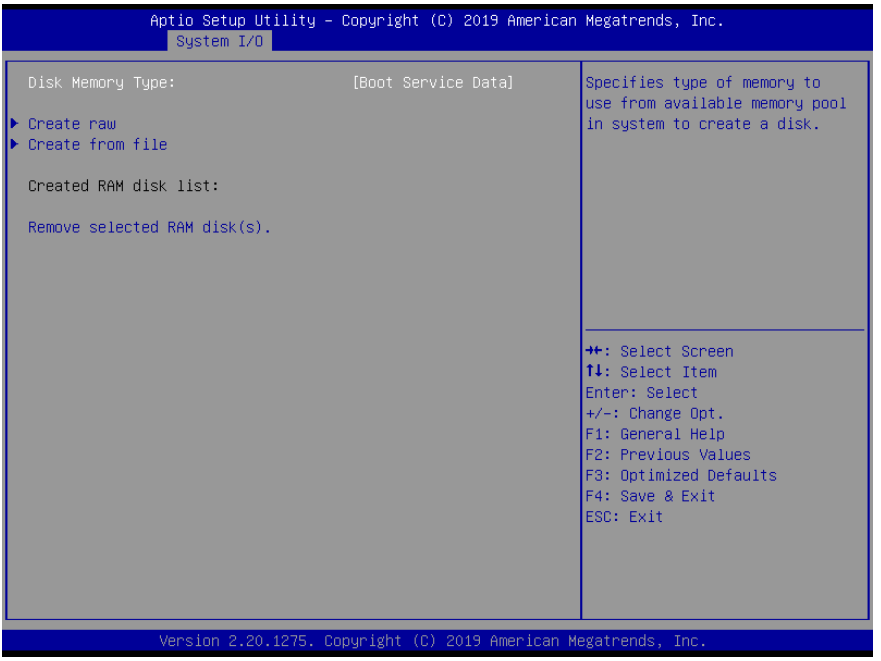
Options Summary		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.5.6.1 Legacy Console Redirection Settings



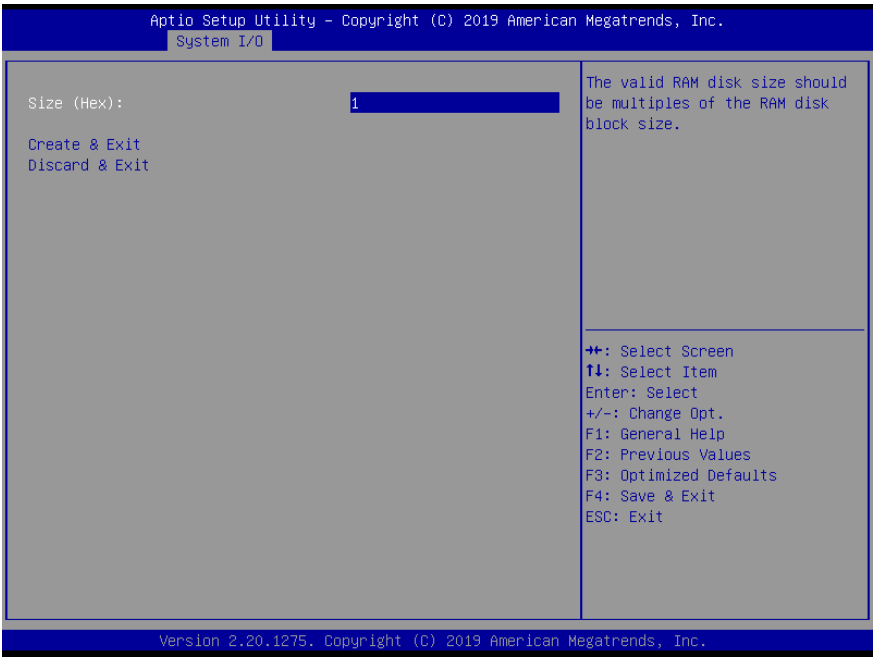
Options Summary		
Redirection COM Port	COM0	Optimal Default, Failsafe Default
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages		
Resolution	80x24	Optimal Default, Failsafe Default
	80x25	
On Legacy OS, the Number of Rows and Columns supported redirection		
Redirect After POST	Always Enable	Optimal Default, Failsafe Default
	BootLoader	
When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.		

3.5.7 RAM Disk Configuration



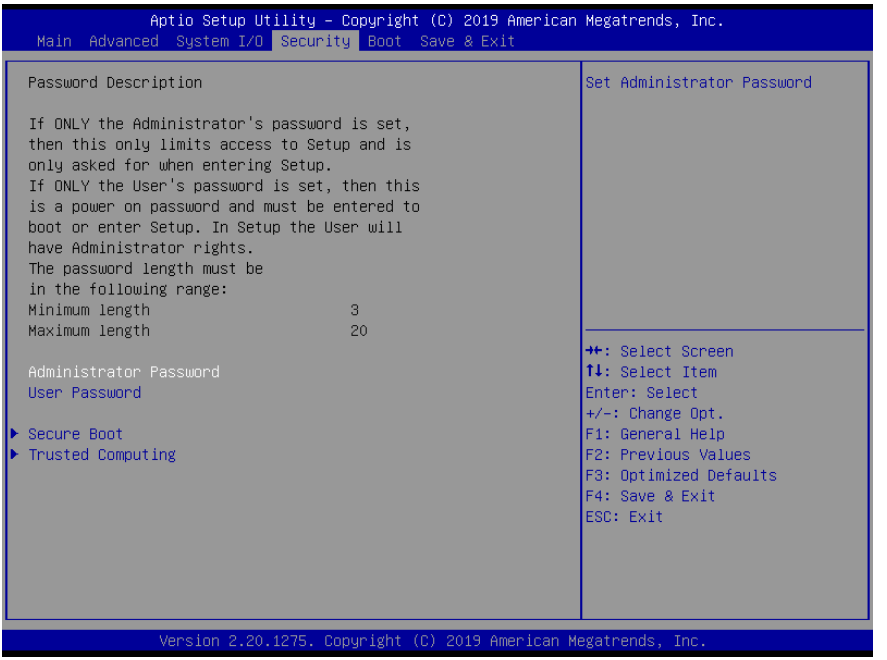
Options Summary		
Disk Memory Type:	Boot Service Data	Optimal Default, Failsafe Default
	Reserved	
Specifies type of memory to use from available memory pool in system to create a disk.		
Create from file	HDD Unknown 96MB	Optimal Default, Failsafe Default
Create a RAM disk from a given file.		
RAM Disk 0: [0x8728E018, 0x8728F017]	Disabled	Optimal Default, Failsafe Default
	Enabled	
Select for remove		
Remove selected RAM disk(s).		
Remove selected RAM disk(s)		

3.5.7.1 RAM Disk Configurator: Create Raw



Options Summary		
Size (Hex)	1	Optimal Default, Failsafe Default
The valid RAM disk size should be multiples of the RAM disk block size.		
Create & Exit		
Create a new RAM disk with the given starting and ending address.		
Discard & Exit		
Discard and exit.		

3.6 Security



Change Administrator/User Password

You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility.

Select the password you want to set and press <Enter>. A dialog box will appear which lets you set the password. Passwords must be between 3 and 20 letters or numbers. Press <Enter> and re-enter the password into the next dialog box that appears. Press <Enter> after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

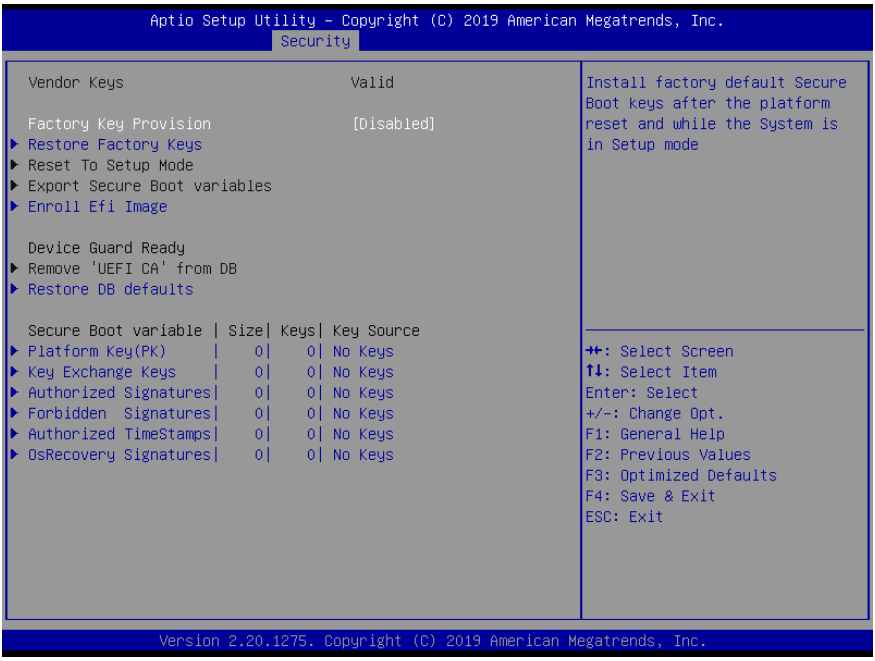
Remove Password

Highlight this item and type in the current password. At the next dialog box press <Enter> to disable password protection.

3.6.1 Security: Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset		
Secure Boot Mode	Standard	
	Custom	Optimal Default, Failsafe Default
Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication		
Restore Factory Keys	Yes	Optimal Default, Failsafe Default
	No	
Force System to User Mode. Install factory default Secure Boot key databases		

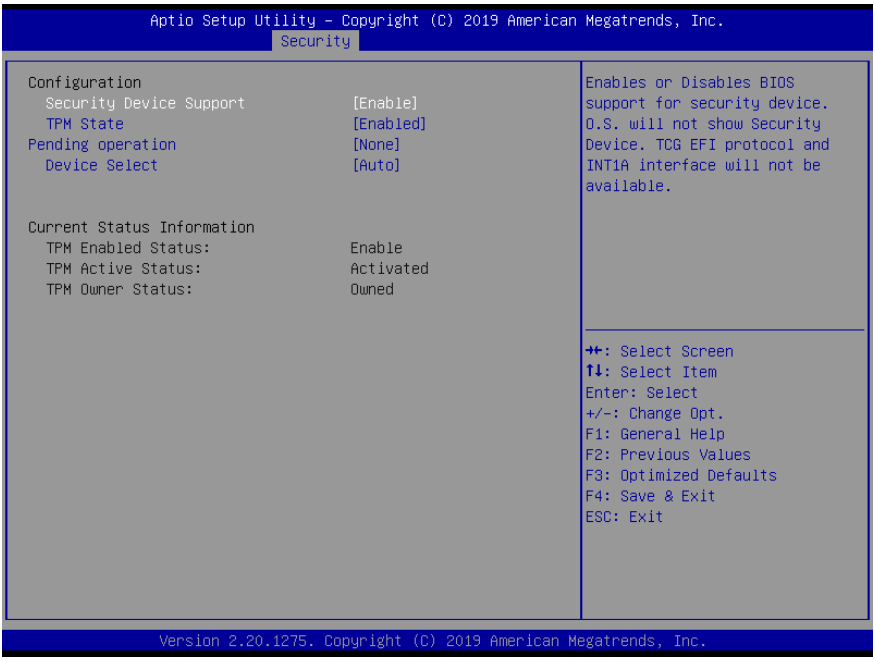
3.6.1.1 Secure Boot: Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode		
Restore Factory Keys	Yes	Optimal Default, Failsafe Default
	No	
Force System to User Mode. Install factory default Secure Boot key databases		
Enroll Efi Image	Acpi(a0341d0, 0)\PCI(1A|0)\DevicePath(Type 3, SubType 29)HD(Part2, Sig ?)\	Optimal Default, Failsafe Default
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)		

Options Summary		
Restore DB defaults	Yes	Optimal Default, Failsafe Default
	No	
Restore DB variable to factory defaults		
Platform Key(PK) | 0| 0| No Keys	Update	Optimal Default, Failsafe Default
Key Exchange Keys| 0| 0| No Keys	Update	Optimal Default, Failsafe Default
	Append	
Authorized Signatures| 0| 0| No Keys	Update	Optimal Default, Failsafe Default
	Append	
Forbidden Signatures| 0| 0| No Keys	Update	Optimal Default, Failsafe Default
	Append	
Authorized TimeStamps| 0| 0| No Keys	Update	Optimal Default, Failsafe Default
	Append	
OsRecovery Signatures | 0| 0| No Keys	Update	Optimal Default, Failsafe Default
	Append	
Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image (SHA256) Key Source: Factory, External, Mixed		

3.6.2 Trusted Computing

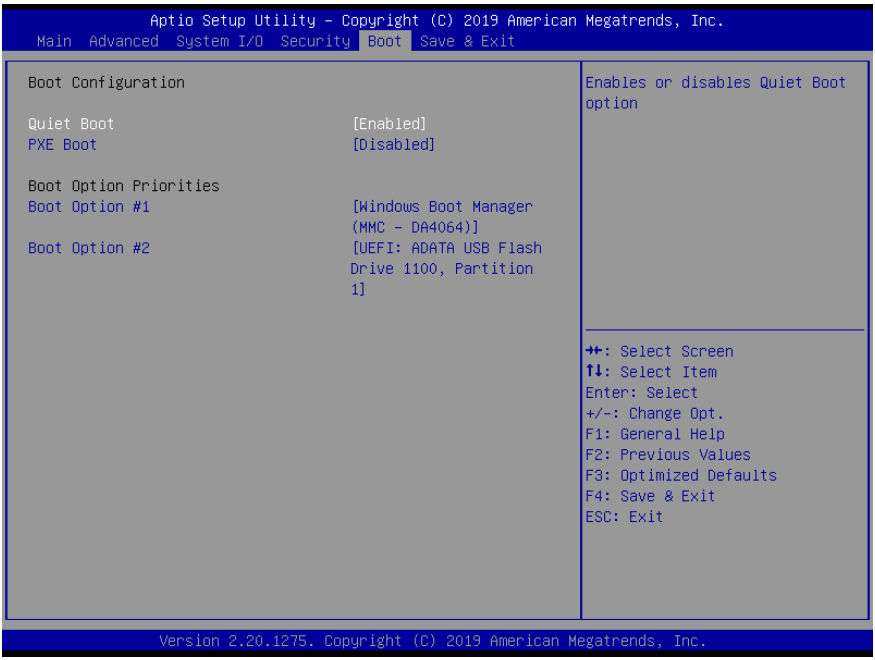


Options Summary		
Security Device Support	Disable	Optimal Default, Failsafe Default
	Enable	
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
TPM State	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Table Continues on Next Page

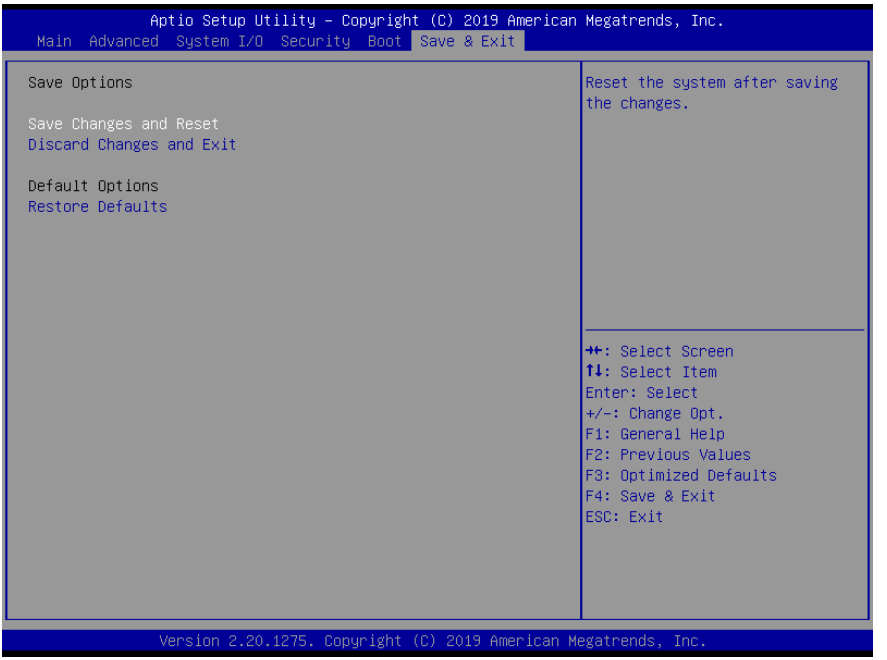
Options Summary		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 Devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

3.7 Setup submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Restore DB variable to factory defaults		
PXE Boot	Disabled	Optimal Default, Failsafe Default
	UEFI	
Controls the execution of UEFI and Legacy Network OpROM		

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the COM-WHUC6 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/com-express-modules-com-whuc6

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Click the **STEP1 - Chipset** folder.
2. Open the **SetupChipset.exe** file.
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Click the **STEP2 - Graphic** folder.
2. Open the **igxpin.exe** file.
3. Follow the instructions.
4. Drivers will be installed automatically.

Step 3 – Install Network Driver

1. Click the **STEP3 - Network** folder.
2. Open the **ProWinx64.exe** file.
3. Follow the instructions.
4. Drivers will be installed automatically.

Step 4 – Install Audio Driver

1. Click the **STEP4 - Audio** folder.
2. Open the **0006-64bit_Win7_Win8_Win81_Win10_R279.exe** file.
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Intel Management Engine Driver

1. Click the **STEP5 – Intel Management Engine** then open folder for your OS.
2. Open the **MEISetup.exe** file.
3. Follow the instructions.
4. Drivers will be installed automatically.

Appendix A

Watchdog Timer

A.1 Watchdog Timer Initial Program

Table 1: Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2: Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte    EcBRAMIndex    //This parameter is represented from Note1
#define byte    EcBRAMData     //This parameter is represented from Note2
#define byte    BRAMLDNReg     //This parameter is represented from Note3
#define byte    BRAMFnDataReg  //This parameter is represented from Note4
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte    TimerReg    //This parameter is represented from Note5
#define byte    TimerVal    // This parameter is represented from Note10
#define byte    UnitReg     //This parameter is represented from Note6
#define byte    UnitBit     //This parameter is represented from Note7
#define byte    UnitVal     //This parameter is represented from Note11
#define byte    RSTReg      //This parameter is represented from Note8
#define byte    RSTBit      //This parameter is represented from Note9
#define byte    RSTVal      //This parameter is represented from Note12
*******************************************************************************
```

```
*******************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*******************************************************************************
```

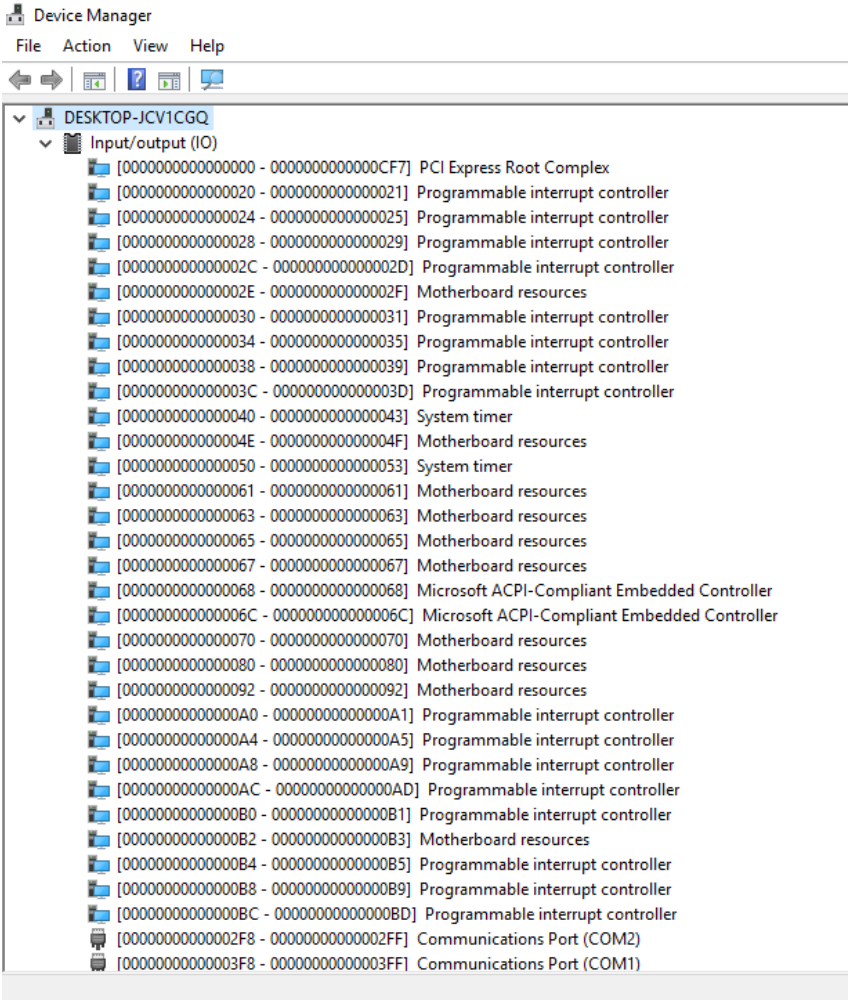
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
         WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(0);
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte Value){
        ECBRAMWriteByte(TimerReg , Value);
}

VOID    WDTParameterSetting(){
        Byte TempByte;

         // Watchdog Timer counter setting
         ECBRAMWriteByte(TimerReg , TimerVal);
        // WDT counting unit setting
         TempByte = ECBRAMReadByte(UnitReg);
         TempByte |= (UnitVal << UnitBit);
         ECBRAMWriteByte(UnitReg , TempByte);
         // WDT RST pulse width setting
         TempByte = ECBRAMReadByte(RSTReg);
         TempByte |= (RSTVal << RSTBit);
         ECBRAMWriteByte(RSTReg , TempByte);
}
*******************************************************************************
```

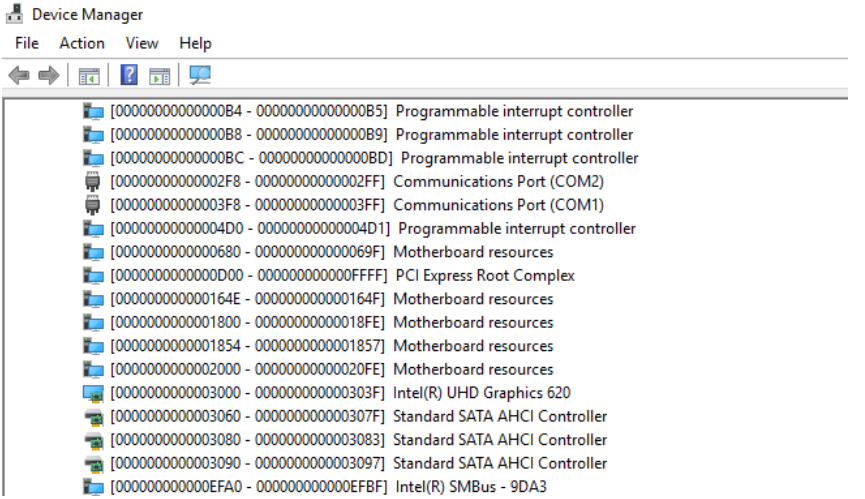
```
*******************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*******************************************************************************
```

Appendix B

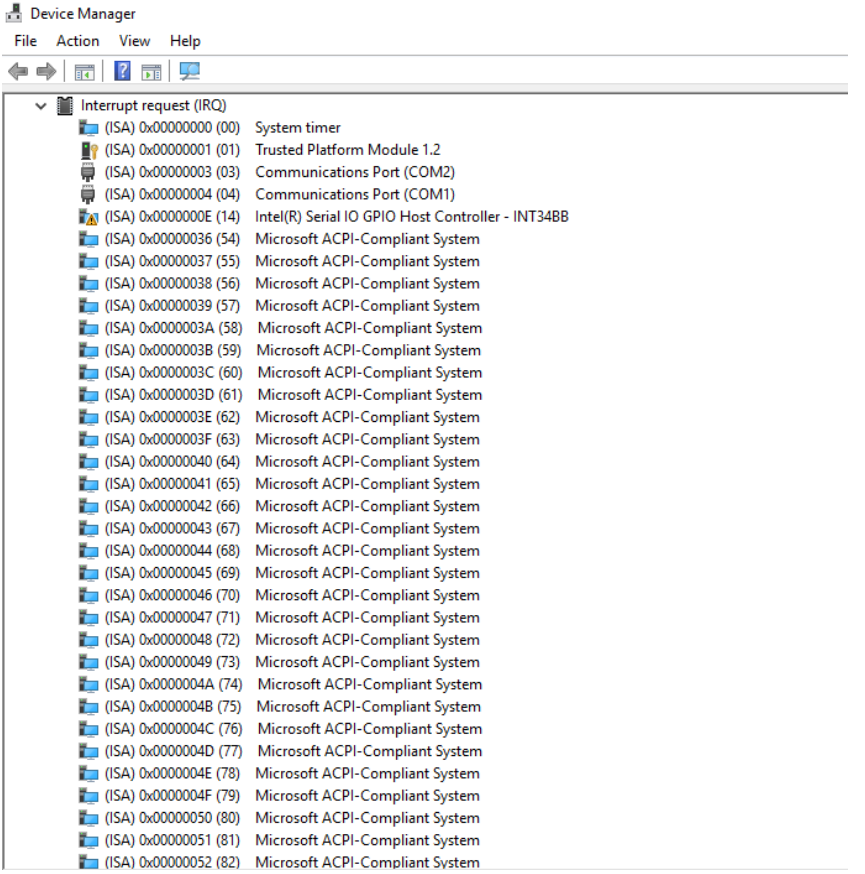
I/O Information

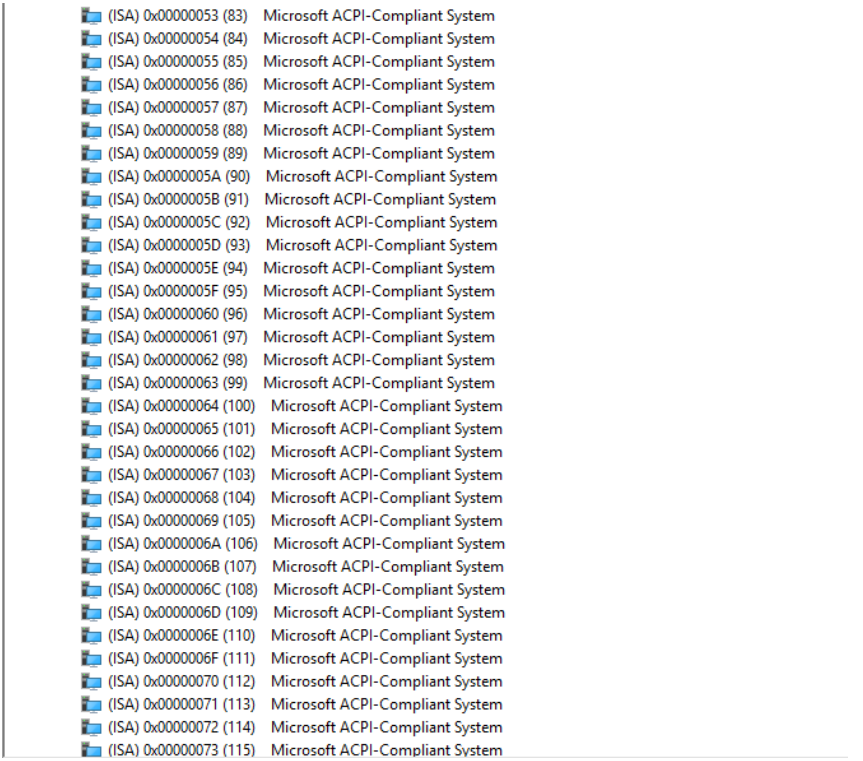
B.1 I/O Address Map

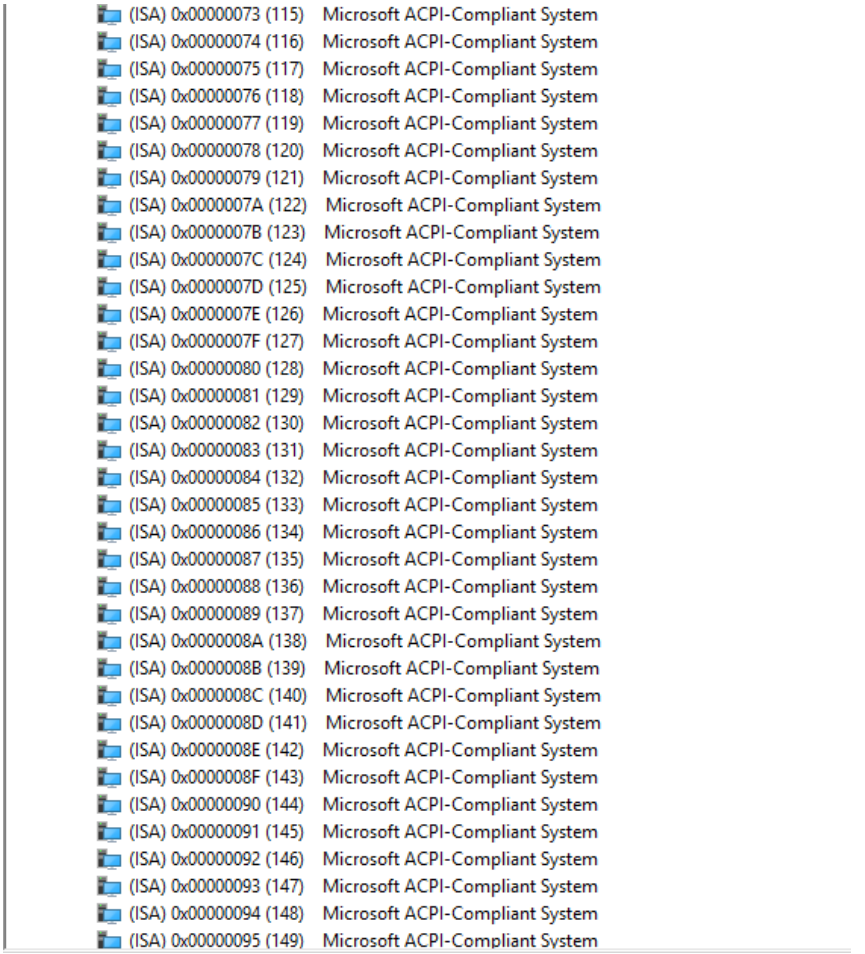



Device Manager
File Action View Help
[00000000000000B4 - 00000000000000B5] Programmable interrupt controller
[00000000000000B8 - 00000000000000B9] Programmable interrupt controller
[00000000000000BC - 00000000000000BD] Programmable interrupt controller
[00000000000002F8 - 00000000000002FF] Communications Port (COM2)
[00000000000003F8 - 00000000000003FF] Communications Port (COM1)
[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 00000000000018FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[0000000000002000 - 00000000000020FE] Motherboard resources
[0000000000003000 - 000000000000303F] Intel(R) UHD Graphics 620
[0000000000003060 - 000000000000307F] Standard SATA AHCI Controller
[0000000000003080 - 0000000000003083] Standard SATA AHCI Controller
[0000000000003090 - 0000000000003097] Standard SATA AHCI Controller
[000000000000EFA0 - 000000000000EFBF] Intel(R) SMBus - 9DA3

B.2 Interrupt Request (IRQ) Address Map




(ISA) 0x00000053 (83) Microsoft ACPI-Compliant System
(ISA) 0x00000054 (84) Microsoft ACPI-Compliant System
(ISA) 0x00000055 (85) Microsoft ACPI-Compliant System
(ISA) 0x00000056 (86) Microsoft ACPI-Compliant System
(ISA) 0x00000057 (87) Microsoft ACPI-Compliant System
(ISA) 0x00000058 (88) Microsoft ACPI-Compliant System
(ISA) 0x00000059 (89) Microsoft ACPI-Compliant System
(ISA) 0x0000005A (90) Microsoft ACPI-Compliant System
(ISA) 0x0000005B (91) Microsoft ACPI-Compliant System
(ISA) 0x0000005C (92) Microsoft ACPI-Compliant System
(ISA) 0x0000005D (93) Microsoft ACPI-Compliant System
(ISA) 0x0000005E (94) Microsoft ACPI-Compliant System
(ISA) 0x0000005F (95) Microsoft ACPI-Compliant System
(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
(ISA) 0x00000066 (102) Microsoft ACPI-Compliant System
(ISA) 0x00000067 (103) Microsoft ACPI-Compliant System
(ISA) 0x00000068 (104) Microsoft ACPI-Compliant System
(ISA) 0x00000069 (105) Microsoft ACPI-Compliant System
(ISA) 0x0000006A (106) Microsoft ACPI-Compliant System
(ISA) 0x0000006B (107) Microsoft ACPI-Compliant System
(ISA) 0x0000006C (108) Microsoft ACPI-Compliant System
(ISA) 0x0000006D (109) Microsoft ACPI-Compliant System
(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System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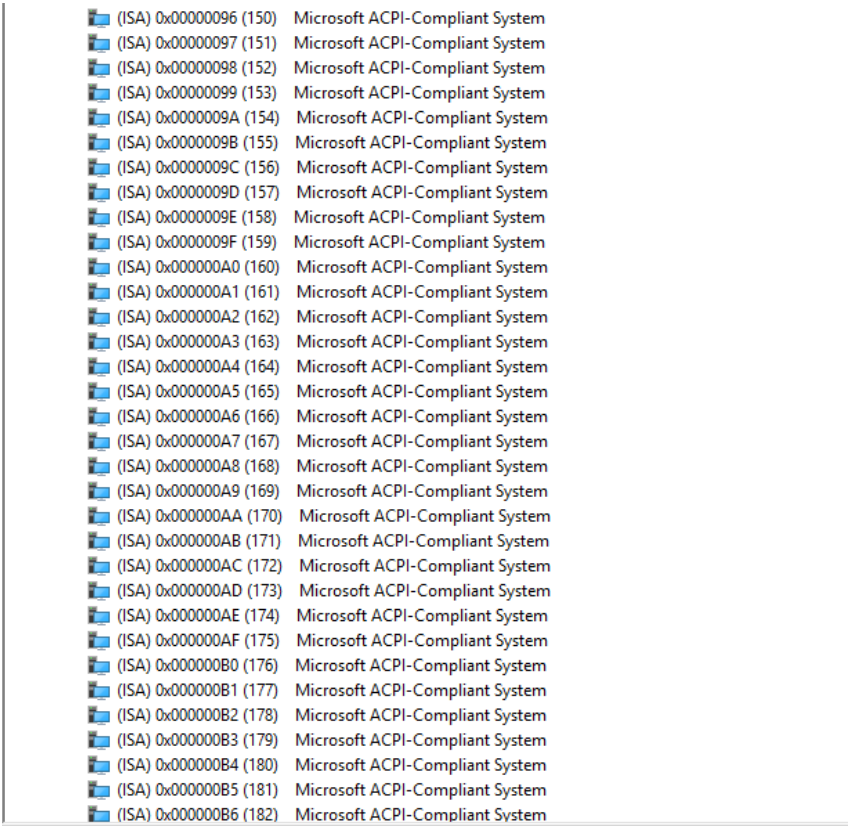
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System


(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
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(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
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(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
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(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
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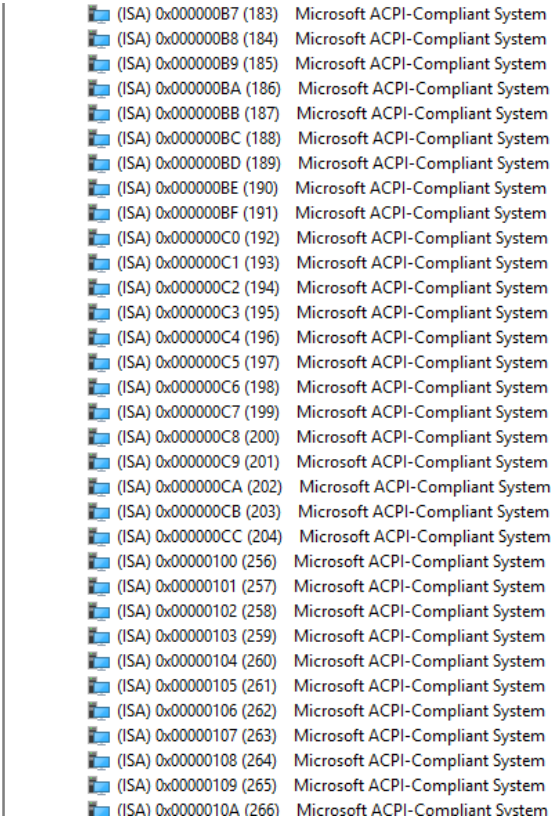
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
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(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
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(ISA) 0x000000C9 (201) Microsoft ACPI-Compliant System
(ISA) 0x000000CA (202) Microsoft ACPI-Compliant System
(ISA) 0x000000CB (203) Microsoft ACPI-Compliant System
(ISA) 0x000000CC (204) Microsoft ACPI-Compliant System
(ISA) 0x00000100 (256) Microsoft ACPI-Compliant System
(ISA) 0x00000101 (257) Microsoft ACPI-Compliant System
(ISA) 0x00000102 (258) Microsoft ACPI-Compliant System
(ISA) 0x00000103 (259) Microsoft ACPI-Compliant System
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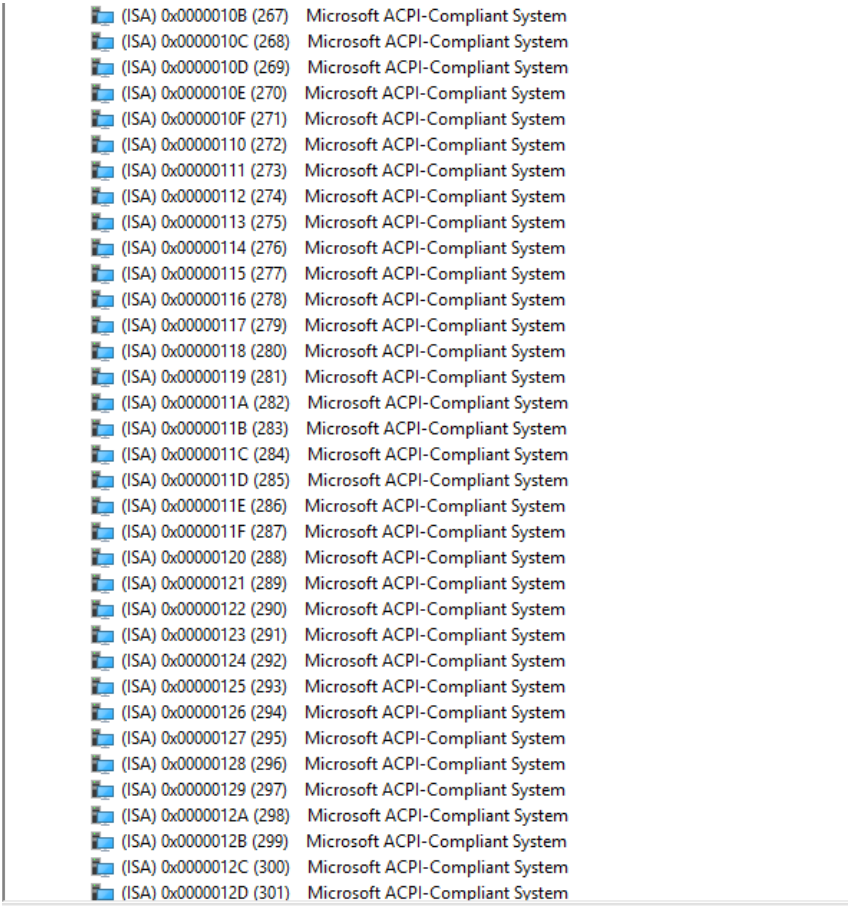
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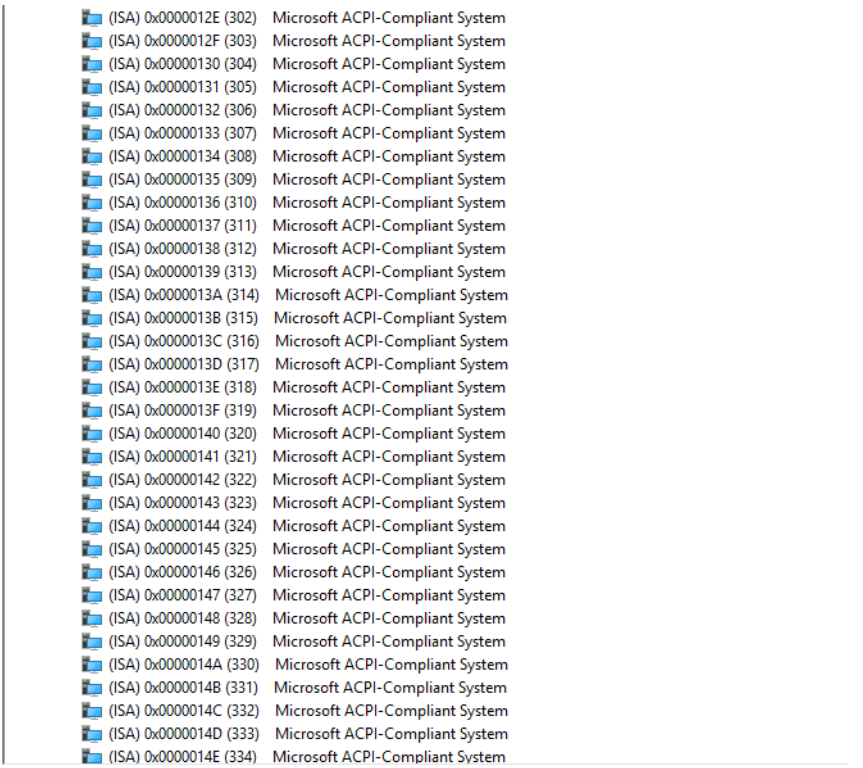
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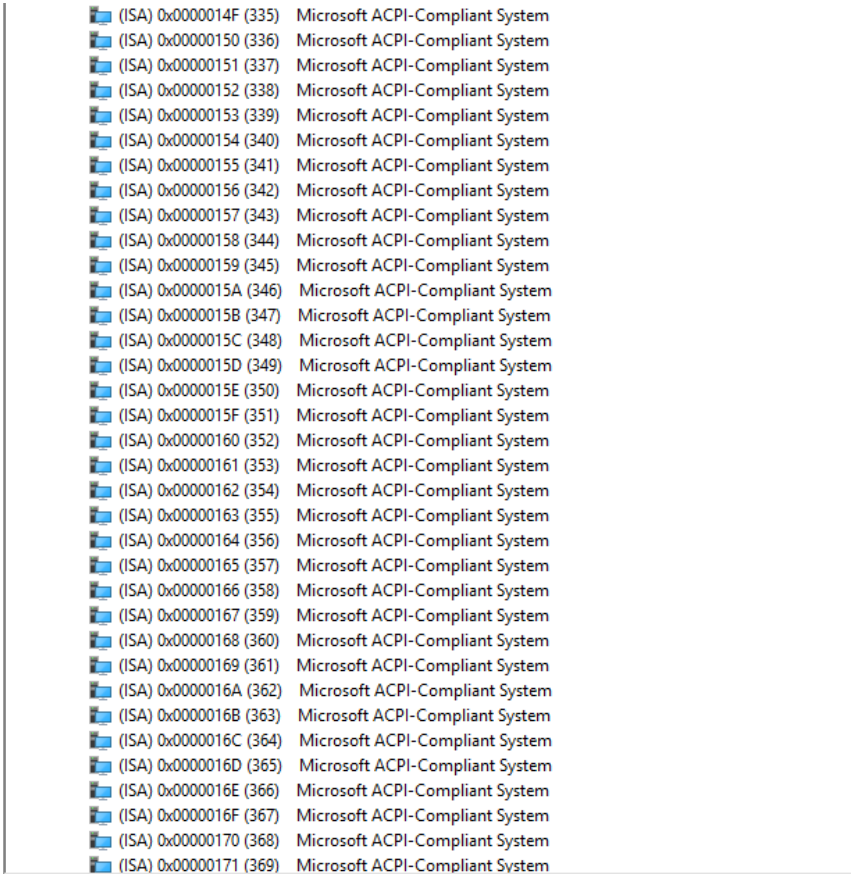
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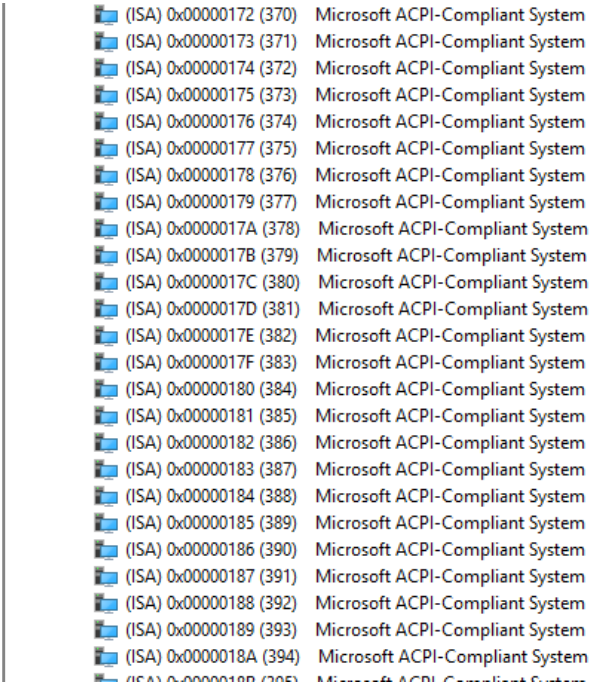
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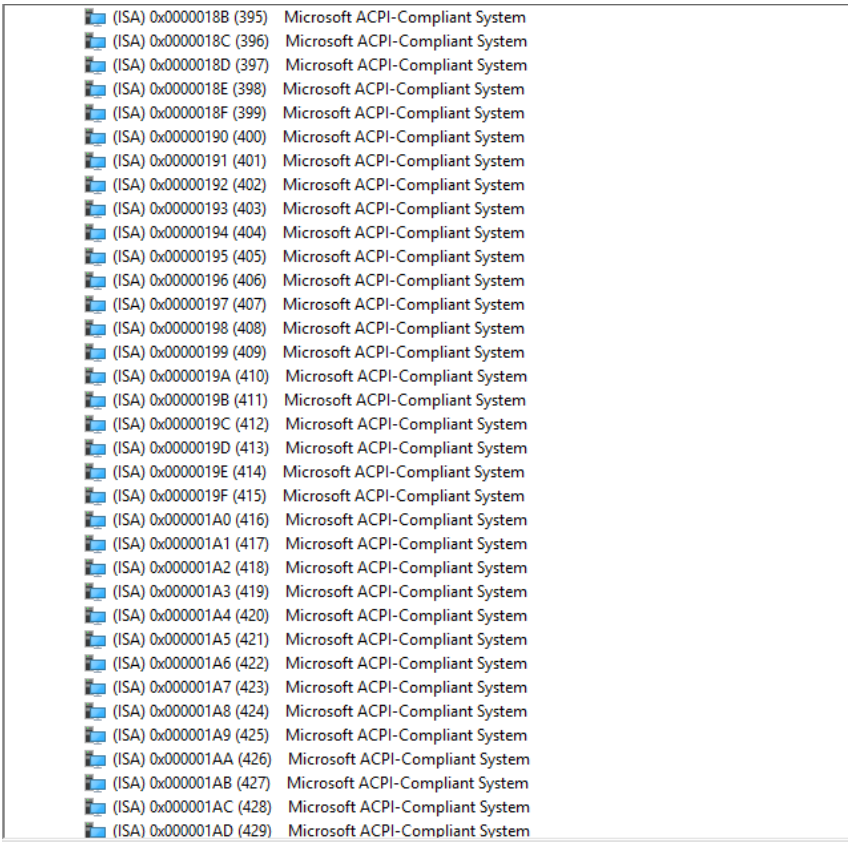
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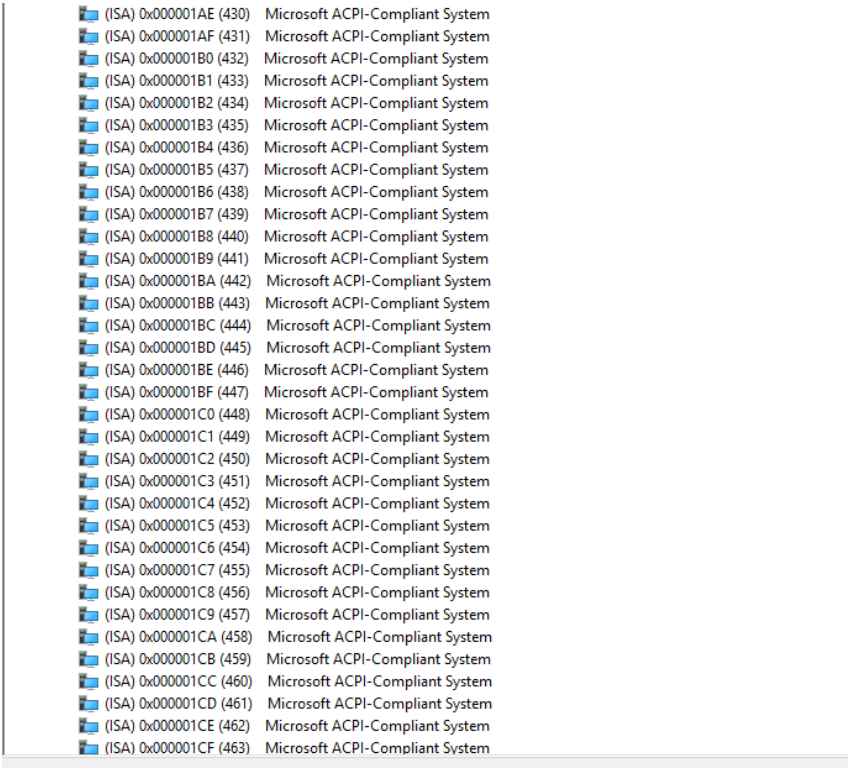
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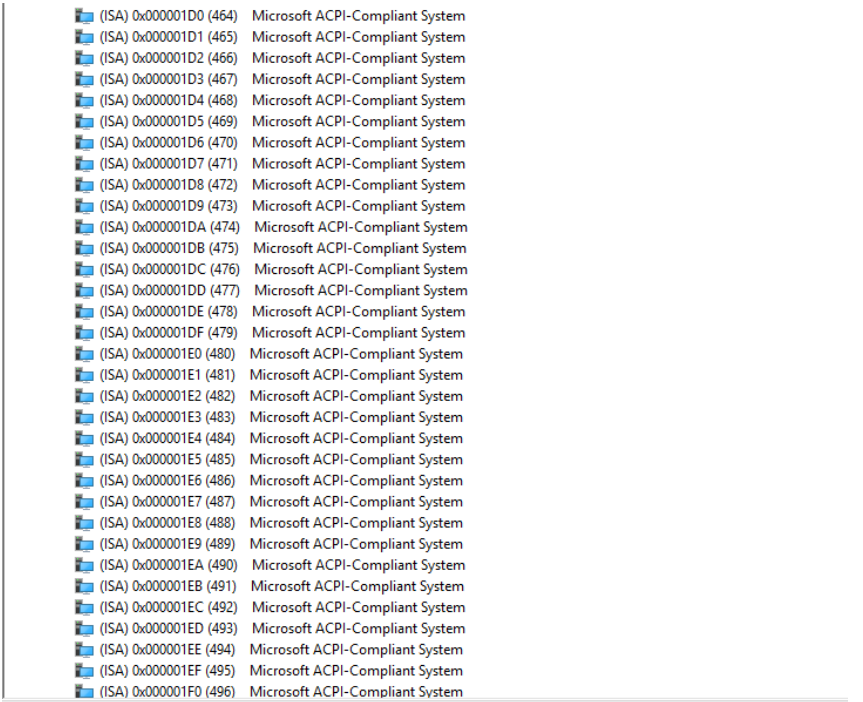
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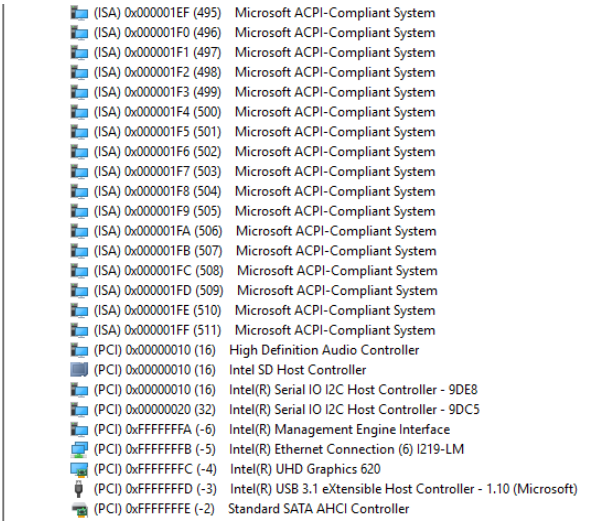
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(PCI) 0xFFFFFFFB (-5) Intel(R) Ethernet Connection (6) I219-LM
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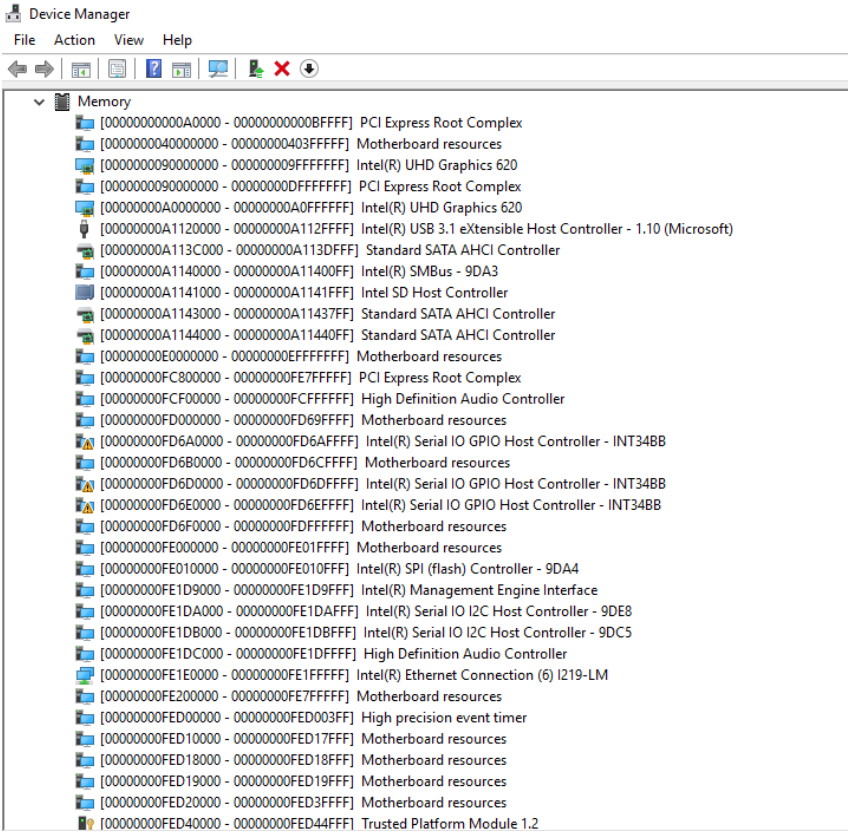
B.3 Memory Address Map



Appendix C

Programming Digital I/O

C.1 Digital I/O Programming

The COM-WHUC6 utilizes an AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration, which you can use to develop a customized program to fit your application.

C.2 Digital I/O Register

Table 1: Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watchdog Logical Device Number
IO Direction Function and Device Number	0x00(Note4)	DIO Input/ Output Function/Device Number
IO Vaule/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2: Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

C.3 Digital I/O Sample Program

```
**********************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte    EcBRAMIndex    //This parameter is represented from Note1
#define byte    EcBRAMData     //This parameter is represented from Note2
#define byte    BRAMLDNReg     //This parameter is represented from Note3
#define byte    BRAMFnData0Reg     //This parameter is represented from Note4
#define byte    BRAMFnData1Reg     //This parameter is represented from Note5
#define    void    EcBRAMWriteByte(byte Offset, byte Value);
#define    byte    EcBRAMReadByte(byte Offset);
#define    void    IOWriteByte(byte Offset, byte Value);
#define    byte    IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte    DIO0ToDIO7Reg    // This parameter is represented from Note6
#define byte    DIO0Bit    // This parameter is represented from Note7
#define byte    DIO1Bit    // This parameter is represented from Note8
#define byte    DIO2Bit    // This parameter is represented from Note9
#define byte    DIO3Bit    // This parameter is represented from Note10
#define byte    DIO4Bit    // This parameter is represented from Note11
#define byte    DIO5Bit    // This parameter is represented from Note12
#define byte    DIO6Bit    // This parameter is represented from Note13
#define byte    DIO7Bit    // This parameter is represented from Note14
#define byte    DIO0Val    // This parameter is represented from Note15
#define byte    DIO1Val    // This parameter is represented from Note16
#define byte    DIO2Val    // This parameter is represented from Note17
#define byte    DIO3Val    // This parameter is represented from Note18
#define byte    DIO4Val    // This parameter is represented from Note19
#define byte    DIO5Val    // This parameter is represented from Note20
#define byte    DIO6Val    // This parameter is represented from Note21
#define byte    DIO7Val    // This parameter is represented from Note22
**********************************************************************************
```

```
*******************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //       Example, Read Digital I/O Pin 3 status
        // Output :
        //      InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //       Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*******************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID    AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
         ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*****************************************************************************
```

```
*********************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, BRAMFnDataReg);

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         IOWriteByte(EcBRAMData, Value);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
         IOWriteByte(EcBRAMData, BRAMLDNReg);
         IOWriteByte(EcBRAMIndex, 0x11);
         IOWriteByte(EcBRAMData, FnDataReg);

         IOWriteByte(EcBRAMIndex, 0x12);
         IOWriteByte(EcBRAMData, 0x10);          //Read start

         IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
         Return      IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```