COM-QM87 Rev.B

Intel® 4th Generation
Core™i7/i5/i3 Processor
Intel® QM87
Gigabit Ethernet
4 SATA
8 USB2.0, up to 4 USB3.0
1 PCI-E[x16], 7 PCI-E[x1]
COM Express Basic Module

COM-QM87 Manual Rev.B 1st Ed.
April 18, 2014

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Packing List

Before you begin installing your card, please make sure that the following materials have been shipped:

- 4 M2.5 Screw
- 1 DVD-ROM for manual (in PDF format) and drivers
- 1 COM-QM87 Rev.B

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

Contents

Chapter

1

General Information

1.1 Introduction

AAEON, a leading embedded board manufacturer, is pleased to announce the debut of their new generation COM Express Module--COM-QM87 Rev..B. The COM-QM87 Rev.B is a cutting-edge product that provides high performance and low power consumption in the embedded market.

COM-QM87 Rev.B adopts the latest Intel® 4th generation Core™ i7/i5/i3 processor. The system memory deploys with two SODIMM 204-pin DDR3/DDR3L 1333/1600 memory up to 16 GB. In addition, Intel® I217LM supports Gigabit Ethernet that allows faster network connections. This model applies seven PCI-Express[x1], one PCI-Express[x16], one LPC bus, one SMBus, one I2C, and two UART. Moreover, four SATA are configured on the COM-QM87 Rev.B. COM-QM87 Rev.B also equips eight USB2.0 (included four USB3.0) for flexible I/O expansions.

The display of COM-QM87 Rev.B supports up to three independent displays simultaneously. This brand new COM Express Module is developed to cater to the requirements of Automation, Medical, ticket machine, transportation, gaming, KIOSK, and POS/POI applications.

1.2 Features

- Onboard 4th Generation Intel® Core™ i7/ i5/ i3 Processor
- Intel® QM87 PCH
- Dual-channel SODIMM DDR3/DDR3L 1333/1600 Memory, Max. 16 GB
- Gigabit Ethernet (iAMT 9.0 Support)
- VGA x 1, eDP x 1
- High Definition Audio Interface
- SATA x 4
- USB2.0 x 8 (Included USB3.0 x 4)
- PCI-Express [x16] x 1 (Gen. 3.0), PCI-Express [x1] x 7 (Gen. 2.0)

Note: Configurable to PCI-Express[x8] Port x 2; Configurable to PCI-Express[x8] Port x 1 and PCI-Express[x4] Port x 2

- DC Input Range, +12V
- COM Express Basic Module, Pin-out Type 6, COM.0 Rev. 2.1

1.3 Specifications

System

Form Factor	COM Express Basic module, Pin-out Type 6, COM. 0 Rev. 2.1
Processor	Onboard 4th Generation Intel® Core™ i7/i5/i3 Processor
System Memory	204-pin DDR3/DDR3L SODIMM x 2, Max. 16GB (DDR3/DDR3L 1333/1600),support dual-channel
	function
Chipset	Intel® QM87 PCH
I/O Chipset	Intel® QM87 (Winbond SIO on the carrier board)
Ethernet	Intel® I217LM, 10/100/1000Base-TX PHY
BIOS	AMI BIOS
	SPI type, 16MB ROM
EEPROM	Atmel® AT24C02, save BIOS and configuration data
Wake On LAN	Yes
Watchdog Timer	ITE8518, 255 levels
H/W Status Monitoring	Supports CPU Temperature Monitoring
Expansion Interface	PCI-Express [x16] x 1
	PCI-Express [x1] x 7
	LPC bus x 1
	SMBus x 1
	UART x 2 (TX/RX only)
Power Requirement	+12V only
	2-pin wafer for RTC battery
Board Size	4.92" (L) x 3.75"(W) (125mm x 95mm)

- **Gross Weight** 0.66lb (0.3kg)
- **Operating Temperature** 32°F ~ 140°F (0°C ~ 60°C)
- **Storage Temperature** -40°F ~ 176°F (-40°C ~ 80°C)
- **Operating Humidity** 0% ~ 90% relative humidity, non-condensing
- **OS Support** Windows® 7, Windows® 8, Linux Fedora

Display

- **Chipset** 4th Generation Intel® Core™ i7/i5/i3 Processor Integrated
- **Memory** Shared system memory up to 512MB/ DVMT 5.0
- **Resolution** Up to 2560 x 2048 for CRT
  Up to 1920 x 1200 for LCD
- **LCD Interface** VGA x 1, eDP x 1

I/O

- **Storage** SATA x 4
- **Serial Port** From LPC to EC, then to the carrier board (EC x 2, CB x 2)
- **USB** USB2.0 x 8 (included USB 3.0 x 4)
- **Audio** High definition audio
- **GPIO** Up to 4 in and 4 out

Chapter

2

Quick Installation Guide

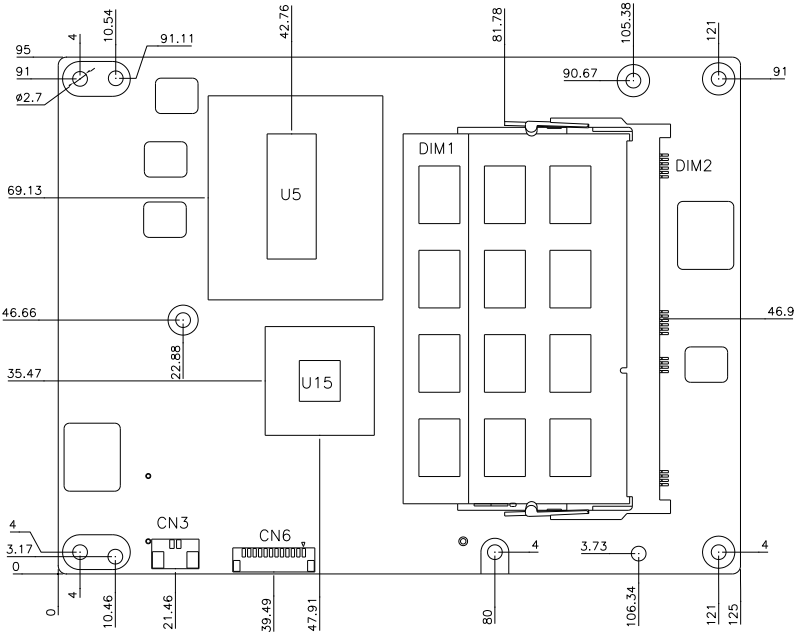
2.1 Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

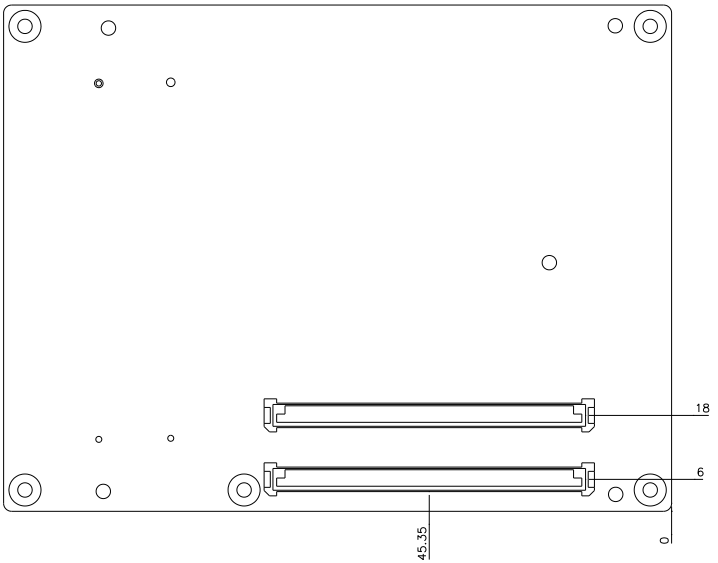
Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Mechanical Drawings of Connectors and Switches

Component Side



Solder Side



2.3 List of Switch

There is a switch on the board that allows you to configure your system to suit your application. The table below shows the function of the switch.

Label	Function
SW1	AT/ATX Setting Switch

2.4 AT/ATX Setting Switch (SW1)

	ON	OFF
1	AT Selection	ATX Selection
2	ME_EN	ME_DIS

Below Table for China RoHS Requirements
产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 **SJT 11363-2006** 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 **SJT 11363-2006** 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

Chapter

3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during these tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal or non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The COM-QM87 Rev.B CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del> or <F2> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

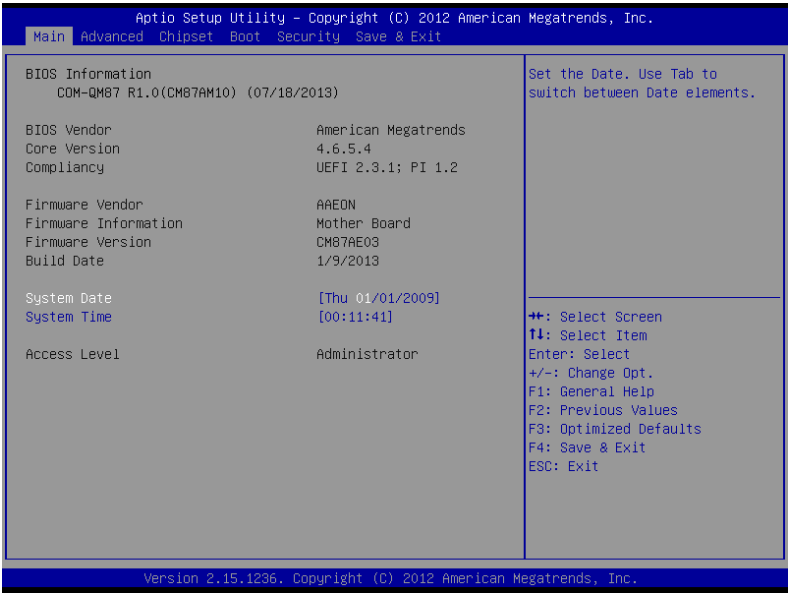
Set setup administrator password.

Save&Exit

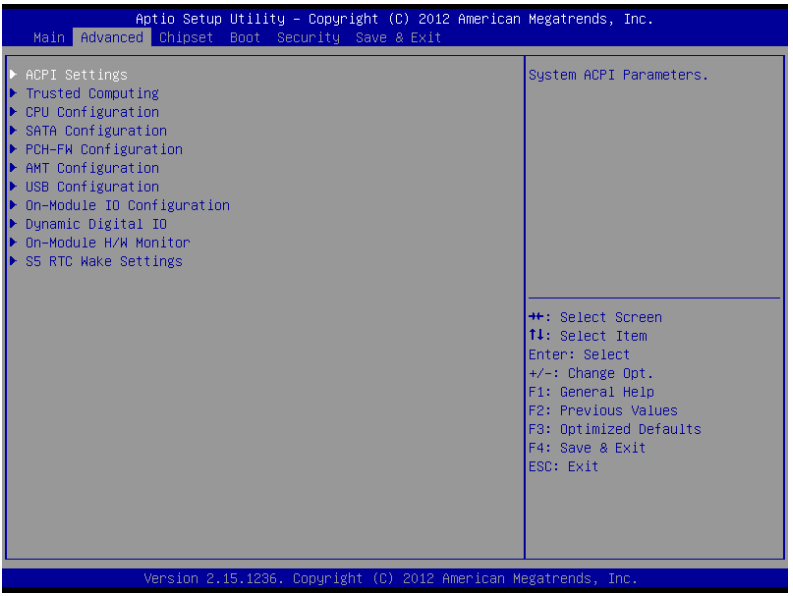
Exit system setup after saving the changes.

Setup Menu

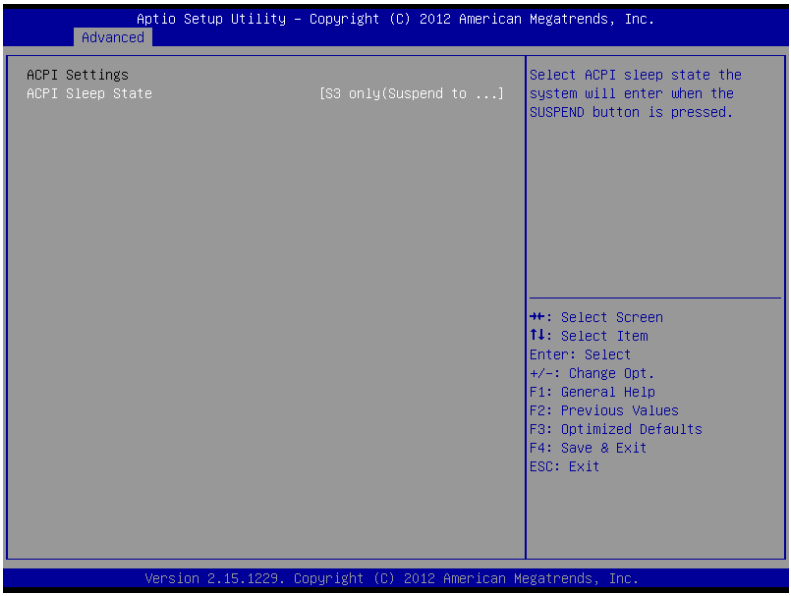
Main



Advanced


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
ACPI Settings
Trusted Computing
CPU Configuration
SATA Configuration
PCH-FW Configuration
AMT Configuration
USB Configuration
On-Module IO Configuration
Dynamic Digital IO
On-Module H/W Monitor
S5 RTC Wake Settings
System ACPI Parameters.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.

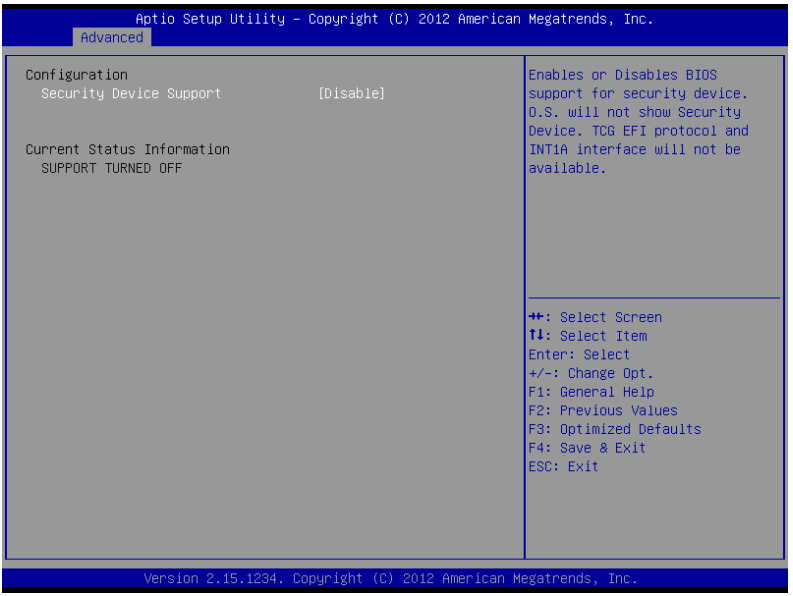
ACPI Settings



Options Summary:

Suspend mode	Supend Disabled	
	S3 (Suspend to RAM)	Default
Select the ACPI state used for System Suspend		

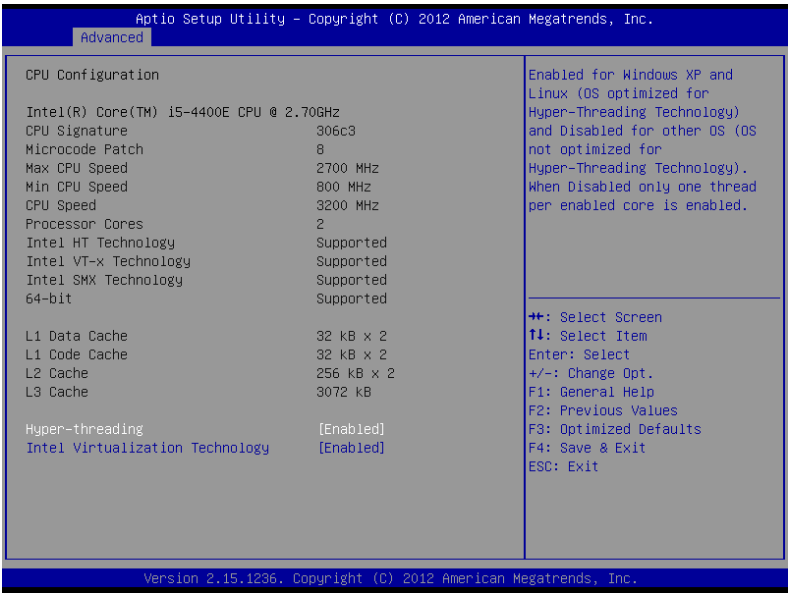
Trusted Computing



Options Summary:

Security Device Support	Disabled	Default
	Enabled	
Enable or Disable BIOS support for security device.		

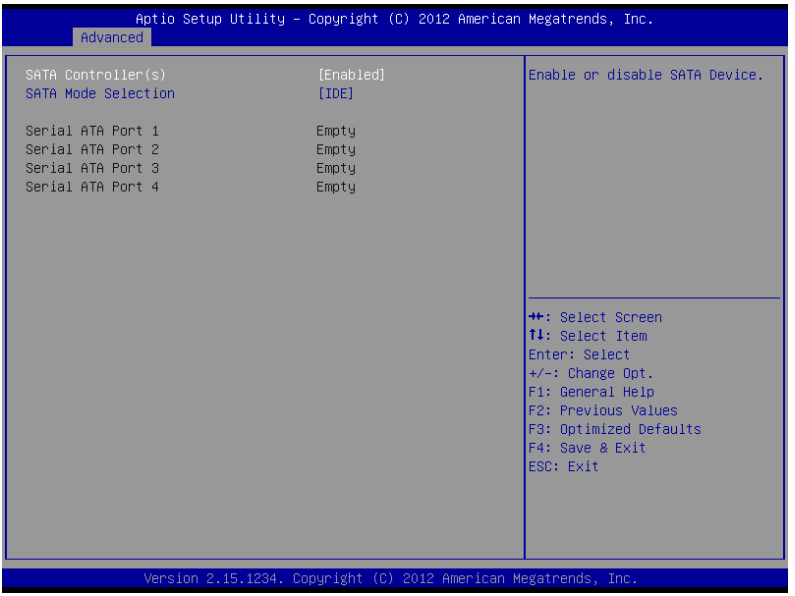
CPU Configuration



Options Summary:

Hyper-Threading	Disabled	
	Enabled	Default
En/Disable Intel Hyper-Threading Technology.		
Intel Virtualization Technology	Disabled	
	Enabled	Default
En/Disable Intel Virtualization Technology.		

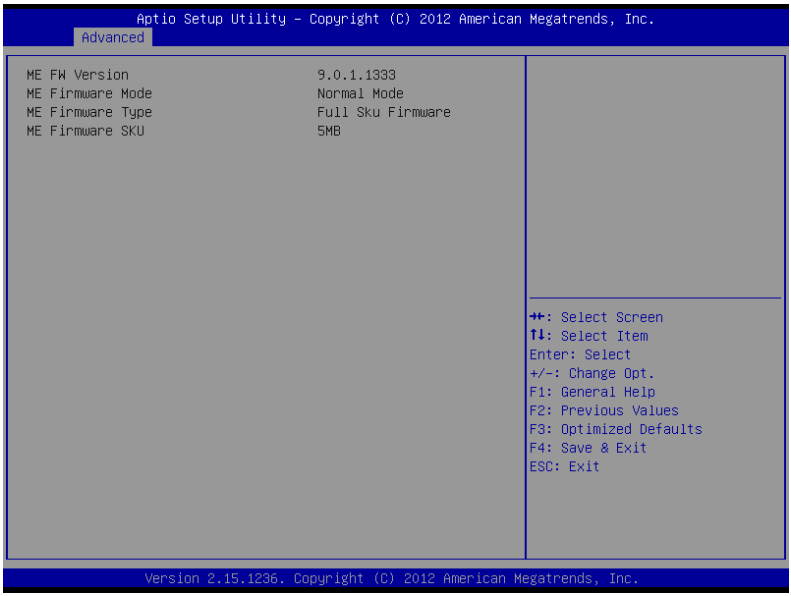
SATA Configuration



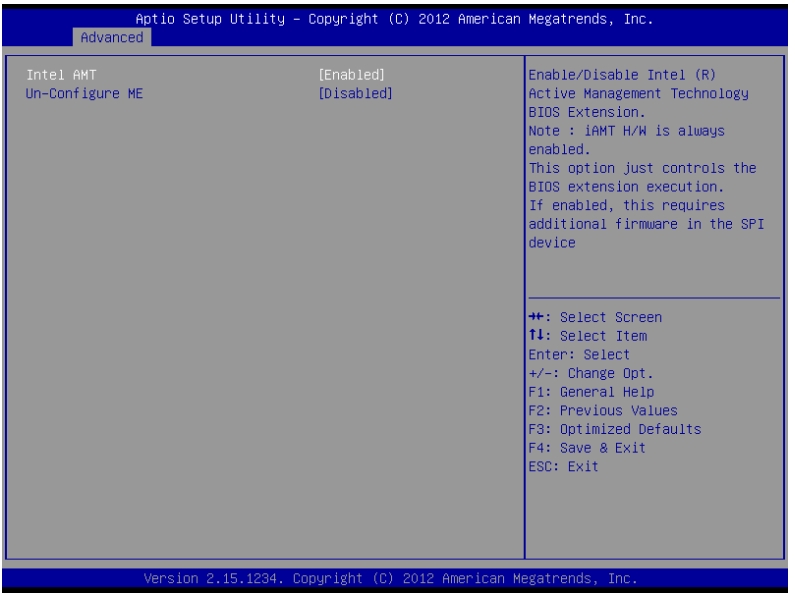
Options Summary:

SATA Controller(s)	Disabled	
	Enabled	Default
En/Disable SATA Controller(s)		
SATA Mode Selection	IDE	Default
	AHCI	
	RAID	
Determines how SATA controller(s) operate		

PCH-FW Configuration



AMT Configuration

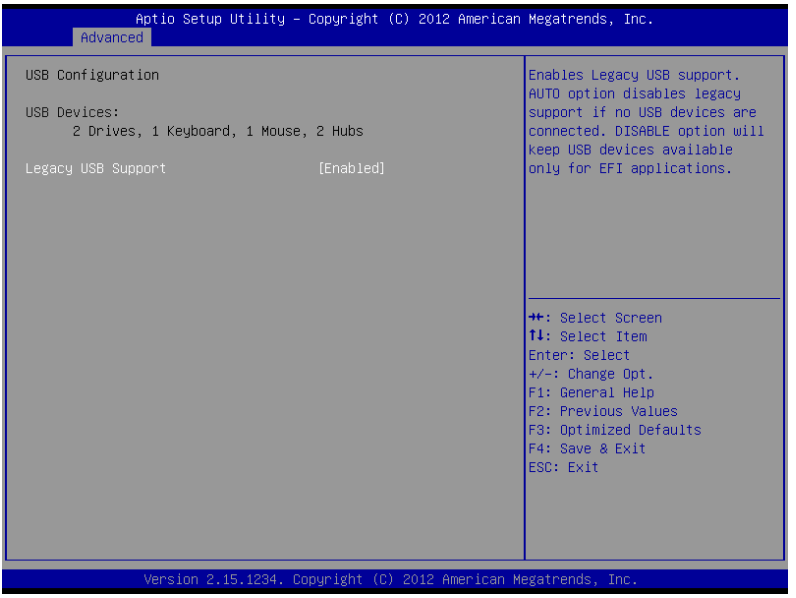


Options Summary:

Intel AMT	Disabled	
	Enabled	Default
Enable/Disable Intel(R) Active Management Technology BIOS Extension.		
Un-Configure ME	Disabled	Default
	Enabled	
OEMFlag Bit 15 : Un-Configure ME without password.		

USB

Configuration



Options Summary:

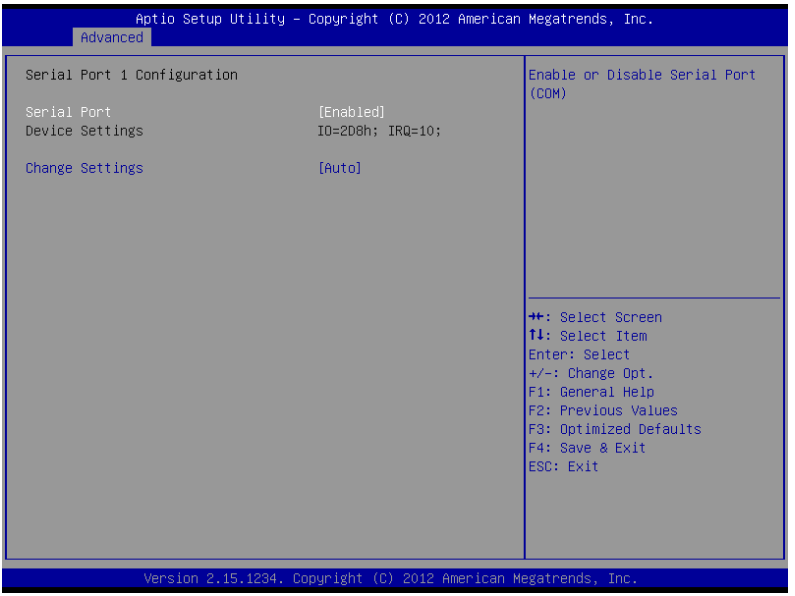
Legacy USB Support	Enabled	Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		

On-Module IO Configuration

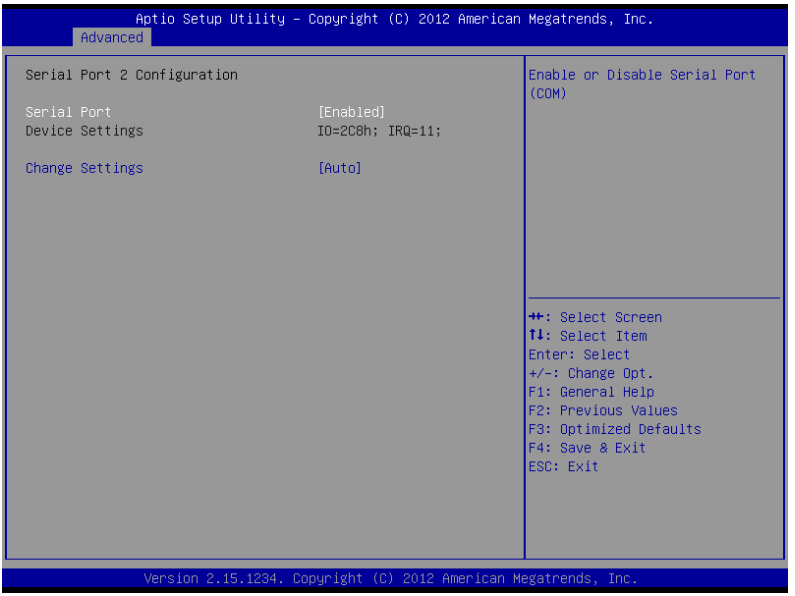
Options Summary:

Restore AC Power Loss	Power Off	Default
	Power On	
	Last State	
Select AC power state when power is re-applied after a power failure.		

Serial Port 1 Configuration



Serial Port 2 Configuration

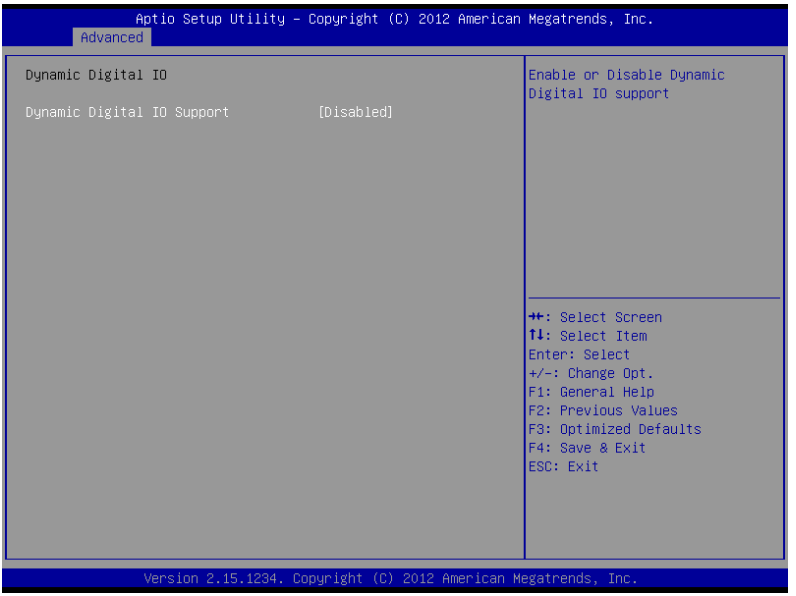


Options Summary:

Serial Port	Disabled	
	Enabled	Default
Allows BIOS to En/Disable corresponding serial port.		
Change Settings (Serial Port 1)	Auto	Default
	IO=3F8h; IRQ=3;	
	IO=3F8h; IRQ=3,4,5,7,10,11;	
	IO=2F8h; IRQ=3,4,5,7,10,11;	
	IO=3E8h; IRQ=3,4,5,7,10,11;	
	IO=2E8h; IRQ=3,4,5,7,10,11;	

Allows BIOS to Select Serial Port resource.		
Change Settings (Serial Port 2)	Auto	Default
	IO=2F8h; IRQ=4;	
	IO=3F8h; IRQ=3,4,5,7,10,11;	
	IO=2F8h; IRQ=3,4,5,7,10,11;	
	IO=3E8h; IRQ=3,4,5,7,10,11;	
	IO=2E8h; IRQ=3,4,5,7,10,11;	
Allows BIOS to Select Serial Port resource.		

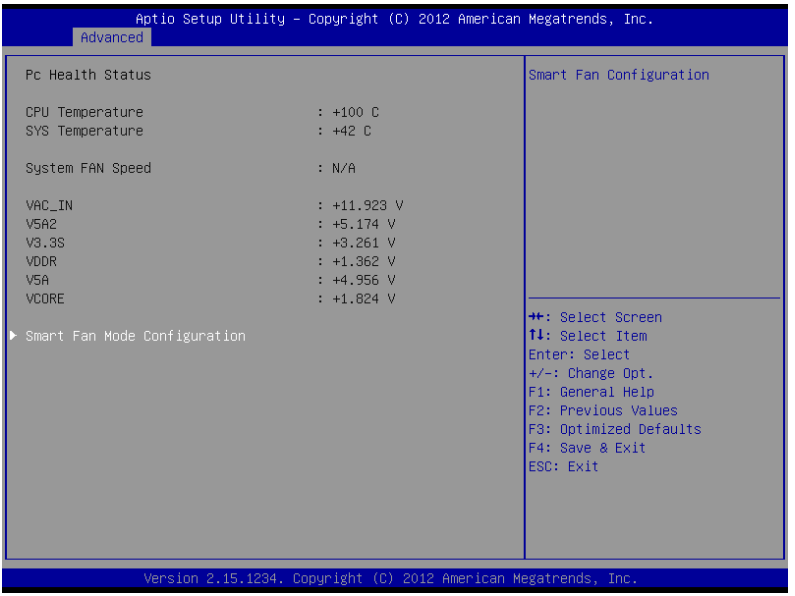
Dynamic Digital IO



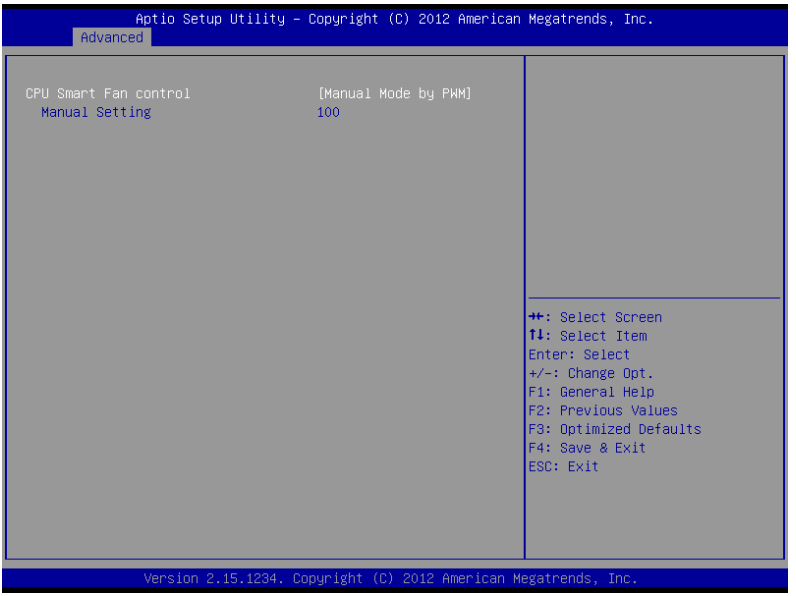
Options Summary:

Dynamic Digital IO Support	Disabled	Default
	Enabled	
Enable or Disable Dynamic Digital IO Support.		

On-Module HW Monitor



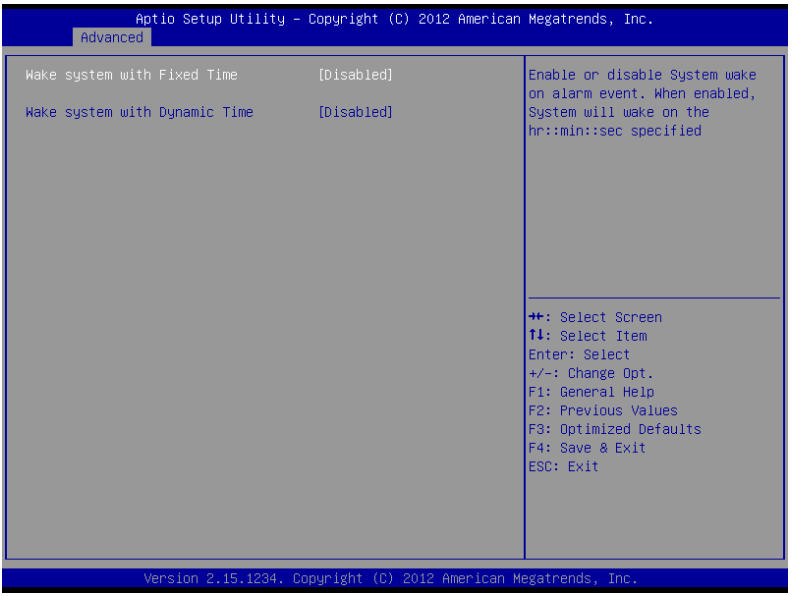
Smart Fan Mode Configuration



Options Summary:

CPU Smart Fan Control	Full Mode	Default
	Manual Mode by PWM	
	Auto Mode by PWM	
Select Fan1 Control Mode.		

S5 RTC Wake Settings



Options Summary:

Wake system with Fixed Time	Disabled	Default
	Enabled	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified.		
Wake up day	0 (Default)	
Select 0 for daily system wake up 1-31 for which day of the month that you would like the system to wake up		
Wake up hour	0 (Default)	
select 0-23 For example enter 3 for 3am and 15 for 3pm		

Wake up minute	0 (Default)	
select 0-59 for minute of an hour.		
Wake up second	0 (Default)	
select 0-59 for second of a minute.		
Wake system with Dynamic Time	Disabled	Default
	Enabled	
Enable or disable System wake on alarm event. When enabled, System will wake on the current time + Increase minute(s)		
Wake up minute increase	0 (Default)	
select 1 - 5 for minute(s).		

Chipset

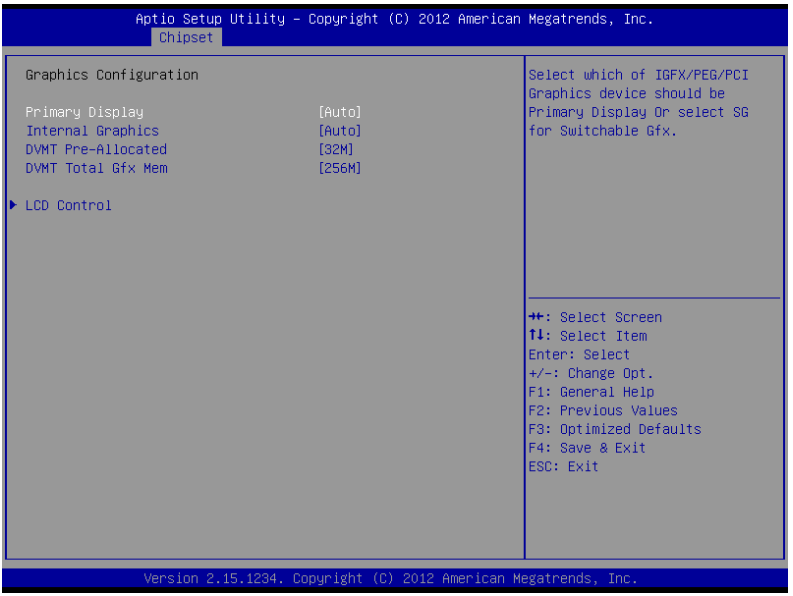

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
System Agent (SA) Configuration
PCH-IO Configuration
System Agent (SA) Parameters
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1234. Copyright (C) 2012 American Megatrends, Inc.

System Agent (SA) Configuration

Options Summary:

VT-d	Disabled	
	Enabled	Default
Check to enable VT-d function on MCH		

Graphics Configuration

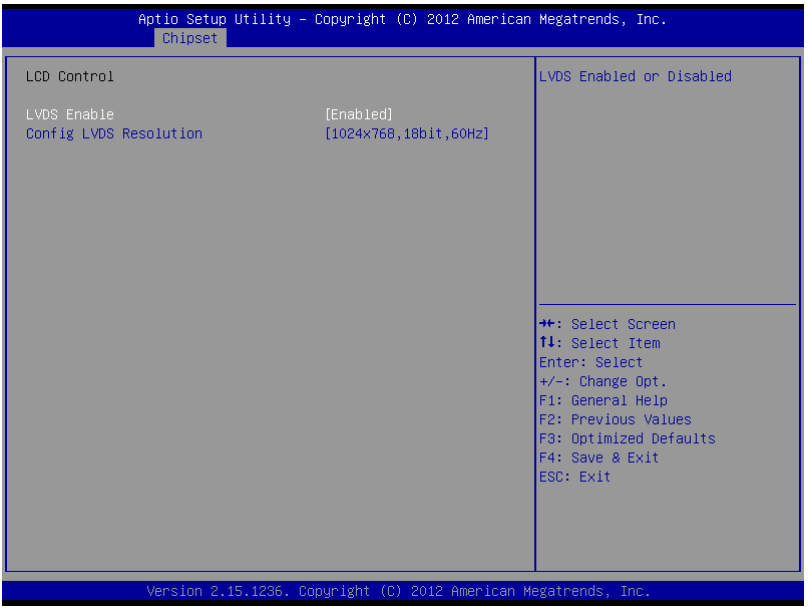


Options Summary:

Primary Display	Auto	Default
	IGFX	
	PEG	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.		
Internal Graphics	Auto	
	Disabled	
	Enabled	Default
Keep IGD enabled based on the setup options.		

DVMT Pre-Allocated	32M	Default
	64M	
	96M	
	128M	
	160M	
	192M	
	224M	
	256M	
	288M	
	320M	
	352M	
	384M	
	416M	
	448M	
	480M	
	512M	
	1024M	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Memory	128M	Default
	256M	
	Max	
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.		

LCD Control

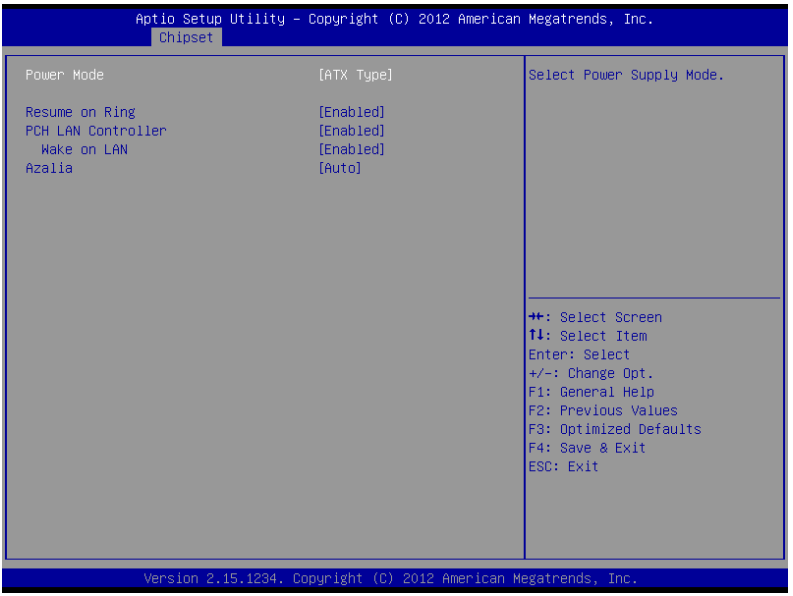


Options Summary:

LVDS Enable	Disabled	
	Enabled	Default
Enable / Disable LVDS function on LCD control.		
Config LVDS Resolution	800x600, 18bit , 60Hz	
	1024x768, 18bit, 60Hz	Default
	1024x768, 24bit, 60Hz	
	1280x768, 24bit, 60Hz	
	1366x768, 24bit, 60Hz	
	1600x1200, 48bit, 60Hz	

	1920x1080, 48bit, 60Hz	
LVDS Panel Config Select.		

PCH-IO Configuration

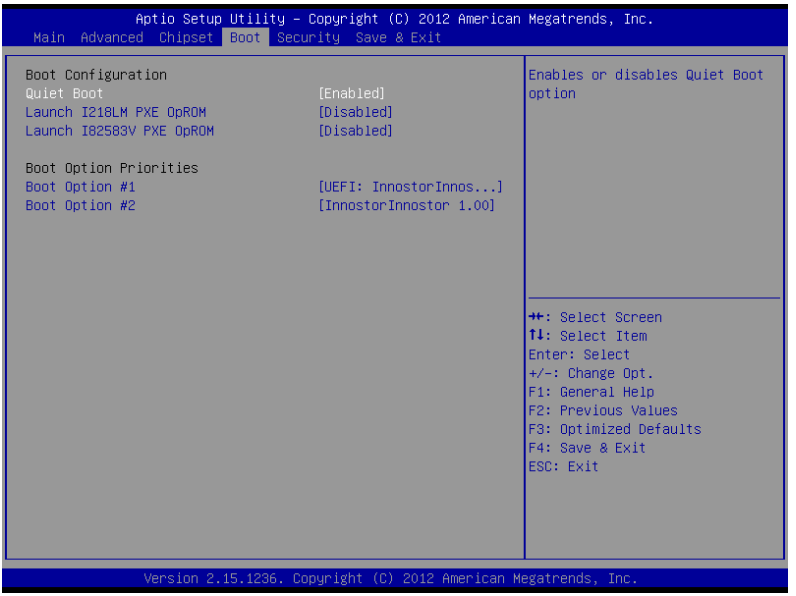


Options Summary:

Power Mode	ATX Type	Default
	AT Type	
Select Power supply mode: ATX: Normal ACPI support AT: Suspend/Sleep disabled, and Always On when restoring from power failure.		
Resume On Ring	Enabled	Default
	Disabled	
Enable or disable wake on ring.		
PCH LAN Controller	Enabled	Default

	Disabled	
Enable or disable onboard NIC.		
Wake on Lan	Enabled	Default
	Disabled	
Enable or disable integrated LAN to wake the system.		
Azalia	Disabled	
	Enabled	
	Auto	Default
Control Detection of the Azalia device.		

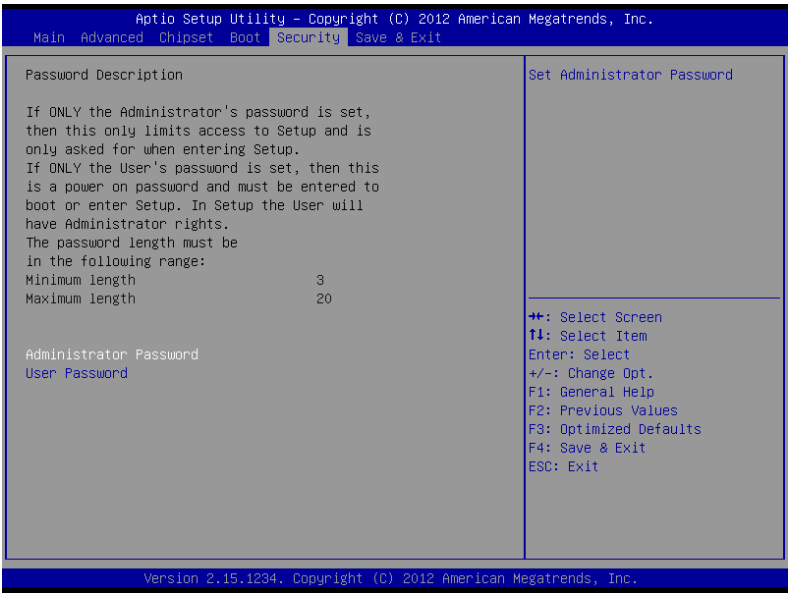
Boot



Options Summary:

Quiet Boot	Disabled	
	Enabled	Default
En/Disable showing boot logo.		
Launch I218LM PXE OpROM	Disabled	Default
	Enabled	
En/Disable I218LM PXE OpROM		
Launch I82583V PXE OpROM	Disabled	Default
	Enabled	
En/Disable I82583V PXE OpROM		

Security



Options summary:

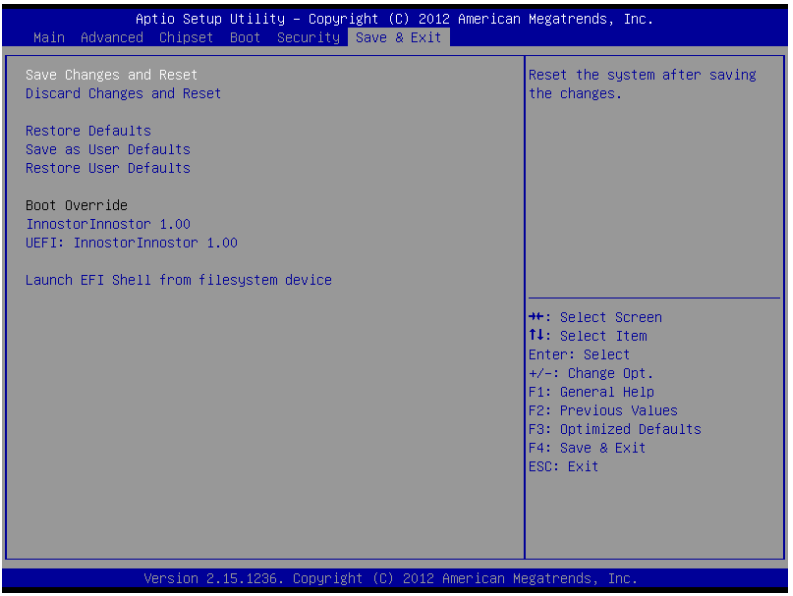
Set User Password/ Set Administrator Password	Not set	
You can install a Master and User password. Before booting to OS, HDD will be set to frozen state. On S3 resume HDD will be unlocked using the HDD Password we entered while system booting. *Install the Password:* Press Enter on this item, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for		

confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password:

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

Exit



Options Summary:

Save Changes and Reset		
Reset the system after saving the changes		
Discard Changes and Reset		
Reset system setup without saving any changes		
Restore Defaults		
Restore/Load Default values for all the setup options.		
Save as User Defaults		
Save the changes done so far as User Defaults		
Restore User Defaults		
Restore the User Defaults to all the setup options		

Chapter

4

Driver Installation

.

The COM-QM87 Rev.B comes with an AutoRun DVD-ROM that contains all drivers and utilities that can help you to install the driver automatically.

Insert the driver DVD, the driver DVD-title will auto start and show the installation guide. If not, please follow the sequence below to install the drivers.

Follow the sequence below to install the drivers:

Step 1 – Install Chipset Driver

Step 2 – Install VGA Driver

Step 3 – Install USB3.0 Driver

Step 4 – Install Audio Driver

Step 5 – Install LAN Driver

Step 6 – Install RAID & AHCI Driver

Step 7 – Install ME Driver

Step 8 – Install TPM Driver (Optional)

Step 9 – Install UART_ITE Driver

Please read instructions below for further detailed installations.

4.1 Installation:

Insert the COM-QM87 Rev.B DVD-ROM into the DVD-ROM drive.

And install the drivers from Step 1 to Step 9 in order.

Step 1 – Install Chipset Driver

1. Click on the ***Step1 - INF*** folder and double click on the ***infinst_autol.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 2 – Install VGA Driver

1. Click on the ***Step2 - VGA*** folder and select the ***Step2.2 - Intel driver*** folder
2. Select the OS folder your system is and double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 3 –Install USB3.0 Driver

1. Click on the ***Step3 - USB3.0*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 4 –Install Audio Driver

1. Click on the ***Step4 - Audio*** folder and select the ***Win7_8***

folder

2. Double click on the ***Setup.exe*** file
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 5 –Install LAN Driver

1. Click on the ***Step5 - LAN*** folder and select the OS folder your system is
2. Double click on the ***.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 6 – Install RAID & AHCI Driver

For AHCI Driver

1. Click on the ***Step6 - RAID&AHCI*** folder and double click on the ***SetupRST.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

For RAID Driver

Please refer to Appendix D RAID Setting

Step 7 – Install ME Driver

1. Click on the ***Step7 - ME*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 8 – Install TPM Driver (Optional)

1. Click on the ***Step8 - TPM (Optional)*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 9 – Install UART_ITE Driver

1. Click on the ***Step9 - UART_ITE*** folder
2. Follow the step instructions (***patch install step1.jpg*** to ***patch install step5.jpg)*** that the window shows
3. The system will help you install the driver successfully

Appendix

A

Programming the Watchdog Timer

A.1 Watchdog Timer Initial Program

Table 1 : Embedded BRAM relative register table		
	Default Value	**Note**
Index	**0x284**(Note1)	BRAM Index Register
Data	**0x285**(Note2)	BRAM Data Register
Logical Device Number	**0xA8**(Note3)	Watch dog Logical Device Number
Function and Device Number	**0x00**(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	**BitNum**	**Value**	**Note**
Timer Counter	**0x00**(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	**0x01**(Note6)	**0**(Note7)	**0**(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	**0x01**(Note8)	**[3:2]**(Note9)	**0**(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*********************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnDataReg   //This parameter is represented from Note4
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerReg    //This parameter is represented from Note5
#define byte   TimerVal    // This parameter is represented from Note10
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note11
#define byte   RSTReg    //This parameter is represented from Note8
#define byte   RSTBit    //This parameter is represented from Note9
#define byte   RSTVal    //This parameter is represented from Note12
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(0);
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte Value){
        ECBRAMWriteByte(TimerReg , Value);
}

VOID   WDTParameterSetting(){
        Byte TempByte;

        // Watchdog Timer counter setting
        ECBRAMWriteByte(TimerReg , TimerVal);
        // WDT counting unit setting
        TempByte = ECBRAMReadByte(UnitReg);
        TempByte |= (UnitVal << UnitBit);
        ECBRAMWriteByte(UnitReg , TempByte);
        // WDT RST pulse width setting
        TempByte = ECBRAMReadByte(RSTReg);
        TempByte |= (RSTVal << RSTBit);
        ECBRAMWriteByte(RSTReg , TempByte);
}
*****************************************************************************
```

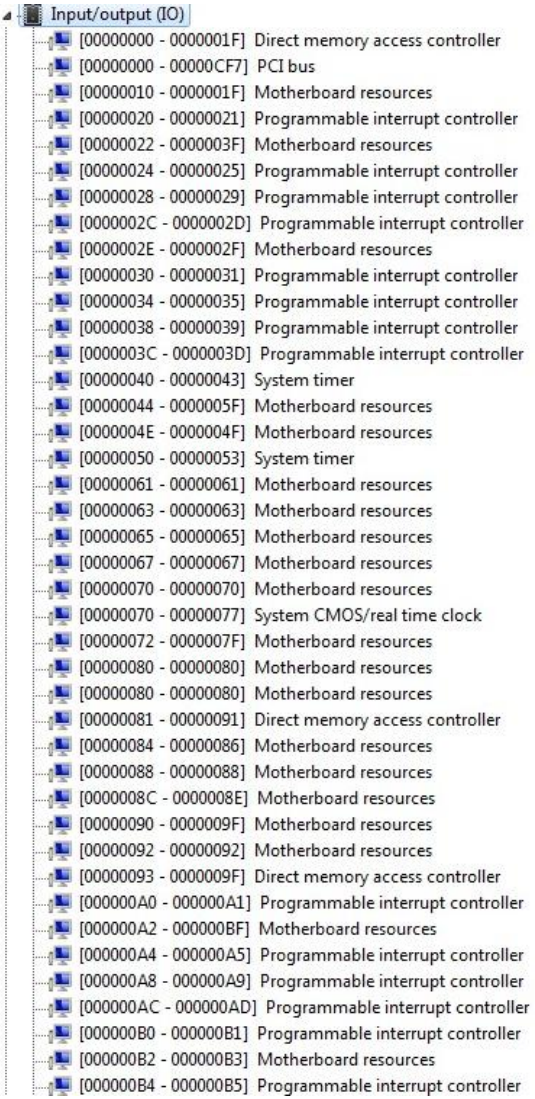
```
*****************************************************************************
VOID   ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        IOWriteByte(EcBRAMData, Value);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x30);          //Write start
}

Byte   ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x10);          //Read start

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        Return  IOReadByte(EcBRAMData, Value);
}
*****************************************************************************
```

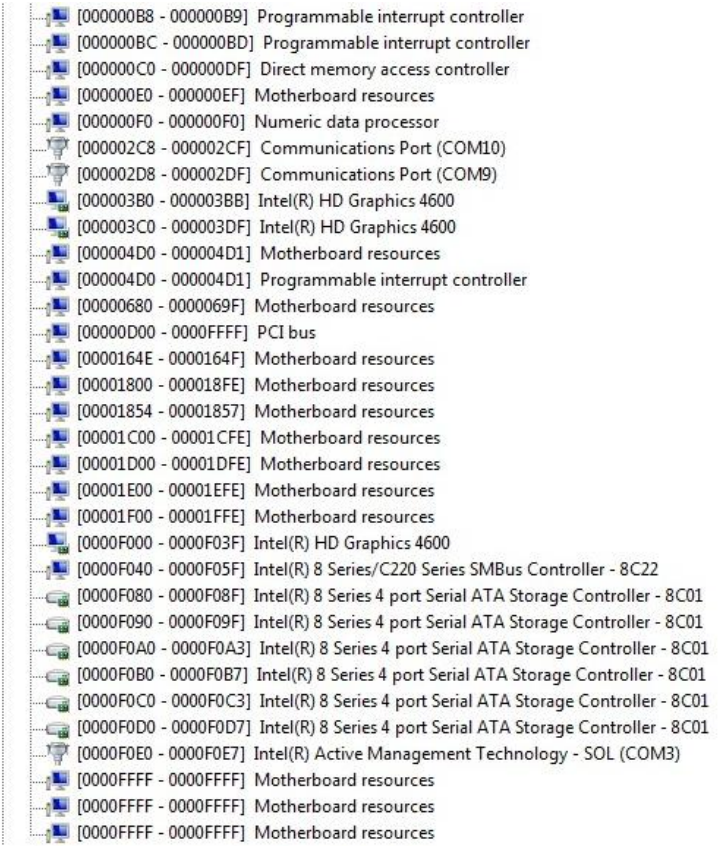
Appendix

B

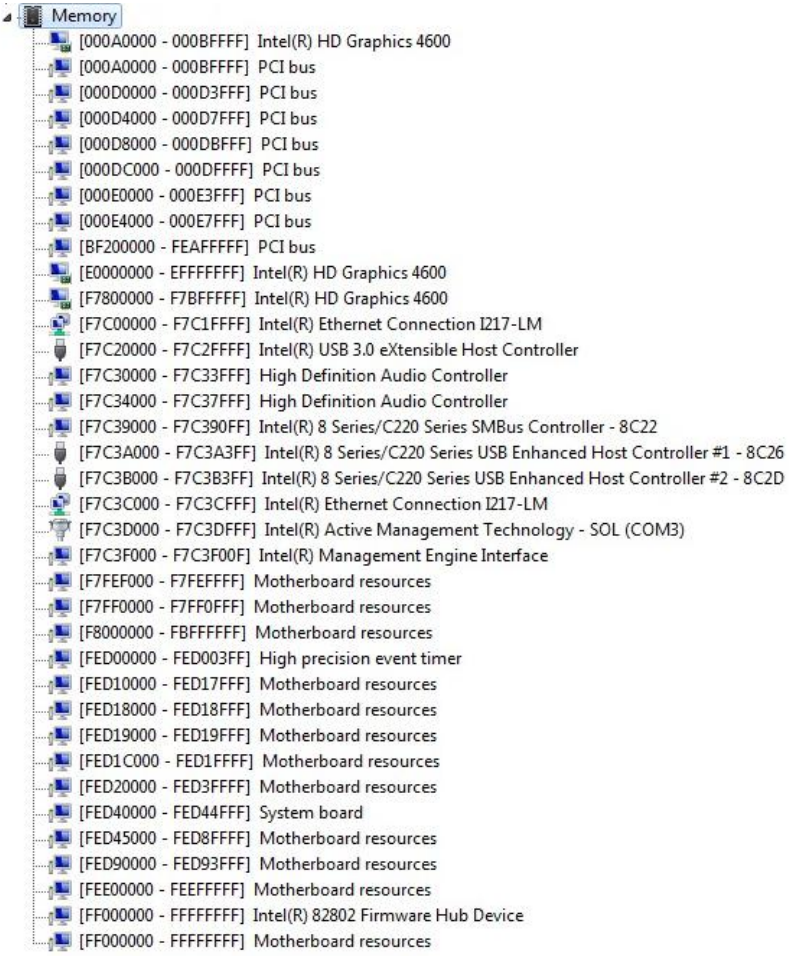
I/O Information

B.1 I/O Address Map

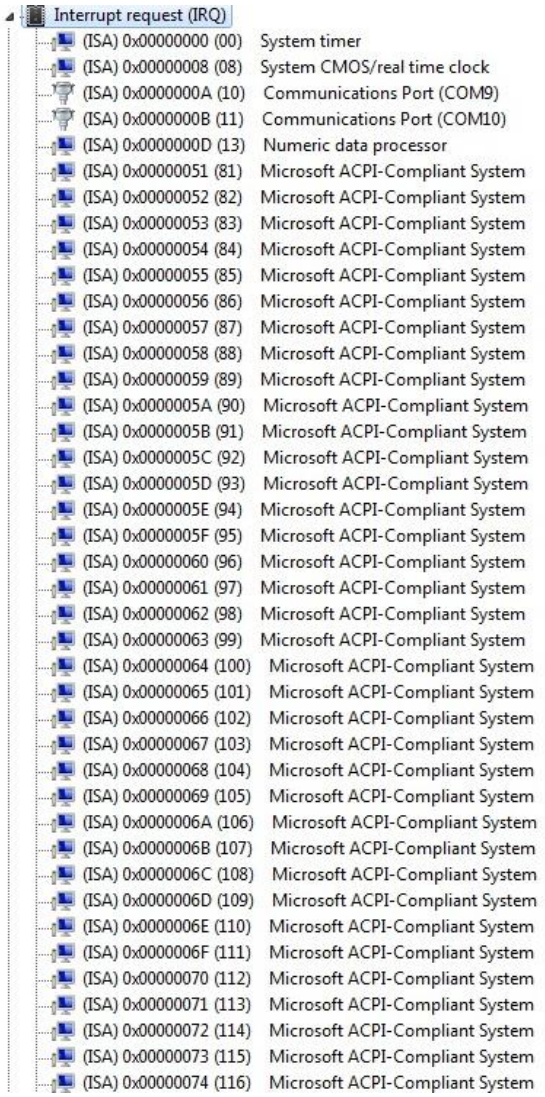



[000000B8 - 000000B9] Programmable interrupt controller
[000000BC - 000000BD] Programmable interrupt controller
[000000C0 - 000000DF] Direct memory access controller
[000000E0 - 000000EF] Motherboard resources
[000000F0 - 000000F0] Numeric data processor
[000002C8 - 000002CF] Communications Port (COM10)
[000002D8 - 000002DF] Communications Port (COM9)
[000003B0 - 000003BB] Intel(R) HD Graphics 4600
[000003C0 - 000003DF] Intel(R) HD Graphics 4600
[000004D0 - 000004D1] Motherboard resources
[000004D0 - 000004D1] Programmable interrupt controller
[00000680 - 0000069F] Motherboard resources
[00000D00 - 0000FFFF] PCI bus
[0000164E - 0000164F] Motherboard resources
[00001800 - 000018FE] Motherboard resources
[00001854 - 00001857] Motherboard resources
[00001C00 - 00001CFE] Motherboard resources
[00001D00 - 00001DFE] Motherboard resources
[00001E00 - 00001EFE] Motherboard resources
[00001F00 - 00001FFE] Motherboard resources
[0000F000 - 0000F03F] Intel(R) HD Graphics 4600
[0000F040 - 0000F05F] Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
[0000F080 - 0000F08F] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F090 - 0000F09F] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F0A0 - 0000F0A3] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F0B0 - 0000F0B7] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F0C0 - 0000F0C3] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F0D0 - 0000F0D7] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
[0000F0E0 - 0000F0E7] Intel(R) Active Management Technology - SOL (COM3)
[0000FFFF - 0000FFFF] Motherboard resources
[0000FFFF - 0000FFFF] Motherboard resources
[0000FFFF - 0000FFFF] Motherboard resources

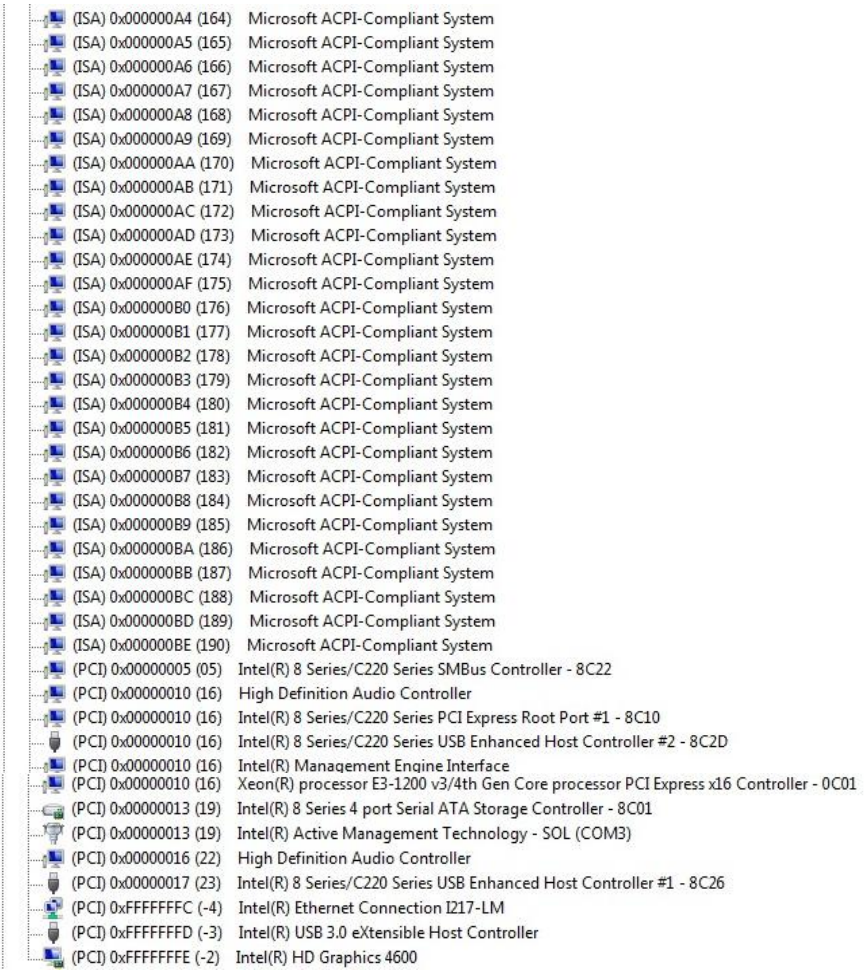
B.2 Memory Address Map



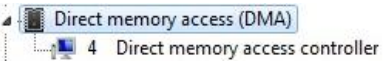
B.3 IRQ Mapping Chart



(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System



B.4 DMA Channel Assignments



Appendix

C

Programming the Digital I/O

C.1 DIO Programming

COM-QM87 Rev.B utilizes ITE8518 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can develop customized program to fit your application.

C.2 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	**Note**
Index	**0x284**(Note1)	BRAM Index Register
Data	**0x285**(Note2)	BRAM Data Register
Logical Device Number	**0xA2**(Note3)	Watch dog Logical Device Number
Input/Output Function and Device Number	**0x00**(Note4)	DIO Input/Output Function/Device Number
Output Data Function and Device Number	**0x01**(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	**BitNum**	**Value**	**Note**
GPI0 Pin Status	**0x00**(Note6)	**0**(Note7)	(Note15)	GPF0
GPI1 Pin Status	**0x00**(Note6)	**1**(Note8)	(Note16)	GPF1
GPI2 Pin Status	**0x00**(Note6)	**2**(Note9)	(Note17)	GPF2
GPI3 Pin Status	**0x00**(Note6)	**3**(Note10)	(Note18)	GPF3
GPO0 Pin Status	**0x00**(Note6)	**4**(Note11)	(Note19)	GPF4
GPO1 Pin Status	**0x00**(Note6)	**5**(Note12)	(Note20)	GPF5
GPO2 Pin Status	**0x00**(Note6)	**6**(Note13)	(Note21)	GPF6
GPO3 Pin Status	**0x00**(Note6)	**7**(Note14)	(Note22)	GPF7

C.3 Digital I/O Sample Program

```
**********************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnData0Reg   //This parameter is represented from Note4
#define byte   BRAMFnData1Reg   //This parameter is represented from Note5
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DIO0ToDIO7Reg   // This parameter is represented from Note6
#define byte   DIO0Bit   // This parameter is represented from Note7
#define byte   DIO1Bit   // This parameter is represented from Note8
#define byte   DIO2Bit   // This parameter is represented from Note9
#define byte   DIO3Bit   // This parameter is represented from Note10
#define byte   DIO4Bit   // This parameter is represented from Note11
#define byte   DIO5Bit   // This parameter is represented from Note12
#define byte   DIO6Bit   // This parameter is represented from Note13
#define byte   DIO7Bit   // This parameter is represented from Note14
#define byte   DIO0Val   // This parameter is represented from Note15
#define byte   DIO1Val   // This parameter is represented from Note16
#define byte   DIO2Val   // This parameter is represented from Note17
#define byte   DIO3Val   // This parameter is represented from Note18
#define byte   DIO4Val   // This parameter is represented from Note19
#define byte   DIO5Val   // This parameter is represented from Note20
#define byte   DIO6Val   // This parameter is represented from Note21
#define byte   DIO7Val   // This parameter is represented from Note22
**********************************************************************************
```

```
**********************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //        Example, Read Digital I/O Pin 3 status
        // Output :
        //        InputStatus :
        //                0: Digital I/O Pin level is low
        //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //        Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
**********************************************************************************
```

```
**************************************************************************************
Boolean    AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID    AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
        ECBRAMWriteByte(OptionReg, BitNum, Value);
}

**************************************************************************************
```

```
*********************************************************************************
VOID   ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, BRAMFnDataReg);

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        IOWriteByte(EcBRAMData, Value);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x30);                  //Write start
}

Byte   ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
        IOWriteByte(EcBRAMData, BRAMLDNReg);
        IOWriteByte(EcBRAMIndex, 0x11);
        IOWriteByte(EcBRAMData, FnDataReg);

        IOWriteByte(EcBRAMIndex, 0x12);
        IOWriteByte(EcBRAMData, 0x10);                  //Read start

        IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
        Return  IOReadByte(EcBRAMData, Value);
}
*********************************************************************************
```

Appendix

D

RAID Setting

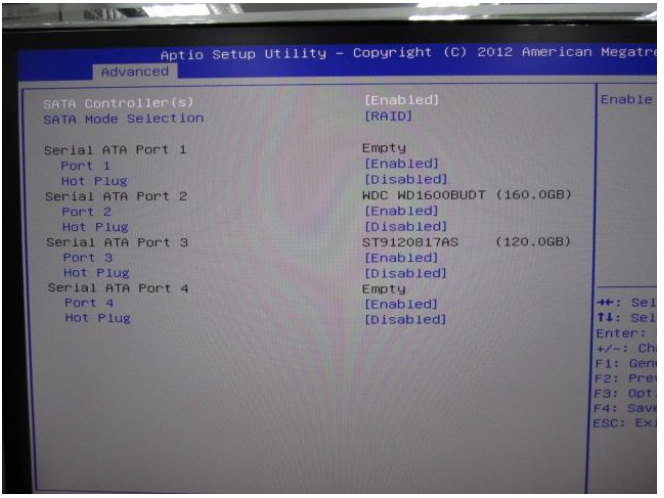
D.1 Setting RAID

OS installation to setup RAID Mode

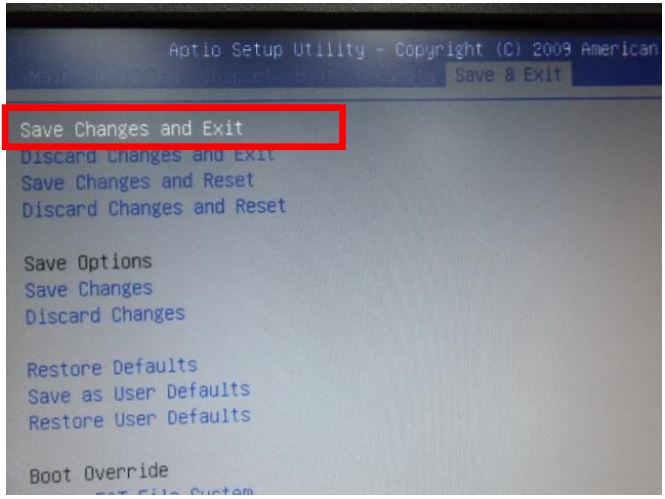
Step 1: Copy the files below from "***Driver CD -> Step6 - RAID&AHCI"*** to Disk

Step 2: Connect the USB Floppy (disk with RAID files) to the board

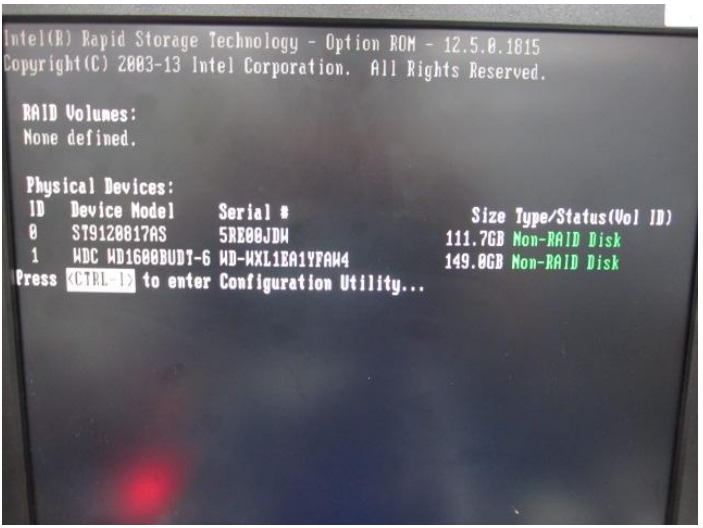
Step 3: The setting procedures " **In BIOS Setup Menu**"
A: Advanced -> SATA Configuration -> SATA Contoller(s) ->Enable -> SATA Mode Selection->Raid



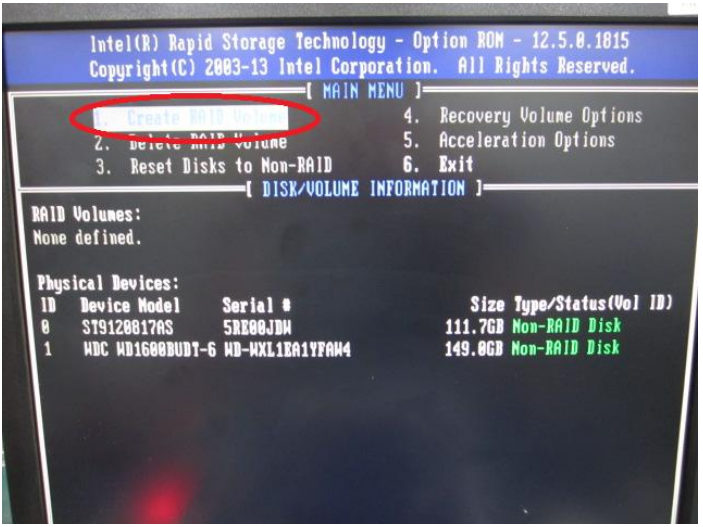
Step 4: The setting procedures "**In BIOS Setup Menu**"
B: Save & Exit -> Save Changes and Exit



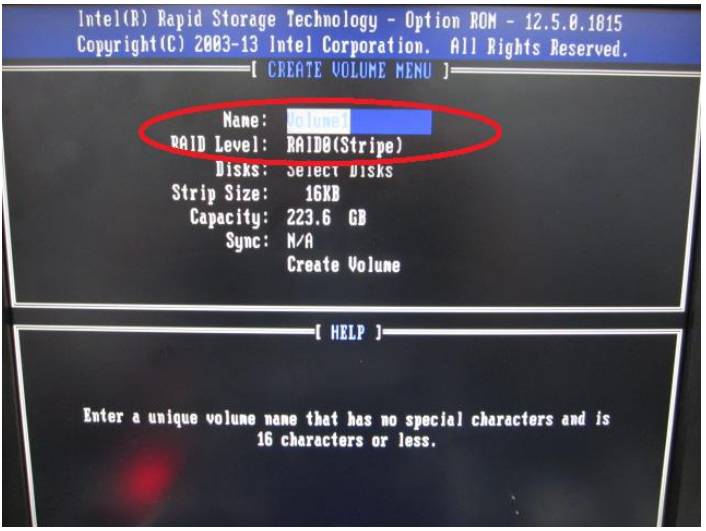
Step 5: Press **Ctrl-I** to enter **MAIN MENU**



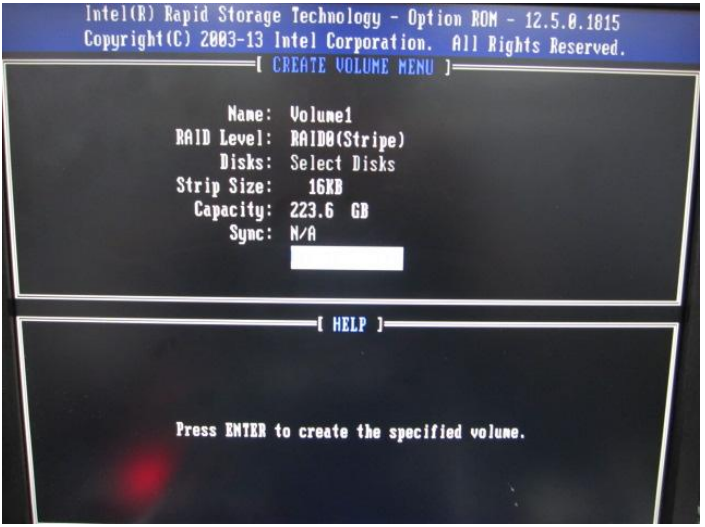
Step 6: Choose "**1.Create RAID Volume**"



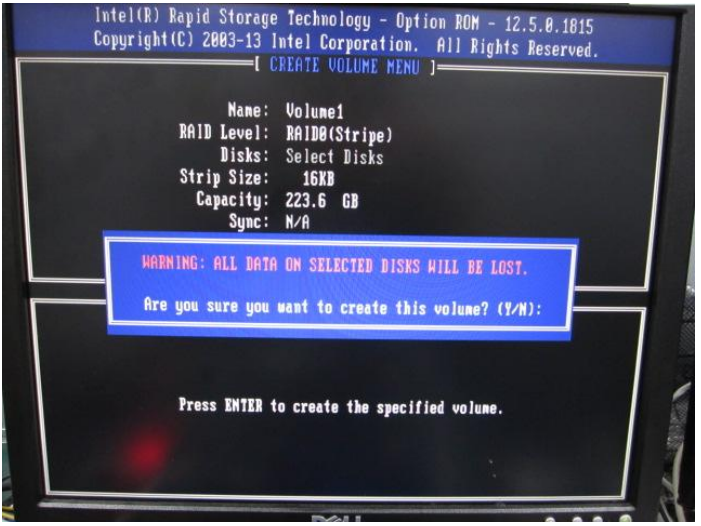
Step 7: RAID Level -> RAID0(Stripe)



Step 8: Choose "**Create Volume**"



Step 9: Choose "**Y**"



Step 10: Choose "**6. Exit**"