COM-ARHC6

COM Express Module

User's Manual 3rd Ed

Last Updated: April 10, 2026

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● COM-ARHC6	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON **主板/子板/背板** QO4-381 Rev.A2

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

环保使用期限(EFUP (Environmental Friendly Use Period)) : 10年

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Name and content of hazardous substances in product

AAEON Main Board/Daughter Board/Backplane QO4-381 Rev.A2

Part Name	Hazardous Substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCB Assemblies	×	○	○	○	○	○
Connector and Cable	×	○	○	○	○	○

The table is prepared in accordance with the provisions of SJ/T 11364.

○：Indicates that said hazardous substance contained in all of the homogenous materials for this product is below the limit requirement of GB/T 26572.

×：Indicates that said hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement of GB/T 26572. But this product still be compliance with 2011/65/EU Directive (allowed with 2011/65/EU Annex III of RoHS exemption with number 6(c),7(a),7(c)-1).

EFUP (Environment Friendly Use Period) value: 10 years

Notes: This product defined period of use is under normal condition.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	COM Express Compact Size, Type 6
CPU	Intel® Core™ Ultra Processors: Intel® Core™ Ultra 9 Processor 285H (16C/16T, up to 5.4 GHz, 45W) Intel® Core™ Ultra 7 Processor 255H (16C/16T, up to 5.1 GHz, 28W) Intel® Core™ Ultra 5 Processor 225H (14C/14T, up to 4.9 GHz, 28W)
Chipset	Integrated with Intel ® SoC
Memory	DDR5 6400MHz Dual-Channel SODIMM x 2, non-ECC, up to 128GB
Onboard Storage	NVMe, up to 256GB, via last PEG [x4] bus (Optional)
BIOS	AMI UEFI
Wake on LAN	Yes
Watchdog Timer	255 Levels
Dimension	3.75" x 3.75" (95mm x 95mm)
Security	fTPM / dTPM (default)

Power	
Power Requirement	+9V – 16V and +5VSB for ATX, +9V – 16V for AT
Power Type	AT/ATX
Power Consumption (Typical)	Intel® Core™ Ultra 9 Processor 285H, 9.13A @+12V

Display

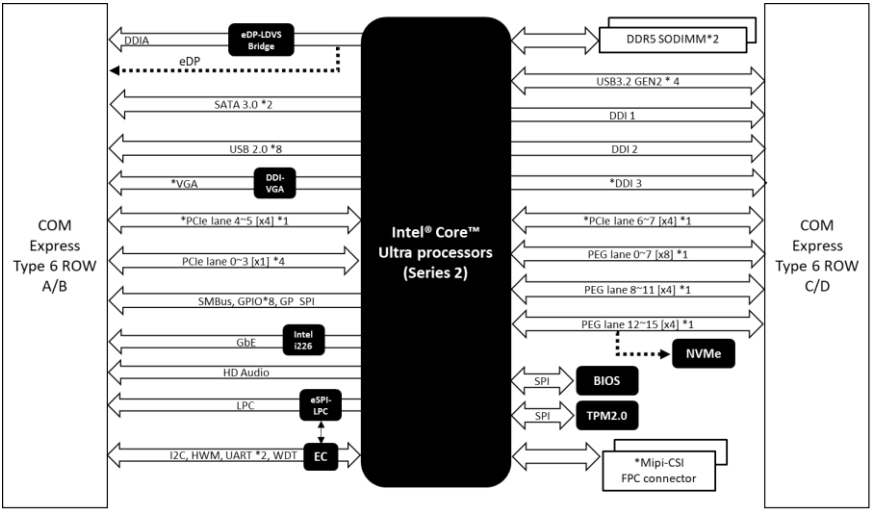
Graphics Controller	Intel® Arc™ graphics
Video Output	4 Simultaneous Displays: LVDS: up to 1920 x 1080 (default) / eDP: up to 3840 x 2160, switch by BOM DDI 1: HDMI/DP, up to 3840 x 2160 DDI 2: HDMI/DP, up to 3840 x 2160 DDI 3: DP/HDMI, up to 3840 x 2160 or VGA, up to 1920 x 1080 (DDI 3 co-lay with VGA)

I/O

Ethernet	Intel® Ethernet Controller I226, 2.5GbE x 1
Audio	High Definition Audio Interface
USB Port	USB 2.0 x 8 USB 3.2 Gen 2 x 4
Serial Port	2-Wire UART x 2 (Tx/Rx)
HDD Interface	SATA 6Gb/s x 2
Expansion	PEG 4.0 [x8] + [x4] + [x4], last PEG [x4] option to be onboard NVMe SSD PCIe 4.0 [x1] x 4 + PCIe [x4]
GPIO	8-bit
SMBus/I2C	I2C x 1, from EC (default) or CPU, switch by BIOS SMBus x 1, from CPU

Environmental	
Operating Temperature	-4°F – 158°F (-20°C – 70°C)
Storage Temperature	-40°F – 185°F (-40°C – 85°C)
Operating Humidity	0% – 90% relative humidity, non-condensing
EMC	CE/FCC Class A
OS Support	Windows® 11 (64-bit)
	Linux Ubuntu 24.04/Kernel 6.11
Weight	0.25 lb (0.12 kg)

1.2 Block Diagram



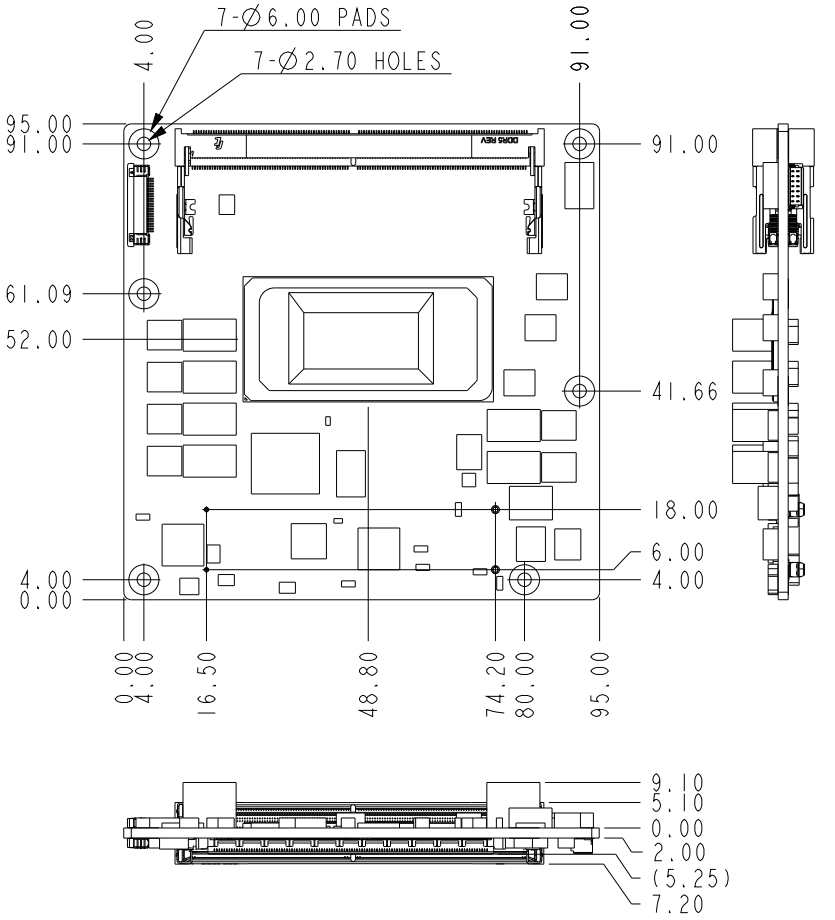
Note 1: VGA (default) co-lay with DDI3
Note 2: CSI camera support available upon request
Note 3: Per platform specification, all PEG ports do not support bifurcation
Note 4: PCIe lanes 4–7 only support [x4]

Chapter 2

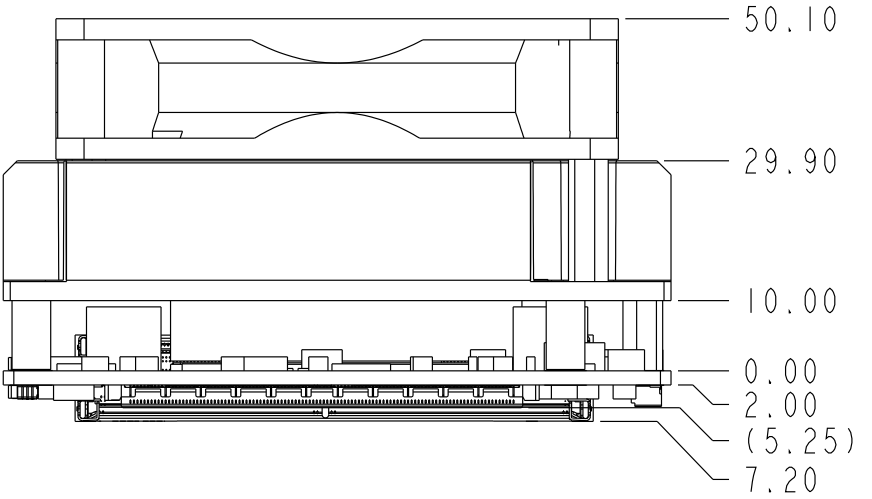
Hardware Information

2.1 Dimensions

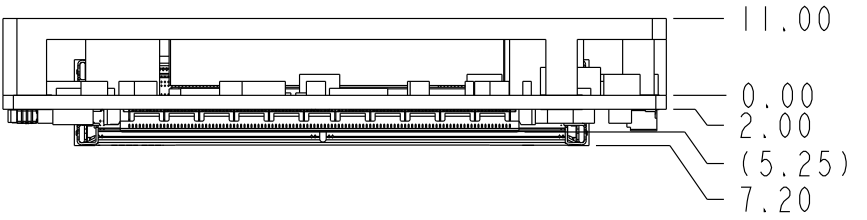
Top Side



With Active Cooling (Part No: COM-MTHC6-FAN01)

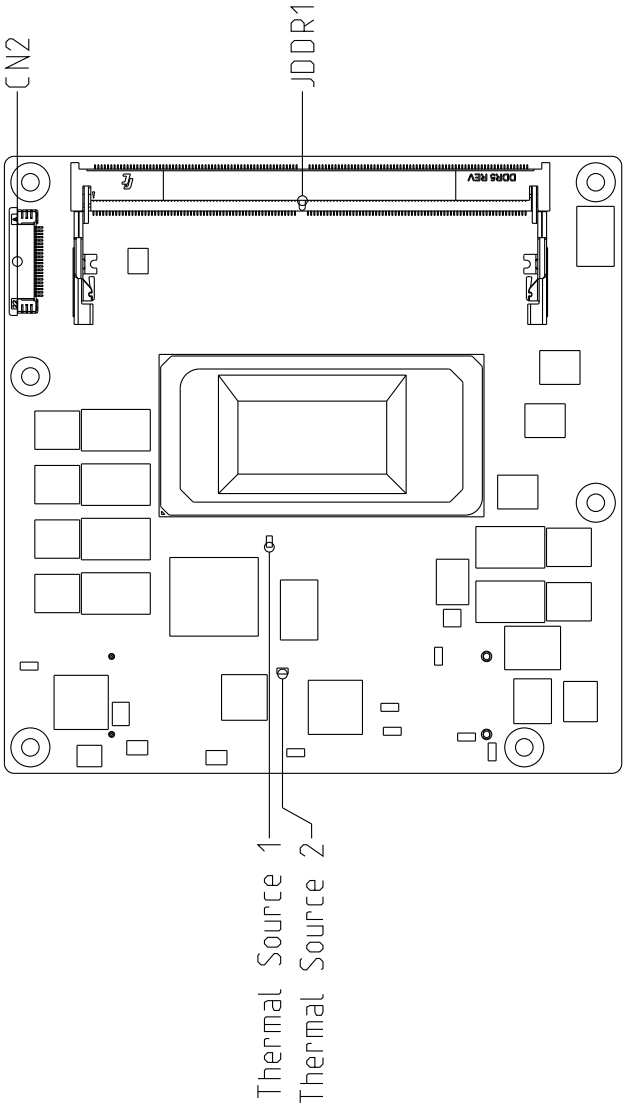


With Heatspreader (Part No: COM-MTHC6-HSP01)

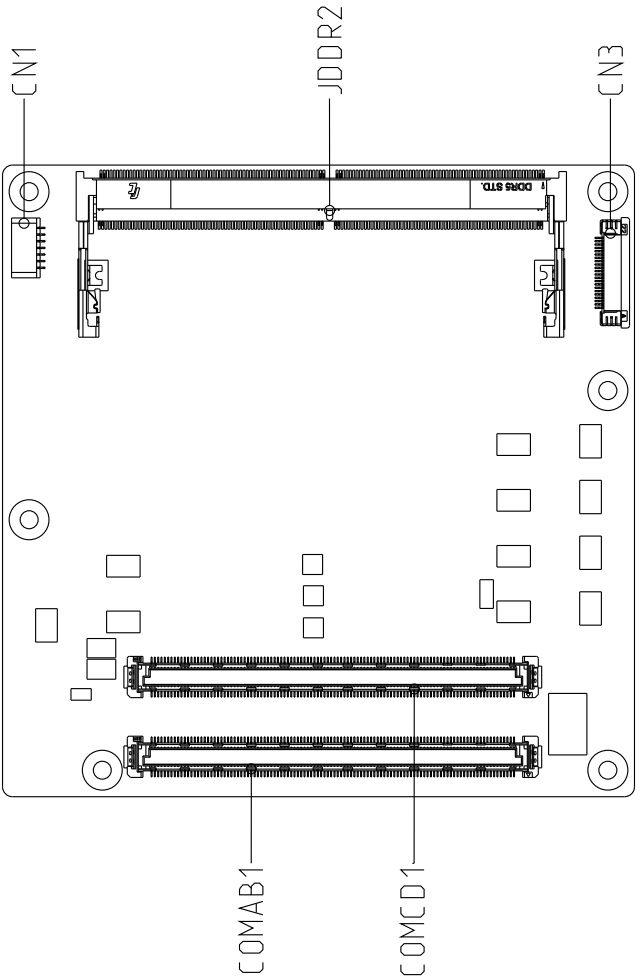


2.2 Jumpers and Connectors

Top Side



Bottom Side

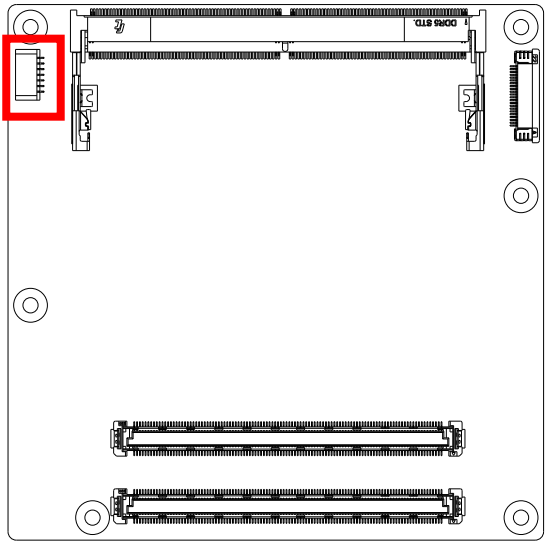


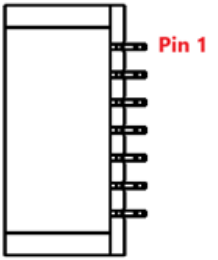
2.3 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
CN1	SPI ROM Flash
CN2	MIPI CSI CH 1
CN3	MIPI CSI CH 2
CN4	Row A/B
CN5	Row C/D
JDDR1	DDR5 SODIMM A
JDDR2	DDR5 SODIMM B

2.3.1 SPI ROM Flash (CN1)

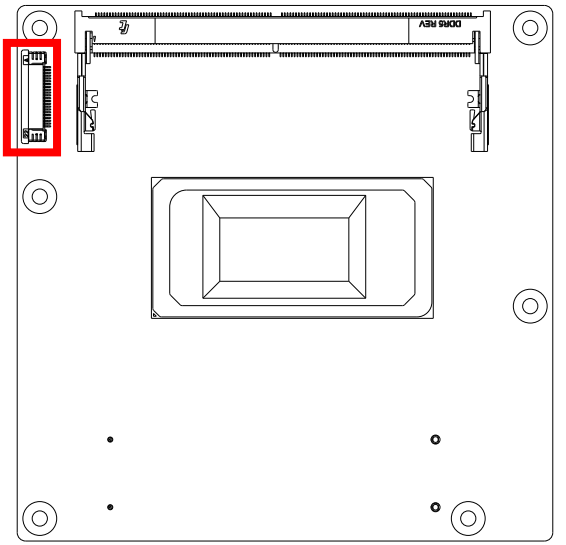


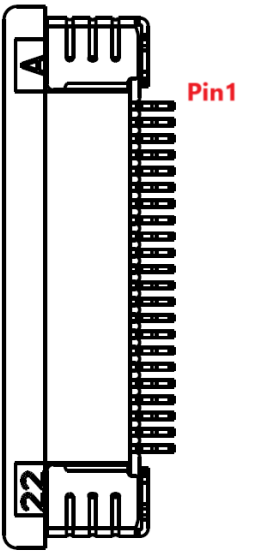


Pin	Signal
1	VCC_3.3V
2	VCC_3.3V
3	GND
4	CSI_DP_0
5	CSI_DN_0
6	GND
7	CSI_DP_1
8	CSI_DN_1
9	GND
10	CSI_DP_2
11	CSI_DN_2
12	CAM_RST#
13	CSI_DP_3
14	CSI_DN_3
15	GND
16	CSI_CLK_P
17	CSI_CLK_N
18	GND
19	I2C_CLK
20	I2C_DAT

Pin	Signal
21	CRD_PWREN
22	IMGCLKOUT

2.3.2 MIPI CSI CH 1 (CN2)

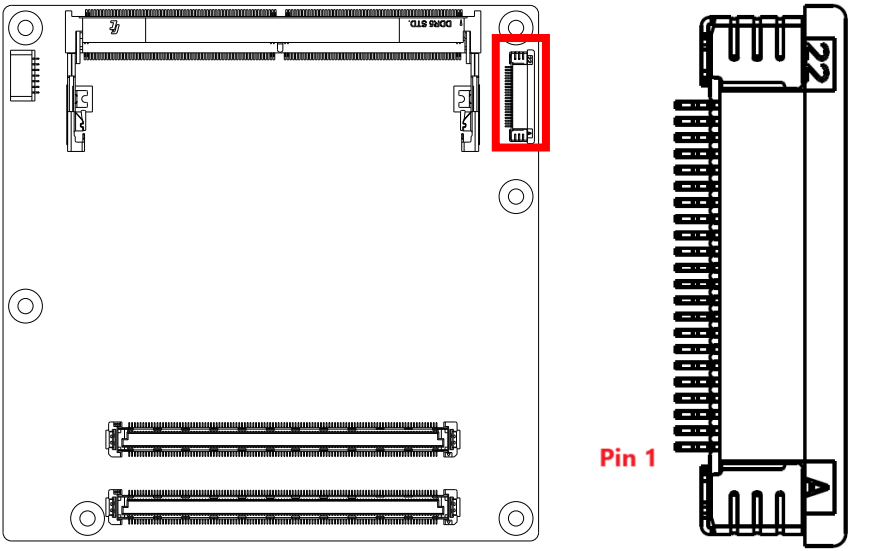




Pin	Signal
1	VCC_3.3V
2	VCC_3.3V
3	GND
4	CSI_DP_0
5	CSI_DN_0
6	GND
7	CSI_DP_1
8	CSI_DN_1
9	GND
10	CSI_DP_2
11	CSI_DN_2
12	CAM_RST#
13	CSI_DP_3
14	CSI_DN_3
15	GND
16	CSI_CLK_P

Pin	Signal
17	CSI_CLK_N
18	GND
19	I2C_CLK
20	I2C_DAT
21	CRD_PWREN
22	IMGCLKOUT

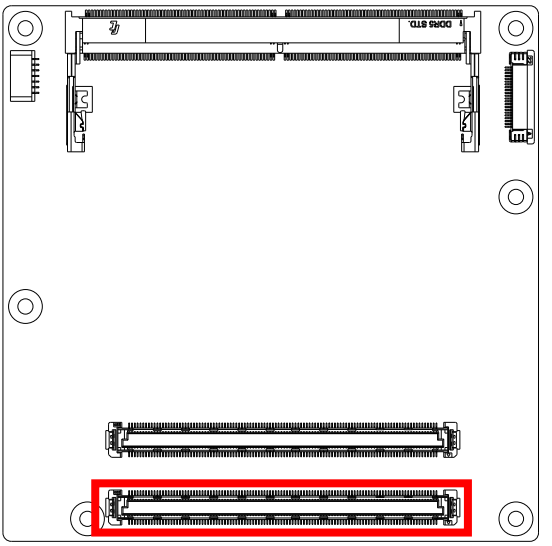
2.3.3 MIPI CSI CH 2 (CN3)

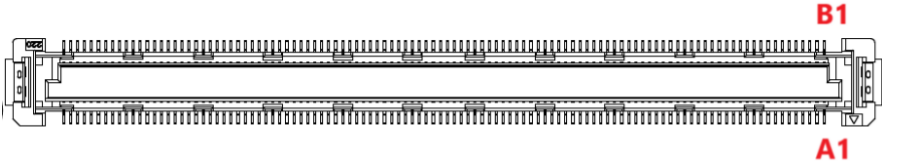


Pin	Signal
1	VCC_3.3V
2	VCC_3.3V
3	GND
4	CSI_DP_0
5	CSI_DN_0
6	GND
7	CSI_DP_1
8	CSI_DN_1
9	GND
10	CSI_DP_2
11	CSI_DN_2
12	CAM_RST#

Pin	Signal
13	CSI_DP_3
14	CSI_DN_3
15	GND
16	CSI_CLK_P
17	CSI_CLK_N
18	GND
19	I2C_CLK
20	I2C_DAT
21	CRD_PWREN
22	IMGCLKOUT

2.3.4 Row A/B Connector (CN4)





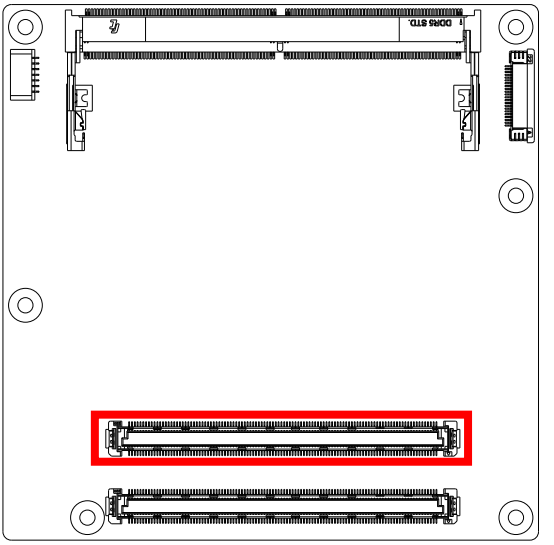
Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#

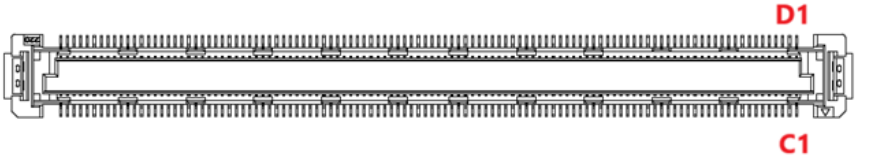
Row A		Row B	
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK1000#	B4	LPC_AD0
A5	GBE0_LINK2500#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CLK (from SOC)
A14	GBE0_CTREF	B14	SMB_DAT (from SOC)
A15	SUS_S3#	B15	SMB_ALERT# (from SOC)
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	N.C	B22	PCIE_6_CLK_DP (reserve)
A23	N.C	B23	PCIE_6_CLK_DN (reserve)
A24	SUS_S5#	B24	PWR_OK
A25	N.C	B25	N.C
A26	N.C	B26	N.C
A27	BATLOW#	B27	WDT
A28	SATA_ACT#	B28	SNDW0_CLK
A29	HDA_SYNC	B29	SNDW0_DAT
A30	HDA _RST#	B30	HDA _SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	HDA _BITCLK	B32	SPKR
A33	HDA _SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	CB_THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)

Row A		Row B	
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	N.C
A48	RSMRST_OUT#	B48	N.C
A49	GBE0_SDP	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	PCIE_TX5+ (CPU)	B52	PCIE_RX5+ (CPU)
A53	PCIE_TX5- (CPU)	B53	PCIE_RX5- (CPU)
A54	GPI0	B54	GPO1
A55	PCIE_TX4+ (CPU)	B55	PCIE_RX4+ (CPU)
A56	PCIE_TX4- (CPU)	B56	PCIE_RX4- (CPU)
A57	GND	B57	GPO2
A58	PCIE_TX3+ (PCH)	B58	PCIE_RX3+ (PCH)
A59	PCIE_TX3- (PCH)	B59	PCIE_RX3- (PCH)
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+ (PCH)	B61	PCIE_RX2+ (PCH)
A62	PCIE_TX2- (PCH)	B62	PCIE_RX2- (PCH)
A63	GPI1	B63	GPO3
A64	PCIE_TX1+ (PCH)	B64	PCIE_RX1+ (PCH)
A65	PCIE_TX1- (PCH)	B65	PCIE_RX1- (PCH)
A66	GND	B66	WAKE0# (PCH)
A67	GPI2_TSYNC0	B67	WAKE1# (EC)
A68	PCIE_TX0+ (PCH)	B68	PCIE_RX0+ (PCH)
A69	PCIE_TX0- (PCH)	B69	PCIE_RX0- (PCH)
A70	GND (FIXED)	B70	GND (FIXED)
A71	**LVDS_A0+** / eDP_PAIR2+	B71	LVDS_B0+
A72	**LVDS_A0-** / eDP_PAIR2-	B72	LVDS_B0-
A73	**LVDS_A1+** / eDP_PAIR1+	B73	LVDS_B1+
A74	**LVDS_A1-** / eDP_PAIR1-	B74	LVDS_B1-
A75	**LVDS_A2+** /eDP_PAIR0+	B75	LVDS_B2+
A76	**LVDS_A2-** /eDP_PAIR0-	B76	LVDS_B2-
A77	LVDS_VDD_EN	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN /eDP_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)

Row A		Row B	
A81	**LVDS_A_CK+** /eDP_PAIR0+	B81	LVDS_B_CK+
A82	**LVDS_A_CK-** /eDP_PAIR0-	B82	LVDS_B_CK-
A83	**LVDS_I2C_CK** /eDP_AUX_DN	B83	**LVDS_BKLT_CTRL** /eDP_BKLT_CTRL
A84	**LVDS_I2C_DAT** /eDP_AUX_DP	B84	VCC_5V_SBY
A85	GPI3_TSYNC1	B85	VCC_5V_SBY
A86	GSPI0_MOSI	B86	VCC_5V_SBY
A87	EDP_HPD	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	GND	B96	VGA_I2C_DAT
A97	N.C	B97	SPI_CS#
A98	CB_STXD1X	B98	GSPI0_MISO
A99	CB_SRXD1X	B99	GSPI0_CLK
A100	GND (FIXED)	B100	GND (FIXED)
A101	CB_STXD2X	B101	CB_FAN_PWM
A102	CB_SRXD2X	B102	CB_FAN_TACH
A103	LID# (EC)	B103	SLEEP# (EC)
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

2.3.5 Row C/D Connector (CN5)





Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND (FIXED)	D2	GND (FIXED)
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND (FIXED)	D5	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND (FIXED)	D8	GND (FIXED)
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	GND (FIXED)	D14	GND (FIXED)
C15	USB4_1_LSTX	D15	DDI1_CTRLCLK_AUX+

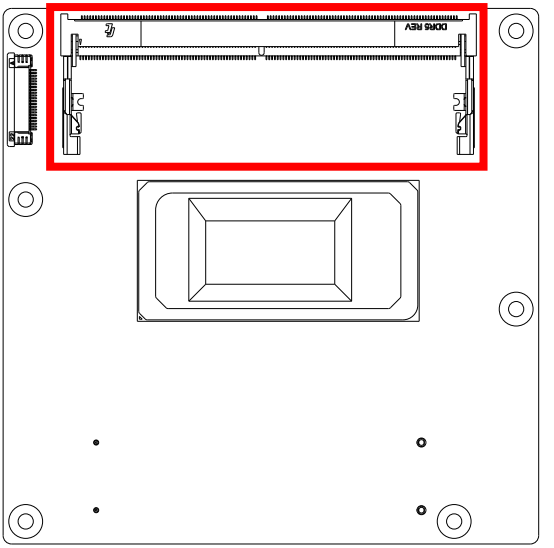
Row C		Row D	
C16	USB4_1_LSRX	D16	DDI1_CTRLDATA_AUX-
C17	USB4_RT_ENA	D17	N.C
C18	GND	D18	USB4_PMCALERT#
C19	PCIE_RX6+ (CPU)	D19	PCIE_TX6+ (CPU)
C20	PCIE_RX6- (CPU)	D20	PCIE_TX6- (CPU)
C21	GND (FIXED)	D21	GND (FIXED)
C22	PCIE_RX7+ (CPU)	D22	PCIE_TX7+ (CPU)
C23	PCIE_RX7- (CPU)	D23	PCIE_TX7- (CPU)
C24	DDI1_HPD	D24	GND
C25	USB4_SML0_CLK	D25	GND
C26	USB4_SML0_DAT	D26	DDI1_PAIR0+
C27	USB4_SML1_CLK	D27	DDI1_PAIR0-
C28	USB4_SML1_DAT	D28	GND
C29	USB4_I2C_CLK	D29	DDI1_PAIR1+
C30	USB4_I2C_DAT	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	USB4_2_LSTX	D35	USB4_2_LSRX
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
C38	DDI3_DDC_AUX_SEL	D38	GND
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	GSPI0_CS0#	D45	GND
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	GND
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+ (CPU x8) *	D52	PEG_TX0+ (CPU x8) *
C53	PEG_RX0- (CPU x8) *	D53	PEG_TX0- (CPU x8) *
C54	N.C	D54	PEG_LANE_RV#

Row C		Row D	
C55	PEG_RX1+ (CPU x8) *	D55	PEG_TX1+ (CPU x8) *
C56	PEG_RX1- (CPU x8) *	D56	PEG_TX1- (CPU x8) *
C57	N.C	D57	GND
C58	PEG_RX2+ (CPU x8) *	D58	PEG_TX2+ (CPU x8) *
C59	PEG_RX2- (CPU x8) *	D59	PEG_TX2- (CPU x8) *
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+ (CPU x8) *	D61	PEG_TX3+ (CPU x8) *
C62	PEG_RX3- (CPU x8) *	D62	PEG_TX3- (CPU x8) *
C63	GND	D63	GND
C64	GND	D64	GND
C65	PEG_RX4+ (CPU x8) *	D65	PEG_TX4+ (CPU x8) *
C66	PEG_RX4- (CPU x8) *	D66	PEG_TX4- (CPU x8) *
C67	N.C	D67	GND (FIXED)
C68	PEG_RX5+ (CPU x8) *	D68	PEG_TX5+ (CPU x8) *
C69	PEG_RX5- (CPU x8) *	D69	PEG_TX5- (CPU x8) *
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+ (CPU x8) *	D71	PEG_TX6+ (CPU x8) *
C72	PEG_RX6- (CPU x8) *	D72	PEG_TX6- (CPU x8) *
C73	GND (FIXED)	D73	GND (FIXED)
C74	PEG_RX7+ (CPU x8) *	D74	PEG_TX7+ (CPU x8) *
C75	PEG_RX7- (CPU x8) *	D75	PEG_TX7- (CPU x8) *
C76	GND (FIXED)	D76	GND (FIXED)
C77	GND	D77	GND
C78	PEG_RX8+ (CPU x4_A)	D78	PEG_TX8+ (CPU x4_A)
C79	PEG_RX8- (CPU x4_A)	D79	PEG_TX8- (CPU x4_A)
C80	GND (FIXED)	D80	GND (FIXED)
C81	PEG_RX9+ (CPU x4_A)	D81	PEG_TX9+ (CPU x4_A)
C82	PEG_RX9- (CPU x4_A)	D82	PEG_TX9- (CPU x4_A)
C83	GND	D83	GND
C84	GND (FIXED)	D84	GND (FIXED)
C85	PEG_RX10+ (CPU x4_A)	D85	PEG_TX10+ (CPU x4_A)
C86	PEG_RX10- (CPU x4_A)	D86	PEG_TX10- (CPU x4_A)
C87	GND (FIXED)	D87	GND (FIXED)
C88	PEG_RX11+ (CPU x4_A)	D88	PEG_TX11+ (CPU x4_A)
C89	PEG_RX11- (CPU x4_A)	D89	PEG_TX11- (CPU x4_A)
C90	GND (FIXED)	D90	GND (FIXED)
C91	PEG_RX12+ (CPU x4_B) Default reserve	D91	PEG_TX12+ (CPU x4_B) Default reserve

Row C		Row D	
C92	PEG_RX12- (CPU x4_B) Default reserve	D92	PEG_TX12- (CPU x4_B) Default reserve
C93	GND	D93	GND
C94	PEG_RX13+ (CPU x4_B) Default reserve	D94	PEG_TX13+ (CPU x4_B) Default reserve
C95	PEG_RX13- (CPU x4_B) Default reserve	D95	PEG_TX13- (CPU x4_B) Default reserve
C96	GND (FIXED)	D96	GND (FIXED)
C97	GND	D97	GND
C98	PEG_RX14+ (CPU x4_B)	D98	PEG_TX14+ (CPU x4_B)
C99	PEG_RX14- (CPU x4_B)	D99	PEG_TX14- (CPU x4_B)
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+ (CPU x4_B)	D101	PEG_TX15+ (CPU x4_B)
C102	PEG_RX15- (CPU x4_B)	D102	PEG_TX15- (CPU x4_B)
C103	GND (FIXED)	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

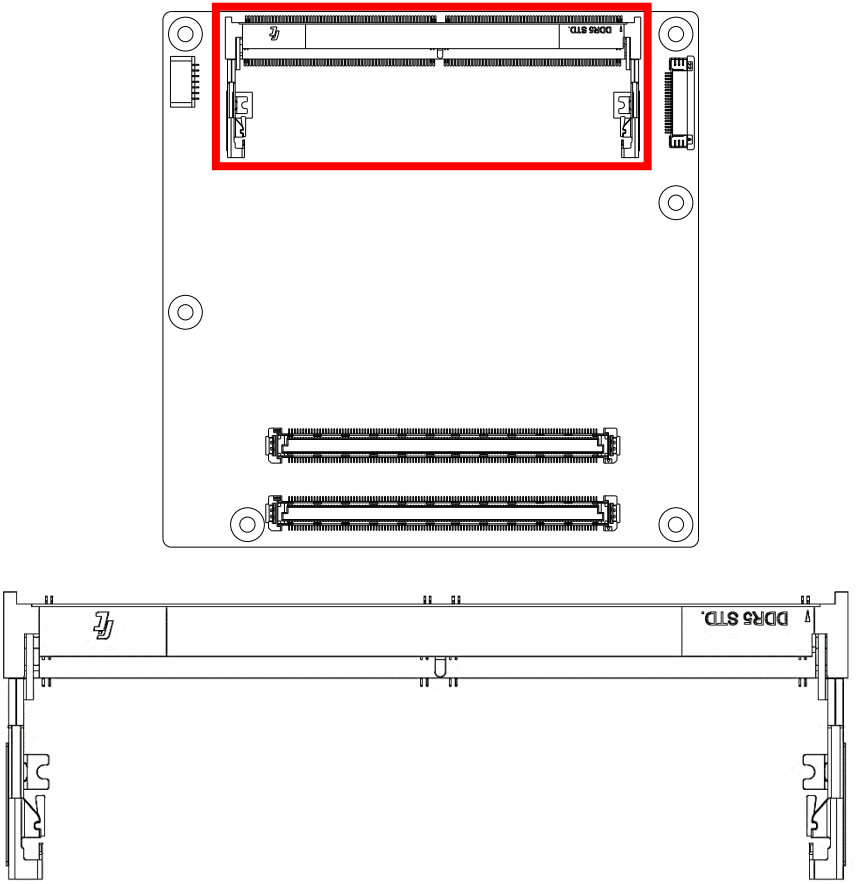
Note: PEG [x4] co-lay onboard NVMe.

2.3.6 DDR5 SODIMM A (JDDR1)



Note: JDDR1 contains a standard DDR5 SODIMM pinout interface.

2.3.7 DDR5 SODIMM B (JDDR2)



Note: JDDR2 contains a standard DDR5 SODIMM pinout interface.

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If a system configuration is not found or a system configuration data error is detected, the system will load the optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

- You are starting your system for the first time.
- You have changed the hardware attached to your system.
- The system configuration is reset by Clear-CMOS jumper
- The CMOS memory has lost power and the configuration information has been erased.

The COM-ARHC6 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the battery when it finally runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This information is stored in the battery-backed CMOS RAM and BIOS NVRAM so it retains the Setup information when the power is turned off.

To enter Setup, power on the computer and press <Del> immediately.

The function of each menu is as follows:

Main – Date and time can be set here. Use <Tab> to switch between date elements.

Advanced – Enable/disable boot option for legacy network devices.

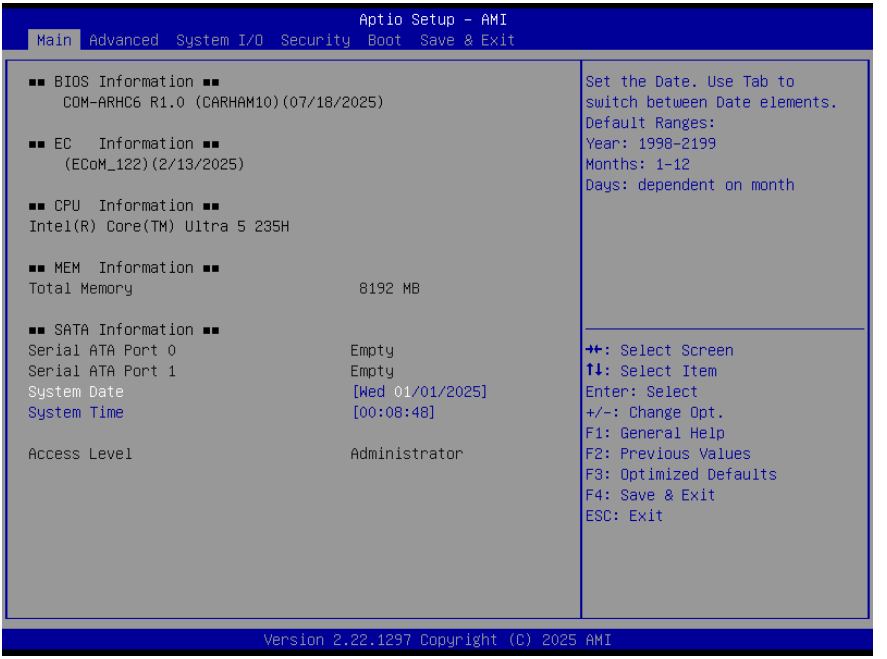
System I/O – Host bridge parameters.

Security – Set administrator password.

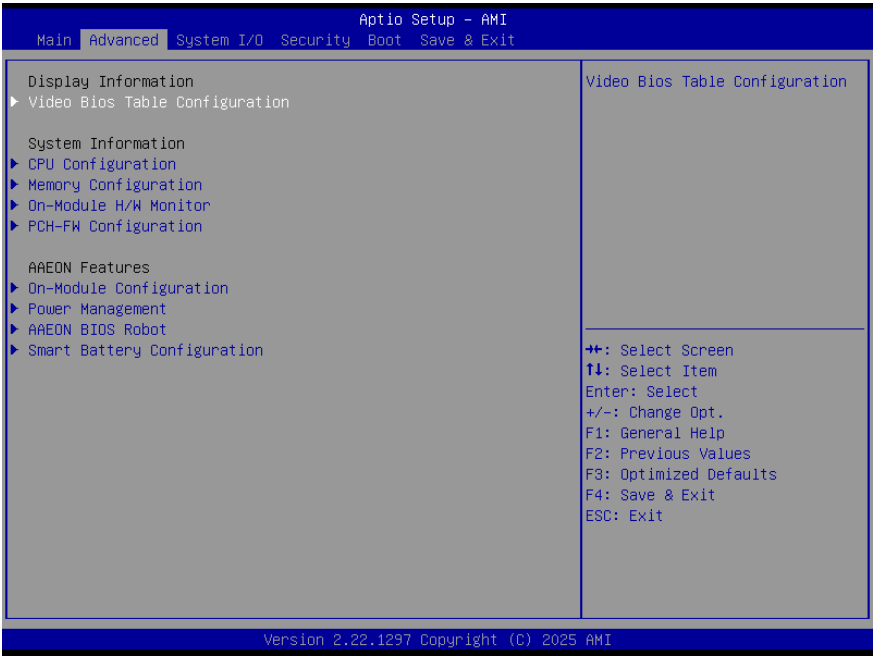
Boot – Enable/disable Quiet Boot option.

Save & Exit – Save changes and exit Setup.

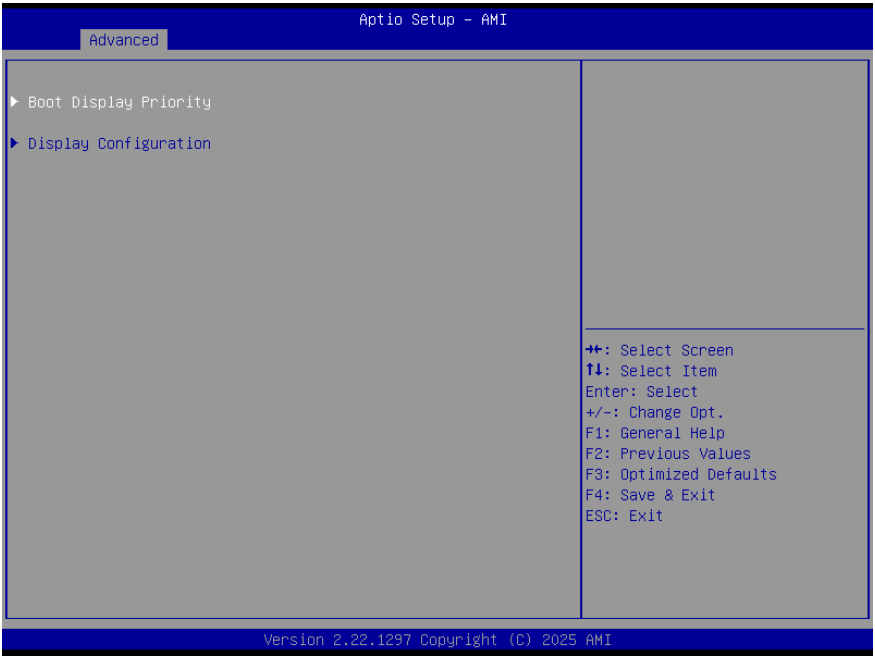
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



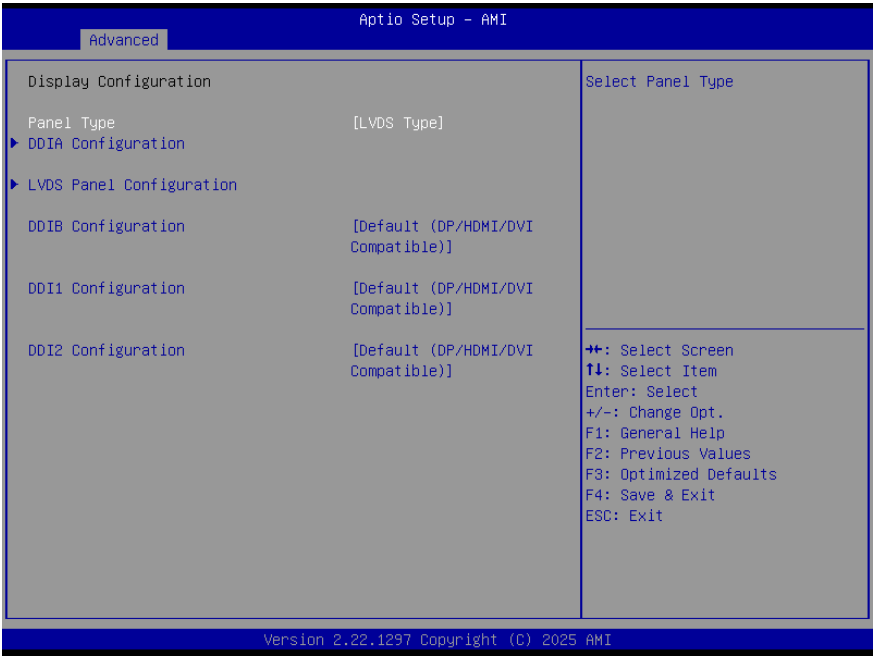
3.4.1 Video BIOS Table Configuration



3.4.1.1 Boot Display Priority

Options Summary		
Boot Display Priority Override	Enabled	
	GOP Default	Optimal Default, Failsafe Default
Boot Display Priority Override.		

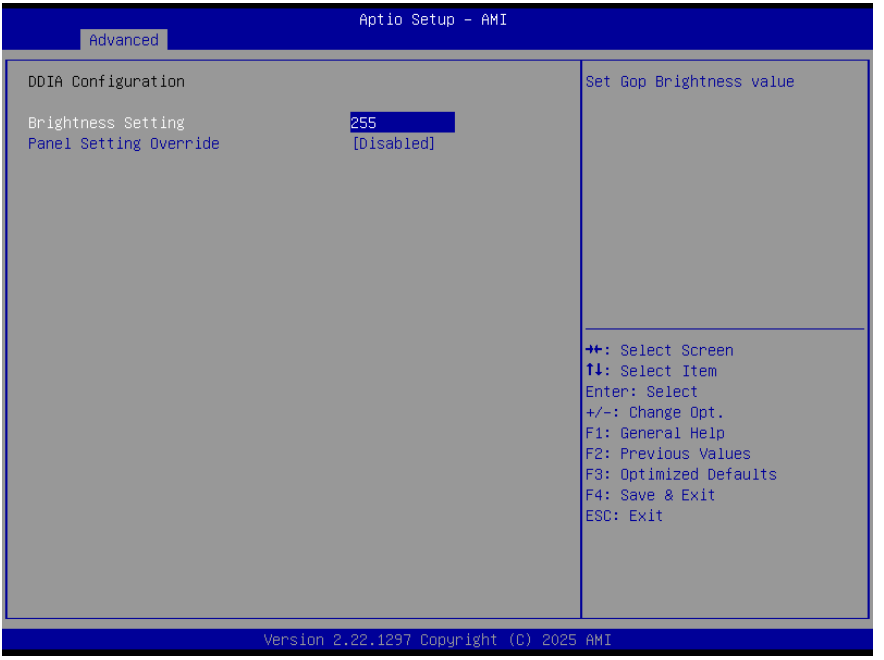
3.4.1.2 Display Configuration



Options Summary		
Panel Type	eDP Type	
	LVDS Type	Optimal Default, Failsafe Default
Select Panel Type.		
DDIB Configuration	No Device	
	DP	
	DP/HDMI/DVI Compatible	
	HDMI/DVI	
	Default (DP/HDMI/DVI Compatible)	Optimal Default, Failsafe Default
Select output type for this device.		
DDI1 Configuration	No Device	
	DP	
	DP/HDMI/DVI Compatible	
	HDMI/DVI	

Options Summary		
DDI1 Configuration (cont.)	Default (DP/HDMI/DVI Compatible)	Optimal Default, Failsafe Default
Select output type for this device.		
DDI2 Configuration	No Device	
	DP	
	DP/HDMI/DVI Compatible	
	HDMI/DVI	
	Default (DP/HDMI/DVI Compatible)	Optimal Default, Failsafe Default
Select output type for this device.		

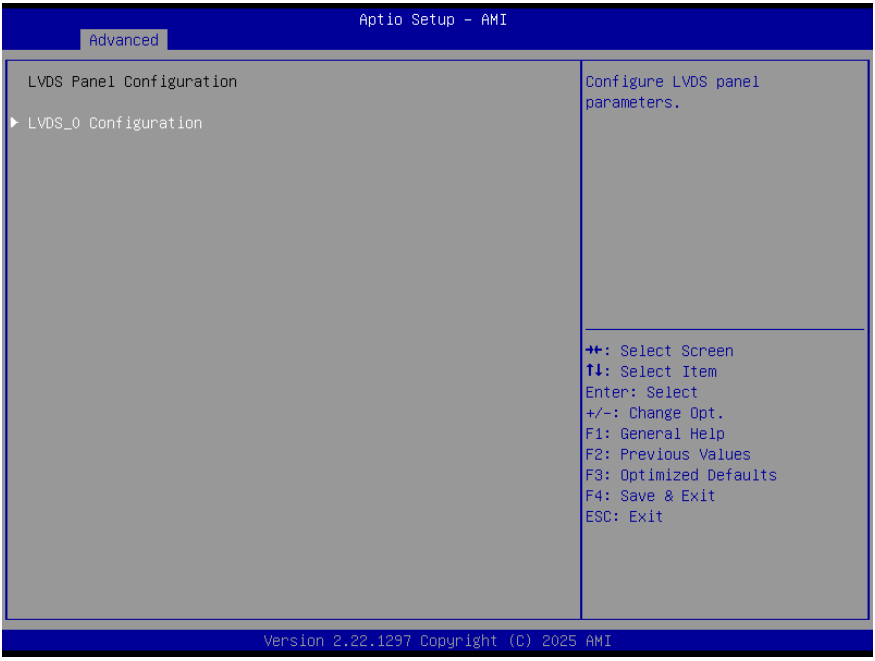
3.4.1.3 DDIA Configuration



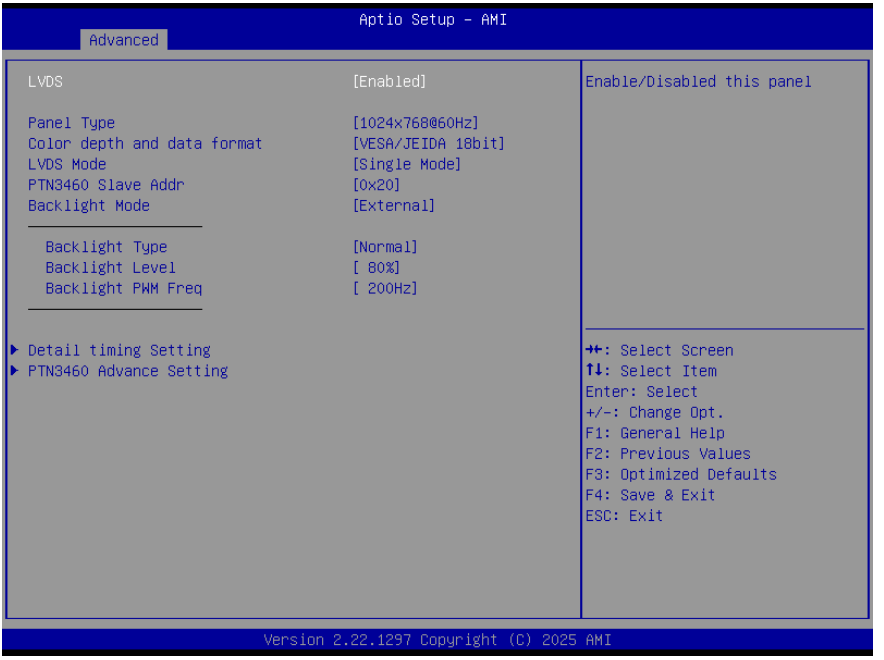
Options Summary		
Brightness Setting	255	Optimal Default, Failsafe Default
Set Gop Brightness value.		

Options Summary		
Panel Setting Override	Enabled	
	Disabled	Optimal Default, Failsafe Default
Panel Setting Override.		

3.4.1.4 LVDS Panel Configuration



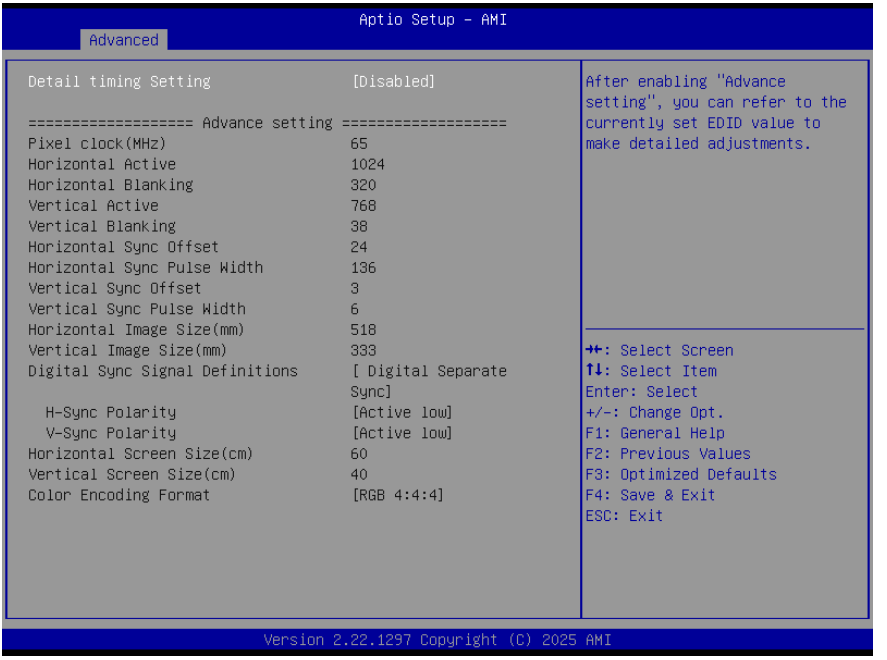
3.4.1.5 LVDS_0 Configuration



Options Summary		
LVDS	Enabled	Optimal Default, Failsafe Default
	Disable	
Enable/Disable this panel		
Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x768@60Hz	
	1280x800@60Hz	
	1280x1024@60hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	
	1920x1200@60Hz	

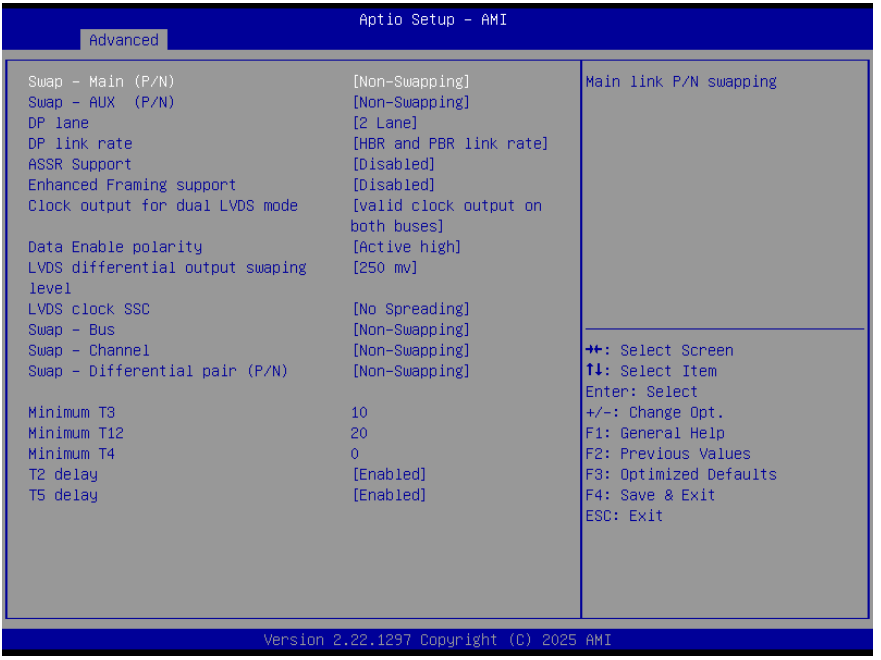
Options Summary		
Select panel type		
Color depth and data format	VESA 24bit	
	JEIDA 24bit	
	VEAS/JEIDA 18bit	Optimal Default, Failsafe Default
Color Depth and Data Packing Format – Sets display color depth and data format. Note: To use 36-bit or 48-bit mode, set LVDS Mode to Dual Mode.		
LVDS mode	Single Mode	Optimal Default, Failsafe Default
	Dual Mode	
Single/Dual Mode		
PTN3460 Slave Addr	0x20	Optimal Default, Failsafe Default
	0x60	
Sets the slave address for the PTN3460 device.		
Backlight Mode	External	Optimal Default, Failsafe Default
	Internal	
Select how the backlight is controlled: Internal – Controlled via driver; supports Windows brightness bar. External – Controlled via EAPI.		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control method.		
Backlight Level	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200 Hz	Optimal Default, Failsafe Default
	220 Hz	
	500 Hz	
	1K Hz	
	2.2K Hz	
	6.5K Hz	
Select PWM Frequency of backlight control signal		

3.4.1.6 Detail Timing Setting



Options Summary		
Detail timing Setting	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, allows detailed adjustments based on the currently set EDID value.		

3.4.1.7 PTN3460 Advance Setting

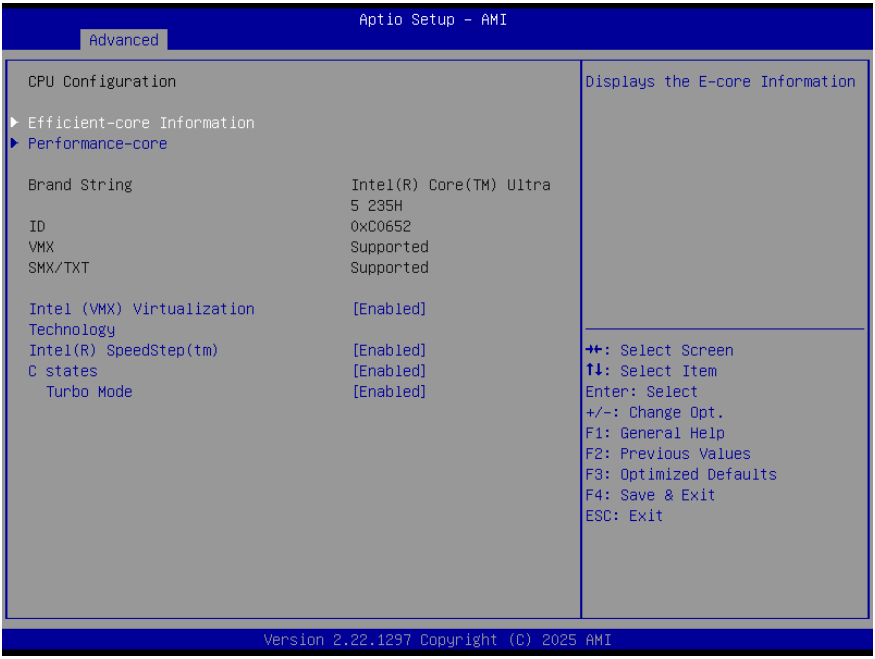


Options Summary		
Swap - Main (P/N)	Non-Swapping	Optimal Default, Failsafe Default
	Swapping	
Main link P/N swapping		
Swap - AUX (P/N)	Non-Swapping	Optimal Default, Failsafe Default
	Swapping	
AUX P/N swapping		
DP lane	2 Lane	Optimal Default, Failsafe Default
	1 Lane	
DP lane configuration		
DP link rate	HBR and PBR link rate	Optimal Default, Failsafe Default
	PBR link rate only DP lane	
DP link configuration		
ASSR Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Alternative Scrambler Seed Reset		

Options Summary		
Enhanced Framing support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enhanced Framing support		
Clock output for dual LVDS mode	valid clock output on even bus only	
	valid clock output on odd bus only	
	valid clock output on both buses	Optimal Default, Failsafe Default
Clock output for dual LVDS mode		
Data Enable polarity	Active high	Optimal Default, Failsafe Default
	Active low	
Data Enable polarity		
LVDS differential output swapping level	150mv	
	200mv	
	250mv	Optimal Default, Failsafe Default
	300mv	
	350mv	
	400mv	
	450mv	
LVDS differential output swapping level		
LVDS clock SSC	No Spreading	Optimal Default, Failsafe Default
	0.5% Spreading	
	1.0% Spreading	
	1.5% Spreading	
	2.0% Spreading	
	2.5% Spreading	
LVDS clock frequency center spreading depth		
Swap - Bus	Non-Swapping	Optimal Default, Failsafe Default
	Swapped	
Odd bus <-> Even Bus		
Swap - Channel	Non-Swapping	Optimal Default, Failsafe Default
	Swapped	
(A ↔ D, B ↔ CLK, C↔ C)		
Swap - Differential pair (P/N)	Non-Swapping	Optimal Default, Failsafe Default
	Swapped	
Differential pair (P/N) Swapping		
Minimum T3	10	Optimal Default, Failsafe Default
Sets the minimum T3 timing of the panel power sequence, expressed in units of 50 ms.		

Options Summary		
Minimum T12	20	Optimal Default, Failsafe Default
Sets the minimum T12 timing of the panel power sequence, expressed in units of 50 ms.		
Minimum T4	0	Optimal Default, Failsafe Default
Sets the minimum T4 timing of the panel power sequence, expressed in units of 50 ms.		
T2 delay	Disabled	
	Enabled	Optimal Default, Failsafe Default
Sets T2 delay to 20 ms.		
T5 delay	Disabled	
	Enabled	Optimal Default, Failsafe Default
Sets T5 delay to 20 ms.		

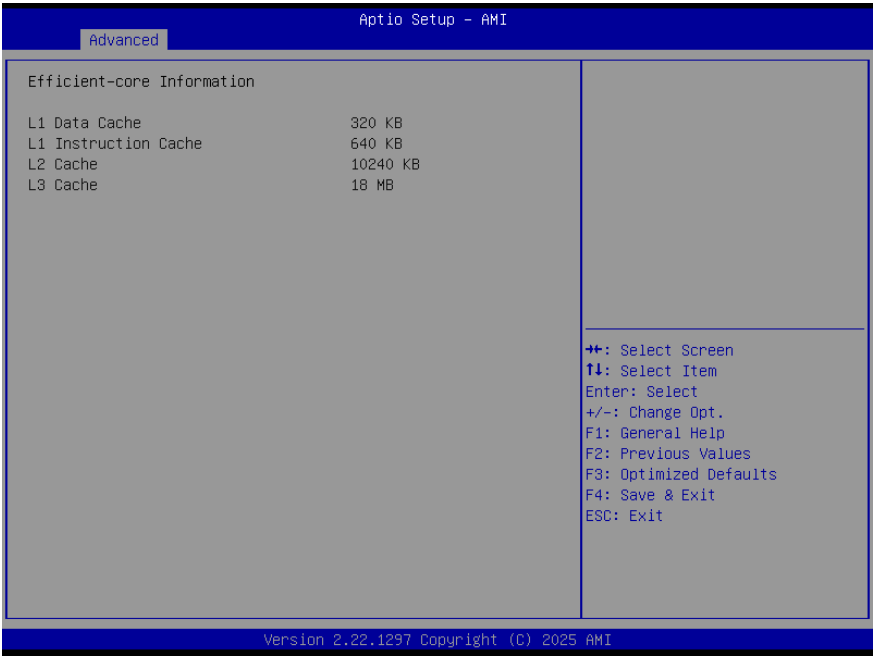
3.4.2 CPU Configuration



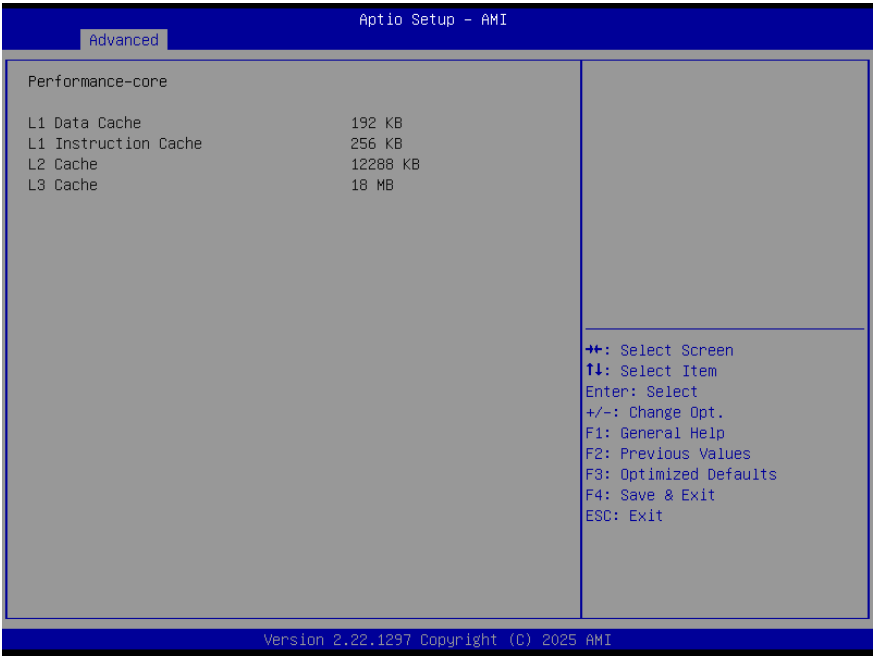
Options Summary		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default

Options Summary		
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Intel(R) SpeedStep(tm)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Allows more than two frequency ranges to be supported.		
C states	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable CPU power management. When enabled, the CPU can enter C-states when not fully utilized.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable processor Turbo Mode.		

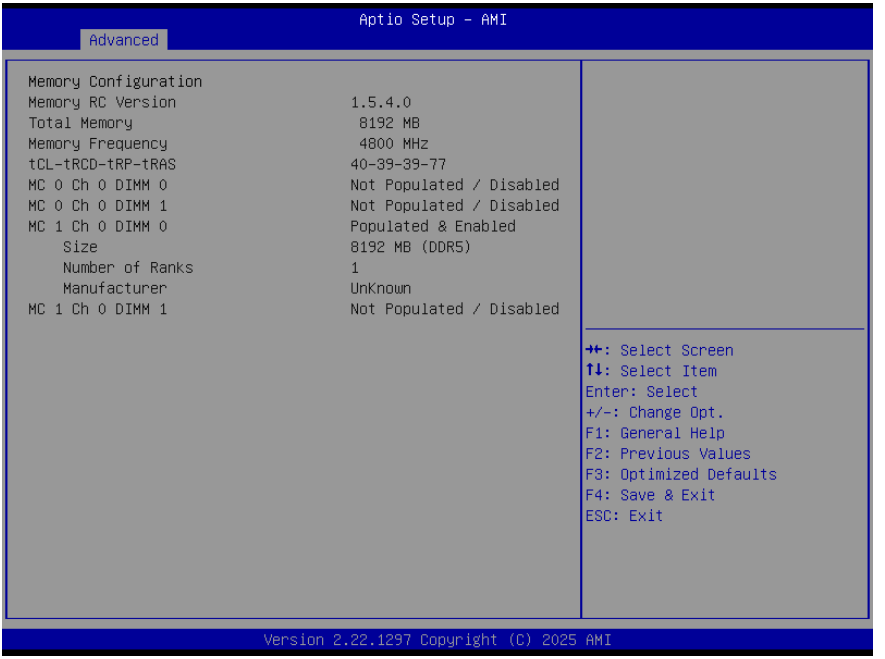
3.4.2.1 Efficient-Core Information



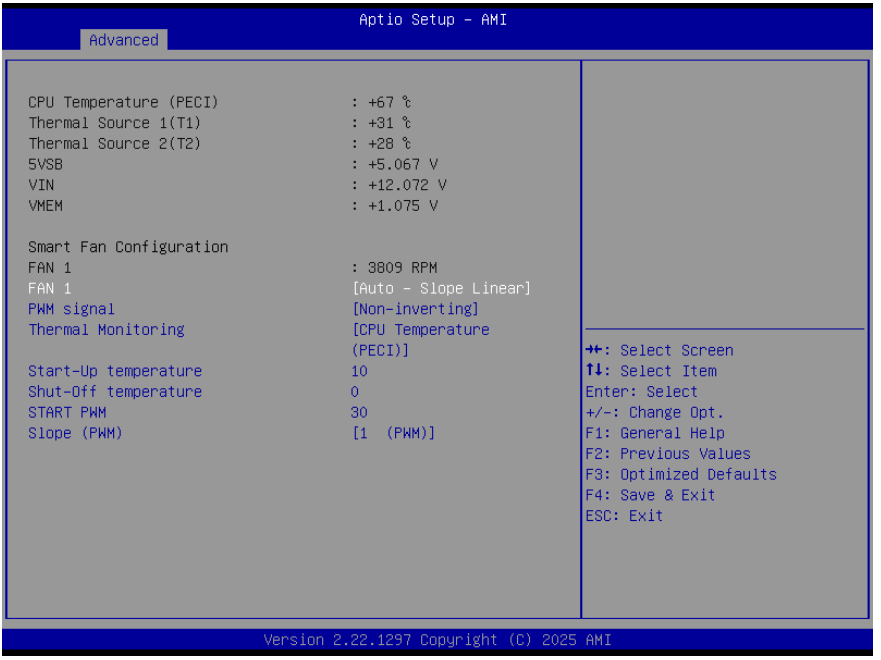
3.4.2.2 Performance-Core Information



3.4.3 Memory Configuration



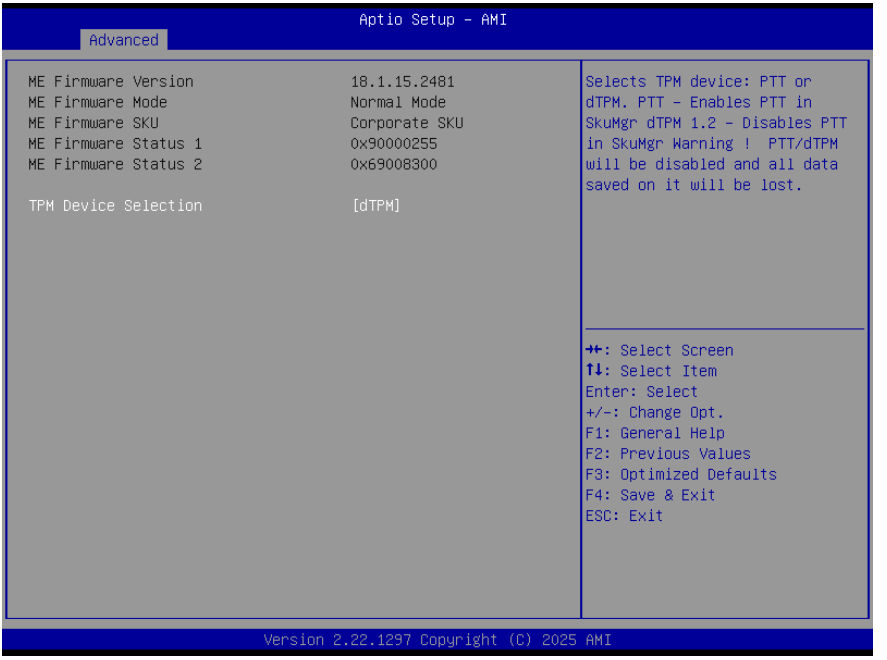
3.4.4 On-Module H/W Monitor



Options Summary		
FAN 1	Full Mode	
	Manual Mode	
	Auto – Slope Linear	Optimal Default, Failsafe Default
Smart Fan Mode Select.		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select whether the PWM output signal is inverting or non-inverting.		
Thermal Monitoring	CPU Temperature (PECI)	Optimal Default, Failsafe Default
	Thermal Source 1 (T1)	
	Thermal Source 2 (T2)	
Thermal Sensor Selection – Choose which thermal sensor to monitor.		
Start-Up temperature	10	Optimal Default, Failsafe Default
Sets the PWM output when the monitored thermal sensor exceeds its threshold. Range: 0–100.		
Shut-Off temperature	0	Optimal Default, Failsafe Default

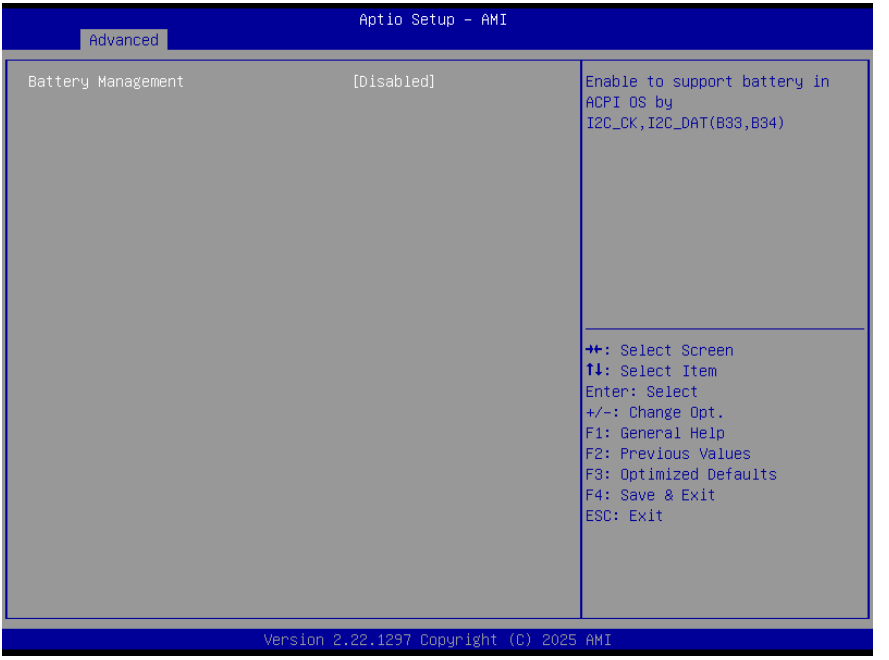
Options Summary		
Turns off PWM output when the monitored thermal sensor is less than or equal to the set value. Range: 0–100.		
START PWM	30	Optimal Default, Failsafe Default
Sets the initial PWM output value when the Start-Up temperature is reached.		
Slope (PWM)	0 (PWM)	
	1 (PWM)	Optimal Default, Failsafe Default
	2 (PWM)	
	4 (PWM)	
	8 (PWM)	
	16 (PWM)	
	32 (PWM)	
	64 (PWM)	
Increases PWM output per degree when the monitored temperature exceeds the Start-Up temperature.		

3.4.5 PCH-FW Configuration



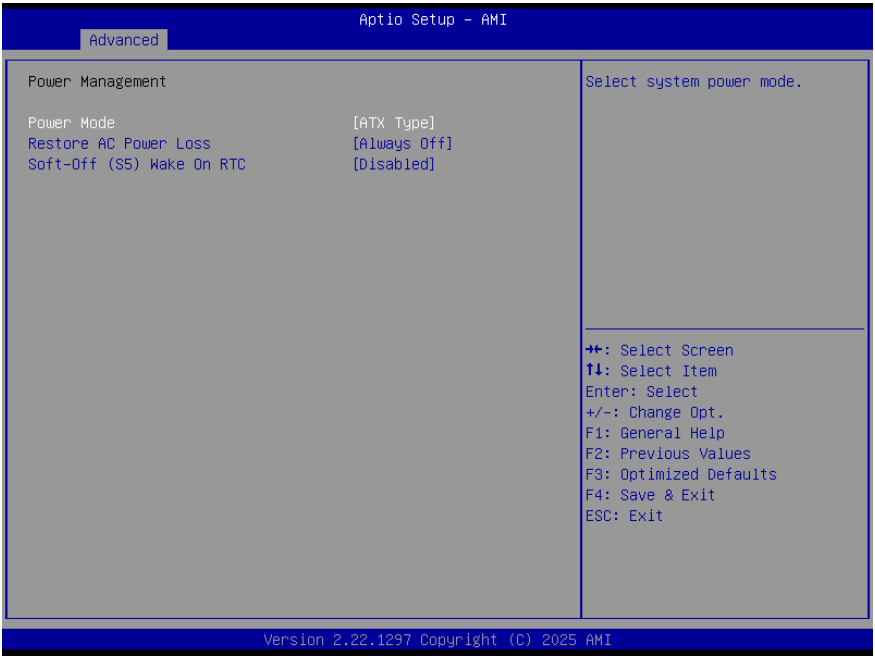
Options Summary		
TPM Device Selection	dTPM	Optimal Default, Failsafe Default
	PTT	
TPM Device Selection – Choose the TPM device: PTT – Enables PTT in SkuMgr. dTPM 1.2 – Disables PTT in SkuMgr. **Warning**: Switching between PTT and dTPM will disable the current TPM and all data stored on it will be lost.		

3.4.6 On-Module Configuration



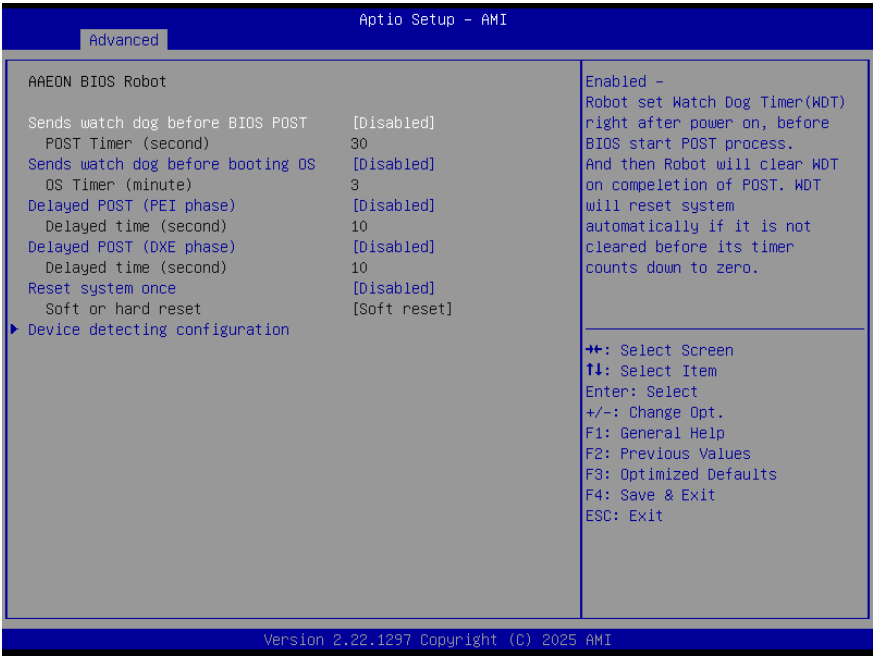
Options Summary		
Battery Management	Disabled	Optimal Default, Failsafe Default
	One Battery	
Enable to support the battery in an ACPI-compliant OS via I2C_CK and I2C_DAT (pins B33, B34).		

3.4.7 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	
	Always On	
	Always Off	Optimal Default, Failsafe Default
IO Restore AC power Loss.		
Soft-Off (S5) Wake On RTC	Disabled	Optimal Default, Failsafe Default
	By Date	
	By Weekday	
	Bypass	
By Date – Wakes on the specified date and time (hr:min:sec). By Weekday – Wakes on the selected weekday and time (hr:min:sec). Bypass – Disables BIOS control of the RTC wake function.		

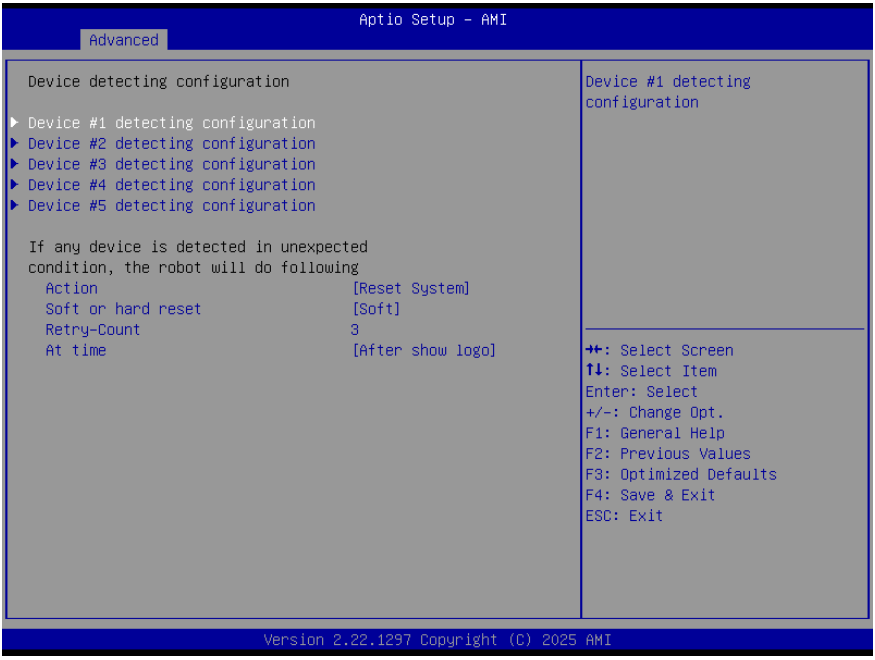
3.4.8 AAEON BIOS Robot



Options Summary		
Sends watch dog before BIOS POST	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, the Robot sets the Watchdog Timer (WDT) immediately after power-on, before BIOS POST. The WDT is cleared after POST completes. If not cleared before timeout, the WDT will automatically reset the system.		
POST Timer (second)	30	Optimal Default, Failsafe Default
Sets the Watchdog Timer duration for POST. **Warning:** Do not set equal to or shorter than normal POST time, or the system may fail to complete POST unless BIOS settings are cleared. Recommended: more than 2× normal POST time.		
Sends watch dog before booting OS	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, the Robot sets the Watchdog Timer (WDT) after POST, before BIOS hands control to the OS. **Warning**: The OS must include a program to clear the WDT. Disable this function if the OS will perform updates.		
OS Timer (minute)	3	Optimal Default, Failsafe Default
Sets the Watchdog Timer duration during OS boot/loading.		

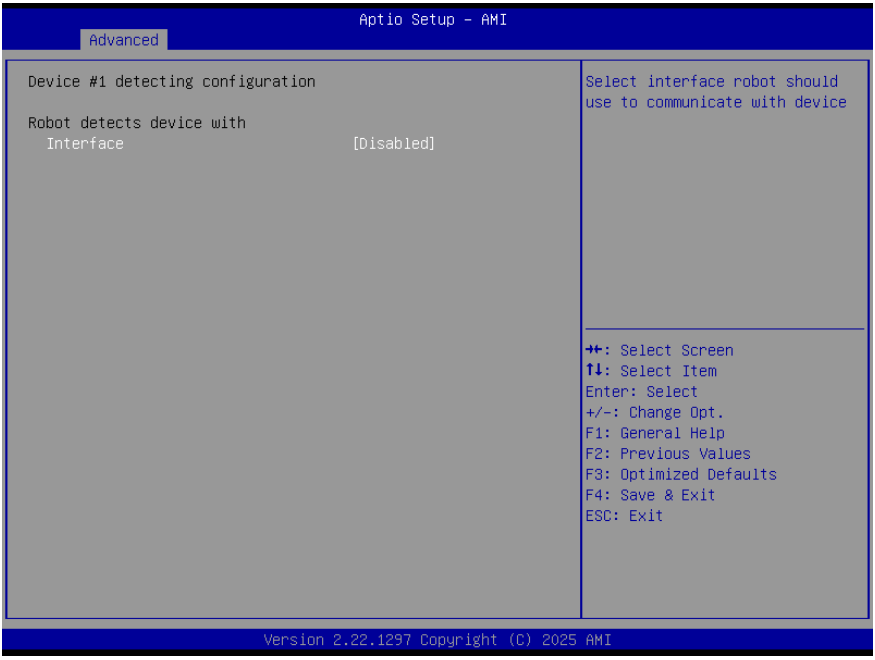
Options Summary		
Delayed POST (PEI phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, the Robot delays BIOS POST immediately after power-on, allowing POST to start with stable power or after system warm-up. *Note:* This occurs before "Send Watchdog."		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Delayed POST (DXE phase)	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, the Robot delays BIOS until POST completes, allowing POST to start with stable power or after system warm-up. *Note:* This occurs after "Send Watchdog before BIOS POST."		
Delayed time (second)	10	Optimal Default, Failsafe Default
Period of time for Robot to hold BIOS from POST.		
Reset system once	Disabled	Optimal Default, Failsafe Default
	Enabled	
When enabled, the Robot performs a single system reset on each boot, sending a soft or hard reset to onboard devices to ensure a more stable state.		
Soft or hard reset	Soft reset	Optimal Default, Failsafe Default
	Hard reset"	
Select the type of reset the Robot will send on each boot (e.g., soft or hard reset).		

3.4.8.1 Device Detecting Configuration



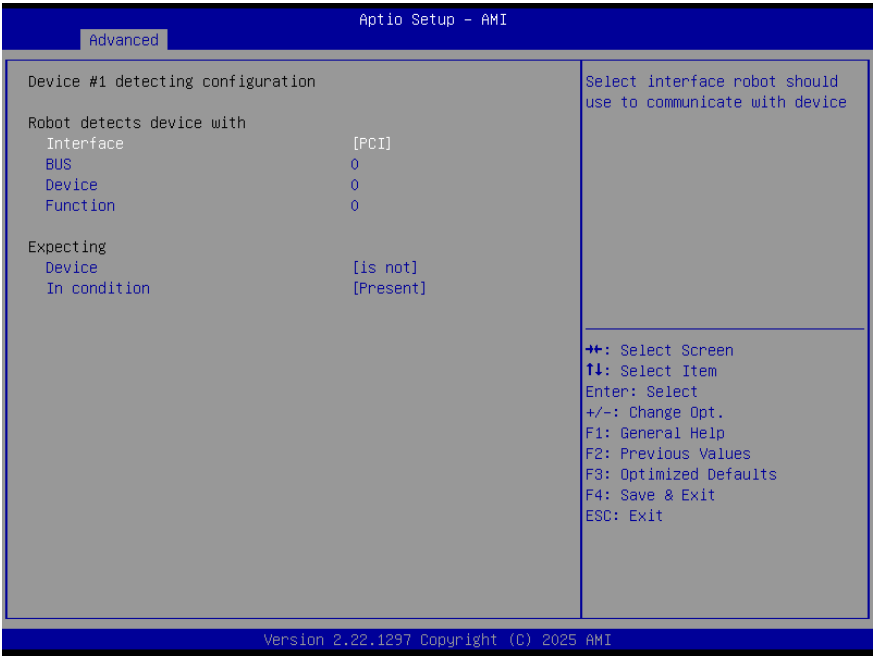
Options Summary		
Action	Reset System	Optimal Default, Failsafe Default
	Hold System	
Select action that robot should do.		
Soft or hard reset	Soft	Optimal Default, Failsafe Default
	Hard	
Select reset type robot should send on each boot.		
Retry-Count	3	Optimal Default, Failsafe Default
Sets the maximum number of system resets the Robot will perform before allowing POST to continue.		
At time	After show logo	Optimal Default, Failsafe Default
	Before show logo	
Select when the Robot performs its action: After Show Logo – Executes after the logo is displayed; most system devices are ready. Before Show Logo – Executes before the logo is displayed; some devices may not be ready.		

3.4.8.1.1 Device #1 Detecting Configuration



Options Summary		
Interface	Disabled	Optimal Default, Failsafe Default
	PCI	
	DIO	
	SMBUS	
	Legacy I/O	
	Super I/O	
	MMIO	
Select interface robot should use to communicate with device.		

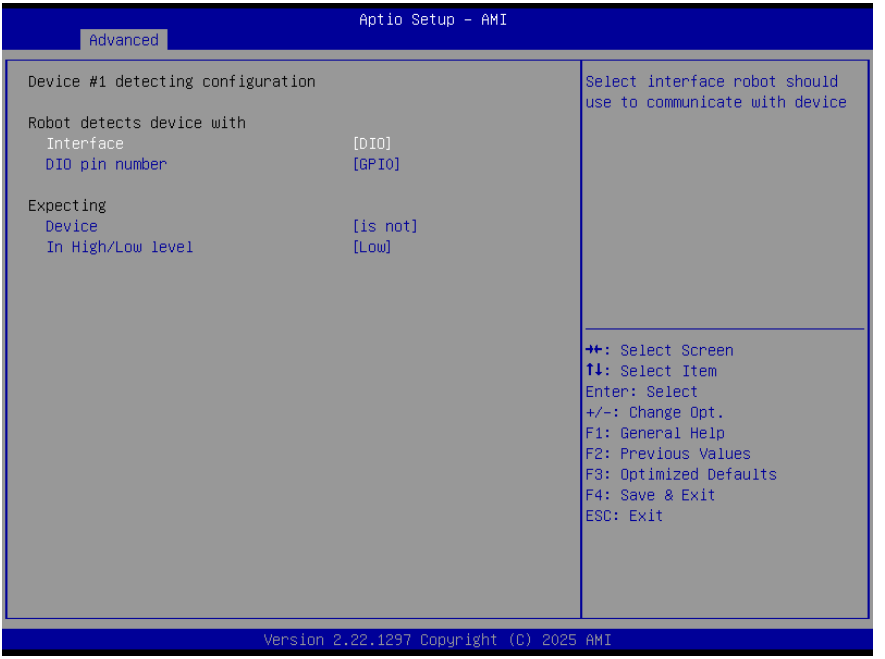
Set to PCI



Options Summary		
When interface item set to "PCI" will show below items		
BUS	0	Optimal Default, Failsafe Default
Enter the bus number of the PCI device in hexadecimal. Range: 0–FF.		
Device	0	Optimal Default, Failsafe Default
Enter the device number of the PCI device in hexadecimal. Range: 0–FF.		
Function	0	Optimal Default, Failsafe Default
Enter the function number of the PCI device in hexadecimal. Range: 0–FF.		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the Robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	

Options Summary
When interface item set to "PCI" will show below items
Select how the Robot verifies a device: Present – Device is detected. According to Register – Robot reads the device register per configuration. Note: A device is considered Present if the data read is not 0xFF.

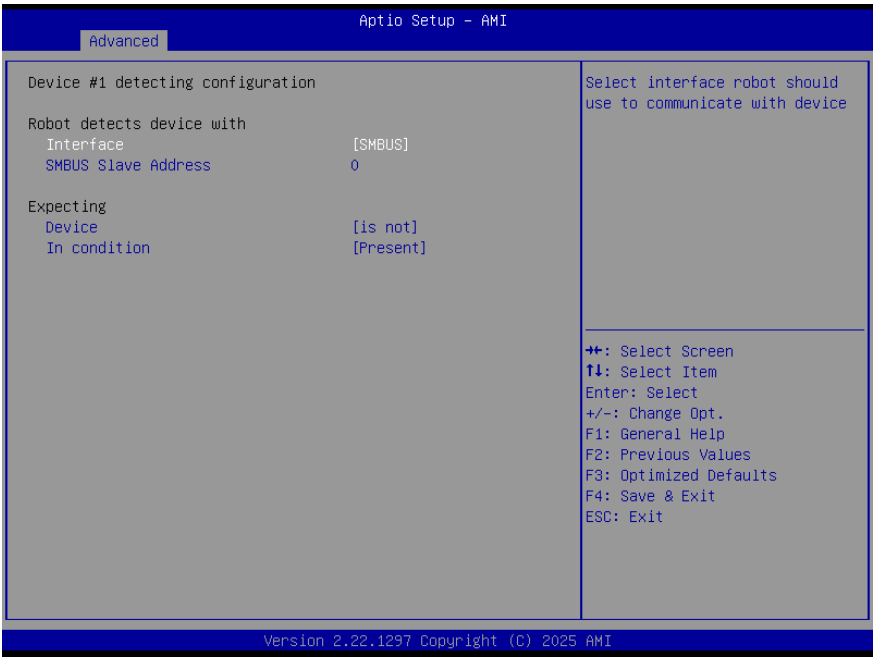
Set to DIO



Options Summary		
When interface item set to "DIO" will show below items		
DIO pin number	GPI 0	Optimal Default, Failsafe Default
	GPI 1	
	GPI 2	
	GPI 3	
	GPO 0	
	GPO 1	
	GPO 2	
	GPO 3	

Options Summary		
When interface item set to "DIO" will show below items		
Assign the DIO pin for Robot actions. For COM Express products: 0-3 → GPI0-3 4-7 → GPO0-3		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the Robot performs the action when the specified condition is met.		
In High/Low level	Low	Optimal Default, Failsafe Default
	High	
Select the signal level (High or Low) of the DIO pin that triggers the Robot action.		

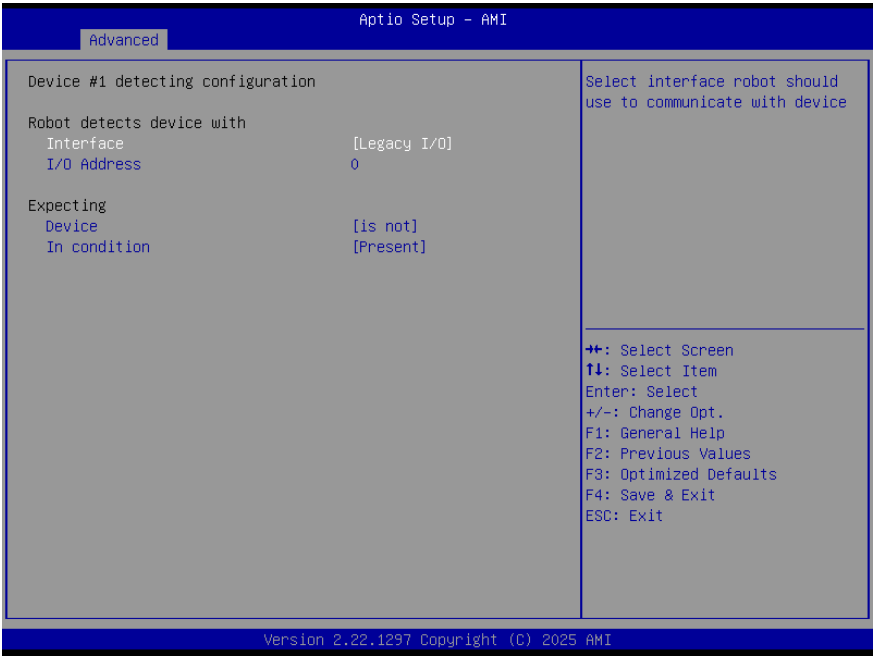
Set to SMBus



Options Summary		
When interface item set to "SMBUS" will show below items		
SMBUS Slave Address	0	Optimal Default, Failsafe Default
Enter the SMBus device's slave address in hexadecimal. Range: 0–FF.		

Options Summary		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the Robot should perform the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select how the Robot verifies a device: Present – Device is detected. According to Register – Robot reads the device register per configuration. *Note:* A device is considered Present if the data read is not 0xFF.		

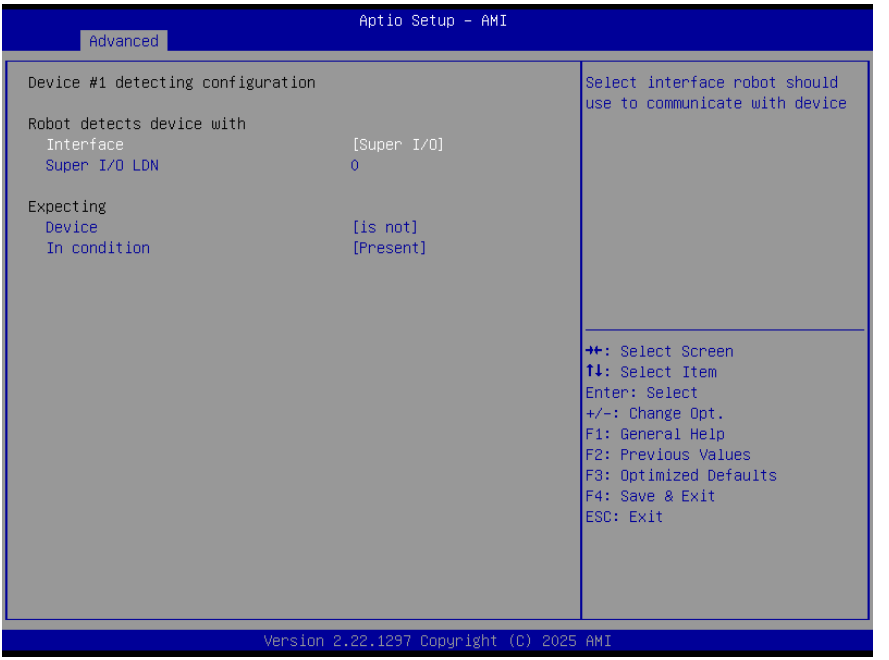
Set to Legacy I/O



Options Summary		
When interface item set to "Legacy I/O" will show below items		
I/O Address	0	Optimal Default, Failsafe Default
Enter the I/O address that the device responds to. Range: 0–FFFF (hexadecimal).		
Device	is	
	Is not	Optimal Default, Failsafe Default

Options Summary		
Select whether the Robot performs the action when the specified condition is met.		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select how the Robot verifies a device: Present – Device is detected. According to Register – Robot reads the device register per configuration. Note: A device is considered Present if the data read is not 0xFF.		

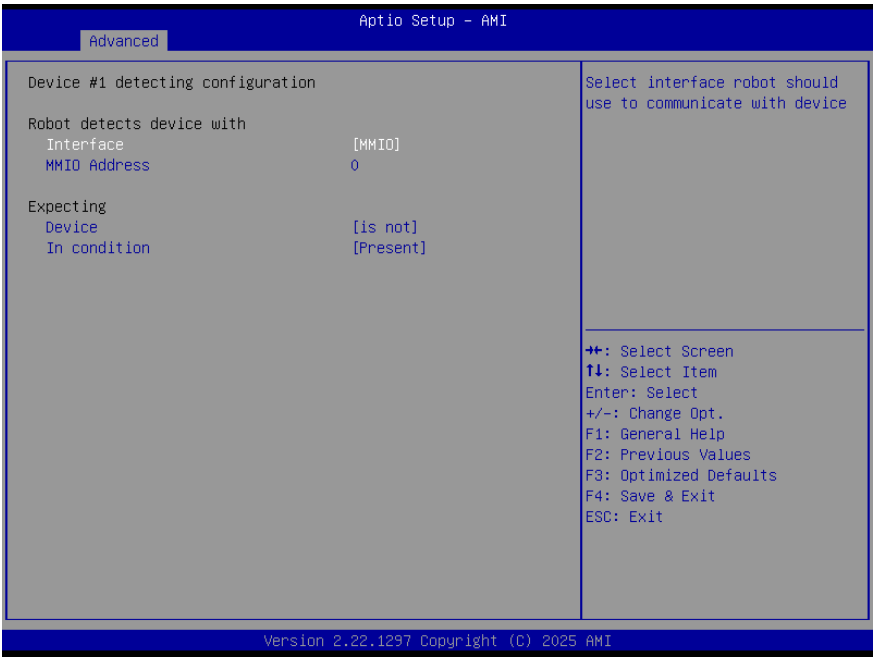
Set to Super I/O



Options Summary		
When interface item set to "Super I/O" will show below items		
Super I/O LDN	0	Optimal Default, Failsafe Default
Enter the Logical Device Number (LDN) of the Super I/O device. Range: 0–FF (hexadecimal).		
Device	Is	
	Is not	Optimal Default, Failsafe Default
Select whether the Robot performs the action when the specified condition is met.		

Options Summary		
When interface item set to "Super I/O" will show below items		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select how the Robot verifies a device: Present – Device is detected. According to Register – Robot reads the device register per configuration. Note: A device is considered Present if the data read is not 0xFF.		

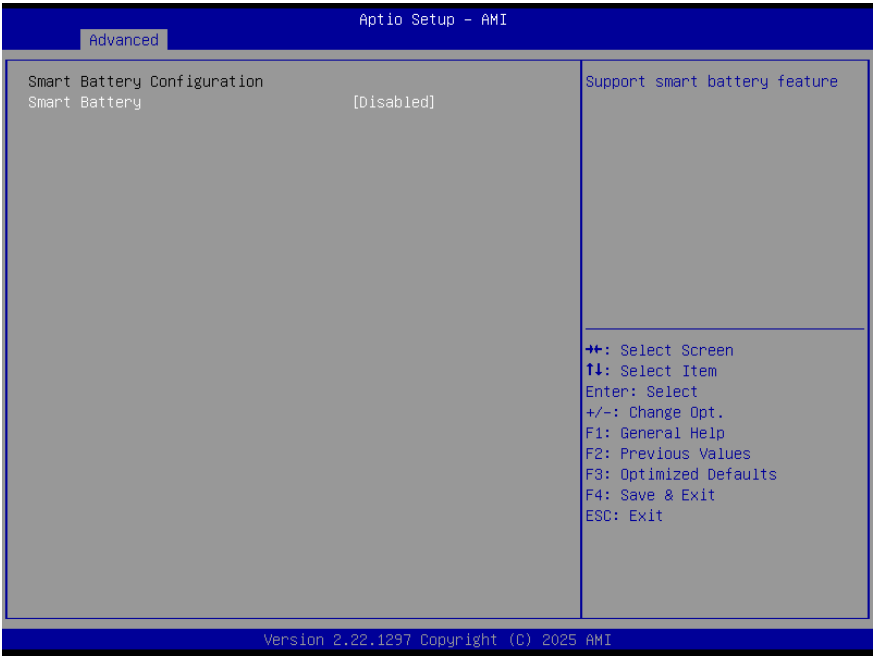
Set to MMIO



Options Summary		
When interface item set to "MMIO" will show below items		
MMIO Address	0	Optimal Default, Failsafe Default
Enter the Memory-Mapped I/O address that the device responds to. Range: 0–FFFFFFFF (hexadecimal).		
Device	is	
	Is not	Optimal Default, Failsafe Default
Select whether the Robot performs the action when the specified condition is met.		

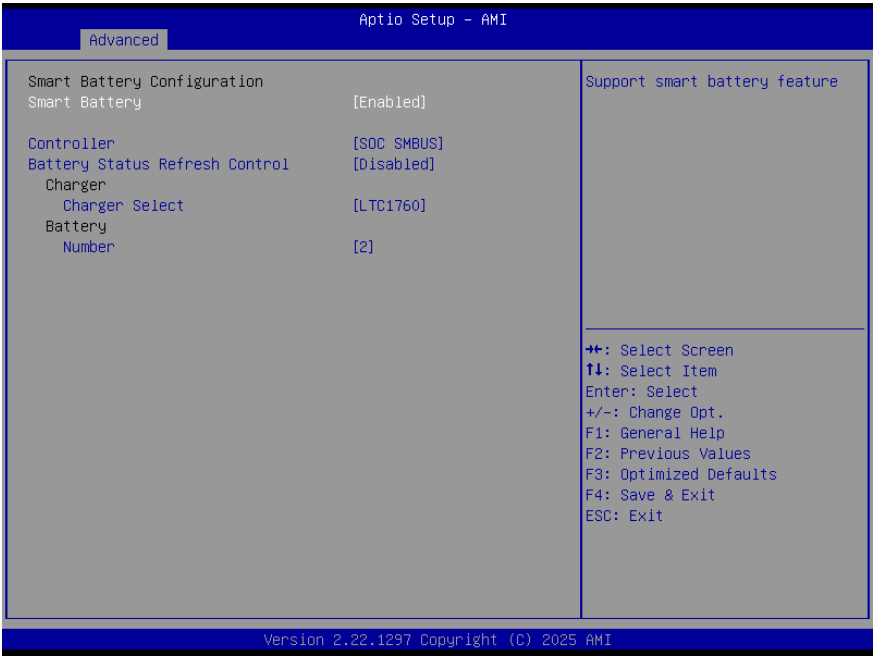
Options Summary		
When interface item set to "MMIO" will show below items		
In condition	Present	Optimal Default, Failsafe Default
	Specified register data	
Select how the Robot verifies a device: Present – Device is detected. According to Register – Robot reads the device register per configuration. Note: A device is considered Present if the data read is not 0xFF.		

3.4.9 Smart Battery Configuration



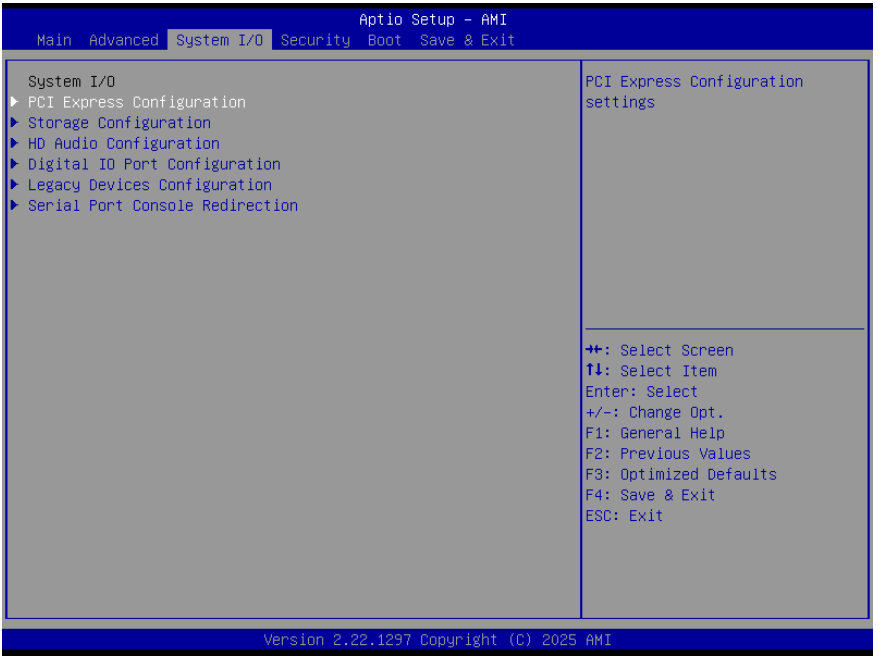
Options Summary		
When interface item set to "Disable" will show below items		
Smart Battery	Disabled	Optimal Default, Failsafe Default
	Enabled	
Support smart battery feature		

Set to Enabled

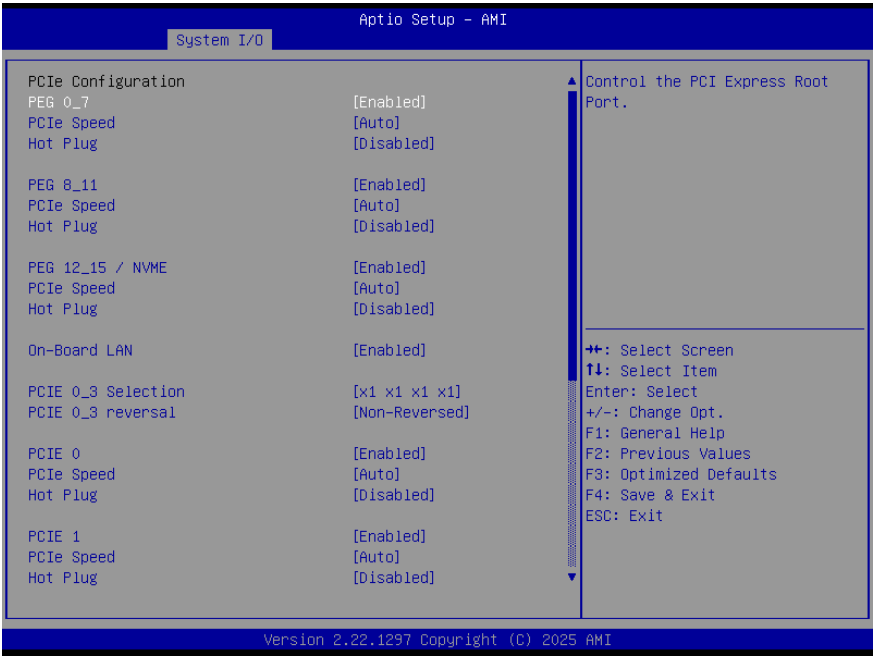


Options Summary		
When interface item set to "Enabled" will show below items		
Controller	SOC SMBUS	Optimal Default, Failsafe Default
	EC I2C	
Select which controller the Robot should use: SOC SMBUS – Uses SMB_CLK and SMB_DAT (pins B13, B14) EC I^2C – Uses I2C_CK and I2C_DAT (pins B33, B34)		
Battery Status Refresh Control	Disabled	Optimal Default, Failsafe Default
	SMBALERT#	
Select the source used to actively refresh battery status in Windows.		
Charger Select	LTC1706	Optimal Default, Failsafe Default
Select Charger support		
Number	0	
	1	
	2	Optimal Default, Failsafe Default
Select maximum number of devices supported		

3.5 Setup Submenu: System I/O



3.5.1 PCI Express Configuration



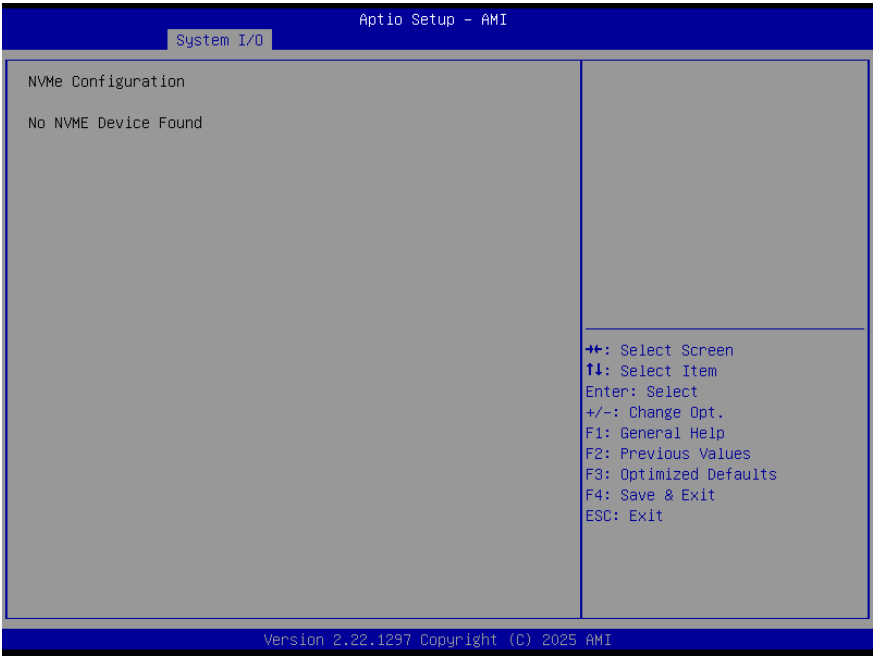
Options Summary		
PEG 0_7	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
	Gen4	
	Gen5	
Configure PCIe Speed.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable.		
PEG 8_11	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		

Options Summary		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
	Gen4	
Configure PCIe Speed.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable.		
PEG12_15 / NVME	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
	Gen4	
Configure PCIe Speed.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable.		
On-Board LAN	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe 0_3 Selection	x1 x1 x1 x1	Optimal Default, Failsafe Default
	X2 x1 x1	
	x2 x2	
	x4	
PCIE Controller Setting		
PCIe 0_3 reversal	Non-Reversed	Optimal Default, Failsafe Default
	Reversed	
PCIE LANE REVERSAL		
PCIE 0~3	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed (PCIE 0~3)	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	

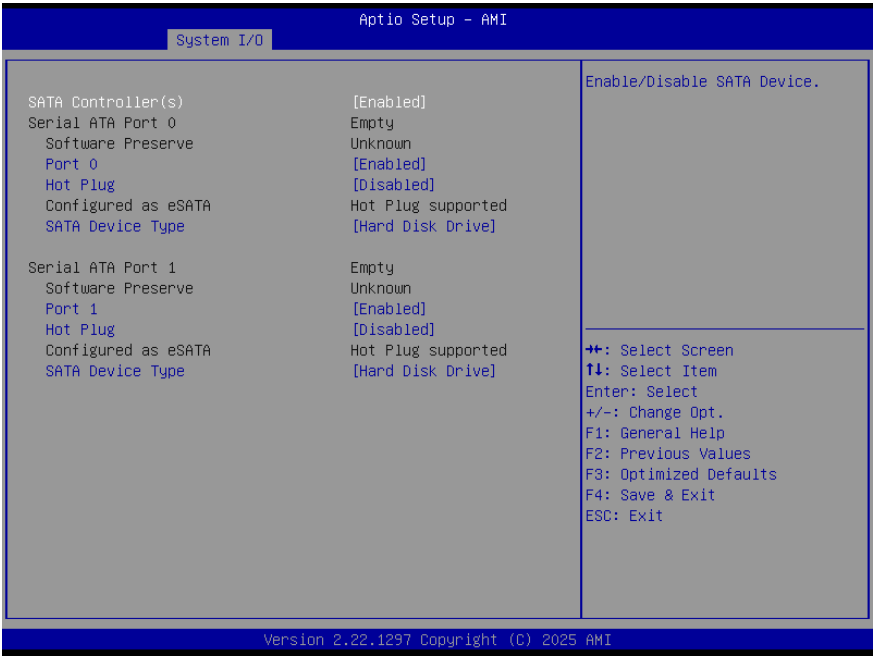
Options Summary		
Configure PCIe Speed.		
Hot Plug (PCIE 0~3)	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable.		
PCIE 4_7 reversal	Non-Reversed	Optimal Default, Failsafe Default
	Reversed	
PCIE LANE REVERSAL		
PCIE 4	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
PCI Express Hot Plug Enable/Disable.		

3.5.2 Storage Configuration

3.5.2.1 NVMe Configuration

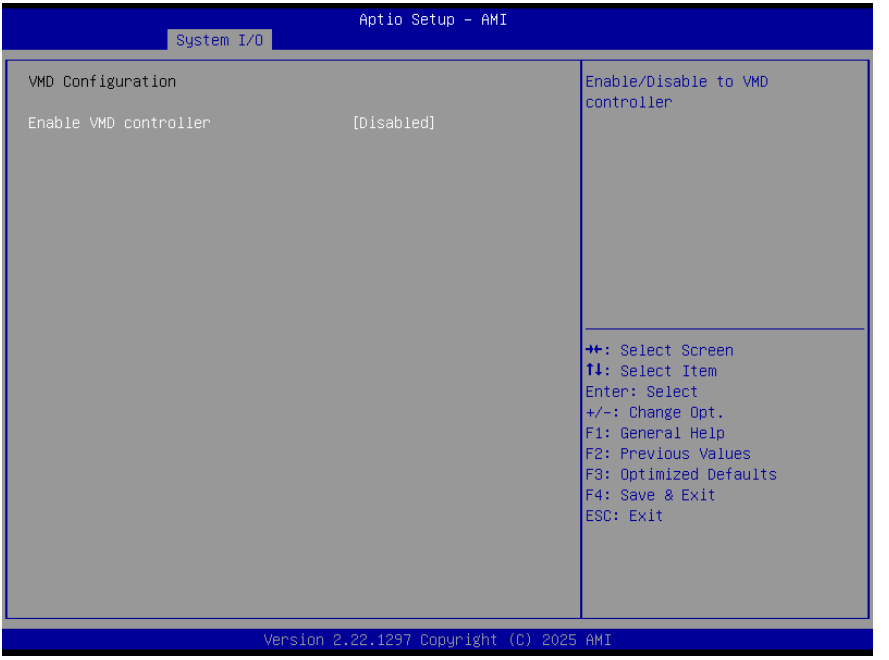


3.5.2.2 SATA Configuration

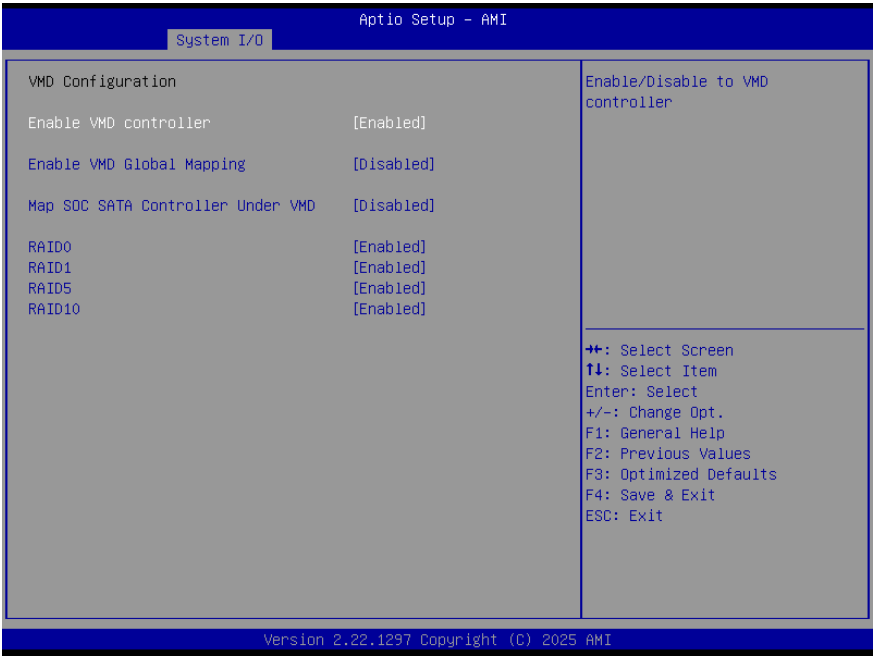


Options Summary		
SATA Controller(s)	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable SATA Device.		
Port 0~1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
Hot Plug	Disabled	Optimal Default, Failsafe Default
	Enabled	
Designates this port as Hot Pluggable.		
SATA Device Type	Hard Disk Drive	Optimal Default, Failsafe Default
	Solid State Drive	
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.		

3.5.2.3 VMD Setup Menu

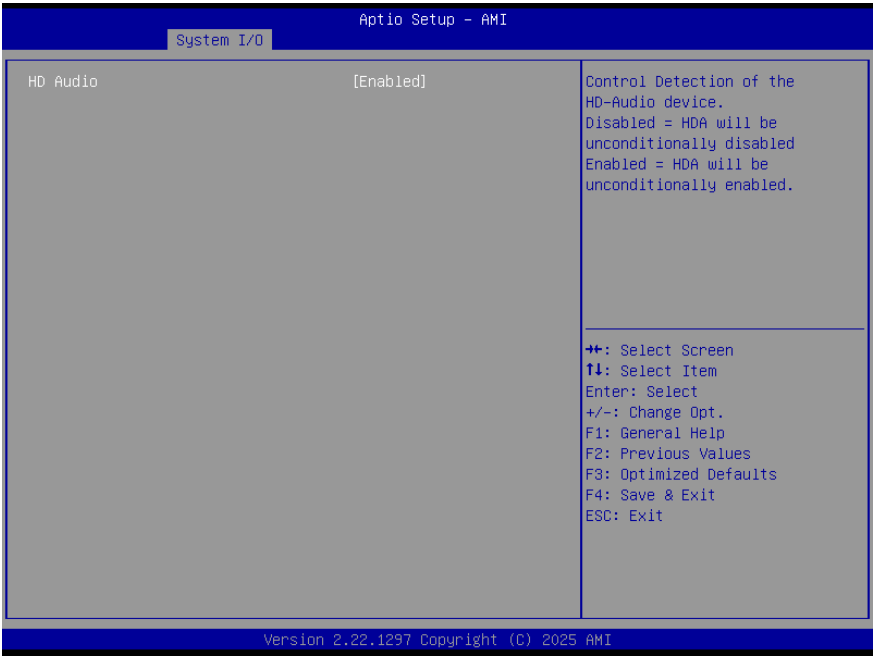


Options Summary		
Enable VMD controller	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable VMD controller		



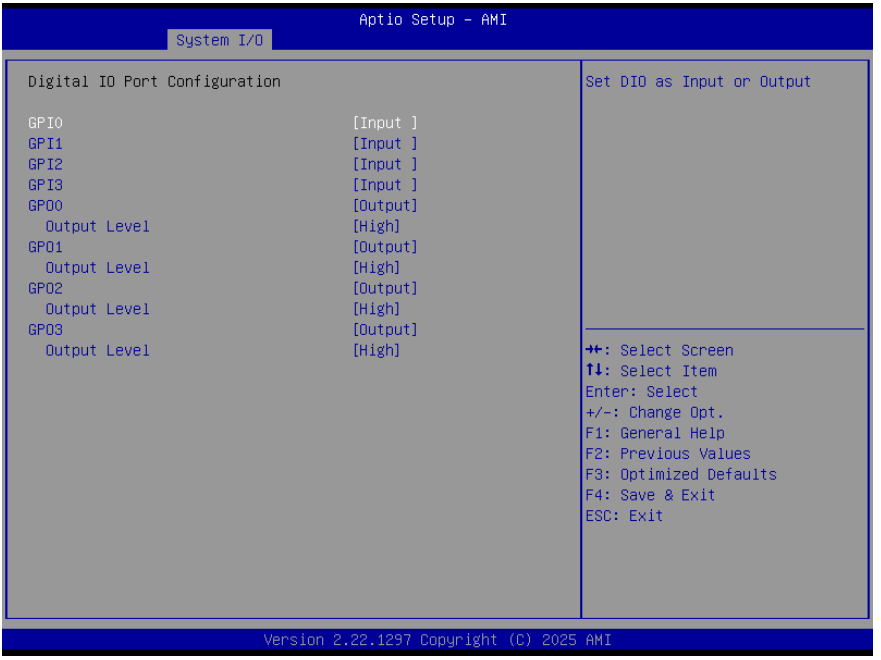
Options Summary		
Enable VMD Global Mapping	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable to Global Mapping.		
Map SOC SATA Controller Under VMD	Disabled	Optimal Default, Failsafe Default
	Enabled	
Map/UnMap this Root Port to VMD.		
RAID0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable RAID0 support.		
RAID1	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable RAID1 support.		
RAID5	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable RAID5 support.		
RAID10	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable RAID10 support.		

3.5.3 HD Audio Configuration



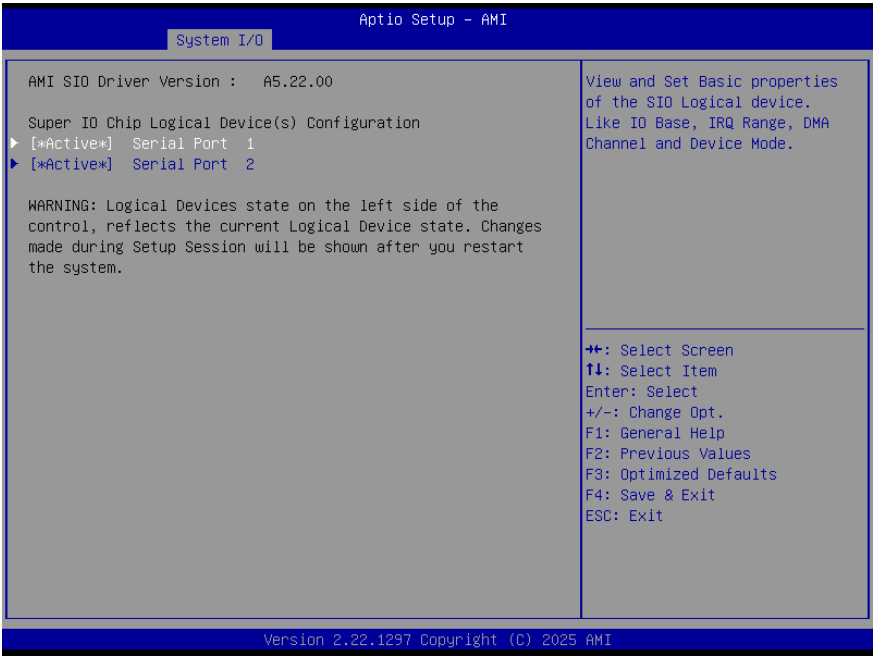
Options Summary		
HD Audio	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable detection of the HD-Audio device. Disabled – HDA is unconditionally disabled. Enabled – HDA is unconditionally enabled.		

3.5.4 Digital IO Port Configuration

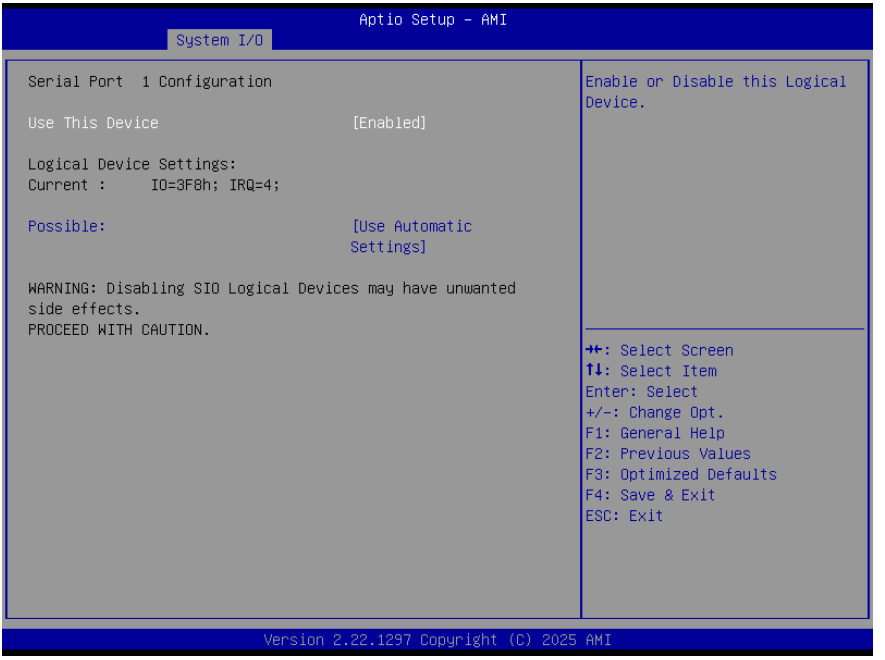


Options Summary		
GPI 0~3	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input or Output.		
GPO 0~3	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input or Output.		
Output Level	High	Optimal Default, Failsafe Default
	Low	
Set output level when DIO pin is output.		

3.5.5 Legacy Logical Devices Configuration

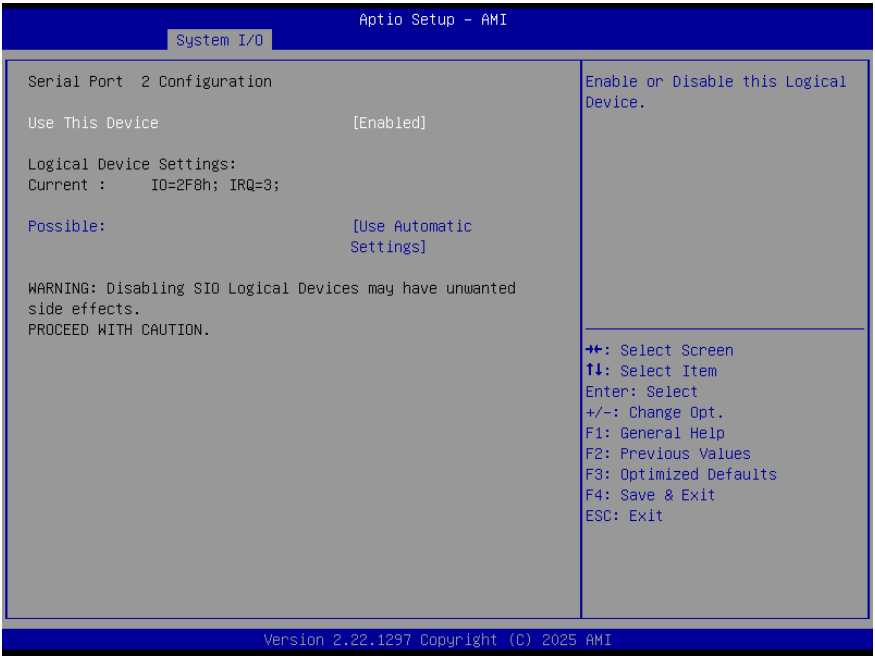


3.5.5.1 Serial Port 1 Configuration



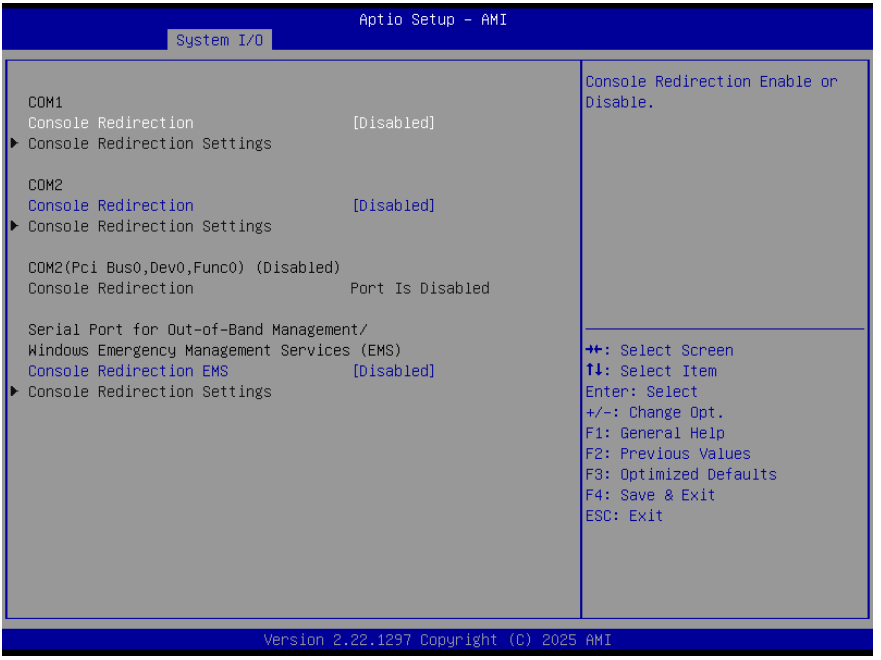
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4; DMA;	
	IO=2C8h; IRQ=11; DMA;	
Allows the user to change device resource settings. New settings take effect and appear on this setup page after a system restart.		

3.5.5.2 Serial Port 2 Configuration



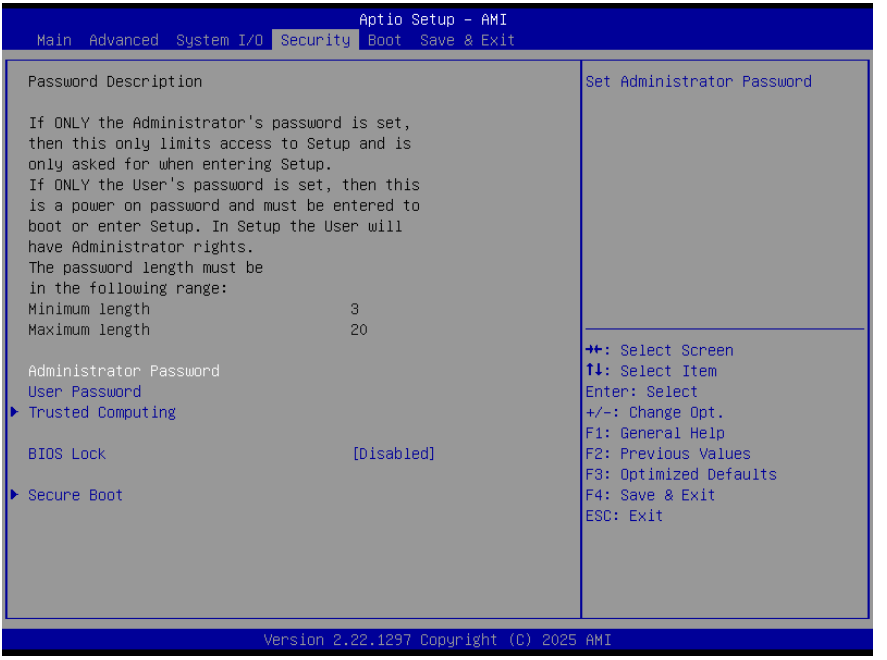
Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8h; IRQ=3; DMA;	
	IO=2D8h; IRQ=10; DMA;	
Allows the user to change device resource settings. New settings take effect and appear on this setup page after a system restart.		

3.5.6 Serial Port Console Redirection



Options Summary		
Console Redirection (COM1)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection (COM2)	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		
Console Redirection EMS	Disabled	Optimal Default, Failsafe Default
	Enabled	
Console Redirection Enable or Disable.		

3.6 Setup Submenu: Security



Change Administrator/User Password

You can set an Administrator password. If you set an Administrator password, you can then set a User password. User passwords do not have access to many of the features in the Setup utility.

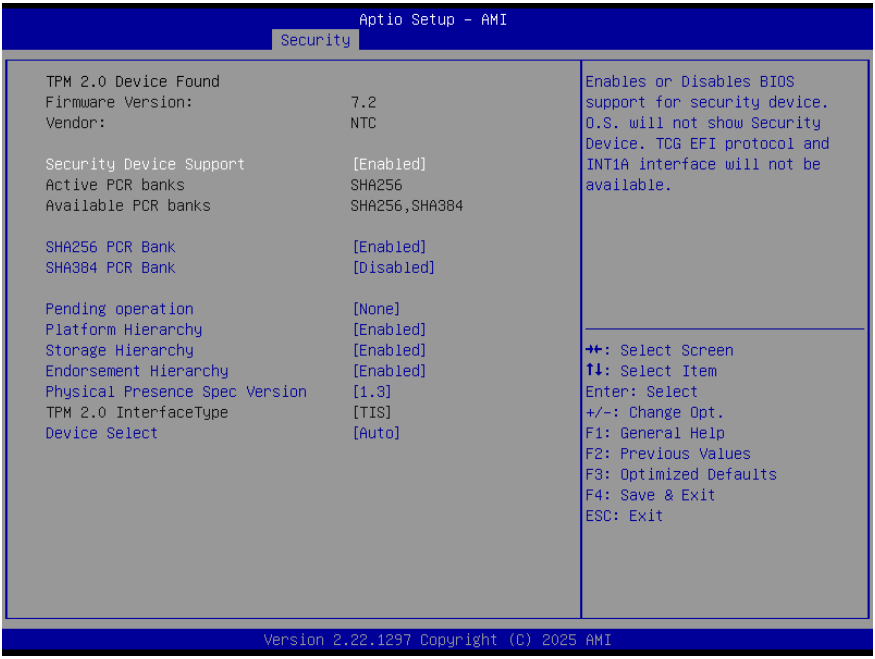
Select the password you want to set and press <Enter>. A dialog box will appear which lets you set the password. Passwords must be between 3 and 20 letters or numbers. Press <Enter> and re-enter the password into the next dialog box that appears. Press <Enter> after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Remove Password

Highlight this item and type in the current password. At the next dialog box press <Enter> to disable password protection.

Options Summary		
BIOS Lock	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or disable the PCH BIOS Lock feature. Must be enabled to ensure SMM flash protection.		

3.6.1 Trusted Computing



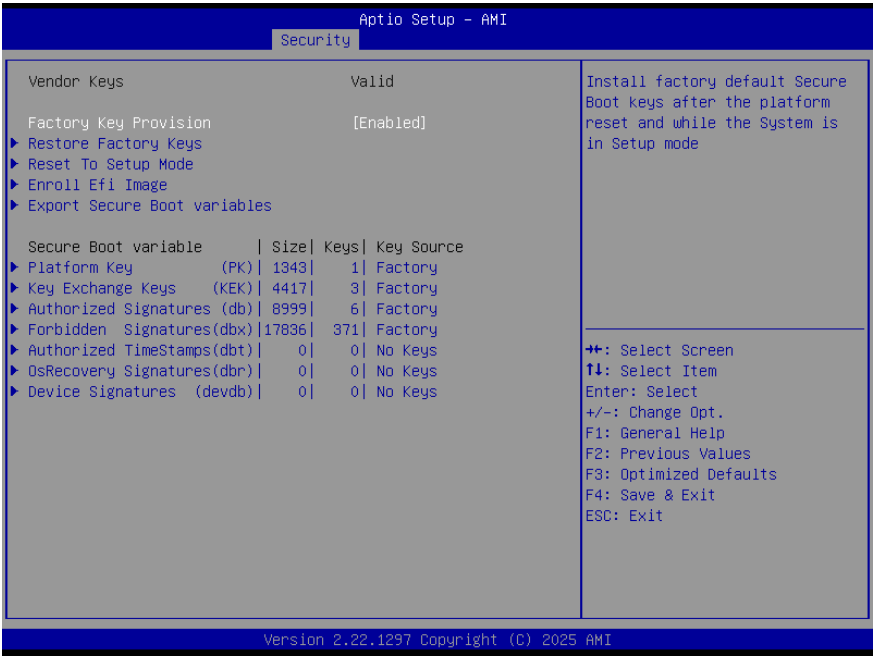
Options Summary		
Security Device Support	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable BIOS support for the security device.		

Options Summary		
Disabled – The OS will not detect the Security Device, and TCG EFI protocol and INT1A interface will be unavailable. Enabled – BIOS supports the Security Device.		
SHA256 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank.		
SHA384 PCR Bank	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable SHA384 PCR Bank.		
Pending Operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. **NOTE**: Your Computer will reboot during restart in order to change State of Security Device.		
Platform Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or disable Platform Hierarchy.		
Storage Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy.		
Endorsement Hierarchy	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy.		
Physical Presence Spec Version	1.2	
	1.3	Optimal Default, Failsafe Default
Select the PPI version the OS should support: 1.2 or 1.3. *Note:* Some HCK tests may not support version 1.3.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
Select the TPM version for system support: TPM 1.2 – Supports only TPM 1.2 devices. TPM 2.0 – Supports only TPM 2.0 devices. Auto – Supports both TPM 2.0 and TPM 1.2 devices; defaults to TPM 2.0 if available, otherwise enumerates TPM 1.2.		

3.6.2 Secure Boot

Options Summary		
Secure Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Secure Boot is active when Secure Boot is enabled, the Platform Key (PK) is enrolled, and the system is in User mode. Changing mode requires a platform reset.		
Secure Boot Mode	Custom	Optimal Default, Failsafe Default
	Standard	
Select the Secure Boot mode: Standard – Uses default Secure Boot policy. Custom – Allows a physically present user to configure Secure Boot Policy variables without full authentication.		
Restore Factory Keys		
Force System to User Mode. Install factory default Secure Boot key databases.		

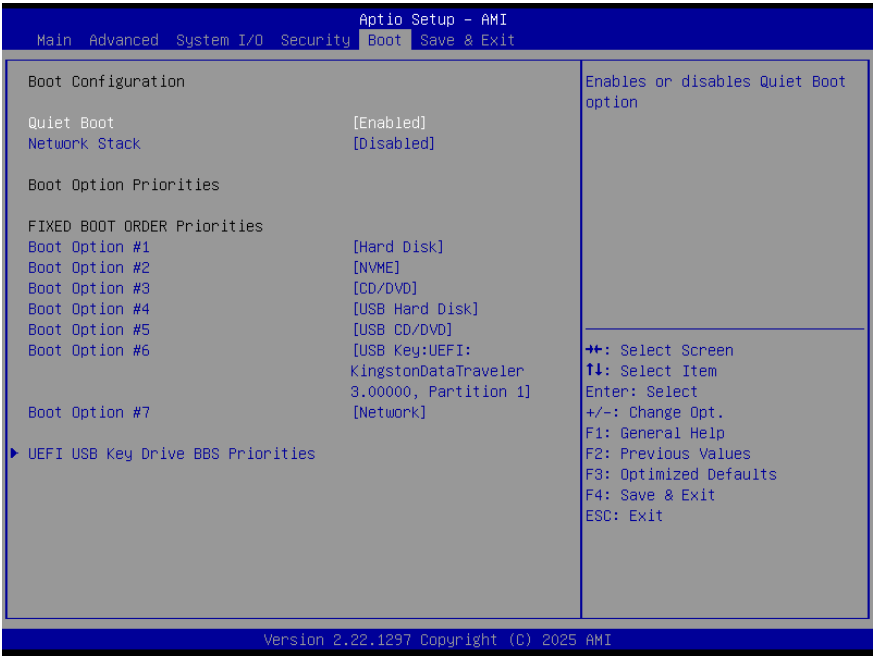
3.6.2.1 Key Management



Options Summary		
Factory Key Provision	Disabled	Optimal Default, Failsafe Default
	Enabled	
Installs the factory default Secure Boot keys after a platform reset while the system is in Setup mode.		
Restore Factory Keys		
Switches the system to User Mode and installs the factory default Secure Boot key databases.		
Reset to Setup Mode		
Deletes all Secure Boot key databases from NVRAM, placing the system in Setup Mode.		
Export Secure Boot variables		
Saves the contents of Secure Boot variables from NVRAM to a file.		
Enroll Efi Image		
Allows a PE image to run in Secure Boot mode by enrolling its SHA256 hash certificate into the Authorized Signature Database (db).		
Platform Key (PK)		Details
		Export

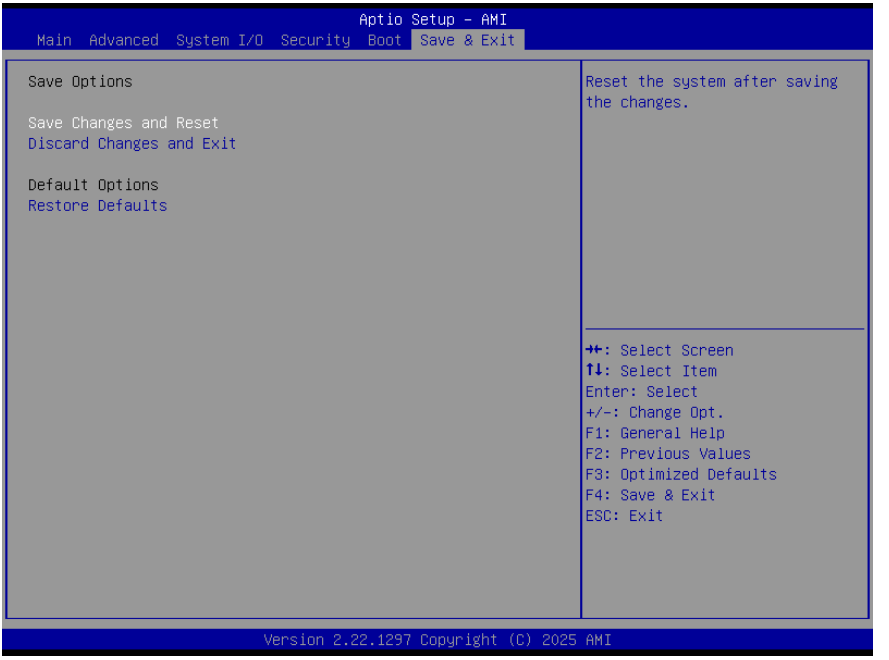
Options Summary	
Platform Key (PK)	Update
	Delete
Key Exchange Keys (KEK)	Details
	Export
	Update
	Append
	Delete
Authorized Signatures (db)	Details
	Export
	Update
	Append
	Delete
Forbidden Signatures (dbx)	Details
	Export
	Update
	Append
	Delete
Authorized TimeStamps (dbt)	Update
	Append
OsRecovery Signatures (dbr)	Update
	Append
Enroll Factory Defaults or load certificates from a file: Public Key Certificate: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXXX Authenticated UEFI Variable EFI PE/COFF Image (SHA256) Key Source: Factory, Modified, Mixed.	

3.7 Setup Submenu: Boot



Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables Quite Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		

3.8 Setup Submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the COM-ARHC6 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/product/detail/computing_on_module_com-arhc6/download

Download the driver(s) you need and follow the steps below to install them.

Chipset Driver

1. Open the **Chipset Driver**folder
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Graphics Driver

1. Open the **Graphics Driver** folder
2. Run the **Installer.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

LAN Drivers

1. Open the **LAN Drivers** folder
2. Read the readme file before proceeding. Caution: Some drivers may require firmware updates first.
3. Identify the subfolder that matches your hardware: choose one of **PRO40GB, PRO1000, PRO2500, PROAVF, PROCGB, PROXGB, RDMA**.
4. Open the appropriate folder for your device, then locate the **e2f.sys** file (system driver) and **e2fmsg.dll** file (supporting library)
5. Run the setup program if provided, or manually install the .sys file using Device Manager → Update driver → Browse my computer for drivers.
6. Follow the on-screen instructions; the driver will be installed automatically.

ME Driver

1. Open the **ME & TXE Drivers** folder
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

Serial I/O Drivers

1. Open the **Serial I/O Driver**folder
2. Identify the drivers you need based on your system hardware:
   - **iaLPSS2_GPIO2_MTL**
   - **iaLPSS2_I2C_MTL**
   - **iaLPSS2_13C_MTL**
   - **iaLPSS2_SPI_MTL**
   - **iaLPSS2_UART2_MTL**
3. Open the folder for the driver you want to install.
4. Run the corresponding setup file (e.g., **iaLPSS2_GPIO2_MTL.sys** or **setup.exe** if provided), then follow the on-screen instructions; the driver will be installed automatically.
5. Repeat steps 4–6 for each additional driver required by your system.
6. After all drivers are installed, restart to complete the installation.

Intel® NPU Drivers

1. Open the **Peripheral Drivers** folder, then select the **Intel-npudriver-32.0.100.3159.zip** file.
2. Identify the drivers you need based on your system hardware:
   - **npu_driver_compiler.dll**
   - **npu_extension.dll**
   - **npu_level_zero_umd.dll**
   - **tbb12.dll**
   - **tbbmalloc.dll**
   - **ze_loader.dll**
   - **ze_tracing_layer.dll**
   - **ze_validation_layer.dll**
3. Run the setup program if provided, or manually install the **.sys** and **.dll** files.
4. Follow the on-screen instructions; drivers and supporting libraries will be installed automatically.

Intel® Platform Monitoring Technology Driver

1. Open the **Peripheral Drivers** folder, then select the **Intel Platform Monitoring Technology-3.1.2.6.zip** file.
2. Locate the **IntcPMT.sys** file.
3. Run the setup program if provided, or manually install the **.sys** file.
4. Follow the on-screen instructions; the driver will be installed automatically.

Install Audio Drivers

Note: Ensure Intel Audio Driver (**Intel(R)_SST_MTL_ARL_v20.40.11988.4_HF.zip**) is installed before the Realtek Audio driver (**Realtek Audio 6.0.9034.2**)

Intel SST Driver

1. Open the **Audio** folder
2. Unzip the **Intel(R)_SST_MTL_ARL_v20.40.11988.4_HF.zip** subfolder
3. Open the **Production** folder followed by the **Drivers** folder.
4. Install **IntcAudioBus.inf** and **IntcOED.inf**

Note: Make sure to install **IntcAudioBus.inf** before installing **IntcOED.inf**.

5. Installation steps using Device Manager:
   - Press **Windows + X** and select **Device Manager**.
   - Locate the device under **System devices** or **Other devices** (may appear as *Unknown device* or *Audio DSP*).
   - Right-click the device → **Update driver**.
   - Select **Browse my computer for drivers**.
   - Navigate to the folder containing **IntcAudioBus.inf**, then click **Next** to install.
   - Repeat the process for **IntcOED.inf**.
6. Verify installation by confirming the Intel® Ethernet adapter appears under **Network adapters** with no warning icons.

Realtek Audio Driver

1. Open the folder where you unzipped the **Audio Drivers**
2. Run the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

Install Linux Peripheral Drivers

1. Open the **Linux Driver-Peripheral** folder.
2. Follow the instructions provided in the **aaeon_wmi_all_V2.7.0.2.zip**. If you have any questions about the supported functions, please contact your regional FAE for more details.

RAID Driver

1. Open the folder where you unzipped the **RAID Driver**
2. Run the **SetupRST.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically
5. Refer to the ReadMe.txt for any assistance.

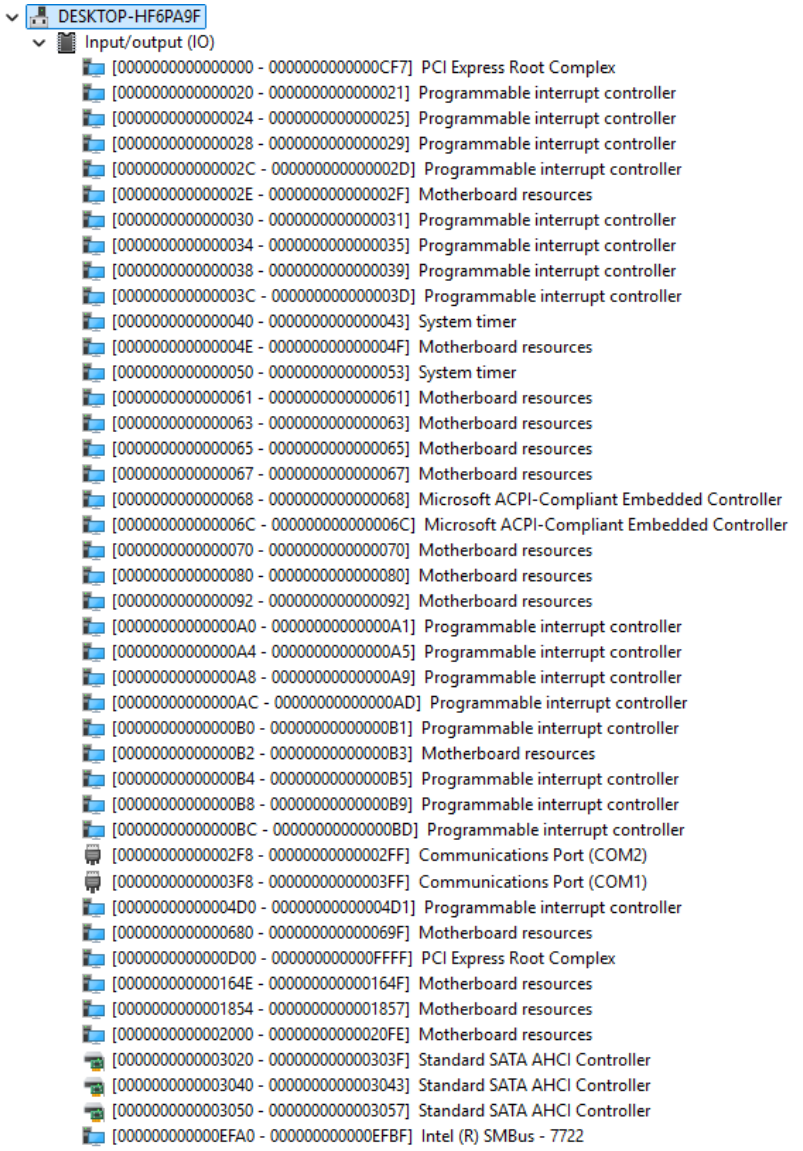
Install Camera Drivers

1. Open the folder where you unzipped the **Camera Drivers**
2. Install core camera drivers first by opening their folders and running the setup programs:
   - **iacamera64.sys** → run setup if provided
   - **Im3643.sys** → run setup if provided
   - **ov01a1s.sys** → run setup if provided
   - **ov13b10.sys** → run setup if provided
3. Install supporting camera libraries and extensions:
   - **iacamera64_extension**
   - **iasp64.sys**
   - **iaisp64.sys**
   - **iaisptrustlet64.dll**
   - **ic2_api.dll**
   - **IntelDeviceMFT64.dll**
   - **intelic.dll**
   - **libia_cp64.dll**
   - **pvl_perspective_control64.dll**
   - **pvl_skin_smoothing64.dll**
   - **pvl64.dll**
   - **tbb12.dll**
   - **XeExpVEX.dll**
4. Install graph descriptors, settings, and AIQB/CPF files:
   - **cpd_component_signed.bin**
   - **cpd_component_signed_arl.bin**
   - **graph_descriptor**
   - **graph_settings_. aiqb /. cpf** for your specific camera model (e.g., **OV13B10_09B13, OV13B10_09B13U, OV01A1S_YHRN**)
5. Follow the on-screen instructions; drivers and supporting files will be installed automatically.:

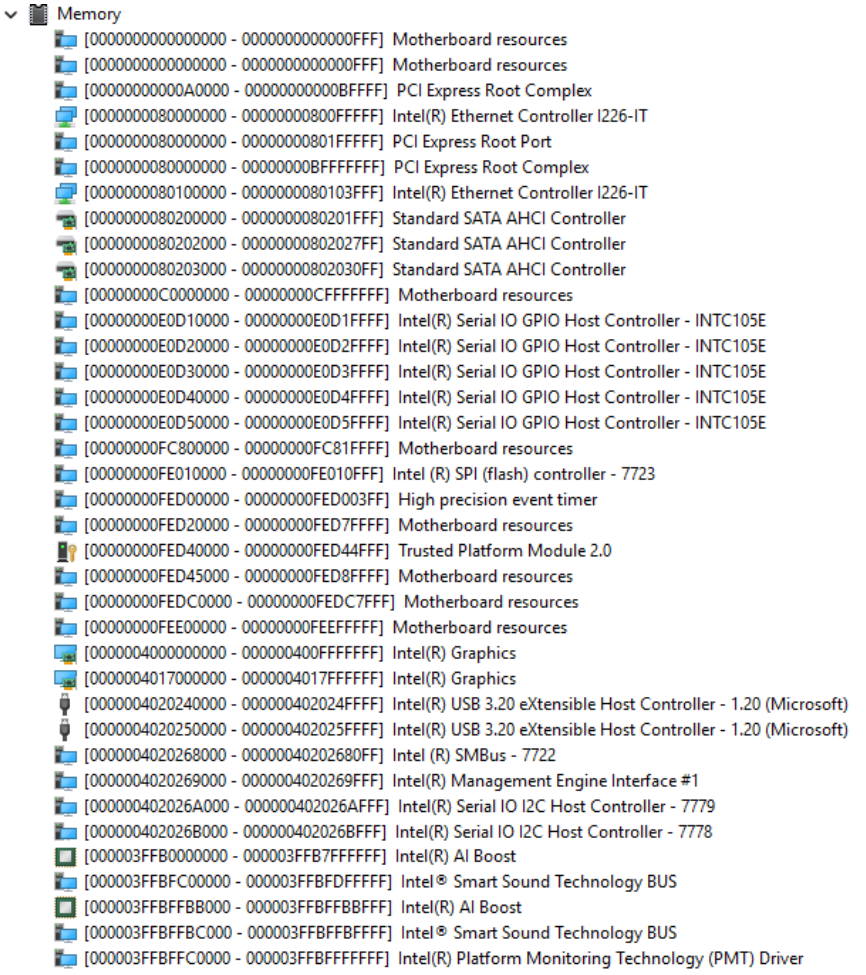
Appendix A

I/O Information

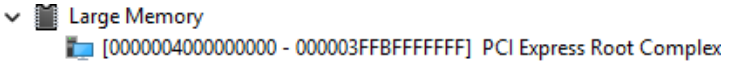
A.1 I/O Address Map



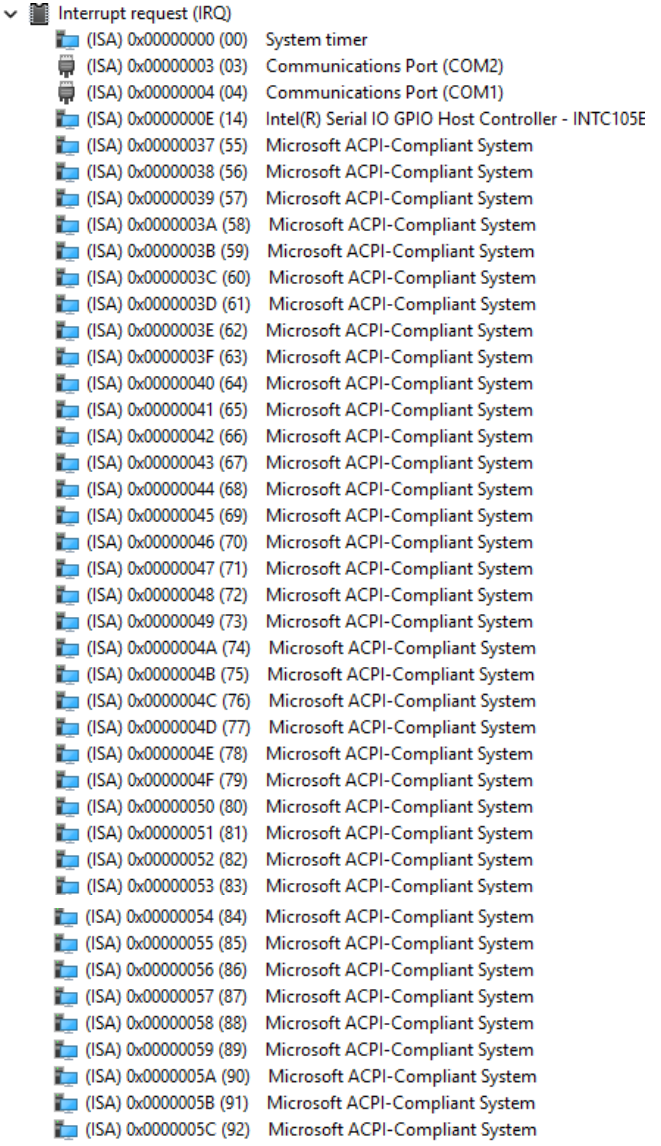
A.2 Memory Address Map



A.3 Large Memory Address Map



A.4 IRQ Mapping Chart



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(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000020 (32) Intel(R) Serial IO I2C Host Controller - 7778
(PCI) 0x00000021 (33) Intel(R) Serial IO I2C Host Controller - 7779
(PCI) 0xFFFFFFF2 (-14) Intel® Smart Sound Technology BUS
(PCI) 0xFFFFFFF3 (-13) Intel(R) AI Boost
(PCI) 0xFFFFFFF4 (-12) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFF5 (-11) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFF6 (-10) Intel(R) Graphics
(PCI) 0xFFFFFFF7 (-9) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFF8 (-8) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFF9 (-7) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFFA (-6) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFFB (-5) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFFC (-4) Intel(R) Ethernet Controller I226-IT
(PCI) 0xFFFFFFFD (-3) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFE (-2) PCI Express Root Port