COM-APLC6

COM Express Module

User's Manual 1st Ed

Last Updated: April 18, 2018

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● COM-APLC6	1
● M2.5 screws	4
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any AC supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur.
Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	O	O	O	O	O	O
外部信号连接器及线材	O	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System

Form Factor	COM Express, Compact, Pin-out Type 6
CPU	Onboard Intel® Atom™ SoC
CPU Frequency	Intel® Atom™ E39xx
Chipset	Intel® Atom™ SoC
Memory Type	DDR3L1867, SODIMM x 2, ECC only
Max Memory Capacity	8 GB
BIOS	AMI BIOS
Wake On LAN	Yes
Watchdog Timer	255 Levels
Power Requirement	Nominal: +12V
Power Supply Type	AT/ATX
Power Consumption (Typical)	E3950 TDP: 12W
Dimensions (L x W)	3.74" x 3.74" (95mm x 95mm)
Operating Temperature	32°F ~ 140°F (0°C ~ 60°C)
Storage Temperature	-40°F ~ 176°F (-40°C ~ 80°C)
Operation Humidity	0% ~ 90% relative humidity, non-condensing
MTBF	—
Certification	CE/FCC

Display

VGA/LCD Controller	Intel® Atom™ SoC Integrated
Video Output	CRT, LVDS/(eDP), DDI

I/O

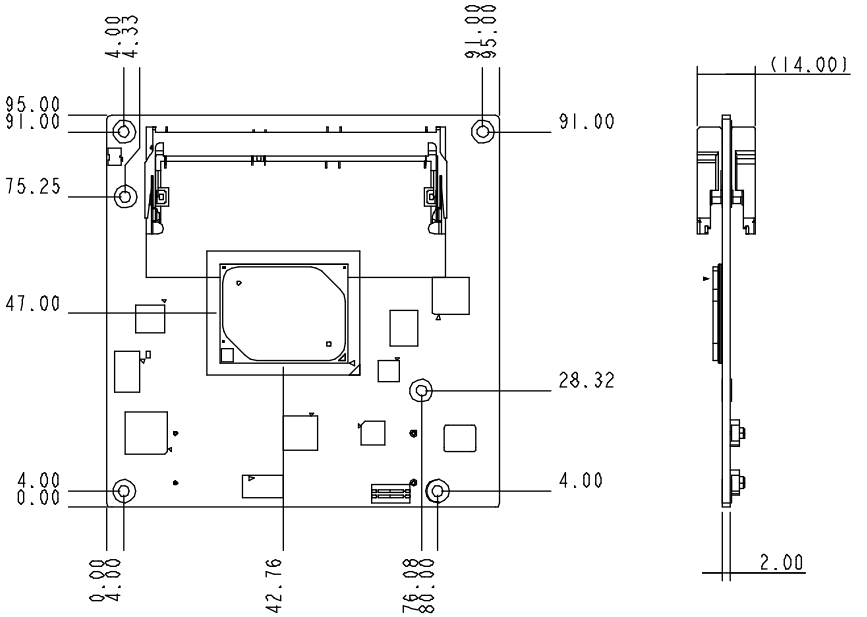
Ethernet	Intel® i210, Gigabit Ethernet
Audio	High Definition Audio Interface
USB	USB 2.0 x 8, USB 3.0 x 2
Serial Port	Tx/Rx x 2
HDD Interface	SATA x 2
Onboard SSD	—
Expansion Slot	PCI-Express[x1] x 3 (devices) LPC Bus x 1, SMbus x 1, I2C x 1
DI/O	GPIO 8-bit
TPM	—

Chapter 2

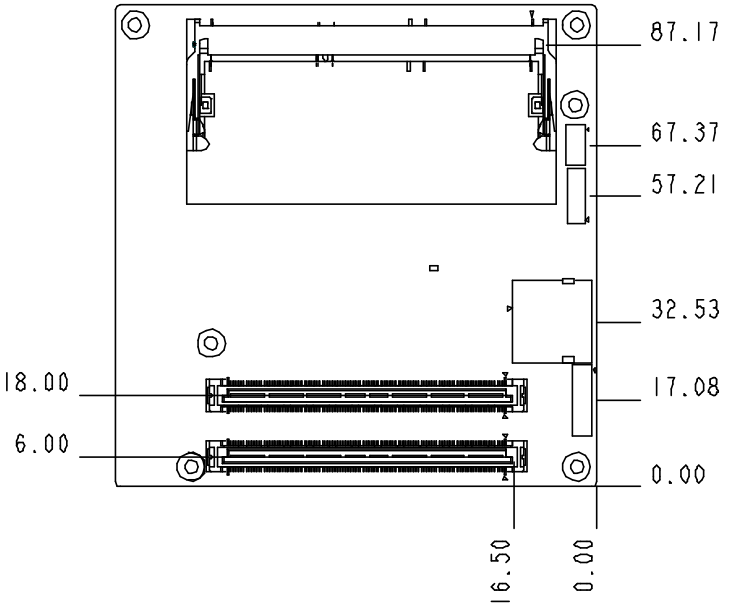
Hardware Information

2.1 Dimensions

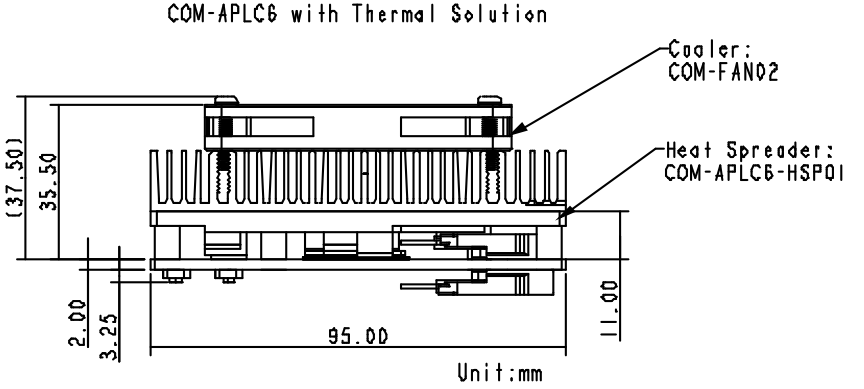
Component Side



Solder Side

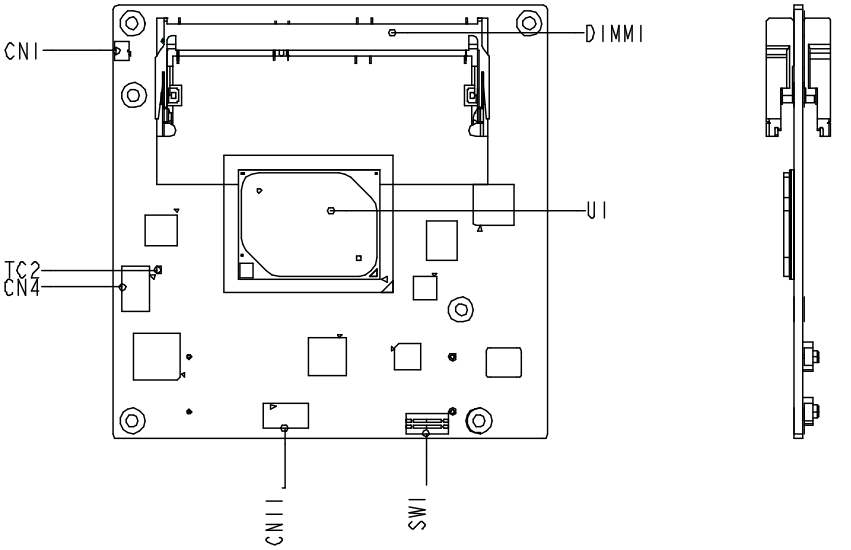


With Heat spreader

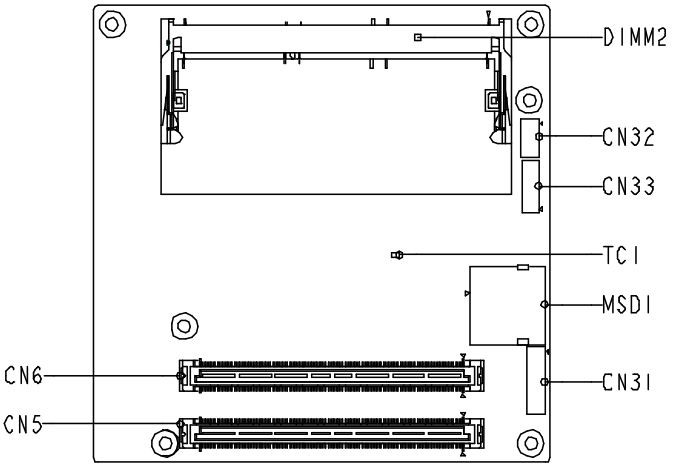


2.2 Jumpers and Connectors

Component Side



Solder Side



2.3 List of Connectors

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
SW1	AT/ATX switch & DDI/VGA switch
DIMM1	DDR3L ECC Socket
DIMM2	DDR3L ECC Socke1
CN1	RTC Connector
CN4	SPI ROM FLASH
CN5	ROW A/B
CN6	ROW C/D

2.3.1 AT/ATX switch & DDI/VGA switch (SW1)

	ON	OFF
1	AT Mode	ATX Mode
2	VGA	DDI

2.3.2 RTC Connector (CN1)

Pin	Signal	Pin	Signal
1	Battery Power	2	GND

2.3.3 SPI ROM FLASH (CN4)

Pin	Signal	Pin	Signal
1	SPI_SO_F	5	SPI_SI_F
2	GND	6	SPI_CE0#_F
3	SPI_CLK_F	7	NC
4	3.3V		

2.3.4 ROW A/B Connector (CN5)

Row A		Row B	
Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK	B8	N.C
A9	GBE0_MDI1-	B9	N.C
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#

A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	N.C	B22	N.C
A23	N.C	B23	N.C
A24	SUS_S5#	B24	PWR_OK
A25	N.C	B25	N.C
A26	N.C	B26	N.C
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	N.C
A29	AC_SYNC	B29	AC_SDIN1
A30	AC_RST#	B30	AC_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR
A33	AC_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	N.C
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-

A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	N.C	B52	N.C
A53	N.C	B53	N.C
A54	GPI0	B54	GPO1
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-

A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+ (EDP_TX2+)	B71	LVDS_B0+
A72	LVDS_A0- (EDP_TX2-)	B72	LVDS_B0-
A73	LVDS_A1+ (EDP_TX1+)	B73	LVDS_B1+
A74	LVDS_A1- (EDP_TX1-)	B74	LVDS_B1-
A75	LVDS_A2+ (EDP_TX0+)	B75	LVDS_B2+
A76	LVDS_A2- (EDP_TX0-)	B76	LVDS_B2-
A77	LVDS_VDD_EN (CB_DDI0_VDDEN)	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN (CB_DDI0_BKLTEN)
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+ (EDP_TX3+)	B81	LVDS_B_CK+
A82	LVDS_A_CK- (EDP_TX3-)	B82	LVDS_B_CK-
A83	LVDS_I2C_CK (EDP_AUXP)	B83	LVDS_BKLT_CTRL (CB_DDI0_BKLTCTL)
A84	LVDS_I2C_DAT (EDP_AUXN)	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY

A86	KBRST#	B86	VCC_5V_SBY
A87	H_A20GATE (DDI0_HPD_3.3S)	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BISO_DIS1#
A89	PCIE0_CK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	+V3.3S(option)	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	GND	B96	VGA_I2C_DAT
A97	N.C	B97	SPI_CS#
A98	CB_STXD1X	B98	SMI#
A99	CB_SRXD1X	B99	SCI#
A100	GND (FIXED)	B100	GND (FIXED)
A101	CB_STXD2X	B101	CB_FAN_PWM
A102	CB_SRXD2X	B102	CB_FAN_TACH
A103	PCH_LID#	B103	PCH_SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

2.3.5 ROW C/D Connector (CN6)

Row C		Row D	
Pin	Signal	Pin	Signal
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND (FIXED)	D2	GND (FIXED)
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND (FIXED)	D5	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND (FIXED)	D8	GND (FIXED)
C9	N.C	D9	N.C
C10	N.C	D10	N.C
C11	GND (FIXED)	D11	GND (FIXED)
C12	N.C	D12	N.C
C13	N.C	D13	N.C
C14	GND (FIXED)	D14	GND (FIXED)
C15	N.C	D15	DDI1_CTRLCLK_AUX+
C16	N.C	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD
C18	RSVD	D18	RSVD
C19	i	D19	N.C
C20	N.C	D20	N.C
C21	GND (FIXED)	D21	GND (FIXED)
C22	N.C	D22	N.C
C23	N.C	D23	N.C

C24	DDI1_HPD	D24	RSVD
C25	N.C	D25	RSVD
C26	N.C	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	N.C	D29	DDI1_PAIR1+
C30	N.C	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	N.C	D36	DDI1_PAIR3+
C37	N.C	D37	DDI1_PAIR3-
C38	N.C	D38	RSVD
C39	N.C	D39	DDI2_PAIR0+
C40	N.C	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	N.C	D42	DDI2_PAIR1+
C43	N.C	D43	DDI2_PAIR1-
C44	N.C	D44	DDI1_HPD
C45	RSVD	D45	RSVD
C46	N.C	D46	DDI2_PAIR2+
C47	N.C	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	N.C	D49	DDI2_PAIR3+
C50	N.C	D50	DDI2_PAIR3-

C51	GND (FIXED)	D51	GND (FIXED)
C52	N.C	D52	N.C
C53	N.C	D53	N.C
C54	N.C	D54	N.C
C55	N.C	D55	N.C
C56	N.C	D56	N.C
C57	N.C	D57	GND
C58	N.C	D58	N.C
C59	N.C	D59	N.C
C60	GND (FIXED)	D60	GND (FIXED)
C61	N.C	D61	N.C
C62	N.C	D62	N.C
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	N.C	D65	N.C
C66	N.C	D66	N.C
C67	RSVD	D67	GND (FIXED)
C68	N.C	D68	N.C
C69	N.C	D69	N.C
C70	GND (FIXED)	D70	GND (FIXED)
C71	N.C	D71	N.C
C72	N.C	D72	N.C
C73	GND (FIXED)	D73	GND (FIXED)
C74	N.C	D74	N.C
C75	N.C	D75	N.C
C76	GND (FIXED)	D76	GND (FIXED)
C77	RSVD	D77	RSVD

C78	N.C	D78	N.C
C79	N.C	D79	N.C
C80	GND (FIXED)	D80	GND (FIXED)
C81	N.C	D81	N.C
C82	N.C	D82	N.C
C83	RSVD	D83	RSVD
C84	GND (FIXED)	D84	GND (FIXED)
C85	N.C	D85	N.C
C86	N.C	D86	N.C
C87	GND (FIXED)	D87	GND (FIXED)
C88	N.C	D88	N.C
C89	N.C	D89	N.C
C90	GND (FIXED)	D90	GND (FIXED)
C91	N.C	D91	N.C
C92	N.C	D92	N.C
C93	GND	D93	GND
C94	N.C	D94	N.C
C95	N.C	D95	N.C
C96	GND (FIXED)	D96	GND (FIXED)
C97	RSVD	D97	RSVD
C98	N.C	D98	N.C
C99	N.C	D99	N.C
C100	GND (FIXED)	D100	GND (FIXED)
C101	N.C	D101	N.C
C102	N.C	D102	N.C
C103	GND (FIXED)	D103	GND
C104	VCC_12V	D104	VCC_12V

C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The COM-APLC6 CMOS memory has an integral lithium battery backup for data retention. However, you will need to replace the complete unit when it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <ESC> immediately. This will allow you to enter Setup.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

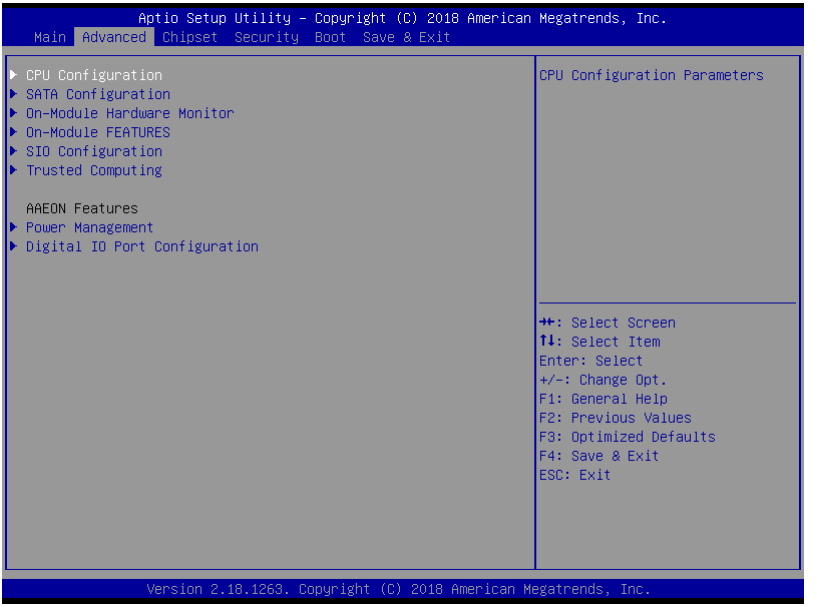
Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

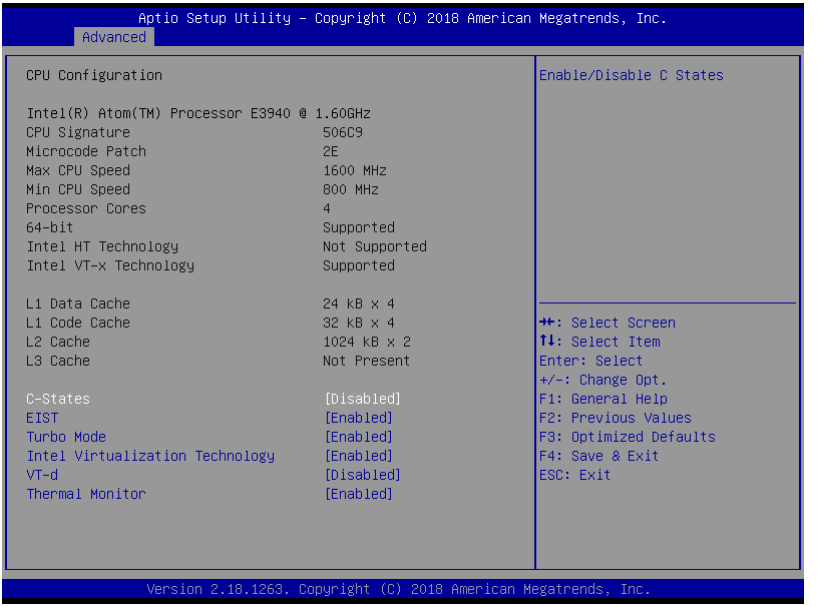
Save & Exit –Save your changes and exit the program

3.3 Setup submenu: Main

3.4 Setup submenu: Advanced



3.4.1 Advanced: CPU Configuration

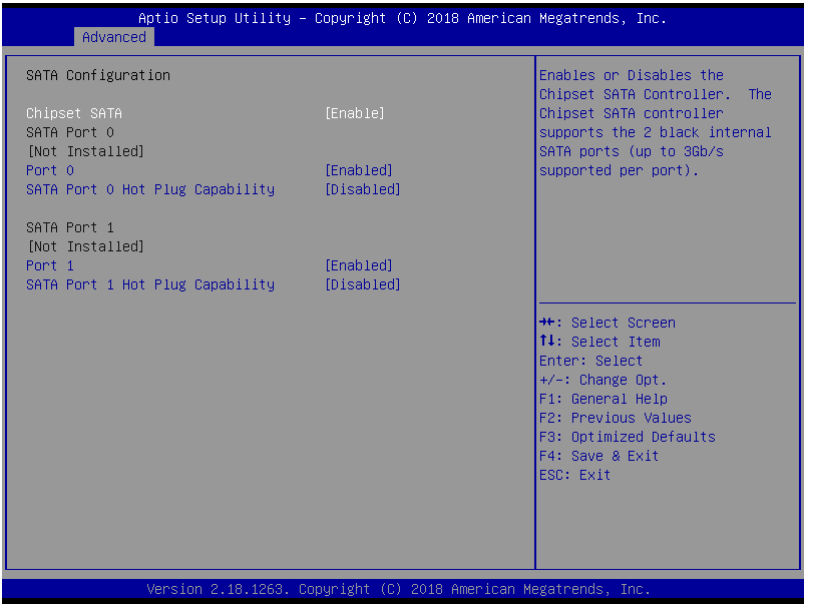


Options summary:

C-states	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable C states.		
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Intel speedstep.		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode.		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable CPU VT-d.		
Thermal Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Thermal Monitor.		

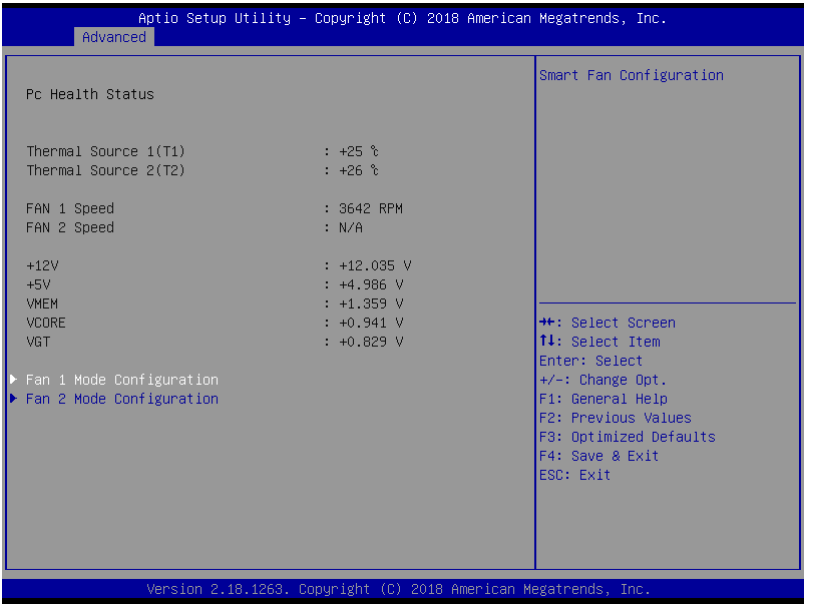
3.4.2 Advanced: SATA Configuration



Options summary:

Chipset SATA	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or disable the Chipset SATA Controller. The Chipset SATA Controller support the 2 black internal SATA ports (up to 3Gb/s supported per port).		
Port 0	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Port.		
SATA Port 0 Hot Plug Capability	Disabled	Optimal Default, Failsafe Default
	Enabled	
If enabled, SATA port will be reported as Hot Plug capable.		

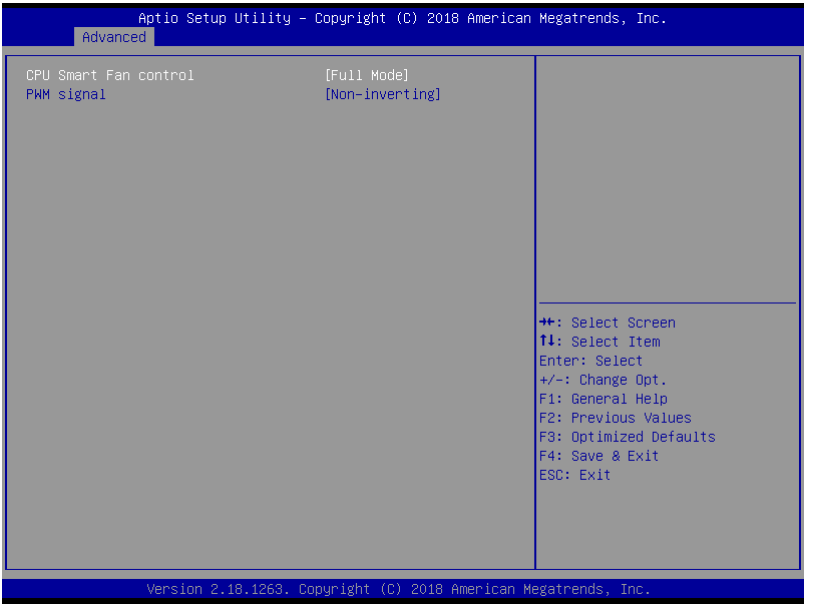
3.4.3 Advanced: On-Module Hardware Monitor



Options summary:

Fan 1 Mode Configuration
Fan 2 Mode Configuration
Smart Fan Configuration

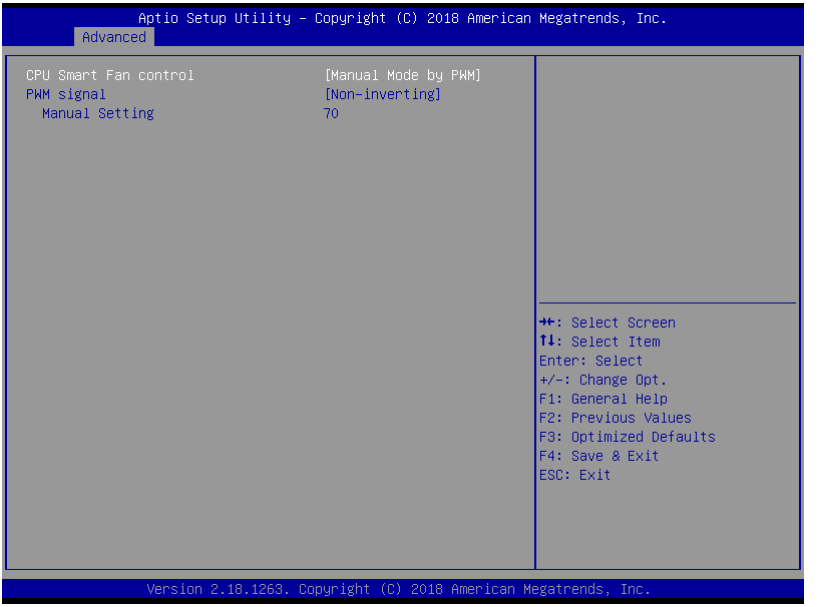
3.4.3.1 Fan Mode Configuration: Full Mode



Options summary:

CPU Smart Fan control	Full Mode	Optimal Default, Failsafe Default
	Manual Mode by PWM	
	Auto Mode by PWM	
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		

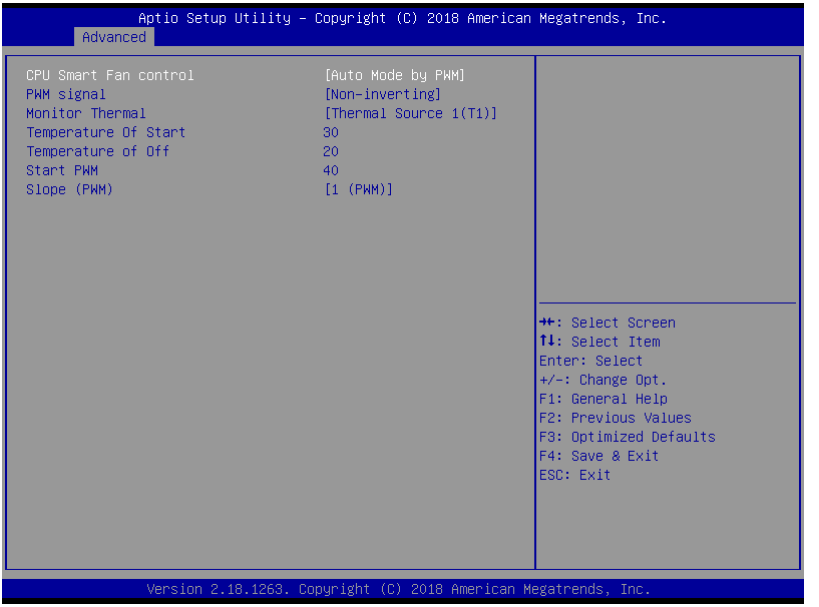
3.4.3.2 Fan Mode Configuration: Manual Mode by PWM



Options summary:

Manual Setting	70	Optimal Default, Failsafe Default
Set Fan at fixed Duty-Cycle Min=0 Max=100 Please input Dec number:		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-inverting signal		

3.4.3.3 Fan Mode Configuration: Auto Mode by PWM



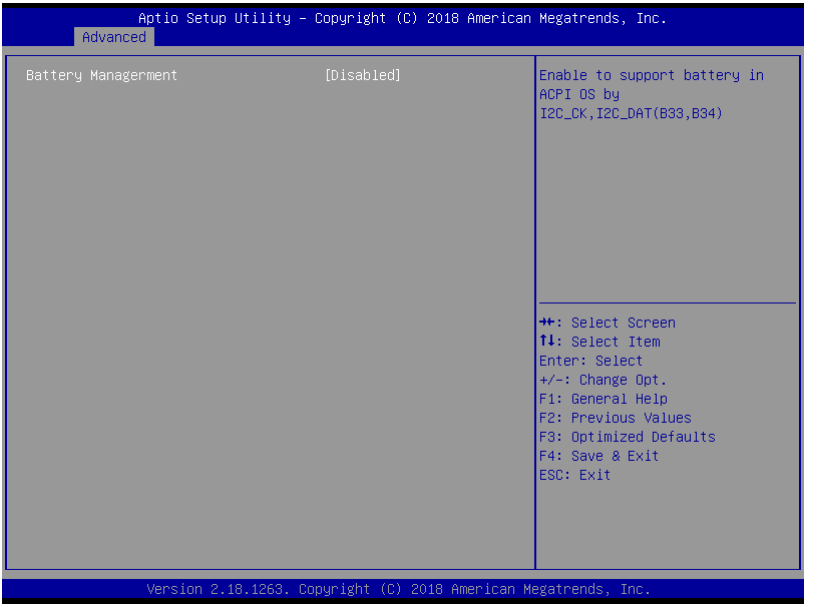
Options summary:

Monitor Thermal	Thermal Source 1(T1)	Optimal Default, Failsafe Default
	Thermal Source 2(T2)	
Select monitor thermal source		
PWM signal	Non-inverting	Optimal Default, Failsafe Default
	Inverting	
Select output PWM of inverting or non-univerting signal		
Temperature of Start	30	Optimal Default, Failsafe Default
Temperature Of Start		
Temperature Of Off	20	Optimal Default, Failsafe Default
Temperature Of Off		

Start PWM	40	Optimal Default, Failsafe Default
Start PWM		

Slope (PWM)	0 (PWM)	
	1 (PWM)	Optimal Default, Failsafe Default
	2 (PWM)	
	4 (PWM)	
	8 (PWM)	
	16 (PWM)	
	32 (PWM)	
	64 (PWM)	
Slope (PWM)		

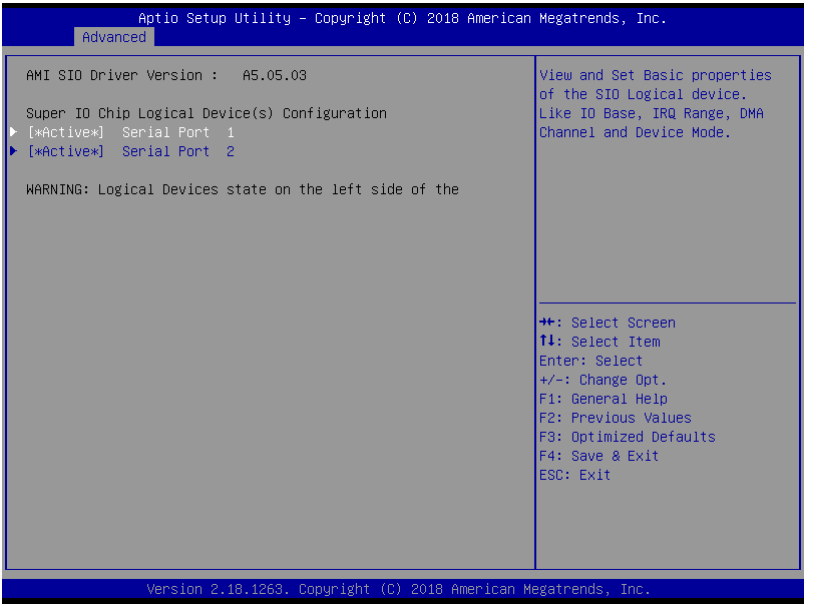
3.4.4 Advanced: On-Module FEATURES



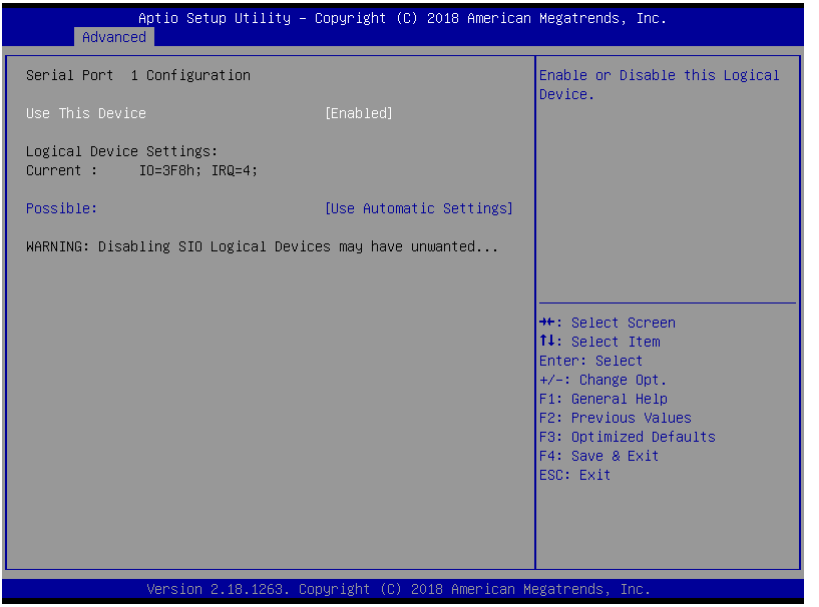
Options summary:

Battery Management	Disable	Optimal Default, Failsafe Default
	enable	
Enable to support battery in ACPI OS by I2C_CK, I2C_DAT(B33, B34)		

3.4.5 Advanced: SIO Configuration



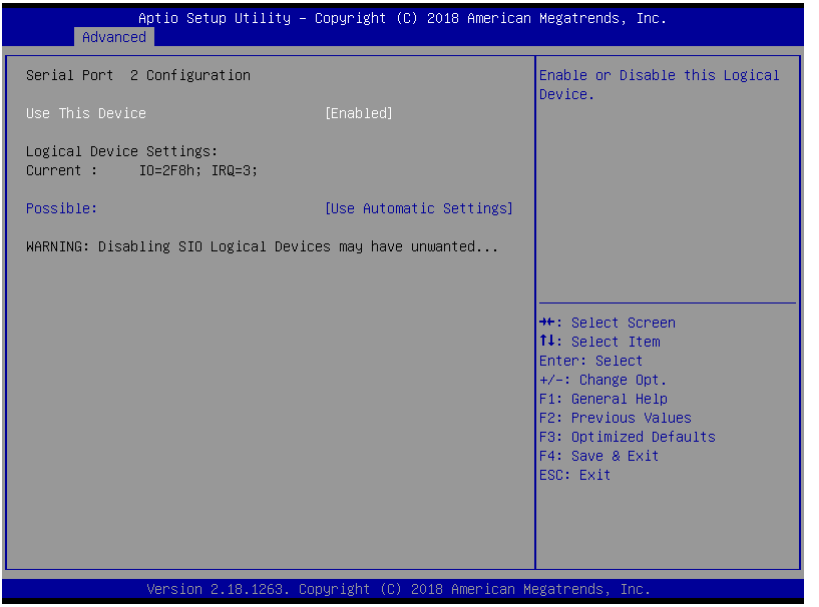
3.4.5.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4; DMA;	
	IO=2C8; IRQ=11; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

3.4.5.2 SIO Configuration: Serial Port 2 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable this Logical Device		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3; DMA;	
	IO=2D8; IRQ=10; DMA;	
Allow user to change Device's Resource settings. New settings will be reflected on This Setup Page after System restarts.		

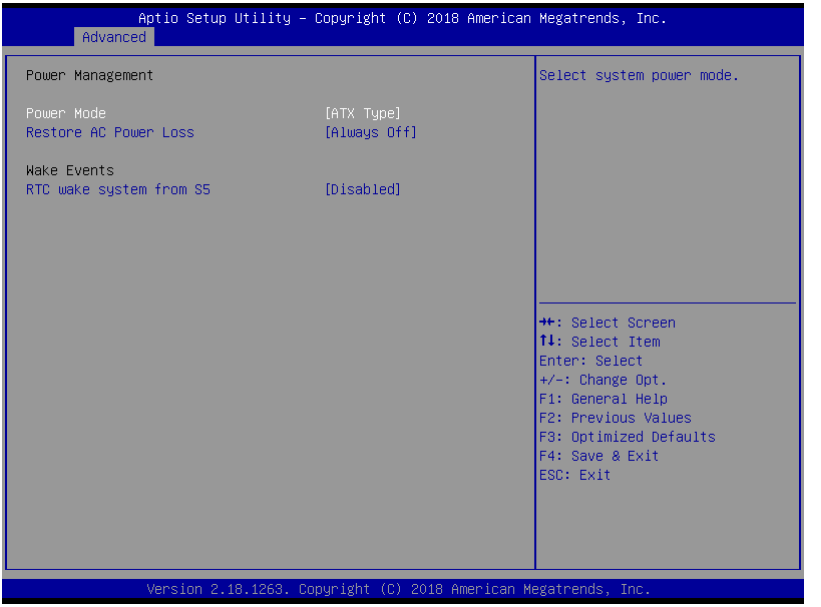
3.4.6 Advanced: Trusted Computing

Options summary:

Security Device Support	Disable	
	Enable	Optimal Default, Failsafe Default
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.		
TPM State	Disable	
	Enable	Optimal Default, Failsafe Default
Enables/Disables Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	

Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change state of Security Device.		
Device Select	TPM 1.2	
	TPM 2.0	
	Auto	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 device, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 device will be enumerated.		

3.4.7 Advanced: Power Management

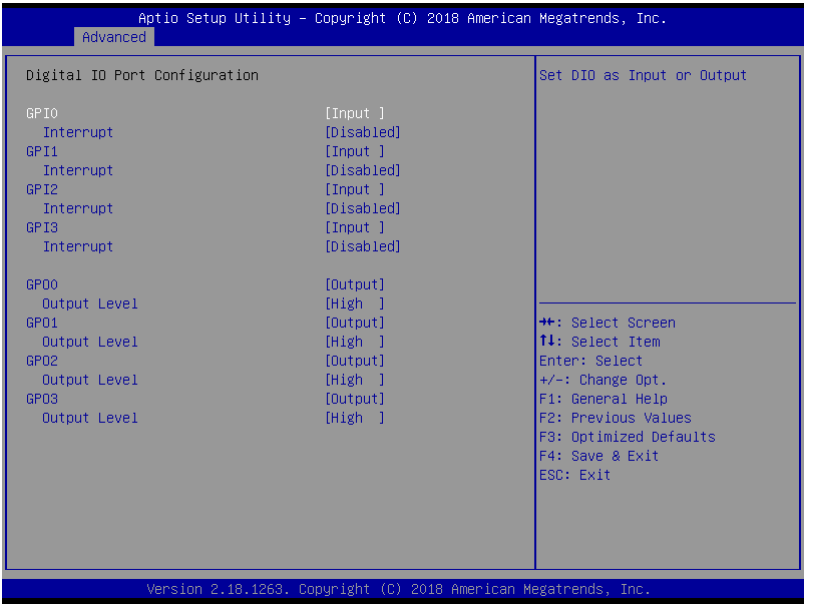


Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	

Fixed Time : System will wake om\n the hr :: min :: sec
Specified Dynamic Time: System will wake on the current time + Increase minutes(s).

3.4.8 Advanced: Digital IO Port Configuration

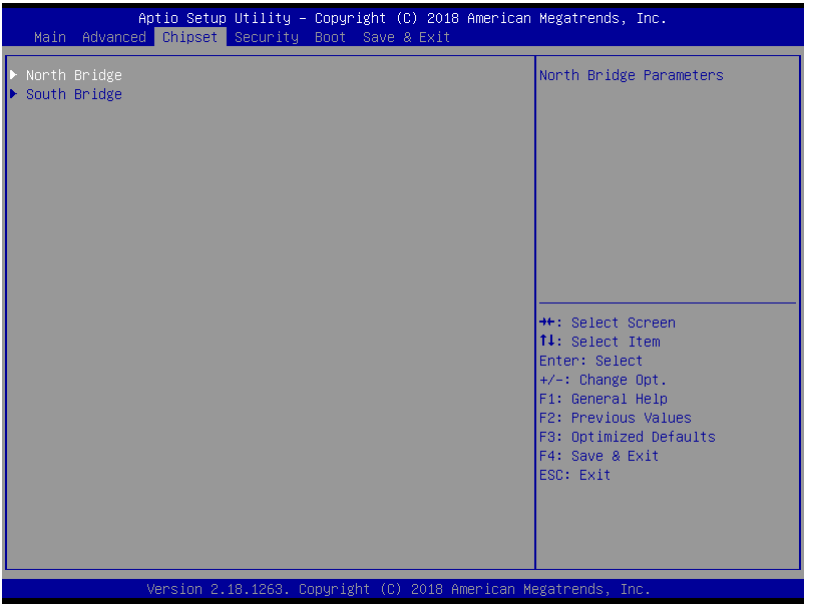


Options summary:

GPI*	Output	
	Input	
Set DIO as Input or Output		
Interrupt	Disable	Optimal Default, Failsafe Default
	Enable	
Enable interrupt function with low pulse mode. This triggered pulse needs more than the 10ms.		
GPO*	Output	
	Input	
Set DIO as Input or Output		
Output Level	High	Optimal Default, Failsafe Default

	Low	
Set output level when DIO pin is output		

3.5 Setup submenu: Chipset

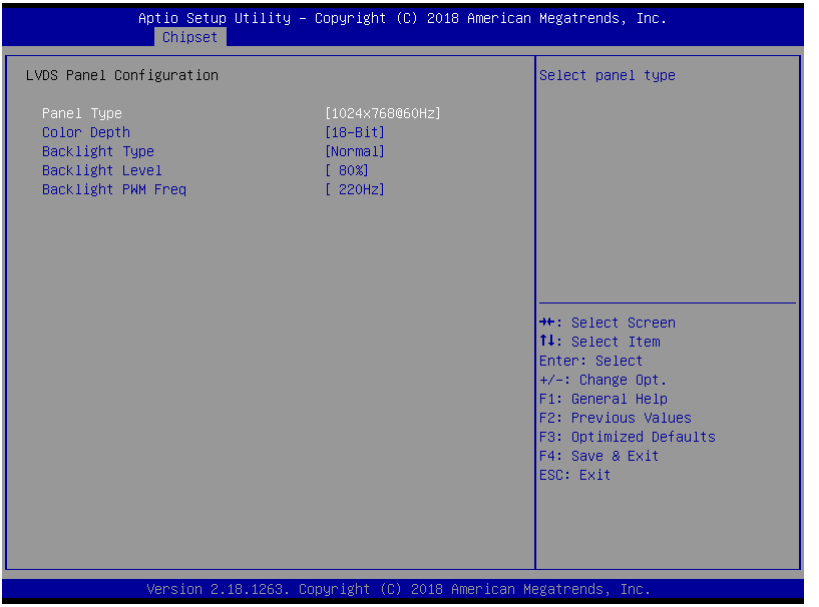


3.5.1 Chipset: North Bridge

Options summary:

Total Memory	8192 MB (LPDDR3)	
LVDS Panel Configuration	Configure LVDS panel parameters.	

3.5.1.1 North Bridge: LVDS Panel Configuration



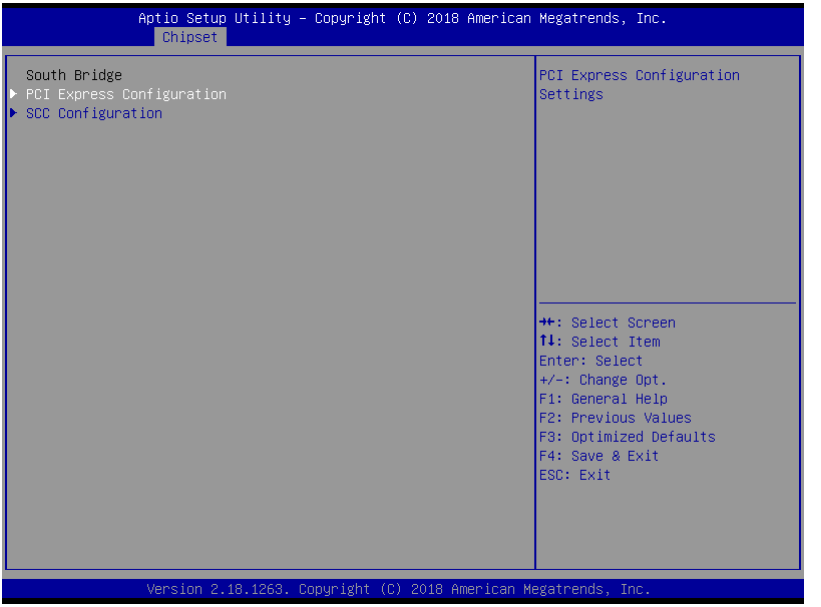
Options summary:

Panel Type	640x480@60Hz	
	800x480@60Hz	
	800x600@60Hz	
	1024x600@60Hz	
	1024x768@60Hz	Optimal Default, Failsafe Default
	1280x800@60Hz	
	1280x1024@60Hz	
	1366x768@60Hz	
	1440x900@60Hz	
	1600x1200@60Hz	
	1920x1080@60Hz	

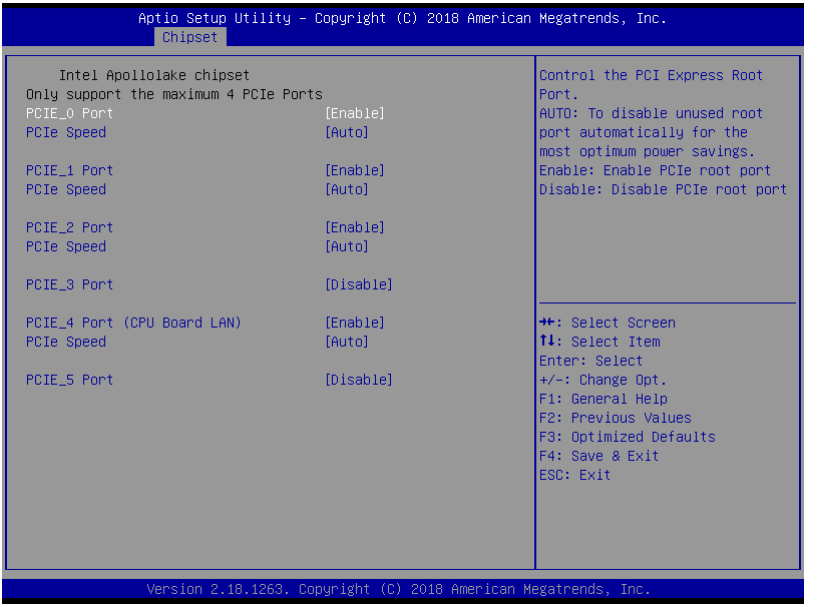
	1920x1200@,60Hz	
Select panel type.		
Color Depth	18-bit	Optimal Default, Failsafe Default
	24-bit	
	36-bit	
	48-bit	
Select panel type		
Backlight Type	Normal	Optimal Default, Failsafe Default
	Inverted	
Select backlight control signal type		
Backlight Level	0%	
	10%	
	20%	
	30%	
	40%	
	50%	
	60%	
	70%	
	80%	Optimal Default, Failsafe Default
	90%	
	100%	
Select backlight control level		
Backlight PWM Freq	100Hz	
	200Hz	
	220Hz	Optimal Default, Failsafe Default
	500Hz	
	1KHz	

	2.2KHz	
	6.5KHz	
Select PWM frequency of backlight control signal		

3.5.2 Chipset: South Bridge



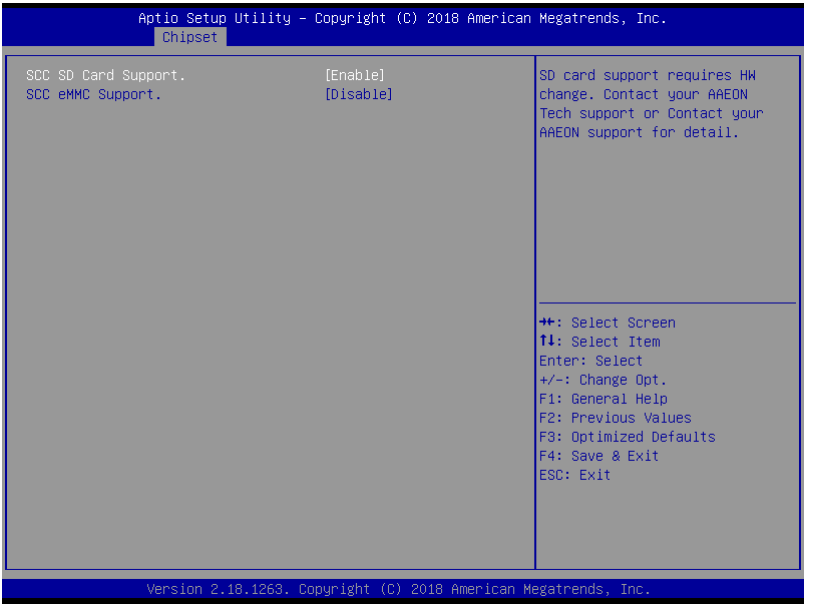
3.5.2.1 South Bridge: PCI Express Configuration



Options summary:

PCIE_* Port	Disabled	
	Enabled	Optimal Default, Failsafe Default
Control the PCI Express Root Port. AUTO : To disable unused root port automatically for the most optimum power savings. Enable : Enable PCIe root port. Disable : Disable PCIe root port.		
PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
Configure PCIe speed.		

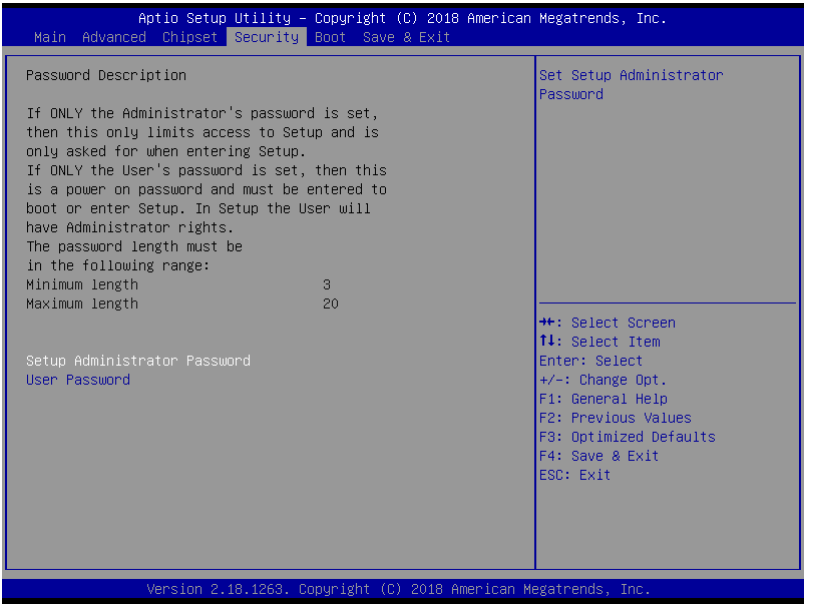
3.5.2.2 South Bridge: SCC Configuration



Options summary:

Scc SD Card Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
SD card support requires HW change. Contact your AAEON Tech support or Contact your AAEON Support for details.		
SCC eMMC Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable / Disable eMMC Support.		

3.6 Setup submenu: Security



Change User/ Supervisor Password

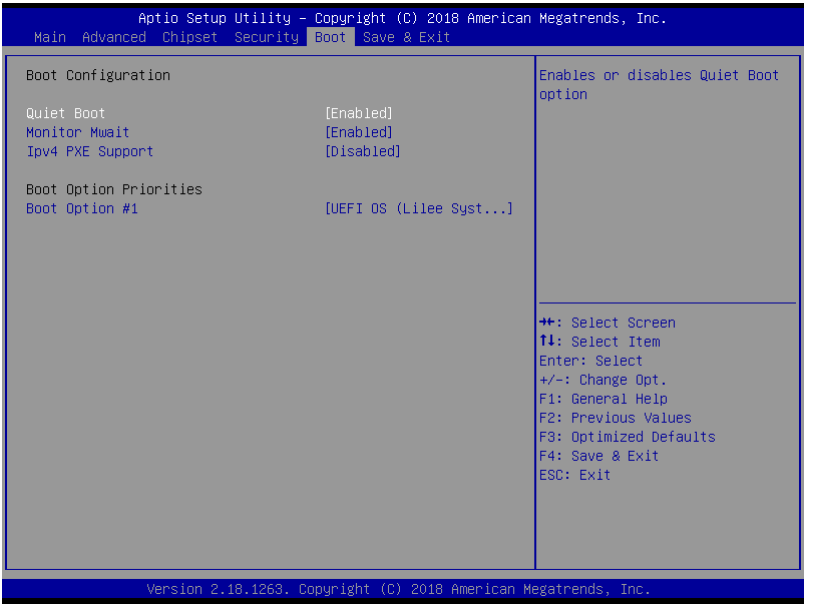
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup submenu: Boot

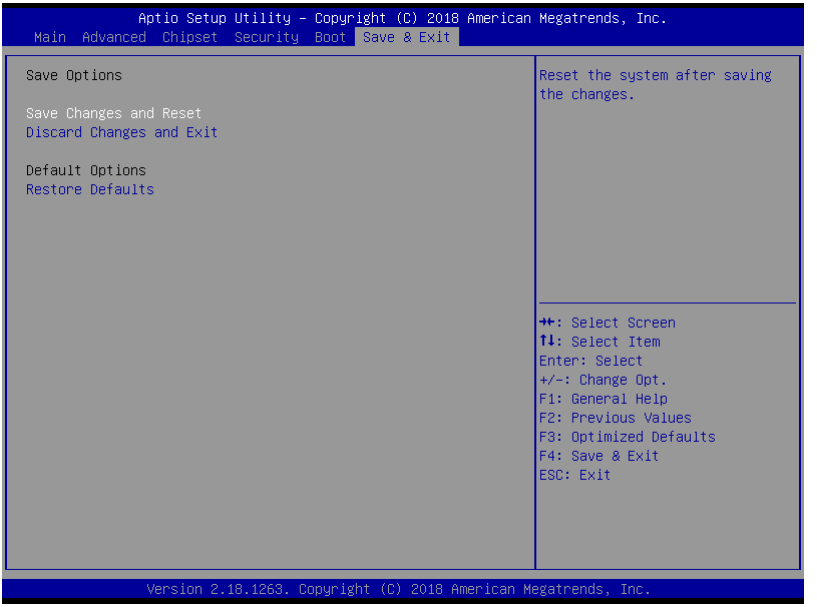


Options summary:

Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Quiet Boot option.		
Monitor	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable / Disable Monitor Mwait. To install Linux OS, please set this item to disable.		
Ipv4 PXE Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable Ipv4 Boot Support. If disabled IPV4 PXE boot option will not be created.		

Boot Option #1	UFEI OS (Lilee System SSM 1GB 0910)	Optimal Default, Failsafe Default
	Disabled	
Sets the system boot order.		

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The COM-APLC6 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **Step1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step2 - Graphics** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Driver

1. Open the **Step3 - LAN** folder followed by **Autorun.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **STEP4 - Audio** folder followed by **0002-Win7_Win8_Win81_R276.exe**

2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **STEP5 – USB3.0** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install ME Driver

1. Open the **STEP6 - TXE** folder followed by **SetupME.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA8(Note3)	Watch dog Logical Device Number
Function and Device Number	0x00(Note4)	Watch dog Function/Device Number

Table 2 : Watchdog relative register table				
	Option Register	BitNum	Value	Note
Timer Counter	0x00(Note5)		(Note10)	Time of watchdog timer (0~255)
Counting Unit	0x01(Note6)	0(Note7)	0(Note11)	Select time unit. 0: second 1: minute
Watchdog RST pulse width	0x01(Note8)	[3:2](Note9)	0(Note12)	0: 20ms 1: 60ms 2: 100ms 3: 250ms

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnDataReg   //This parameter is represented from Note4
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerReg   //This parameter is represented from Note5
#define byte   TimerVal   // This parameter is represented from Note10
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note11
#define byte   RSTReg   //This parameter is represented from Note8
#define byte   RSTBit   //This parameter is represented from Note9
#define byte   RSTVal   //This parameter is represented from Note12
*******************************************************************************
```

```
*******************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
// This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*******************************************************************************
```

```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable ()
WDTEnableDisable(1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig ()
// Disable WDT counting
WDTEnableDisable(0);
// WDT relative parameter setting
WDTParameterSetting();
}

VOID    WDTEnableDisable(byte Value)
        ECBRAMWriteByte(TimerReg , Value);
}

VOID    WDTParameterSetting()
        Byte TempByte;

// Watchdog Timer counter setting
ECBRAMWriteByte(TimerReg , TimerVal);
        // WDT counting unit setting
TempByte = ECBRAMReadByte(UnitReg);
TempByte |= (UnitVal << UnitBit);
ECBRAMWriteByte(UnitReg , TempByte);
// WDT RST pulse width setting
TempByte = ECBRAMReadByte(RSTReg);
TempByte |= (RSTVal << RSTBit);
ECBRAMWriteByte(RSTReg , TempByte);
}
*****************************************************************************
```

```
*******************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg);
IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
IOWriteByte(EcBRAMData, Value);

IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x30);                  //Write start
}

Byte    ECBRAMReadByte(byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg);
IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x10);                  //Read start

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
Return          IOReadByte(EcBRAMData, Value);
}
*******************************************************************************
```

Appendix B

Programming Digital I/O

B.1 DIO Programming

COM-APLC6 utilizes AAEON chipset as its Digital I/O controller.

Below are the procedures to complete its configuration which you can develop customized program to fit your application.

B.2 Digital I/O Register

Table 1 : Embedded BRAM relative register table		
	Default Value	Note
Index	0x284(Note1)	BRAM Index Register
Data	0x285(Note2)	BRAM Data Register
Logical Device Number	0xA2(Note3)	Watch dog Logical Device Number
IO Direction Function and Device Number	0x00(Note4)	DIO Input/Output Function/Device Number
IO Vaule/Status Function and Device Number	0x01(Note5)	DIO Output Data Function/Device Number

Table 2 : Digital I/O relative register table				
	Register			
	Option Register	BitNum	Value	Note
GPI0 Pin Status	0x00(Note6)	0(Note7)	(Note15)	GPA2
GPI1 Pin Status	0x00(Note6)	1(Note8)	(Note16)	GPA3
GPI2 Pin Status	0x00(Note6)	2(Note9)	(Note17)	GPA4
GPI3 Pin Status	0x00(Note6)	3(Note10)	(Note18)	GPA5
GPO0 Pin Status	0x00(Note6)	4(Note11)	(Note19)	GPJ0
GPO1 Pin Status	0x00(Note6)	5(Note12)	(Note20)	GPJ1
GPO2 Pin Status	0x00(Note6)	6(Note13)	(Note21)	GPJ2
GPO3 Pin Status	0x00(Note6)	7(Note14)	(Note22)	GPJ3

B.3 Digital I/O Sample Program

```
*******************************************************************************
// Embedded BRAM relative definition (Please reference to Table 1)
#define byte   EcBRAMIndex   //This parameter is represented from Note1
#define byte   EcBRAMData    //This parameter is represented from Note2
#define byte   BRAMLDNReg    //This parameter is represented from Note3
#define byte   BRAMFnData0Reg    //This parameter is represented from Note4
#define byte   BRAMFnData1Reg    //This parameter is represented from Note5
#define   void   EcBRAMWriteByte(byte Offset, byte Value);
#define   byte   EcBRAMReadByte(byte Offset);
#define   void   IOWriteByte(byte Offset, byte Value);
#define   byte   IOReadByte(byte Offset);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DIO0ToDIO7Reg    // This parameter is represented from Note6
#define byte   DIO0Bit    // This parameter is represented from Note7
#define byte   DIO1Bit    // This parameter is represented from Note8
#define byte   DIO2Bit    // This parameter is represented from Note9
#define byte   DIO3Bit    // This parameter is represented from Note10
#define byte   DIO4Bit    // This parameter is represented from Note11
#define byte   DIO5Bit    // This parameter is represented from Note12
#define byte   DIO6Bit    // This parameter is represented from Note13
#define byte   DIO7Bit    // This parameter is represented from Note14
#define byte   DIO0Val    // This parameter is represented from Note15
#define byte   DIO1Val    // This parameter is represented from Note16
#define byte   DIO2Val    // This parameter is represented from Note17
#define byte   DIO3Val    // This parameter is represented from Note18
#define byte   DIO4Val    // This parameter is represented from Note19
#define byte   DIO5Val    // This parameter is represented from Note20
#define byte   DIO6Val    // This parameter is represented from Note21
#define byte   DIO7Val    // This parameter is represented from Note22
*******************************************************************************
```

```
*****************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //      Example, Read Digital I/O Pin 3 status
// Output :
//      InputStatus :
//              0: Digital I/O Pin level is low
//              1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DIO0ToDIO7Reg, DIO3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //      Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DIO0ToDIO7Reg, DIO6Bit, DIO6Val);
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte OptionReg, byte BitNum){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        If (TempByte & BitNum == 0)
                Return 0;
        Return 1;
}
VOID    AaeonSetOutputLevel(byte OptionReg, byte BitNum, byte Value){
        Byte TempByte;

        TempByte = ECBRAMReadByte(BRAMFnData1Reg, OptionReg);
        TempByte |= (Value << BitNum);
ECBRAMWriteByte(OptionReg, BitNum, Value);
}

*****************************************************************************
```

```
*******************************************************************************
VOID    ECBRAMWriteByte(byte OPReg, byte OPBit, byte Value){
        IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg);
IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, BRAMFnDataReg);

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
IOWriteByte(EcBRAMData, Value);

IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x30);                  //Write start
}

Byte    ECBRAMReadByte(byte FnDataReg, byte OPReg){
        IOWriteByte(EcBRAMIndex, 0x10);
IOWriteByte(EcBRAMData, BRAMLDNReg);
IOWriteByte(EcBRAMIndex, 0x11);
IOWriteByte(EcBRAMData, FnDataReg);

IOWriteByte(EcBRAMIndex, 0x12);
IOWriteByte(EcBRAMData, 0x10);                  //Read start

IOWriteByte(EcBRAMIndex, 0x13 + OPReg);
Return          IOReadByte(EcBRAMData, Value);
}
*******************************************************************************
```