BOXER-8331AI

Embedded AI Vision System

User's Manual 1st Ed

Last Updated: October 22, 2019

Copyright Notice

Acknowledgement

Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
BOXER-8331AI	1
NVIDIA GeForce RTX-2060S or RTX-2080 Ti Graphics Card	1
Wallmount bracket	2
3-pin DC in Power Connector	2
Screw Package	1
Thermal Pad Package	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the BOXER-8331AI product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON System QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚(PBDE)
印刷电路板及其电子组件	×	○	○	○	○	○
外部信号连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件仍符合欧盟指令2011/65/EU 的规范。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

China RoHS Requirement (EN)

Hazardous and Toxic Materials List

AAEON System QO4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CrVI)	Polybrominated biphenyls (PBBs)	Polybrominated diphenyl ethers
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext.Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

System	
CPU	6th / 7th Gen Intel® Core™ desktop and Xeon® server grade processors -Intel® Core™ i7-6700TE, 2.4 GHz -Intel® Core™ i5-6500TE, 2.3 GHz -Intel® Core™ i3-6100TE, 2.7 GHz -Intel® Core™ i7-7700T, 2.9 GHz -Intel® Core™ i7-7700, 3.6 Ghz -Intel® Core™ i3-7101TE, 3.4 GHz -Intel® Xeon® E3-1268L v5, 2.40 GHz -Intel® Xeon® E3-1275 v6, 3.80 GHz
Chipset	Intel® C236 PCH
System Memory	DDR4 2133/2400 ECC or Non-ECC SODIMM up to 32GB
AI Solution	NVIDIA Graphics Card (RTX-2060 S or RTX-2080 Ti)
Display Interface System	HDMI 1.4b (built in interface for debug mode)
Display Interface GPU	via Graphics Card display interface
Storage Device	2 x 2.5" Drive Bay
Ethernet	10/100/1000 Base-TX x5
I/O	2 pin Remote Power on/off connector Power ON/OFF Switch x 1 HDMI type A x2 for HDMI v1.4b Audio x 2 (MIC-in, Line-out) USB 3.0 x 4, DB-9 x 1 for RS-232/422/485 3 pin DC Power input x 1 (+, - , GND) RJ-45 x5 for GbE LAN (Intel i211AT x4, i219LM x1)

System

Expansion	Full-size Mini card x2 (USB/PCIe, w/ 1 SIM slot) (A1) 1 x PCIe[x16], Built in NVIDIA RTX-2060 Super **(A1)** Built in NVIDIA RTX-2080 Ti **(A2)** Graphics card size limit: 114.55mm(H) x 350mm (L)
Indicator	Power LED x1, HDD active LED x1
OS Support	**6th Gen Intel® Core™/Xeon® (Skylake S):** Windows® 10, Windows® 10 IoT, Windows® 8 .1, Windows® Embedded Standard 8, Windows® 7, Windows® Embedded Standard 7, Ubuntu 16.04.2 **7th Gen Intel® Core™/Xeon® (Kabylake):** Windows® 10, Windows® 10 IoT, Ubuntu 16.04.2

Power Supply

SKU	CPU	Graphics Card Power consumption	Power Adapter	
			System Power	Graphics Power
A1	Under 73W	Under 180W	DC 12~24V 240W	DC 12V 240W
A2	Under 73W	180W to 250W		

Mechanical

Mounting	Wallmount
Dimensions (W x H x D)	6.10" x 7.87" x 15.75" (155mm x 200mm x 400mm)
Gross Weight	18.29 lbs. (8.3 kg)
Net Weight	14.53 lbs. (7 kg)

Environmental

Operating Temperature	0°C ~ 40°C according to IEC60068-2 with 0.5 m/s airflow
Storage Temperature	-4°F ~ 176°F (-40°C ~ 80°C)
Storage Humidity	5 ~ 95% @ 40C, non-condensing
Anti-Vibration	Random, 1Grm, 5~500Hz, Anti-vibration design
Certification	CE/FCC class A

1.2 SKU List

PN	PCH	I/O	PCIe (x16)	PCIe (x8)	PCIe (x1)	Chasis	Expansion Supported
BOXER-8331AI-A1	C236	4USB3, 5LAN, 1COM, 2HDMI DC12-24V	1	N/A	1	L/Fan	Graphics 180W
BOXER-8331AI-A2	C236		1	N/A	1	L/Fan	Graphics 250W

Chasis Key

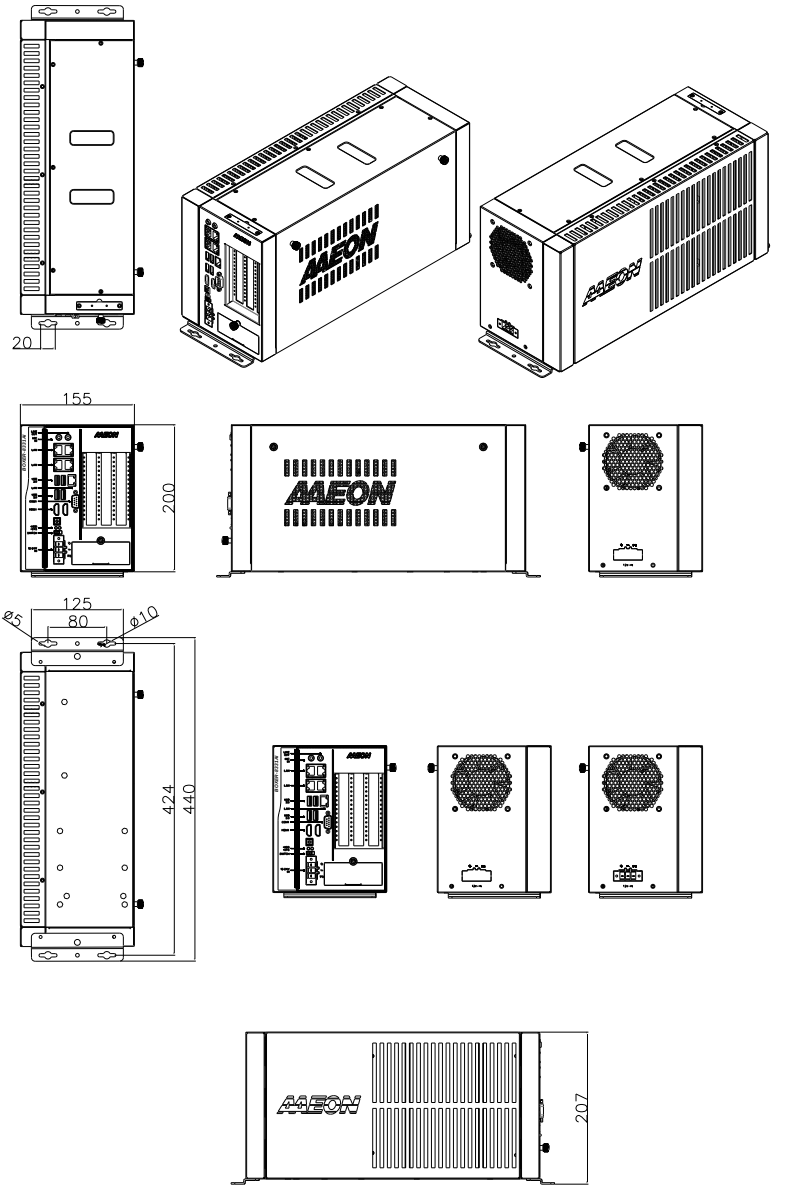
L/Fan – Long Fan System

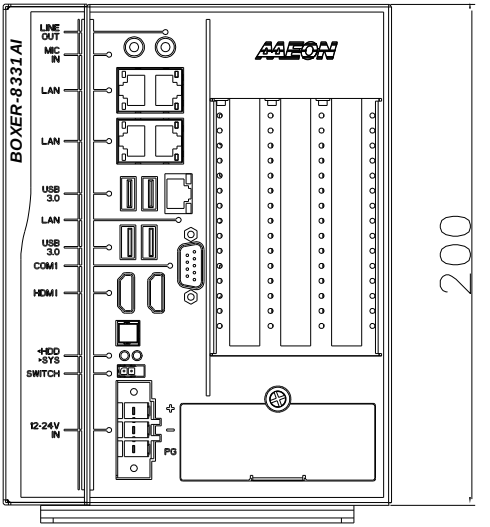
Chapter 2

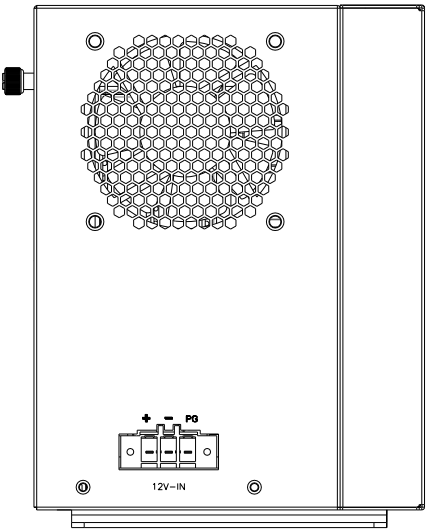
Hardware Information

2.1 Dimensions

BOXER-8331AI-A1/A2

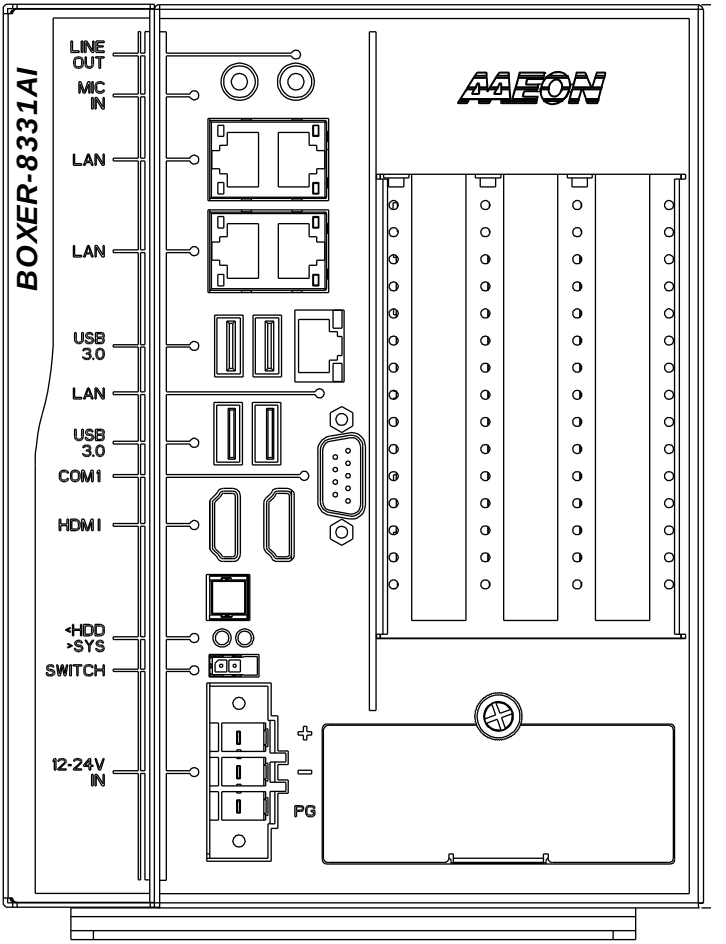



BOXER-8331AI
LINE OUT
MIC IN
LAN
LAN
USB 3.0
LAN
USB 3.0
COM1
HDMI
+HDD
+SYS
SWITCH
12-24V IN
+
-
PG
200


+
-
PG
12V-IN

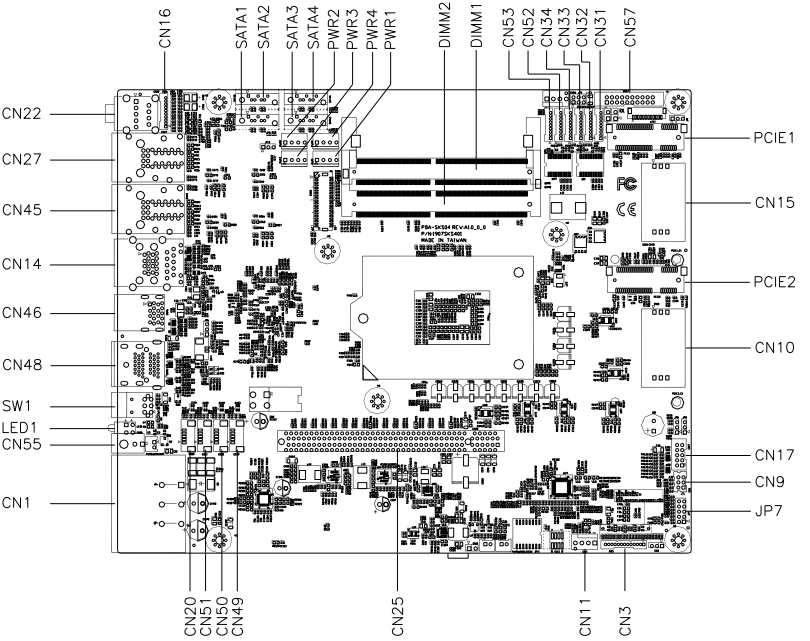
2.1.1 I/O Location

BOXER-8331AI-A1/A2

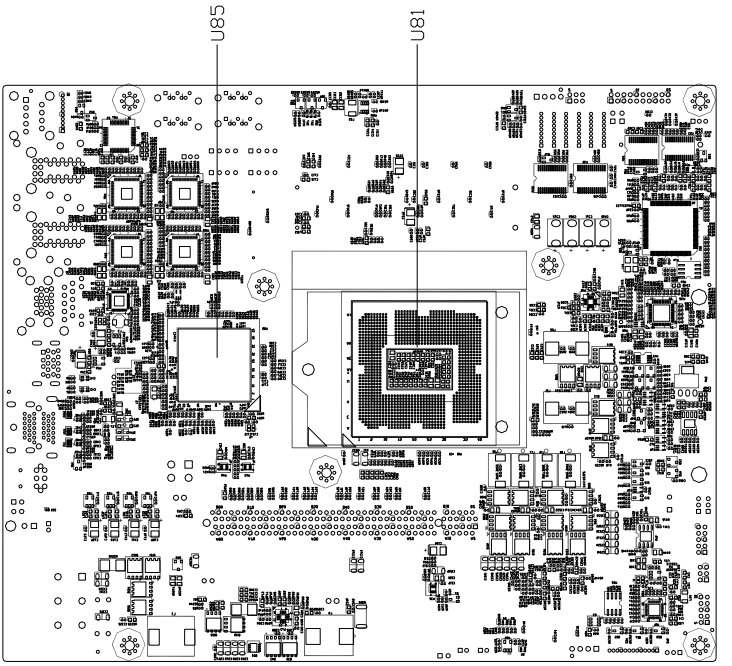


2.2 Jumpers and Connectors

Component Side



Solder Side

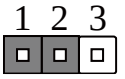


2.3 List of Jumpers

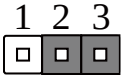
Please refer to the table below for all of the system's jumpers that you can configure for your application.

Label	Function
JP1	Auto Power Button Enable/Disable Selection
JP5	COM1 pin 9 function select
JP6	Clear CMOS Jumper
JP8	PEG Lanes CFG6 selection
JP9	PEG Lanes CFG5 selection

2.3.1 Auto Power Button Enable/Disable Selection (JP1)



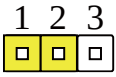
Disabled



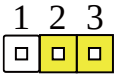
Enabled (Default)

Note: If Auto-Power Button (JP1) is set to Disabled (1-2), need to use power button (JP1) (1-2) to power on system.

2.3.2 Clear CMOS Jumper (JP6)



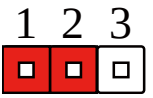
Normal (Default)



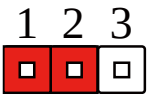
Clear CMOS

2.3.3 PEG Lanes CFG6 / CFG5 Selection (JP8 / JP9)

For PCI Express [x16]



(JP8 1-2)



(JP9 1-2)

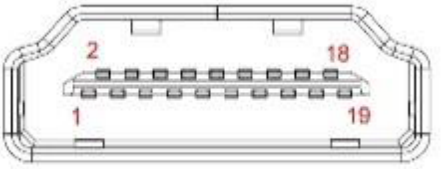
Note: PCIe[x16] slot jumper for use with one [x16] riser card.

2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

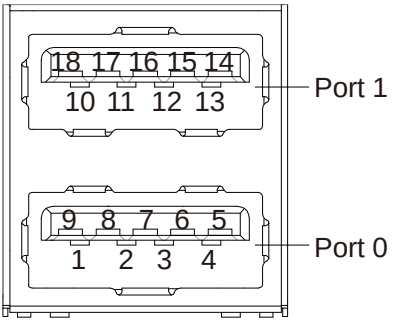
Label	Function
HDMI1	HDMI Connector (Only for Debug Mode)
HDMI2	HDMI Connector (Only for Debug Mode)
USB3.0 Port 1~4	USB 3.0 port
LAN Port 1~5	RJ45 10/100/1000Bps LAN connector
Audio Jack	3.5mm Audio Line-out/Mic-in connector
Remote Power Button	2-pin Remote Power On/Off button
Power Switch	Power On/Off switch
SATA Power Connector 1~2	SATA Storage power connector
SATA Signal Connector 1~2	SATA Storage signal connector
COM 1	DB9 RS232/485/422 connector
Mini Card 1-2	Mini-PCIE slot
SIM Slot	SIM card connector
DDR4 SODIMM SLOT 1~2	DDR4 260-pin memory slot

2.4.1 HDMI Port



Pin	Pin name	Signal Type	Signal Level
1	HDMI_DATA2_P	IN	
2	GND	PWR	
3	HDMI_DATA2_N		
4	HDMI_DATA1_P	GND	
5	GND		
6	HDMI_DATA1_N	PWR	
7	HDMI_DATA0_P	IN	
8	GND	PWR	
9	HDMI_DATA0_N	GND	
10	HDMI_CLK_P	I/O	
11	GND	DIFF	
12	HDMI_CLK_N	IN	
13	NC	DIFF	
14	NC	IN	
15	HDMI_SCL	GND	
16	HDMI_SDA	PWR	
17	GND		
18	HDMI_PWR	GND	
19	HDMI_HDP		

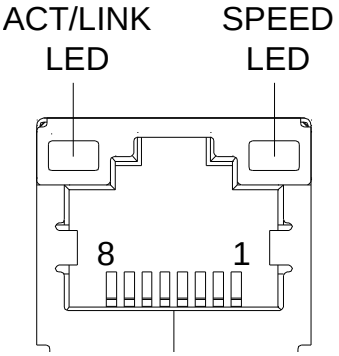
2.4.2 Dual USB 3.0



Pin	Pin name	Signal Type	Signal Level
U1	+5VSB	PWR	+5V
U2	USB0_D-	DIFF	
U3	USB0_D+	DIFF	
U4	GND	GND	
U5	USB0_SSRX−	DIFF	
U6	USB0_SSRX+	DIFF	
U7	GND	GND	
U8	USB0_SSTX−	DIFF	
U9	USB0_SSTX+	DIFF	
U10	+5VSB	PWR	+5V
U11	USB1_D-	DIFF	
U12	USB1_D+	DIFF	
U13	GND	GND	
U14	USB1_SSRX−	DIFF	
U15	USB1_SSRX+	DIFF	
U16	GND	GND	
U17	USB1_SSTX−	DIFF	
U18	USB1_SSTX+	DIFF	

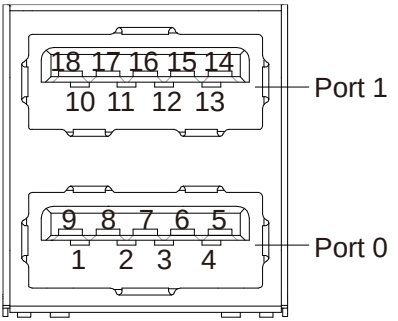
2.4.3 LAN (RJ-45) and Dual USB 3.0

LAN (RJ-45)



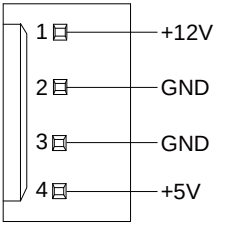
Pin	Pin name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

Dual USB 3.0



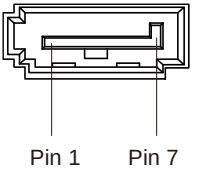
Pin	Pin name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX−	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX−	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX−	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX−	DIFF	
18	USB1_SSTX+	DIFF	

2.4.4 SATA Power connector 1~2



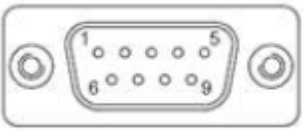
Pin	Pin name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	
3	GND	GND	
4	+5V	PWR	+5V

2.4.5 SATA Signal connector 1~2



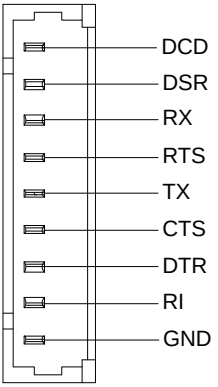
Pin	Pin name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

2.4.6 COM1 DB9 connector



Pin	RS232	RS422	RS485
1	DCD	TX-	D-
2	RXD	TX+	D+
3	TXD	RX+	NC
4	DTR	RX-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.7 COM1 (Wafer Box, Optional)



Pin	Pin name	Signal Type	Signal Level
1	DCD1	IN	
2	DSR1	IN	
3	RX1	IN	
4	RTS1	OUT	±9V
5	TX1	OUT	±9V
6	CTS1	IN	
7	DTR1	OUT	±9V
8	RI1	IN	
9	GND	GND	

2.4.8 Mini-Card Slot (Full-Mini Card)

Pin	Pin name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	N/A
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	
11	PCIE_REF_CLK-	DIFF	N/A
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	N/A
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	N/A
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	N/A
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V

Pin	Pin name	Signal Type	Signal Level
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	N/A
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	N/A
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.4.9 SIM Slot

Pin	Pin name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	GND	GND	
5	UIM_VPP	PWR	
6	UIM_DATA	I/O	

2.4.10 CPU FAN Socket

Pin	Pin name	Signal Type	Signal Level
1	GND	GND	
2	+VCC_FAN_CPU_CON	PWR	12V
3	FAN_TAC_CPU_CON		
4	FAN_CTL_CPU_CON		

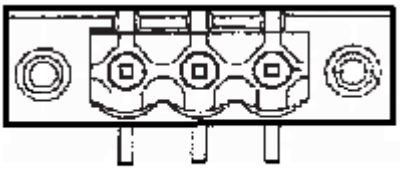
2.4.11 PCIEx16 Port

Standard specification

2.4.12 SPI Flash Port

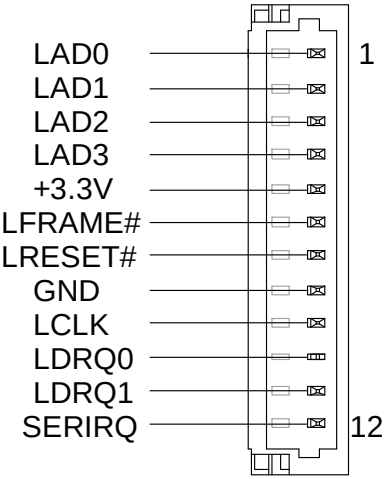
Pin	Pin name	Signal Type	Signal Level
1	+3.3VSB	PWR	+3.3V
2	GND	GND	
3	SPI_CS	IN	
4	SPI_CLK	IN	
5	SPI_MISO	OUT	
6	SPI_MOSI	IN	
7	NC		
8	NC		

2.4.13 DC-IN CONNECTOR



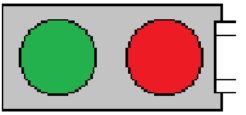
Pin	Pin name	Signal Type	Signal Level
1	VIN	PWR	+12V~+24V
2	GND	GND	
3	GND_EARTH	GND	

2.4.14 LPC Port



Pin	Pin name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.4.15 PWR LED/HDD LED



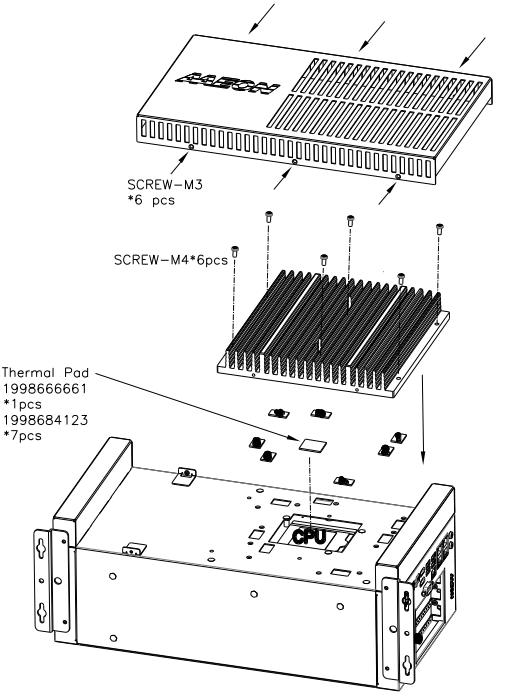
Pin	Pin name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	HDD_LED-		
3	+5V	PWR	+5V
4	PWR_LED-		

2.5 CPU Installation

Step 1: Shut down the system, disconnect power cord and ensure the system is turned off.

Step 2: Have Intel KabyLake/Skylake/Xeon FCLGA1151 Processor (Max. TDP 65W – KabyLake/Skylake; 73W – Xeon) ready.

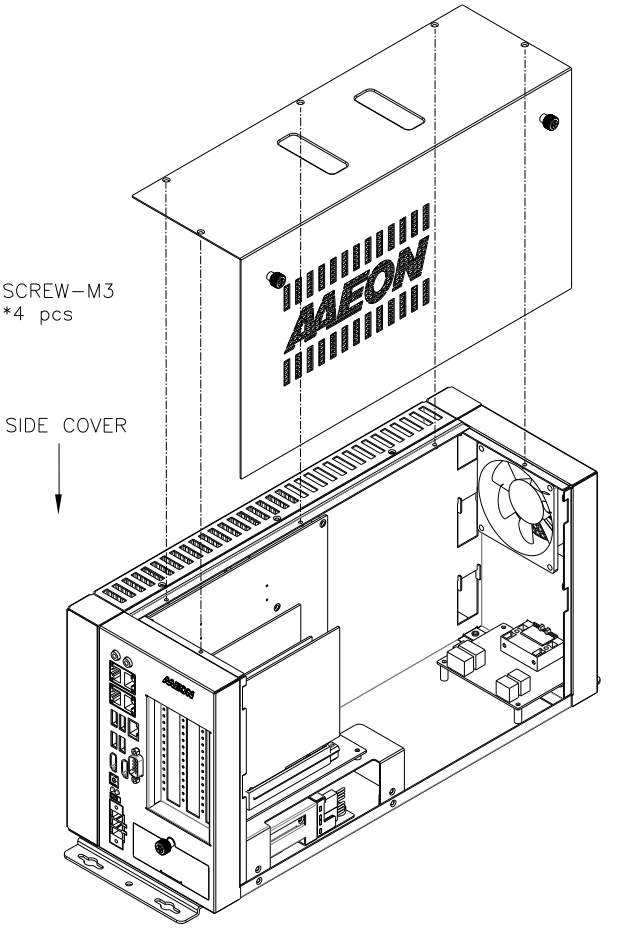
Step 3: Install the CPU into the socket and place the thermal pad onto it.



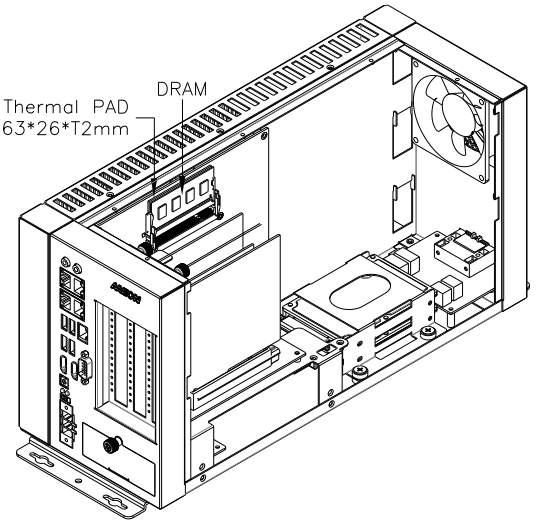
2.6 DDR4 Memory Module Installation

Step 1: Shut down the system, disconnect power cord and ensure the system is turned off.

Step 2: Remove the screws as shown below and remove the heatsink.



Step 3: Place the thermal pads onto the RAM modules as instructed below.



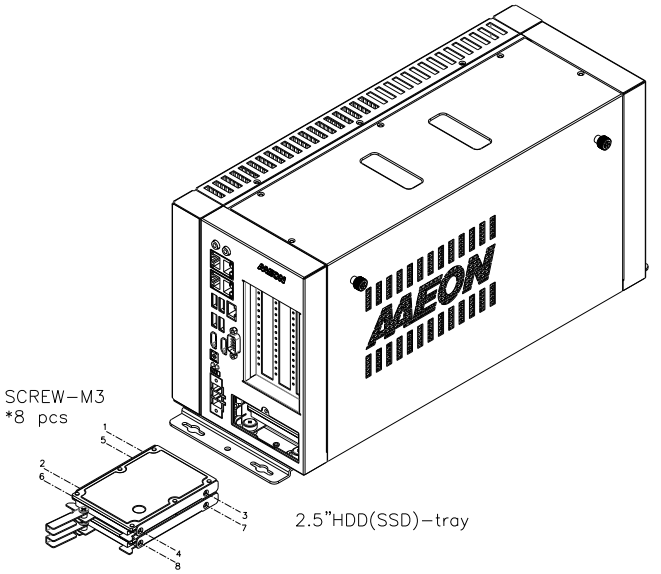
2.7 2.5" SATA Drive Installation

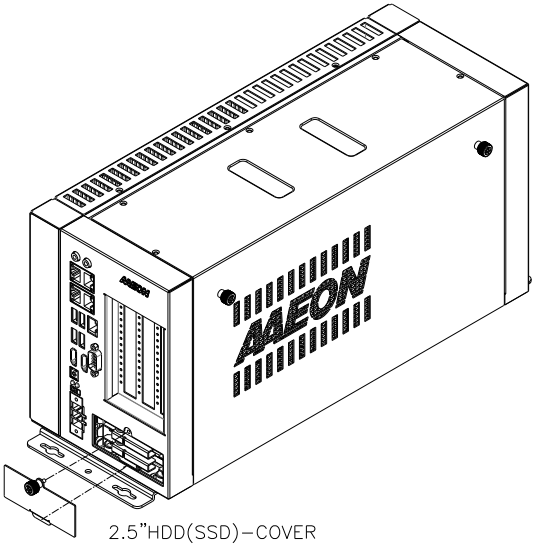
Step 1: Shut down the system, disconnect power cord and ensure the system is turned off.

Step 2: Remove the HDD cover.

Step 3: Use the HDD screws provided to assemble 2.5" SATA drive with the HDD Bracket. Insert HDD assembly into HDD Bay.

Step 4: Replace the HDD cover.

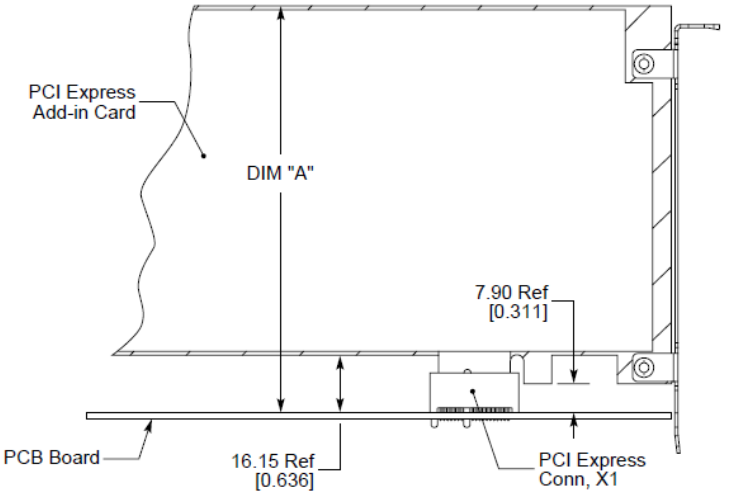




2.5”HDD(SSD)–COVER

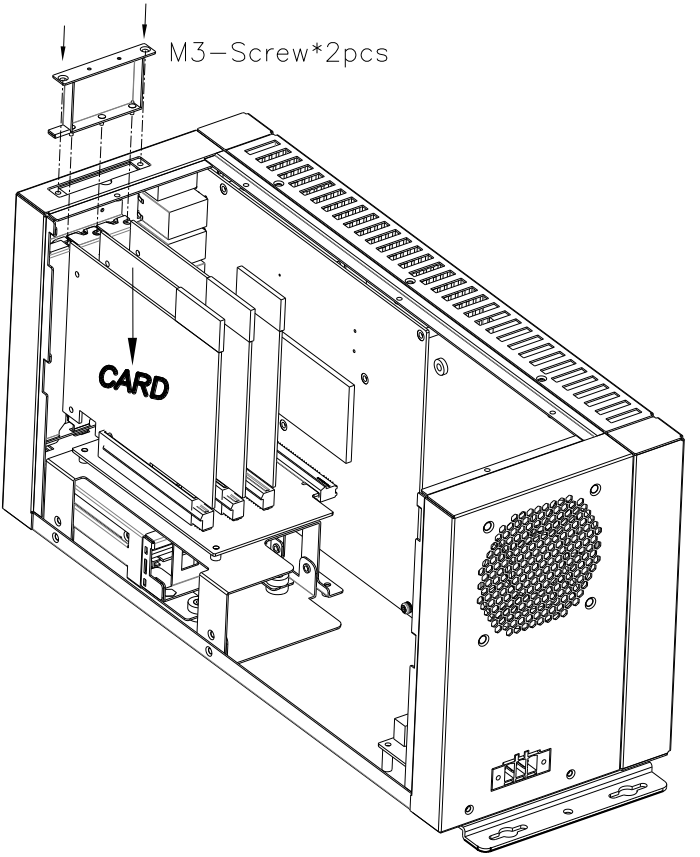
2.8 Graphics Card Installation

BOXER-8331AI-A1/A2 supports PCIe [x16] graphics card standard height at 114.55mm as below. Length should be under 350mm.

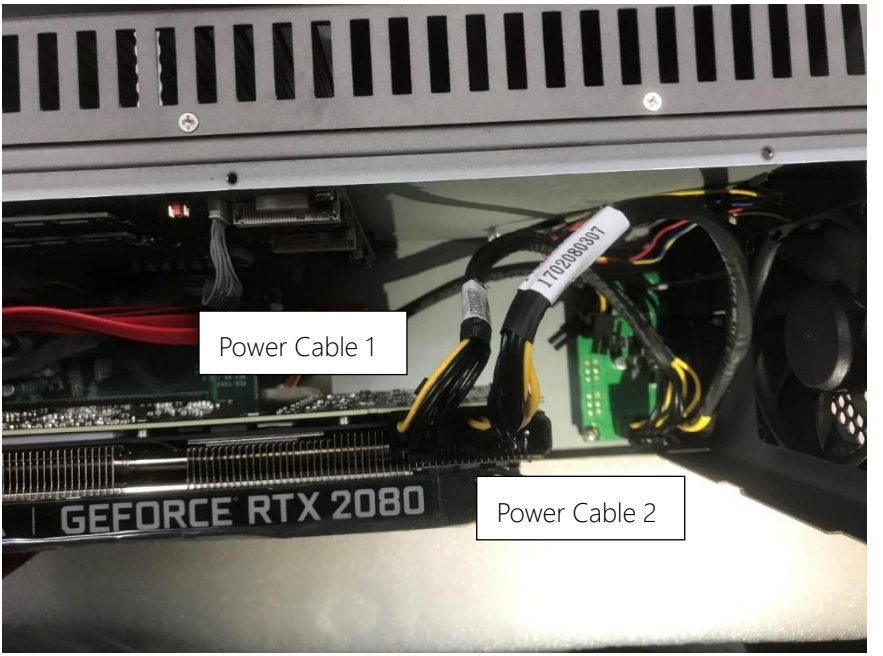


DIM "A"	
STANDARD HEIGHT	114.55 [4.510] MAX.
LOW PROFILE	72.30 [2.846] MAX.

Note: Lock the extension card with the RISER Bracket.



BOXER-8331AI-A1/A2 supports graphics cards up to 180W (A1) or up to 250W (A2). Graphics cards up to 250W require dual power connectors from the board. Connect the graphics card to Power Cable 1 and Power Cable 2.



The dual power system requires a special power sequence.

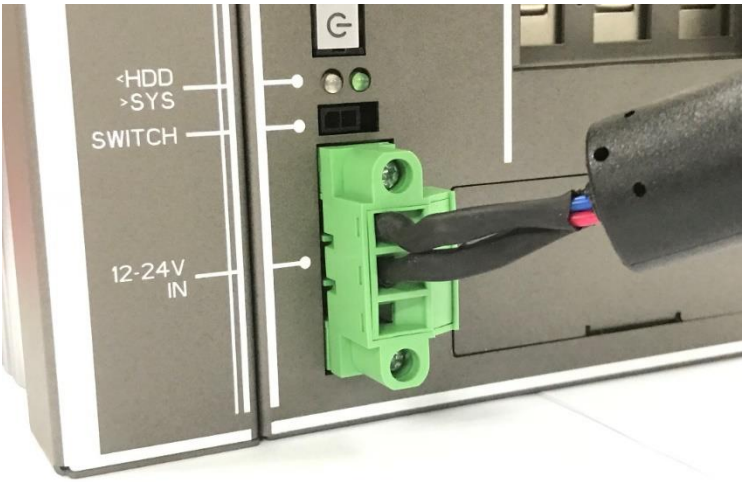
Please follow the power-up steps below

1. Insert 12V-240W adaptor graphics power input.

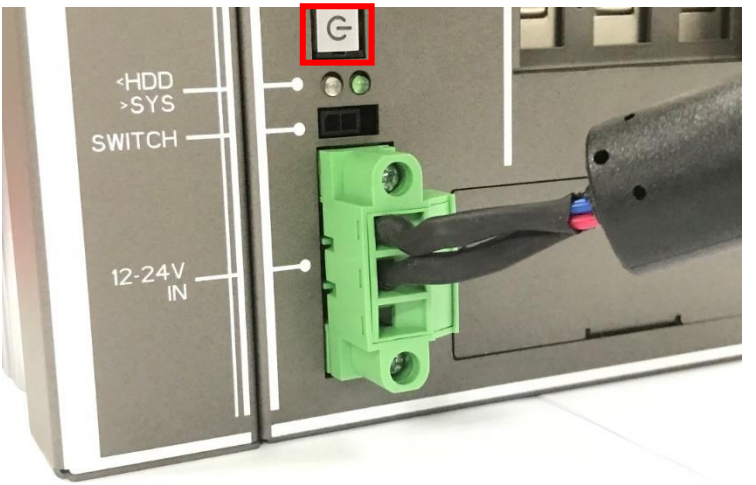
2. Turn on the 12V adaptor.

3. Check the 12V adaptor indicator LED is blue.

4. Insert 12V-24V adaptor system power input.



5. Switch on the system and you will see the screen display on the monitor.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, the system will sound a few short beeps or output an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, the system will output an error message, in which case you will need to run the BIOS setup program to set the configuration.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is required to be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

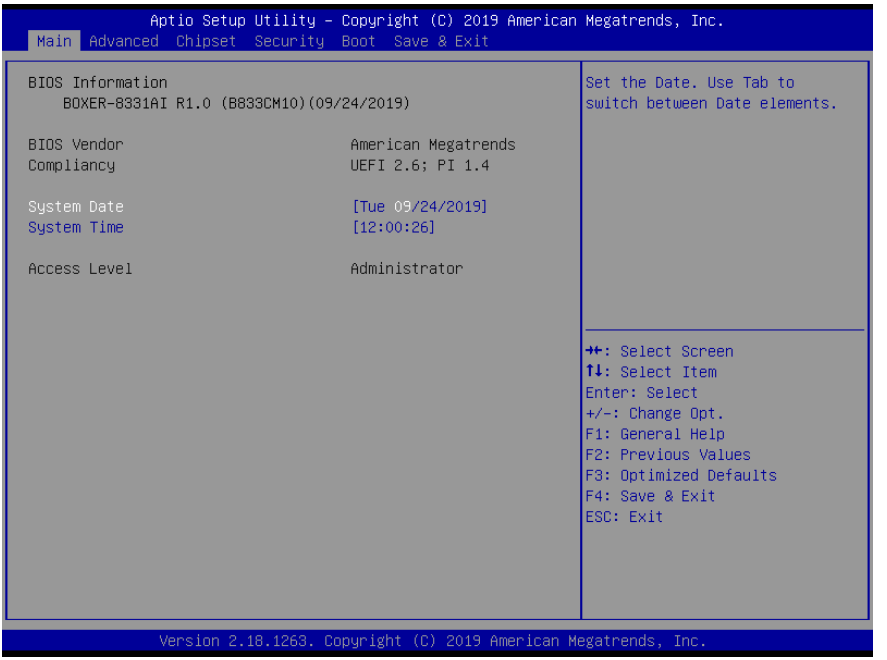
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

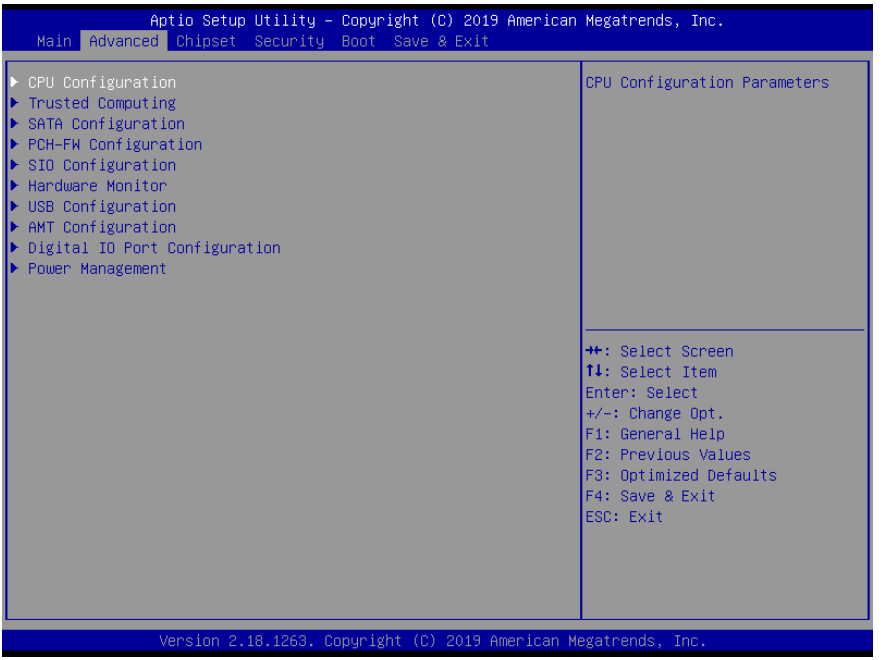
Boot – Enable/ Disable quiet Boot Option

Save & Exit –Save your changes and exit the program

3.3 Setup Submenu: Main



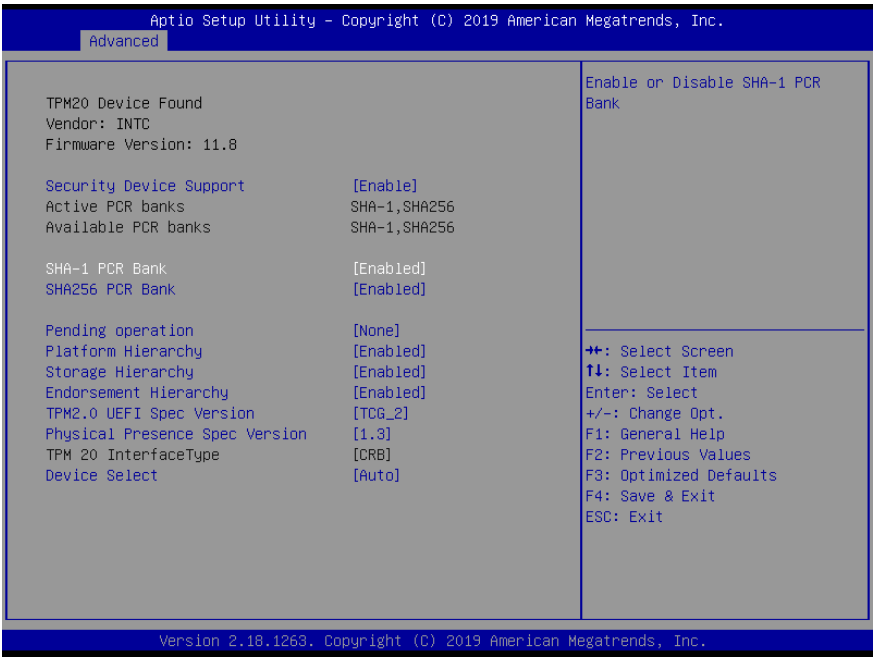
3.4 Setup Submenu: Advanced



3.4.1 Advanced: CPU Configuration

Options Summary		
Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Active Processor Cores	1	
	2	
	3	
	All	Optimal Default, Failsafe Default
Number of cores to enable in each processor package.		

3.4.2 Advanced: Trusted Computing



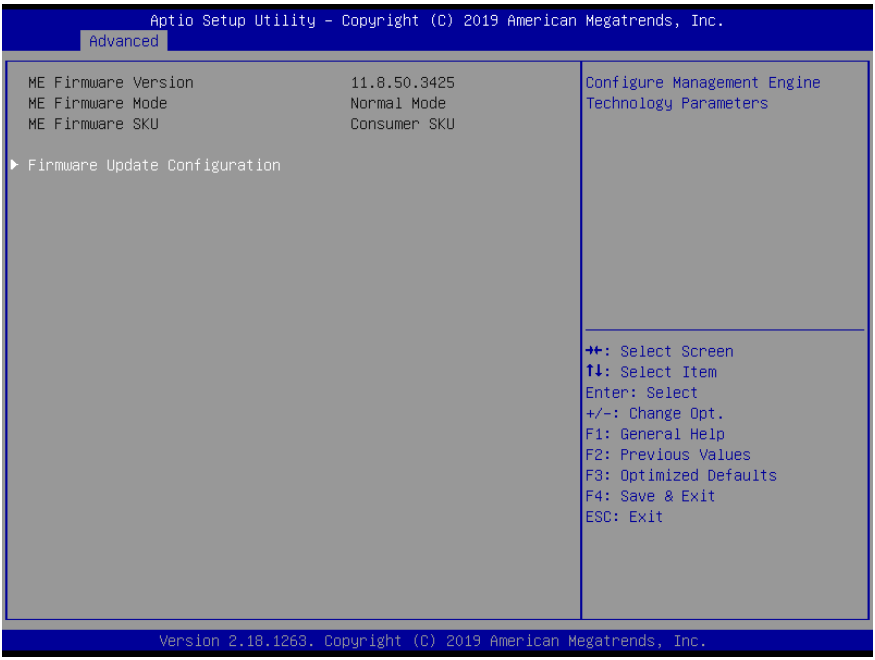
Options Summary		
Security Device Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
SHA-1 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA256 PCR Bank		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Options Summary		
Platform Hierarchy	Enabled Disabled	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
Storage Hierarchy	Enabled Disabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Enabled Disabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_2 TCG_1_2	Optimal Default, Failsafe Default
Select the TCG2 Spec Version Support TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.3 1.2	Optimal Default, Failsafe Default
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note: some HCK tests might not support 1.3.		
TPM 20 InterfaceType	CRB TIS	Optimal Default, Failsafe Default
Select the Communication Interface to TPM 20 Device.		
Device Select	Auto TPM 1.2 TPM 2.0	Optimal Default, Failsafe Default
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

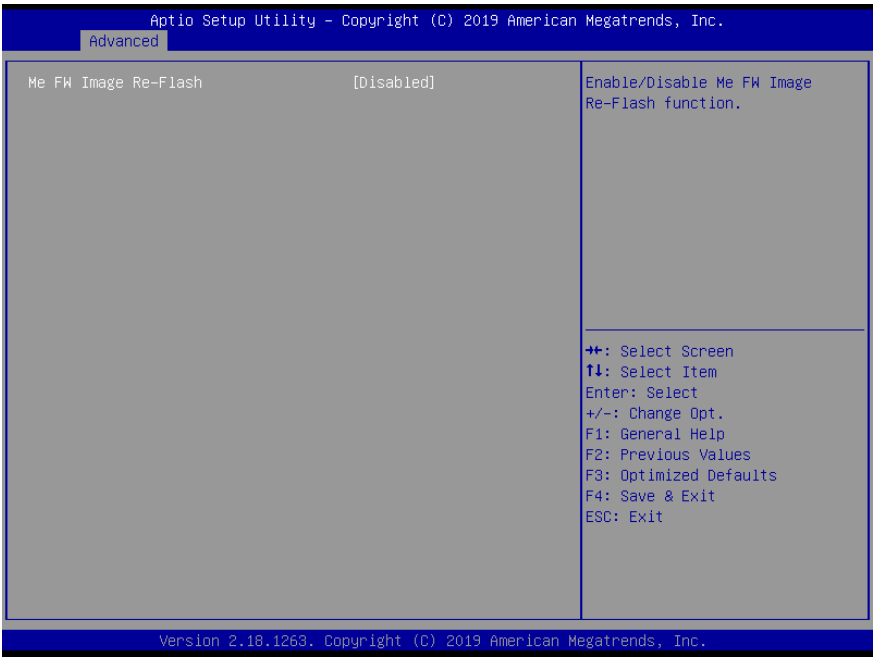
3.4.3 Advanced: SATA Configuration

Options Summary		
SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Device.		
SATA Mode Selection	AHCI Mode	Optimal Default, Failsafe Default
	Intel RST Premium With Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
Port 0/1/2/3	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Port.		
Hot Plug	Enabled	
	Disabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		

3.4.4 Advanced: PCH-FW Configuration

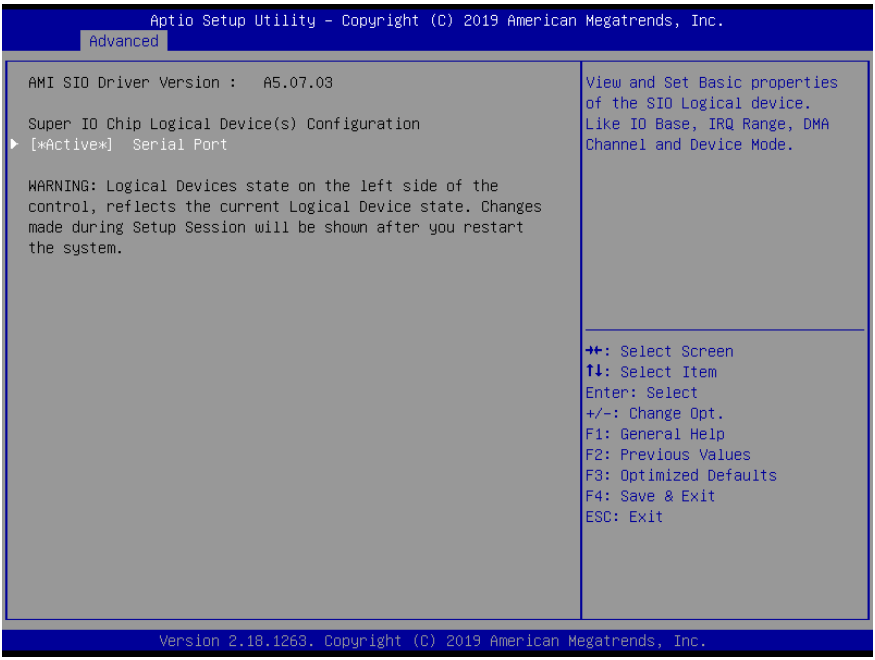


3.4.4.1 Firmware Update Configuration

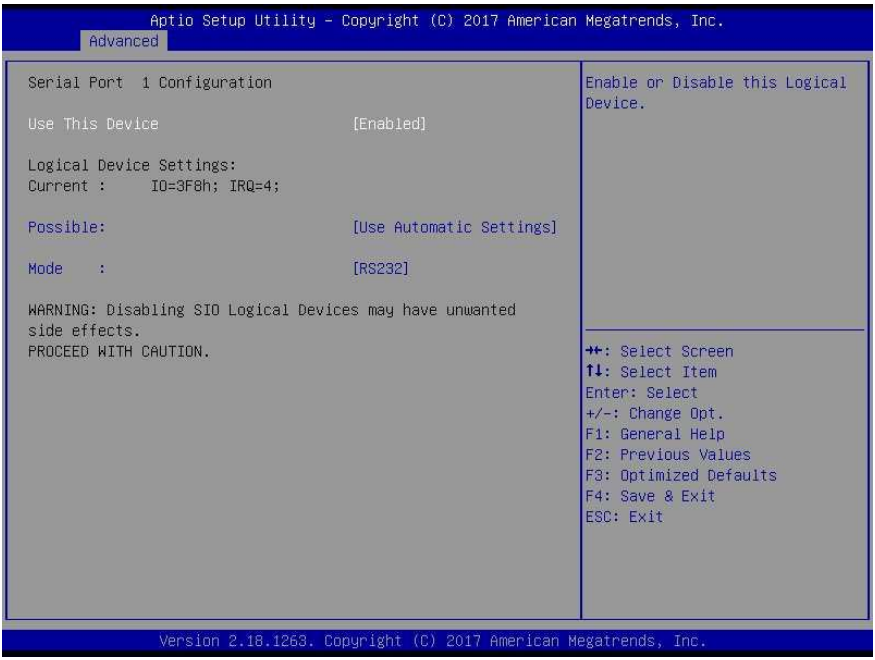


Options Summary		
ME FW Image Re-Flash	Enabled	
	Disabled	Optimal Default, Failsafe Default
Enable or Disable ME FW Image Re-Flash function.		

3.4.5 Advanced: SIO Configuration

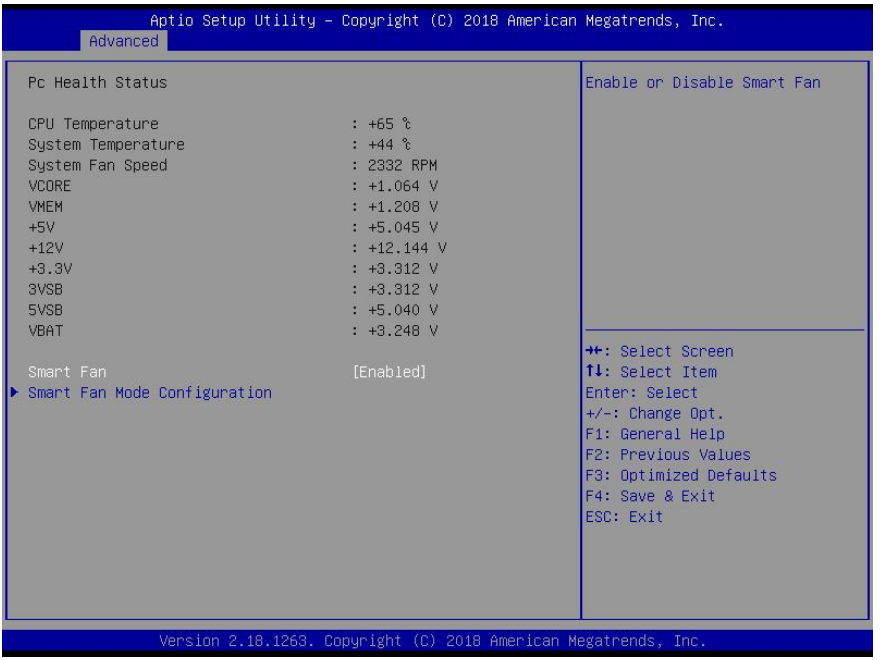


3.4.5.1 Serial Port 1 Configuration



Options Summary		
Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

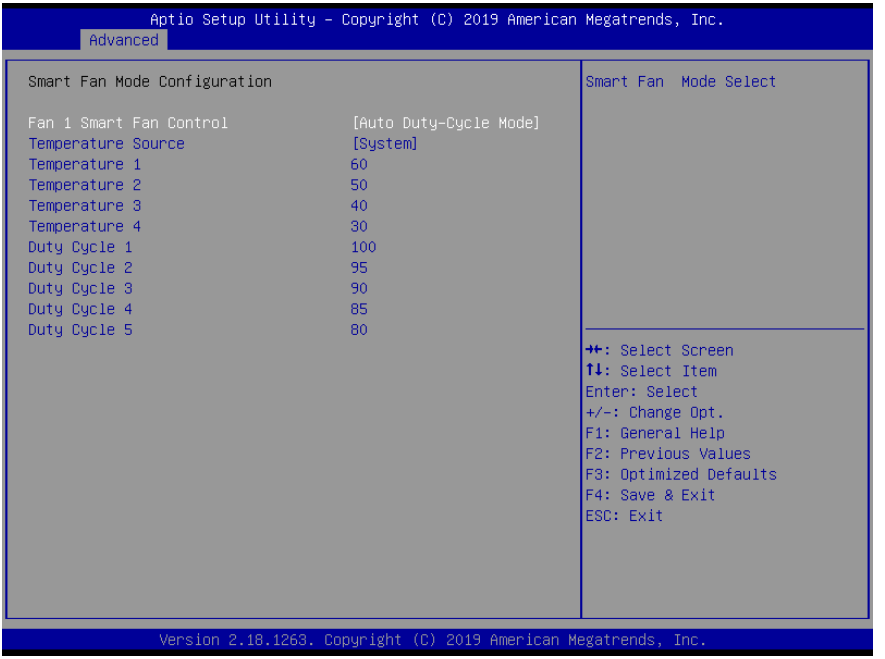
3.4.6 Advanced: Hardware Monitor



Options Summary		
Smart Fan	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Smart Fan		

3.4.6.1 Smart Fan Mode Configuration

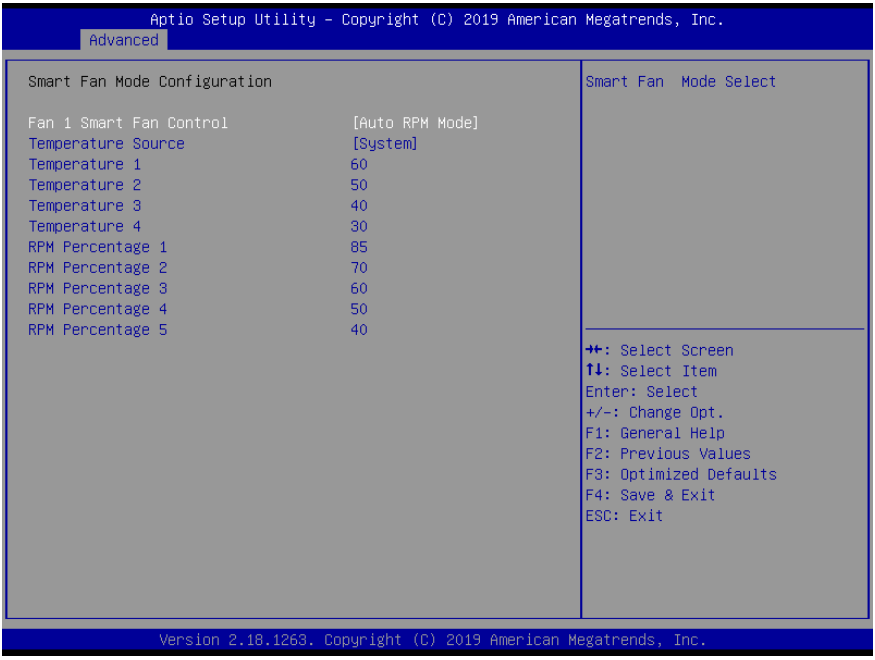
Auto Duty-Cycle Mode



Options Summary		
Fan 1 Smart Fan Control	Manual RPM Mode	
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU	
	System	Optimal Default, Failsafe Default
Select the monitored temperature source for this fan		
Temperature 1/2/3/4	1-100	Range
	60/50/40/30	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		

Options Summary		
Duty Cycle	1-100	Range
1/2/3/4/5	100/95/90/85/80	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		

Auto RPM Mode

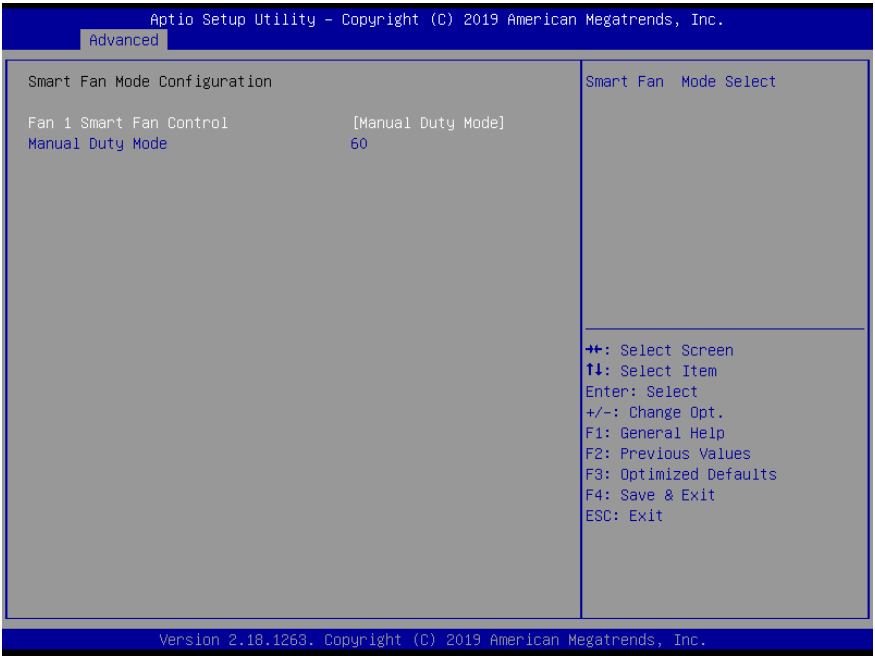


Options Summary		
Fan 1 Smart Fan Control	Manual RPM Mode	
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Temperature Source	CPU	
	System	Optimal Default, Failsafe Default
Select the monitored temperature source for this fan		

Table Continues on Next Page

Options Summary		
Temperature 1/2/3/4	1-100	Range
	60/50/40/30	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different RPM 1-100		
RPM Percentage 1/2/3/4/5	1-100	Range
	85/70/60/50/40	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different RPM cycle 1-100		

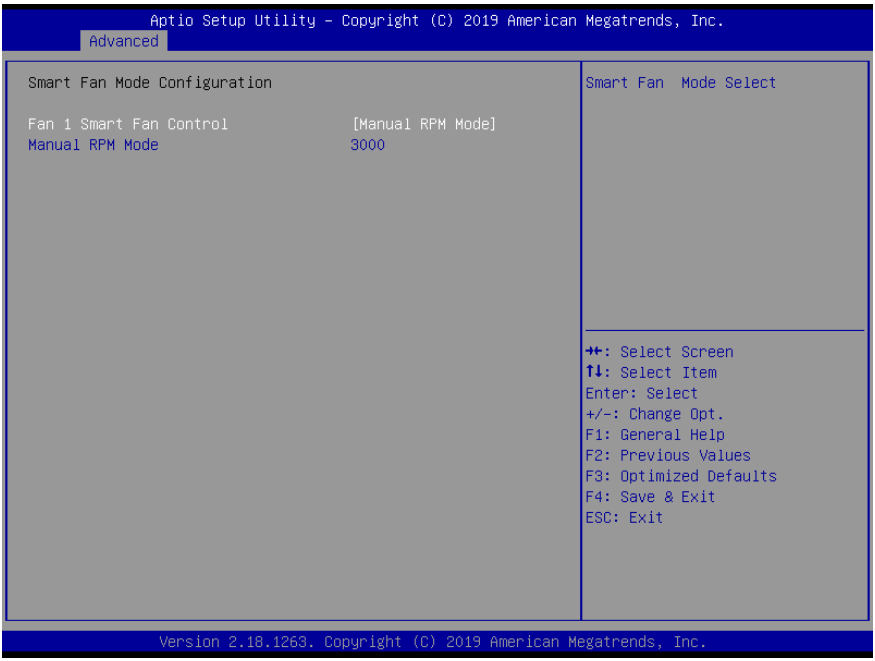
Manual Duty Mode



Options Summary		
Fan 1 Smart Fan Control	Manual RPM Mode	
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		

Options Summary		
Manual Duty	1-100	Range
Mode	60	Optimal Default, Failsafe Default
Manual mode fan control. User can write expected duty cycle(PWM fan type) 1-100		

Manual RPM Mode

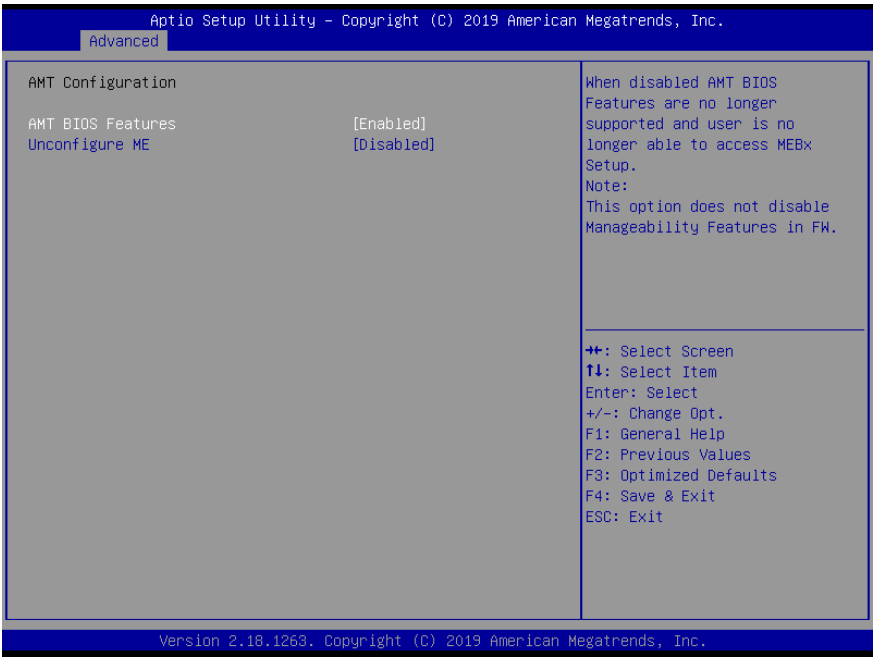


Options Summary		
Fan 1 Smart Fan Control	Manual RPM Mode	
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	Optimal Default, Failsafe Default
Smart Fan Mode Select		
Manual RPM	500-10000	Range
Mode	3000	Optimal Default, Failsafe Default
Manual mode fan control. User can write expected RPM count 500-10000		

3.4.7 Advanced: USB Configuration

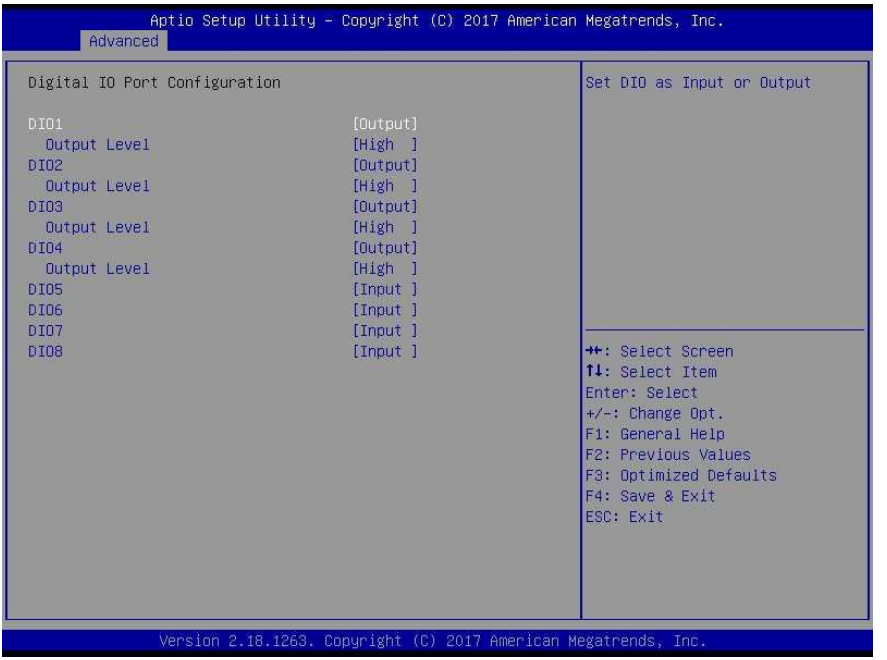
Options Summary		
Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		

3.4.8 AMT Configuration



Options Summary		
AMT BIOS Features	Enabled	Optimal Default, Failsafe Default
	Disabled	
When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx setup. Note: This option does not disable Manageability Features in FW		
Unconfigure ME	Disabled	Optimal Default, Failsafe Default
	Enable	
OEMFlag Bit 15: Unconfigure ME with resetting MEBx password to default		

3.4.9 Advanced: Digital IO Port Configuration

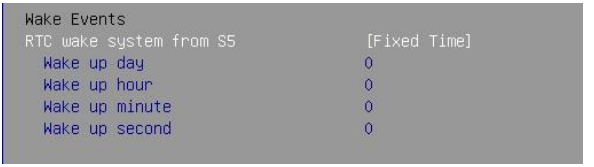


Options Summary		
DIO Type	Output	Optimal Default, Failsafe Default
	Input	
DIO Direction Type Setting		
DIO Data	Low	
	High	Optimal Default, Failsafe Default
DIO Output High/Low Setting		

3.4.10 Advanced: Power Management

Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

RTC: Fixed Time



Options Summary	
RTC wake system from S5	Fixed Time
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified	
Wake up day	0
Select 0 for daily system wake up, 1-31 for which day of the month that you would like the system to wake up	
Wake up hour	0
Select 0-23 For example enter 3 for 3am and 15 for 3pm	
Wake up minute	0
0 - 59	
Wake up second	0
0 - 59	

RTC: Dynamic Time

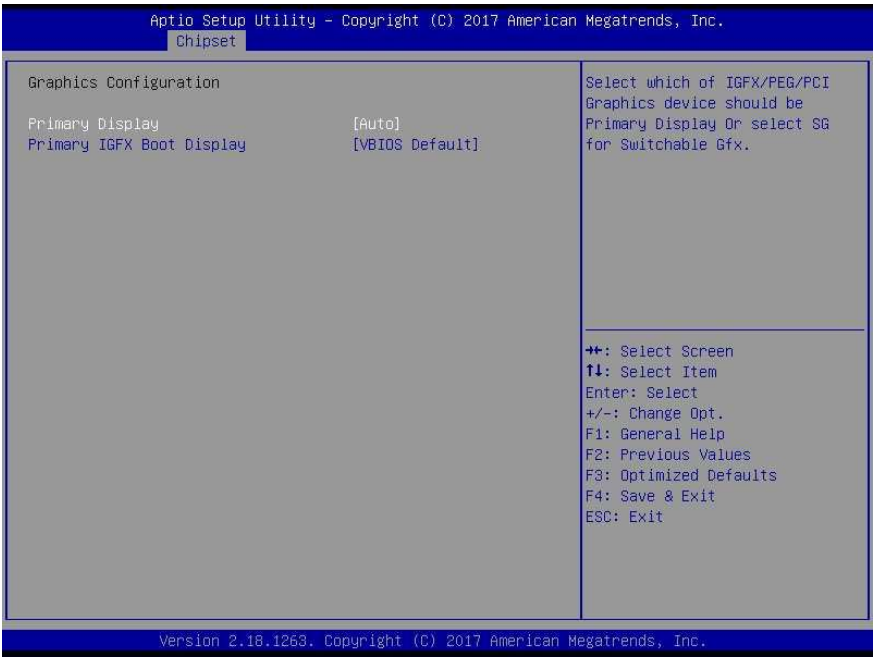
Options Summary	
RTC wake system from S5	Dynamic Time
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified	
Wake up minute increase	1
1-5	

3.5 Setup submenu: Chipset

3.5.1 Chipset: System Agent (SA) Configuration

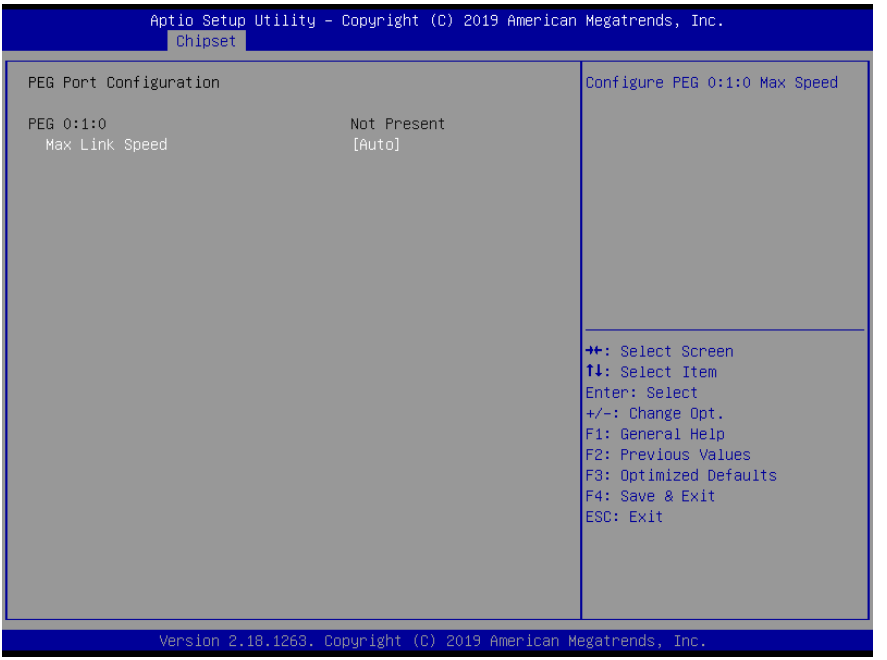
Options Summary		
Max TOLUD	Dynamic	Optimal Default, Failsafe Default
	1 GB	
	1.25 GB	
	1.5 GB	
	1.75 GB	
	2 GB	
	2.25 GB	
	2.5 GB	
	2.75 GB	
	3 GB	
	3.25 GB	
	3.5 GB	
Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.		

3.5.1.1 Graphics Configuration



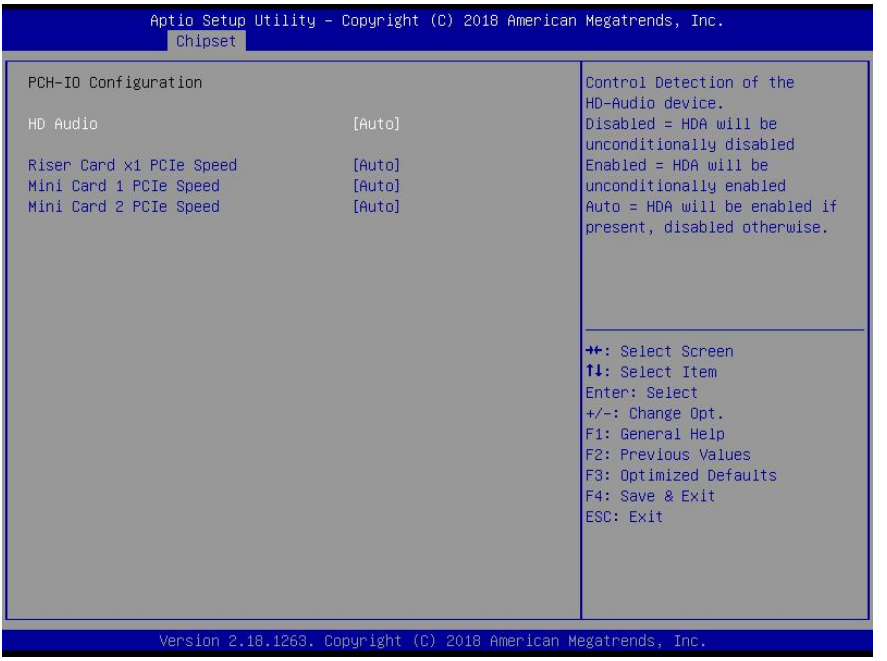
Options Summary		
Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCIE	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Primary IGFX Boot Display	VBIOS default	Optimal Default, Failsafe Default
	HDMI 1	
	HDMI 2	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.		

3.5.2 Chipset: PEG Port Configuration



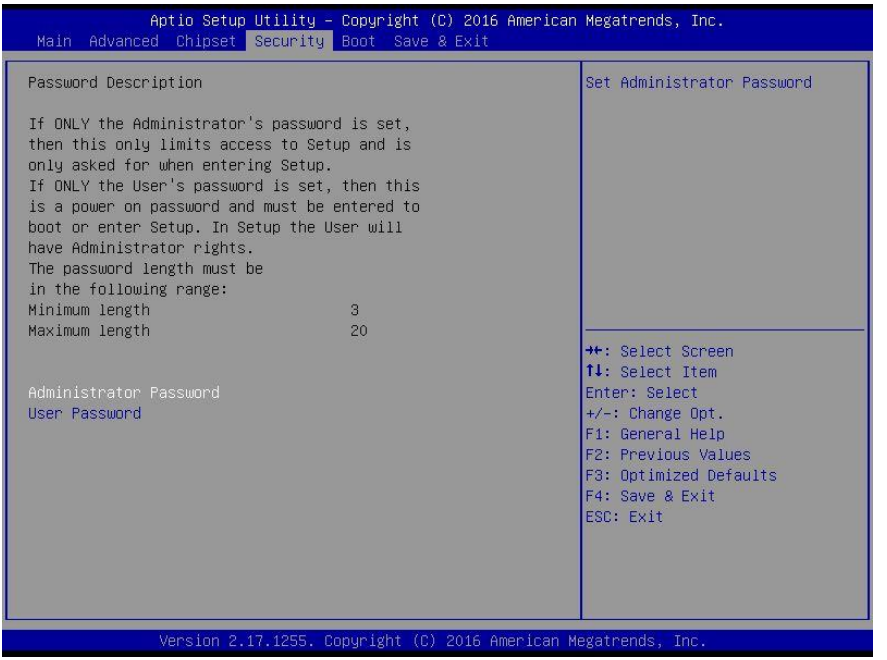
Options Summary		
MAX Link Speed	Gen1	
	Gen2	
	Gen3	
	Auto	Optimal Default, Failsafe Default
Configure PEG Max Speed		

3.5.3 Chipset: PCH-IO Configuration



Options Summary		
HD Audio	Disabled	
	Enabled	
	Auto	Optimal Default, Failsafe Default
Control Detection of the HD-Audio device. Disabled / Enabled = HDA will be unconditionally disabled / enabled Auto = HDA will be enabled if present, disabled otherwise.		
Riser Card x1 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		
Mini-Card 1/2 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		

3.6 Setup submenu: Security



Change User/Administrator Password

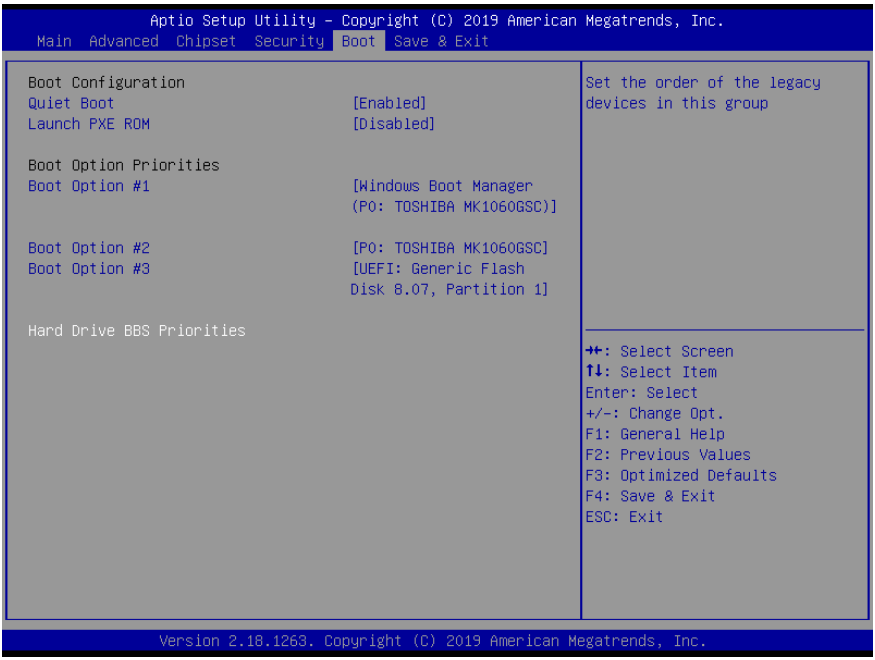
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

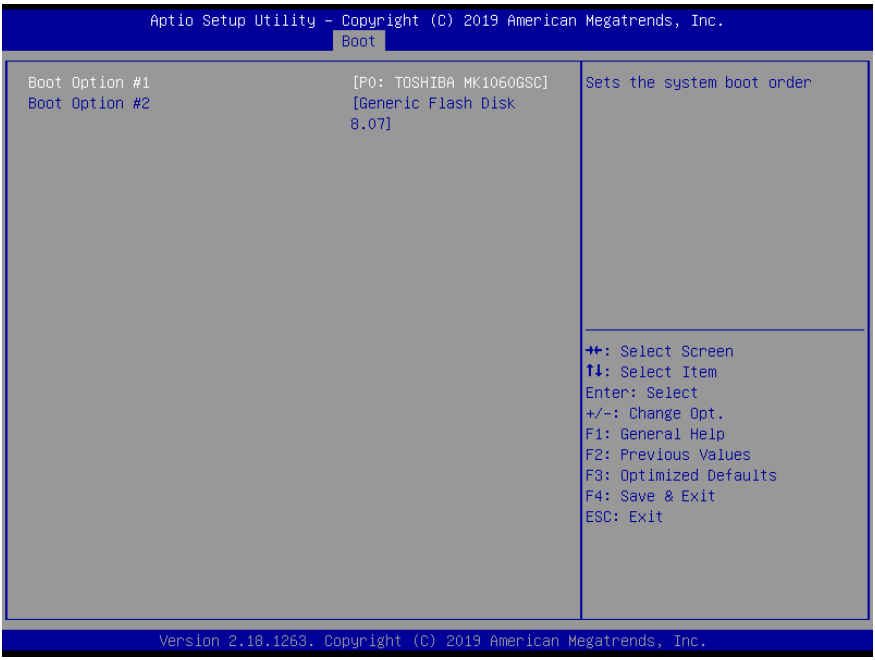
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.7 Setup submenu: Boot

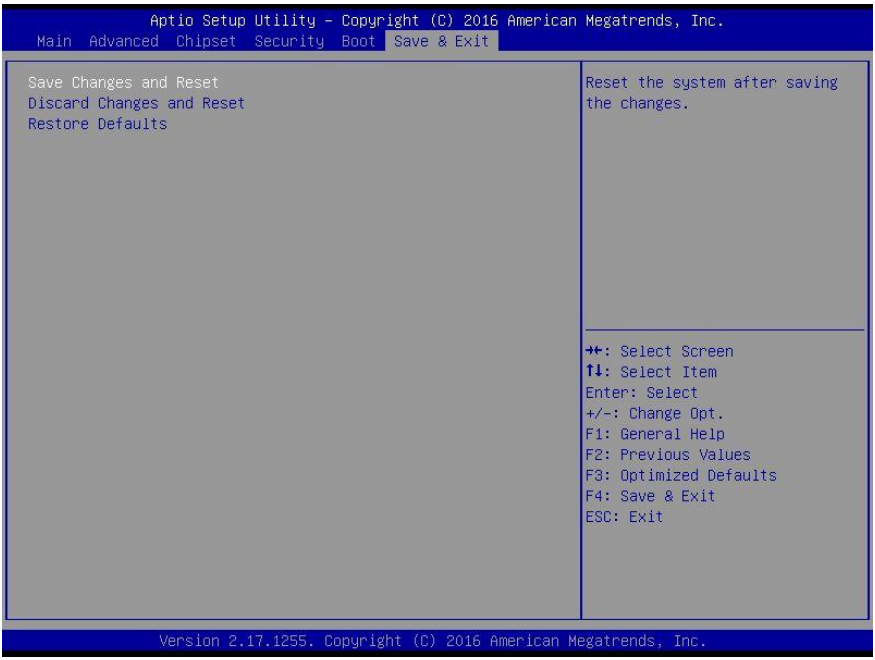


Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or disables Quiet Boot option.		
Launch PXE OpROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		

3.7.1 Boot: BBS Priorities



3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Installation

Drivers for the BOXER-8331AI can be downloaded from the product page on the AAEON website.

Download the driver(s) you need and follow the steps below to install them.

Note: System Driver only supports "Win7 64bit". "Win7 32bit" is not supported.

Step 1 – Install Chipset Driver

1. Open the **Step 1 - Chipset** folder and select the correct chipset and OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **Step 2 - Graphic** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Driver

1. Open the **Step 3 - LAN** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **Step 4 - Audio** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install USB3.0 Driver

1. Open the **Step 5 – USB3.0** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install ME Driver

1. Open the **Step 6 - ME** folder and select the correct chipset and OS
2. Open the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 7 – Install Serial Port Driver

1. Open the **Step 7 - Serial Port Driver (Optional)** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 8 – Install TPM Hotfix Driver

1. Open the **Step 8 – TPM Hotfix (Optional)** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
//*****************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
//*****************************************************************************
```

```
*************************************************************************************
VOID   Main(){
       // Procedure : AaeonWDTConfig
       // (byte)Timer : Time of WDT timer.(0x00~0xFF)
       // (boolean)Unit : Select time unit(0: second, 1: minute).
       AaeonWDTConfig();

       // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
       AaeonWDTEnable();
}
*************************************************************************************
```

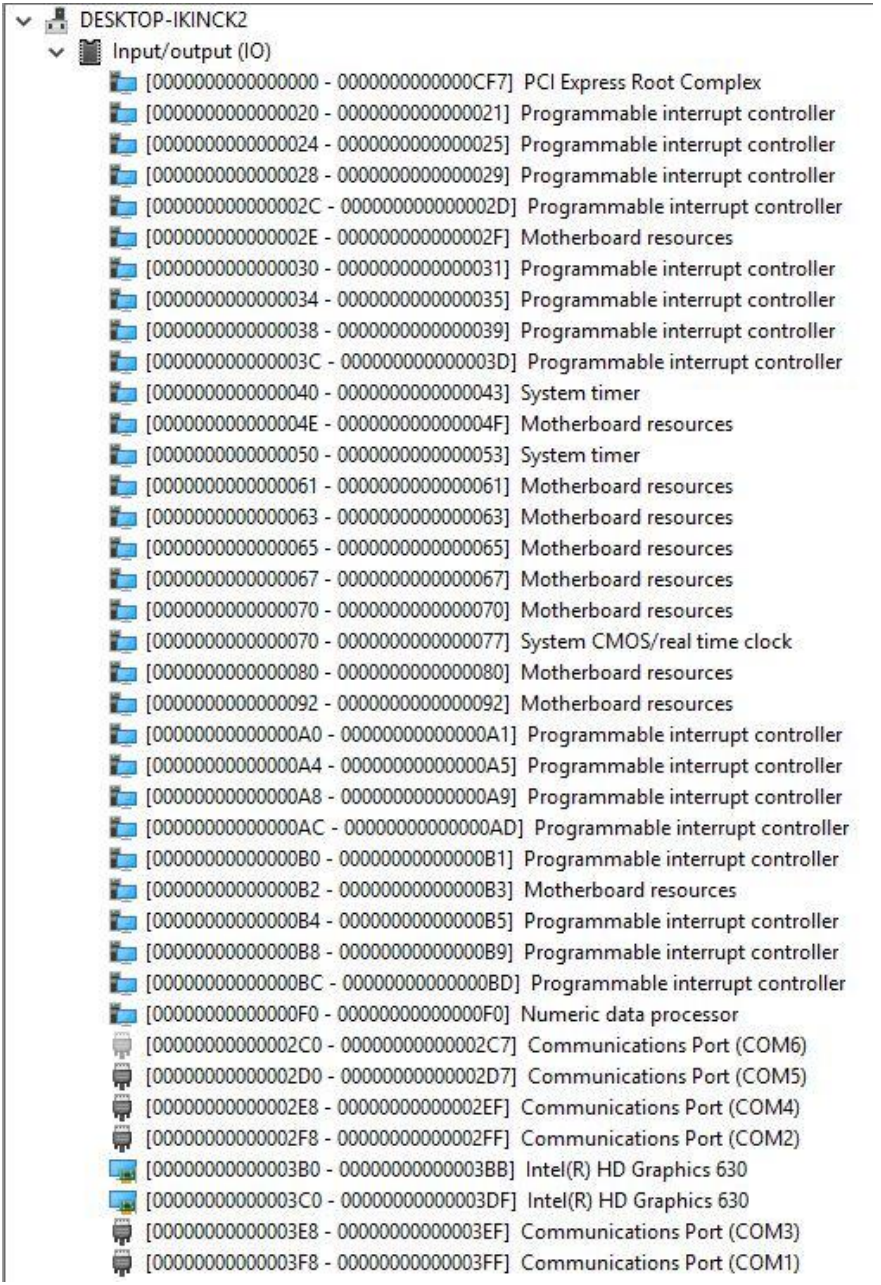
```
*****************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****************************************************************************
```

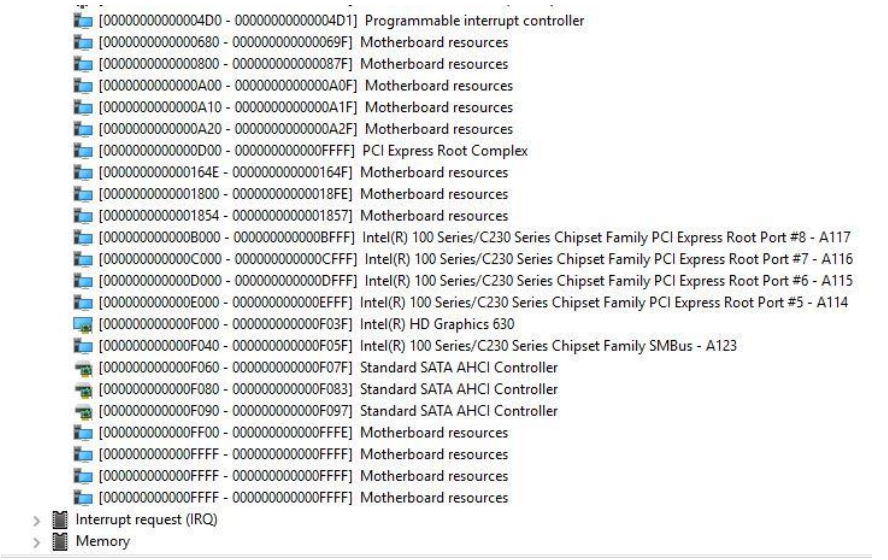
```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

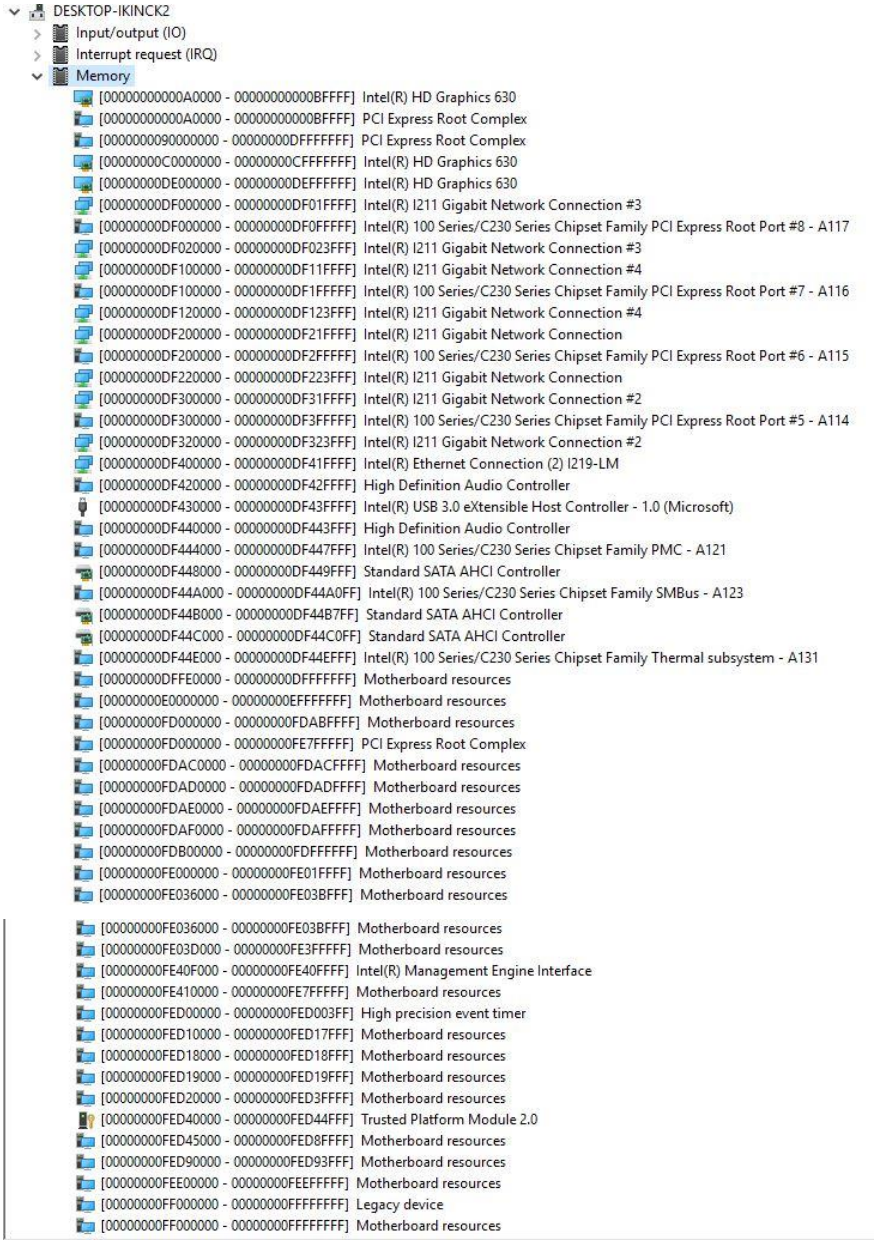
I/O Information

B.1 I/O Address Map

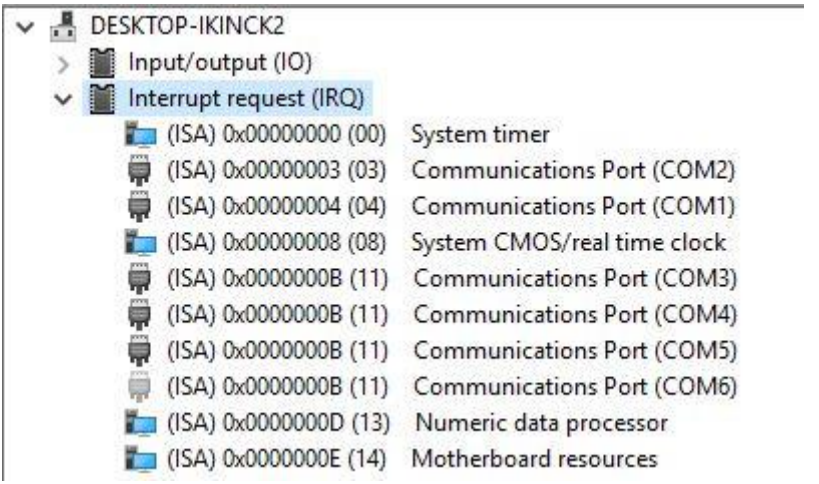



[00000000000004D0 - 00000000000004D1] Programmable interrupt controller
[0000000000000680 - 000000000000069F] Motherboard resources
[0000000000000800 - 000000000000087F] Motherboard resources
[0000000000000A00 - 0000000000000A0F] Motherboard resources
[0000000000000A10 - 0000000000000A1F] Motherboard resources
[0000000000000A20 - 0000000000000A2F] Motherboard resources
[0000000000000D00 - 000000000000FFFF] PCI Express Root Complex
[000000000000164E - 000000000000164F] Motherboard resources
[0000000000001800 - 00000000000018FE] Motherboard resources
[0000000000001854 - 0000000000001857] Motherboard resources
[000000000000B000 - 000000000000BFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #8 - A117
[000000000000C000 - 000000000000CFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #7 - A116
[000000000000D000 - 000000000000DFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #6 - A115
[000000000000E000 - 000000000000EFFF] Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #5 - A114
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics 630
[000000000000F040 - 000000000000F05F] Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
[000000000000FFFF - 000000000000FFFF] Motherboard resources
Interrupt request (IRQ)
Memory

B.2 Memory Address Map



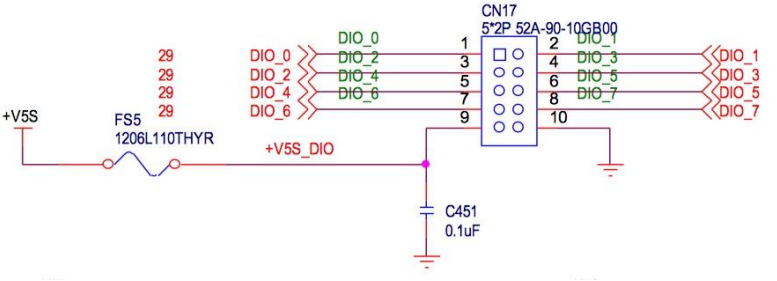
B.3 IRQ Mapping Chart



Appendix C

Electrical Specifications for I/O Ports

C.1 Electrical Specifications for I/O Ports



C.2 DIO Programming

BOXER-8331AI utilizes the FINTEK 81866 chipset as its Digital I/O controller. This section details procedures to complete configuration of the chipset, as well as AAEON initial Watchdog Timer program which can be customized to fit your application.

There are three steps to complete the configuration setup.

Step 1 Enter the MB PnP Mode

Step 2 Modify the data of configuration registers

Step 3 Exit the MB PnP Mode. Undesired results may occur if the MB PnP Mode is not exited normally.

Note: These three steps are the same for programming the Watchdog Timer

C.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A (Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A (Note10)	3(Note11)		GPIO83
DIO-4 Pin Status	0x06(Note12)	0x8A (Note13)	2(Note14)		GPIO82
DIO-5 Pin Status	0x06(Note15)	0x8A (Note16)	5(Note17)		GPIO85
DIO-6 Pin Status	0x06(Note18)	0x8A (Note19)	4(Note20)		GPIO84
DIO-7 Pin Status	0x06(Note21)	0x8A (Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A (Note25)	7(Note26)		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89 (Note32)	1(Note33)	(Note34)	GPIO81

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-3 Output Data	0x06(Note35)	0x89 (Note36)	3(Note37)	(Note38)	GPIO83
DIO-4 Output Data	0x06(Note39)	0x89 (Note40)	2(Note41)	(Note42)	GPIO82
DIO-5 Output Data	0x06(Note43)	0x89 (Note44)	5(Note45)	(Note46)	GPIO85
DIO-6 Output Data	0x06(Note47)	0x89 (Note48)	4(Note49)	(Note50)	GPIO84
DIO-7 Output Data	0x06(Note51)	0x89 (Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89 (Note56)	7(Note57)	(Note58)	GPIO87

C.4 Digital I/O Sample Program

```
//**************************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN   // This parameter is represented from Note3
#define byte   DInput1Reg   // This parameter is represented from Note4
#define byte   DInput1Bit   // This parameter is represented from Note5
#define byte   DInput2LDN   // This parameter is represented from Note6
#define byte   DInput2Reg   // This parameter is represented from Note7
#define byte   DInput2Bit   // This parameter is represented from Note8
#define byte   DInput3LDN   // This parameter is represented from Note9
#define byte   DInput3Reg   // This parameter is represented from Note10
#define byte   DInput3Bit   // This parameter is represented from Note11
#define byte   DInput4LDN   // This parameter is represented from Note12
#define byte   DInput4Reg   // This parameter is represented from Note13
#define byte   DInput4Bit   // This parameter is represented from Note14
#define byte   DInput5LDN   // This parameter is represented from Note15
#define byte   DInput5Reg   // This parameter is represented from Note16
#define byte   DInput5Bit   // This parameter is represented from Note17
#define byte   DInput6LDN   // This parameter is represented from Note18
#define byte   DInput6Reg   // This parameter is represented from Note19
#define byte   DInput6Bit   // This parameter is represented from Note20
#define byte   DInput7LDN   // This parameter is represented from Note21
#define byte   DInput7Reg   // This parameter is represented from Note22
#define byte   DInput7Bit   // This parameter is represented from Note23
#define byte   DInput8LDN   // This parameter is represented from Note24
#define byte   DInput8Reg   // This parameter is represented from Note25
#define byte   DInput8Bit   // This parameter is represented from Note26
//**************************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*******************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //       Example, Read Digital I/O Pin 3 status
        // Output :
        //       InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //       Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
*******************************************************************************
```

```
*****************************************************************************
Boolean   AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID   AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*******************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*******************************************************************************
```