

BOXER-6841M

Fanless Embedded Box PC

User's Manual 1st Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● BOXER-6841M	1
● Wallmount bracket	2
● Screw Package	1
● Thermal Pad Package	1
● Phoenix power connector	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○

○: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注:
一、此产品所标示之环保使用期限, 系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products
 AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○
<p>O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.</p> <p>X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.</p> <p>Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only</p>						

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Chapter 1

Product Specifications

1.1 Specifications

System

- **Processor**
 - Xeon Processor:**
 - Intel® Xeon® E3-1268L v5, 2.40 GHz
 - Intel® Xeon® E3-1275 v6, 3.80 GHz
 - KabyLake Processor:**
 - Intel® Core™ i7-7700T, 2.9 GHz
 - Intel® Core™ i5-7500T, 2.8 GHz
 - Intel® Core™ i3-7101TE, 3.4 GHz
 - SkyLake Processor:**
 - Intel® Core™ i7-6700TE, 2.4 GHz
 - Intel® Core™ i5-6500TE, 2.3 GHz
 - Intel® Core™ i3-6100TE, 2.7 GHz
- **System Memory** DDR4 2133 SODIMM slot x 2, up to 32 GB, ECC or Non-ECC support
- **Display** HDMI x 2
- **Ethernet** Intel® i211AT, 10/100/1000 Base- TX x 4 i219LM, 10/100/1000 Base- TX x 1
- **Storage Device** 2.5" SSD/HDD Bay x 2
- **Serial Port** RS-232/422/485 x 1
- **USB** USB 3.0 x 4
- **Digital I/O** Option for 8 bit (DIO)
- **LED Indicator** Sys LED x 1
HDD LED x 1
- **Expansion Slot** Full-size Mini-Card x 2
SIM Slot x 1 H110 (1PCIe+USB), C236 (2PCIe+USB)

- A1~A4PCIEx[16]*1
 - PCIEx[1]*1
 - A5/A6
 - PCIEx[8]*2
 - PCIEx[1]*1
 - A1/A3
 - PCIEx[16] Slot power total support 180W
 - A2/A4
 - PCIEx[16] Slot power total support 250W
- **OS Support**
 - Windows 10 IOT (64bit)
 - Windows 8.1 (64bit)
 - Windows embedded 8 standard (64bit)
 - Windows 7 (32bit)
 - Windows embedded standard 7 (32/64bit)
 - Ubuntu 16.04 above

Mechanical

- **Construction** Rugged aluminum extrusion and heavy-duty steel
- **Mounting** Wallmount
- **Dimension (W x H x D)**
 - A1-A4 : 6.10" x 7.87" x 15.75" (155mm x 200mm x 400mm)
 - A5/A6 : 6.10" x 7.87" x 10.24" (155mm x 200mm x 260mm)
- **Gross Weight** A1~A4: 14.53 lb (7 Kg) A5~A6: 9.9 lb (4.5 Kg)
- **Net Weight** A1~A4: 18.29 lb (8.3 Kg) A5~A6: 12.75 lb (5.8 kg)

Environmental

- **Operating Temperature** -20°C ~ 55°C according to IEC60068-2 with 0.5m/s airflow
-20°C ~ 45°C according to IEC60068-2 with 0.5m/s airflow
- **Storage Temperature** -45°C ~ 80°C (-49°F ~ 185°F)
- **Storage Humidity** 5~95% @ 40°C, non-condensing
- **Anti-Vibration** HDD-1: Random, 1Grm, 5~500Hz, Anti-vibration design
HDD-2: None
- **EMC** CE/FCC Class A

Power Supply

- **DC Input** A1-A6
(CPU under 65W, No Graphic Card)
3-pin Phoenix DC Input 12~24V 100-240V 120W AC adapter(BOM Optional)
- A2-A4
2 x 3-pin Phoenix DC Input 12V 110/230V 240W AC adapter(BOM Optional)
- A1-A3
3-pin Phoenix DC Input 19.5V 110/240V 330W AC adapter(BOM Optional)

1.2 SKU List

PN	PCH	I/O	PCIe (x16)	PCIe (x8)	PCIe (x1)	Model
BOXER-6841M-A1	H110	4USB3, 5LAN, 1COM, 2HDMI DC12-24V	1	N/A	1	L/Fan
BOXER-6841M-A2	H110		1	N/A	1	L/Fan
BOXER-6841M-A3	C236		1	N/A	1	L/Fan
BOXER-6841M-A4	C236		1	N/A	1	L/Fan
BOXER-6841M-A5	C236		N/A	2	1	S/Fanless
BOXER-6841M-A6	C236	4 Extra RS232 & 1 VGA	N/A	2	1	S/Fanless

Model Key

L/Fan – Long Fan System

S/Fanless – Short Fanless

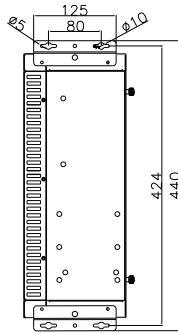
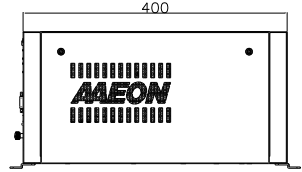
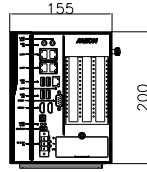
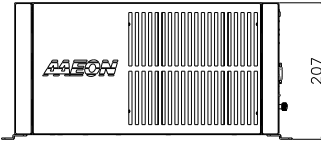
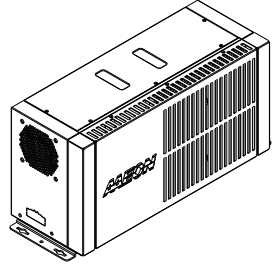
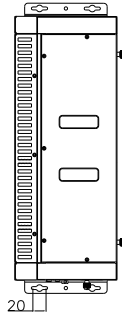
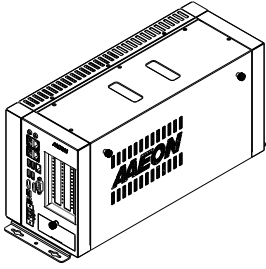
S/Fan – Short Fan System

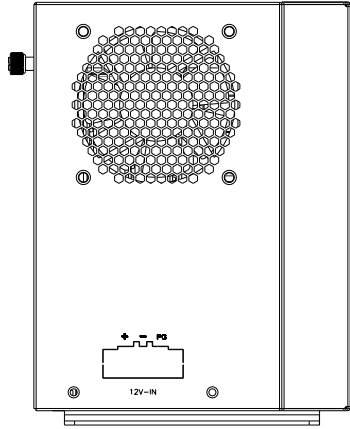
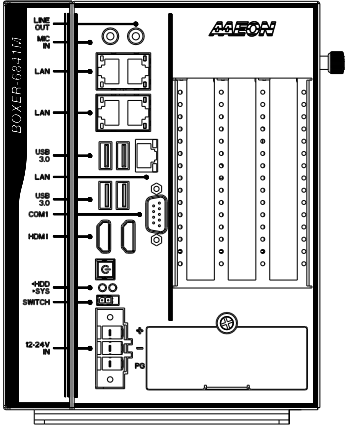
Chapter 2

Hardware Information

2.1 Dimensions

BOXER-6841M-A1(A3)

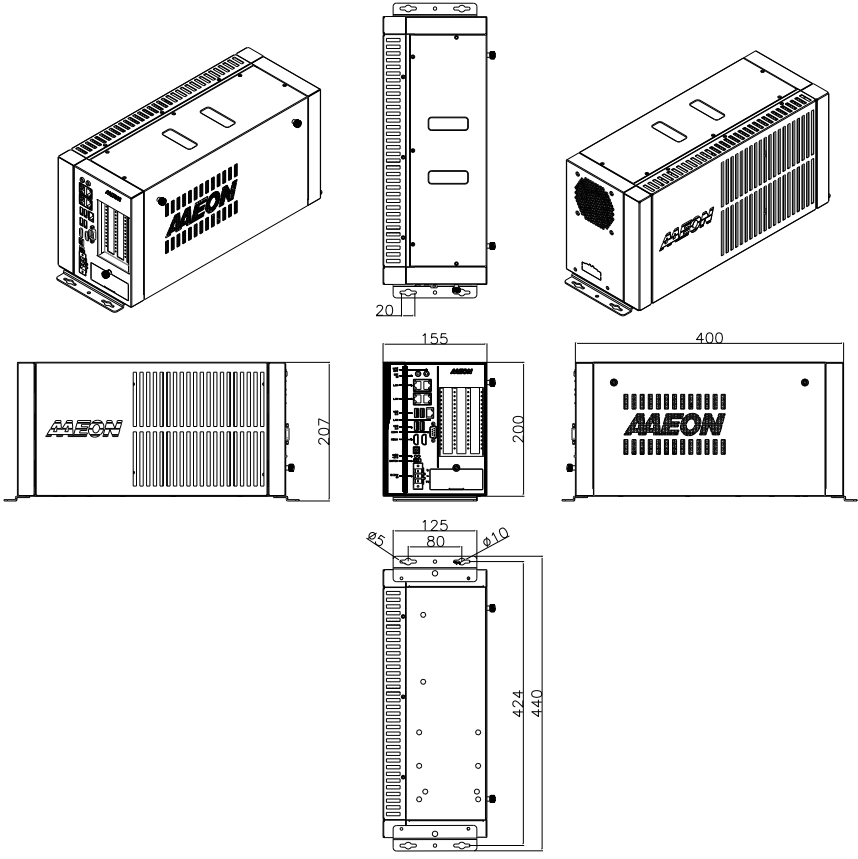


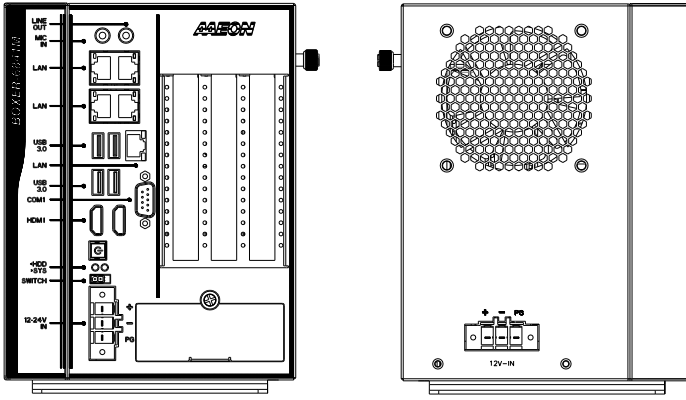


BOXER-6841M-A2(A4)

Fanless Embedded Box PC

BOXER-6841M

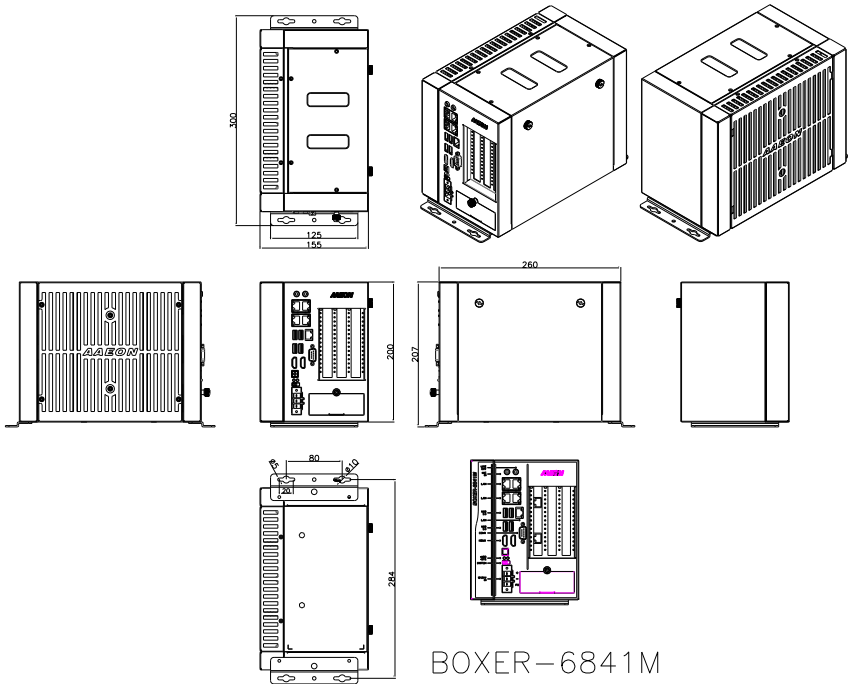




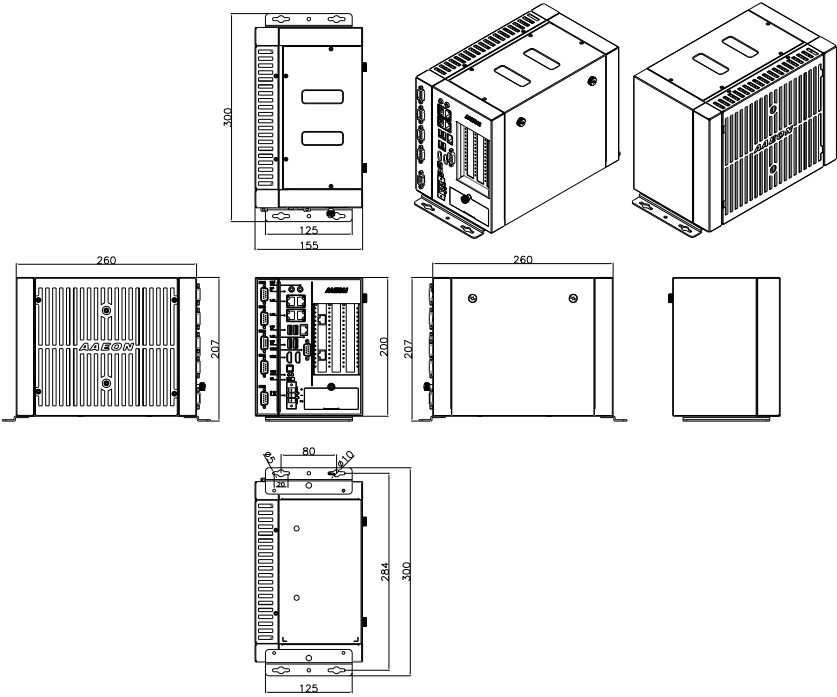
BOXER-6841M-A5

Fanless Embedded Box PC

BOXER-6841M

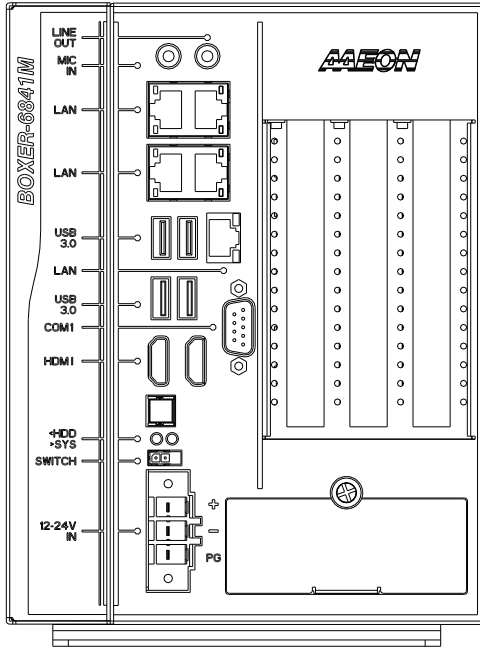


BOXER-6841M-A6

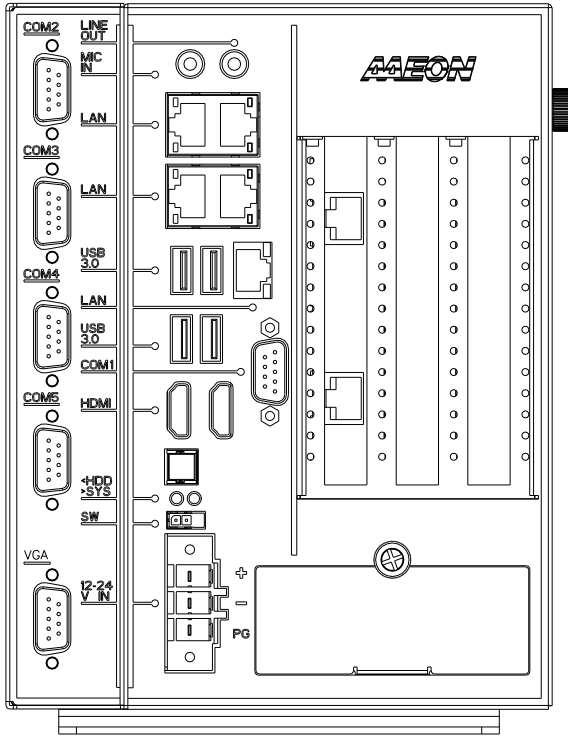


2.1.1 I/O Location

BOXER-6841M-A1~A5



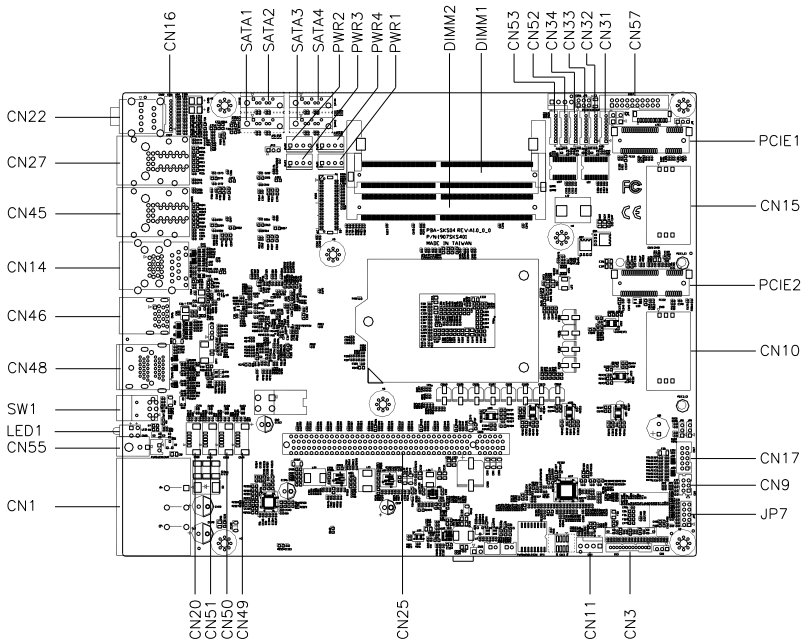
BOXER-6841M-A6



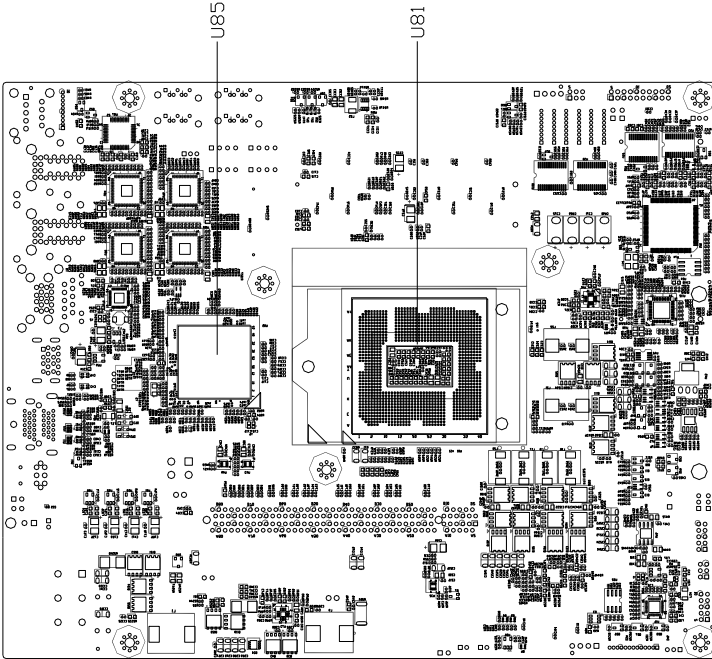
- DOS display in VGA mode, not HDMI mode.

2.2 Jumpers and Connectors

Component Side



Solder Side

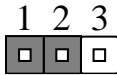


2.3 List of Jumpers

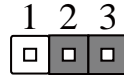
Please refer to the table below for all of the system's jumpers that you can configure for your application.

Label	Function
JP1	Auto Power Button Enable/Disable Selection
JP5	Com1 pin9 function select
JP6	Clear CMOS Jumper
JP8	PEG Lanes CFG6 selection
JP9	PEG Lanes CFG5 selection

2.3.1 Auto Power Button Enable/Disable Selection (JP1)



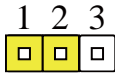
Disable



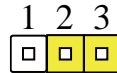
Enable (Default)

※ Disable Auto Power Button JP1(1-2) : Need to use power button JP1(1-2) to power on the system

2.3.2 Clear CMOS Jumper (JP6)



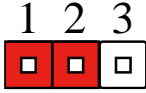
Normal (Default)



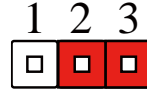
Clear CMOS

2.3.3 PEG Lanes CFG6 / CFG5 Selection (JP8 / JP9)

For 2 x8 PCI Express

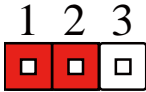


(JP8 1-2)

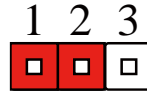


(JP9 2-3)

For 1 x16 PCI Express



(JP8 1-2)



(JP9 1-2)

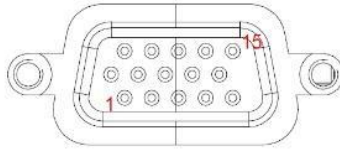
※ PCIE X16 SLOT JUMPER to use 2 X8 riser card or 1x16 riser card.

2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
VGA	D-SUB 15 CRT Port
HDMI1	HDMI Connector
HDMI2	HDMI Connector
USB3.0 Port 1~4	USB 3.0 Port
LAN Port 1~5	RJ45 10/100/1000Bps LAN connector
Audio Jack	3.5mm Audio Line-out/Mac-in Connector
Remote Power Button	2-pin Remote Power On/Off button
Power Switch	Power On/Off Switch
SATA Power Connector 1~2	SATA Storage power Connector
SATA signal Connector 1~2	SATA Storage signal Connector
COM 1	DB9 RS232/485/422 CONNECTOR
COM 2/3/4/5	DB9 RS232 CONNECTOR
Mini Card 1-2	Mini-PCIE Slot
SIM Slot	SIM card connector
DDR4 SODIMM SLOT 1~2	DDR4 260-pin memory Slot

2.4.1 VGA Port



Pin	Pin name	Signal Type	Signal Level
1	RED		
2	GREEN		
3	BLUE		
4	GND		
5	GND		
6	GND		
7	GND		
8	GND		
9	VGA_VCC		
10	GND		
11	NC		
12	DDC_DATA		
13	VGA_HSYNC		
14	VGA_VSYNC		
15	DDC_CLK		

2.4.2 SIM Slot

Pin	Pin name	Signal Type	Signal Level
1	UIM_PWR	PWR	
2	UIM_RST	IN	
3	UIM_CLK	IN	
4	GND	GND	
5	UIM_VPP	PWR	
6	UIM_DATA	I/O	

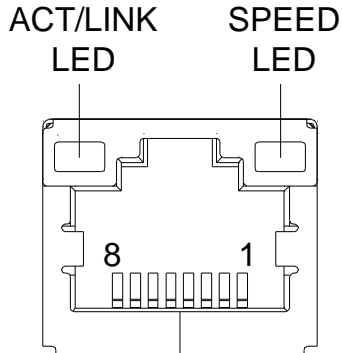
2.4.3 CPU FAN Socket

Pin	Pin name	Signal Type	Signal Level
1	GND	GND	
2	+VCC_FAN_CPU_CON	PWR	12V
3	FAN_TAC_CPU_CON		
4	FAN_CTL_CPU_CON		

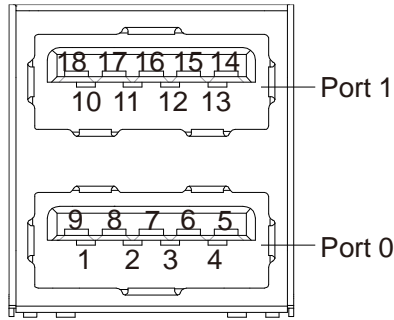
2.4.4 SPI Port

Pin	Pin name	Signal Type	Signal Level
1	SPI_MISO	OUT	
2	GND	GND	
3	SPI_CLK	IN	
4	+3.3VSB	PWR	+3.3V
5	SPI_MOSI	IN	
6	SPI_CS	IN	
7	NC		

2.4.5 LAN (RJ-45)+DUAL USB3.0



Pin	Pin name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

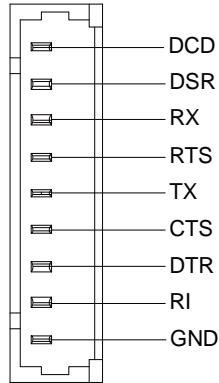


Pin	Pin name	Signal Type	Signal Level
1	+5VSB	PWR	+5V
2	USB0_D-	DIFF	
3	USB0_D+	DIFF	
4	GND	GND	
5	USB0_SSRX-	DIFF	
6	USB0_SSRX+	DIFF	
7	GND	GND	
8	USB0_SSTX-	DIFF	
9	USB0_SSTX+	DIFF	
10	+5VSB	PWR	+5V
11	USB1_D-	DIFF	
12	USB1_D+	DIFF	
13	GND	GND	
14	USB1_SSRX-	DIFF	
15	USB1_SSRX+	DIFF	
16	GND	GND	
17	USB1_SSTX-	DIFF	
18	USB1_SSTX+	DIFF	

2.4.6 PCIe16 Port

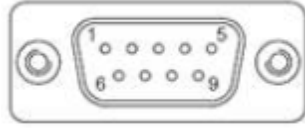
Standard specification

2.4.7 COM1 (Wafer Box, Optional)



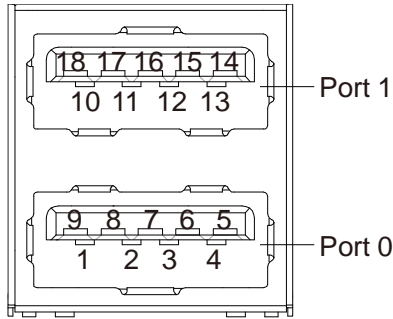
Pin	Pin name	Signal Type	Signal Level
1	DCD1	IN	
2	DSR1	IN	
3	RX1	IN	
4	RTS1	OUT	±9V
5	TX1	OUT	±9V
6	CTS1	IN	
7	DTR1	OUT	±9V
8	RI1	IN	
9	GND	GND	

2.4.8 COM1 DB9 connector



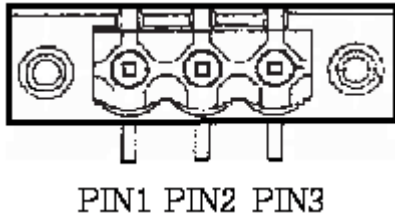
Pin	RS232	RS422	RS485
1	DCD	TX-	D-
2	RXD	TX+	D+
3	TXD	RX+	NC
4	DTR	RX-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.9 DUAL USB3.0



Pin	Pin name	Signal Type	Signal Level
U1	+5VSB	PWR	+5V
U2	USB0_D-	DIFF	
U3	USB0_D+	DIFF	
U4	GND	GND	
U5	USB0_SSRX-	DIFF	
U6	USB0_SSRX+	DIFF	
U7	GND	GND	
U8	USB0_SSTX-	DIFF	
U9	USB0_SSTX+	DIFF	
U10	+5VSB	PWR	+5V
U11	USB1_D-	DIFF	
U12	USB1_D+	DIFF	
U13	GND	GND	
U14	USB1_SSRX-	DIFF	
U15	USB1_SSRX+	DIFF	
U16	GND	GND	
U17	USB1_SSTX-	DIFF	
U18	USB1_SSTX+	DIFF	

2.4.10 DC-IN CONNECTOR

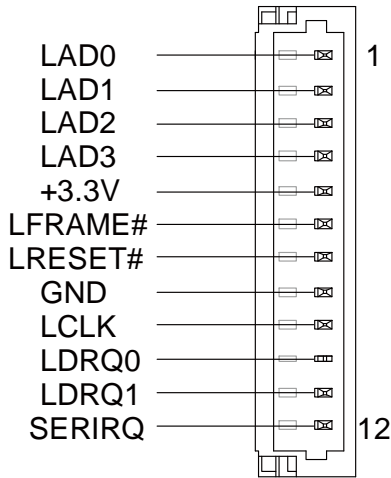


Pin	Pin name	Signal Type	Signal Level
1	VIN	PWR	+12V~+24V
2	GND	GND	
3	GND_EARTH	GND	

2.4.11 COM2/3/4/5

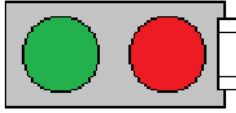
Pin	RS232	RS422	RS485
1	DCD	NC	NC
2	RXD	NC	NC
3	TXD	NC	NC
4	DTR	NC	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.12 LPC Port



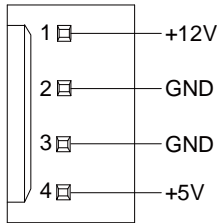
Pin	Pin name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.4.13 PWR LED/HDD LED



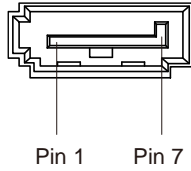
Pin	Pin name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	HDD_LED-		
3	+5V	PWR	+5V
4	PWR_LED-		

2.4.14 SATA Power connector 1~2



Pin	Pin name	Signal Type	Signal Level
1	+12V	PWR	+12V
2	GND	GND	
3	GND	GND	
4	+5V	PWR	+5V

2.4.15 SATA Signal connector 1~2



Pin	Pin name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

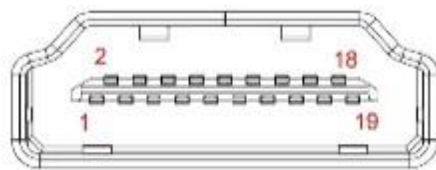
2.4.16 Mini-Card Slot (Full-Mini Card)

Pin	Pin name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	N/A
8	UIM_PWR	PWR	
9	GND	GND	
10	UIM_DATA	I/O	

11	PCIE_REF_CLK-	DIFF	N/A
12	UIM_CLK	IN	
13	PCIE_REF_CLK+	DIFF	N/A
14	UIM_RST	IN	
15	GND	GND	
16	UIM_VPP	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	N/A
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	N/A
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	N/A
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	N/A
34	GND	GND	
35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	

39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.4.17 HDMI Port



Pin	Pin name	Signal Type	Signal Level
1	HDMI_DATA2_P	IN	
2	GND	PWR	
3	HDMI_DATA2_N		
4	HDMI_DATA1_P	GND	
5	GND		
6	HDMI_DATA1_N	PWR	

7	HDMI_DATA0_P	IN
8	GND	PWR
9	HDMI_DATA0_N	GND
10	HDMI_CLK_P	I/O
11	GND	DIFF
12	HDMI_CLK_N	IN
13	NC	DIFF
14	NC	IN
15	HDMI_SCL	GND
16	HDMI_SDA	PWR
17	GND	
18	HDMI_PWR	GND
19	HDMI_HDP	

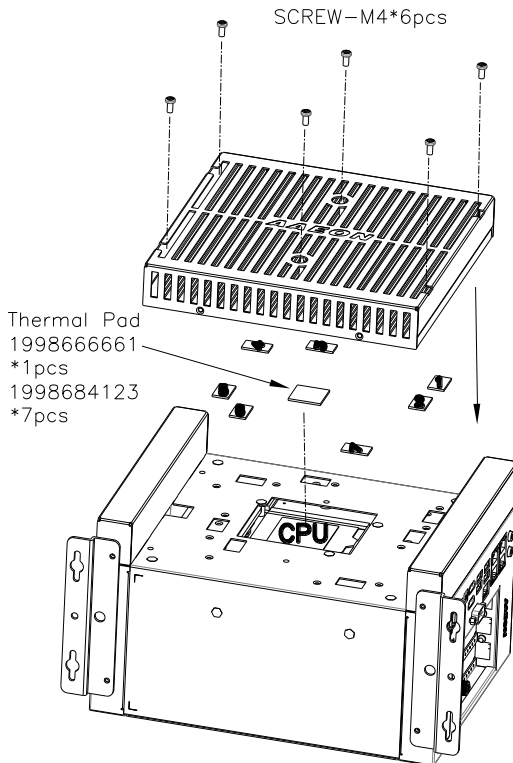
2.5 CPU Installation

Step 1: Turn off the system, unplug the power cord and make sure the system is off.

Step 2: Have Intel KabyLake/Skylake/Xeon FCLGA1151 Processor (Max. TDP 35W – KabyLake/Skylake; 73W – Xeon) ready.



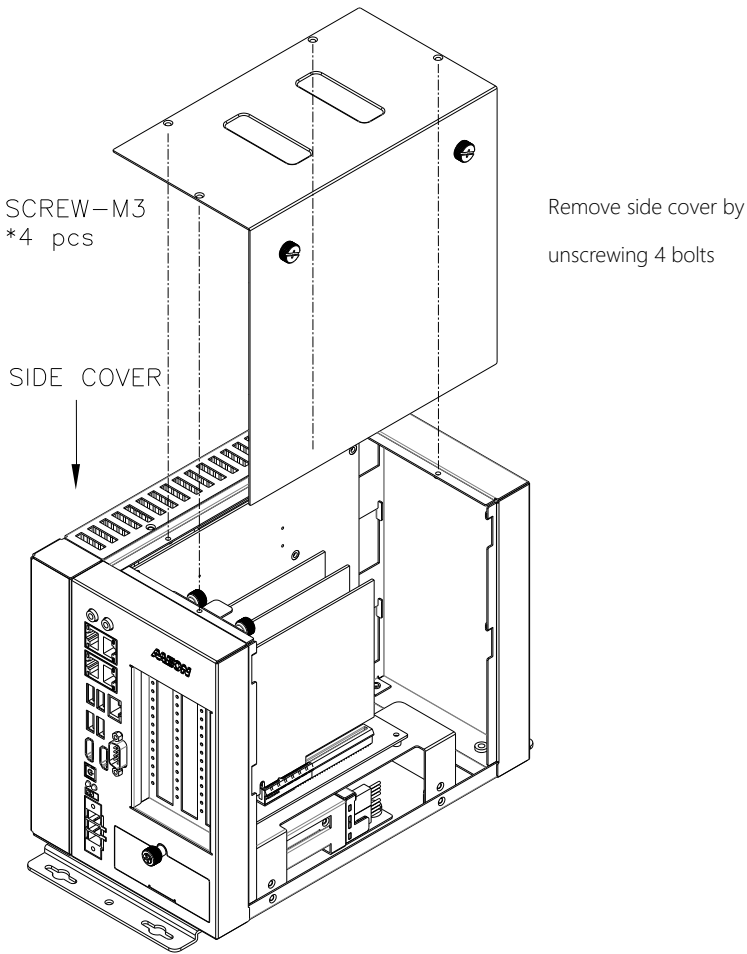
Step 3: Install the CPU into the socket and place the thermal pad onto it.



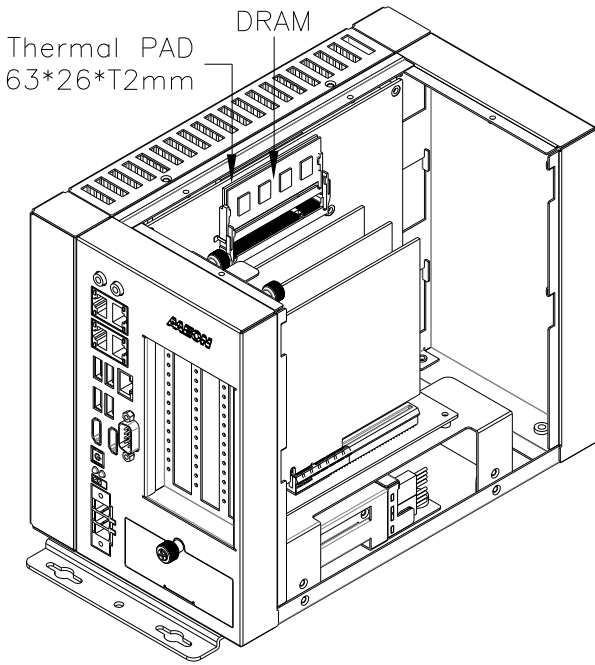
2.6 DDR4 Memory Module Installation

- Turn off the system, unplug the power cord to make sure the system is power off.

Step 1: Remove the screws as instructed below and remove the heatsink.



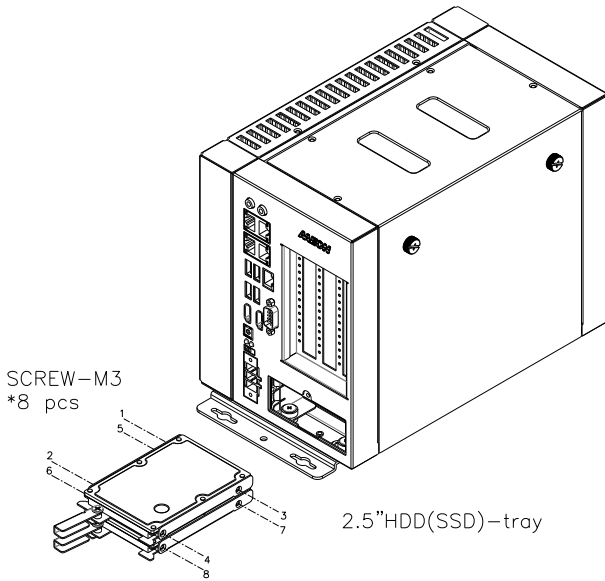
Step 2: Place the thermal pads onto the RAM modules as instructed below.



2.7 2.5" SATA Drive Installation

Turn off the system, unplug the power cord to make sure the system is power off.

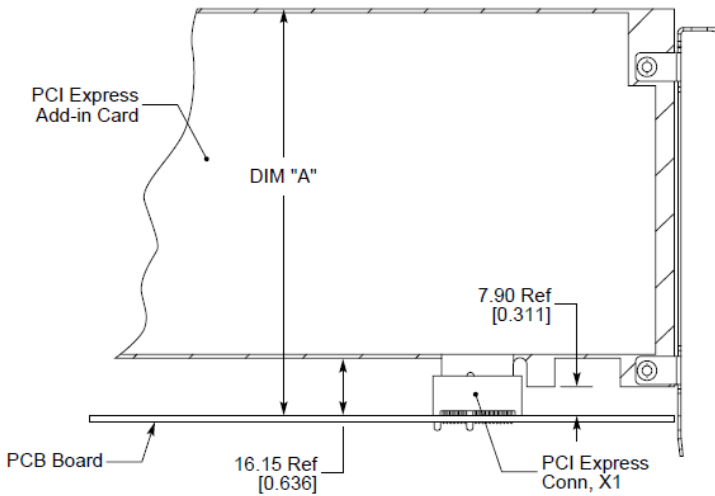
Use the HDD screws provided to assemble 2.5" SATA drive with the HDD Bracket.



2.8 Graphic Card Installation

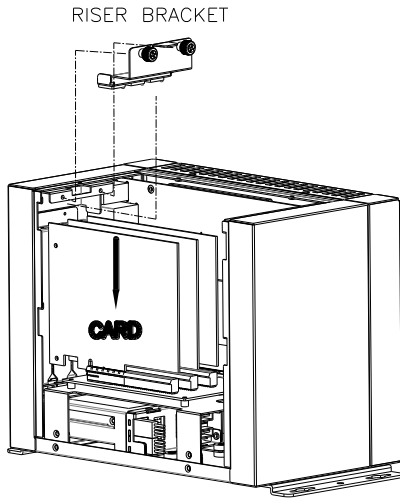
BOXER-6841M-A1 to A4 SKUs support PCIe[x16] graphic card standard high at 114.55mm as below. Length should be under 350mm.

BOXER-6841M-A5 and A6 SKUs support PCIe[x8] extension card standard high at 114.55mm as below. Length should be under 192mm.

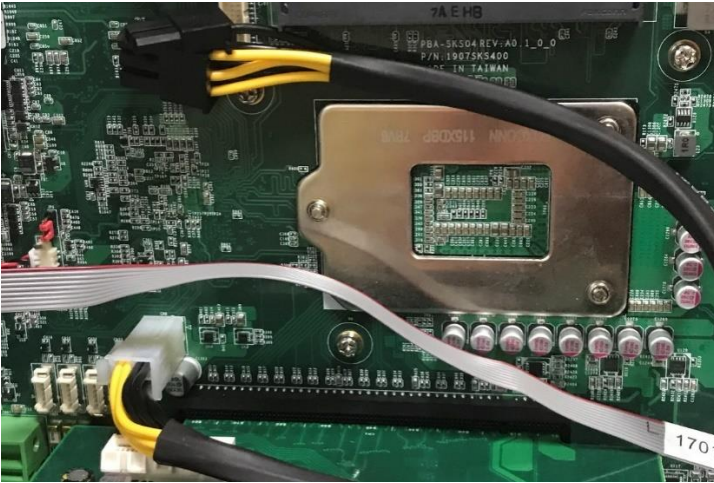


DIM "A"	
STANDARD HEIGHT	114.55 [4.510] MAX.
LOW PROFILE	72.30 [2.846] MAX.

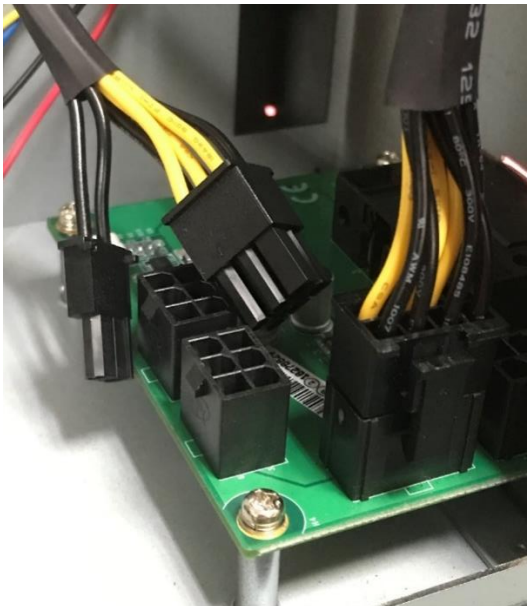
**Lock the extension card with the RISER BRACKET.



For SKU BOXER-6841M-A1/A3, Graphic Card max support 180W, please connect graphic card to power connector cable 1.

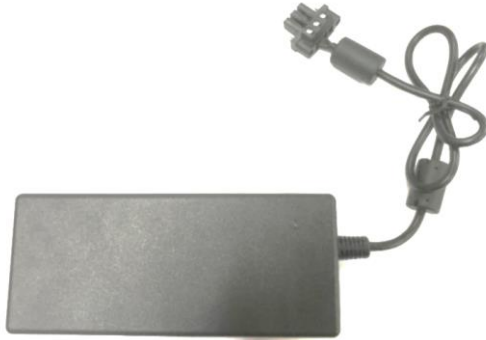


For SKU BOXER-6841M-A2/A4 , Graphic Card max support 250W, require dual power adapter to provide up to 400W power, please connect graphic card to power cable 1 and power cable 2.



250W Graphic need an extra power board and special power sequence
Please follow the power-up steps below

1. Insert 12V-240W adaptor Graphic power input



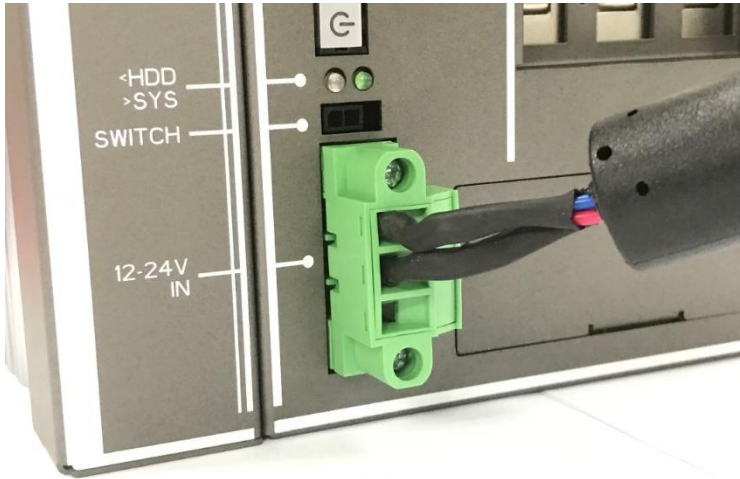
2. Turn on the 12V adaptor



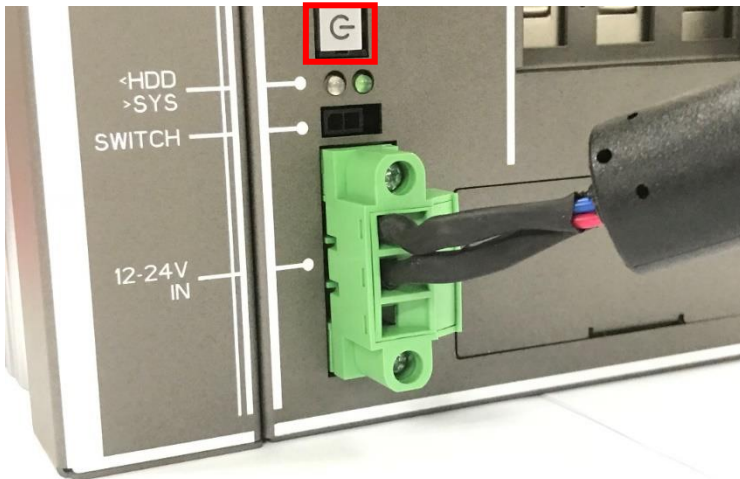
3. Check the 12V adaptor indicator LED is blue



4. Insert 12V-24V adaptor system power input



5. Switch on the system and you will see screen on the monitor



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

Security – The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main

Apdio Setup Utility - Copyright (C) 2018 American Megatrends, Inc.

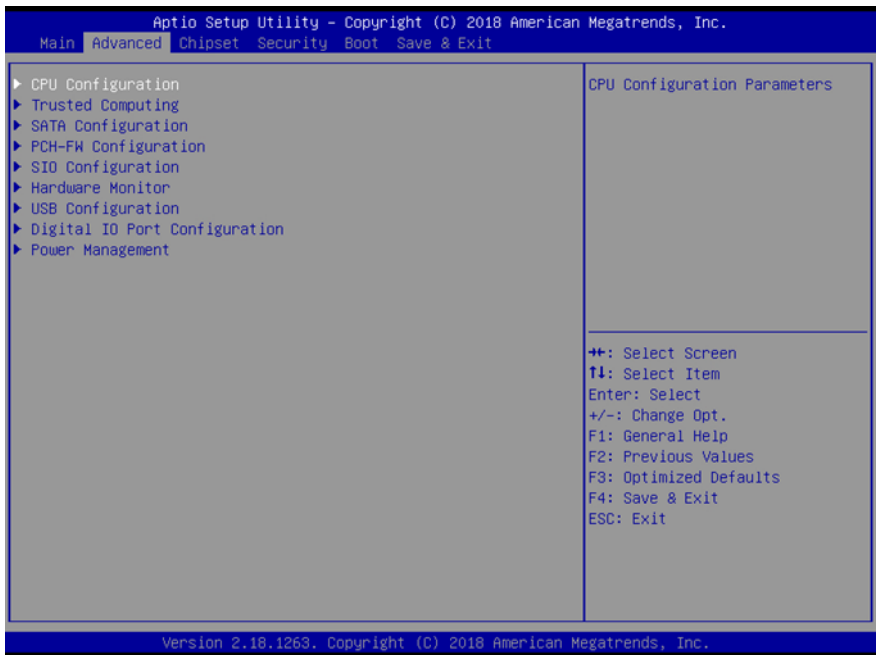
Main Advanced Chipset Security Boot Save & Exit

BIOS Information BOXER-6841M R1.0 (B841CM10) (09/11/2018)		Set the Date. Use Tab to switch between Date elements.
BIOS Vendor	American Megatrends	
Compliance	UEFI 2.6; PI 1.4	
System Date	[Thu 01/01/2009]	
System Time	[00:14:47]	
Access Level	Administrator	

++: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.18.1263. Copyright (C) 2018 American Megatrends, Inc.

3.4 Setup Submenu: Advanced



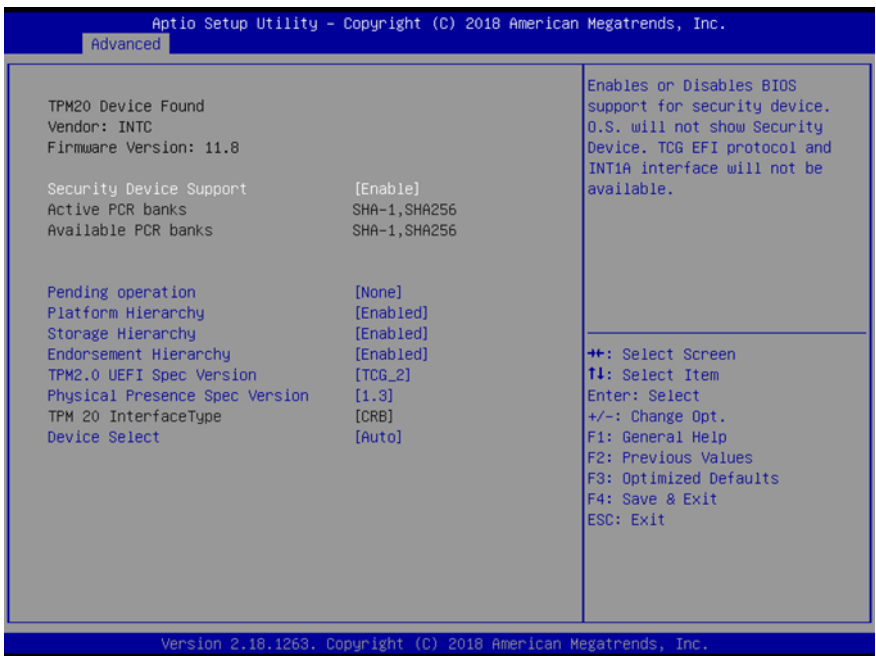
3.4.1 Advanced: CPU Configuration



Options summary:

Hyper-Threading	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology).		
Intel (VMX) Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
Active Processor Cores	1	
	All	Optimal Default, Failsafe Default
Number of cores to enable in each processor package.		

3.4.2 Advanced: Trusted Computing



Options summary:

Security Device Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
SHA-1 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SHA256 PCR Bank		
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		
Platform Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	

Enable or Disable Platform Hierarchy		
Storage Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Storage Hierarchy		
Endorsement Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Endorsement Hierarchy		
TPM2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCG2 Spec Version Support TCG_1_2: the Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later		
Physical Presence Spec Version	1.3	Optimal Default, Failsafe Default
	1.2	
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
TPM 20 InterfaceType	CRB	Optimal Default, Failsafe Default
	TIS	
Select the Communication Interface to TPM 20 Device.		
Device Select	Auto	Optimal Default, Failsafe Default
	TPM 1.2	
	TPM 2.0	
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

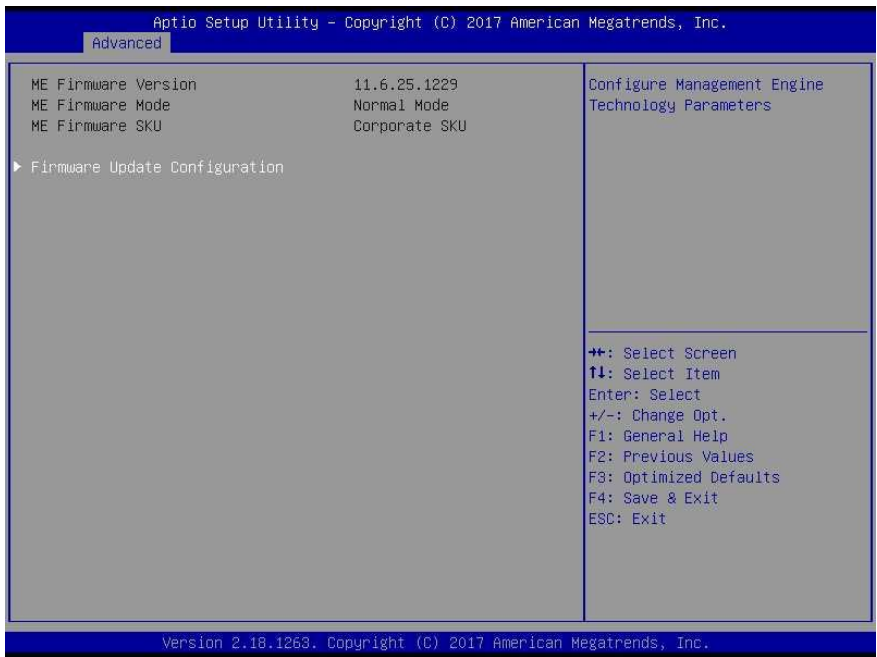
3.4.3 Advanced: SATA Configuration



Options summary:

SATA Controller(s)	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Device.		
SATA Mode Selection	AHCI Mode	Optimal Default, Failsafe Default
	Intel RST Premium With Intel Optane System Acceleration	
Determines how SATA controller(s) operate.		
Port 0/1/2/3	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable SATA Port.		
Hot Plug	Enabled	
	Disabled	Optimal Default, Failsafe Default
Designates this port as Hot Pluggable.		

3.4.4 Advanced: PCH-FW Configuration



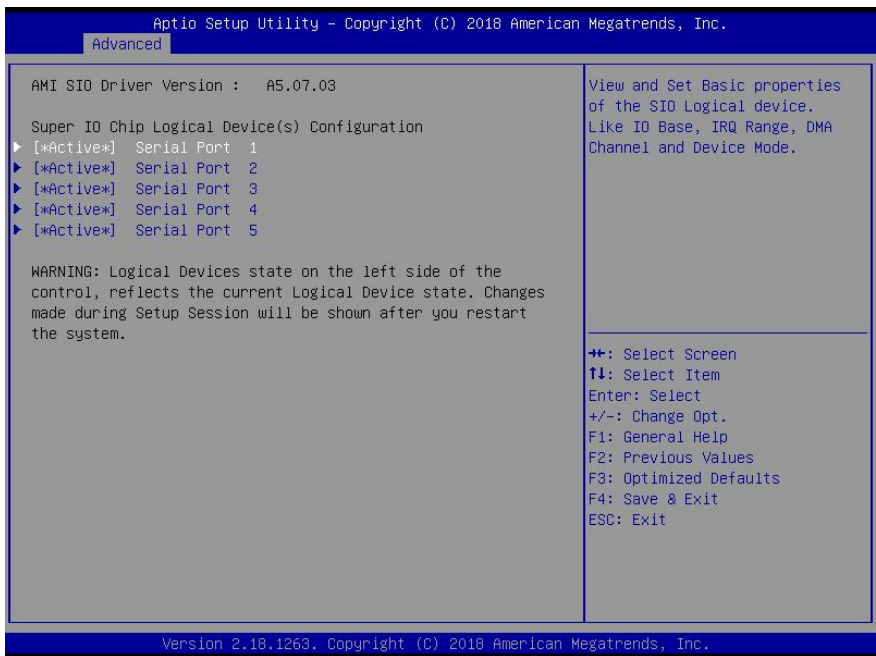
3.4.4.1 PCH-FW Configuration: Firmware Update Configuration



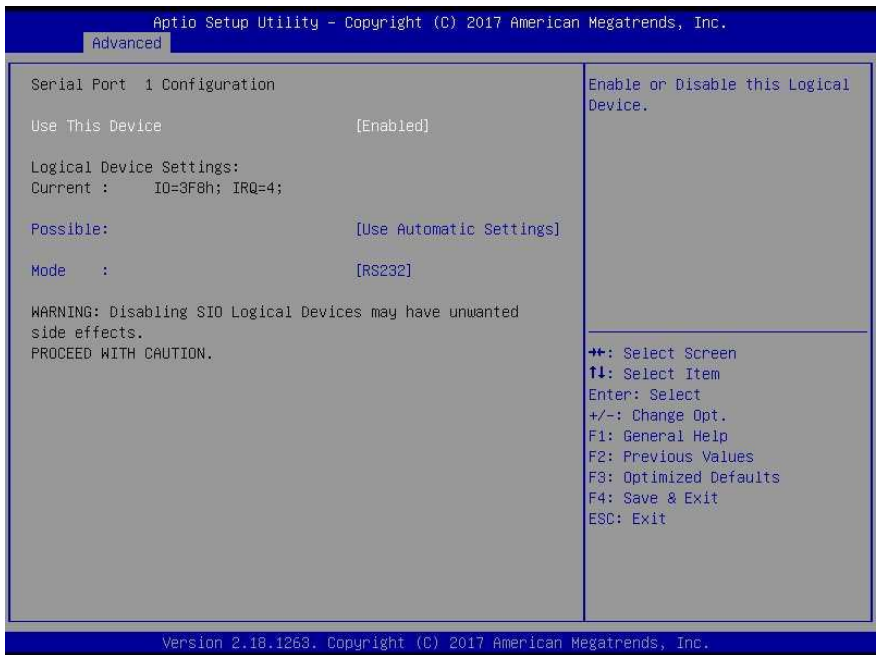
Options summary:

ME FW Image Re-Flash	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable ME FW Image Re-Flash function.		

3.4.5 Advanced: SIO Configuration



3.4.5.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	
UART RS232, 422, 485 selection		

3.4.5.2 SIO Configuration: Serial Port 2 Configuration

*This setup menu is ONLY for BOXER-6841M-A6 SKU.

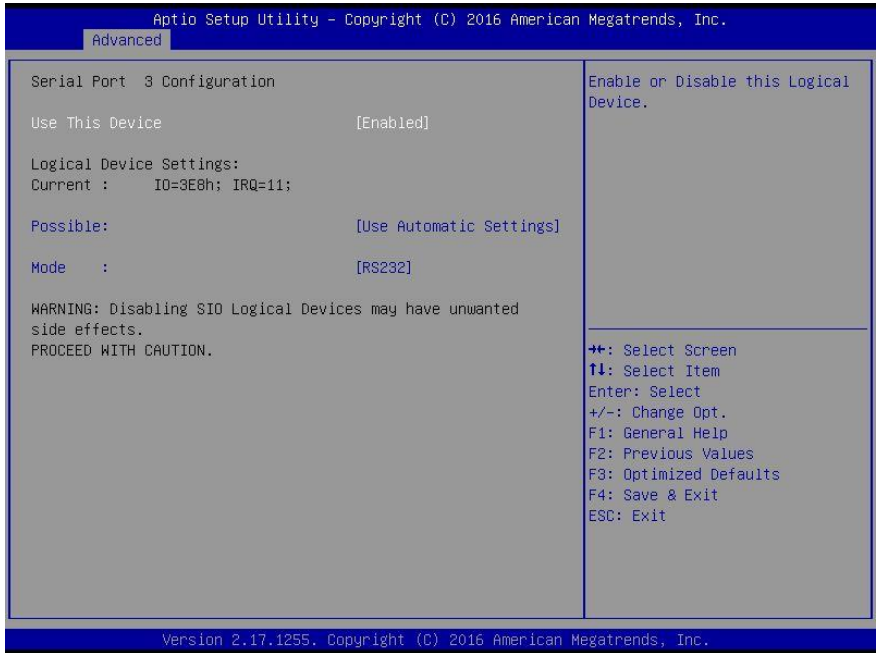


Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		

3.4.5.3 SIO Configuration: Serial Port 3 Configuration

*This setup menu is ONLY for BOXER-6841M-A6 SKU.

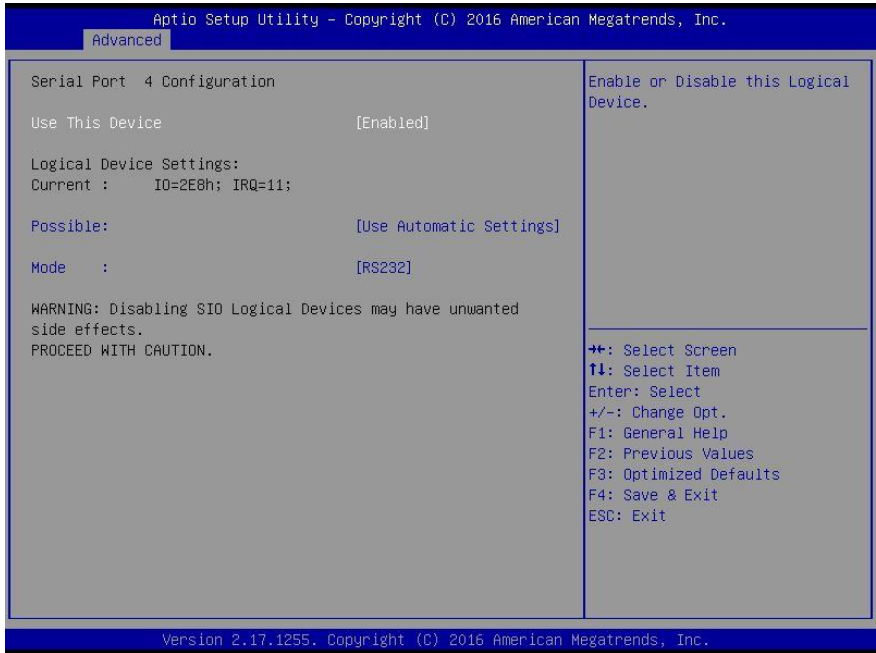


Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=11;	
	IO=3F8; IRQ=11;	
Select an optimal setting for IO device		

3.4.5.4 SIO Configuration: Serial Port 4 Configuration

*This setup menu is ONLY for BOXER-6841M-A6 SKU.

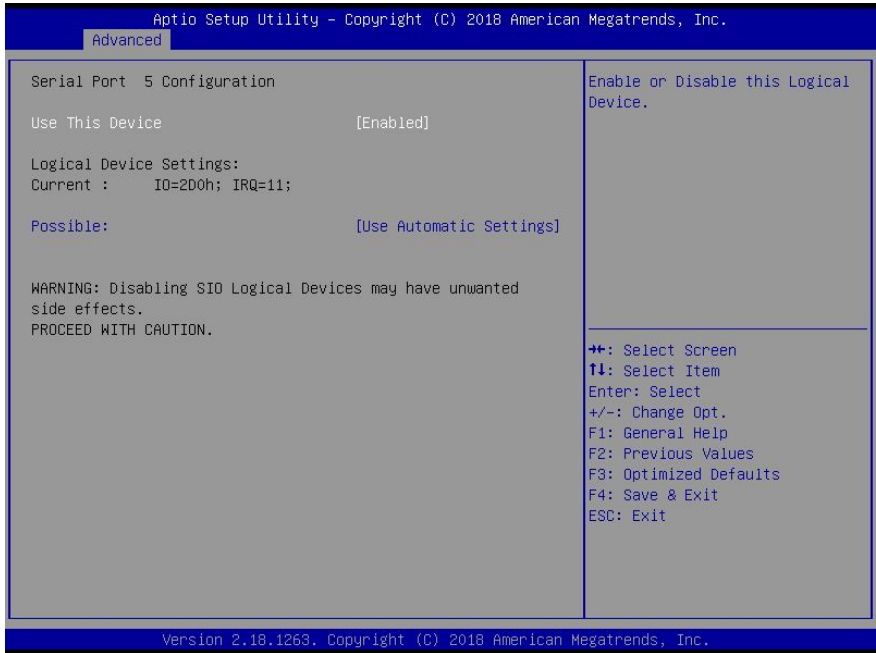


Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=11;	
	IO=3F8; IRQ=11;	
Select an optimal setting for IO device		

3.4.5.5 SIO Configuration: Serial Port 5 Configuration

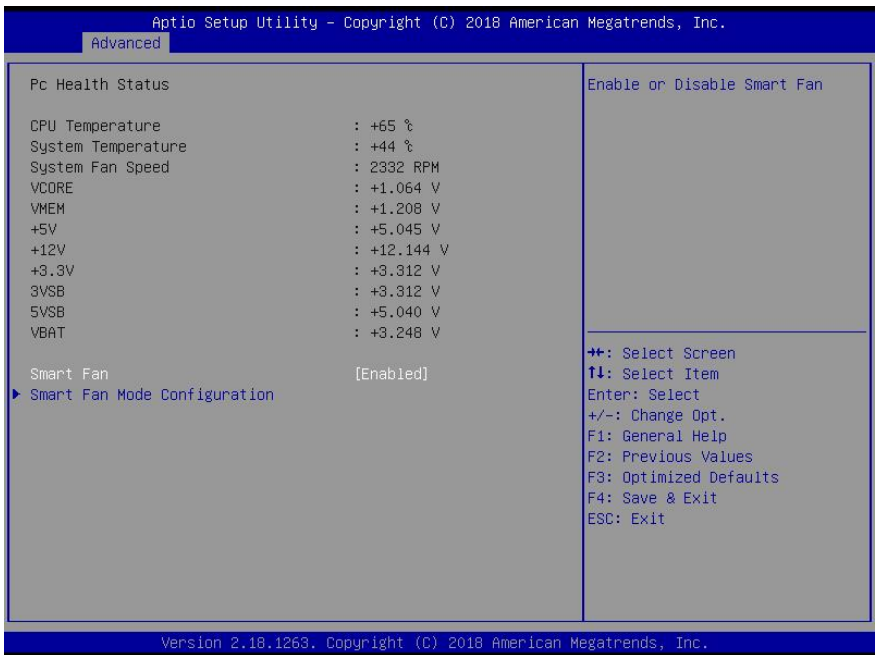
*This setup menu is ONLY for BOXER-6841M-A6 SKU.



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2D0; IRQ=11;	
	IO=2C0; IRQ=11;	
Select an optimal setting for IO device		

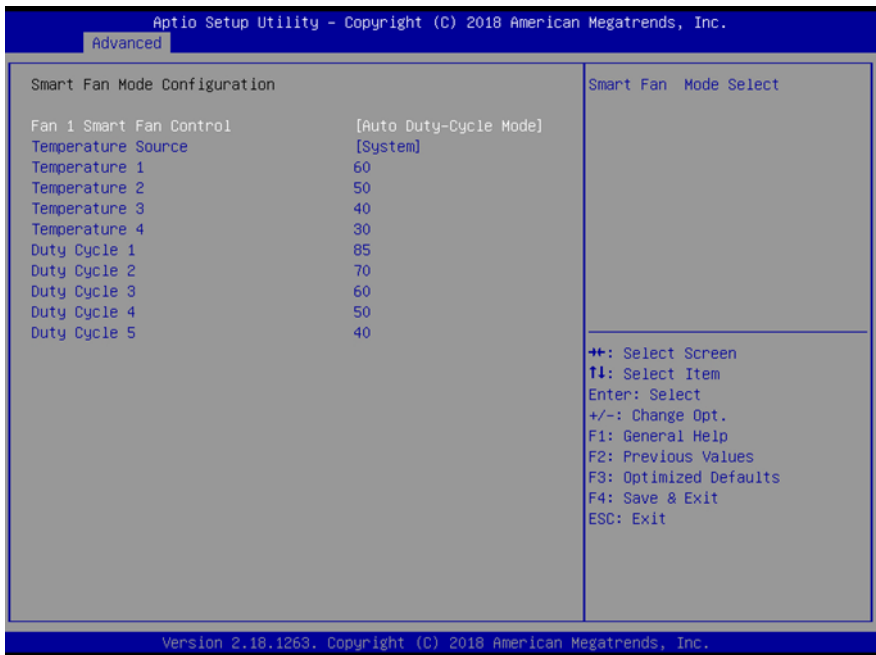
3.4.6 Advanced: Hardware Monitor



Options summary:

Smart Fan	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Smart Fan		

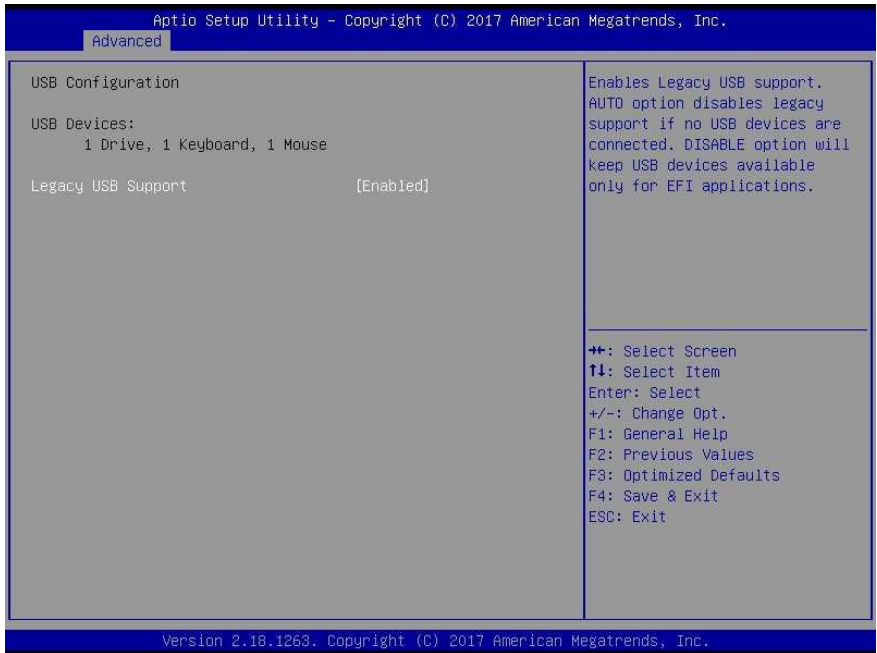
3.4.6.1 Hardware Monitor: Smart Fan Mode Configuration



Options summary:

Fan 1 Smart Fan Control	Manual RPM Mode	Optimal Default, Failsafe Default
	Manual Duty Mode	
	Auto RPM Mode	
	Auto Duty-Cycle Mode	
Smart Fan Mode Select		
Temperature Source	CPU	Optimal Default, Failsafe Default
	System	
Select the monitored temperature source for this fan		
Temperature 1/2/3/4	1-100	Range
	60/50/40/30	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		
Duty Cycle 1/2/3/4/5	1-100	Range
	85/70/60/50/40	Optimal Default, Failsafe Default
Auto fan speed control. Fan speed will follow different temperature by different duty cycle 1-100		

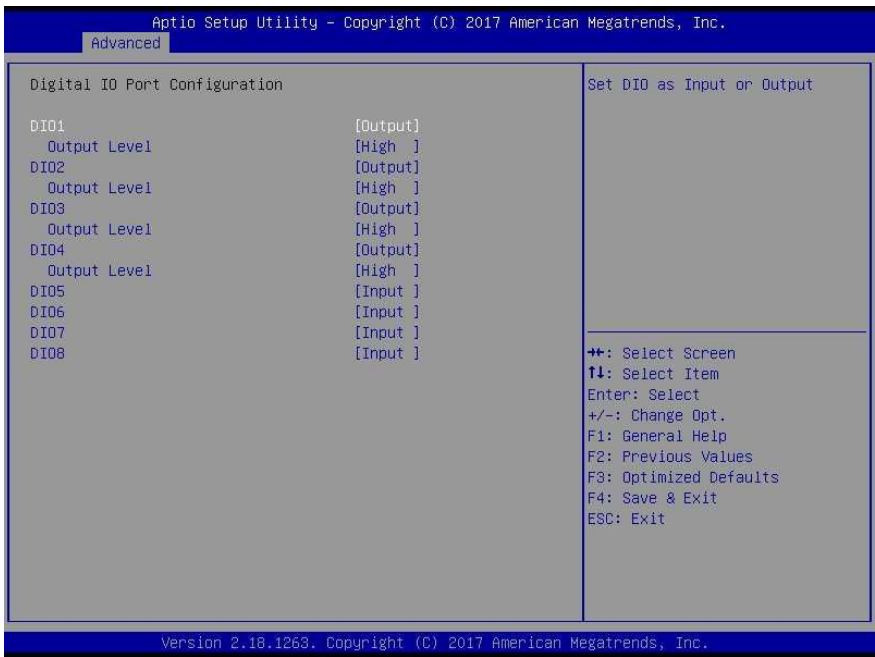
3.4.7 Advanced: USB Configuration



Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
<p>Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS.</p> <p>AUTO option disables legacy support if no USB devices are connected</p>		

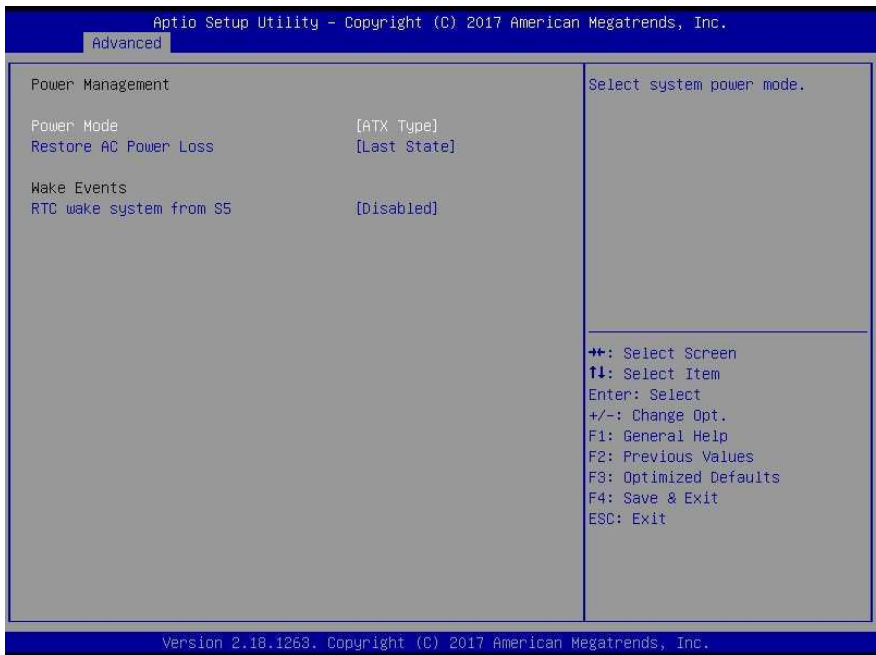
3.4.8 Advanced: Digital IO Port Configuration



Options summary:

DIO Type	Output	Optimal Default, Failsafe Default
	Input	
DIO Direction Type Setting		
DIO Data	Low	Optimal Default, Failsafe Default
	High	
DIO Output High/Low Setting		

3.4.9 Advanced: Power Management



Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

3.5 Setup submenu: Chipset



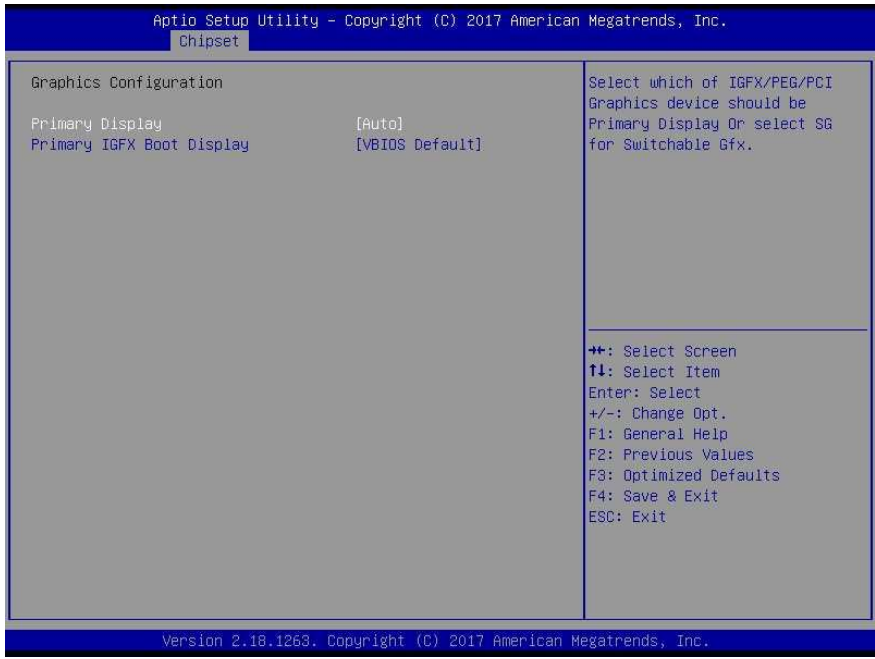
3.5.1 Chipset: System Agent (SA) Configuration



Options summary:

Max TOLUD	Dynamic	Optimal Default, Failsafe Default
	1 GB	
	1.25 GB	
	1.5 GB	
	1.75 GB	
	2 GB	
	2.25 GB	
	2.5 GB	
	2.75 GB	
	3 GB	
	3.25 GB	
3.5 GB		
<p>Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.</p>		

3.5.1.1 System Agent (SA) Configuration: Graphics Configuration

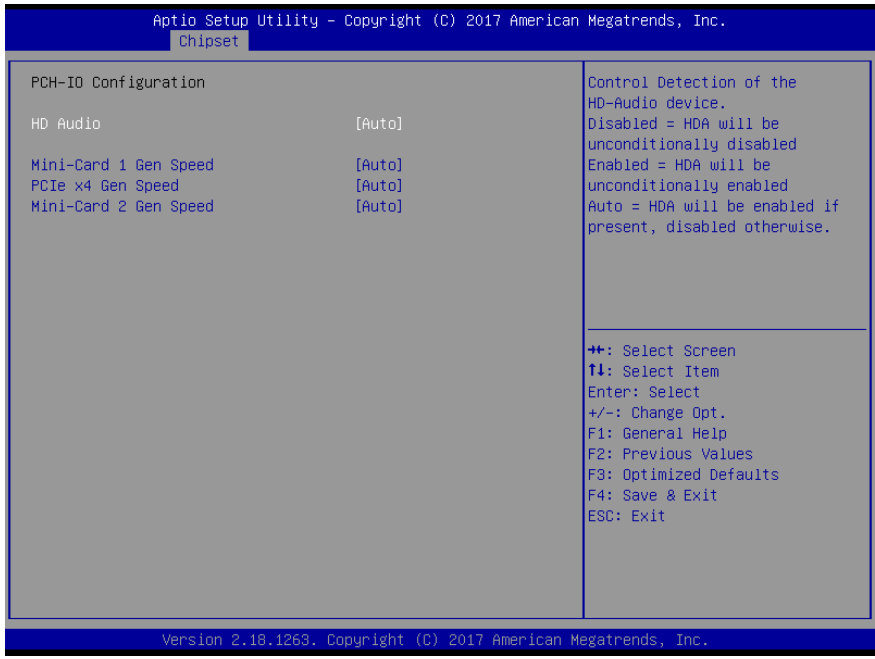


Options summary:

Primary Display	Auto	Optimal Default, Failsafe Default
	IGFX	
	PEG	
	PCIe	
Select which of IGFX/PEG/PCI Graphics device should be Primary Display Or select SG for Switchable Gfx.		
Primary IGFX Boot Display	VBIOS default	Optimal Default, Failsafe Default
	HDMI 1	
	VGA	
	HDMI 2	
Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.		
*Setup option VGA is ONLY for BOXER-6841M-A6 SKU.		
Secondary IGFX Boot Display	Disabled	Optimal Default, Failsafe Default
	HDMI 1	
	VGA	

	HDMI 2	
Select Secondary Display Device *Setup option VGA is ONLY for BOXER-6841M-A6 SKU.		

3.5.2 Chipset: PEG Port Configuration

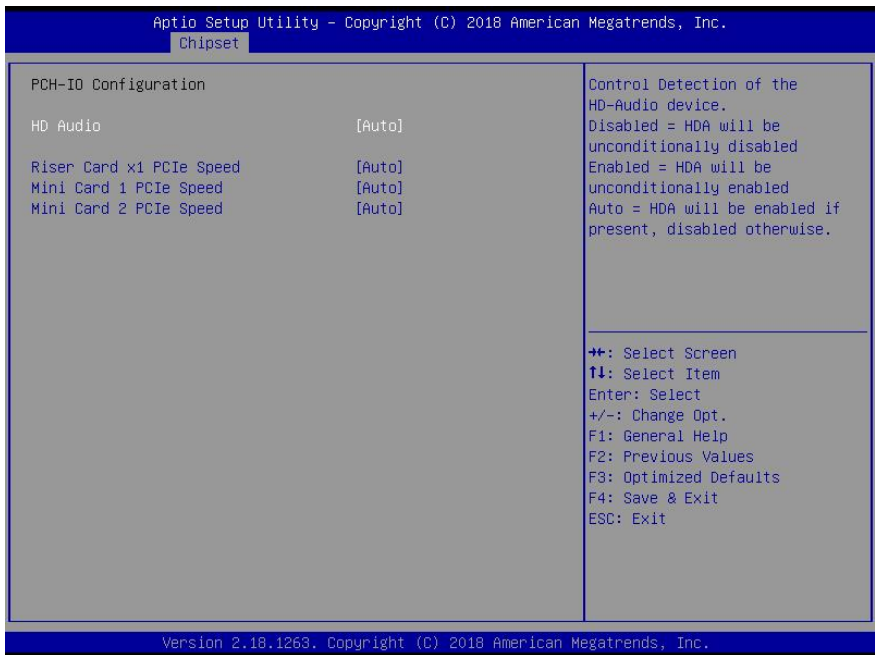


Options summary:

MAX Link Speed	Gen1	Optimal Default, Failsafe Default
	Gen2	
	Gen3	
	Auto	
Configure PEG Max Speed		

***Setup item PEG 0:1:1 is ONLY for BOXER-6841M-A3/A4/A5/A6 SKU.**

3.5.3 Chipset: PCH-IO Configuration



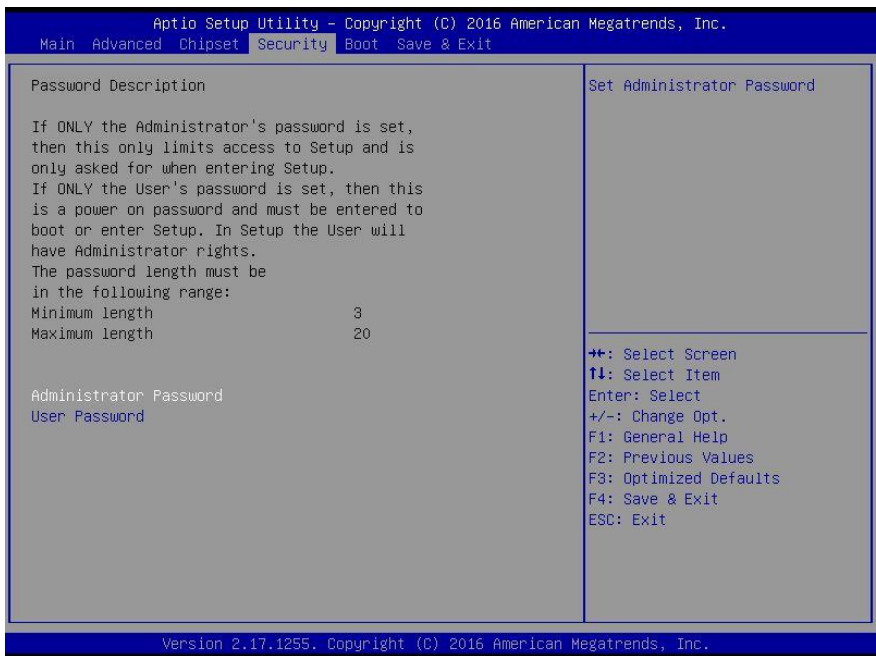
Options summary:

HD Audio	Disabled	Optimal Default, Failsafe Default
	Enabled	
	Auto	
Control Detection of the HD-Audio device. Disabled / Enabled = HDA will be unconditionally disabled / enabled Auto = HDA will be enabled if present, disabled otherwise.		
Riser Card x1 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	
Configure PCIe Speed		
Mini-Card 1/2 PCIe Speed	Auto	Optimal Default, Failsafe Default
	Gen1	
	Gen2	
	Gen3	

Configure PCIe Speed

***Setup item Mini-Card 1 PCIe Speed is ONLY for BOXER-6841M-A3/A4/A5/A6 SKU.**

3.6 Setup submenu: Security



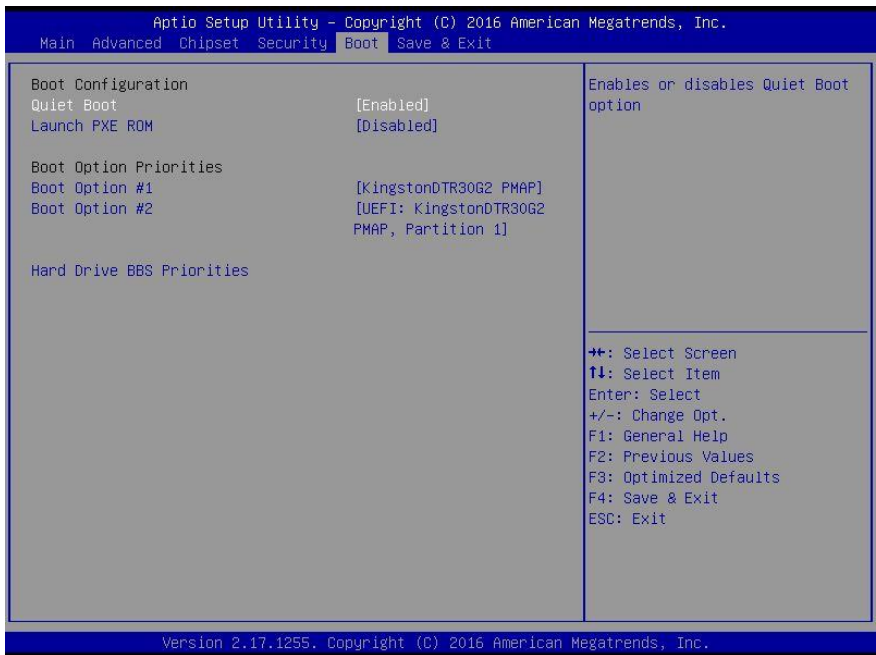
Change User/Administrator Password

You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

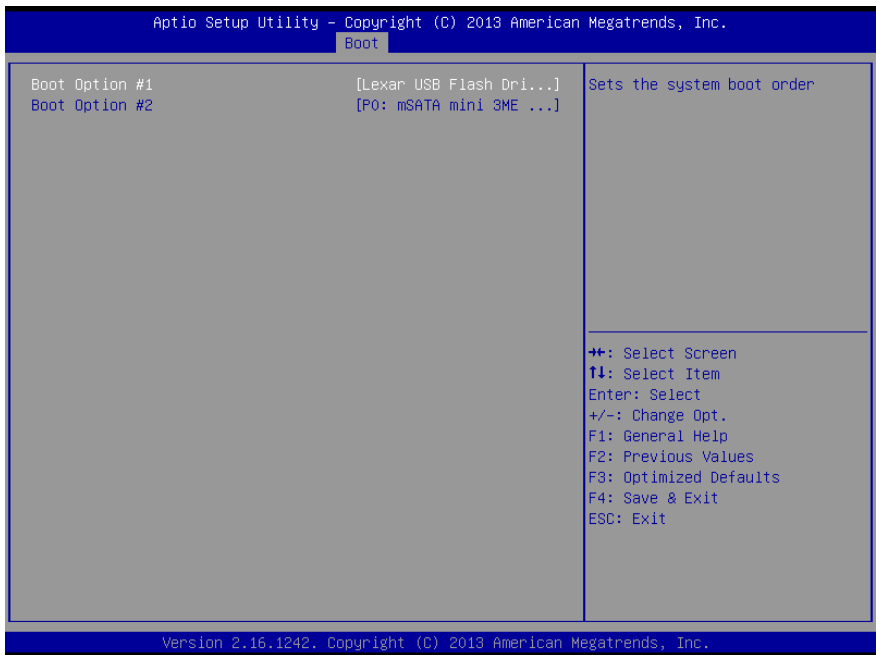
3.7 Setup submenu: Boot



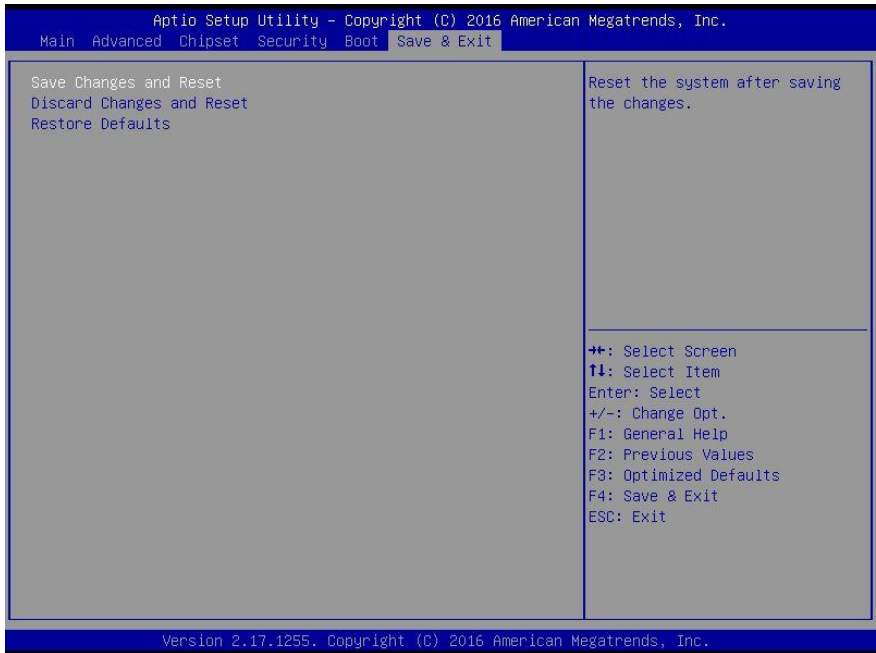
Options summary:

Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enables or disables Quiet Boot option.		
Launch PXE OpROM	Disabled	Optimal Default, Failsafe Default
	Enabled	
Controls the execution of UEFI and Legacy PXE OpROM.		

3.8 Boot: BBS Priorities



3.9 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The BOXER-6841M comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

PS: System Driver only supports "Win7 64bit", "Win7 32bit" will not supported.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **Step 1 - Chipset** folder and select the correct chipset and OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphic Driver

1. Open the **Step 2 - Graphic** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install LAN Driver

1. Open the **Step 3 - LAN** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install Audio Driver

1. Open the **Step 4 - Audio** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install USB3.0 Driver

1. Open the **Step 5 – USB3.0** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install ME Driver

1. Open the **Step 6 - ME** folder and select the correct chipset and OS
2. Open the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 7 – Install Serial Port Driver

1. Open the **Step 7 - Serial Port Driver (Optional)** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 8 – Install TPM Hotfix Driver

1. Open the **Step 8 – TPM Hotfix (Optional)** folder and select the correct chipset and OS
2. Open the **.exe** file in the folder

3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table

	Default Value	Note
Index	0x2E ^(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F ^(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table

	LDN	Register	BitNum	Value	Note
Timer Counter	0x07 ^(Note3)	0xF6 ^(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07 ^(Note5)	0xF5 ^(Note6)	3 ^(Note7)	0 ^(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07 ^(Note9)	0xF5 ^(Note10)	5 ^(Note11)	1 ^(Note12)	0: Disable 1: Enable
Timeout Status	0x07 ^(Note13)	0xF5 ^(Note14)	6 ^(Note15)	1	1: Clear timeout status
Output Mode	0x07 ^(Note16)	0xF5 ^(Note17)	4 ^(Note18)	1 ^(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07 ^(Note20)	0xFA ^(Note21)	0 ^(Note22)	1 ^(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex //This parameter is represented from Note1
#define byte   SIOData //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN //This parameter is represented from Note3
#define byte   TimerReg //This parameter is represented from Note4
#define byte   TimerVal // This parameter is represented from Note24
#define byte   UnitLDN //This parameter is represented from Note5
#define byte   UnitReg //This parameter is represented from Note6
#define byte   UnitBit //This parameter is represented from Note7
#define byte   UnitVal //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
#define byte   ModeLDN // This parameter is represented from Note16
#define byte   ModeReg // This parameter is represented from Note17
#define byte   ModeBit // This parameter is represented from Note18
#define byte   ModeVal // This parameter is represented from Note19
#define byte   WDTRstLDN // This parameter is represented from Note20
#define byte   WDTRstReg // This parameter is represented from Note21
#define byte   WDTRstBit // This parameter is represented from Note22
#define byte   WDTRstVal // This parameter is represented from Note23
*****

```



```
*****  
VOID Main(){  
    // Procedure : AaeonWDTConfig  
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)  
    // (boolean)Unit : Select time unit(0: second, 1: minute).  
    AaeonWDTConfig();  
  
    // Procedure : AaeonWDTEnable  
    // This procedure will enable the WDT counting.  
    AaeonWDTEnable();  
}  
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable 0{
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig 0{
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID WDTParameterSetting0{
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus0{
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```
*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;










































    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

Appendix B

I/O Information

B.1 I/O Address Map

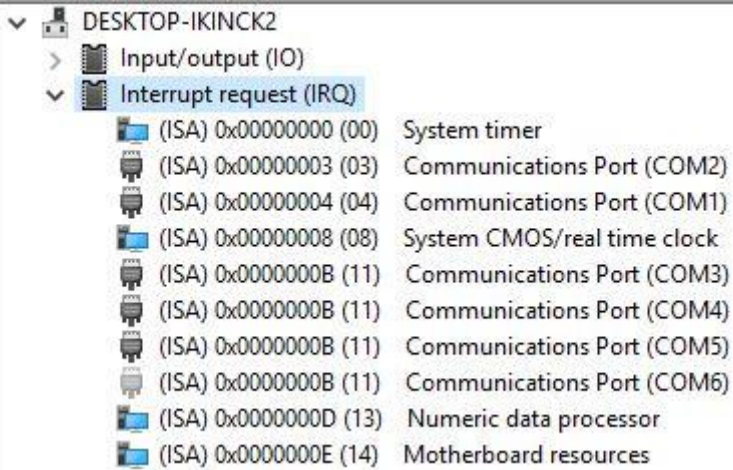
▼		DESKTOP-IKINCK2	
▼		Input/output (IO)	
		[0000000000000000 - 000000000000CF7]	PCI Express Root Complex
		[0000000000000020 - 000000000000021]	Programmable interrupt controller
		[0000000000000024 - 000000000000025]	Programmable interrupt controller
		[0000000000000028 - 000000000000029]	Programmable interrupt controller
		[000000000000002C - 00000000000002D]	Programmable interrupt controller
		[000000000000002E - 00000000000002F]	Motherboard resources
		[0000000000000030 - 000000000000031]	Programmable interrupt controller
		[0000000000000034 - 000000000000035]	Programmable interrupt controller
		[0000000000000038 - 000000000000039]	Programmable interrupt controller
		[000000000000003C - 00000000000003D]	Programmable interrupt controller
		[0000000000000040 - 000000000000043]	System timer
		[000000000000004E - 00000000000004F]	Motherboard resources
		[0000000000000050 - 000000000000053]	System timer
		[0000000000000061 - 000000000000061]	Motherboard resources
		[0000000000000063 - 000000000000063]	Motherboard resources
		[0000000000000065 - 000000000000065]	Motherboard resources
		[0000000000000067 - 000000000000067]	Motherboard resources
		[0000000000000070 - 000000000000070]	Motherboard resources
		[0000000000000070 - 000000000000077]	System CMOS/real time clock
		[0000000000000080 - 000000000000080]	Motherboard resources
		[0000000000000092 - 000000000000092]	Motherboard resources
		[00000000000000A0 - 0000000000000A1]	Programmable interrupt controller
		[00000000000000A4 - 0000000000000A5]	Programmable interrupt controller
		[00000000000000A8 - 0000000000000A9]	Programmable interrupt controller
		[00000000000000AC - 0000000000000AD]	Programmable interrupt controller
		[00000000000000B0 - 0000000000000B1]	Programmable interrupt controller
		[00000000000000B2 - 0000000000000B3]	Motherboard resources
		[00000000000000B4 - 0000000000000B5]	Programmable interrupt controller
		[00000000000000B8 - 0000000000000B9]	Programmable interrupt controller
		[00000000000000BC - 0000000000000BD]	Programmable interrupt controller
		[00000000000000F0 - 0000000000000F0]	Numeric data processor
		[0000000000002C0 - 0000000000002C7]	Communications Port (COM6)
		[0000000000002D0 - 0000000000002D7]	Communications Port (COM5)
		[0000000000002E8 - 0000000000002EF]	Communications Port (COM4)
		[0000000000002F8 - 0000000000002FF]	Communications Port (COM2)
		[0000000000003B0 - 0000000000003BB]	Intel(R) HD Graphics 630
		[0000000000003C0 - 0000000000003DF]	Intel(R) HD Graphics 630
		[0000000000003E8 - 0000000000003EF]	Communications Port (COM3)
		[0000000000003F8 - 0000000000003FF]	Communications Port (COM1)

[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[0000000000000680 - 000000000000069F]	Motherboard resources
[0000000000000800 - 000000000000087F]	Motherboard resources
[0000000000000A00 - 0000000000000A0F]	Motherboard resources
[0000000000000A10 - 0000000000000A1F]	Motherboard resources
[0000000000000A20 - 0000000000000A2F]	Motherboard resources
[0000000000000D00 - 0000000000000FFF]	PCI Express Root Complex
[000000000000164E - 000000000000164F]	Motherboard resources
[0000000000001800 - 00000000000018FE]	Motherboard resources
[0000000000001854 - 0000000000001857]	Motherboard resources
[000000000000B000 - 000000000000BFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #8 - A117
[000000000000C000 - 000000000000CFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #7 - A116
[000000000000D000 - 000000000000DFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #6 - A115
[000000000000E000 - 000000000000EFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #5 - A114
[000000000000F000 - 000000000000F03F]	Intel(R) HD Graphics 630
[000000000000F040 - 000000000000F05F]	Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[000000000000F060 - 000000000000F07F]	Standard SATA AHCI Controller
[000000000000F080 - 000000000000F083]	Standard SATA AHCI Controller
[000000000000F090 - 000000000000F097]	Standard SATA AHCI Controller
[000000000000FF00 - 000000000000FFFE]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources
[000000000000FFFF - 000000000000FFFF]	Motherboard resources
> Interrupt request (IRQ)	
> Memory	

B.2 Memory Address Map

DESKTOP-IKINCK2	
Input/output (IO)	
Interrupt request (IRQ)	
Memory	
[0000000000A0000 - 0000000000BFFFF]	Intel(R) HD Graphics 630
[0000000000A0000 - 0000000000BFFFF]	PCI Express Root Complex
[0000000090000000 - 00000000DFFFFFFF]	PCI Express Root Complex
[00000000C0000000 - 00000000CFFFFFFF]	Intel(R) HD Graphics 630
[00000000DE000000 - 00000000DEFFFFFF]	Intel(R) HD Graphics 630
[00000000DF000000 - 00000000DF01FFFF]	Intel(R) I211 Gigabit Network Connection #3
[00000000DF000000 - 00000000DF0FFFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #8 - A117
[00000000DF020000 - 00000000DF023FFF]	Intel(R) I211 Gigabit Network Connection #3
[00000000DF100000 - 00000000DF11FFFF]	Intel(R) I211 Gigabit Network Connection #4
[00000000DF100000 - 00000000DF1FFFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #7 - A116
[00000000DF120000 - 00000000DF123FFF]	Intel(R) I211 Gigabit Network Connection #4
[00000000DF200000 - 00000000DF21FFFF]	Intel(R) I211 Gigabit Network Connection
[00000000DF200000 - 00000000DF2FFFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #6 - A115
[00000000DF220000 - 00000000DF223FFF]	Intel(R) I211 Gigabit Network Connection
[00000000DF300000 - 00000000DF31FFFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000DF300000 - 00000000DF3FFFFF]	Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #5 - A114
[00000000DF320000 - 00000000DF323FFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000DF400000 - 00000000DF41FFFF]	Intel(R) Ethernet Connection (2) I219-LM
[00000000DF420000 - 00000000DF42FFFF]	High Definition Audio Controller
[00000000DF430000 - 00000000DF43FFFF]	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
[00000000DF440000 - 00000000DF443FFF]	High Definition Audio Controller
[00000000DF444000 - 00000000DF447FFF]	Intel(R) 100 Series/C230 Series Chipset Family PMC - A121
[00000000DF448000 - 00000000DF449FFF]	Standard SATA AHCI Controller
[00000000DF44A000 - 00000000DF44A0FF]	Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123
[00000000DF44B000 - 00000000DF44B7FF]	Standard SATA AHCI Controller
[00000000DF44C000 - 00000000DF44C0FF]	Standard SATA AHCI Controller
[00000000DF44E000 - 00000000DF44EFFF]	Intel(R) 100 Series/C230 Series Chipset Family Thermal subsystem - A131
[00000000DFFE0000 - 00000000DFFFFFFF]	Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000FD000000 - 00000000FDABFFFF]	Motherboard resources
[00000000FD000000 - 00000000FE7FFFFF]	PCI Express Root Complex
[00000000FDAC0000 - 00000000FDACFFFF]	Motherboard resources
[00000000FDAD0000 - 00000000FDADFFFF]	Motherboard resources
[00000000FDAE0000 - 00000000FDAEFFFF]	Motherboard resources
[00000000FDAF0000 - 00000000FDAFFFFF]	Motherboard resources
[00000000FDB00000 - 00000000FDBFFFFF]	Motherboard resources
[00000000FE000000 - 00000000FE01FFFF]	Motherboard resources
[00000000FE036000 - 00000000FE03BFFF]	Motherboard resources
[00000000FE036000 - 00000000FE03BFFF]	Motherboard resources
[00000000FE03D000 - 00000000FE3FFFFF]	Motherboard resources
[00000000FE40F000 - 00000000FE40FFFF]	Intel(R) Management Engine Interface
[00000000FE410000 - 00000000FE7FFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED10000 - 00000000FED17FFF]	Motherboard resources
[00000000FED18000 - 00000000FED18FFF]	Motherboard resources
[00000000FED19000 - 00000000FED19FFF]	Motherboard resources
[00000000FED20000 - 00000000FED3FFFF]	Motherboard resources
[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 2.0
[00000000FED45000 - 00000000FED8FFFF]	Motherboard resources
[00000000FED90000 - 00000000FED93FFF]	Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFFFF]	Motherboard resources
[00000000FF000000 - 00000000FFFFFFFF]	Legacy device
[00000000FF000000 - 00000000FFFFFFFF]	Motherboard resources

B.3 IRQ Mapping Chart



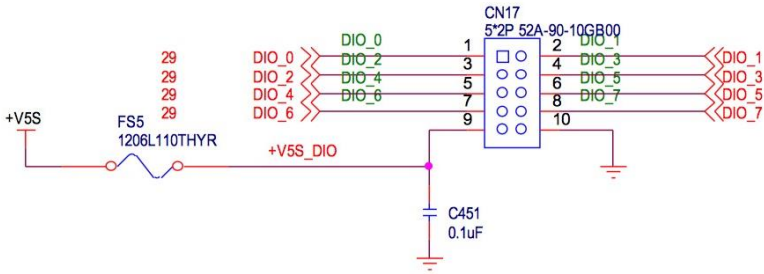
The screenshot shows the Windows Device Manager for a system named 'DESKTOP-IKINCK2'. The 'Interrupt request (IRQ)' category is expanded, showing a list of hardware devices and their assigned IRQs. The IRQs are listed in ascending order, with some sharing the same IRQ number.

Device	IRQ
System timer	(ISA) 0x00000000 (00)
Communications Port (COM2)	(ISA) 0x00000003 (03)
Communications Port (COM1)	(ISA) 0x00000004 (04)
System CMOS/real time clock	(ISA) 0x00000008 (08)
Communications Port (COM3)	(ISA) 0x0000000B (11)
Communications Port (COM4)	(ISA) 0x0000000B (11)
Communications Port (COM5)	(ISA) 0x0000000B (11)
Communications Port (COM6)	(ISA) 0x0000000B (11)
Numeric data processor	(ISA) 0x0000000D (13)
Motherboard resources	(ISA) 0x0000000E (14)

Appendix C

Electrical Specifications for I/O Ports

C.1 Electrical Specifications for I/O Ports



C.2 DIO Programming

BOXER-6841M utilizes FINTEK 81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3)

Exit the MB PnP Mode. Undesired result may occur if the MB PnP

Mode is not exited normally.(These three steps are the same as programming WDT)

C.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0x8A(Note4)	0(Note5)		GPIO80
DIO-2 Pin Status	0x06(Note6)	0x8A (Note7)	1(Note8)		GPIO81
DIO-3 Pin Status	0x06(Note9)	0x8A (Note10)	3(Note11)		GPIO83
DIO-4 Pin Status	0x06(Note12)	0x8A (Note13)	2(Note14)		GPIO82
DIO-5 Pin Status	0x06(Note15)	0x8A (Note16)	5(Note17)		GPIO85
DIO-6 Pin Status	0x06(Note18)	0x8A (Note19)	4(Note20)		GPIO84
DIO-7 Pin Status	0x06(Note21)	0x8A (Note22)	6(Note23)		GPIO86
DIO-8 Pin Status	0x06(Note24)	0x8A (Note25)	7(Note26)		GPIO87

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0x89(Note28)	0(Note29)	(Note30)	GPIO80
DIO-2 Output Data	0x06(Note31)	0x89 (Note32)	1(Note33)	(Note34)	GPIO81
DIO-3 Output	0x06(Note35)	0x89 (Note36)	3(Note37)	(Note38)	GPIO83

Data					
DIO-4 Output Data	0x06(Note39)	0x89 (Note40)	2(Note41)	(Note42)	GPIO82
DIO-5 Output Data	0x06(Note43)	0x89 (Note44)	5(Note45)	(Note46)	GPIO85
DIO-6 Output Data	0x06(Note47)	0x89 (Note48)	4(Note49)	(Note50)	GPIO84
DIO-7 Output Data	0x06(Note51)	0x89 (Note52)	6(Note53)	(Note54)	GPIO86
DIO-8 Output Data	0x06(Note55)	0x89 (Note56)	7(Note57)	(Note58)	GPIO87

C.4 Digital I/O Sample Program

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte  SIOIndex  //This parameter is represented from Note1
#define byte  SIOData   //This parameter is represented from Note2
#define void  IOWriteByte(byte IOPort, byte Value);
#define byte  IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte  DInput1LDN // This parameter is represented from Note3
#define byte  DInput1Reg // This parameter is represented from Note4
#define byte  DInput1Bit // This parameter is represented from Note5
#define byte  DInput2LDN // This parameter is represented from Note6
#define byte  DInput2Reg // This parameter is represented from Note7
#define byte  DInput2Bit // This parameter is represented from Note8
#define byte  DInput3LDN // This parameter is represented from Note9
#define byte  DInput3Reg // This parameter is represented from Note10
#define byte  DInput3Bit // This parameter is represented from Note11
#define byte  DInput4LDN // This parameter is represented from Note12
#define byte  DInput4Reg // This parameter is represented from Note13
#define byte  DInput4Bit // This parameter is represented from Note14
#define byte  DInput5LDN // This parameter is represented from Note15
#define byte  DInput5Reg // This parameter is represented from Note16
#define byte  DInput5Bit // This parameter is represented from Note17
#define byte  DInput6LDN // This parameter is represented from Note18
#define byte  DInput6Reg // This parameter is represented from Note19
#define byte  DInput6Bit // This parameter is represented from Note20
#define byte  DInput7LDN // This parameter is represented from Note21
#define byte  DInput7Reg // This parameter is represented from Note22
#define byte  DInput7Bit // This parameter is represented from Note23
#define byte  DInput8LDN // This parameter is represented from Note24
#define byte  DInput8Reg // This parameter is represented from Note25
#define byte  DInput8Bit // This parameter is represented from Note26
*****
```

```

*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN // This parameter is represented from Note27
#define byte   DOutput1Reg // This parameter is represented from Note28
#define byte   DOutput1Bit // This parameter is represented from Note29
#define byte   DOutput1Val // This parameter is represented from Note30
#define byte   DOutput2LDN // This parameter is represented from Note31
#define byte   DOutput2Reg // This parameter is represented from Note32
#define byte   DOutput2Bit // This parameter is represented from Note33
#define byte   DOutput2Val // This parameter is represented from Note34
#define byte   DOutput3LDN // This parameter is represented from Note35
#define byte   DOutput3Reg // This parameter is represented from Note36
#define byte   DOutput3Bit // This parameter is represented from Note37
#define byte   DOutput3Val // This parameter is represented from Note38
#define byte   DOutput4LDN // This parameter is represented from Note39
#define byte   DOutput4Reg // This parameter is represented from Note40
#define byte   DOutput4Bit // This parameter is represented from Note41
#define byte   DOutput4Val // This parameter is represented from Note42
#define byte   DOutput5LDN // This parameter is represented from Note43
#define byte   DOutput5Reg // This parameter is represented from Note44
#define byte   DOutput5Bit // This parameter is represented from Note45
#define byte   DOutput5Val // This parameter is represented from Note46
#define byte   DOutput6LDN // This parameter is represented from Note47
#define byte   DOutput6Reg // This parameter is represented from Note48
#define byte   DOutput6Bit // This parameter is represented from Note49
#define byte   DOutput6Val // This parameter is represented from Note50
#define byte   DOutput7LDN // This parameter is represented from Note51
#define byte   DOutput7Reg // This parameter is represented from Note52
#define byte   DOutput7Bit // This parameter is represented from Note53
#define byte   DOutput7Val // This parameter is represented from Note54
#define byte   DOutput8LDN // This parameter is represented from Note55
#define byte   DOutput8Reg // This parameter is represented from Note56
#define byte   DOutput8Bit // This parameter is represented from Note57
#define byte   DOutput8Val // This parameter is represented from Note58
*****

```

```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
*****
```



```
*****
Boolean  AeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```

*****
VOID  SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```