

BOXER-6710

Fanless Embedded Box PC

User's Manual 7th Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
BOXER-6710	1
3 Pin DC-In Power Connector	1
Din Rail Bracket	1
Screw Package	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

- 1. All cautions and warnings on the device should be noted.
- All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
- 3. Make sure the power source matches the power rating of the device.
- 4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
- Always completely disconnect the power before working on the system's hardware.
- No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
- 7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
- 8. Always disconnect this device from any AC supply before cleaning.
- 9. While cleaning, use a damp cloth instead of liquid or spray detergents.
- 10. Make sure the device is installed near a power outlet and is easily accessible.
- 11. Keep this device away from humidity.
- 12. Place the device on a solid surface during installation to prevent falls
- 13. Do not cover the openings on the device to ensure optimal heat dissipation.
- 14. Watch out for high temperatures when the system is running.
- 15. Do not touch the heat sink or heat spreader when the system is running
- 16. Never pour any liquid into the openings. This could cause fire or electric shock.

Preface

- As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
- 18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device

19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A0

	有毒有害物质或元素					
部件名称	铅	汞	镉	六价铬	多溴联苯	多溴二苯
	(Pb)	(Hg)	(Cd)	(Cr(VI))	(PBB)	醚(PBDE)
印刷电路板		\sim	\sim	\sim	\sim	\sim
及其电子组件	×	0	0	0	0	0
外部信号		\circ	\circ	\circ	\bigcirc	\sim
连接器及线材	×	0	0	0	0	0
外壳	0	0	0	0	0	0
中央处理器	~	\circ	\circ	\bigcirc	\bigcirc	\bigcirc
与内存	×	0	0	0	0	0
硬盘	×	0	0	0	0	0
液晶模块	×	×	0	0	0	0
光驱	×	0	0	0	0	0
触控模块	×	0	0	0	0	0
电源	×	0	0	0	0	0
电池	×	0	0	0	0	0

本表格依据 SJ/T 11364 的规定编制。

〇: 表示该有毒有害物质在该部件所有均质材料中的含量均在

GB/T 26572标准规定的限量要求以下。

×: 表示该有害物质的某一均质材料超出了GB/T 26572的限量要求, 然而该 部件

仍符合欧盟指令2011/65/EU 的规范。

备注:

一、此产品所标示之环保使用期限,系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。

三、上述部件物质液晶模块、触控模块仅一体机产品适用。

Hazardous and Toxic Materials List

AAEON System

QO4-381 Rev.A0

	Hazardous or Toxic Materials or Elements					
Component Name	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominat ed biphenyls (PBBs)	Polybrominat ed diphenyl ethers (PBDEs)
PCB and Components	Х	0	0	0	0	0
Wires &	~	0	0	0	0	
Ext.Connections	^	0	0	0	0	0
Chassis	0	0	0	0	0	0
CPU & RAM	Х	0	0	0	0	0
HDD Drive	Х	0	0	0	0	0
LCD Module	Х	Х	0	0	0	0
Optical Drive	Х	0	0	0	0	0
Touch Control Module	Х	0	0	0	0	0
PSU	Х	0	0	0	0	0
Battery	Х	0	0	0	0	0

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2). Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.

2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.

3. LCD Module and Touch Control Module only applies to certain products which feature these components.

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Chapter 1

Product Specifications

1.1 Specifications

System	
CPU	Intel® Pentium® Processor N4200
	Intel® Celeron® Processor N3350
Chipset	Intel® System on Chip
System Memory	DDR3L 1866MHz SODIMM x 1 (Max. 8GB, up to
	1600MHz)
	(Note: Memory with frequency greater than 1600MHz
	will automatically fix to 1600MHz)
Display Interface	VGA x 1
	HDMI x 1
Storage Device	HDD/SSD
	mSATA (Optional)
Ethernet	Intel® i211-AT x 2
I/O	VGA x 1
	HDMI x 1
	RJ-45 x 2 for GbE LAN
	USB 3.2 Gen 1 (Type-A) x 4
	Mic-in x 1
	Line-out x 1
	RS-232/422/485 x 3 with automatic flow control
	Power On/Off Button x 1
	9~24V 3-Pin DC-in Terminal Block x 1
Expansion	Full-Size Mini Card x 1 w/ SIM Slot
	Half-Size Mini Card x 1 (Optional for mSATA)
Indicator	Power LED on Power Button

System OS Support

Mechanical

Gross Weight

Mounting Dimensions

Net Weight	1.32 lb. (0.6kg)
Environmental	
Operating Temperature	-20°C \sim 60°C with W.T. SSD/HDD/mSATA (according
	to IEC68-2-14 with 0.5 m/s airflow; with industrial
	devices)
Storage Temperature	-49°F ~ 176°F (-45°C ~ 80°C)
Storage Humidity	95% @ 40°C, non-condensing
Anti-Vibration	3 Grms/ 5 ~ 500Hz/ operation – mSATA/SSD
	1 Grms/ 5~ 500Hz/ operation – HDD
Certification	CE/FCC Class A

OS Support Windows® 10 IoT 64-bit Linux Ubuntu 16.04.4 Note: To avoid random non-booting issue caused by the incompatibility of Intel®

Pentium[®] Processor N Series with certain unstable 1866MHz memories, memory with frequency greater than 1600MHz will automatically fix to 1600MHz, while memory that

runs at a speed lower than 1600MHz will maintain its original speed.

DIN Rail Mount

3.08 lb. (1.4kg)

1.7" x 6.5" x 4.1" (44mm x 166mm x 106mm)

Power Supply

Power Requirement 9 ~ 24V with 3-pin Terminal Block

Chapter 2

Hardware Information

2.1 Dimensions



2.2 Jumpers and Connectors



2.3 List of Jumpers

Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP5	AT/ATX Mode Select
JP10	Clear CMOS

2.3.1 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip.

To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application,

contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.



2.3.3 Clear CMOS (JP10)



2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
CN65	CRT Port (Box Connector)
CN38	DC-In
CN61	HDMI Connector
CN8	SPI ROM Connector
CN26	Dual Stack USB (3.0/2.0)
CN27	Dual Stack USB (3.0/2.0)
CN7	Audio Jack Connector (Box Connector)
CN36	Remote Button Cable Connector (Box Connector)
CN53	USB 2.0 Connector (Box Connector)
CN54	USB 2.0 Connector (Box Connector)
CN46	RJ-45 LAN Connector
CN47	RJ-45 LAN Connector
CN18	COM Port 1 Box Connector (RS-232/422/485)
CN9	COM Port 2 Box Connector (RS-232/422/485)
CN12	COM Port 3 Box Connector (RS-232/422/485)
SW1	Power Button Connector (Box Connector)
CN43	DIO Connector
CN3	SATA PWR Connector
CN4	SATA Connector
BAT1	RTC Battery Connector
CN45	Debug Port Connector
CN33	Mini Card Connector
CN5	Mini Card Connector

Label	Function
SIM1	SIM 1 Card Connector
CN39	SATA LED Connector
DIMM1	SODIMM Connector

2.4.1 Mini Card Connector (CN5/CN33)

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	+V3.3A
3	NC	4	GND
5	NC	6	+1.5V
7	PCIE_CLK_REQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	PCIE_REF_CLK-	12	UIM_CLK
13	PCIE_REF_CLK+	14	UIM_RST
15	GND	16	UIM_VPP
17	NC	18	GND
19	NC	20	W_DISABLE#
21	GND	22	PCIE_RST#
23	PCIE_RX-	24	+V3.3A
25	PCIE_RX+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PCIE_TX-	32	SMB_DATA
33	PCIE_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+V3.3A	40	GND
41	+V3.3A	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	+1.5V

Pin	Signal	Pin	Signal
49	NC	50	GND
51	NC	52	+V3.3A

2.4.2 LPC Port (CN45)

Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	I2C CLK	I/O	+3.3V
11	I2C DATA	I/O	+3.3V
12	SERIRQ	I/O	+3.3V

2.4.3 SATA Port (CN4)

Pin	Pin Name	Signal Type	Signal Level
1	GND #	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

Pin 1

Pin 7

2.4.4 SATA PWR Port (CN3)

Pin	Signal	Pin
1	+12V	12V
2	GND	GND
3	GND	GND
4	+5V	5V

2.4.5 USB 3.0 (CN26/CN27)



Pin	Signal	Pin	Signal
1	VBUS_1	2	VBUS_2
3	(A)D-	4	(B)D-
5	(A)D+	6	(B)D+
7	GND	8	GND
9	(A)SSRX-	10	(B)SSRX-
11	(A)SSRX+	12	(B)SSRX+
13	GND	14	GND
15	(A)SSTX-	16	(B)SSTX-
17	(A)SSTX+	18	(B)SSTX+

2.4.6 CRT Port (Box Connector) (CN65)

Pin	Signal	Pin	Signal
1	VSYNC	2	HSYNC
3	NC	4	DDC_CLK
5	DDC_DATA	6	GND

Pin	Signal	Pin	Signal
7	Blue	8	GND
9	Green	10	GND
11	Red	12	GND
13	VGA_VCC		

2.4.7 DC-In (CN38)

Pin	Signal	Pin	Signal
1	PWR_IN	2	GND
3	NC		

2.4.8 HDMI Port (CN61)

Pin	Signal	Pin	Signal
1	HDMI_DATA2_P	2	GND
3	HDMI_DATA2_N	4	HDMI_DATA1_P
5	GND	6	HDMI_DATA1_N
7	HDMI_DATA0_P	8	GND
9	HDMI_DATA0_N	10	HDMI_CLK_P
11	GND	12	HDMI_CLK_N
13	NC	14	NC
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	HDMI_PWR
19	HDMI_HDP		

2.4.9 SPI ROM Connector (CN8)

Pin	Signal	Pin	Signal
1	SPI_VCC	2	GND
3	SPI_CE	4	SPI_CLK
5	SPI_DATA_OUT	6	SPI_DATA_IN
7	NC	8	NC

2.4.10 USB 2.0 Connector (Box Connector) (CN53/CN54)



Pin	Signal	Pin	Signal
1	VBUS	2	USB1-
3	USB+	4	GND
5	GND		

2.4.11 Remote Button Cable Connector (Box Connector) (CN36)

Pin	Signal	Pin	Signal
1	PANSWH#	2	GND-

2.4.12 Physical COM Port (COM 1/COM 2/COM 3)



Pin	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RXD	RX+	DATA+
3	TXD	TX+	NC
4	DTR	RX-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.4.13 COM Port Box Connector (CN18/CN9/CN12)

Pin	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	DSR	NC	NC
3	RXD	TX+	DATA+

Pin	RS-232	RS-422	RS-485
4	RTS	NC	NC
5	TXD	RX+	NC
6	CTS	NC	NC
7	DTR	RX-	NC
8	RI	NC	NC
9	GND	NC	NC

1. Remove the screws as shown below; then remove the chassis cover.





2. Put the thermal pad on between the chassis and the RAM, insert the RAM into the slot diagonally and push down to secure.



2.6 Din Rail Installation



Chapter 3

AMI BIOS Setup

BOXER-671

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.
Fanless Embedded Box PC

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced - Enable/ Disable boot option for legacy network devices

Chipset - For hosting bridge parameters

Security - The setup administrator password can be set here

Boot – Enable/ Disable quiet Boot Option

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced

Aptio Setup Utility – Copyright (C) 2018 America Main <mark>Advanced </mark> Chipset Security Boot Save & Exit	n Megatrends, Inc.
 Trusted Computing CPU Configuration SATA Drives Hardware Monitor SIO Configuration AAEON Features Power Management 	Trusted Computing Settings ++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.18.1263. Copyright (C) 2018 American (Megatrends, Inc.

3.4.1 Trusted Computing

Aptio Setup Utility - Advanced	- Copyright (C) 2018 America	n Megatrends, Inc.
TPM20 Device Found Vendor: IFX Firmware Version: 5.51 Security Device Support Active PCR banks Available PCR banks SHA-1 PCR Bank SHA256 PCR Bank Pending operation Platform Hierarchy Storage Hierarchy Endorsement Hierarchy TPM2.0 UEFI Spec Version Physical Presence Spec Version TPM 20 InterfaceType Device Select	[Enable] SHA-1,SHA256 SHA-1,SHA256 [Enabled] [Enabled] [Enabled] [Enabled] [Enabled] [TTG_2] [1.3] [TTS] [Auto]	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available. **: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Options Summary			
Security Device Support	Disabled	Optimal Default, Failsafe Default	
	Enabled		
Enable/Disable Security Dev	ice.		
NOTE: Your Computer will re	eboot during restart in ord	der to change State of the Device.	
SHA-1 PCR Bank	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable SHA-1 PC	R Bank.		
SHA256 PCR Bank	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable SHA256 PCR Bank.			
Pending Operation	TPM Clear		
	None	Optimal Default, Failsafe Default	
Schedule an Operation for the Security Device.			
NOTE: Your Computer will re	eboot during restart in ord	der to change State of Security	
Device.			

Options Summary			
Platform Hierarchy	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable Platform H	Hierarchy.		
Storage Hierarchy	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable Storage H	ierarchy.		
Endorsement Hierarchy	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable Endorsem	ent Hierarchy.		
TPM2.0 UEFI Spec Version	TCG_2	Optimal Default, Failsafe Default	
	TCG_1_2		
Select the TCG2 Spec Versio	n Support.		
TCG_1_2: The Compatible m	ode for Win8/Win10.		
TCG_2: Support new TCG2 p	protocol and event format	for Win10 or later.	
Physical presence Spec	1.3	Optimal Default, Failsafe Default	
Version	1.2		
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not			
support 1.3.			
TPM 20 InterfaceType	TIS	Optimal Default, Failsafe Default	
	CRB		
Select the Communication Interface to TPM 20 Device.			
Device Select	Auto	Optimal Default, Failsafe Default	
	TPM 1.2		
	TPM 2.0		
TPM 1.2 will restrict support to TPM 1.2 devices.			
TPM 2.0 will restrict support to TPM 2.0 devices			
Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2			
devices will be enumerated			

3.4.2 CPU Configuration



Options Summary		
Active Processor Cores	Disabled	Optimal Default, Failsafe Default
	Enabled	
Number of cores to enable in	n each processor package	2.
Intel Virtualization	Disabled	
Technology	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can u	utilize the additional hard	ware capabilities provided by
vanderpool lechnology.	Disabled	1
vi-a		Orational Default Failante Default
Englate (Disable CDUL)/T. d	Enabled	Optimal Default, Falisale Default
	Disabled	1
EIST	Disabled	
	Enabled	Optimal Default, Falisate Default
Enable/Disable Intel SpeedSt	ep.	1
lurbo Mode	Disabled	
T 1 1 1	Enabled	Optimal Default, Failsafe Default
lurbo Mode.		
Boot performance mode	Max performance	Optimal Default, Failsafe Default
	Max battery	
Select the performance state that the BIOS will set before OS handoff.		
Power Limit 1 Enable	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1.		
C-States	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable C States.		

3.4.3 SATA Drives

Aptio Setup Utility - Advanced	Copyright (C) 2018 Americar	n Megatrends, Inc.
SATA Configuration		Enables or Disables the
Chipset SATA		Chipset SATA controller supports the 2 black internal
SATA Port Port	TS64GSSD370 (64.0GB) [Enabled]	SATA ports (up to 3Gb/s supported per port).
mSATA Port	[Not Installed] [Enabled]	
		++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help
		F2: Optimized Defaults F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.18.1263. C	opyright (C) 2018 American ⊧	Aegatrends, Inc.

Options Summary		
Chipset SATA	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable the Chipse	t SATA Controller. The Chi	pset SATA controller supports the
2 black internal SATA ports (u	up to 3Gb/s supported pe	er port).
Port	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable SATA Port.		
Port	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable SATA Port.		

3.4.4 Hardware Monitor

Aptio Set Advanced	up Utility – Copyright	(C) 2018 American	Megatrends, Inc.
Advanced Pc Health Status CPU Temperature System Temperature VCORE +5V VMEM +3.3V 3VSB	: +56 % : +37 % : +0.728 : +5.045 : +1.344 : +3.296 : +3.312	V V V V V	
SVSB VBAT	: +4.944 : +3.200	V	++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version	2 18 1263 Conuright (C) 2018 American Me	egatrends Inc

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3.4.5 SIO Configuration



3.4.5.1 Serial Port 1 Configuration

Aptio Setup Utility – Advanced	Copyright (C) 2018 American	Megatrends, Inc.
Serial Port 1 Configuration		Enable or Disable this Logical
Use This Device		Device.
Logical Device Settings: Current : IO=3F8h; IRQ=4;		
Possible: Mode :	[Use Automatic Settings] [RS232]	
WARNING: Disabling SIO Logical Devic	ces may have unwanted	
		<pre>**: Select Screen 1↓: Select Item</pre>
		Enter: Select +/−: Change Opt.
		F1: General Help F2: Previous Values
		F3: Optimized Defaults F4: Save & Exit
		ESU: EXIT

version 2.18.1263. Copyright (C) 2018 American Megatrends, Inc.

Options Summary			
Use This Device	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable this Logica	l Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default	
	10=3F8; IRQ=4;		
	IO=2F8; IRQ=3;		
Allows the user to change the device resource settings. New settings will be reflected			
on this setup page after system restarts.			
Mode:	RS232	Optimal Default, Failsafe Default	
	RS422		
	RS458		
UART RS232 RS422 RS485 se	election.		

Serial Port 2 Configuration 3.4.5.2

Aptio Setup Utility - Advanced	Copyright (C) 2018 American	Megatrends, Inc.
Serial Port 2 Configuration		Enable or Disable this Logical
Use This Device		Device.
Logical Device Settings: Current : IO=2F8h; IRQ=3;		
Possible: Mode :	[Use Automatic Settings] [RS232]	
WARNING: Disabling SIO Logical Devic	es may have unwanted	
		++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit FSC: Fxit

Options Summary			
Use This Device	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable this Logica	l Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default	
	IO=2F8; IRQ=3;		
	10=3F8; IRQ=4;		
Allows the user to change the device resource settings. New settings will be reflected			
on this setup page after system restarts.			
Mode:	RS232	Optimal Default, Failsafe Default	
	RS422		
	RS458		
UART RS232 RS422 RS485 se	election.		

3.4.5.3 Serial Port 3 Configuration

Aptio Setup Utility - Advanced	Copyright (C) 2018 American	Megatrends, Inc.
Serial Port 3 Configuration		Enable or Disable this Logical
Use This Device		Device.
Logical Device Settings: Current : IO=3E8h; IRQ=11;		
Possible: Mode :	[Use Automatic Settings] [RS232]	
WARNING: Disabling SIO Logical Devic	es may have unwanted	
		<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

Version 2.18.1263. Copyright (C) 2018 American Megatrends, Inc.

Options Summary			
Use This Device	Disabled		
	Enabled	Optimal Default, Failsafe Default	
Enable or Disable this Logica	l Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default	
	IO=3E8; IRQ=11;		
	IO=2E8; IRQ=11;		
Allows the user to change the device resource settings. New settings will be reflected			
on this setup page after system restarts.			
Mode:	RS232	Optimal Default, Failsafe Default	
	RS422		
	RS458		
UART RS232 RS422 RS485 selection.			

3.4.6 Power Management

Aptio Setup Utility Advanced	– Copyright (C) 2018 American	n Megatrends, Inc.
Power Management		Select system power mode.
Power Mode Restore AC Power Loss	[ATX Type] [Last State]	
Wake Events RTC wake system from S5	[Disabled]	
		<pre>+: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2,18,1263.	Convright (C) 2018 American M	legatrends. Inc.

Options Summary		
Power Mode	АТХ Туре	Optimal Default, Failsafe Default
	АТ Туре	
Select system power mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Loss	
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the		
hr::min::sec specified.		

3.5 Setup Submenu: Chipset



3.5.1 North Bridge

Aptio Setup Uti Chipset	lity – Copyright (C) 2018 Amer	ican Megatrends, Inc.
Memory Information		Select DVMT5.0 Total Graphic
Total Memory	4096 MB (LPDDR3)	Internal Graphics Device
D∨MT Total Gf× Mem		
		<pre>++: Select Screen f↓: Select Item</pre>
		Enter: Select +/-: Change Opt.
		F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit
Version 2.18.1	263. Copyright (C) 2018 Americ	an Megatrends, Inc.

Options Summary		
DCMT Total Gfx Mem	128M	
	256M	Optimal Default, Failsafe Default
	MAX	
Select DVMT5.0 Total Graphics Memory size used by the Internal Graphics Device.		

3.5.2 South Bridge

Aptio Setup Chipset	Utility – Copyright (C) 2018 Amer	ican Megatrends, Inc.
HD-Audio Support	[Enable]	Enable/Disable HD-Audio Support
Mini-Card 1 Speed Mini-Card 2 Speed	(Auto] [Auto]	
		++: Select Screen 11: Select Item Enter: Select
		+/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults
		F4: Save & Exit ESC: Exit
Version 2.1	18,1263, Convright (C) 2018 Americ	an Megatrends, Trc.

Options Summary			
HD-Audio Support	Disable		
	Enable	Optimal Default, Failsafe Default	
Enable/Disable HD-Audio Su	ipport.		
Mini-Card 1 Speed	Auto	Optimal Default, Failsafe Default	
	Gen 1		
	Gen 2		
Configure PCIe Speed.			
Mini-Card 2 Speed	Auto	Optimal Default, Failsafe Default	
	Gen 1		
	Gen 2		
Configure PCIe Speed.			

3.6 Setup Submenu: Security

Password Description Set Setup If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights. The password length must be in the following range: Minimum length Maximum length 3 Maximum length 20 ++: Select Setup Administrator Password +/-: Chang	, Inc.
Maximum length 20 ++: Select 11: Select Setup Administrator Password Enter: Sel User Password +/-: Chang	Administrator
F1: Genera F2: Previo F3: Optimi F4: Save & ESC: Exit	Screen Item ect e Opt. l Help us Values zed Defaults Exit

Change User/Administrator Password

You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility. Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

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3.7 Setup Submenu: Boot

Aptio Setup Utility Main Advanced Chipset Security	– Copyright (C) 2018 American <mark>Boot</mark> Save & Exit) Megatrends, Inc.
Boot Configuration		Enables or disables Quiet Boot
Quiet Boot Network Stack	[Enabled] [Disabled]	briton
Boot Option Priorities Boot Option #1 Boot Option #2	[Windows Boot Manage] [UEFI: KingstonDTR30]	
		↔: Select Screen 1↓: Select Item Enter: Select
		+/-: Change Opt. F1: General Help F2: Previous Values
		F4: Save & Exit ESC: Exit
Version 2.18.1263.	Copyright (C) 2018 American M	egatrends, Inc.

Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Quiet Boot option.		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack.		

3.8 Setup Submenu: Save & Exit

Aptio Setup Utility – Copyright (C) 2018 American Main Advanced Chipset Security Boot <mark>Save & Exit</mark>	Megatrends, Inc.
Save Options Save Changes and Reset Discard Changes and Exit Default Options Restore Defaults	Reset the system after saving the changes.
	++: Select Screen 14: Select Item Enter: Select
	+/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.18.1263. Copyright (C) 2018 American Mu	egatrends, Inc.

Chapter 4

Drivers Installation

4.1 Driver Download and Installation

Drivers for the BOXER-6710 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/fanless-embedded-box-pc-boxer-6710

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Drivers

- 1. Open the STEP1-Chipset folder and select your OS
- 2. Open the SetupChipset.exe file in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 2 - Install Graphics Driver

- 1. Open the STEP2-Graphics folder
- 2. Open the Setup.exe file in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 3 - Install TXE Driver

- 1. Open the STEP3-TXE folder and select your OS
- 2. Open the Setup.exe file in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 4 – Install LAN Drivers

- 1. Open the STEP4–LAN folder and select your OS
- 2. Open the **tar.gz** or **.exe** file
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 5 – Install Audio Drivers

- 1. Open the STEP5–Audio folder and select your OS
- 2. Open the .exe file
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 6 – Install Serial IO Drivers

- 1. Open the STEP6–Serial IO Driver folder
- 2. Open the SetupSeriallO.exe file
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 7 – Install Serial Port Driver (Optional)

- 1. Open the STEP7–Serial Port Driver (Optional) folder and select your OS
- 2. Open the Setup_x64.exe file
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 8 – Install Linux Peripheral Drivers

- 1. Open the Peripheral Driver-Linux folder
- 2. Follow the instructions provided in the project user guide to manually install drivers

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1: Super I/O Relative Register Table			
	Default Value	Note	
Index	0x2E(Note1)	SIO MB PnP Mode Index Register	
		0x2E or 0x4E	
Data	0x2F(Note2)	SIO MB PnP Mode Data Register	
		0x2F or 0x4F	

Table 2: Watchdog Relative Register Table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07 (Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07 (Note5)	0xF5(Note6)	3 (Note7)	0 (Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07 (Note9)	0xF5 (Note10)	5(Note11)	1 (Note12)	0: Disable 1: Enable
Timeout Status	0x07 (Note13)	0xF5 (Note14)	6 (Note15)	1	1: Clear timeout status
Output Mode	0x07 (Note16)	0xF5 (Note17)	4 (Note18)	1 (Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07 (Note20)	0xFA (Note21)	0 (Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

A.2 Watchdog Sample Program

// SuperIO rela	ative definition (Please reference to Table 1)	
#define byte	SIOIndex //This parameter is represented from Note1	
#define byte	SIOData //This parameter is represented from Note2	
#define void	IOWriteByte(byte IOPort, byte Value);	
#define byte	e IOReadByte(byte IOPort);	
// Watch Dog	relative definition (Please reference to Table 2)	
#define byte	TimerLDN //This parameter is represented from Note3	
#define byte	TimerReg //This parameter is represented from Note4	
#define byte	TimerVal // This parameter is represented from Note24	
#define byte	UnitLDN //This parameter is represented from Note5	
#define byte	UnitReg //This parameter is represented from Note6	
#define byte	UnitBit //This parameter is represented from Note7	
#define byte	UnitVal //This parameter is represented from Note8	
#define byte	EnableLDN //This parameter is represented from Note9	
#define byte	EnableReg //This parameter is represented from Note10	
#define byte	EnableBit //This parameter is represented from Note11	
#define byte	EnableVal //This parameter is represented from Note12	
#define byte	StatusLDN // This parameter is represented from Note13	
#define byte	StatusReg // This parameter is represented from Note14	
#define byte	StatusBit // This parameter is represented from Note15	
#define byte	ModeLDN // This parameter is represented from Note16	
#define byte	ModeReg // This parameter is represented from Note17	
#define byte	ModeBit // This parameter is represented from Note18	
#define byte	ModeVal // This parameter is represented from Note19	
#define byte	WDTRstLDN // This parameter is represented from Note20	
#define byte	WDTRstReg // This parameter is represented from Note21	
#define byte	WDTRstBit // This parameter is represented from Note22	
#define byte	WDTRstVal // This parameter is represented from Note23	
************	***************************************	

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- VOID Main(){
 - // Procedure : AaeonWDTConfig
 - // (byte)Timer : Time of WDT timer.(0x00~0xFF)
 - // (boolean)Unit : Select time unit(0: second, 1: minute).

AaeonWDTConfig();

// Procedure : AaeonWDTEnable

// This procudure will enable the WDT counting.

AaeonWDTEnable();

}

}

}

// Procedure : AaeonWDTEnable

VOID AaeonWDTEnable (){ WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);

// Procedure : AaeonWDTConfig

VOID AaeonWDTConfig (){

// Disable WDT counting WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0); // Clear Watchdog Timeout Status WDTClearTimeoutStatus(); // WDT relative parameter setting WDTParameterSetting();

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){ SIOBitSet(LDN, Register, BitNum, Value);

VOID WDTParameterSetting(){

// Watchdog Timer counter setting SIOByteSet(TimerLDN, TimerReg, TimerVal); // WDT counting unit setting SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal); // WDT output mode setting, level / pulse SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal); // Watchdog timeout output via WDTRST# SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);

}

VOID WDTClearTimeoutStatus(){ SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);

*****	***************************************
VOID	SIOEnterMBPnPMode(){ IOWriteByte(SIOIndex, 0x87); IOWriteByte(SIOIndex, 0x87);
VOID }	SIOExitMBPnPMode(){ IOWriteByte(SIOIndex, 0xAA);
VOID	SIOSelectLDN(byte LDN){ IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07 IOWriteByte(SIOData, LDN);
VOID	SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){ Byte TmpValue; SIOEnterMBPnPMode(); SIOSelectLDN(byte LDN); IOWriteByte(SIOIndex, Register); TmpValue = IOReadByte(SIOData); TmpValue &= ~(1 << BitNum); TmpValue &= ~(1 << BitNum); IOWriteByte(SIOData, TmpValue); SIOExitMBPnPMode();
VOID }	SIOByteSet(byte LDN, byte Register, byte Value){ SIOEnterMBPnPMode(); SIOSelectLDN(LDN); IOWriteByte(SIOIndex, Register); IOWriteByte(SIOData, Value); SIOExitMBPnPMode();

Appendix B

I/O Information

B.1 I/O Address Map

V III Input/output (IO)	
[00000000000000000 - 0000000000006F1 PCI Express Root Complex	
[0000000000000000000000000000000000000	ntroller
[0000000000000024 - 0000000000000000025] Programmable interrupt co	ntroller
[0000000000000028 - 000000000000000000000	ntroller
[000000000000002C - 0000000000000002D] Programmable interrupt co	ontroller
[000000000000002E - 00000000000002F] Motherboard resources	
[0000000000000000000000000000000000000	ntroller
[0000000000000034 - 0000000000000035] Programmable interrupt co	ntroller
[0000000000000038 - 00000000000000039] Programmable interrupt co	ntroller
[000000000000003C - 00000000000000000] Programmable interrupt co	ontroller
[00000000000000040 - 0000000000000043] System timer	
[000000000000004E - 00000000000004F] Motherboard resources	
[00000000000000050 - 000000000000053] System timer	
[0000000000000061 - 0000000000000061] Motherboard resources	
[0000000000000063 - 00000000000063] Motherboard resources	
🚋 [000000000000065 - 00000000000065] Motherboard resources	
[0000000000000067 - 00000000000067] Motherboard resources	
[000000000000000000000000000000000000	
time clo 🚛 [0000000000000070 - 0000000000000077] System CMOS/real time clo	ck
[000000000000078 - 000000000000CF7] PCI Express Root Complex	
🚛 [000000000000080 - 0000000000008F] Motherboard resources	
🛅 [000000000000092 - 000000000000092] Motherboard resources	
🏣 [0000000000000000 - 000000000000000000	ontroller
🏣 [00000000000000A4 - 00000000000000A5] Programmable interrupt co	ontroller
🚛 [0000000000000A8 - 0000000000000A9] Programmable interrupt co	ontroller
늘 [0000000000000AC - 000000000000AD] Programmable interrupt c	ontroller
들 [0000000000000080 - 000000000000081] Programmable interrupt co	ntroller
totherboard resources [0000000000000000083] [10000000000083] [10000000000000000082]	
🏣 [00000000000000B4 - 0000000000000B5] Programmable interrupt co	ntroller
🛅 [0000000000000B8 - 000000000000B9] Programmable interrupt co	ntroller
🛅 [0000000000000BC - 000000000000BD] Programmable interrupt c	ontroller
[0000000000002F8 - 000000000002FF] Communications Port (COI	v12)
[00000000000003E8 - 000000000003EF] Communications Port (COI	VI3)
[0000000000003F8 - 000000000003FF] Communications Port (COI	v11)
🛅 [0000000000000400 - 000000000000047F] Motherboard resources	
🚛 [0000000000004D0 - 000000000004D1] Programmable interrupt co	ontroller
늘 [00000000000000000 - 0000000000005FE] Motherboard resources	
🏣 [000000000000680 - 0000000000069F] Motherboard resources	
들 [0000000000000000 - 0000000000000000 Motherboard resources	
🚛 [0000000000000A10 - 000000000000A1F] Motherboard resources	

- 🏣 [0000000000000000 00000000000DFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port 5AD9

B.2 Memory Address Map

~	Memory	
	to 00000007B800001 - 000000007BFFFFF]	PCI Express Root Complex
	to 00000007C000001 - 000000007FFFFFF]	PCI Express Root Complex
	[00000008000000 - 00000008FFFFFF]	Intel(R) HD Graphics
	to 000000000000000000 - 0000000000000000	PCI Express Root Complex
	[00000009000000 - 000000090FFFFF]	Intel(R) HD Graphics
	[000000091000000 - 0000000910FFFF]	High Definition Audio Controller
	to 0000000091100000 - 00000000911FFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
	[00000000911DC000 - 0000000911DFFFF]	Intel(R) I211 Gigabit Network Connection #2
	[00000000911E0000 - 00000000911FFFFF]	Intel(R) I211 Gigabit Network Connection #2
	to 000000091200000 - 0000000912FFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
	[00000000912DC000 - 0000000912DFFF]	Intel(R) I211 Gigabit Network Connection
	[00000000912E0000 - 00000000912FFFF]	Intel(R) I211 Gigabit Network Connection
	[0000000091300000 - 000000009130FFFF]	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
	to 000000091310000 - 0000000091313FFF]	High Definition Audio Controller
	mage [0000000091314000 - 0000000091315FFF]	Standard SATA AHCI Controller
	Tel: [0000000091318000 - 00000000913180FF]	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
	mage [0000000091319000 - 00000000913197FF]	Standard SATA AHCI Controller
	mail[00000009131A000 - 000000009131A0FF]	Standard SATA AHCI Controller
	[000000009131E000 - 000000009131EFFF]	Intel(R) Trusted Execution Engine Interface
	Tel: [00000000000000 - 00000000000000000000	Intel(R) Serial IO GPIO Host Controller - INT3452
	[000000000000000000000000000000000000] Intel(R) Serial IO GPIO Host Controller - INT3452
	to 000000000000000000000000000000000000] Intel(R) Serial IO GPIO Host Controller - INT3452
	[000000000000000000000000000000000000] Intel(R) Serial IO GPIO Host Controller - INT3452
	10000000000000000000 - 0000000000000000	Motherboard resources
	[00000000E000000 - 0000000EFFFFFF]	PCI Express Root Complex
	Telefond (000000000000000000000000000000000000	Motherboard resources
	[00000000FED00000 - 00000000FED003FF]	High precision event timer
	Telefond - 00000000000000000000000000000000000	Motherboard resources
	[00000000FED03000 - 00000000FED03FFF]	Motherboard resources
	[0000000FED06000 - 0000000FED06FFF]	Motherboard resources
	[00000000FED08000 - 00000000FED09FFF]	Motherboard resources
	[0000000FED1C000 - 0000000FED1CFFF] Motherboard resources
	[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 2.0
	[00000000FED80000 - 00000000FEDBFFFF]	Motherboard resources
	[00000000FEE00000 - 00000000FEEFFFF]	Motherboard resources

B.3 IRQ Mapping Chart

✓	
to (ISA) 0x00000000 (00)	System timer
(ISA) 0x00000003 (03)	Communications Port (COM2)
(ISA) 0x00000004 (04)	Communications Port (COM1)
(ISA) 0x00000008 (08)	High precision event timer
(ISA) 0x0000000B (11)	Communications Port (COM3)
to (ISA) 0x000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
Tal: (ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
to (ISA) 0x000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452
(ISA) 0x0000000E (14)	Intel(R) Serial IO GPIO Host Controller - INT3452

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Appendix C

Glue Removal Procedure

C.1 Removing Glue from Your System

To protect components from damage and ensure proper operation out of the box, glue may have been applied to some cables or connectors to keep them in place during shipping. This glue must be removed before attempting to swap components or perform maintenance. This section details the steps needed to remove the glue.

Before performing any kind of system maintenance, ensure the system is shut down (not in sleep or hibernate mode) and the power cable has been removed. Follow steps in Chapter 2 to access the components inside.

You will need the following items for this step:

- Cotton or cotton swab
- Anti-static tweezers

- An alcohol solution that is at least 99.5% alcohol (ethanol solution or denatured alcohol). AAEON recommends using an eye dropper or a bottle with a nozzle as in the picture below:



Appendix C – Glue Removal Procedure
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Step 1: Using an eyedropper or bottle as shown above, apply a few drops of alcohol to the glue.

Step 2: Allow the alcohol to soak for 10 seconds, then use a cotton swab or cotton with anti-static tweezers to evenly rub the alcohol over the glue.



Step 3: Let soak for 10 more seconds, then use anti-static tweezers to remove the glue.



If you encounter any issues or need support, please contact your AAEON representative or visit our <u>Support Page</u> at AAEON.com.