

BOXER-6641

Fanless Embedded Box PC

User's Manual 2nd Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

| Item | Quantity |
|-------------------------------|----------|
| ● BOXER-6641 | 1 |
| ● Wallmount bracket | 2 |
| ● Screw Package | 1 |
| ● 3 Pin DC-In Power Connector | 1 |

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page at AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

产品中有毒有害物质或元素名称及含量

AAEON System

QO4-381 Rev.A0

| 部件名称 | 有毒有害物质或元素 | | | | | |
|-------------|-----------|-----------|-----------|-----------------|---------------|-----------------|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯 醚(PBDE) |
| 印刷电路板及其电子组件 | × | ○ | ○ | ○ | ○ | ○ |
| 外部信号连接器及线材 | × | ○ | ○ | ○ | ○ | ○ |
| 外壳 | ○ | ○ | ○ | ○ | ○ | ○ |
| 中央处理器与内存 | × | ○ | ○ | ○ | ○ | ○ |
| 硬盘 | × | ○ | ○ | ○ | ○ | ○ |
| 液晶模块 | × | × | ○ | ○ | ○ | ○ |
| 光驱 | × | ○ | ○ | ○ | ○ | ○ |
| 触控模块 | × | ○ | ○ | ○ | ○ | ○ |
| 电源 | × | ○ | ○ | ○ | ○ | ○ |
| 电池 | × | ○ | ○ | ○ | ○ | ○ |

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在 GB/T 26572 标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了 GB/T 26572 的限量要求，然而该部件

仍符合欧盟指令 2011/65/EU 的规范。

备注：

- 一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
- 二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。
- 三、上述部件物质液晶模块、触控模块仅一体机产品适用。

Hazardous and Toxic Materials List

AAEON System

QO4-381 Rev.A0

| Component Name | Hazardous or Toxic Materials or Elements | | | | | |
|--|--|--------------|--------------|------------------------------|---------------------------------|--|
| | Lead (Pb) | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (Cr(VI)) | Polybrominated biphenyls (PBBS) | Polybrominated diphenyl ethers (PBDES) |
| PCB and Components | X | O | O | O | O | O |
| Wires & Connectors for Ext.Connections | X | O | O | O | O | O |
| Chassis | O | O | O | O | O | O |
| CPU & RAM | X | O | O | O | O | O |
| HDD Drive | X | O | O | O | O | O |
| LCD Module | X | X | O | O | O | O |
| Optical Drive | X | O | O | O | O | O |
| Touch Control Module | X | O | O | O | O | O |
| PSU | X | O | O | O | O | O |
| Battery | X | O | O | O | O | O |

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

Notes:

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.
2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

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Chapter 1

Product Specifications

1.1 Specifications

System

| | |
|-------------------|---|
| CPU | Intel® Xeon® E-2124G (A2 only) Intel® i9-9900T Intel® i7-9700TE Intel® i7-8700T Intel® i5-8500T Intel® i3-8100T Pentium® G5400T Celeron® G4900T |
| Chipset | Intel® C246/H310 |
| System Memory | DDR4 2666MHz SO-DIMM slot x 2, up to 32GB, ECC or Non-ECC Supported |
| Display Interface | HDMI x 2 |
| Storage Device | 2.5" SATA HDD/SSD Bay x 1 (Optional x 2) |
| Ethernet | — |
| I/O | HDMI x 2 RJ-45 x 4 for GbE LAN (i211 x 3, i219 x 1) USB3.2 Gen 1 x 4, USB2.0 x 4 (H310) USB3.2 Gen 1 x 8 (C246) DB-9 x 6 for RS-232/422/485 Audio x 1 (MIC-in, Line-out) 3-pin 10~35V DC Power Input x 1 Power Button x 1 Remote Power Switch x 1 Reset Button x 1 HDD LED x 1 SYS LED x 1 |
| Expansion | Full-size Mini card x 2 (w/ SIM Slot x 1, optional for mSATA x 1) |
| Indicator | HDD LED x 1 SYS LED x 1 |

System

| | |
|------------|--|
| OS Support | Windows® 10 64-bit Linux Ubuntu 18.04 |
|------------|--|

Power Supply

| | |
|-------------------|-----------------------|
| Power Requirement | 3-pin DC Input 10~35V |
|-------------------|-----------------------|

Mechanical

| | |
|------------------------|---|
| Mounting | Wallmount |
| Dimensions (W x H x D) | 10.4" x 3.19" x 6.15" (264.2mm x 80.92mm x 156.2mm) |
| Gross Weight | 16.4 lbs. (7.0 kg) |
| Net Weight | 13.72 lbs. (6.2 kg) |

Environmental

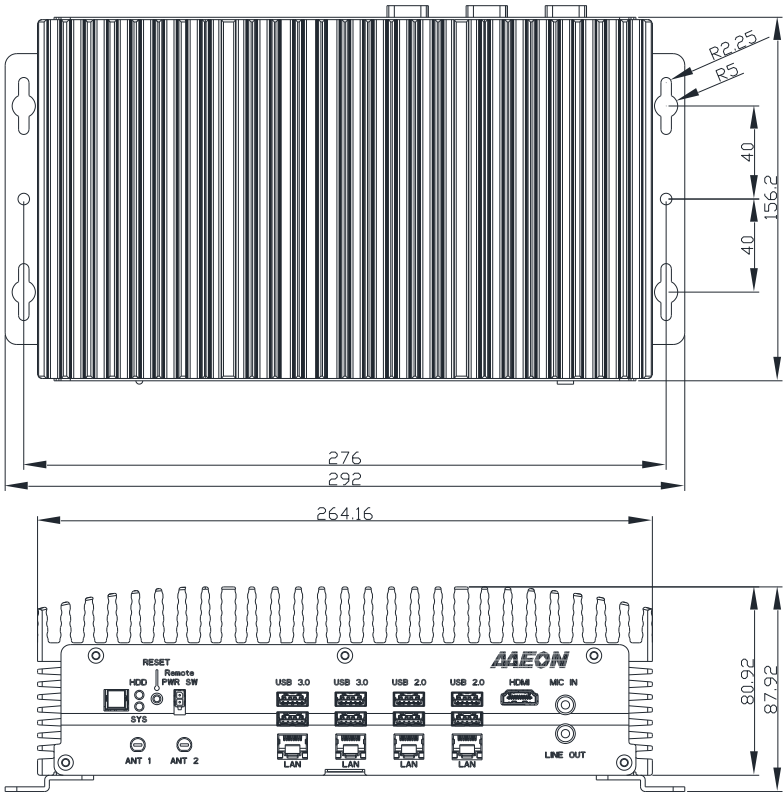
| | |
|-----------------------|--|
| Operating Temperature | -4°F ~ 131°F (-20°C ~ 55°C) with 0.5 m/s airflow with TDP ≤ 35W CPU -4°F ~ 113°F (-20°C ~ 45°C) with 0.5 m/s airflow with TDP > 35W CPU |
| Storage Temperature | -40°F ~ 176°F (-40°C ~ 80°C) |
| Storage Humidity | 5 ~ 95% @ 40°C, non-condensing |
| Anti-Vibration | 2 Grms/ 5 ~ 500Hz/ operation – SSD/mSATA |
| Certification | CE/FCC class A |

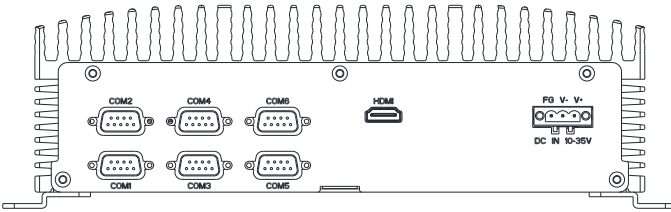
Chapter 2

Hardware Information

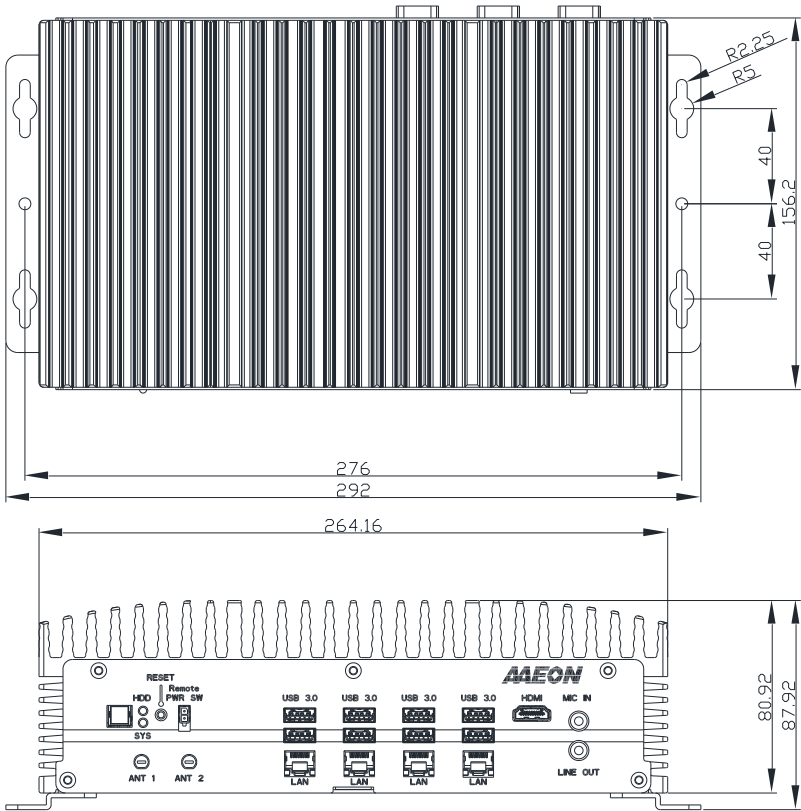
2.1 BOXER-6641 Dimensions

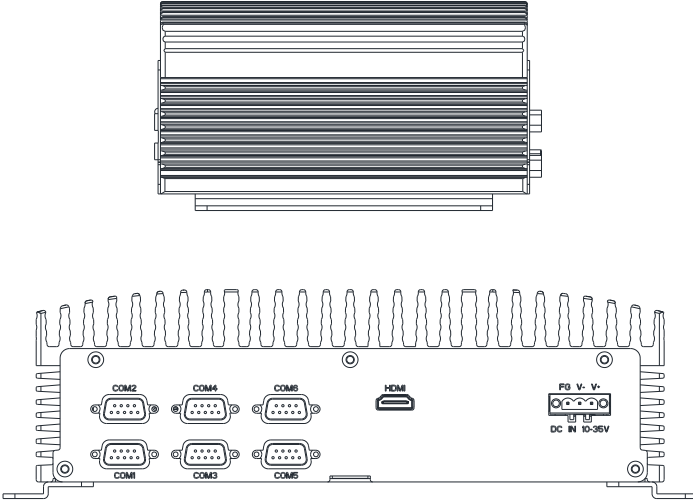
BOXER-6641-A1 (H310 Chipset)





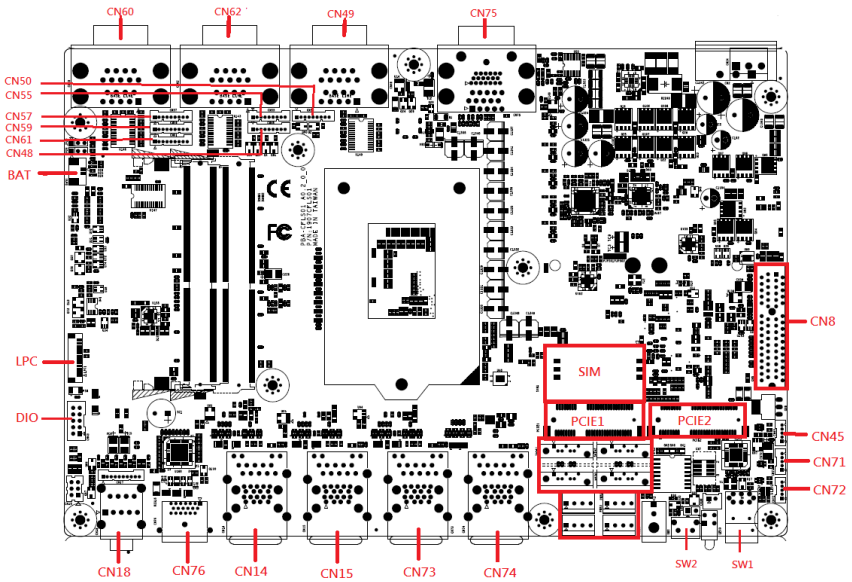
BOXER-6641-A2 (C246 Chipset)

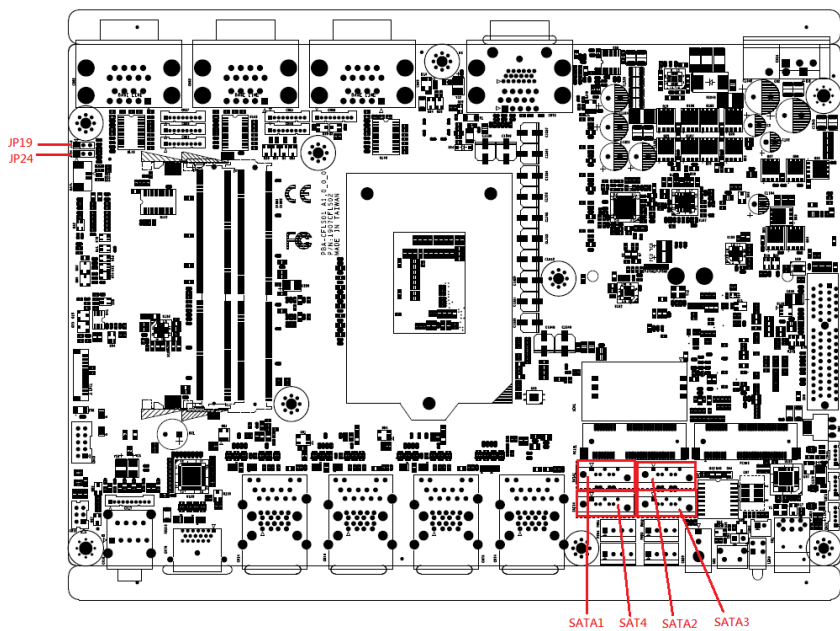




2.2 Jumpers and Connectors

Note: Board dimensions are 225mm x 151.5mm x 1.8mm





2.3 List of Jumpers

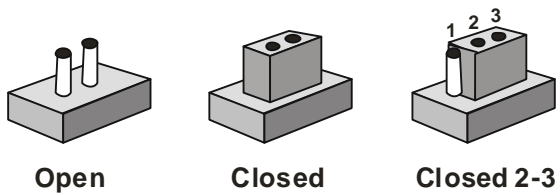
Please refer to the table below for all of the system's jumpers that you can configure for your application.

| Label | Function |
|-------|-------------------------------------|
| JP19 | ATX/AT Mode Selection |
| JP24 | CMOS Control Selection (Clear CMOS) |

2.3.1 Setting Jumpers

You can configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip.

To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.

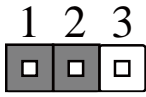


A pair of needle-nose pliers may be helpful when working with jumpers.

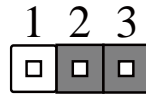
If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

2.3.2 ATX/ AT Mode Selection (JP19)



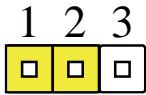
ATX (default)



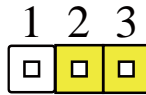
AT

Note: Disable Auto Power Button JP1 (1-2) requires user to use power button JP1 (1-2) to power on the system.

2.3.3 CMOS Control Selection (JP24)



Normal (Default)



Clear CMOS

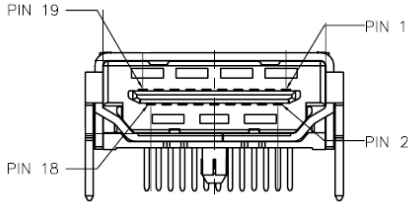
2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

| Label | Function |
|-------|---------------------------------------|
| BAT1 | RTC Battery |
| CN7 | SPI flash port |
| CN8 | PCIE [x4] Slot |
| CN14 | LAN+USB3.2 Gen 1 x2 Connector |
| CN15 | LAN+USB3.2 Gen 1 x2 Connector |
| CN17 | Audio Wafer |
| CN18 | Audio Connector |
| CN20 | Remote Button |
| CN23 | Phoenix Connector Power Input |
| CN43 | DIO (Wafer Box) |
| CN45 | USB2.0 (HEADER) |
| CN48 | COM5 HEADER RS232/RS422/RS485 |
| CN49 | COM5+COM6 Connector RS232/RS422/RS485 |
| CN50 | COM6 HEADER RS232/RS422/RS485 |
| CN55 | COM4 HEADER RS232/RS422/RS485 |
| CN57 | COM2 HEADER RS232/RS422/RS485 |
| CN59 | COM1 HEADER RS232/RS422/RS485 |
| CN60 | COM1+COM2 Connector RS232/RS422/RS485 |
| CN61 | COM3 HEADER RS232/RS422/RS485 |
| CN62 | COM3+COM4 Connector RS232/RS422/RS485 |
| CN71 | USB2.0 (HEADER) |
| CN72 | USB2.0 (HEADER) |

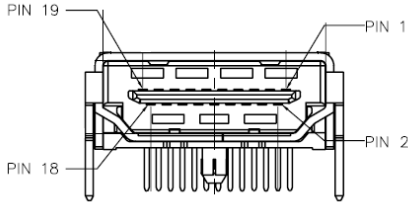
| Label | Function |
|-------|---|
| CN73 | LAN+USB3.2 Gen 1 x2 Connector (USB2.0x2 for H310 Chipset) |
| CN74 | LAN+USB3.2 Gen 1 x2 Connector (USB2.0x2 for H310 Chipset) |
| CN75 | HDMI Port |
| CN76 | HDMI Port |
| LPC1 | LPC Port |
| PCIE1 | Mini-PCIE slot |
| PCIE2 | Mini-PCIE slot |
| PWR1 | SATA PWR Connector |
| PWR2 | SATA PWR Connector |
| PWR3 | SATA PWR Connector |
| PWR4 | SATA PWR Connector |
| SATA1 | SATA1 |
| SATA2 | SATA2 |
| SATA3 | SATA3 |
| SATA4 | SATA4 |
| SIM1 | SIM Card Slot |
| SW1 | Power Button |
| SW2 | Reset Switch |

2.4.1 HDMI Port (CN75)



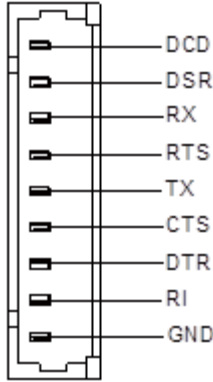
| Pin | Signal | Signal Type | Signal Level |
|-----|---------------|-------------|--------------|
| 1 | HDMI2_DATA2_P | DIFF | |
| 2 | GND | | |
| 3 | HDMI2_DATA2_N | DIFF | |
| 4 | HDMI2_DATA1_P | DIFF | |
| 5 | GND | | |
| 6 | HDMI2_DATA1_N | DIFF | |
| 7 | HDMI2_DATA0_P | DIFF | |
| 8 | GND | | |
| 9 | HDMI2_DATA0_N | DIFF | |
| 10 | HDMI2_CLK_P | DIFF | |
| 11 | GND | GND | |
| 12 | HDMI2_CLK_N | I/O | |
| 13 | NC | I/O | |
| 14 | NC | | |
| 15 | SCL | I/O | |
| 16 | SDA | I/O | |
| 17 | GND | GND | |
| 18 | PWR | PWR | 5V |
| 19 | HPD | I/O | |

2.4.2 HDMI Port (CN76)



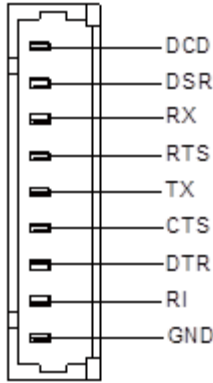
| Pin | Signal | Signal Type | Signal Level |
|-----|---------------|-------------|--------------|
| 1 | HDMI2_DATA2_P | DIFF | |
| 2 | GND | | |
| 3 | HDMI2_DATA2_N | DIFF | |
| 4 | HDMI2_DATA1_P | DIFF | |
| 5 | GND | | |
| 6 | HDMI2_DATA1_N | DIFF | |
| 7 | HDMI2_DATA0_P | DIFF | |
| 8 | GND | | |
| 9 | HDMI2_DATA0_N | DIFF | |
| 10 | HDMI2_CLK_P | DIFF | |
| 11 | GND | GND | |
| 12 | HDMI2_CLK_N | I/O | |
| 13 | NC | I/O | |
| 14 | NC | | |
| 15 | SCL | I/O | |
| 16 | SDA | I/O | |
| 17 | GND | GND | |
| 18 | PWR | PWR | 5V |
| 19 | HPD | I/O | |

2.4.3 COM Port 1 (Wafer Box, Optional) (CN59)



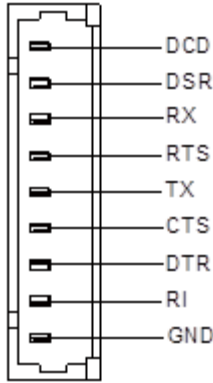
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD1 | IN | |
| 2 | DSR1 | IN | |
| 3 | RX1 | IN | |
| 4 | RTS1 | OUT | ±9V |
| 5 | TX1 | OUT | ±9V |
| 6 | CTS1 | IN | |
| 7 | DTR1 | OUT | ±9V |
| 8 | RI1 | IN | |
| 9 | GND | GND | |

2.4.4 COM Port 2 (Wafer Box, Optional) (CN57)



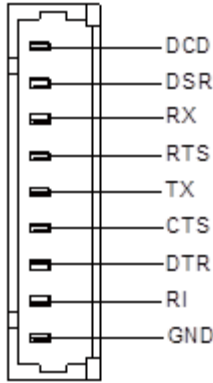
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD2 | IN | |
| 2 | DSR2 | IN | |
| 3 | RX2 | IN | |
| 4 | RTS2 | OUT | ±9V |
| 5 | TX2 | OUT | ±9V |
| 6 | CTS2 | IN | |
| 7 | DTR2 | OUT | ±9V |
| 8 | RI2 | IN | |
| 9 | GND | GND | |

2.4.5 COM Port 3 (Wafer Box, Optional) (CN61)



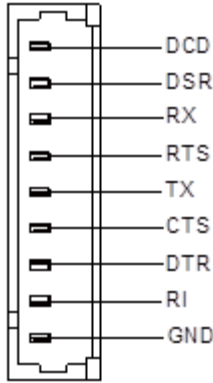
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD3 | IN | |
| 2 | DSR3 | IN | |
| 3 | RX3 | IN | |
| 4 | RTS3 | OUT | ±9V |
| 5 | TX3 | OUT | ±9V |
| 6 | CTS3 | IN | |
| 7 | DTR3 | OUT | ±9V |
| 8 | RI3 | IN | |
| 9 | GND | GND | |

2.4.6 COM Port 4 (Wafer Box, Optional) (CN55)



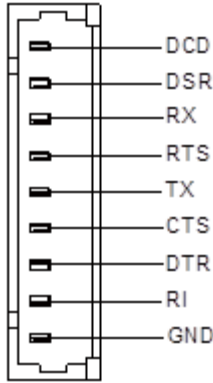
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD4 | IN | |
| 2 | DSR4 | IN | |
| 3 | RX4 | IN | |
| 4 | RTS4 | OUT | ±9V |
| 5 | TX4 | OUT | ±9V |
| 6 | CTS4 | IN | |
| 7 | DTR4 | OUT | ±9V |
| 8 | RI4 | IN | |
| 9 | GND | GND | |

2.4.7 COM Port 5 (Wafer Box, Optional) (CN48)



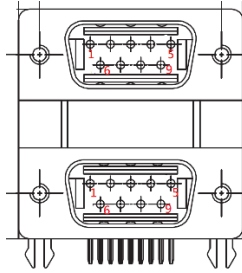
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD5 | IN | |
| 2 | DSR5 | IN | |
| 3 | RX5 | IN | |
| 4 | RTS5 | OUT | ±9V |
| 5 | TX5 | OUT | ±9V |
| 6 | CTS5 | IN | |
| 7 | DTR5 | OUT | ±9V |
| 8 | RI5 | IN | |
| 9 | GND | GND | |

2.4.8 COM Port 6 (Wafer Box, Optional) (CN50)



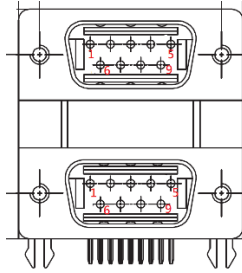
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DCD6 | IN | |
| 2 | DSR6 | IN | |
| 3 | RX6 | IN | |
| 4 | RTS6 | OUT | ±9V |
| 5 | TX6 | OUT | ±9V |
| 6 | CTS6 | IN | |
| 7 | DTR6 | OUT | ±9V |
| 8 | RI6 | IN | |
| 9 | GND | GND | |

2.4.9 COM1 + COM2 Connector RS232/RS422/RS485 (CN60)



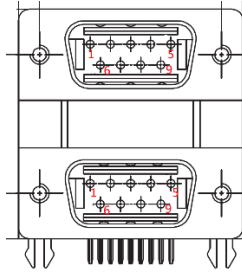
| Pin | RS232 | RS422 | RS485 |
|--------------------|-------|-------|-------|
| Top Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |
| Bottom Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |

2.4.10 COM3 + COM4 Connector RS232/RS422/RS485 (CN62)



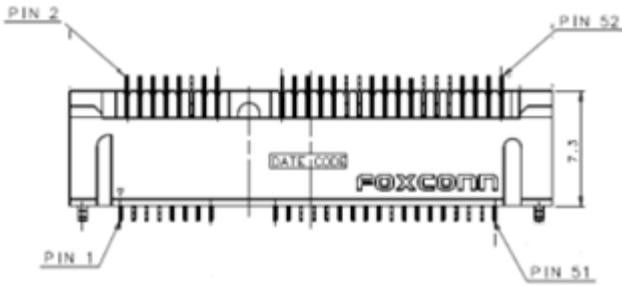
| Pin | RS232 | RS422 | RS485 |
|--------------------|-------|-------|-------|
| Top Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |
| Bottom Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |

2.4.11 COM5 + COM6 Connector RS232/RS422/RS485 (CN49)



| Pin | RS232 | RS422 | RS485 |
|--------------------|-------|-------|-------|
| Top Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |
| Bottom Port | | | |
| 1 | DCD | TX- | D- |
| 2 | RX | TX+ | D+ |
| 3 | TX | RX+ | NC |
| 4 | DTR | RX- | NC |
| 5 | GND | NC | NC |
| 6 | DSR | NC | NC |
| 7 | RTS | NC | NC |
| 8 | CTS | NC | NC |
| 9 | RI | NC | NC |

2.4.12 Mini-Card Slot (Full Mini-Card) (PCIe1)

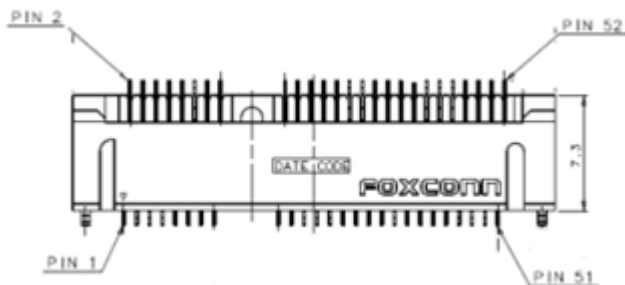


| Pin | Signal | Signal Type | Signal Level |
|-----|---------------|-------------|--------------|
| 1 | PCIE_WAKE# | IN | |
| 2 | +3.3V | PWR | +3.3V |
| 3 | NC | | |
| 4 | GND | GND | |
| 5 | NC | | |
| 6 | +1.5V | PWR | +1.5V |
| 7 | PCIE_CLK_REQ# | IN | |
| 8 | NC | PWR | |
| 9 | GND | GND | |
| 10 | NC | I/O | |
| 11 | PCIE_REF_CLK- | DIFF | |
| 12 | NC | IN | |
| 13 | PCIE_REF_CLK+ | DIFF | |
| 14 | NC | IN | |
| 15 | GND | GND | |
| 16 | NC | PWR | |
| 17 | NC | | |

| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 18 | GND | GND | |
| 19 | NC | | |
| 20 | W_DISABLE# | OUT | +3.3V |
| 21 | GND | GND | |
| 22 | PCIE_RST# | OUT | +3.3V |
| 23 | PCIE_RX- | DIFF | |
| 24 | +3.3VSB | PWR | +3.3V |
| 25 | PCIE_RX+ | DIFF | |
| 26 | GND | GND | |
| 27 | GND | GND | |
| 28 | +1.5V | PWR | +1.5V |
| 29 | GND | GND | |
| 30 | SMB_CLK | I/O | +3.3V |
| 31 | PCIE_TX- | DIFF | |
| 32 | SMB_DATA | I/O | +3.3V |
| 33 | PCIE_TX+ | DIFF | |
| 34 | GND | GND | |
| 35 | GND | GND | |
| 36 | USB_D- | DIFF | |
| 37 | GND | GND | |
| 38 | USB_D+ | DIFF | |
| 39 | +3.3VSB | PWR | +3.3V |
| 40 | GND | GND | |
| 41 | +3.3VSB | PWR | +3.3V |
| 42 | NC | | |
| 43 | GND | GND | |

| Pin | Signal | Signal Type | Signal Level |
|-----|---------|-------------|--------------|
| 44 | NC | | |
| 45 | NC | | |
| 46 | NC | | |
| 47 | NC | | |
| 48 | +1.5V | PWR | +1.5V |
| 49 | NC | | |
| 50 | GND | GND | |
| 51 | NC | | |
| 52 | +3.3VSB | PWR | +3.3V |

2.4.13 Mini-Card Slot (Full Mini-Card) (PCIE2)

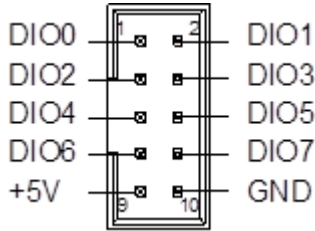


| Pin | Signal | Signal | Signal Level |
|-----|---------------|--------|--------------|
| 1 | PCIE_WAKE# | IN | |
| 2 | +3.3V | PWR | +3.3V |
| 3 | NC | | |
| 4 | GND | GND | |
| 5 | NC | | |
| 6 | +1.5V | PWR | +1.5V |
| 7 | PCIE_CLK_REQ# | IN | |

| Pin | Signal | Signal | Signal Level |
|-----|---------------|--------|--------------|
| 8 | NC | PWR | |
| 9 | GND | GND | |
| 10 | NC | I/O | |
| 11 | PCIE_REF_CLK- | DIFF | |
| 12 | NC | IN | |
| 13 | PCIE_REF_CLK+ | DIFF | |
| 14 | NC | IN | |
| 15 | GND | GND | |
| 16 | NC | PWR | |
| 17 | NC | | |
| 18 | GND | GND | |
| 19 | NC | | |
| 20 | W_DISABLE# | OUT | +3.3V |
| 21 | GND | GND | |
| 22 | PCIE_RST# | OUT | +3.3V |
| 23 | PCIE_RX- | DIFF | |
| 24 | +3.3VSB | PWR | +3.3V |
| 25 | PCIE_RX+ | DIFF | |
| 26 | GND | GND | |
| 27 | GND | GND | |
| 28 | +1.5V | PWR | +1.5V |
| 29 | GND | GND | |
| 30 | SMB_CLK | I/O | +3.3V |
| 31 | PCIE_TX- | DIFF | |
| 32 | SMB_DATA | I/O | +3.3V |
| 33 | PCIE_TX+ | DIFF | |

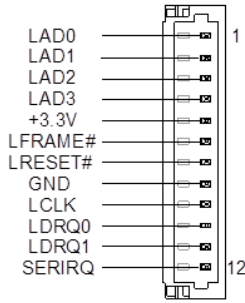
| Pin | Signal | Signal | Signal Level |
|-----|---------|--------|--------------|
| 34 | GND | GND | |
| 35 | GND | GND | |
| 36 | USB_D- | DIFF | |
| 37 | GND | GND | |
| 38 | USB_D+ | DIFF | |
| 39 | +3.3VSB | PWR | +3.3V |
| 40 | GND | GND | |
| 41 | +3.3VSB | PWR | +3.3V |
| 42 | NC | | |
| 43 | GND | GND | |
| 44 | NC | | |
| 45 | NC | | |
| 46 | NC | | |
| 47 | NC | | |
| 48 | +1.5V | PWR | +1.5V |
| 49 | NC | | |
| 50 | GND | GND | |
| 51 | NC | | |
| 52 | +3.3VSB | PWR | +3.3V |

2.4.14 Digital IO Port (CN43)



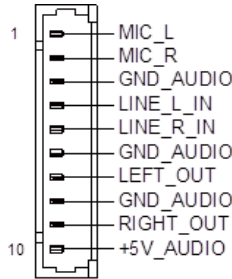
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | DIO0 | I/O | +5V |
| 2 | DIO1 | I/O | +5V |
| 3 | DIO2 | I/O | +5V |
| 4 | DIO3 | I/O | +5V |
| 5 | DIO4 | I/O | +5V |
| 6 | DIO5 | I/O | +5V |
| 7 | DIO6 | I/O | +5V |
| 8 | DIO7 | I/O | +5V |
| 9 | +5V | PWR | +5V |
| 10 | GND | GND | |

2.4.15 LPC Port (LPC1)



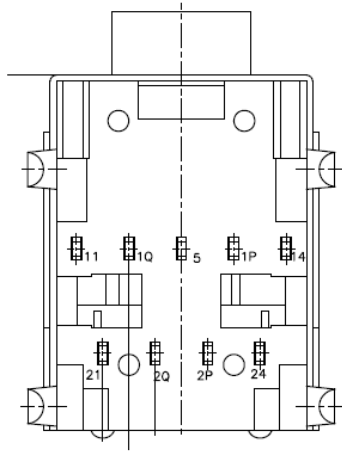
| Pin | Signal | Signal Type | Signal Level |
|-----|---------|-------------|--------------|
| 1 | LAD0 | I/O | +3.3V |
| 2 | LAD1 | I/O | +3.3V |
| 3 | LAD2 | I/O | +3.3V |
| 4 | LAD3 | I/O | +3.3V |
| 5 | +3.3V | PWR | +3.3V |
| 6 | LFRAME# | IN | |
| 7 | LRESET# | OUT | +3.3V |
| 8 | GND | GND | |
| 9 | LCLK | OUT | |
| 10 | LDRQ0 | IN | |
| 11 | LDRQ1 | IN | |
| 12 | SERIRQ | I/O | +3.3V |

2.4.16 Audio I/O Port (10P Pitch: 1.25mm) (CN17)



| Pin | Signal | Signal Type | Signal Level |
|-----|-----------|-------------|--------------|
| 1 | MIC_L | IN | |
| 2 | MIC_R | IN | |
| 3 | GND_AUDIO | GND | |
| 4 | LINE_L_IN | IN | |
| 5 | LINE_R_IN | IN | |
| 6 | GND_AUDIO | GND | |
| 7 | LEFT_OUT | OUT | |
| 8 | GND_AUDIO | GND | |
| 9 | RIGHT_OUT | OUT | |
| 10 | +5V_AUDIO | PWR | +5V |

2.4.17 Audio Connector (CN18)

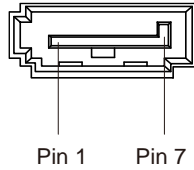


| Pin | Signal | Signal Type | Signal Level |
|-----|----------|-------------|--------------|
| 5 | AUD_GND | GND | |
| 24 | LOUT_L | OUT | |
| 21 | LOUT_R | OUT | |
| 2P | HP_DET_3 | IN | |
| 2Q | HP_DET_4 | IN | |
| 14 | MIC_L | IN | |
| 11 | MIC_R | IN | |
| 1P | HP_DET_1 | IN | |
| 1Q | HP_DET2 | IN | |

2.4.18 SPI Flash Port (CN7)

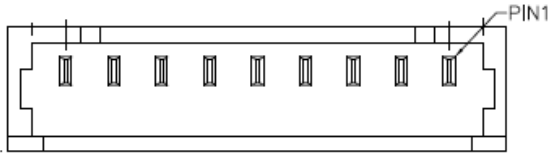
| Pin | Signal | Signal Type | Signal Level |
|-----|----------|-------------|--------------|
| 1 | SPI_MISO | OUT | |
| 2 | GND | GND | |
| 3 | SPI_CLK | IN | |
| 4 | +3.3VSB | PWR | +3.3V |
| 5 | SPI_MOSI | IN | |
| 6 | SPI_CS | IN | |
| 7 | NC | | |
| 8 | NC | | |

2.4.19 SATA Port (SATA 1,2,3,4)



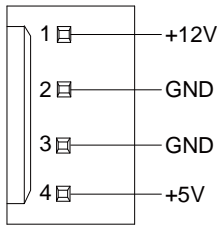
| Pin | Signal | Signal Type | Signal Level |
|-----|----------|-------------|--------------|
| 1 | GND | GND | |
| 2 | SATA_TX+ | DIFF | |
| 3 | SATA_TX- | DIFF | |
| 4 | GND | GND | |
| 5 | SATA_RX- | DIFF | |
| 6 | SATA_RX+ | DIFF | |
| 7 | GND | GND | |

2.4.20 USB2.0 Wafer BOX (5P Pitch: 1.25mm) (CN 45,71,72)



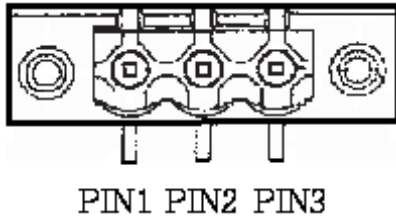
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | +5V | GND | +5V |
| 2 | USBD- | DIFF | |
| 3 | USBD+ | DIFF | |
| 4 | GND | GND | |
| 5 | GND | GND | |

2.4.21 SATA PWR (PWR 1,2,3,4)



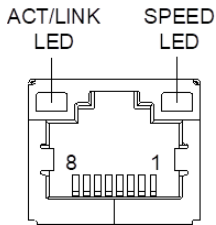
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | +12V | PWR | +12V |
| 2 | GND | GND | |
| 3 | GND | GND | |
| 4 | +5V | PWR | +5V |

2.4.22 DC-IN Connector (CN23)



| Pin | Signal | Signal Type | Signal Level |
|-----|-----------|-------------|--------------|
| 1 | VIN | PWR | +10V~+35V |
| 2 | GND | GND | |
| 3 | GND_EARTH | | |

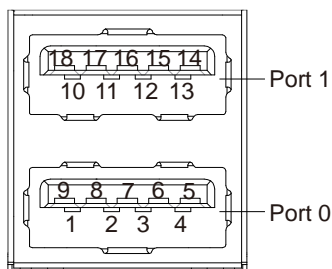
2.4.23 LAN (RJ-45) + Dual USB3.2 Gen 1 (CN74)



| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | MDIO+ | DIFF | |
| 2 | MDIO- | DIFF | |
| 3 | MDI1+ | DIFF | |
| 4 | MDI2+ | DIFF | |
| 5 | MDI2- | DIFF | |
| 6 | MDI1- | DIFF | |

| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 7 | MDI3+ | DIFF | |
| 8 | MDI3- | DIFF | |

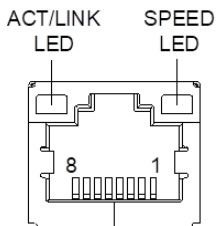
Note: USB2.0x2 for H310 Chipset



| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 1 | +5VSB | PWR | +5V |
| 2 | USB1_D- | DIFF | |
| 3 | USB1_D+ | DIFF | |
| 4 | GND | GND | |
| 5 | USB1_SSRX- | DIFF | |
| 6 | USB1_SSRX+ | DIFF | |
| 7 | GND | GND | |
| 8 | USB1_SSTX- | DIFF | |
| 9 | USB1_SSTX+ | DIFF | |
| 10 | +5VSB | PWR | +5V |
| 11 | USB2_D- | DIFF | |
| 12 | USB2_D+ | DIFF | |
| 13 | GND | GND | |
| 14 | USB2_SSRX- | DIFF | |

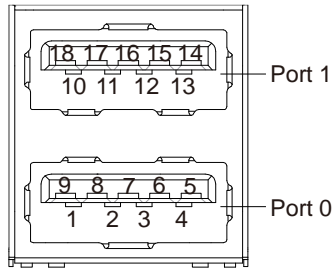
| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 15 | USB2_SSRX+ | DIFF | |
| 16 | GND | GND | |
| 17 | USB2_SSTX- | DIFF | |
| 18 | USB2_SSTX+ | DIFF | |

2.4.24 LAN (RJ-45) + Dual USB3.2 Gen 1 (CN73)



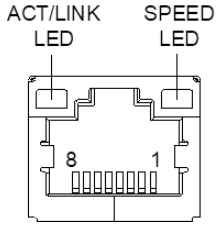
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | MDI0+ | DIFF | |
| 2 | MDI0- | DIFF | |
| 3 | MDI1+ | DIFF | |
| 4 | MDI2+ | DIFF | |
| 5 | MDI2- | DIFF | |
| 6 | MDI1- | DIFF | |
| 7 | MDI3+ | DIFF | |
| 8 | MDI3- | DIFF | |

Note: USB2.0x2 for H310 Chipset

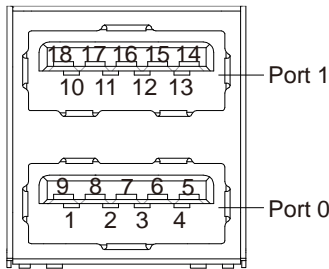


| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 1 | +5VSB | PWR | +5V |
| 2 | USB3_D- | DIFF | |
| 3 | USB3_D+ | DIFF | |
| 4 | GND | GND | |
| 5 | USB3_SSRX- | DIFF | |
| 6 | USB3_SSRX+ | DIFF | |
| 7 | GND | GND | |
| 8 | USB3_SSTX- | DIFF | |
| 9 | USB3_SSTX+ | DIFF | |
| 10 | +5VSB | PWR | +5V |
| 11 | USB4_D- | DIFF | |
| 12 | USB4_D+ | DIFF | |
| 13 | GND | GND | |
| 14 | USB4_SSRX- | DIFF | |
| 15 | USB4_SSRX+ | DIFF | |
| 16 | GND | GND | |
| 17 | USB4_SSTX- | DIFF | |
| 18 | USB4_SSTX+ | DIFF | |

2.4.25 LAN (RJ-45) + Dual USB3.2 Gen 1 (CN15)



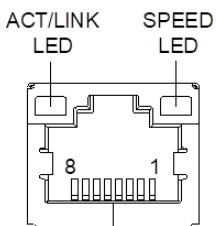
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | MDIO+ | DIFF | |
| 2 | MDIO- | DIFF | |
| 3 | MDI1+ | DIFF | |
| 4 | MDI2+ | DIFF | |
| 5 | MDI2- | DIFF | |
| 6 | MDI1- | DIFF | |
| 7 | MDI3+ | DIFF | |
| 8 | MDI3- | DIFF | |



| Pin | Signal | Signal Type | Signal Level |
|-----|---------|-------------|--------------|
| 1 | +5VSB | PWR | +5V |
| 2 | USB5_D- | DIFF | |

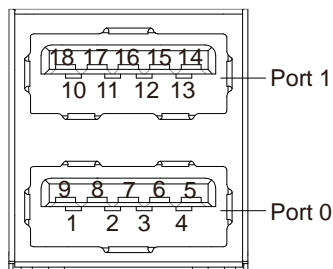
| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 3 | USB5_D+ | DIFF | |
| 4 | GND | GND | |
| 5 | USB5_SSRX- | DIFF | |
| 6 | USB5_SSRX+ | DIFF | |
| 7 | GND | GND | |
| 8 | USB5_SSTX- | DIFF | |
| 9 | USB5_SSTX+ | DIFF | |
| 10 | +5VSB | PWR | +5V |
| 11 | USB6_D- | DIFF | |
| 12 | USB6_D+ | DIFF | |
| 13 | GND | GND | |
| 14 | USB6_SSRX- | DIFF | |
| 15 | USB6_SSRX+ | DIFF | |
| 16 | GND | GND | |
| 17 | USB6_SSTX- | DIFF | |
| 18 | USB6_SSTX+ | DIFF | |

2.4.26 LAN (RJ-45) + Dual USB3.2 Gen 1 (CN14)



| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 1 | MDIO+ | DIFF | |

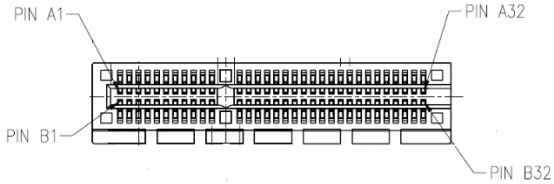
| Pin | Signal | Signal Type | Signal Level |
|-----|--------|-------------|--------------|
| 2 | MDI0- | DIFF | |
| 3 | MDI1+ | DIFF | |
| 4 | MDI2+ | DIFF | |
| 5 | MDI2- | DIFF | |
| 6 | MDI1- | DIFF | |
| 7 | MDI3+ | DIFF | |
| 8 | MDI3- | DIFF | |



| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 1 | +5VSB | PWR | +5V |
| 2 | USB7_D- | DIFF | |
| 3 | USB7_D+ | DIFF | |
| 4 | GND | GND | |
| 5 | USB7_SSRX- | DIFF | |
| 6 | USB7_SSRX+ | DIFF | |
| 7 | GND | GND | |
| 8 | USB7_SSTX- | DIFF | |
| 9 | USB7_SSTX+ | DIFF | |
| 10 | +5VSB | PWR | +5V |

| Pin | Signal | Signal Type | Signal Level |
|-----|------------|-------------|--------------|
| 11 | USB8_D- | DIFF | |
| 12 | USB8_D+ | DIFF | |
| 13 | GND | GND | |
| 14 | USB8_SSRX- | DIFF | |
| 15 | USB8_SSRX+ | DIFF | |
| 16 | GND | GND | |
| 17 | USB8_SSTX- | DIFF | |
| 18 | USB8_SSTX+ | DIFF | |

2.4.27 PCIe [x4] Slot (CN8)



| Pin | Signal | Signal | Signal |
|-----|-----------|--------|--------|
| A1 | PRSNT1# | I/O | |
| A2 | +12V | PWR | +V12S |
| A3 | +12V | PWR | +V12S |
| A4 | GND | GND | |
| A5 | PCIE_TXN5 | DIFF | |
| A6 | PCIE_TXP5 | DIFF | |
| A7 | PCIE_RXN5 | DIFF | |
| A8 | PCIE_RXP5 | DIFF | |

| Pin | Signal | Signal | Signal |
|-----|------------------|--------|--------|
| A9 | +3.3V | PWR | +V3.3S |
| A10 | +3.3V | PWR | +V3.3S |
| A11 | PERST# | I/O | |
| A12 | GND | GND | |
| A13 | PCIE_x4SLOT_CLK | DIFF | |
| A14 | PCIE_x4SLOT_CLK# | DIFF | |
| A15 | GND | GND | |
| A16 | PCIE_RXP24 | DIFF | |
| A17 | PCIE_RXN24 | DIFF | |
| A18 | GND | GND | |
| A19 | NC | | |
| A20 | GND | GND | |
| A21 | PCIE_RXP23 | DIFF | |
| A22 | PCIE_RXN23 | DIFF | |
| A23 | GND | GND | |
| A24 | GND | GND | |
| A25 | PCIE_RXP22 | DIFF | |
| A26 | PCIE_RXP22 | DIFF | |
| A27 | GND | GND | |
| A28 | GND | GND | |
| A29 | PCIE_RXP21 | DIFF | |
| A30 | PCIE_RXN21 | DIFF | |
| A31 | GND | GND | |
| A32 | NC | | |
| B1 | +12V | PWR | +V12S |
| B2 | +12V | PWR | +V12S |

| Pin | Signal | Signal | Signal |
|-----|------------|--------|--------|
| B3 | +12V | PWR | +V12S |
| B4 | GND | GND | |
| B5 | SMB_CLK | I/O | |
| B6 | SMB_DATA | I/O | |
| B7 | GND | GND | |
| B8 | +V3.3S | PWR | +V3.3S |
| B9 | NC | | |
| B10 | 3.3Vaux | PWR | +V3.3A |
| B11 | WAKE# | I/O | |
| B12 | NC | | |
| B13 | GND | GND | |
| B14 | PCIE_TXP24 | DIFF | |
| B15 | PCIE_TXN24 | DIFF | |
| B16 | GND | GND | |
| B17 | PRSNT | I/O | |
| B18 | GND | GND | |
| B19 | PCIE_TXP23 | DIFF | |
| B20 | PCIE_TXN23 | DIFF | |
| B21 | GND | GND | |
| B22 | GND | GND | |
| B23 | PCIE_TXP22 | DIFF | |
| B24 | PCIE_TXN22 | DIFF | |
| B25 | GND | GND | |
| B26 | GND | GND | |
| B27 | PCIE_TXP21 | DIFF | |
| B28 | PCIE_TXN21 | DIFF | |

| Pin | Signal | Signal | Signal |
|-----|--------|--------|--------|
| B29 | GND | GND | |
| B30 | NC | | |
| B31 | PRSNT | I/O | |
| B32 | GND | GND | |

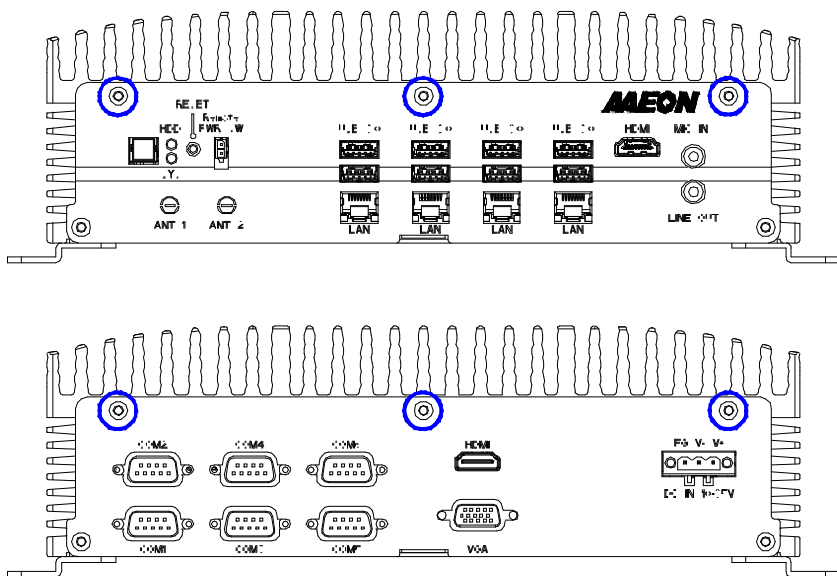
2.4.28 SIM Slot (SIM1)

| Pin | Signal | Signal Type | Signal Level |
|-----|----------|-------------|--------------|
| 1 | UIM_PWR | PWR | |
| 2 | UIM_RST | IN | |
| 3 | UIM_CLK | IN | |
| 4 | GND | GND | |
| 5 | UIM_VPP | PWR | |
| 6 | UIM_DATA | I/O | |

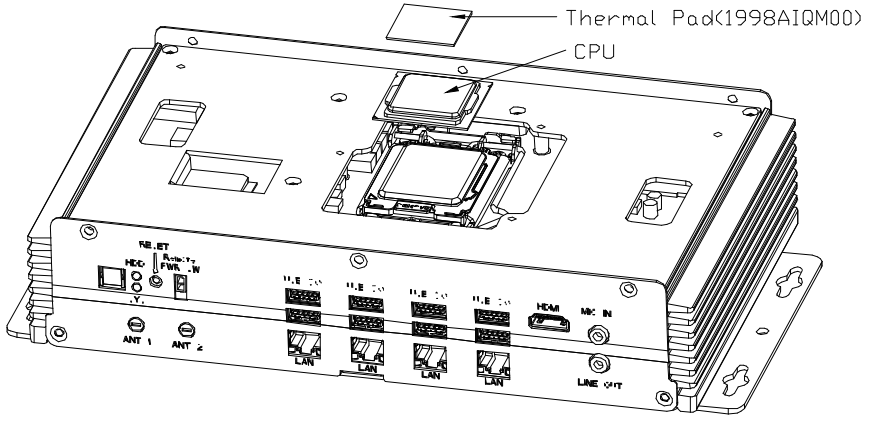
2.5 CPU Installation

Before installing the CPU, ensure the system is powered down and disconnect the power cord from the system. Make sure you have the processor ready to install. See Chapter 1 Specifications for list of compatible CPU/processors.

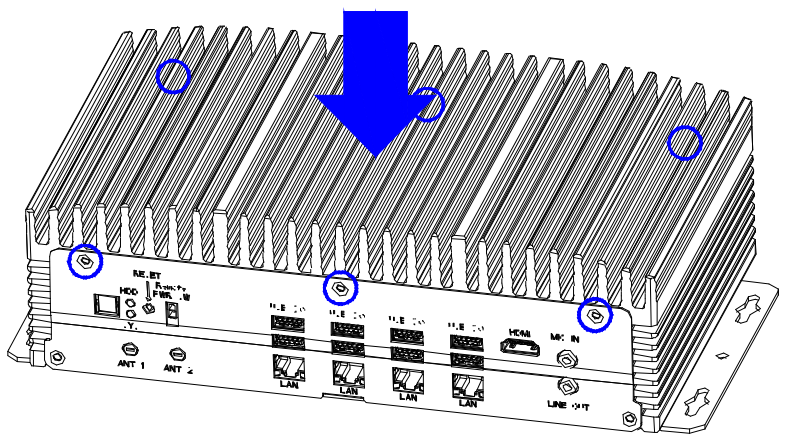
Step 1: Remove the screws on the front and back of the BOXER-6641 as shown in the figure below (six in total), and remove the top heatsink.



Step 2: Install the CPU into the socket and place the thermal pad on top of the processor.



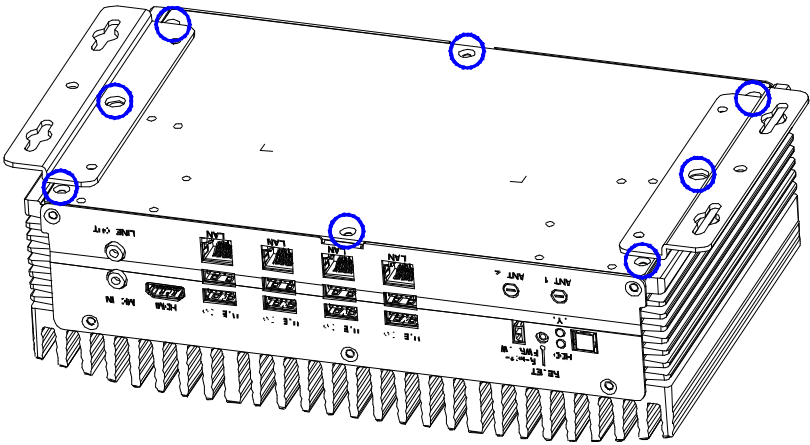
Step 3: Place the heatsink back on and secure with the screws you removed in Step 1.



2.6 Memory RAM Module Installation

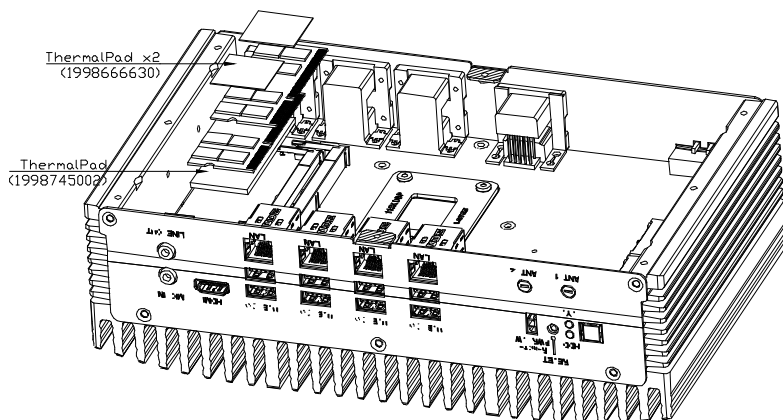
Before installing the RAM, ensure the system is powered down and disconnect the power cord from the system. Make sure you have the RAM module ready to install. See Chapter 1 for RAM requirements and specifications.

Step 1: Remove the eight (8) screws from the bottom of the BOXER-6641 as shown in the figure below. Remove the bottom panel from the system.



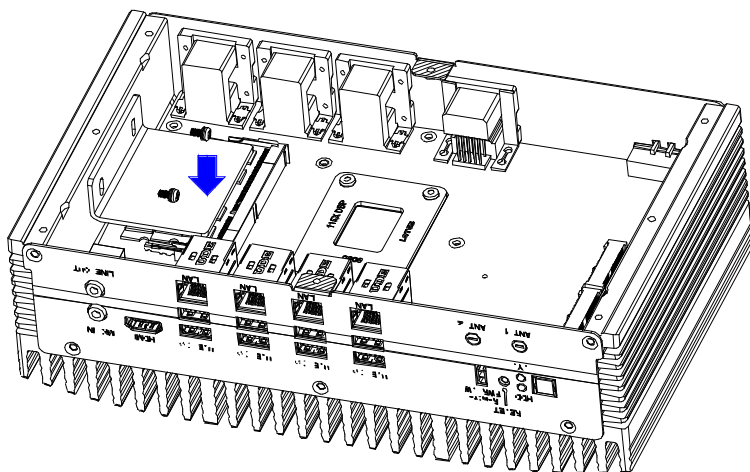
Step 2: Place thermal pads on the RAM modules and insert them into the RAM slots.

Note the figure below for placement of thermal pads. When inserting the modules into the RAM slots, first insert at an angle ($\sim 30^\circ$), then gently push down until secure.



Step 3: Install the RAM bracket. Ensure it is oriented as shown in the figure below.

Attach the bracket to the chassis using two screws.

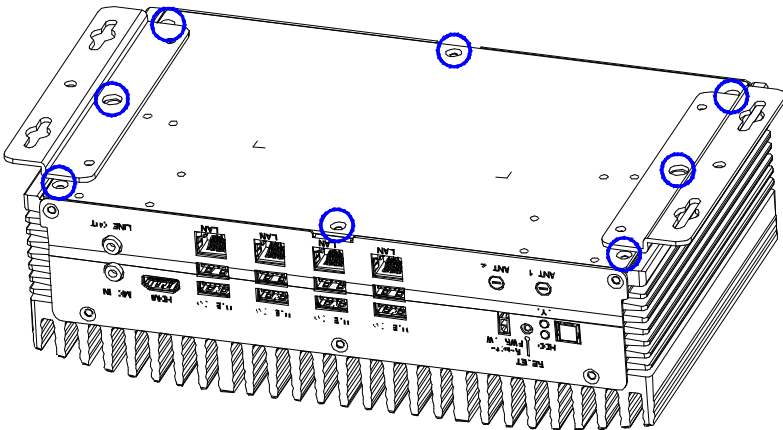


RAM installation is complete. If you also need to install the 2.5" SATA Drive, continue to the next section. If you are done, replace the bottom panel and secure with the eight (8) screws you removed in Step 1 of this section.

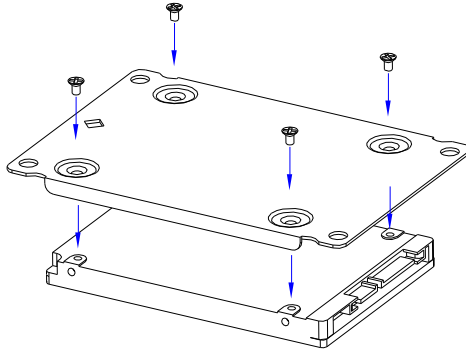
2.7 2.5" SATA Drive Installation

Before installing the SATA Drive, ensure the system is powered down and disconnect the power cord from the system. Make sure you have the SATA Drive ready to install. See Chapter 1 for SATA drive specifications for compatibility.

Step 1: If you have not already done so, remove the eight (8) screws from the bottom of the BOXER-6641 as shown in the figure below. Remove the bottom panel from the system.

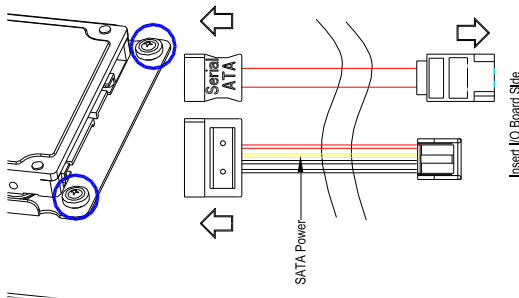
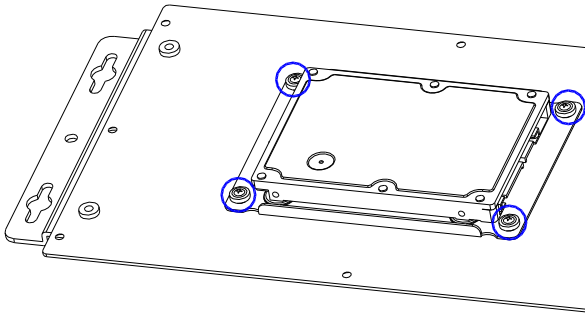


Step 2: Attach the SATA drive to the HDD Bracket using the screws provided.

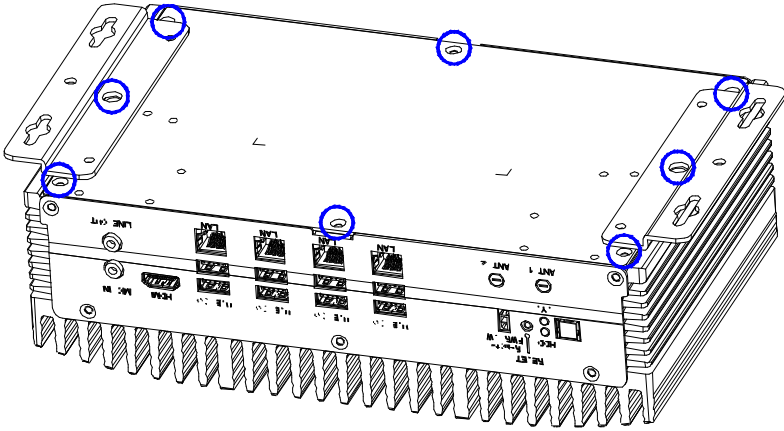


Step 3: Attach the HDD Bracket to the bottom panel using four screws as shown in the figure below. Attach the SATA and SATA Power cables to the board and the SATA drive.

Step 1: Use the HDD screws provided to assemble 2.5" SATA drive with the HDD Bracket



Step 4: Replace the bottom panel and secure with the eight (8) screws you removed in Step 1.

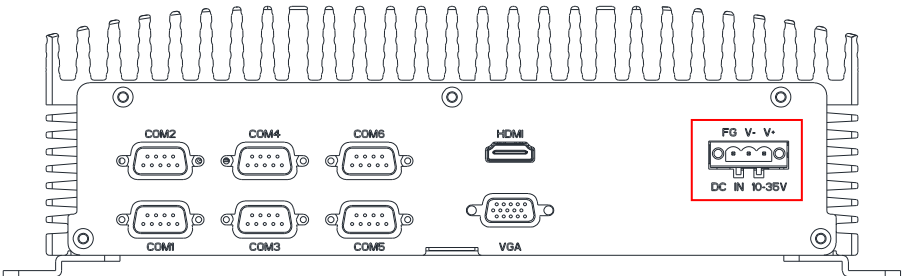


2.8 Power Connector Installation

Step 1: Take out the 3-pin green phoenix power connector from the accessory kit.



Step 2: Connect to the power input port shown in the diagram:



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

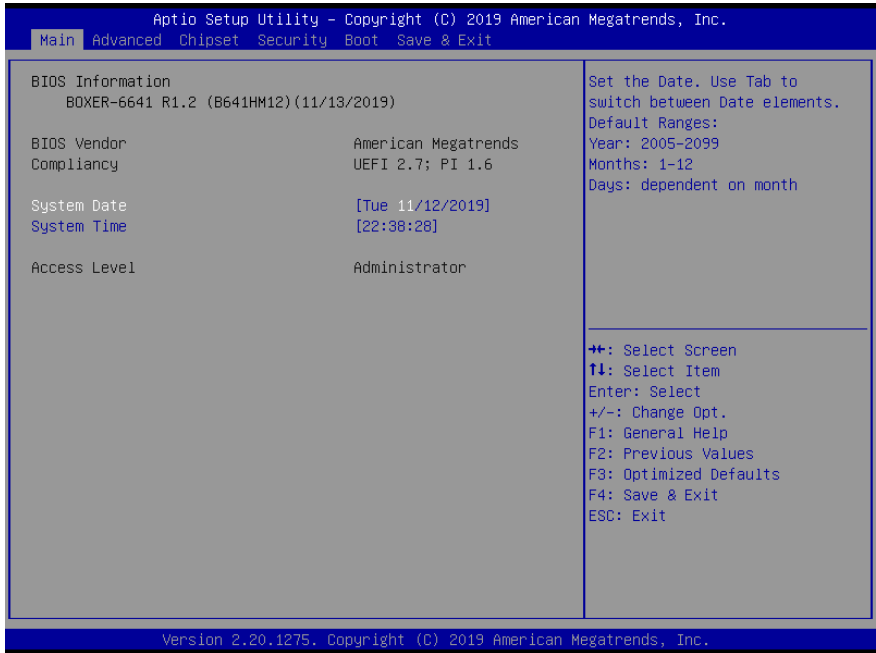
Chipset – For hosting bridge parameters

Security – The setup administrator password can be set here

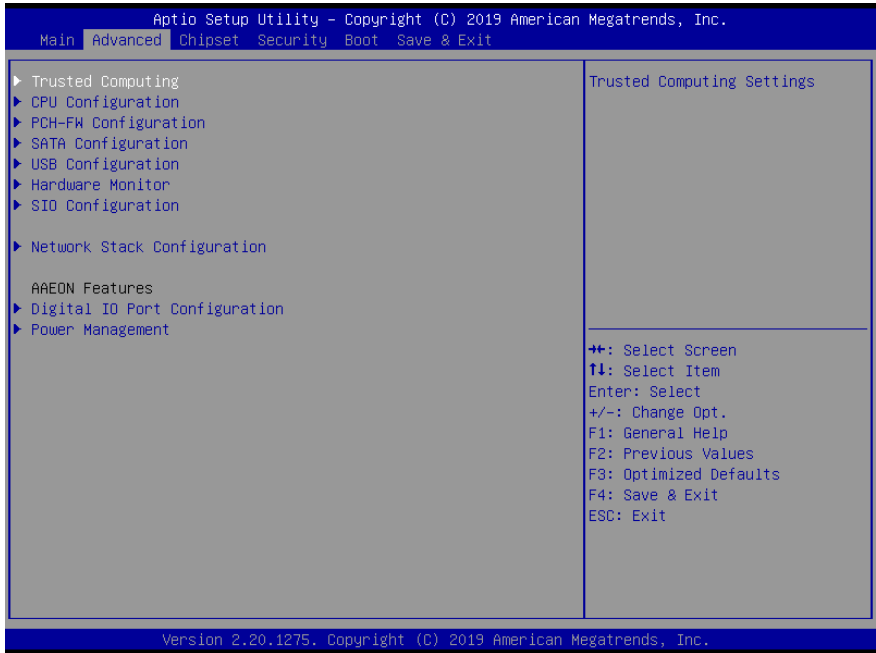
Boot – Enable/ Disable Quiet Boot option

Save & Exit – Save your changes and exit the program

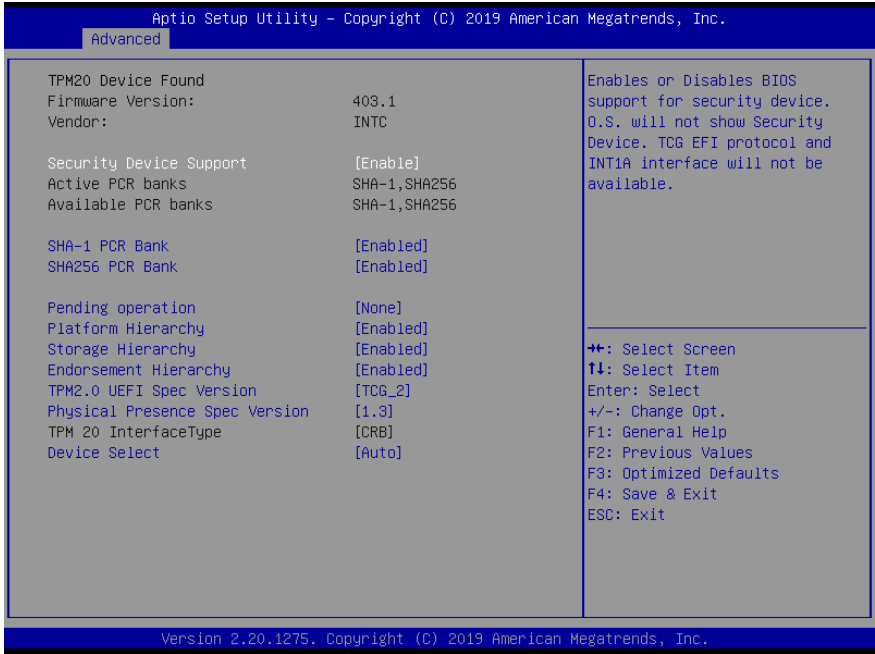
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



3.4.1 Advanced: Trusted Computing



| Options Summary | | |
|--|-----------|-----------------------------------|
| Security Device Support | Enable | Optimal Default, Failsafe Default |
| | Disable | |
| Enable or Disable BIOS support for security device. TCG EFI protocol and INT1A interface will not be available. | | |
| SHA-1 PCR Bank | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable SHA-1 PCR Bank | | |
| SHA256 PCR Bank | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable SHA256 PCR Bank | | |
| Pending operation | None | Optimal Default, Failsafe Default |
| | TPM Clear | |
| Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device. | | |

| Options Summary | | |
|---|----------|-----------------------------------|
| Platform Hierarchy | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable Platform Hierarchy | | |
| Storage Hierarchy | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable Storage Hierarchy | | |
| Endorsement Hierarchy | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable Endorsement Hierarchy | | |
| TPM2.0 UEFI Spec Version | TCG_2 | Optimal Default, Failsafe Default |
| | TCG_1_2 | |
| Select the TCG2 Spec Version Support TCG_1_2: Compatible mode for Win8/Win10 TCG_2: Support new TCG2 protocol and event format for Win10 or later | | |
| Physical Presence Spec Version | 1.3 | Optimal Default, Failsafe Default |
| | 1.2 | |
| Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3. | | |
| Device Select | Auto | Optimal Default, Failsafe Default |
| | TPM 1.2 | |
| | TPM 2.0 | |
| TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated | | |

3.4.2 Advanced: CPU Configuration

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Advanced

| | | |
|--|---|--|
| CPU Configuration | | Enabled or Disabled Hyper-Threading Technology. |
| Name | CoffeeLake DT | |
| Type | Intel(R) Xeon(R) E-2176G CPU @ 3.70GHz | |
| Speed | 3700 MHz | |
| ID | 0x906EA | |
| Stepping | U0 | |
| Package | LGA1151 | |
| Number of Processors | 6Core(s) / 12Thread(s) | |
| Microcode Revision | C6 | |
| GT Info | GT2 (0x3E96) | |
| eDRAM Size | N/A | |
| VMX | Supported | |
| SMX/TXT | Supported | |
| Intel (VMX) Virtualization Technology | [Enabled] | |
| Active Processor Cores | [All] | |
| Intel(R) SpeedStep(tm) | [Enabled] | |
| Intel(R) Speed Shift Technology | [Disabled] | |
| Turbo Mode | [Enabled] | |
| C states | [Disabled] | |
| Hyper-Threading | [Enabled] | |

++: Select Screen
 ↑↓: Select Item
 Enter: Select
 +/-: Change Opt.
 F1: General Help
 F2: Previous Values
 F3: Optimized Defaults
 F4: Save & Exit
 ESC: Exit

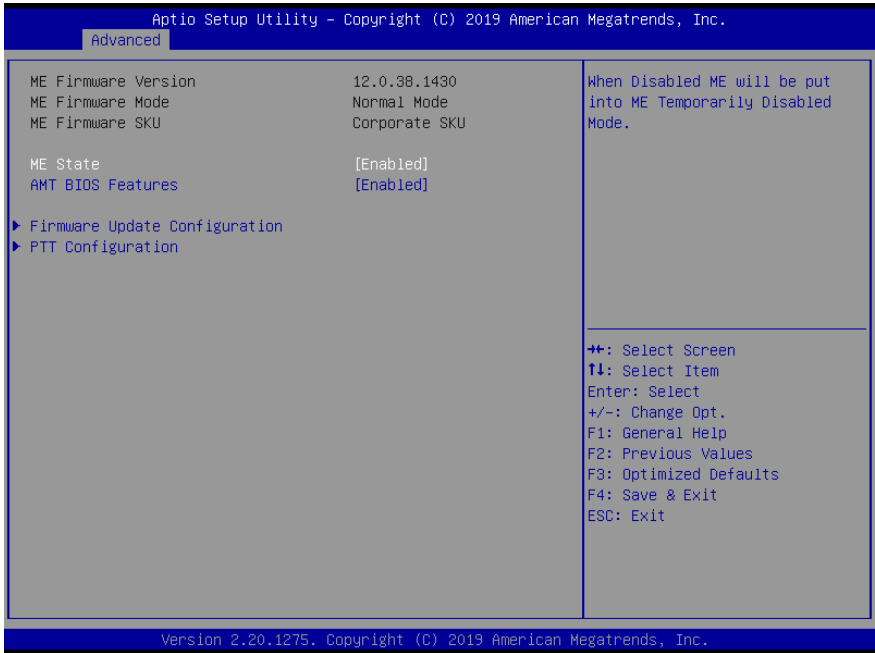
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| Options Summary | | |
|---|----------|-----------------------------------|
| Intel (VMX) Virtualization Technology | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology. | | |
| Active Processor Cores | 1 | Optimal Default, Failsafe Default |
| | 2 | |
| | 3 | |
| | All | |
| Number of cores to enable in each processor package. | | |
| Intel(R) SpeedStep(tm) | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Allows more than two frequency ranges to be supported. | | |

Table Continues on Next Page...

| Options Summary | | |
|---|----------|-----------------------------------|
| Intel(R) Speed Shift Technology | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable Intel(R) Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states. | | |
| Turbo Mode | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable Processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available or enabled). | | |
| C states | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable CPU Power Management. Allows CPU to go C states when it's not 100% utilized | | |
| Hyper-Threading | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enabled or Disabled Hyper-Threading Technology. | | |

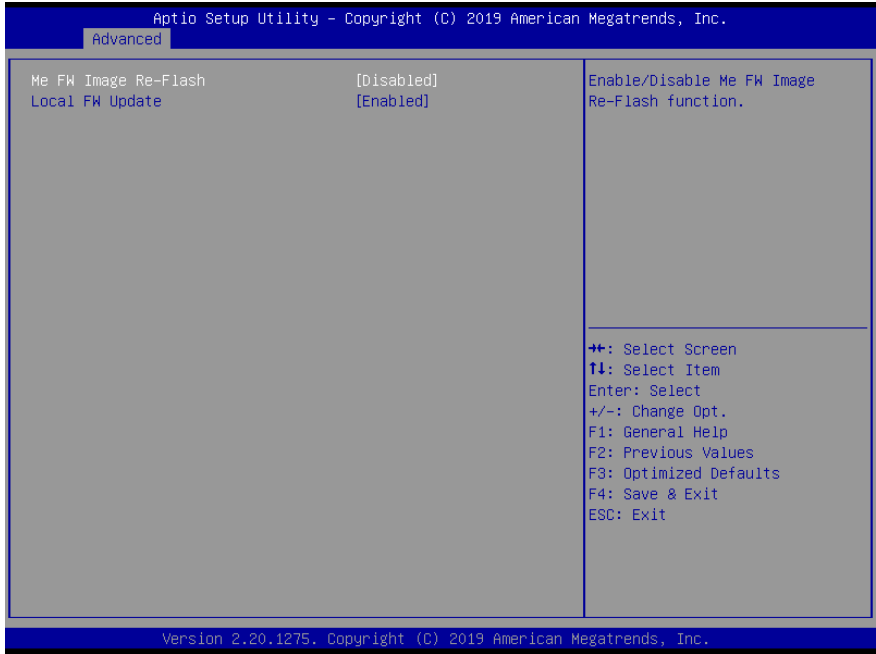
3.4.3 Advanced: PCH-FW Configuration



Options Summary

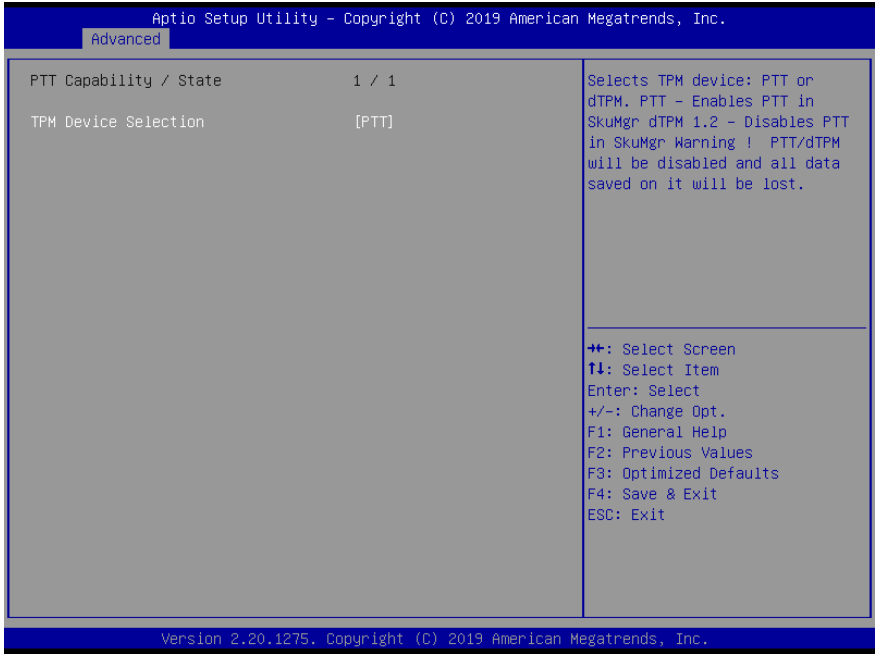
| | | |
|--|----------|-----------------------------------|
| ME State | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| When Disabled ME will be put into ME Temporarily Disabled Mode. | | |
| AMT BIOS Feature | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. | | |
| Note: This option does not disable Manageability Features in FW. | | |

3.4.3.1 Firmware Update Configuration



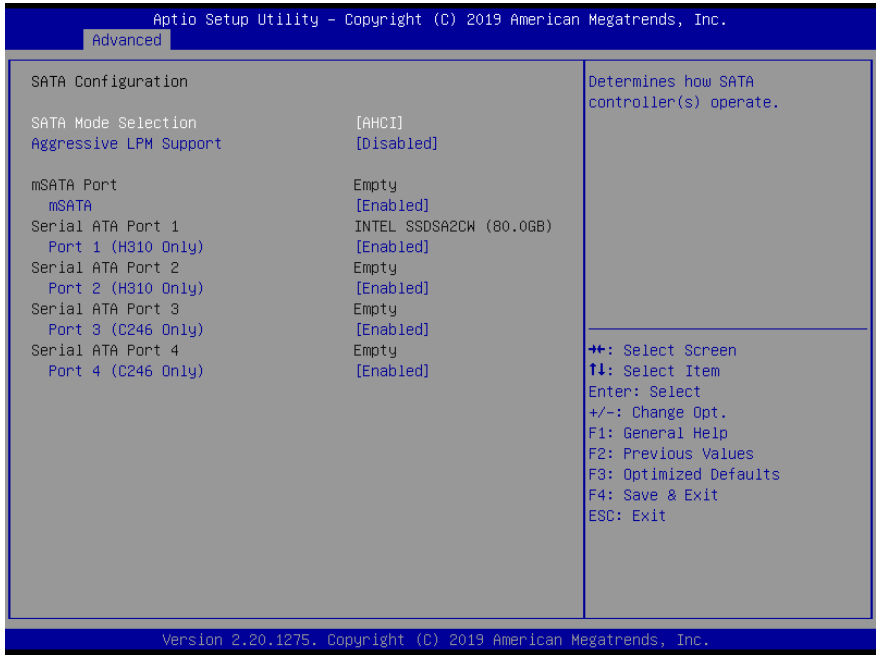
| Options Summary | | |
|---|----------|-----------------------------------|
| ME FW Image Re-Flash | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable/Disable ME FW Image Re-Flash function. | | |
| Local FW Update | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Options for Local FW Update function. | | |

3.4.3.2 PTT Configuration



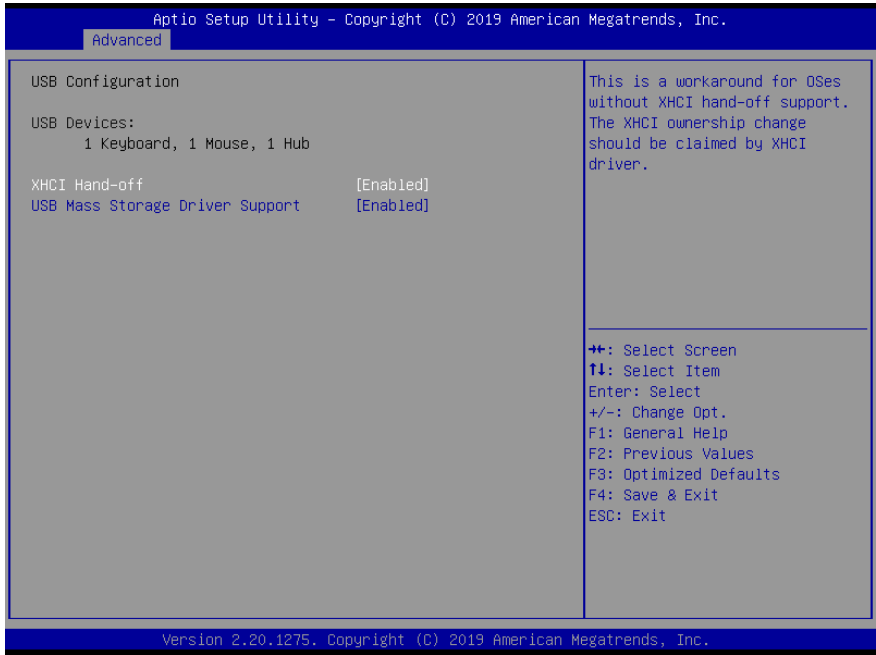
| Options Summary | | |
|--|------|-----------------------------------|
| ME FW Image Re-Flash | dTPM | |
| | PTT | Optimal Default, Failsafe Default |
| <p>Selects TPM device: PTT or dTPM. PTT – Enables PTT in SkuMgr dTPM 1.2 – Disables PTT in SkuMgr Warning! PTT/dTPM will be disabled and all saved data will be lost.</p> | | |

3.4.4 Advanced: SATA Configuration



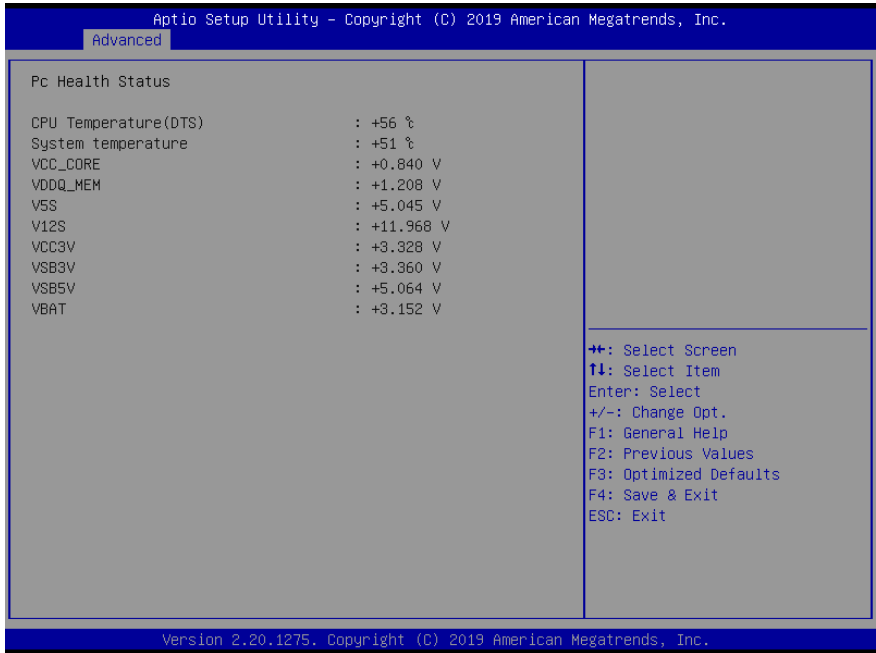
| Options Summary | | |
|--|---|-----------------------------------|
| SATA Mode Selection | AHCI Mode | Optimal Default, Failsafe Default |
| | Intel RST Premium With Intel Optane System Acceleration | |
| Determines how SATA controller(s) operate. | | |
| Aggressive LPM Support | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable PCH to aggressively enter link power state. | | |
| mSATA | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable SATA Port. | | |
| Port 1/2/3/4 | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable or Disable SATA Port. | | |

3.4.5 Advanced: USB Configuration

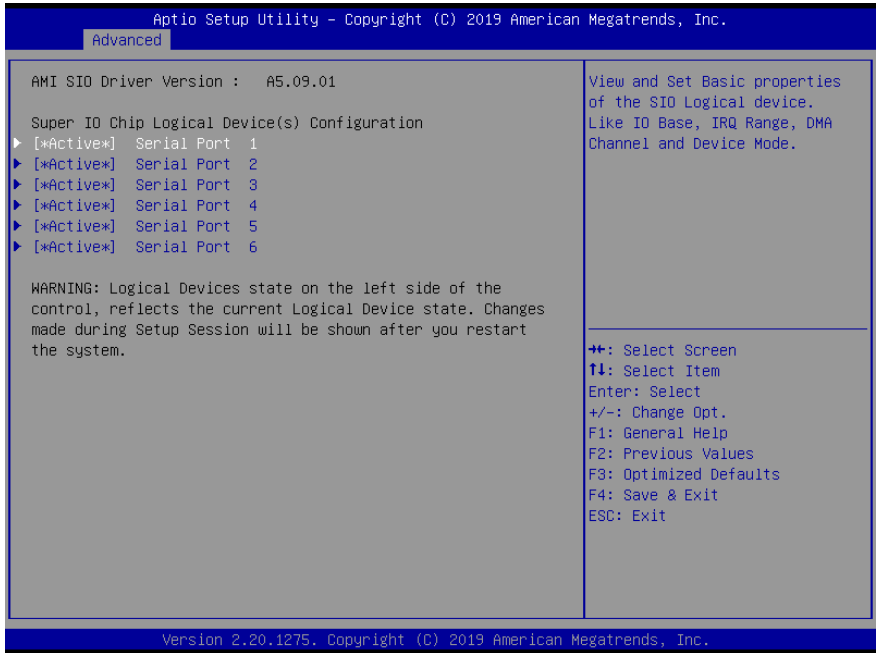


| Options Summary | | |
|--|----------|-----------------------------------|
| XHCI Hand-off | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| This is a workaround for OSes without XHCI Hand-off support. The XHCI ownership change should be claimed by XHCI driver. | | |
| USB Mass Storage Driver Support | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable/Disable USB Mass Storage Driver Support. | | |

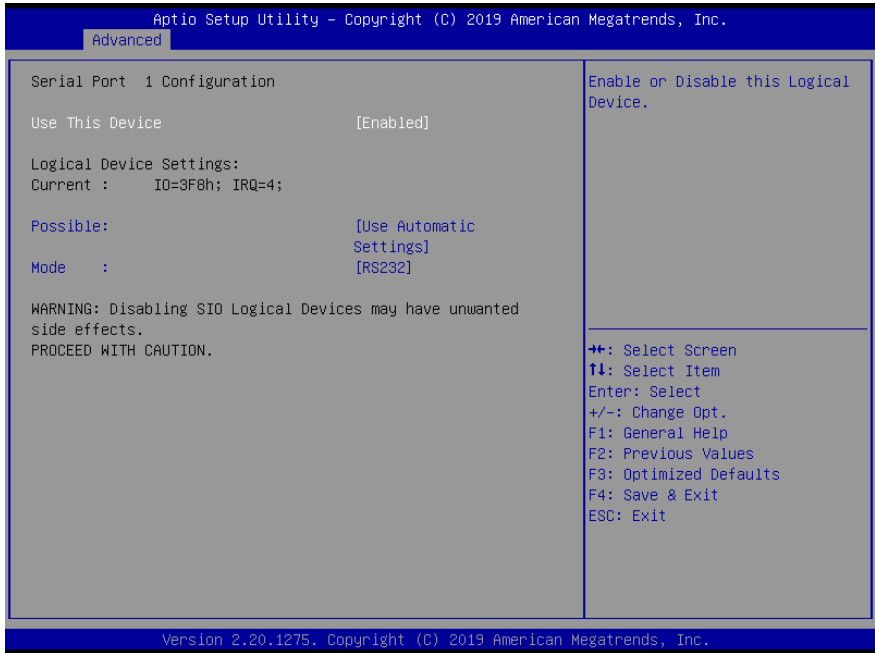
3.4.6 Advanced: Hardware Monitor



3.4.7 Advanced: SIO Configuration

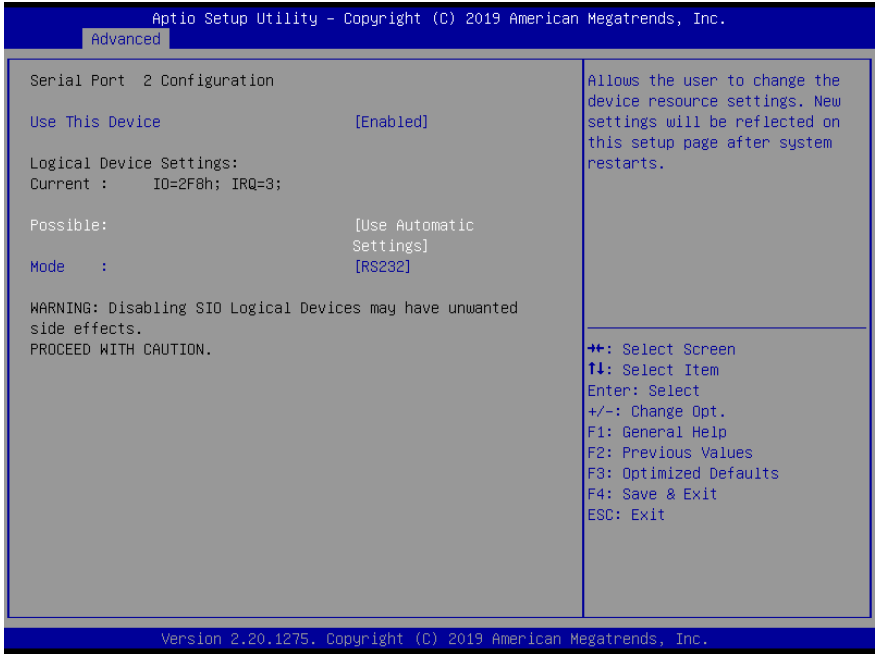


3.4.7.1 Serial Port 1 Configuration



| Options Summary | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=3F8h; IRQ = 4; | |
| | IO=2F8h; IRQ = 3; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

3.4.7.2 Serial Port 2 Configuration



| Options Summary | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=2F8h; IRQ = 3; | |
| | IO=3F8h; IRQ = 4; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

3.4.7.3 Serial Port 3 Configuration

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Advanced

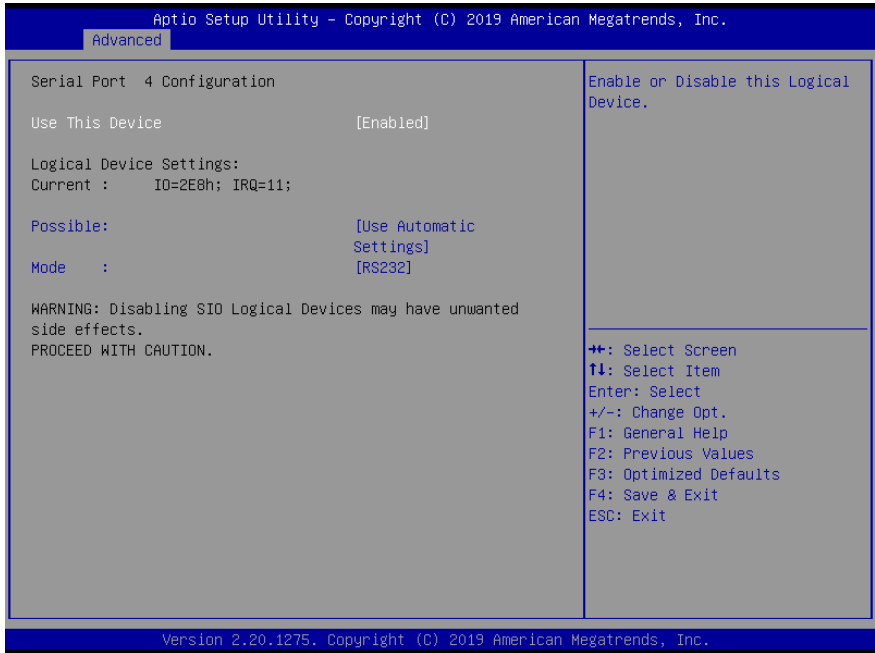
| | |
|--|---|
| <p>Serial Port 3 Configuration</p> <p>Use This Device [Enabled]</p> <p>Logical Device Settings: Current : IO=3E8h; IRQ=11;</p> <p>Possible: [Use Automatic Settings]</p> <p>Mode : [RS232]</p> <p>WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.</p> | <p>Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.</p> <p> ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit </p> |
|--|---|

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Options Summary

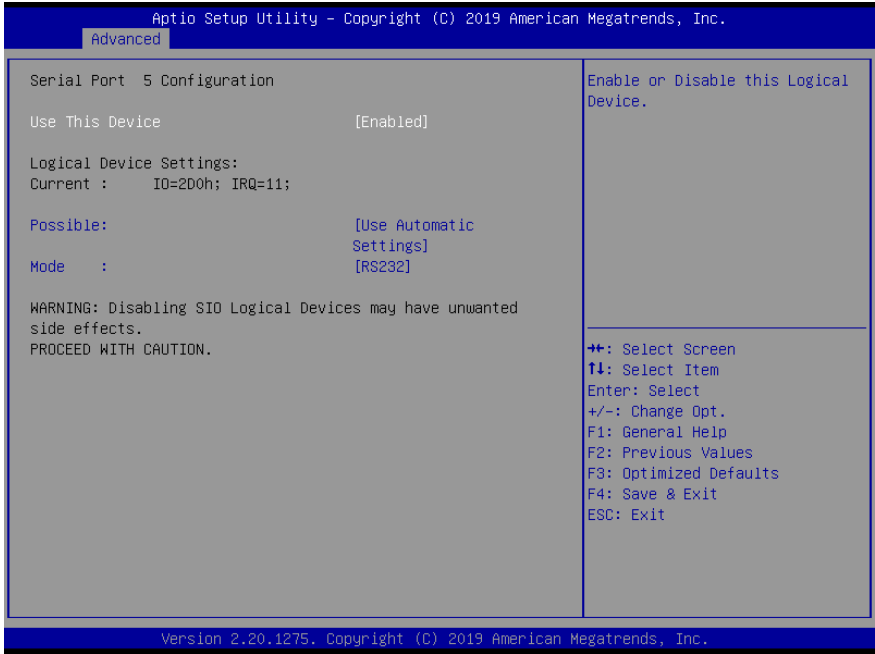
| | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=3E8h; IRQ = 11; | |
| | IO=2E8h; IRQ = 11; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

3.4.7.4 Serial Port 4 Configuration



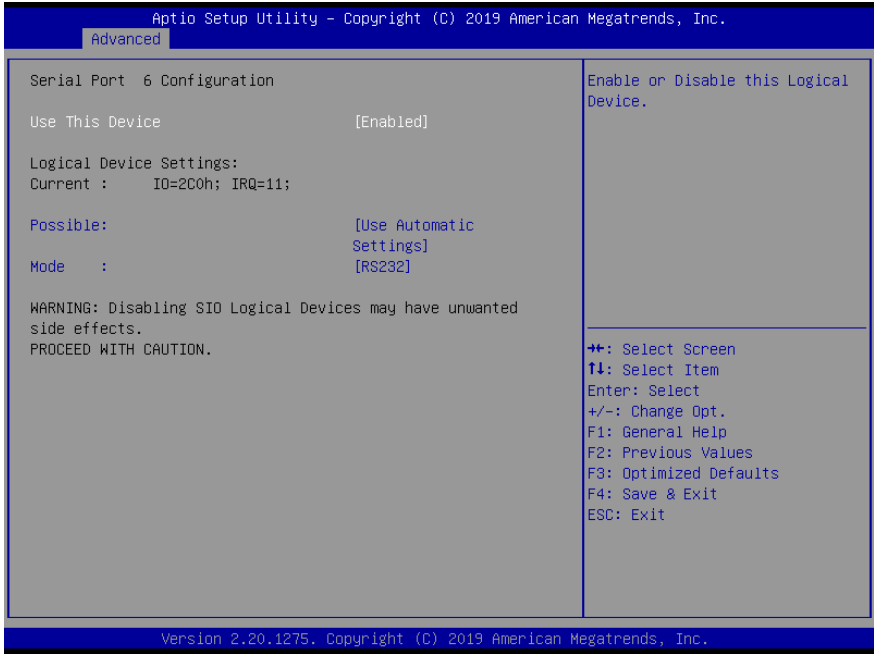
| Options Summary | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=2E8h; IRQ = 11; | |
| | IO=3E8h; IRQ = 11; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

3.4.7.5 Serial Port 5 Configuration



| Options Summary | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=2D0h; IRQ = 11; | |
| | IO=2C0h; IRQ = 11; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

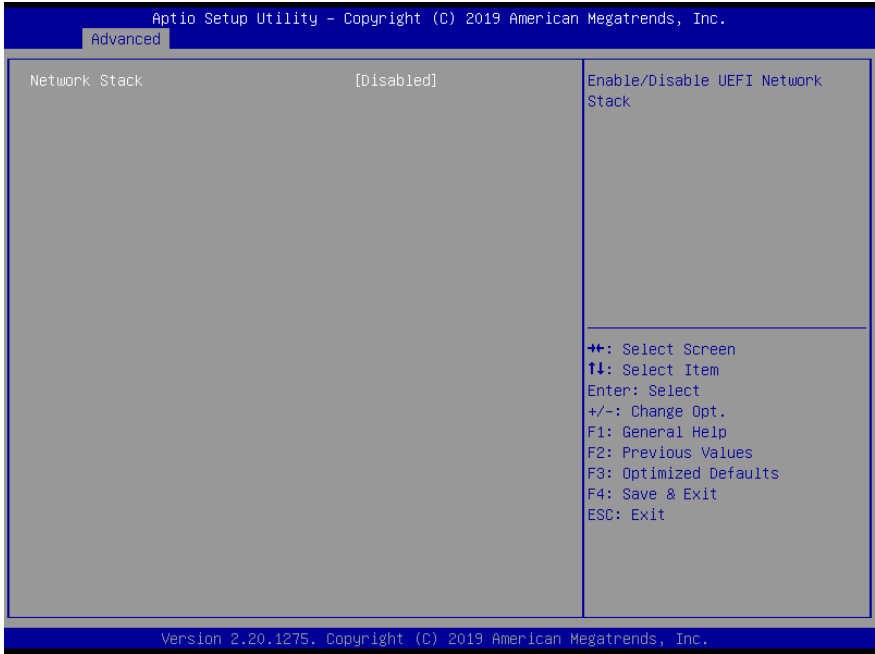
3.4.7.6 Serial Port 6 Configuration



| Options Summary | | |
|--|-----------------------|-----------------------------------|
| Use This Device | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enabled or Disabled this Logical Device. | | |
| Device resource settings | USB Automatic Setting | Optimal Default, Failsafe Default |
| | IO=2C0h; IRQ = 11; | |
| | IO=2D0h; IRQ = 11; | |
| Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts. | | |
| UART selection | RS232 | Optimal Default, Failsafe Default |
| | RS422 | |
| | RS485 | |
| UART RS232, 422, 485 selection. | | |

3.4.8 Advanced: Network Stack Configuration

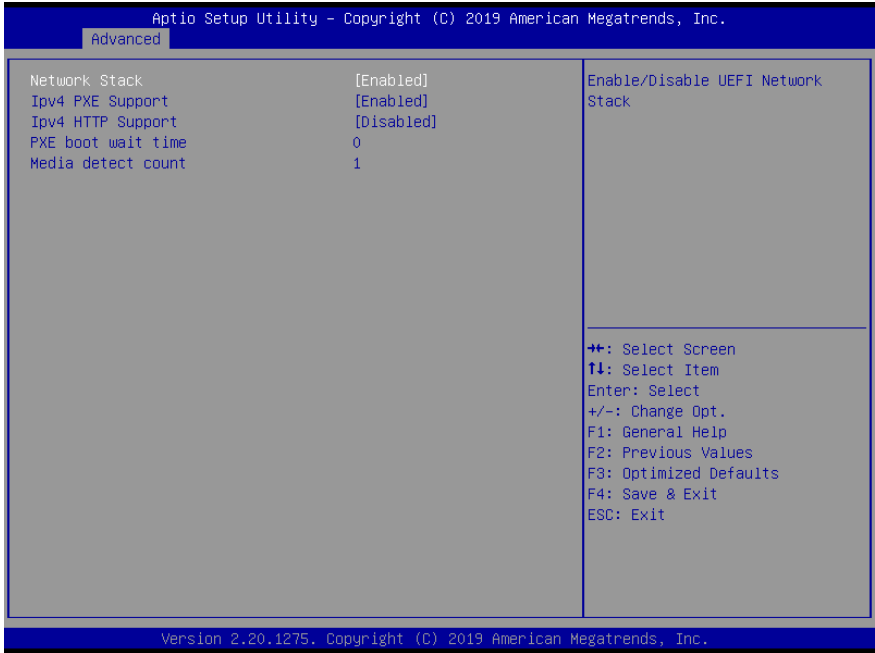
Network Stack Disabled:



Options Summary

| | | |
|-----------------------------------|----------|-----------------------------------|
| Network Stack | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable UEFI Network Stack | | |

Network Stack Enabled:



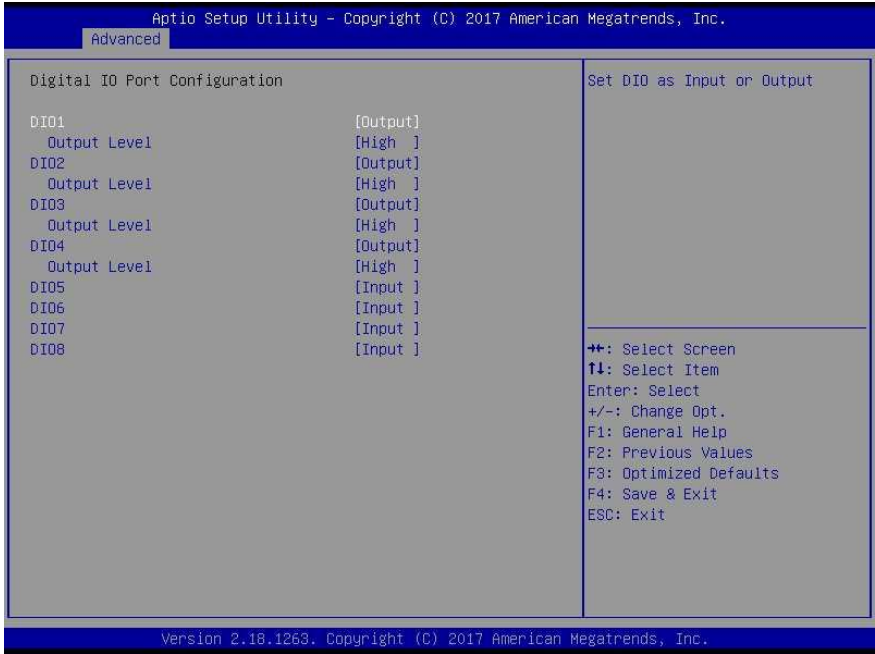
| Options Summary | | |
|---|----------|-----------------------------------|
| Network Stack | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable UEFI Network Stack | | |
| Ipv4 PXE Support | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available. | | |
| Ipv4 HTTP Support | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available. | | |
| PXE boot wait time | 0 | Optimal Default, Failsafe Default |
| Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value. | | |

Table Continues on Next Page...

Options Summary

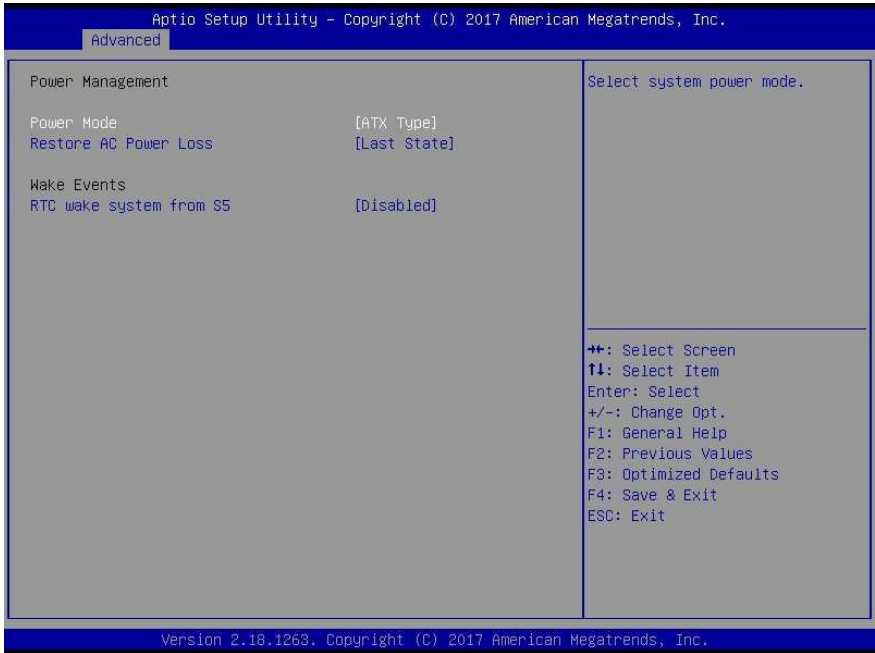
| | | |
|---|---|-----------------------------------|
| Media detect count | 1 | Optimal Default, Failsafe Default |
| Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value. | | |

3.4.9 Advanced: Digital IO Port Configuration



| Options Summary | | |
|--|--------|-----------------------------------|
| DIO Type | Output | Optimal Default, Failsafe Default |
| | Input | |
| Set DIO as Input or Output | | |
| DIO Data | Low | Optimal Default, Failsafe Default |
| | High | |
| Set is output level when DIO pin is output | | |

3.4.10 Advanced: Power Management

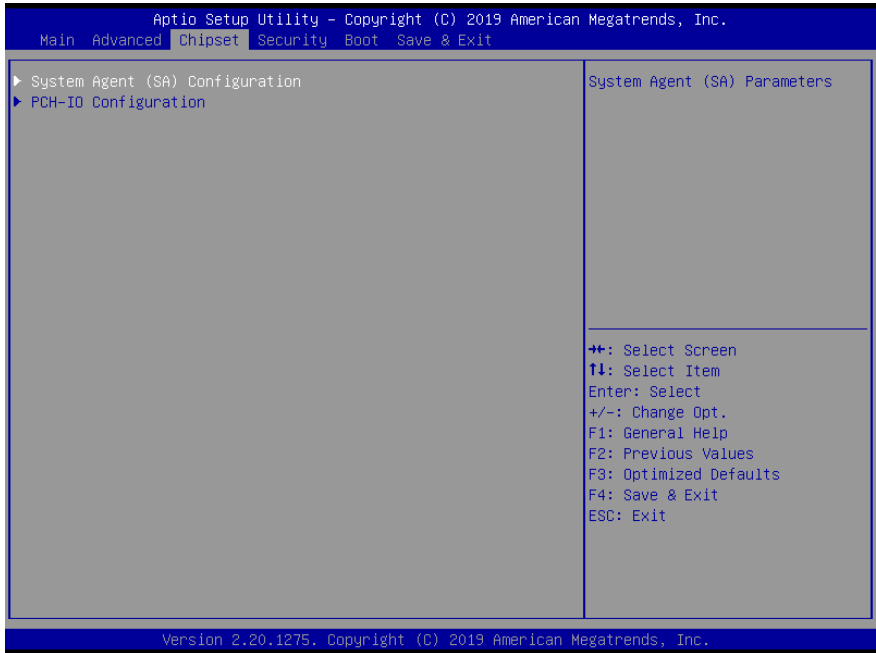


| Options Summary | | |
|---|------------|-----------------------------------|
| Power Mode | ATX Type | Optimal Default, Failsafe Default |
| | AT Type | |
| Select power supply mode. | | |
| AC Power Loss | Last State | Optimal Default, Failsafe Default |
| | Power On | |
| | Power Off | |
| Select power state when power is re-applied after a power failure. | | |
| RTC wake system from S5 | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Fixed Time: System will make on the hr::min::sec specified. | | |
| Dynamic Time: System will wake on the current time + Increase minute(S) | | |

Table Continues on Next Page...

| Options Summary | |
|--|---------|
| RTC wake system from S5 | Enabled |
| Wake up day | 0 |
| Select 0 for daily system wake up, 1-31 for which day of the month that you would like system to wake up | |
| Wake up hour | 0 |
| Select 0-23; For example enter 3 for 3am and 15 for 3pm | |
| Wake up minute | 0 |
| 0 – 59 | |
| Wake up second | 0 |
| 0 - 59 | |

3.5 Setup submenu: Chipset



3.5.1 Chipset: System Agent (SA) Configuration

Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

Chipset

| | | |
|------------------------------------|--------------------------|--|
| System Agent (SA) Configuration | | System Agent Geyserville. Fixed Low/Mid/High: SA GV disabled, MRC only runs tasks from Low, Mid, or High point. SA GV will be disabled on DT/Halo CPUs, regardless of this setting. |
| Total Memory | 16384 MB | |
| Memory Frequency | 2133 MHz | |
| Memory Timings (tCL-tRCD-tRP-tRAS) | 15-15-15-36 | |
| Channel 0 Slot 0 | Populated & Enabled | |
| Size | 16384 MB (DDR4) | |
| Number of Ranks | 2 | |
| Channel 1 Slot 0 | Not Populated / Disabled | |
| VT-d | Supported | |
| SA GV | [Enabled] | ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit |
| PM Support | [Enabled] | |
| RC6(Render Standby) | [Enabled] | |
| DVMT Total Gfx Mem | [MAX] | |
| VT-d | [Disabled] | |
| Skip Scanning of External Gfx Card | [Disabled] | |

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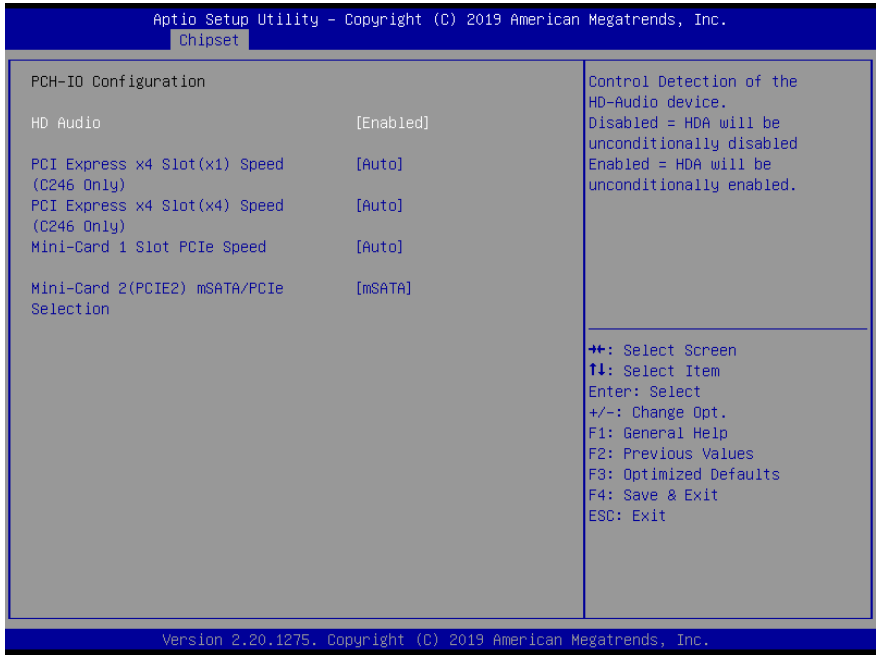
Options Summary

| | | |
|---|------------|-----------------------------------|
| SA GV | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| | Fixed Low | |
| | Fixed High | |
| System Agent Geyserville. Fixed Low/Mid/High: SA GV disabled, MRC only runs tasks from Low, Mid, or High point. SA GV will be disabled on DT/Halo CPUs, regardless of this setting. | | |
| PM Support | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Enable/Disable PM Support. | | |
| RC6(Render Standby) | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Check to enable render standby support. | | |

Table Continues on Next Page...

| Options Summary | | |
|---|----------|-----------------------------------|
| DVMT Total Gfx Mem | 128M | Optimal Default, Failsafe Default |
| | 256M | |
| | MAX | |
| Select DVMT5.0 Total Graphic Memory sized used by the Internal Graphics Device. | | |
| VT-d | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| VT-d capability. | | |
| Skip Scanning of External Gfx Card | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| If Enabled, it will not scan for External Gfx Card on PEG and PCH PCIE Ports | | |

3.5.2 Chipset: PCH-IO Configuration

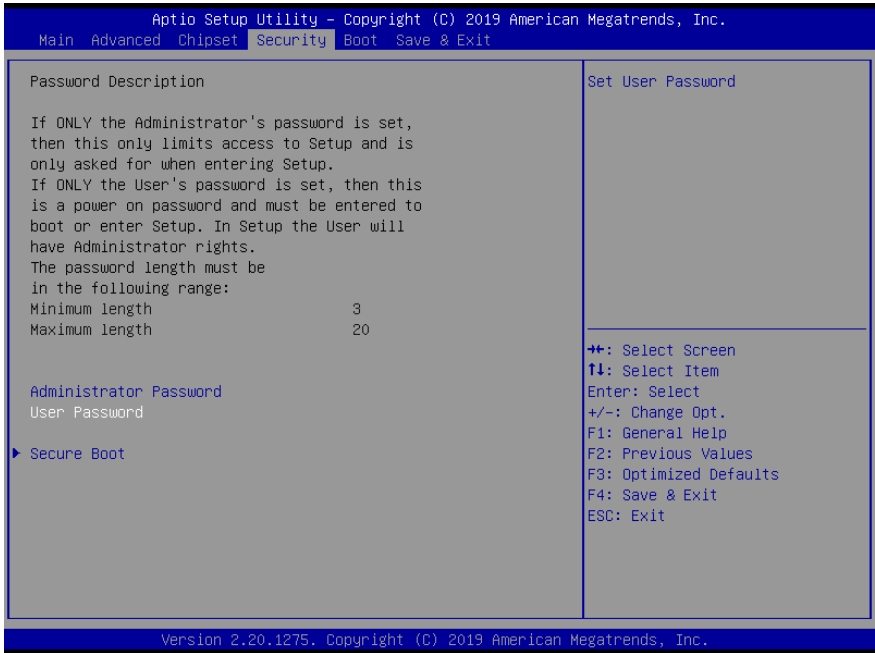


Options Summary

| | | |
|--|----------|-----------------------------------|
| HD Audio | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| Control the Detection of the Audio device. Disabled = HDA will be unconditionally disabled. Enabled = HDA will be unconditionally enabled. | | |
| PCI Express x4 Slot(x1) Speed (C246 Only) | Auto | Optimal Default, Failsafe Default |
| | Gen 1 | |
| | Gen 2 | |
| | Gen 3 | |
| Configure PCIe Speed. | | |
| PCI Express x4 Slot(x4) Speed (C246 Only) | Auto | Optimal Default, Failsafe Default |
| | Gen 1 | |
| | Gen 2 | |
| | Gen 3 | |
| Configure PCIe Speed. | | |

| Options Summary | | |
|---|-------|-----------------------------------|
| Mini-Card 1 Slot PCIe Speed | Auto | Optimal Default, Failsafe Default |
| | Gen 1 | |
| | Gen 2 | |
| Configure PCIe Speed. | | |
| Mini-Card 2(PCIE2) mSATA/PCIe Selection | mSATA | Optimal Default, Failsafe Default |
| | PCIe | |
| Select mSATA or PCIe function for Mini-Card 2(PCIE2). | | |

3.6 Setup submenu: Security



Change User/Administrator Password

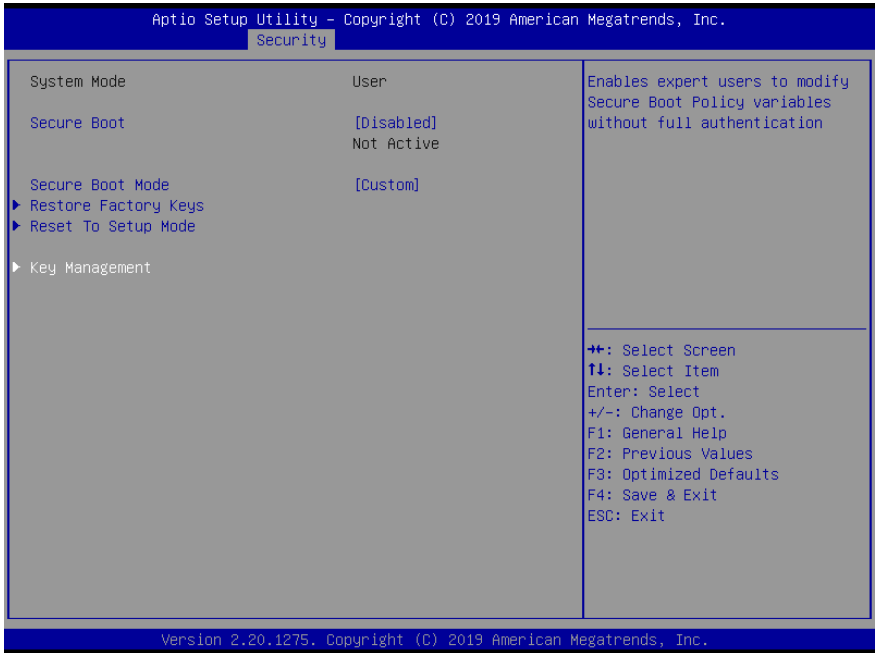
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

Removing the Password

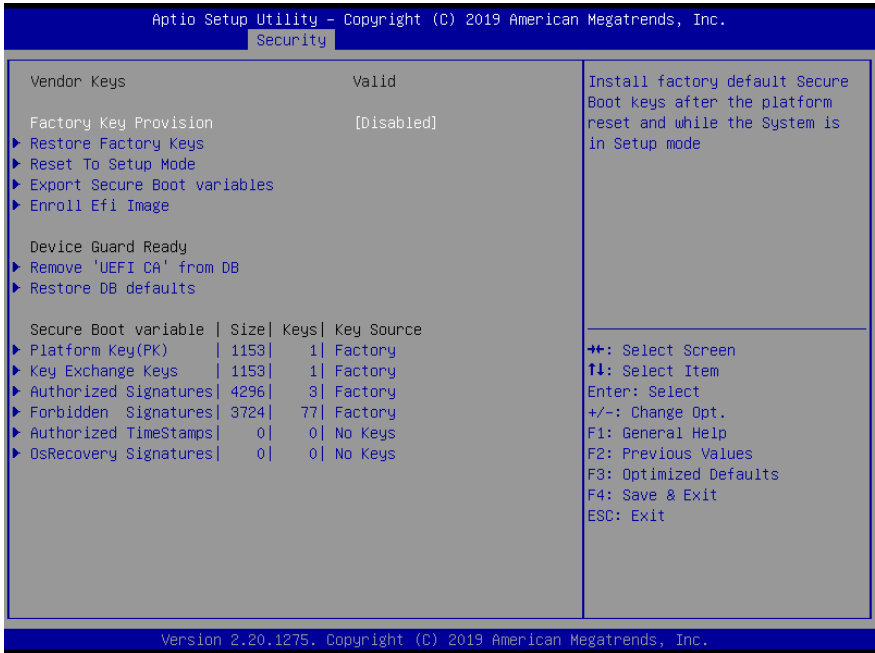
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

3.6.1 Security: Secure Boot



| Options Summary | | |
|---|----------|-----------------------------------|
| Secure Boot | Disable | Optimal Default, Failsafe Default |
| | Enable | |
| Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System mode is in User mode. The mode change requires platform reset. | | |
| Secure Boot Mode | Standard | Optimal Default, Failsafe Default |
| | Custom | |
| Secure Boot Mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication. | | |
| Restore Factory Keys | Yes | |
| | No | |
| Force System to User Mode. Install factory default Secure Boot key databases | | |
| Key Management | | |
| Enables expert users to modify Secure Boot Policy variables without full authentication | | |

3.6.1.1 Key Management



| Options Summary | | | | |
|--|--|----------|---------|---|
| Factory key Provision | <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>Disabled</td></tr> <tr><td>Enabled</td></tr> </table> | Disabled | Enabled | Optimal Default, Failsafe Default |
| Disabled | | | | |
| Enabled | | | | |
| Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode. | | | | |
| Restore Factory Keys | <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>No</td></tr> <tr><td>Yes</td></tr> </table> | No | Yes | Press 'Yes' to install factory default keys |
| No | | | | |
| Yes | | | | |
| Force System to User Mode. Install Factory default Secure Boot key databases. | | | | |
| Reset To Setup Mode | <table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>No</td></tr> <tr><td>Yes</td></tr> </table> | No | Yes | Deleting all variables will reset the System to Setup Mode. |
| No | | | | |
| Yes | | | | |
| Delete all Secure Boot key databases from NVRAM. | | | | |
| Export Secure Boot variables | | | | |
| Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device. | | | | |

| Options Summary | |
|--|--|
| Enroll Efi Image | |
| Allow the image to run in Secure Boot mode. Enroll SHA256 Hash Certificate of a PE Image into Authorized Signature Database (db). | |

| Device Guard Ready | | |
|---|-----|---|
| Remove 'UEFI CA' from SB | No | Press 'Yes' to remove 'UEFI CA' from SB |
| | Yes | |
| Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database(db). | | |
| Restore DB defaults | No | Press 'Yes' to Restore DB defaults |
| | Yes | |
| Restore DB variable to factory defaults. | | |

| Secure Boot variable Size Keys# key Source | | |
|--|---------|---|
| Platform key(PK) 1153 1 No Key | Details | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Export | |
| | Update | |
| | Delete | |
| Key Exchange keys 1153 1 No Key | Details | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Export | |
| | Update | |
| | Append | |
| | Delete | |

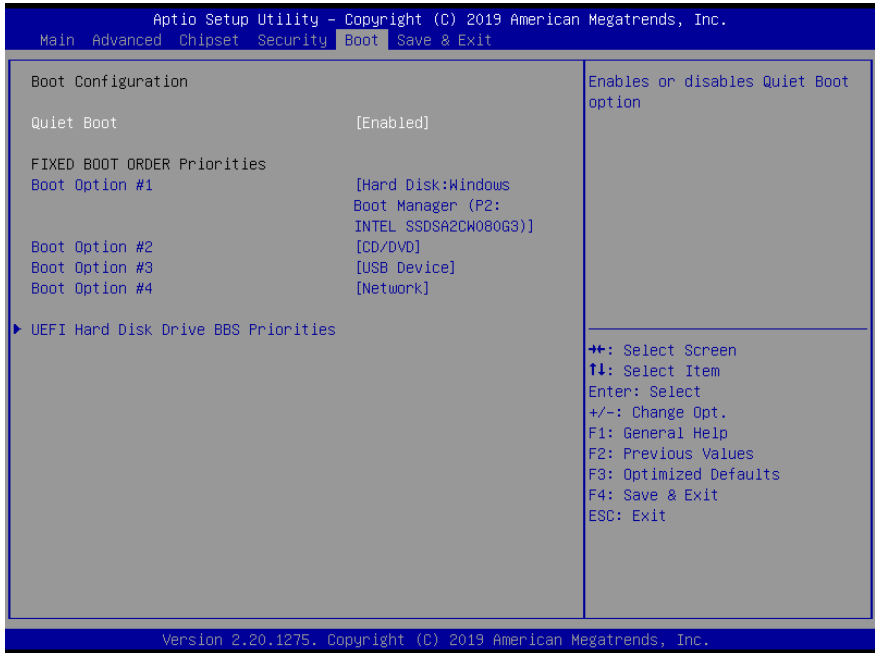
Table Continues on Next Page...

| Secure Boot variable Size Keys# key Source | | |
|--|---------|---|
| Authorized Signatures 4296 3 No Key | Details | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Export | |
| | Update | |
| | Append | |
| | Delete | |
| Forbidden Signatures 3274 77 No Key | Details | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Export | |
| | Update | |
| | Append | |
| | Delete | |
| Authorized TimeStamps 0 0 No Key | Update | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Append | |

Table Continues on Next Page

| Secure Boot variable | Size | Keys# | key Source |
|---------------------------------------|--------|-------|---|
| OsRecovery Signatures 0 0 No Key | Update | | Enroll Factory Defaults or load certificates from a file: 1.Public key Certificate: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHAXXX 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory, External, Mixed |
| | Append | | |

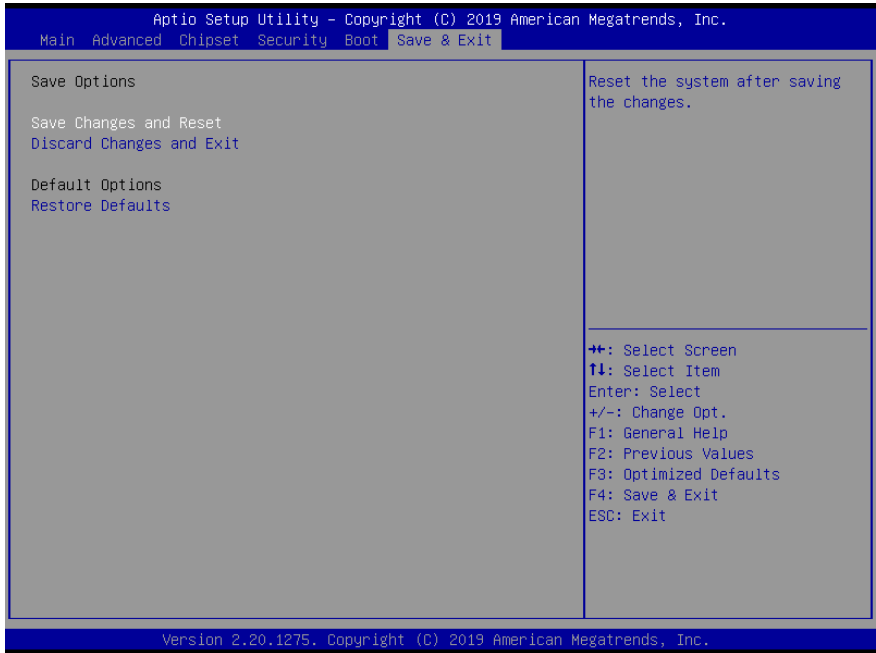
3.7 Setup submenu: Boot



Options Summary

| | | |
|--|----------|-----------------------------------|
| Quiet Boot | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| Enables or disables Quiet Boot option. | | |

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Drivers Download and Installation

Drivers for the BOXER-6641 can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/p/fanless-embedded-box-pc-socket-type-boxer-6641>

Download the driver(s) you need and follow the steps below to install them.

Step 1 – Install Chipset Driver

1. Open the **Step1 - Chipset** folder and select your OS
2. Run the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step2 - Graphic** folder and select your OS
2. Run the **igxpin.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install ME Driver

1. Open the **Step3 - ME** folder and select your OS
2. Run the **SetupME.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – LAN

1. Open the **Step4 - LAN** folder and select your OS
2. Run the **PROWinx64_23.5.2.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 5 – Install Audio Driver

1. Open the **Step5 – Audio** folder and select your OS
2. Run the **0008-64bit_Win7_Win8_Win81_Win10_R281.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 6 – Install Intel RST Driver

1. Open the **Step6 – Intel RST** folder and select your OS
2. Run the **SetupRST.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 7 – Install Serial Port Driver (Optional)

1. Open the **Step7 – Serial Port Driver (Optional)** folder
2. Run the **FintekSerial.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

| Table 1 : SuperIO relative register table | | |
|---|---------------|--|
| | Default Value | Note |
| Index | 0x2E(Note1) | SIO MB PnP Mode Index Register 0x2E or 0x4E |
| Data | 0x2F(Note2) | SIO MB PnP Mode Data Register 0x2F or 0x4F |

| Table 2 : Watchdog relative register table | | | | | |
|--|--------------|--------------|-----------|-----------|--|
| | LDN | Register | BitNum | Value | Note |
| Timer Counter | 0x07(Note3) | 0xF6(Note4) | | (Note24) | Time of watchdog timer (0~255) This register is byte access |
| Counting Unit | 0x07(Note5) | 0xF5(Note6) | 3(Note7) | 0(Note8) | Select time unit. 0: second 1: minute |
| Watchdog Enable | 0x07(Note9) | 0xF5(Note10) | 5(Note11) | 1(Note12) | 0: Disable 1: Enable |
| Timeout Status | 0x07(Note13) | 0xF5(Note14) | 6(Note15) | 1 | 1: Clear timeout status |
| Output Mode | 0x07(Note16) | 0xF5(Note17) | 4(Note18) | 1(Note19) | Select WDRST# output mode 0: level 1: pulse |
| WDRST output | 0x07(Note20) | 0xFA(Note21) | 0(Note22) | 1(Note23) | Enable/Disable time out output via WDRST# 0: Disable 1: Enable |

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte TimerLDN //This parameter is represented from Note3
#define byte TimerReg //This parameter is represented from Note4
#define byte TimerVal // This parameter is represented from Note24
#define byte UnitLDN //This parameter is represented from Note5
#define byte UnitReg //This parameter is represented from Note6
#define byte UnitBit //This parameter is represented from Note7
#define byte UnitVal //This parameter is represented from Note8
#define byte EnableLDN //This parameter is represented from Note9
#define byte EnableReg //This parameter is represented from Note10
#define byte EnableBit //This parameter is represented from Note11
#define byte EnableVal //This parameter is represented from Note12
#define byte StatusLDN // This parameter is represented from Note13
#define byte StatusReg // This parameter is represented from Note14
#define byte StatusBit // This parameter is represented from Note15
#define byte ModeLDN // This parameter is represented from Note16
#define byte ModeReg // This parameter is represented from Note17
#define byte ModeBit // This parameter is represented from Note18
#define byte ModeVal // This parameter is represented from Note19
#define byte WDRstLDN // This parameter is represented from Note20
#define byte WDRstReg // This parameter is represented from Note21
#define byte WDRstBit // This parameter is represented from Note22
#define byte WDRstVal // This parameter is represented from Note23
*****

```

```
*****
VOID Main() {
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

Appendix B














I/O Information

B.1 I/O Address Map

| | |
|---------------------------------------|-----------------------------------|
| Input/output (IO) | |
| [0000000000000000 - 000000000000CF7] | PCI Express Root Complex |
| [0000000000000020 - 0000000000000021] | Programmable interrupt controller |
| [0000000000000024 - 0000000000000025] | Programmable interrupt controller |
| [0000000000000028 - 0000000000000029] | Programmable interrupt controller |
| [000000000000002C - 000000000000002D] | Programmable interrupt controller |
| [000000000000002E - 000000000000002F] | Motherboard resources |
| [0000000000000030 - 0000000000000031] | Programmable interrupt controller |
| [0000000000000034 - 0000000000000035] | Programmable interrupt controller |
| [0000000000000038 - 0000000000000039] | Programmable interrupt controller |
| [000000000000003C - 000000000000003D] | Programmable interrupt controller |
| [0000000000000040 - 0000000000000043] | System timer |
| [000000000000004E - 000000000000004F] | Motherboard resources |
| [0000000000000050 - 0000000000000053] | System timer |
| [0000000000000061 - 0000000000000061] | Motherboard resources |
| [0000000000000063 - 0000000000000063] | Motherboard resources |
| [0000000000000065 - 0000000000000065] | Motherboard resources |
| [0000000000000067 - 0000000000000067] | Motherboard resources |
| [0000000000000070 - 0000000000000070] | Motherboard resources |
| [0000000000000070 - 0000000000000077] | System CMOS/real time clock |
| [0000000000000080 - 0000000000000080] | Motherboard resources |
| [0000000000000092 - 0000000000000092] | Motherboard resources |
| [00000000000000A0 - 00000000000000A1] | Programmable interrupt controller |
| [00000000000000A4 - 00000000000000A5] | Programmable interrupt controller |
| [00000000000000A8 - 00000000000000A9] | Programmable interrupt controller |
| [00000000000000AC - 00000000000000AD] | Programmable interrupt controller |
| [00000000000000B0 - 00000000000000B1] | Programmable interrupt controller |
| [00000000000000B2 - 00000000000000B3] | Motherboard resources |
| [00000000000000B4 - 00000000000000B5] | Programmable interrupt controller |
| [00000000000000B8 - 00000000000000B9] | Programmable interrupt controller |
| [00000000000000BC - 00000000000000BD] | Programmable interrupt controller |
| [00000000000000F0 - 00000000000000F0] | Numeric data processor |
| [00000000000002E8 - 00000000000002EF] | Communications Port (COM4) |
| [00000000000002F8 - 00000000000002FF] | Communications Port (COM2) |
| [00000000000003B0 - 00000000000003BB] | Intel(R) HD Graphics 530 |
| [00000000000003C0 - 00000000000003DF] | Intel(R) HD Graphics 530 |
| [00000000000003E8 - 00000000000003EF] | Communications Port (COM3) |
| [00000000000003F8 - 00000000000003FF] | Communications Port (COM1) |
| [00000000000004D0 - 00000000000004D1] | Programmable interrupt controller |
| [0000000000000680 - 000000000000069F] | Motherboard resources |

| | |
|---------------------------------------|--|
| [0000000000000680 - 00000000000069F] | Motherboard resources |
| [000000000000800 - 00000000000087F] | Motherboard resources |
| [000000000000A00 - 000000000000A0F] | Motherboard resources |
| [000000000000A10 - 000000000000A1F] | Motherboard resources |
| [000000000000A20 - 000000000000A2F] | Motherboard resources |
| [000000000000D00 - 000000000000FFFF] | PCI Express Root Complex |
| [000000000000164E - 000000000000164F] | Motherboard resources |
| [0000000000001800 - 00000000000018FE] | Motherboard resources |
| [0000000000001854 - 0000000000001857] | Motherboard resources |
| [000000000000E000 - 000000000000EFFF] | Intel(R) 100 Series/C230 Series Chipset Family PCI Express Root Port #9 - A118 |
| [000000000000F000 - 000000000000F03F] | Intel(R) HD Graphics 530 |
| [000000000000F000 - 000000000000F03F] | Intel(R) HD Graphics 630 |
| [000000000000F000 - 000000000000F03F] | Intel(R) HD Graphics 630 |
| [000000000000F040 - 000000000000F05F] | Intel(R) 100 Series/C230 Series Chipset Family SMBus - A123 |
| [000000000000F060 - 000000000000F07F] | Standard SATA AHCI Controller |
| [000000000000F080 - 000000000000F083] | Standard SATA AHCI Controller |
| [000000000000F090 - 000000000000F097] | Standard SATA AHCI Controller |
| [000000000000FF00 - 000000000000FFFE] | Motherboard resources |
| [000000000000FFFF - 000000000000FFFF] | Motherboard resources |
| [000000000000FFFF - 000000000000FFFF] | Motherboard resources |
| [000000000000FFFF - 000000000000FFFF] | Motherboard resources |

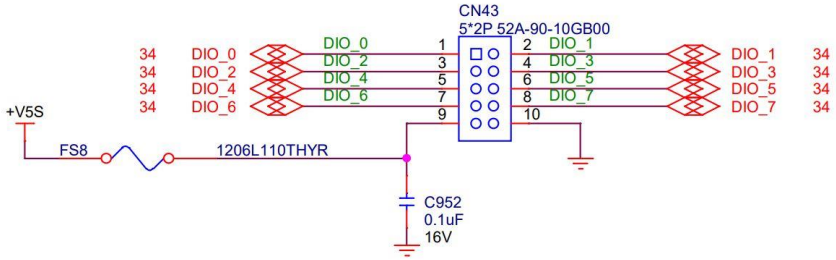
B.2 IRQ Mapping Chart

| | | | |
|---|---|-------------------------|--|
| ▼ |  | Interrupt request (IRQ) | |
| |  | (ISA) 0x00000000 (00) | System timer |
| |  | (ISA) 0x00000003 (03) | Communications Port (COM2) |
| |  | (ISA) 0x00000004 (04) | Communications Port (COM1) |
| |  | (ISA) 0x00000005 (05) | Intel(R) Ethernet Connection (2) I219-LM |
| |  | (ISA) 0x00000005 (05) | Intel(R) HD Graphics 630 |
| |  | (ISA) 0x00000005 (05) | Intel(R) HD Graphics 630 |
| |  | (ISA) 0x00000005 (05) | Intel(R) I211 Gigabit Network Connection |
| |  | (ISA) 0x00000008 (08) | System CMOS/real time clock |
| |  | (ISA) 0x0000000B (11) | Communications Port (COM3) |
| |  | (ISA) 0x0000000B (11) | Communications Port (COM4) |
| |  | (ISA) 0x0000000D (13) | Numeric data processor |
| |  | (ISA) 0x0000000E (14) | Motherboard resources |

Appendix C

Digital I/O Ports

C.1 Electrical Specifications for Digital I/O Ports



| | |
|--------|-------|
| GPIO70 | DIO_0 |
| GPIO71 | DIO_1 |
| GPIO72 | DIO_2 |
| GPIO73 | DIO_3 |
| GPIO74 | DIO_4 |
| GPIO75 | DIO_5 |
| GPIO76 | DIO_6 |
| GPIO77 | DIO_7 |

C.2 DIO Programming

BOXER-6641 utilizes FINTEK F81966 chipset as its Digital I/O controller. The following sections detail the procedures to complete its configuration. The AAEON initial DIO program is also attached to help with developing a customized program for your application.

There are three steps to complete the configuration setup:

- Step 1** Enter MB PnP Mode.
- Step 2** Modify the data in the configuration registers.
- Step 3** Exit MB PnP Mode. Undesired results may occur if MB PnP Mode is not exited properly.

C.2 Digital I/O Register

Table 1: SuperIO relative register table

| | Default Value | Note |
|-------|---------------|--|
| Index | 0x2E(Note1) | SIO MB PnP Mode Index Register 0x2E or 0x4E |
| Data | 0x2F(Note2) | SIO MB PnP Mode Data Register 0x2F or 0x4F |

Table 2: Digital Input relative register table

| | LDN | Register | BitNum | Value | Note |
|------------------|--------------|--------------|-----------|-------|--------|
| DIO-1 Pin Status | 0x06(Note3) | 0x82(Note4) | 0(Note5) | | GPIO70 |
| DIO-2 Pin Status | 0x06(Note6) | 0x82(Note7) | 1(Note8) | | GPIO71 |
| DIO-3 Pin Status | 0x06(Note9) | 0x82(Note10) | 2(Note11) | | GPIO72 |
| DIO-4 Pin Status | 0x06(Note12) | 0x82(Note13) | 3(Note14) | | GPIO73 |
| DIO-5 Pin Status | 0x06(Note15) | 0x82(Note16) | 4(Note17) | | GPIO74 |
| DIO-6 Pin Status | 0x06(Note18) | 0x82(Note19) | 5(Note20) | | GPIO75 |
| DIO-7 Pin Status | 0x06(Note21) | 0x82(Note22) | 6(Note23) | | GPIO76 |
| DIO-8 Pin Status | 0x06(Note24) | 0x82(Note25) | 7(Note26) | | GPIO77 |

Table 3: Digital Output relative register table

| | LDN | Register | BitNum | Value | Note |
|-------------------|--------------|--------------|-----------|----------|--------|
| DIO-1 Output Data | 0x06(Note27) | 0x81(Note28) | 0(Note29) | (Note30) | GPIO70 |
| DIO-2 Output Data | 0x06(Note31) | 0x81(Note32) | 1(Note33) | (Note34) | GPIO71 |
| DIO-3 Output Data | 0x06(Note35) | 0x81(Note36) | 2(Note37) | (Note38) | GPIO72 |
| DIO-4 Output Data | 0x06(Note39) | 0x81(Note40) | 3(Note41) | (Note42) | GPIO73 |
| DIO-5 Output Data | 0x06(Note43) | 0x81(Note44) | 4(Note45) | (Note46) | GPIO74 |
| DIO-6 Output Data | 0x06(Note47) | 0x81(Note48) | 5(Note49) | (Note50) | GPIO75 |
| DIO-7 Output Data | 0x06(Note51) | 0x81(Note52) | 6(Note53) | (Note54) | GPIO76 |
| DIO-8 Output Data | 0x06(Note55) | 0x81(Note56) | 7(Note57) | (Note58) | GPIO77 |

C.3 Digital I/O Sample Program

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```

```

*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte DOutput1LDN // This parameter is represented from Note27
#define byte DOutput1Reg // This parameter is represented from Note28
#define byte DOutput1Bit // This parameter is represented from Note29
#define byte DOutput1Val // This parameter is represented from Note30
#define byte DOutput2LDN // This parameter is represented from Note31
#define byte DOutput2Reg // This parameter is represented from Note32
#define byte DOutput2Bit // This parameter is represented from Note33
#define byte DOutput2Val // This parameter is represented from Note34
#define byte DOutput3LDN // This parameter is represented from Note35
#define byte DOutput3Reg // This parameter is represented from Note36
#define byte DOutput3Bit // This parameter is represented from Note37
#define byte DOutput3Val // This parameter is represented from Note38
#define byte DOutput4LDN // This parameter is represented from Note39
#define byte DOutput4Reg // This parameter is represented from Note40
#define byte DOutput4Bit // This parameter is represented from Note41
#define byte DOutput4Val // This parameter is represented from Note42
#define byte DOutput5LDN // This parameter is represented from Note43
#define byte DOutput5Reg // This parameter is represented from Note44
#define byte DOutput5Bit // This parameter is represented from Note45
#define byte DOutput5Val // This parameter is represented from Note46
#define byte DOutput6LDN // This parameter is represented from Note47
#define byte DOutput6Reg // This parameter is represented from Note48
#define byte DOutput6Bit // This parameter is represented from Note49
#define byte DOutput6Val // This parameter is represented from Note50
#define byte DOutput7LDN // This parameter is represented from Note51
#define byte DOutput7Reg // This parameter is represented from Note52
#define byte DOutput7Bit // This parameter is represented from Note53
#define byte DOutput7Val // This parameter is represented from Note54
#define byte DOutput8LDN // This parameter is represented from Note55
#define byte DOutput8Reg // This parameter is represented from Note56
#define byte DOutput8Bit // This parameter is represented from Note57
#define byte DOutput8Val // This parameter is represented from Note58
*****

```

```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean  AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```

*****
VOID  SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

```
*****
Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID  ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****
```