BOXER-6403WT

Fanless Embedded Box PC

User's Manual 1st Ed

Last Updated: March 25, 2016

Copyright Notice

Acknowledgement

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● BOXER-6403WT	1
● Burn-proof bracket	1
● RJ-45 to D-sub cable	3
● Power adapter	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

18. If any of the following situations arises, please the contact our service personnel:

    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device

19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

FCC Statement

This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.
Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	○	○	○	○	○	○
外部信号连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：

一、此产品所标示之环保使用期限，系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	O	O	O	O	O	O
Wires & Connectors for External Connections	O	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	O	O	O	O	O	O
Hard Disk	O	O	O	O	O	O
PSU	O	O	O	O	O	O

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

Table of Contents

Chapter 1

Product Specifications

1.1 Specifications

● Processor		Intel® Celeron®/Atom™ Processor
● System Memory		DDR3L 1333 MHz SODIMM x 1, up to 8 GB
● Chipset		Intel® Atom™ E3845
● Display Interface	HDMI	-
	DVI	DVI-D x 1
	VGA	VGA x 1
	Others	18/24-bit single channel Onboard LVDS x 1 (internal)
● Storage Device	CF-SATA	-
	HDD/SSD	-
	Others	mSATA (half-size)
● Network	LAN	Gigabit Ethernet
	Wireless	Optional
● Front I/O	USB Host	USB 3.0 x 1 USB 2.0 x 2
	LAN	-
	Serial Port	-
	DIO	DIO x 6 (DI x 4, DO x 2, w/o isolation)
	Audio	-
	KB/MS	-
	Others	Power Button x 1
● Rear I/O	USB Host	-
	LAN	RJ-45 x 2
	Serial Port	RJ-45 x 2 for RS-232/422/485 (BIO Selection)

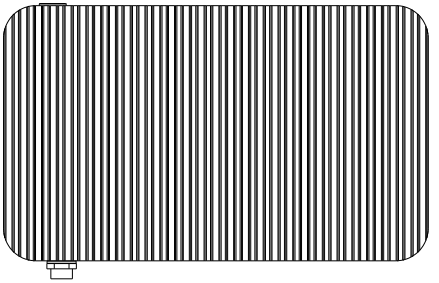
	DIO	-
	Audio	-
	KB/MS	-
	Others	Lockable DC Jack x 1, HDMI x 1
● Expansion	PCIe	—
	PCI	—
	MiniCard	Half-size MiniCard (mSATA only) x 1 Full-size MiniCard w/ SIM slot x 1
	Mini PCI	—
	Others	Onboard USB Pin header x 1
● Indicator	Front	—
	Rear	—
● Power Requirement		12V DC in with lockable connector ATX mode (optional for AT by jumper/BIOS setting)
● Power Consumption		-
● System Cooling		Passive cooling
● Mounting		VESA/ DIN-rail (Wall/ DIN-rail kit)
● Dimension (W x H x D)		158 x 95 x 20mm (6.22 x 3.74 x 0.79")
● Gross Weight		1.16 kg (2.56 lbs)
● Certification	EMC	CE/FCC Class A
	Safety	—
● Operating Temperature		-20 ~ 40°C (-4 ~ 104°F) without airflow (mSATA) -30 ~ 70°C (-4 ~ 158°F) with airflow (mSATA)
● Storage Temperature		-30C ~ 80°C (-22 ~ 176°F)
● Anti-Vibration		3 Grms/ 5~500 Hz/ operation (mSATA)

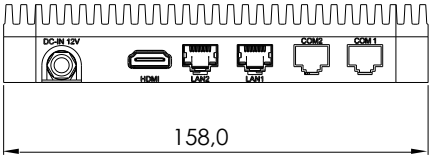
- **Anti-Shock** 20 G peak acceleration (11 msec. duration, mSATA)

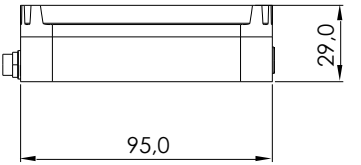
Chapter 2

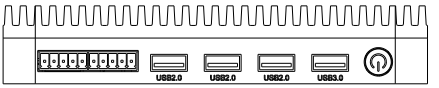
Hardware Information

2.1 Dimensions







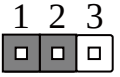


2.2 List of Jumpers

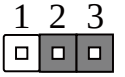
Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP1	AT/ATX Mode Selection
JP2	LVDS BKLT Control Selection
JP3	LVDS Power Selection
JP4	LVDS BKLT Control Selection
JP5	Clear CMOS Jumper
JP6	Dry and Wet Contact Digital Input Power Selection
JP7	Dry and Wet Contact Digital Output Power Selection

2.2.1 AT/ATX Mode Selection (JP1)

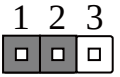


ATX Mode (Default)

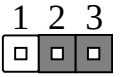


AT Mode

2.2.2 LVDS BKLT Control Selection (JP2)

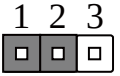


VR Mode

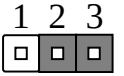


PWM Mode (Default)

2.2.3 LVDS Power Selection (JP3)

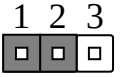


5 V

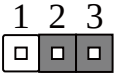


3.3 V (Default)

2.2.4 LVDS BKLT Power Selection (JP4)

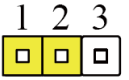


12 V

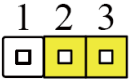


5 V (Default)

2.2.5 Clear CMOS Jumper (JP5)

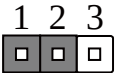


Normal (Default)

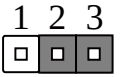


Clear CMOS

2.2.6 Dry and Wet Contact Digital Input Power Selection (JP6)

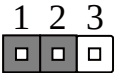


Wet Contact Digital Input

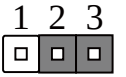


Dry Contact Digital Input (Default)

2.2.7 Dry and Wet Contact Digital Output Power Selection (JP7)



Wet Contact Digital Output



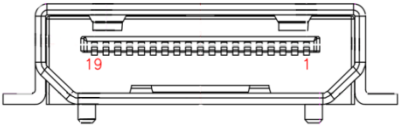
Dry Contact Digital Output (Default)

2.3 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
CN1	HDMI Display
CN2	USB 3.0 Connector
CN4	COM2 RS-232/422/485
CN11	LPC Expansion I/F
CN16	COM3 RS-232 I/F
CN17	COM1 RS-232/422/485
CN22	BIOS SPI Flash Header
CN23	Dry and Wet Contact Digital Input
CN24	Dry and Wet Contact Digital Output
CN26	RJ-45 Ethernet Port
CN27	RJ-45 Ethernet Port
USB1	USB 2.0 Port 1 Connector
USB2	USB 2.0 Port 2 Connector
USB3	USB 2.0 Port 3 Connector
BAT1	Battery Connector
DIMM1	DDR3L SODIMM Slot
PCIE1	mSATA Half Size MiniCard Slot
PCIE2	PCI-E Full Size MiniCard Slot

2.3.1 HDMI Display (CN1)

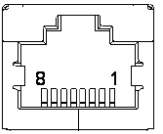


Pin	Pin Name	Signal Type	Signal Level
1	HDMI_TX2+		DIFF
2	GND	GND	
3	HDMI_TX2-		DIFF
4	HDMI_TX1+		DIFF
5	GND		GND
6	HDMI_TX1-		DIFF
7	HDMI_TX0+		DIFF
8	GND		GND
9	HDMI_TX0-		DIFF
10	HDMI_CLK+		DIFF
11	GND		GND
12	HDMI_CLK-		DIFF
13	NC		NC
14	NC		NC
15	HDMI_DDC_CLK	I/O	+5V
16	HDMI_DDC_DATA	I/O	+5V
17	GND		GND
18	HDMI_PWR	PWR	+5V
19	HDMI_HPD		IN

2.3.2 USB 3.0 Connector (CN2)

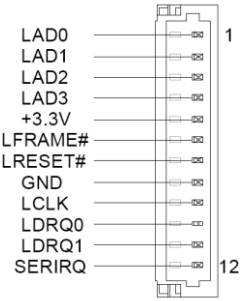
Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	
5	USB3.0 RX-	DIFF	
6	USB3.0 RX+	DIFF	
7	GND	GND	
8	USB3.0 TX-	DIFF	
9	USB3.0 TX+	DIFF	

2.3.3 COM2 RS-232/422/485 Connector (CN4)



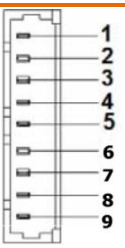
Pin	RS-232	RS-422	RS-485
1	DSR		
2	RTS		
3	GND		
4	TX	RX+	
5	RX	TX+	DATA+
6	DCD	TX-	DATA-
7	CTS		
8	DTR	RX	

2.3.4 LPC Expansion I/F (CN11)



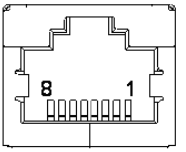
Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	LDRQ0	IN	
11	LDRQ1	IN	
12	SERIRQ	I/O	+3.3V

2.3.5 COM3 RS-232 I/F (CN16)



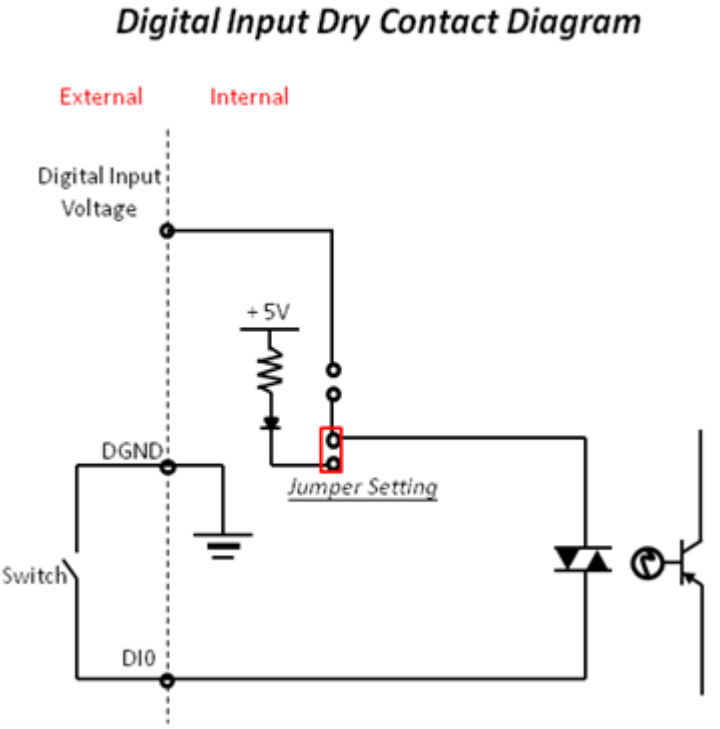
Pin	RS-232
1	DCD
2	DSR
3	RX
4	RTS
5	TX
6	CTS
7	DTR
8	RI
9	GND

2.3.6 COM1 RS-232/422/485 Connector (CN17)

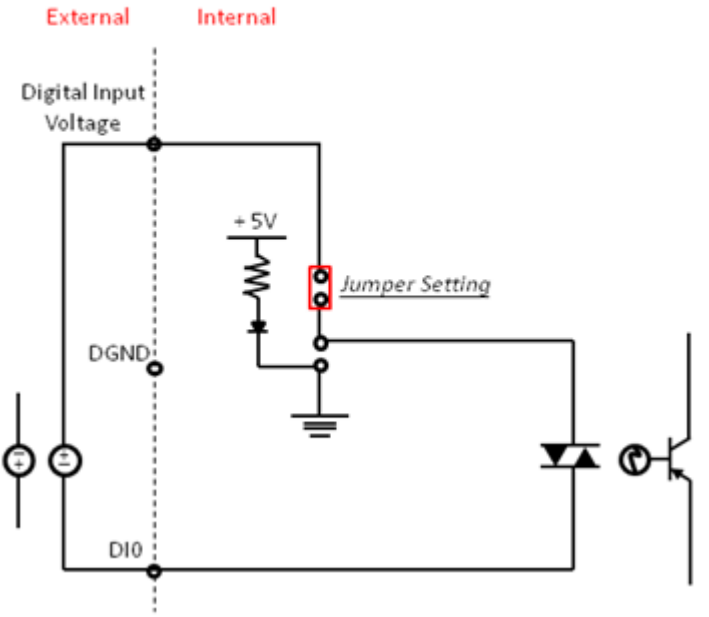


Pin	RS-232	RS-422	RS-485
1	DSR		
2	RTS		
3	GND		
4	TX	RX+	
5	RX	TX+	DATA+
6	DCD	TX-	DATA-
7	CTS		
8	DTR	RX	

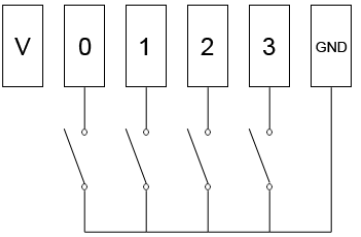
2.3.7 Dry and Wet Contact Digital Input (CN23)

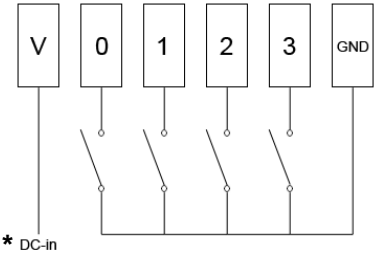


Digital Input Wet Contact Diagram



Dry Contact Wiring	Wet Contact Wiring





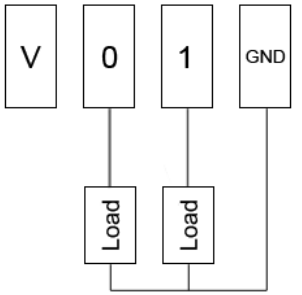
Digital input voltage range	
Max	Min
10 ~ 25 V	5 V

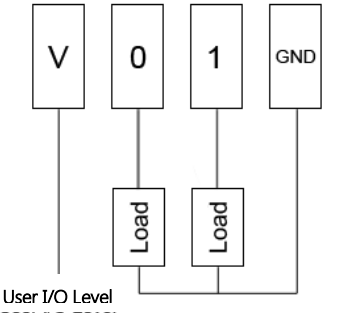
Pin	Pin Name	Signal Type	Signal Level
1	Digital input 3	Input	DRY (5V) WET (3~30V)

2	Digital input 2	Input	DRY (5V) WET (3~30V)
3	Digital input 1	Input	DRY (5V) WET (3~30V)
4	Digital input 0	Input	DRY (5V) WET (3~30V)
5	WET contact POWER	PWR	3~30V

2.3.8 Dry and Wet Contact Digital Output (CN24)

Dry Contact Wiring	Wet Contact Wiring

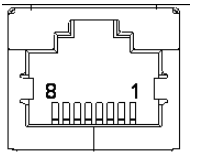




Digital output voltage range	
Max	Min
30 V	5 V

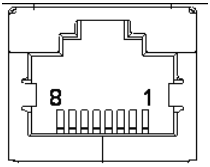
Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	Digital output 5	Input	Open collector to 30 VDC
3	Digital output 4	Input	Open collector to 30 VDC
4	Digital output POWER	Input	3 ~ 30 V
5	GND	GND	

2.3.9 RJ-45 Ethernet Port (CN26)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	
7	MDI3+	DIFF	
8	MDI3-	DIFF	

2.3.10 RJ-45 Ethernet Port (CN27)



Pin	Pin Name	Signal Type	Signal Level
1	MDI0+	DIFF	
2	MDI0-	DIFF	
3	MDI1+	DIFF	
4	MDI2+	DIFF	
5	MDI2-	DIFF	
6	MDI1-	DIFF	

7	MDI3+	DIFF
8	MDI3-	DIFF

2.3.11 USB 2.0 Port 1 Connector (USB1)

Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	

2.3.12 USB 2.0 Port 2 Connector (USB2)

Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	

2.3.13 USB 2.0 Port 3 Connector (USB3)

Pin	Pin Name	Signal Type	Signal Level
1	+5V	PWR	+5V
2	USB_D-	DIFF	
3	USB_D+	DIFF	
4	GND	GND	

2.3.14 DDR3L SODIMM Slot (DIMM1)

Standard Specifications

2.3.15 Half Size MiniCard Slot (PCIE1)

Pin	Pin Name	Signal Type	Signal Level
1		NC	
2	+3.3V	PWR	+3.3V
3		NC	
4	GND	GND	
5		NC	
6	+1.5V	PWR	+1.5V
7		NC	
8		NC	
9	GND	GND	
10		NC	
11		NC	
12		NC	
13		NC	
14		NC	
15	GND	GND	
16		NC	
17		NC	
18	GND	GND	
19		NC	
20		NC	
21	GND	GND	

22		NC	
23	mSATA RX+	DIFF	
24	+3.3V	PWR	+3.3V
25	mSATA RX-	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	mSATA_TX	DIFF	
32	SMB_DATA	I/O	+3.3V
33	mSATA_TX+	DIFF	
34	GND	GND	
35	GND	GND	
36		NC	
37	GND	GND	
38		NC	
39	+3.3V	PWR	+3.3V
40	GND	GND	
41	+3.3V	PWR	+3.3V
42		NC	
43		NC	
44		NC	
45		NC	
46		NC	
47		NC	
48	+1.5V	PWR	+1.5V

49		NC	
50	GND	GND	
51		NC	
52	+3.3V	PWR	+3.3V

2.3.16 PCI-E Full Size MiniCard Slot (PCIE2)

Pin	Pin Name	Signal Type	Signal Level
1		NC	
2	+3.3V	PWR	+3.3V
3		NC	
4	GND	GND	
5		NC	
6	+1.5V	PWR	+1.5V
7		NC	
8		NC	
9	GND	GND	
10		NC	
11		NC	
12		NC	
13		NC	
14		NC	
15	GND	GND	
16		NC	
17		NC	
18	GND	GND	
19		NC	

20		NC	
21	GND	GND	
22		NC	
23	PCIE RX-	DIFF	
24	+3.3V	PWR	+3.3V
25	PCIE RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE TX	DIFF	
32	SMB_DATA	I/O	
33	PCIE TX+	DIFF	
34	GND	GND	
35	GND	GND	
36		NC	
37	GND	GND	
38		NC	
39	+3.3V	PWR	+3.3V
40	GND	GND	
41	+3.3V	PWR	+3.3V
42		NC	
43		NC	
44		NC	
45		NC	
46		NC	

47		NC	
48	+1.5V	PWR	+1.5V
49		NC	
50	GND	GND	
51		NC	
52	+3.3V	PWR	+3.3V

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

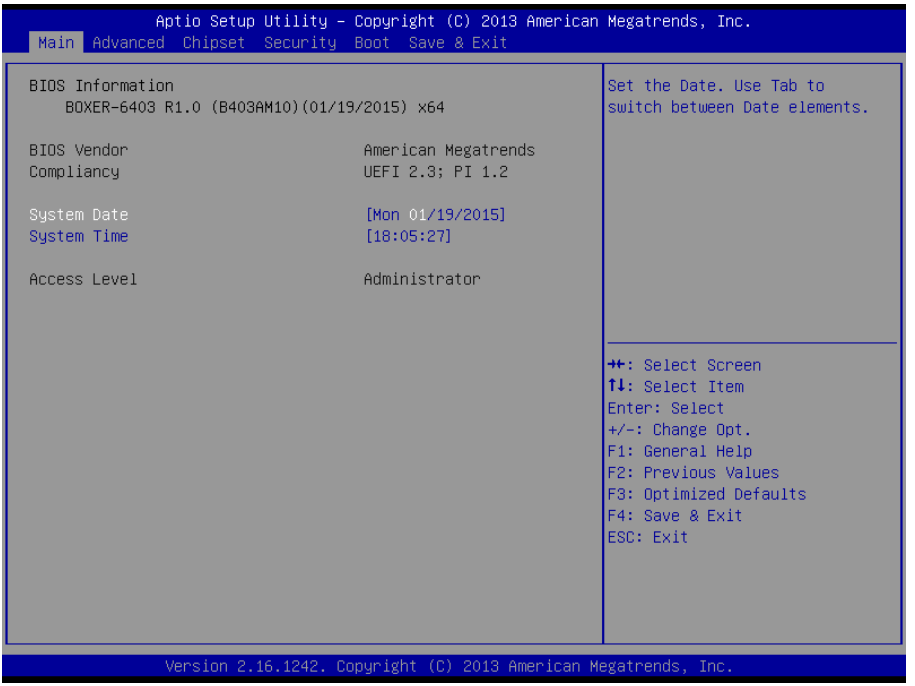
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

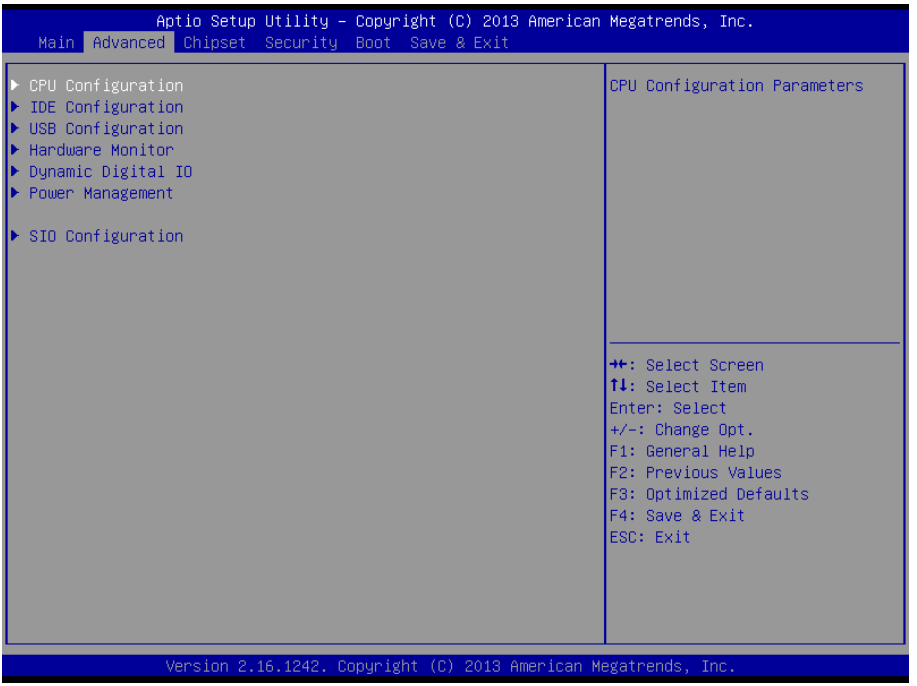
Security – The setup administrator password can be set here

Save & Exit –Save your changes and exit the program

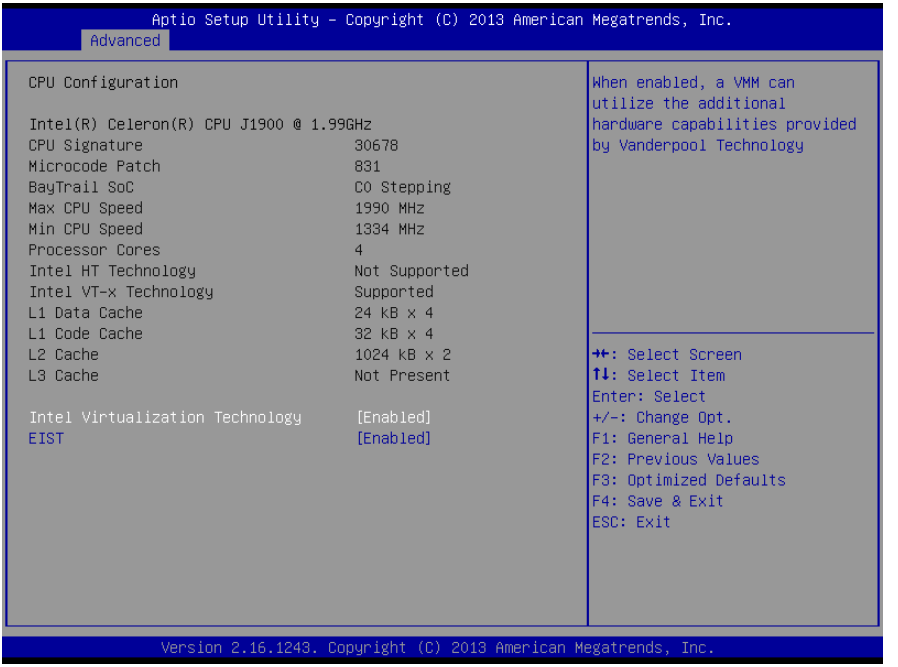
3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



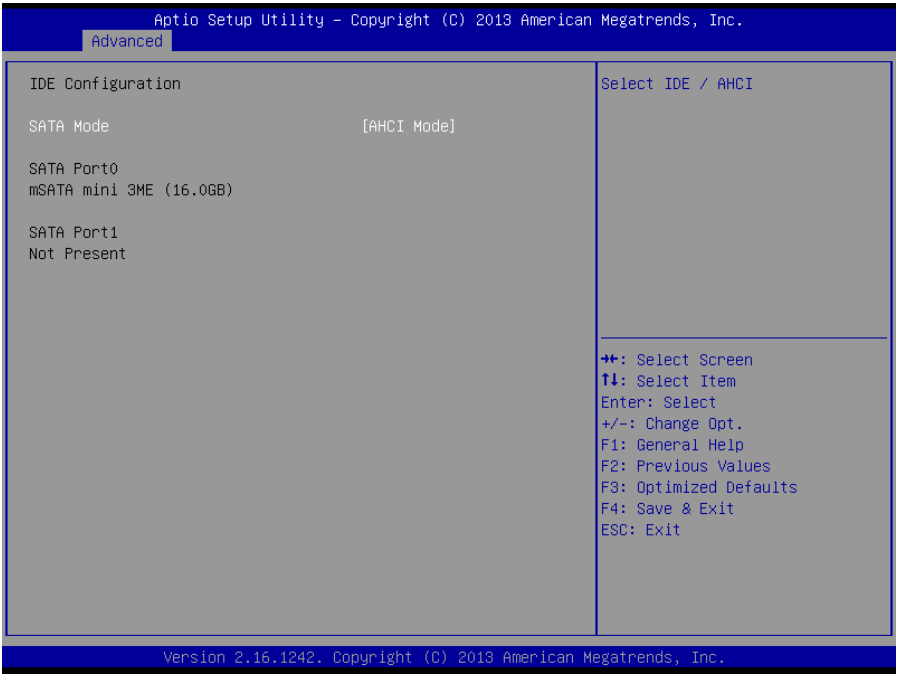
3.4.1 Advanced: CPU Configuration



Options summary:

Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default

3.4.2 Advanced: IDE Configuration



Options summary:

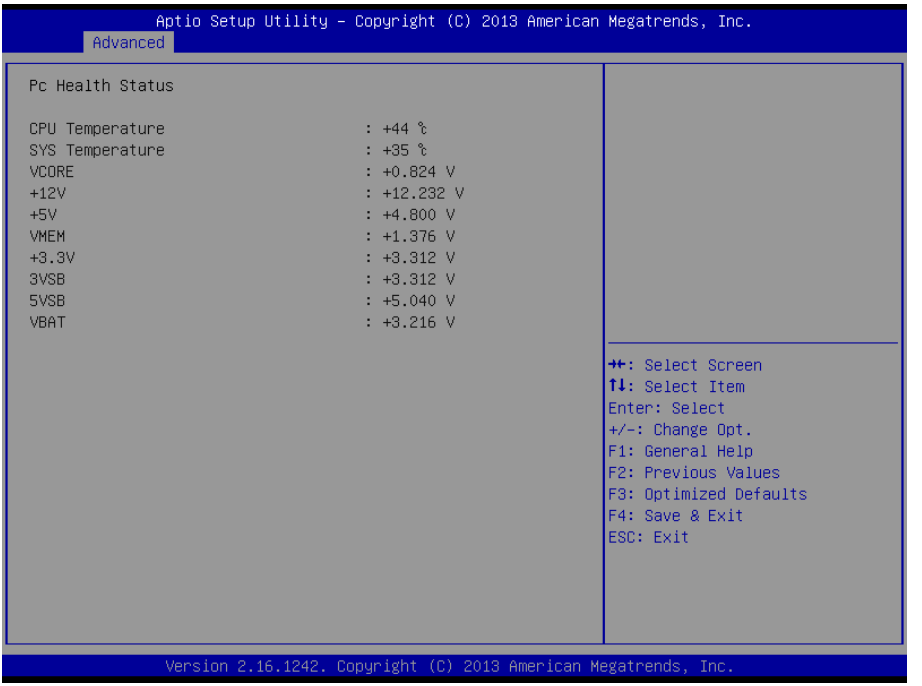
SATA Mode	IDE Mode	
	AHCI Mode	Optimal Default, Failsafe Default

3.4.3 Advanced: USB Configuration

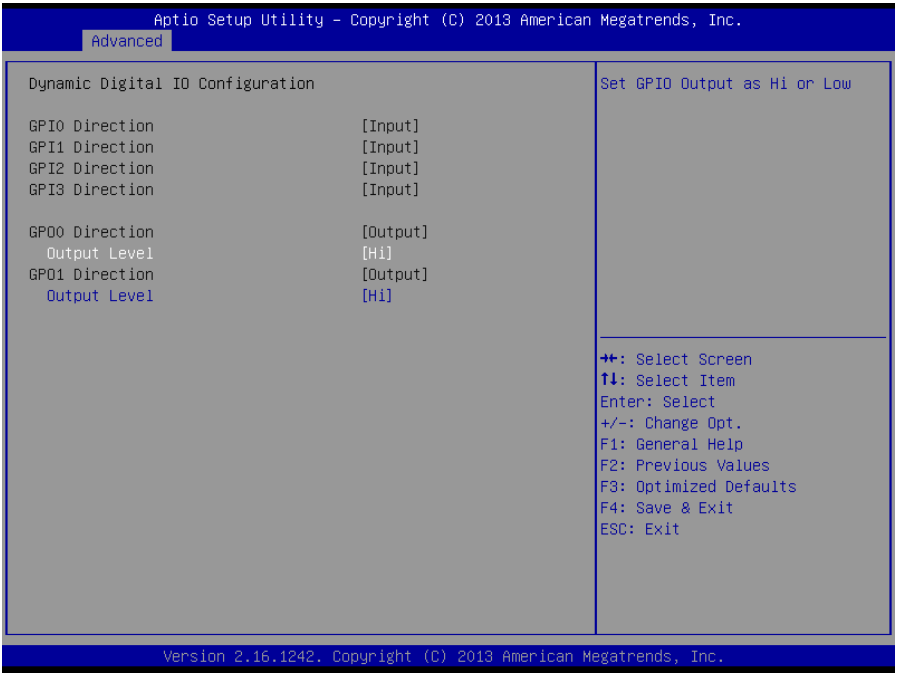
Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected		

3.4.4 Advanced: Hardware Monitor



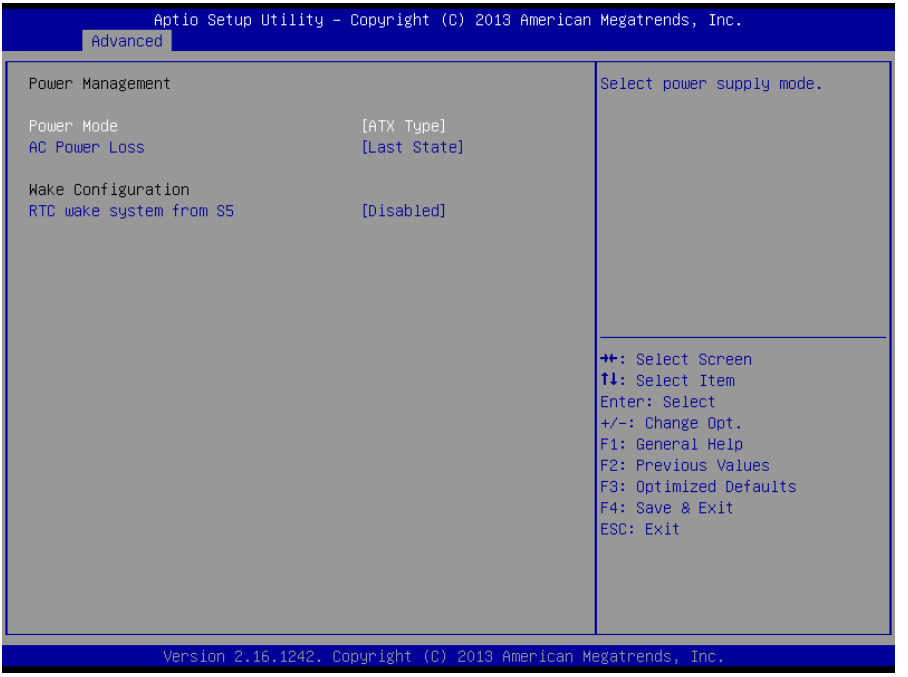
3.4.5 Advanced: Dynamic Digital IO Configuration



Options summary:

GPO0 Direction [Output] Output Level	Low	
	Hi	Optimal Default, Failsafe Default
GPO1 Direction [Output] Output Level	Low	
	Hi	Optimal Default, Failsafe Default

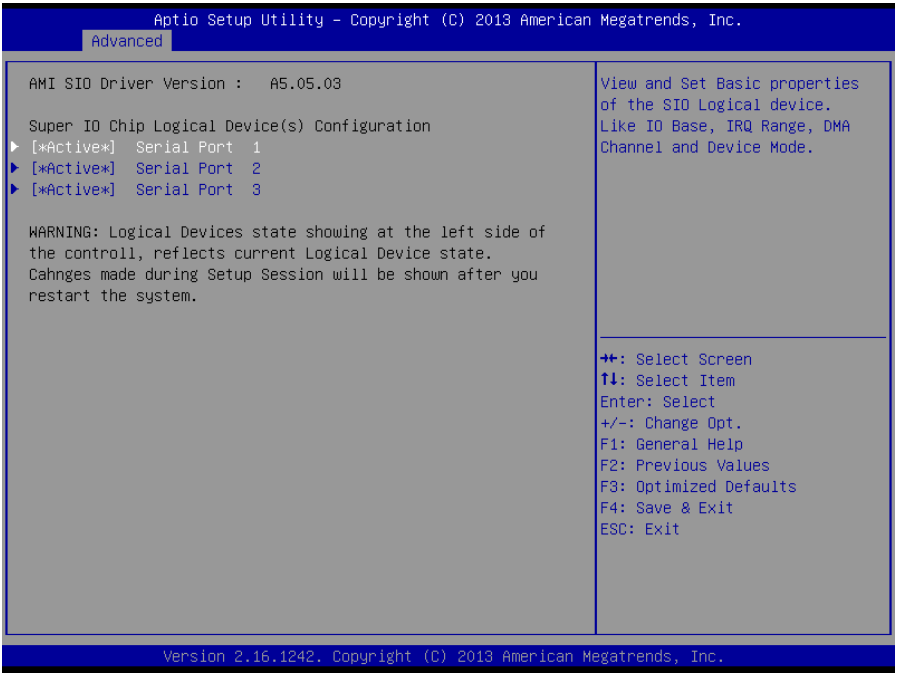
3.4.6 Advanced: Power Management



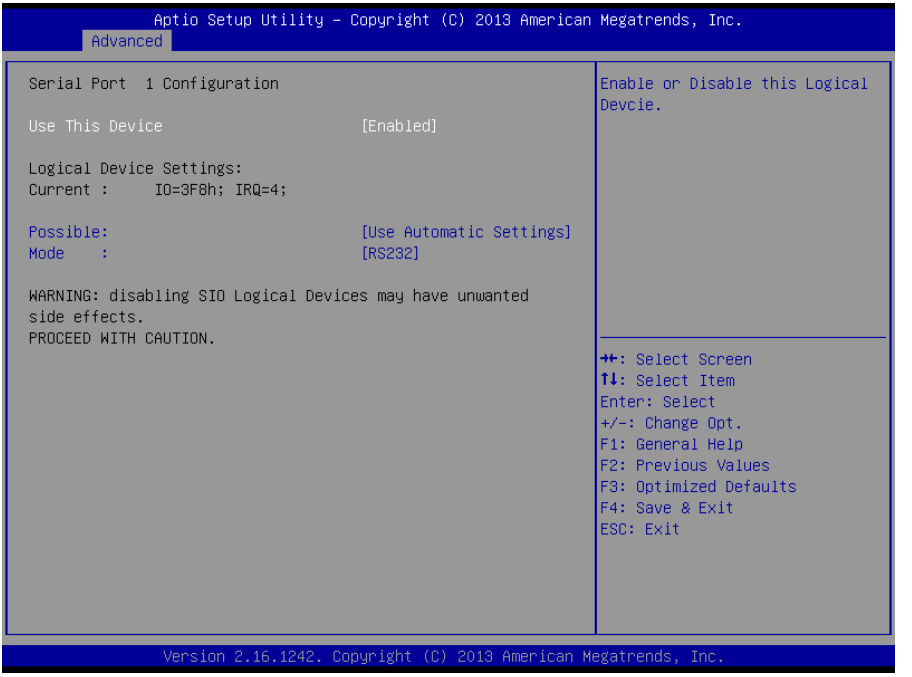
Options summary:

Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select power supply mode.		
AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Off	
Select power state when power is re-applied after a power failure.		
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		

3.4.7 Advanced: SIO Configuration



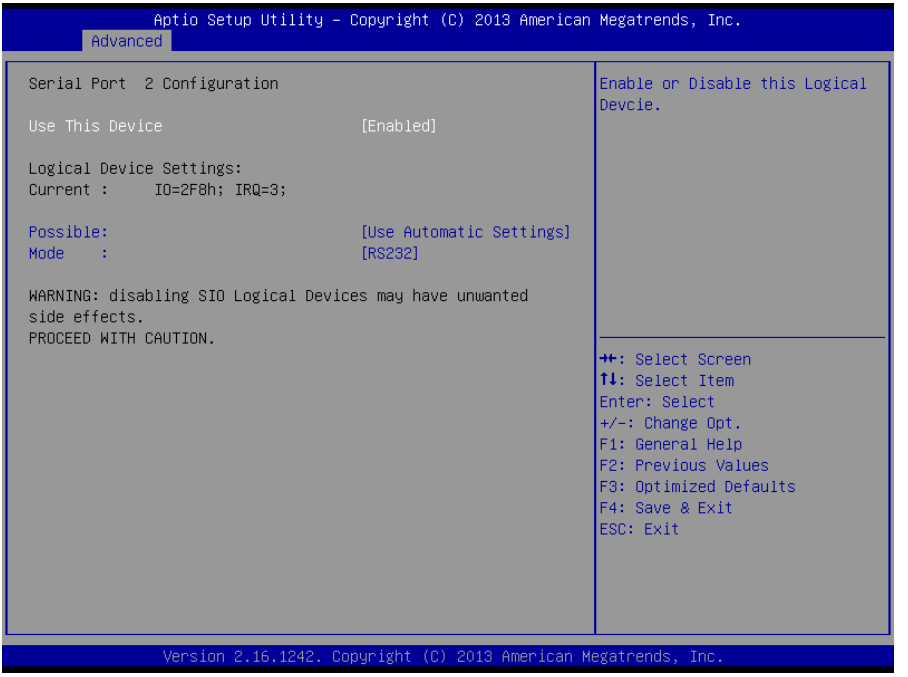
3.4.7.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	

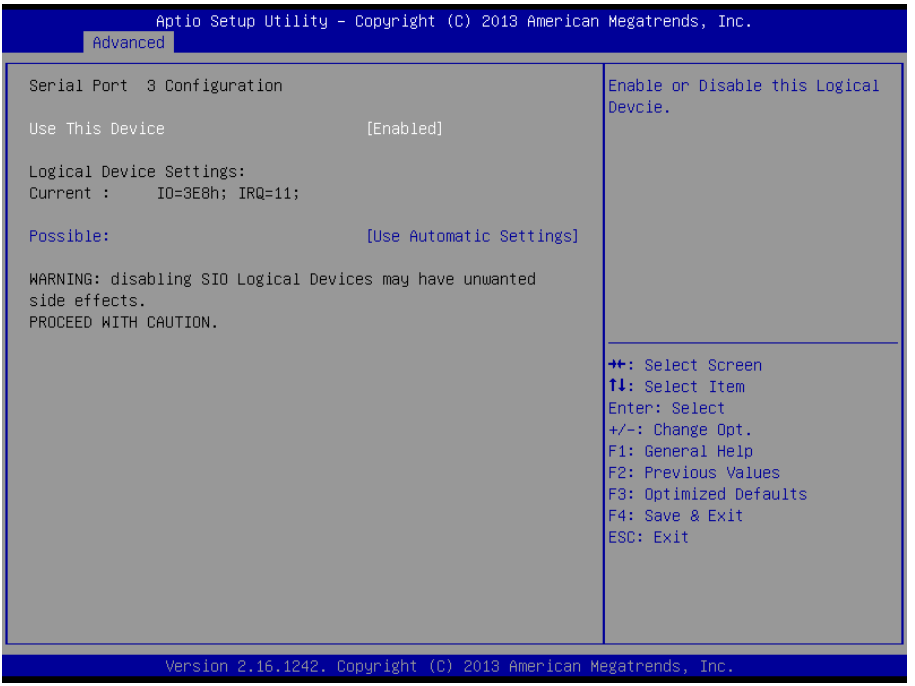
3.4.7.2 SIO Configuration: Serial Port 2 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS485	

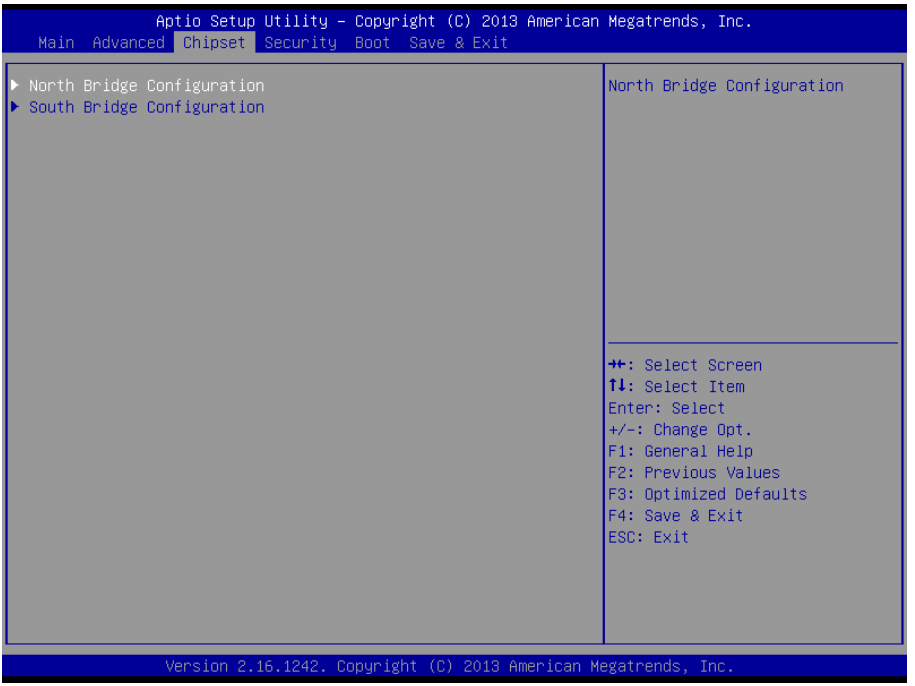
3.4.7.3 SIO Configuration: Serial Port 3 Configuration



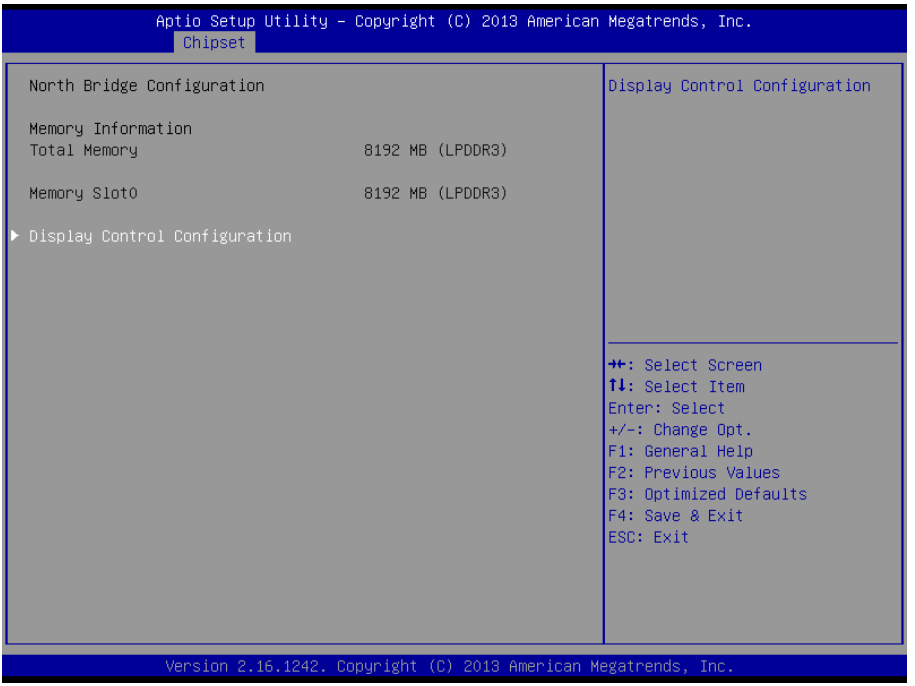
Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8; IRQ=11;	
	IO=2E8; IRQ=11;	
Select an optimal setting for IO device		

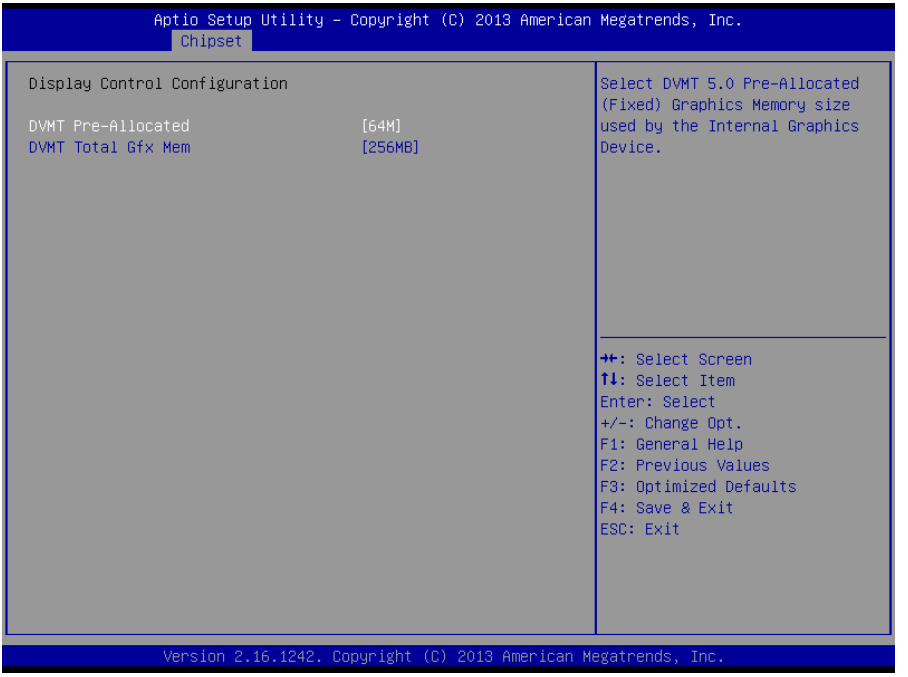
3.5 Setup submenu: Chipset



3.5.1 Chipset: North Bridge



3.5.1.1 Display Control Configuration

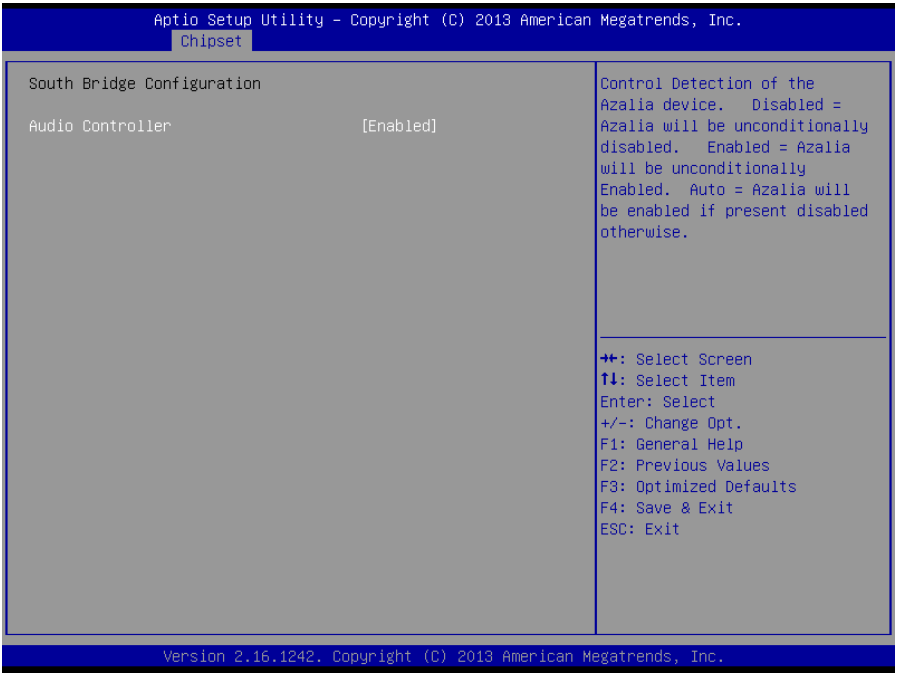


Options summary:

DVMT Pre-Allocated	64M	Optimal Default, Failsafe Default
	96M	
	128M	
	160M	
	192M	
	224M	
	256M	
	288M	
	320M	
	352M	
	384M	
	416M	
	448M	
	480M	
	512M	
DVMT Total Gfx Mem	128MB	

	256MB	Optimal Default, Failsafe Default
	Max	

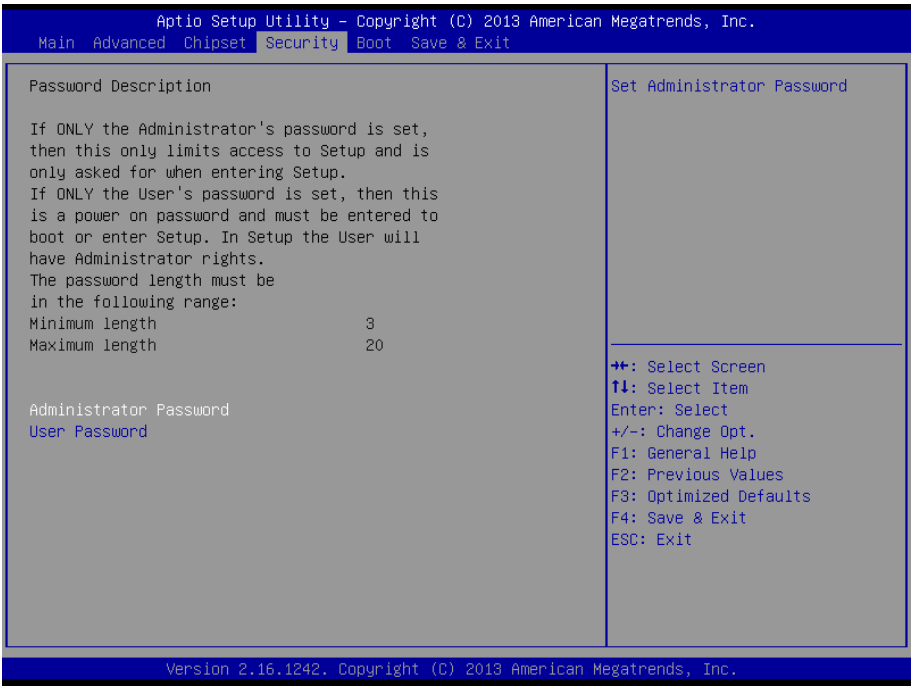
3.5.2 South Bridge



Options summary:

Audio Controller	Disabled	Optimal Default, Failsafe Default
	Enabled	

3.6 Security



Change User/Administrator Password

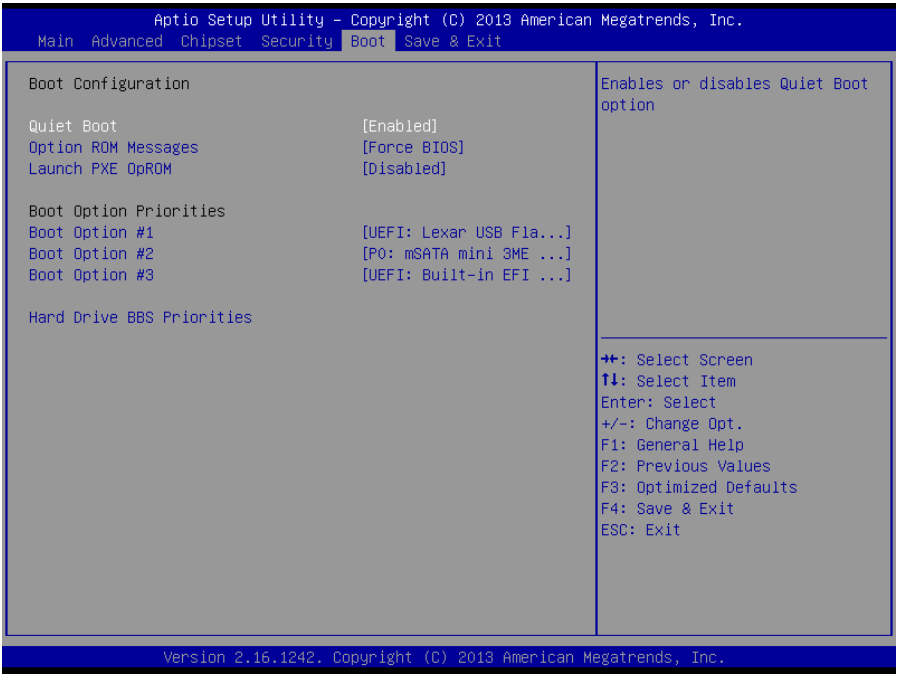
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

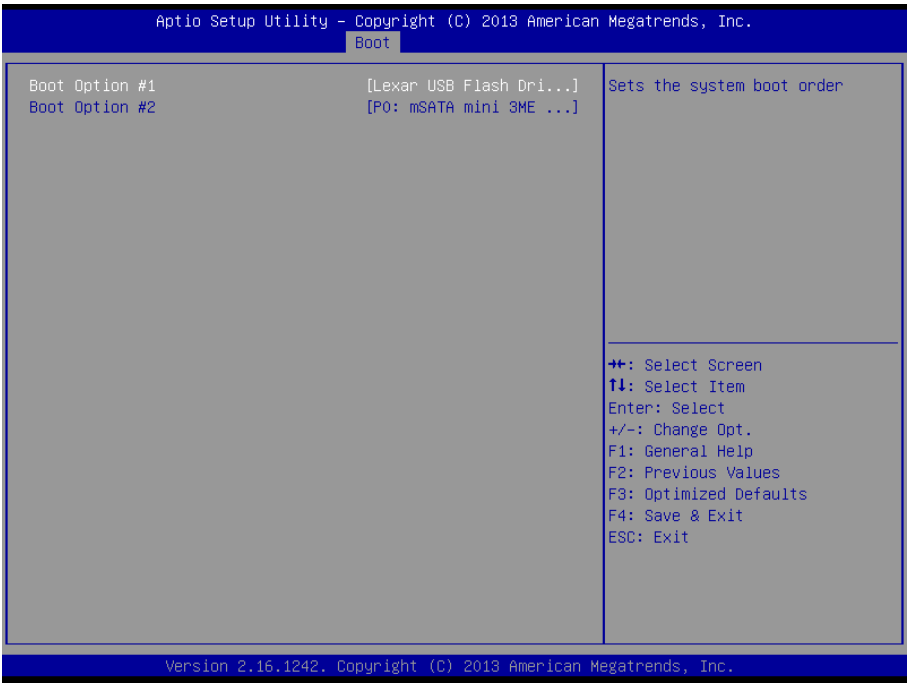
3.7 Setup submenu: Boot



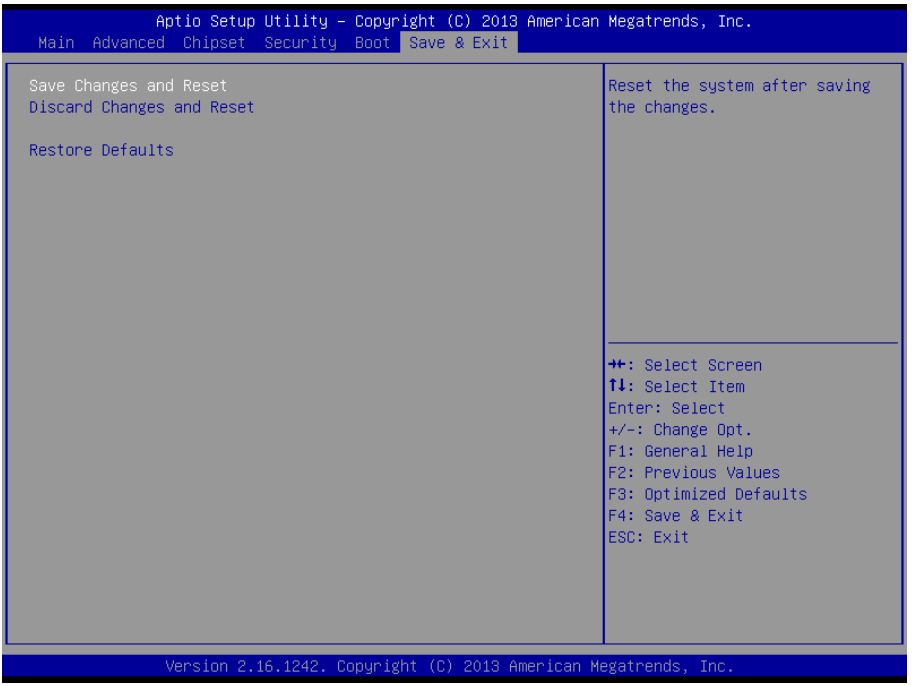
Options summary:

Quiet Boot	Disabled	
	Enabled	Default
En/Disable showing boot logo.		
Option ROM Messages	Force BIOS	Default
	Keep Current	
Set display mode for Option ROM		
Launch PXE OpROM	Disabled	Default
	Enabled	
En/Disable Legacy Boot Option		

3.7.1 BBS Priorities



3.8 Setup submenu: Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The BOXER-6403WT comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder followed by the **SetupChipset.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphics** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 – Install Network Driver

1. Open the **Step 3 - Network** folder and select your OS
2. Open the**.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 – Install xHCI Driver (Windows 7 only)

1. Open the **Step 4 - xHCI** folder and followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Step 5 – Install Intel Sideband Fabric Device Drivers (Windows 8.1 only)

1. Open the **Step 5 - Intel Sideband Fabric Device** followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
*******************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN    //This parameter is represented from Note5
#define byte   UnitReg    //This parameter is represented from Note6
#define byte   UnitBit    //This parameter is represented from Note7
#define byte   UnitVal    //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
*******************************************************************************
```

```
*********************************************************************************
VOID    Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

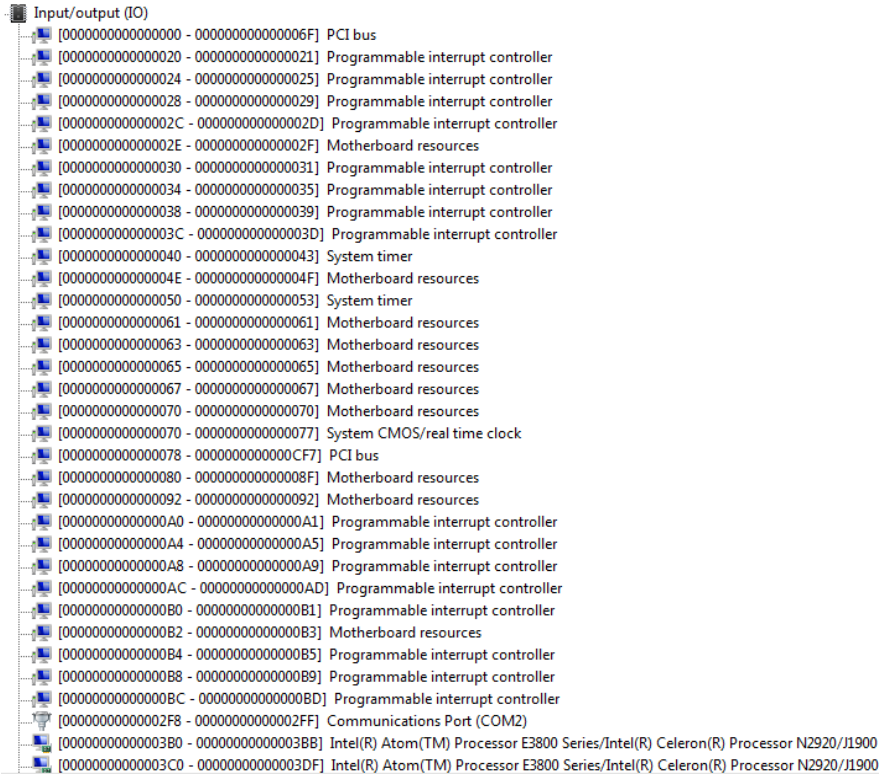
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
       SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
       SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*******************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix B

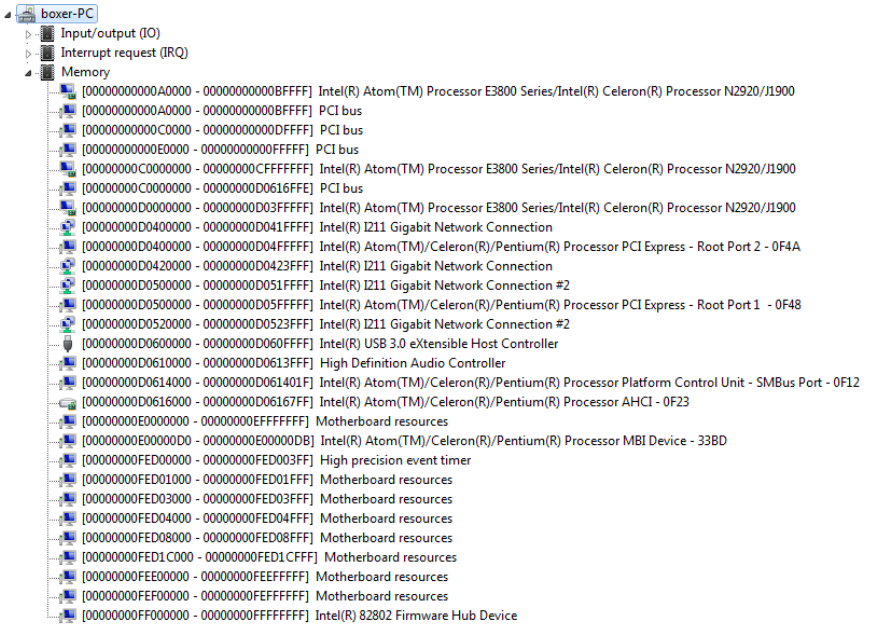
I/O Information

B.1 I/O Address Map

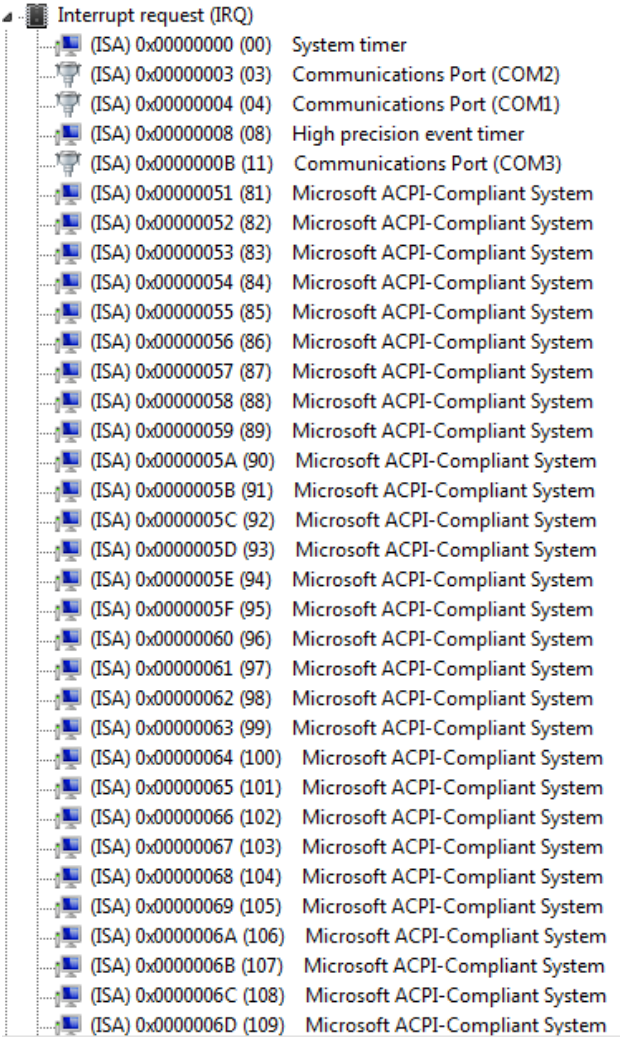


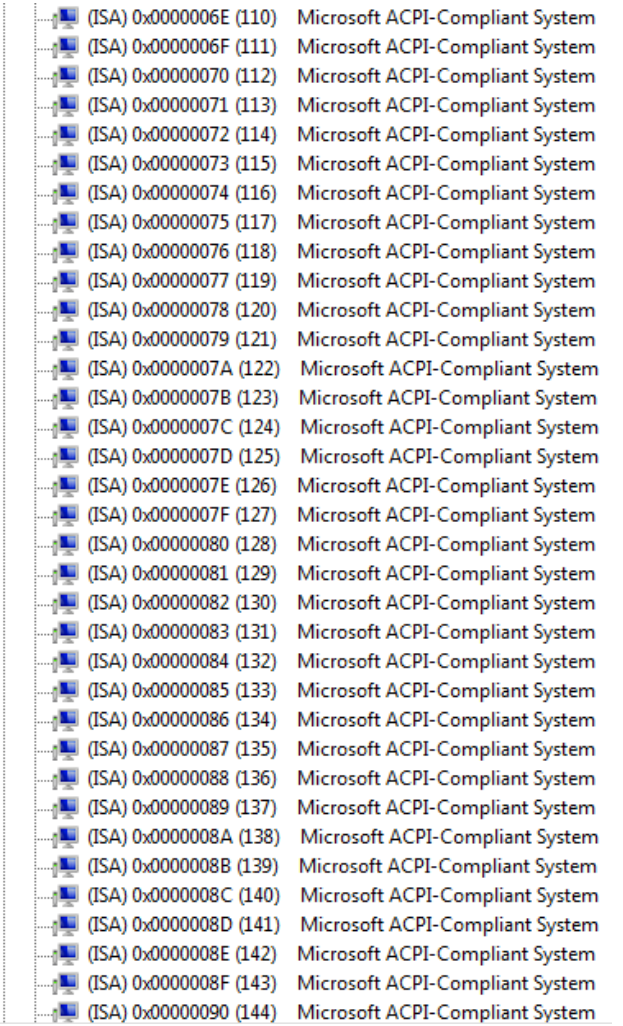
- [0000000000000078 - 0000000000000CF7] PCI bus
- [0000000000000080 - 000000000000008F] Motherboard resources
- [0000000000000092 - 0000000000000092] Motherboard resources
- [00000000000000A0 - 00000000000000A1] Programmable interrupt controller
- [00000000000000A4 - 00000000000000A5] Programmable interrupt controller
- [00000000000000A8 - 00000000000000A9] Programmable interrupt controller
- [00000000000000AC - 00000000000000AD] Programmable interrupt controller
- [00000000000000B0 - 00000000000000B1] Programmable interrupt controller
- [00000000000000B2 - 00000000000000B3] Motherboard resources
- [00000000000000B4 - 00000000000000B5] Programmable interrupt controller
- [00000000000000B8 - 00000000000000B9] Programmable interrupt controller
- [00000000000000BC - 00000000000000BD] Programmable interrupt controller
- [00000000000002F8 - 00000000000002FF] Communications Port (COM2)
- [00000000000003B0 - 00000000000003BB] Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900
- [00000000000003C0 - 00000000000003DF] Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900
- [00000000000003E8 - 00000000000003EF] Communications Port (COM3)
- [00000000000003F8 - 00000000000003FF] Communications Port (COM1)
- [0000000000000400 - 000000000000047F] Motherboard resources
- [00000000000004D0 - 00000000000004D1] Programmable interrupt controller
- [0000000000000500 - 00000000000005FE] Motherboard resources
- [0000000000000600 - 000000000000061F] Motherboard resources
- [0000000000000680 - 000000000000069F] Motherboard resources
- [0000000000000A00 - 0000000000000A0F] Motherboard resources
- [0000000000000A10 - 0000000000000A1F] Motherboard resources
- [0000000000000A20 - 0000000000000A2F] Motherboard resources
- [0000000000000D00 - 000000000000FFFF] PCI bus
- [000000000000C000 - 000000000000CFFF] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 2 - 0F4A
- [000000000000D000 - 000000000000DFFF] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 1 - 0F48
- [000000000000E000 - 000000000000E01F] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Platform Control Unit - SMBus Port - 0F12
- [000000000000E020 - 000000000000E03F] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- [000000000000E040 - 000000000000E043] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- [000000000000E050 - 000000000000E057] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- [000000000000E060 - 000000000000E063] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- [000000000000E070 - 000000000000E077] Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- [000000000000E080 - 000000000000E087] Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900

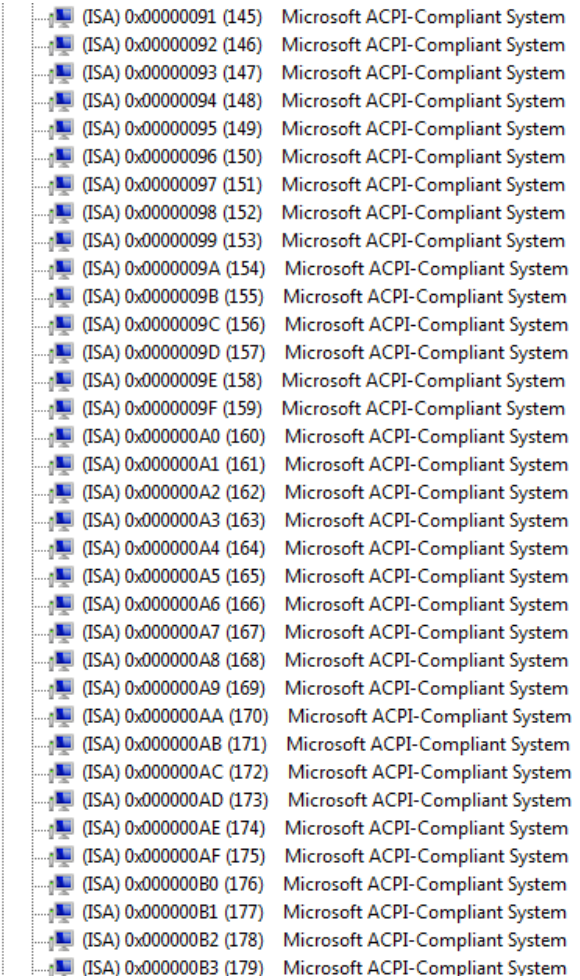
B.2 Memory Address Map



B.3 IRQ Mapping Chart




(ISA) 0x0000006E (110) Microsoft ACPI-Compliant System
(ISA) 0x0000006F (111) Microsoft ACPI-Compliant System
(ISA) 0x00000070 (112) Microsoft ACPI-Compliant System
(ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
(ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
(ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
(ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
(ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
(ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
(ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
(ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
(ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
(ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
(ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
(ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
(ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
(ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
(ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
(ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
(ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
(ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
(ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
(ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
(ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
(ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
(ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
(ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
(ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
(ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
(ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
(ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
(ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
(ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
(ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
(ISA) 0x00000090 (144) Microsoft ACPI-Compliant System


(ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
(ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
(ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
(ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
(ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
(ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
(ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
(ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
(ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
(ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
(ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
(ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
(ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
(ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
(ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
(ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
(ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
(ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
(ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
(ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
(ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
(ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
(ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
(ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
(ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
(ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
(ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System

- (ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
- (ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
- (ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
- (ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
- (ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
- (ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
- (ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
- (ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
- (ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
- (ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
- (ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
- (PCI) 0x00000005 (05) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor Platform Control Unit - SMBus Port - 0F12
- (PCI) 0x00000010 (16) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 1 - 0F48
- (PCI) 0x00000011 (17) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 2 - 0F4A
- (PCI) 0x00000012 (18) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 3 - 0F4C
- (PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor AHCI - 0F23
- (PCI) 0x00000013 (19) Intel(R) Atom(TM)/Celeron(R)/Pentium(R) Processor PCI Express - Root Port 4 - 0F4E
- (PCI) 0x00000016 (22) High Definition Audio Controller
- (PCI) 0xFFFFFFF1 (-15) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF2 (-14) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF3 (-13) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF4 (-12) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF5 (-11) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF6 (-10) Intel(R) I211 Gigabit Network Connection
- (PCI) 0xFFFFFFF7 (-9) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFF8 (-8) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFF9 (-7) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFFA (-6) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFFB (-5) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFFC (-4) Intel(R) I211 Gigabit Network Connection #2
- (PCI) 0xFFFFFFFD (-3) Intel(R) USB 3.0 eXtensible Host Controller
- (PCI) 0xFFFFFFFE (-2) Intel(R) Atom(TM) Processor E3800 Series/Intel(R) Celeron(R) Processor N2920/J1900

Appendix C

Electrical Specifications for I/O Ports

C.1 Electrical Specifications for I/O Ports

I/O	Reference	Signal Name	Rate Output
Backlight Brightness Control Connector	CN19	+VCC_LVDS_BKLT	+5V/0.5 or +12V/0.5
Iternal LVDS Connector	CN25	VCC	+3.3V/1A or +5V/1A
HDMI Connector	CN1	+5V	+5V/1A
USB3.0 Connector	USB3	+5V	+5V/1Aer channel)
mSATA Connector	PCIE1_A1	+3.3VSB +1.5V	+3.3V/1.1A +1.5V/0.375A
COM1 RS232/422/485 Connector	CN17	+5V/+12V	+5V/0.5A or +12V/0.5A
COM2 RS232/422/485 Connector	CN4	+5V/+12V	+5V/0.5A or +12V/0.5A
USB2.0 Connector	USB1	+5V	+5V/0.5A~1Aer channel)
USB2.0 Connector	USB2	+5V	+5V/0.5A~1Aer channel)
USB2.0 Connector	USB3	+5V	+5V/0.5A~1Aer channel)

Appendix D

Digital I/O Ports

D.1 DI/O Programming

The BOXER-6403WT utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

(1) Enter the MB PnP Mode

(2) Modify the data of configuration registers

(3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

D.2 Digital I/O Register

Table 2 : SuperIO relative register table		
	Default Value	Note
Index	0x2E	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0xA2(Note4)	0(Note5)		GPIO50
DIO-2 Pin Status	0x06(Note6)	0xA2(Note7)	1(Note8)		GPIO51
DIO-3 Pin Status	0x06(Note9)	0xA2(Note10)	2(Note11)		GPIO52
DIO-4 Pin Status	0x06(Note12)	0xA2(Note13)	3(Note14)		GPIO53
DIO-5 Pin Status	0x06(Note15)	0xA2(Note16)	4(Note17)		GPIO54
DIO-5 Pin Status	0x06(Note18)	0xA2(Note19)	5(Note20)		GPIO55

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note21)	0xA1(Note22)	0(Note23)	(Note24)	GPIO50
DIO-2 Output Data	0x06(Note25)	0xA1(Note26)	1(Note27)	(Note28)	GPIO51
DIO-3 Output Data	0x06(Note29)	0xA1(Note30)	2(Note31)	(Note32)	GPIO52
DIO-4 Output Data	0x06(Note33)	0xA1(Note34)	3(Note35)	(Note36)	GPIO53
DIO-5 Output Data	0x06(Note37)	0xA1(Note38)	4(Note39)	(Note40)	GPIO54
DIO-5 Output Data	0x06(Note41)	0xA1(Note42)	4(Note43)	(Note44)	GPIO55

D.3 Digital I/O Sample Program

```
********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN    // This parameter is represented from Note3
#define byte   DInput1Reg    // This parameter is represented from Note4
#define byte   DInput1Bit    // This parameter is represented from Note5
#define byte   DInput2LDN    // This parameter is represented from Note6
#define byte   DInput2Reg    // This parameter is represented from Note7
#define byte   DInput2Bit    // This parameter is represented from Note8
#define byte   DInput3LDN    // This parameter is represented from Note9
#define byte   DInput3Reg    // This parameter is represented from Note10
#define byte   DInput3Bit    // This parameter is represented from Note11
#define byte   DInput4LDN    // This parameter is represented from Note12
#define byte   DInput4Reg    // This parameter is represented from Note13
#define byte   DInput4Bit    // This parameter is represented from Note14
#define byte   DInput5LDN    // This parameter is represented from Note15
#define byte   DInput5Reg    // This parameter is represented from Note16
#define byte   DInput5Bit    // This parameter is represented from Note17
#define byte   DInput6LDN    // This parameter is represented from Note18
#define byte   DInput6Reg    // This parameter is represented from Note19
#define byte   DInput6Bit    // This parameter is represented from Note20
********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note21
#define byte   DOutput1Reg   // This parameter is represented from Note22
#define byte   DOutput1Bit   // This parameter is represented from Note23
#define byte   DOutput1Val   // This parameter is represented from Note24
#define byte   DOutput2LDN   // This parameter is represented from Note25
#define byte   DOutput2Reg   // This parameter is represented from Note26
#define byte   DOutput2Bit   // This parameter is represented from Note27
#define byte   DOutput2Val   // This parameter is represented from Note28
#define byte   DOutput3LDN   // This parameter is represented from Note29
#define byte   DOutput3Reg   // This parameter is represented from Note30
#define byte   DOutput3Bit   // This parameter is represented from Note31
#define byte   DOutput3Val   // This parameter is represented from Note32
#define byte   DOutput4LDN   // This parameter is represented from Note33
#define byte   DOutput4Reg   // This parameter is represented from Note34
#define byte   DOutput4Bit   // This parameter is represented from Note35
#define byte   DOutput4Val   // This parameter is represented from Note36
#define byte   DOutput5LDN   // This parameter is represented from Note37
#define byte   DOutput5Reg   // This parameter is represented from Note38
#define byte   DOutput5Bit   // This parameter is represented from Note39
#define byte   DOutput5Val   // This parameter is represented from Note40
#define byte   DOutput6LDN   // This parameter is represented from Note41
#define byte   DOutput6Reg   // This parameter is represented from Note42
#define byte   DOutput6Bit   // This parameter is represented from Note43
#define byte   DOutput6Val   // This parameter is represented from Note44
*********************************************************************************
```

```
*********************************************************************************
VOID   Main(){
       Boolean PinStatus ;

       // Procedure : AaeonReadPinStatus
       // Input :
       //      Example, Read Digital I/O Pin 3 status
        // Output :
        //     InputStatus :
        //              0: Digital I/O Pin level is low
        //              1: Digital I/O Pin level is High
       PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

       // Procedure : AaeonSetOutputLevel
       // Input :
       //      Example, Set Digital I/O Pin 6 level
       AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*********************************************************************************
```

```
**************************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
**************************************************************************************
```

```
*****************************************************************************
VOID    SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID    SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID    SIOSelectLDN(byte LDN){
         IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID    SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID    SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
         IOWriteByte(SIOData, Value);
         SIOExitMBPnPMode();
}
*****************************************************************************
```

```
*****************************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************************
```